A Compact Bias and Gain Control Solution for Avalanche Photodiodes

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***Abstract*—An integrable solution for stable bias control of avalanche photodiodes up to 30 V is presented. This circuit enables gain control to an accuracy of 3% for values of multiplication gain up to 100.**

I. Introduction

The biasing of avalanche photodiodes (APDs) requires higher voltages than are available in the electronic circuitry used in most applications. This typically means using a dedicated power supply to bias the APD, or using some DC-DC conversion techniques to achieve the desired bias voltage from a standard CMOS or TTL voltage rail. An alternative to these solutions is to use a charge pump to provide the bias voltage for the APD, where the charge pump operates from the available V_{dd} voltage rail. The gain or multiplication factor for photo-generated carriers is a function of the reverse bias voltage and so it is essential that the bias is stabilised to maintain a predictable gain. The multiplication gain can be approximated by the equation:

$$M_{ph} = \frac{I_M}{I_P} \tag{1}$$

Where I_M and I_P are the multiplied and unmultiplied photocurrent of the APD. The precise control of the bias voltage and, by extension, the multiplication gain ensures accurate performance for critical applications such as those in nuclear medicine [1]. One technique to control the gain requires the use of two matched APDs where one is biased at unitary gain (unmultiplied) and the other one is biased at a high gain (multiplied) mode [2]. Since the two matched APDs have near identical performance, the gain is simply the ratio of the currents flowing in the two APDs.

This paper describes a bias and gain control circuit for planar APDs which are typically designed with a breakdown voltage less than 30 V. The circuit uses the two matched APDs approach to set the multiplication gain. A charge pump is used to provide the bias voltage for the high gain APD whose gain or multiplication factor is set by a gain control circuit. The whole circuit is sourced from a 5 V power supply and allows the end user to specify the multiplication gain and have it controlled accurately (within 3%) by the circuit.

II. Circuit Description

Fig. 1 shows the schematic of the proposed circuit. In the circuit, a charge pump is used to generate the high (approaching 30 V) bias voltage for photodiode APD2 to generate a multiplied current, I_M. The other photodiode APD1 is biased at 5 V to give an unmultiplied current, I_P. In the gain control circuit, an op-amp and an NMOS-transistor are used to sense the voltage feedback from both photodiodes and control the bias voltage from the charge pump to adjust the gain or multiplication factor of APD2.

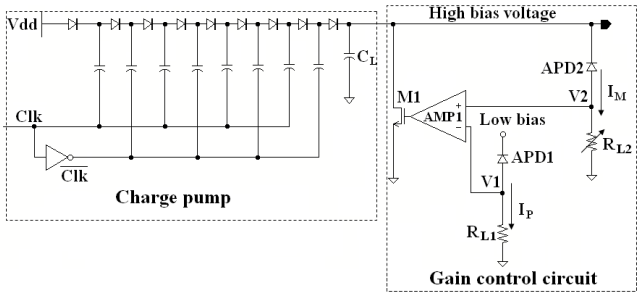

Fig. 1. Schematic of the proposed circuit

The charge pump used in Fig. 1 is a Dickson pump circuit [3]. An inverter is used to invert the phase of the input clocks. The neighbouring pumping capacitors are connected to these two inverse clocks. Through every stage, the positive charge is transferred by the diodes and pumping clocks to the output. At the output, a high voltage is obtained to bias APD2. With the low and high bias voltages, the unmultiplied and multiplied currents are generated in APD1 and APD2 and flow through the load resistors R_{L1} and R_{L2}. Voltages V1 and V2 can be seen at the anode of both photodiodes. V1 is connected to the inverting input of an op-amp, Amp1 and V2 is connected to the non-inverting input of Amp1. If V2 exceeds V1, the op-amp generates an output voltage proportional to the difference between V2 and V1 and the NMOS-transistor M1 will be biased to divide the output current. The bias voltage of APD2 will be decreased and V2 will decrease. If V2 falls below V1, M1 will be turned off, the bias voltage of APD2 can be continuously charged up and V2 will increase. In this way, V2 can be set equal to V1 which makes the multiplication gain in APD2 equal to the ratio of R_{L1} and R_{L2}. When R_{L1} is fixed, by setting the value of the load resistor R_{L2}, the gain of APD2 can be altered.

III. Simulation Results

An avalanche photodiode model shown in Fig. 2(a) is used for simulation. In the model, diode D1 accounts for the forward conduction. R1, R2 and R3 represent the internal resistance when the APD is reverse biased far from, near and above the breakdown voltage which are set to 3 MΩ, 25 kΩ and 200 Ω repectively. The voltage sources V1 (set to 23 V) and the diode D2 model the rapid gain increase that occurs when the APD is biased close to its breakdown voltage. V2 (set to 26 V) and D3 model the reverse breakdown voltage to about 28 V. Fig. 2(b) shows the simulation result of this model with a 10 kΩ load resistor when the reverse bias is varied from 0 to 35 V, demonstrating an approximate I-V characteristic for a planar APD with increasing gain approaching breakdown.

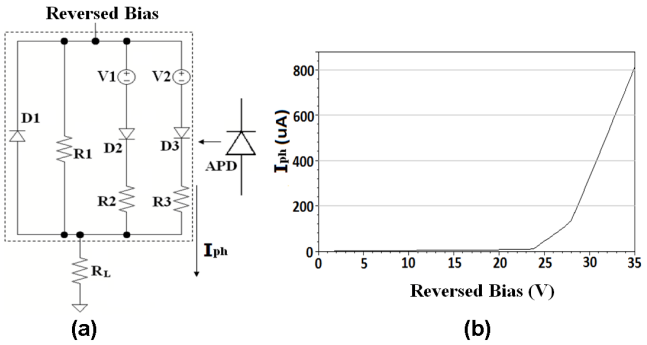

Fig. 2. APD model and its simulation result

The simulations of the proposed circuit were completed using the L-foundry 0.15 μm CMOS process in the Cadence design environment. An 8-stage charge pump is used with the pumping capacitors and load capacitor set to 20 pF and 1 nF, respectively. The clock frequency is 50 MHz with V_{dd} = V_{clk} = 5 V. APD1 is biased at V_{dd} to give a unit gain and R_{L1} is set to 500 kΩ. Fig. 3 shows the gain and the bias voltage of APD2 when its gain is set to 100 (R_{L2} = 5 kΩ). As can be seen from Fig. 3, the op-amp adjusts the bias voltage according to the feedback from the two photodiodes and control the gain precisely.

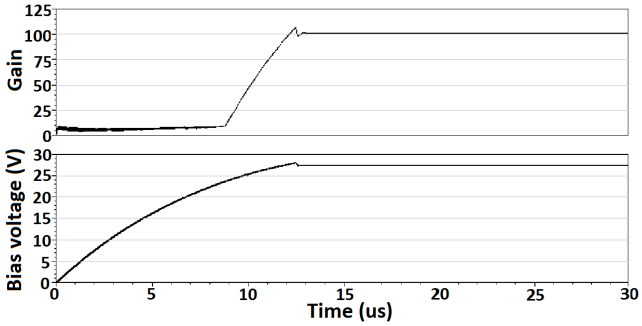

Fig. 3. Gain and the bias voltage of APD2 when its gain is set to 100

Fig. 4 describes the gain in APD2 for different values of R_{L2}. The resolution of R_{L2} here is set to 1 kΩ. A high precision variable resistor can be used to achieve a higher resolution in R_{L2} (e.g. a 256 position digital 10 kΩ potentiometer gives a resistance resolution of 39 Ω) that facilitates more accurate gain setting and control.

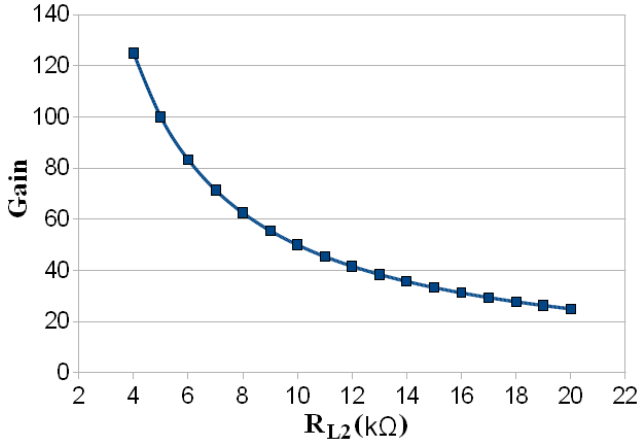

Fig. 4. Gains in APD2 with different values of R_{L2}

IV. Conclusions

A bias and gain control circuit for planar APDs is presented. The circuit can provide the required bias voltage to achieve high gain in the APD as well as stabilising the user-set multiplication gain. Simulation results show that the gain of APD can be controlled to within 3% of the value set by varying the value of its load resistor. The circuit presented is integrable as a single chip application specific integrated circuit (ASIC) and can provide a single package solution for bias and gain control of APDs for a variety of demanding applications.

V. Acknowledgments

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References

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