Design of a hold-off time control circuit for Geiger-mode avalanche photodiodes

Shijie Deng and Alan P. Morrison

***Abstract*—A high-resolution hold-off time control circuit for Geiger-mode avalanche photodiodes (GM-APDs) that enables linear changes to the hold-off time from several nanoseconds to microseconds is presented. The resolution of the hold-off time can be varied from nanoseconds to tens of nanoseconds with a range up to microseconds to cater for a variety of GM-APDs. This circuit allows setting of the optimal '*afterpulse-free*' hold-off time for any GM-APD through digital inputs or additional signal processing circuitry. With this circuit, the APD is automatically reset following the end of the hold-off period that further simplifies the end-user's control. A layout of this circuit is designed using a conventional 0.15 µm complementary metal oxide semiconductor (CMOS) process, resulting a area of 95 µm × 55 µm which makes it suitable for use with APD arrays.**

***Index Terms*—Geiger-mode avalanche photodiodes (GM-APD), Afterpulsing, Quench circuit, Hold-off time.**

I. INTRODUCTION

Geiger-mode avalanche photodiodes (GM-APD) are commonly used where high sensitivity low-light intensity detection is required. Typical applications include DNA sequencing, quantum key distribution, LIDAR and medical imaging. In the Geiger-mode, the APD is biased above its breakdown voltage. When a photon is absorbed by the APD an avalanche event is triggered and the event is counted. After every avalanche event, some residual charge is stored in traps in the APD. The release of this stored charge when the GM-APD is active often leads to an avalanche current correlated to a previous avalanche event, but not related to a new photon arrival. This is an unwanted source of noise and is typically termed "afterpulsing". Waiting for all the trapped charge to dissipate before resetting the GM-APD can reduce the amount of afterpulsing. This is generally achieved using an appropriate control circuit that quenches the APD avalanche current by lowering the bias voltage below the breakdown voltage. The APD is kept in the OFF state for fixed period of time, called the "hold-off" time, before resetting the device to its original bias voltage to await the next avalanche event. If the hold-off time is less than the mean trap lifetime then afterpulsing will significantly affect the photon counting statistics. If the hold-off time is much greater than the mean trap lifetime then the counting rate will be limited and the validity of the counting statistics will also be affected. The hold-off time must be set according to the nature and density of the traps present in a particular device to minimize the significance of afterpulsing.

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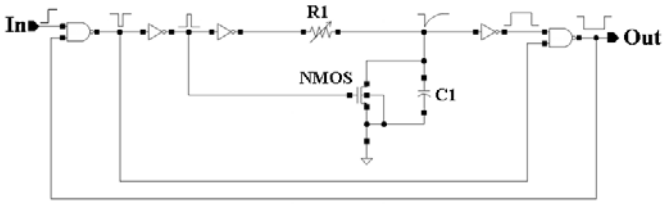

Fig. 1. Schematic of the monostable circuit.

The most popular method used for setting hold-off time is uses monostables which have been widely applied in active quench and reset circuits [1], [2], [3], that are still reported recently [4], [5]. Fig. 1 shows the schematic of a monostable. An RC delay configuration is used in the circuit. By setting the value of the variable resistor, R1, the RC delay time can be varied and a user-set pulse-width can be created for setting the hold-off time. With the monostables, a wide range of hold-off times (from nanoseconds to microseconds) can be generated. However it is difficult to accurately and digitally adjust the hold-off time.

In [6], the delay line technique is used to set the hold-off time. A diagram of the delay line technique used in [6] is shown in Fig. 2. The rising-edge ramp generators in the circuit are current sources that are connected through capacitors to ground. 16 discrete current mirrors were used with each having an individual capacitor to generate 16 predefined delays. The delay can be selected by the end-user using a 4–16 decoder with inputs h3 to h0. The outputs of the 16 SR-latches are connected to a 16–1 multiplexor and the same inputs h3 to h0 are used to determine the SR-latch output sent to the next stage. This output is then connected to a logic stage to create one of the selected 16 predefined hold-off time pulse widths that are determined by the size of the capacitors C1–C16 and the current flowing through them. This technique makes it easier to select an appropriate hold-off time, but it uses several capacitors, which leads to an increased layout area. In addition, there are only a finite number

of hold-off times available, thus requiring an increased layout area to obtain additional hold-off times. An additional disadvantage to all the traditional techniques for setting the hold-off time is the requirement for an additional monostable or pulse generator to reset the APD, which further adds to the complexity of the control circuit.

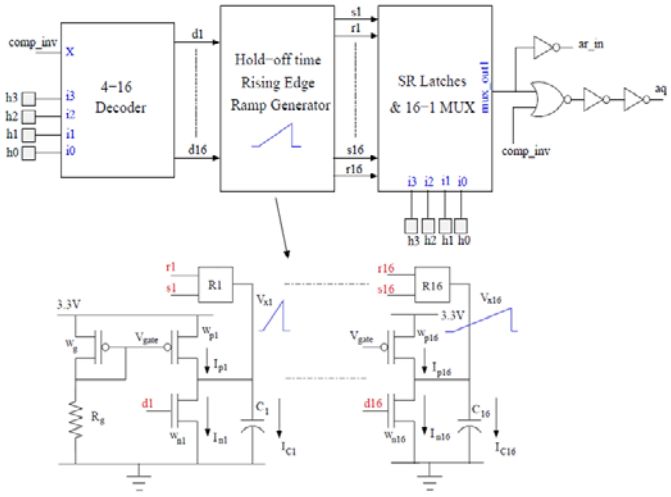

Fig. 2. Diagram of delay line technique from [6].

In this paper, we present a high-resolution hold-off time control circuit that allows linear setting of the hold-off time from several nanoseconds to microseconds. Its small size, reduced complexity and automatic reset make it attractive for use with a wide variety of GM-APD architectures. The step-size of the hold-off time can be altered from several nanoseconds to dozens of nanoseconds by varying the period of the external clock. This clock controls a counter through which the hold-off time can be varied linearly. This circuit, shown in Fig. 3, will reset the APD automatically at the end of the hold-off period without the requirement for an additional monostable or delay line circuit.

II. Circuit Description

Fig. 3 shows the block diagram of the high-resolution hold-off time control circuit. The non-inverting input of the comparator is connected to the anode of the APD that is biased at a voltage between the avalanche breakdown voltage, V_{break}, to (V_{break} +V_{dd}). The comparator is used to sense the avalanche current at the anode of the APD which also has an inverse output, $\overline{compo}$, that is connected to an external bond pad for readout. One PMOS and one NMOS transistor are used as the switches for quenching or resetting the APD. An external clock signal provides the counting clock during the hold-off period and a counter is used to control the hold-off time.

Initially, when there is no avalanche current, *compo* is low, the external clock is blocked and the 6-bit counter is reset to 0 ("000000"), both PMOS and NMOS transistors are turned off. When an avalanche event happens in the APD, current flows through the load resistor, R_L, and the voltage increases at the anode of APD. The comparator senses the voltage rise and *compo* goes from low to high. *Qp* goes low to turn on the PMOS transistor and the anode of the APD is connected to V_{dd} for quenching. Meanwhile, the counter is receiving clocks from the external clock (*Clk_in*).

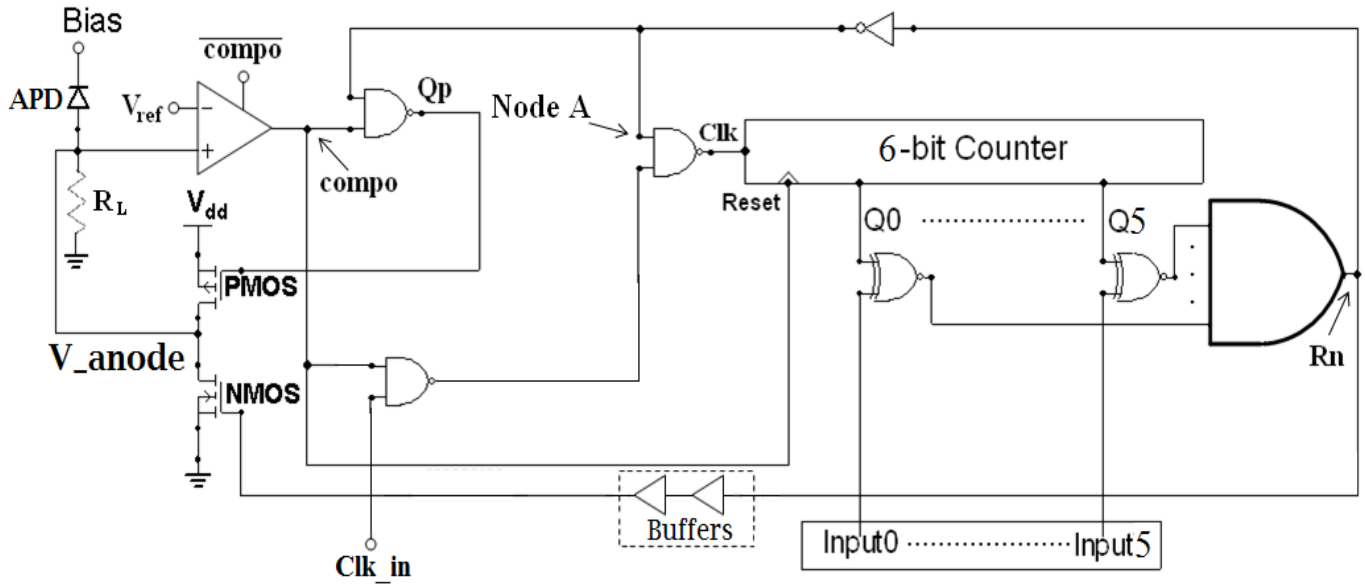

Fig. 3. Block diagram of the high-resolution hold-off time control circuit.

The counter used here is a 6-bit synchronous binary counter which consists of 6 J-K flip-flops with the clock signal connected to the clock input of every flip-flop and the J and K inputs are tied together, see Fig. 4. The J and K inputs of the first flip-flop are connected to V_{dd}; the J and K inputs of the other flip-flops are connected to the output *Q* of each front end.

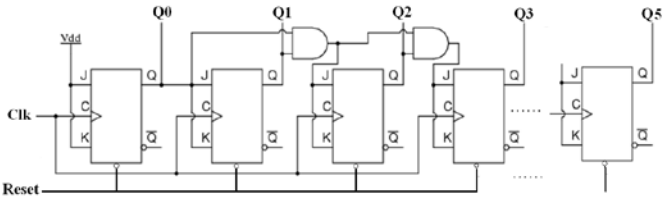

Fig. 4. Schematic of the 6-bit synchronous binary counter used.

When the reset signal *compo* is high, the counter receives clocks from *Clk_in* and counts upwards from 0 ("000000") to 63 ("111111"). Each output of the counter is connected to one input of an XNOR gate. The other input of the XNOR is connected to an external input (controlled by end user). When the output of the counter is equal to the external inputs, all the outputs of the XNOR gates go to logic "1" (high). Then *Rn* goes high which makes *Qp* go high to stop the hold-off process and turn on the NMOS transistor to reset the APD (two buffers are used here to make sure the reset process starts after the hold-off process is finished). At this time, the '*Node A*' goes low to stop the clock to the counter and the counter is stopped. This then makes *Rn* remain high for resetting. When the anode of the APD is reset back to ground, *compo* is low, the *Clk_in* is blocked again and the counter is reset to 0 ("000000"). Now the outputs of the counter do not match the external inputs, *Rn* goes low and the NMOS transistor is turned off to complete the reset process. The APD is then ready to detect the next photon. By setting the external inputs, the counting number can be determined and the hold-off time can be altered. The step resolution is decided by the counting speed, which depends on the period of the external clock *Clk_in*.

III. Layout and Simulations

The layout of the proposed circuit was completed using L-Foundry 0.15 µm CMOS process and is illustrated in Fig.5. The overall chip dimension is about 700 µm × 700 µm which mostly occupied by the bond pads. The dimensions of IC core (without bond pads) are 95 µm × 55 µm. In the layout, the counter and the amplifier occupy 27% and 33% of the IC core's area; other control logic occupies the rest of the area. All the simulations reported are post-layout simulations.

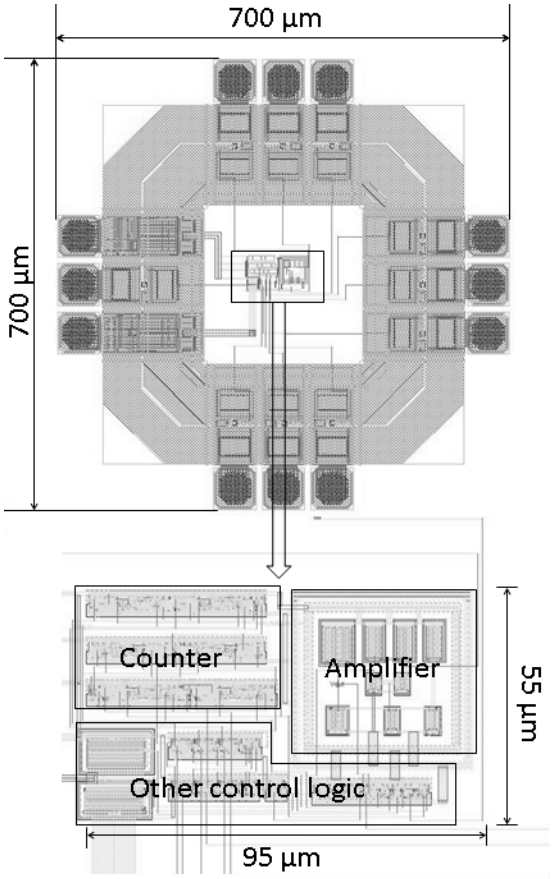

Fig. 5. Layout of the proposed circuit.

For circuit simulations, a linear model of the GM-APD is used, as illustrated in Fig. 6 [7]. V_b is a voltage source that represents the breakdown voltage, which is set at 27 V. The bias voltage is set to 30 V. R_d is the internal resistance, which is set to 250 Ω. Cd, is the junction capacitance, which is set to 2 pF. The simulations were run in the Cadence design environment with V_{dd} = 3.3 V.

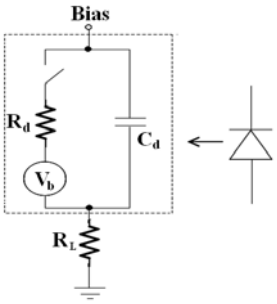

Fig. 6. Simulation model of the GM-APD.

Fig. 7 shows an example of the circuit operation when the external inputs are set to 30 ("011110"). The period of external clocks is set to 2 ns. As can be seen from the figure, at 5 ns when a photon absorbed, the comparator senses the voltage change from the anode of the APD and *Qp* goes low for quenching. Meanwhile, the external clock is not blocked and providing the clocks to the counter. The 6-bit counter counts upwards from 0 ("000000") at a rate set by the external clocks (here is set to 2 ns). When the outputs of the counter match the external inputs, which in this case are set to 30 ("011110"), *Rn* goes high which makes *Qp* go high to stop the hold-off process and turn on the NMOS transistor to reset the APD. At this time, the clocks to the counter are blocked and the counter is stopped thereby making *Rn* high for resetting the APD. When the anode of the APD is set back to ground, the counter is reset to 0 ("000000") and *Rn* goes low to stop the reset process. In this way, with the external inputs of 30 ("011110"), the hold-off time is set to around 60 ns. Another example of the circuit operation when the hold-off time is set to 108 ns is illustrated in Fig. 8. Results show the accurate control of the hold-off time using external digital inputs.

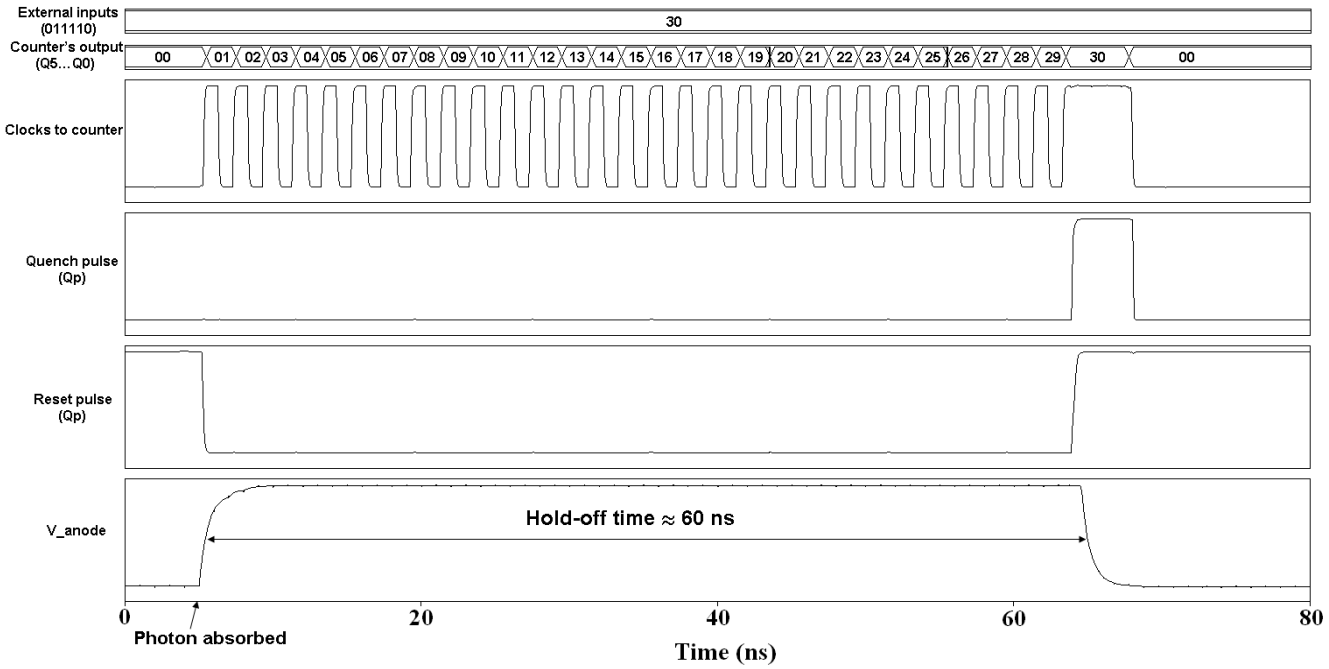

Fig. 7. Example of the circuit operation when the external inputs are set to 30 ("011110").

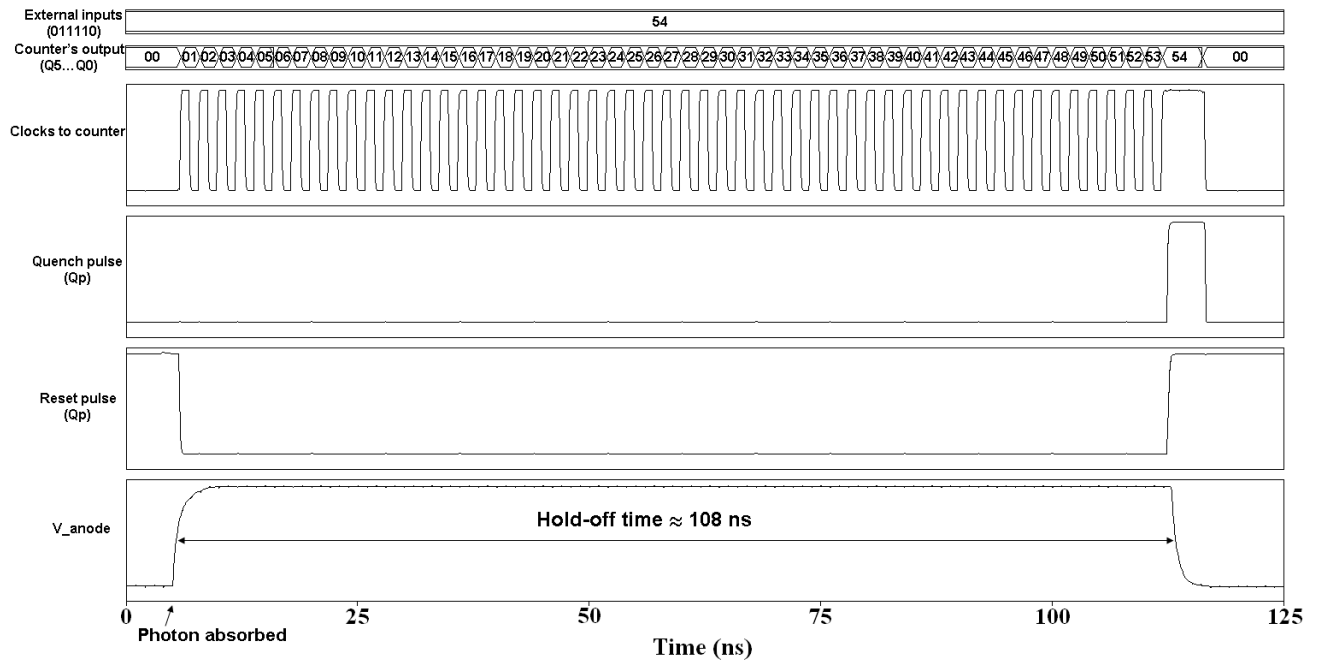

Fig. 8. Example of the circuit operation when the external inputs are set to 54 ("110110").

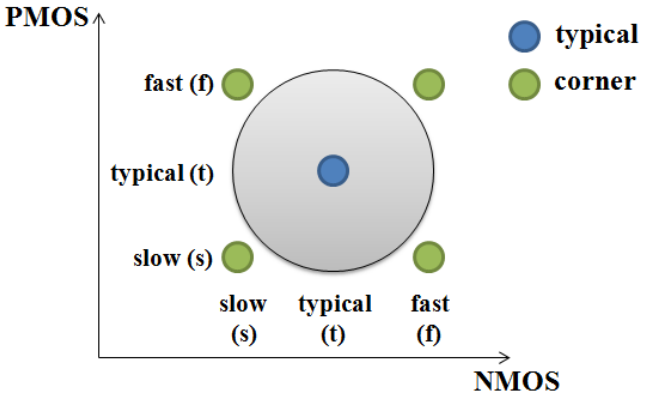

Fig. 9. Simulation models in corner analysis

To test the stability of the circuit, corner analysis was performed. NMOS and PMOS transistors were set to different models in the simulations, see Fig. 9. In Fig.10, results of the corner analysis are illustrated. Corners ff, fs, tt, sf and ss represent (fast NMOS, fast PMOS), (fast NMOS, slow PMOS), (typical NMOS and PMOS), (slow NMOS, fast PMOS) and (slow NMOS, slow PMOS) respectively. As can be seen from the figure, the variations of the hold-off time for different cases are less than 1 ns, demonstrating a stable performance of the proposed circuit in the corner analysis.

Fig. 11 shows the simulation results when the power supply drift is taken into account. In the simulations, V_{dd} was varied from 3.0 V to 3.6 V with a step of 0.1 V. Results show that the circuit functions correctly and the effect of the power supply drift is the potential variations at the GM-APD's anode (V_anode) when it is kept in OFF state (quenching voltage). When biasing the GM-APD, the excess voltage must be set less than the quenching voltage in the worst case so that the bias of the GM-APD can be set lower than its breakdown voltage during the hold-off process.

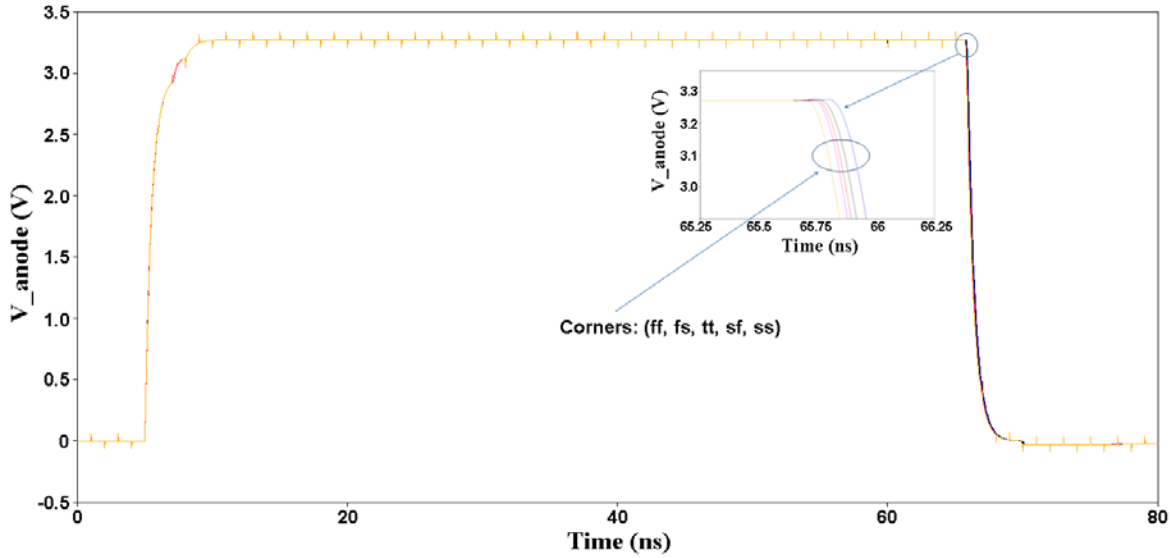

Fig. 10. Corner analysis results.

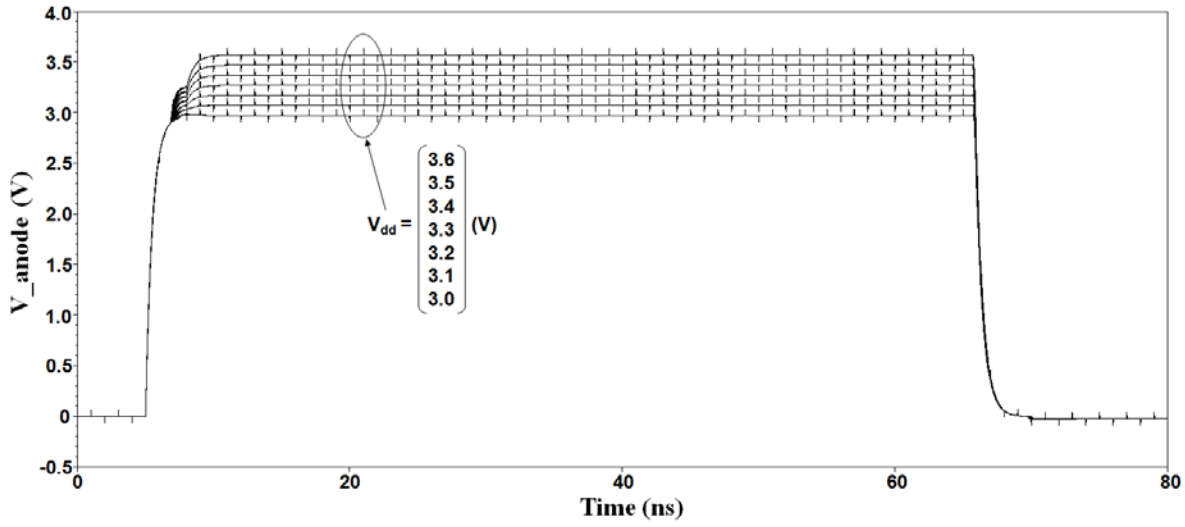

Fig. 11. Simulation results with power supply drift.

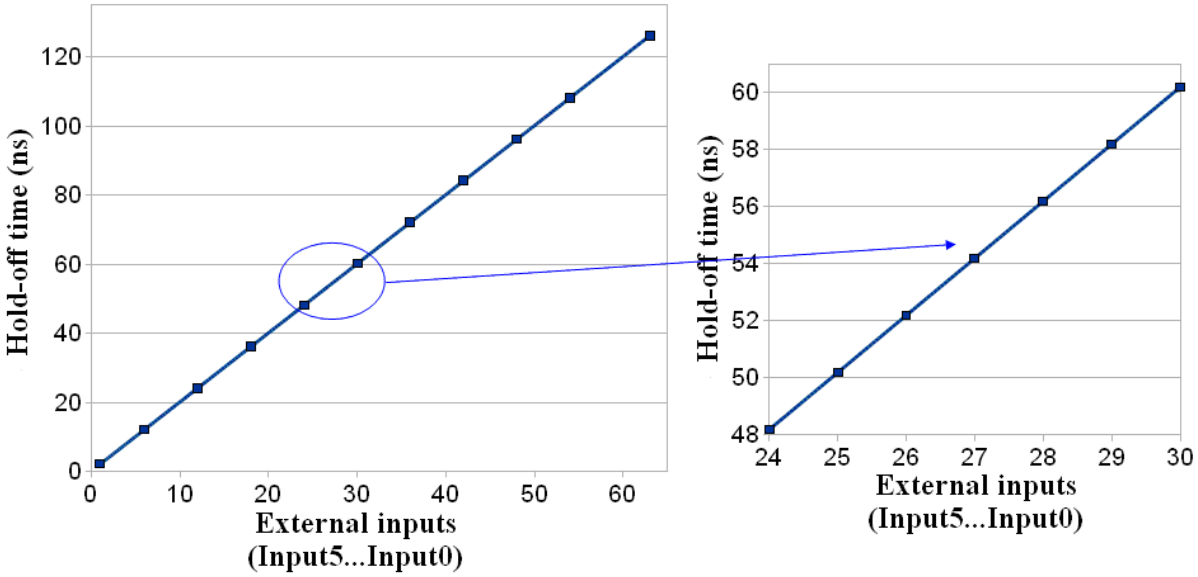

Fig. 12. External input codes versus resultant hold-off time when the step resolution is set to 2 ns.

Fig. 12 shows the simulation results of varying the external input codes versus the resultant hold-off time. It shows when the input code increases from 1 ("000001") to 63 ("111111") the hold-off time linearly increases to more than 120 ns with a step resolution of about 2 ns.

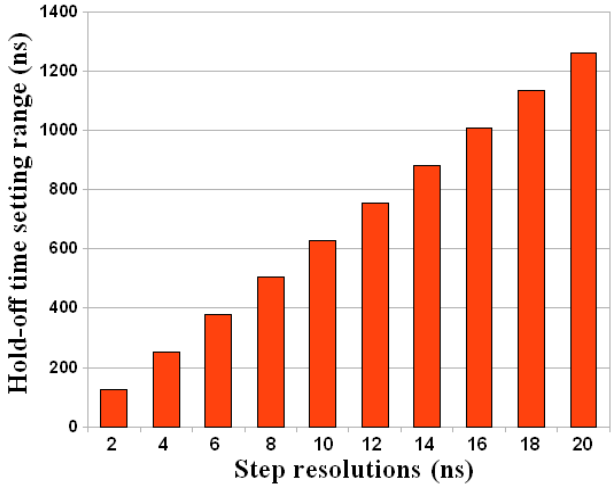

Fig. 13. Setting range of the hold-off time for different step resolutions.

In Fig. 13, the setting range of the hold-off time for different step resolutions is demonstrated. As can be seen from the figure, when the step resolution is varied from 2 ns to 20 ns the range of the hold-off can be altered by more than a microsecond.

IV. Conclusion

A high-resolution hold-off time control circuit for Geiger-mode avalanche photodiodes is described in this paper. With this circuit, the hold-off time can be linearly varied from several nanoseconds to microseconds with a user-set resolution. The optimal '*afterpulse-free*' hold-off time for any GM-APD can be easily set through the circuit's digital inputs or via an additional signal processing circuit. A layout of this circuit was completed using a conventional CMOS process, resulting in a small layout area that makes it suitable for integration with arrays of GM-APDs. The circuit also incorporates a facility designed to reset the APD automatically at the end of the hold-off time that further simplifies the control for the end-user.

Acknowledgment

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