An integrable bias solution for avalanche photodiodes

S. Deng and A. P. Morrison

A bias circuit for avalanche photodiodes (APDs) based on a dual-rail charge pump configuration operating from a 5 V supply that is capable of supplying a bias voltage in excess of 50 V is presented. For shallow-junction planar APDs that operate between 25 V and 45 V this circuit is capable of delivering more that 50 mW of power, allowing avalanche currents in the mA range. The circuit design requires only 2 external load capacitors, while the rest of the circuit can be implemented as an application specific integrated circuit (ASIC) which makes the circuit highly integrable. The bias voltage can be accurately controlled and easily adjusted by the end user using the shunt regulator incorporated for voltage control.

Introduction: Avalanche photodiodes are used in wide range of low-light sensing applications such as astronomy, DNA sequencing, quantum key distribution, LIDAR and medical sensing. Planar APDs have been developed over a number of years by many organisations for low-light sensing applications requiring both linear, multiplicative and Geiger-mode operation [1], [2]. Typically these APDs are designed with a breakdown voltage less than 30 V. The difficulty that remains is the requirement to bias these devices at voltages in excess of the voltage requirements for the rest of the sensing system. Existing APD-based sensing solutions use external high-voltage supplies or a DC-DC converter chip with significant additional external circuits to bias the APD. There are also some commercially available chips on the market specifically designed for biasing APDs, such as [3], [4]. These chips,

however, require several external discrete components to function correctly, thereby limiting their usefulness in compact or integrated applications.

This paper describes an adjustable bias circuit that is capable of delivering more than 50 V with more than 50 mW output power in the bias range from 25 V to 45 V. The circuit uses a dual-rail charge pump (positive and negative charge pump) to generate the high bias voltage and includes shunt regulators to control the magnitude of the voltage. The circuit is designed using standard CMOS process design rules and requires only two external load capacitors. The combination of ASIC, APD and external capacitors can all be hybridly integrated in a single package to operate seamlessly from a 5 V supply, thereby taking the additional responsibility for biasing the APD from the end-user.

Circuit Description: An overview of the bias voltage circuit is shown in Fig. 1 and consists of two main parts: (i) A dual-rail charge pump which provides the high bias voltage for the load. (ii) Two shunt regulators which are used to control the output voltage for the positive and negative nodes of the load.

Fig. 2 shows the schematic of the dual-rail charge pump. The positive and negative charge pumps used in Fig. 2 are Dickson pump circuits [5]. The MOS transistors in the circuit are connected in diode fashion. The neighbouring pumping capacitors are connected to two inverse pumping clocks. NMOS is used for the positive charge pump to transfer the positive charge. PMOS is used for the negative charge pump to transfer the negative charge [6]. The charge is sourced from the system power supply, V_{dd} or $-V_{dd}$. Through every stage, the output voltage is increased or decreased by the pumping clock. At the output, a higher potential exceeding the magnitude of the system supply is obtained.

For maximizing output current, shunt regulators are needed to control the output of the charge pump. With the shunt regulator, the charge pump operates continuously. Fig. 3 shows the schematic of the shunt regulator. This regulator uses a MOS transistor (NMOS for positive output and PMOS for negative output) in parallel with the load and behaves functionally like a variable current divider to obtain load voltage regulation [7]. R1 and R2 are used to decrease the output voltage to a comparable level V_1. A two-stage op amp is used as the error amplifier. A power supply of V_{dd} and GND are used for amplifying the positive error, a power supply of GND and $-V_{dd}$ is used for amplifying the negative error. If V_1 exceeds the regulation level V_{ref}, the error amplifier generates an output voltage proportional to the difference between V_{ref} and V_1 and the MOS transistor will be biased to divide the output current. If the output falls below the regulation level, the MOS transistor will be turned off, and the output can be continuously charged up. In this way, V_1 can be set equal to V_{ref}. By setting the reference voltage V_{ref}, the output voltage can be altered.

Simulations: A 7-stage dual-rail charge pump with shunt regulators was designed. The pumping capacitors are 20 pF. The two load capacitors are 3 nF each and are the only external components required for this design. The simulations were completed using Austria Microsystem's 0.35 μm CMOS process running in the Cadence design environment. The clock frequency is 50 MHz with $V_{dd} = V_{clk} = 5$ V. Simulation results show that the bias voltage can be regulated accurately with a peak-peak ripple of 25 mV. Fig. 4 shows the maximum load current and output power for different bias voltages. From the simulations it is clear that the circuit is capable of meeting load current demands in excess of 1 mA at bias voltages up to 45 V.

Conclusions: This paper describes an adjustable bias circuit which can provide in excess of 50 V for biasing planar APDs. Simulations show the output bias voltage can be adjusted precisely and can sustain mA current output when operating

between 25 V and 45 V. This circuit can be hybrid integrated with the APD and 2 surface mount external capacitors in a single package (TO-can or Dual-in-line) which is very attractive for applications requiring a compact integrated APD device solution.

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References

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Figure captions:

Fig. 1 Block-diagram of overall bias circuit solution

Fig. 2 Schematic of Dual-rail Charge Pump

Fig. 3 Schematic of Shunt Regulator

Fig. 4 Simulation results of maximum load current and output power for different bias voltages

Figure 1

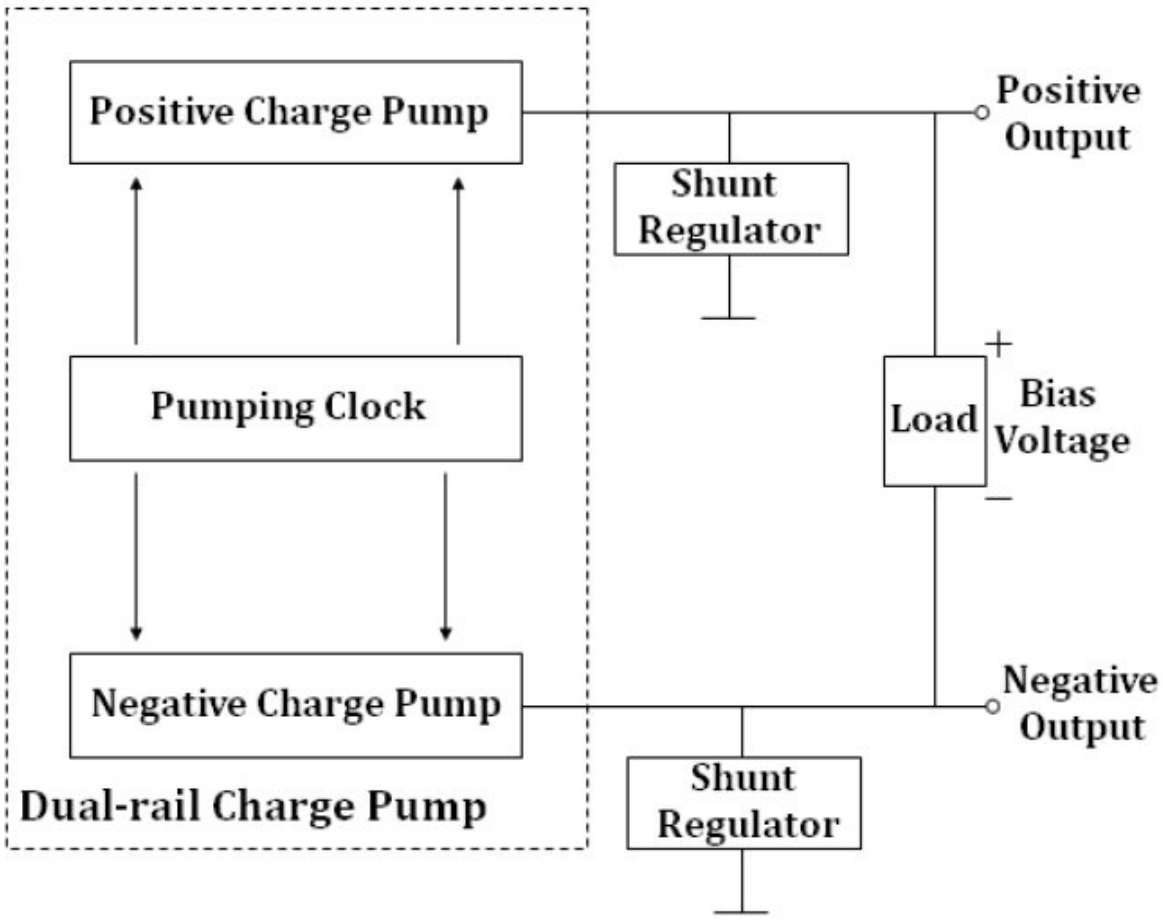

Positive Charge Pump
Positive Output
Shunt Regulator
Pumping Clock
Load
+
Bias Voltage
−
Negative Charge Pump
Negative Output
Shunt Regulator
Dual-rail Charge Pump

Figure 2

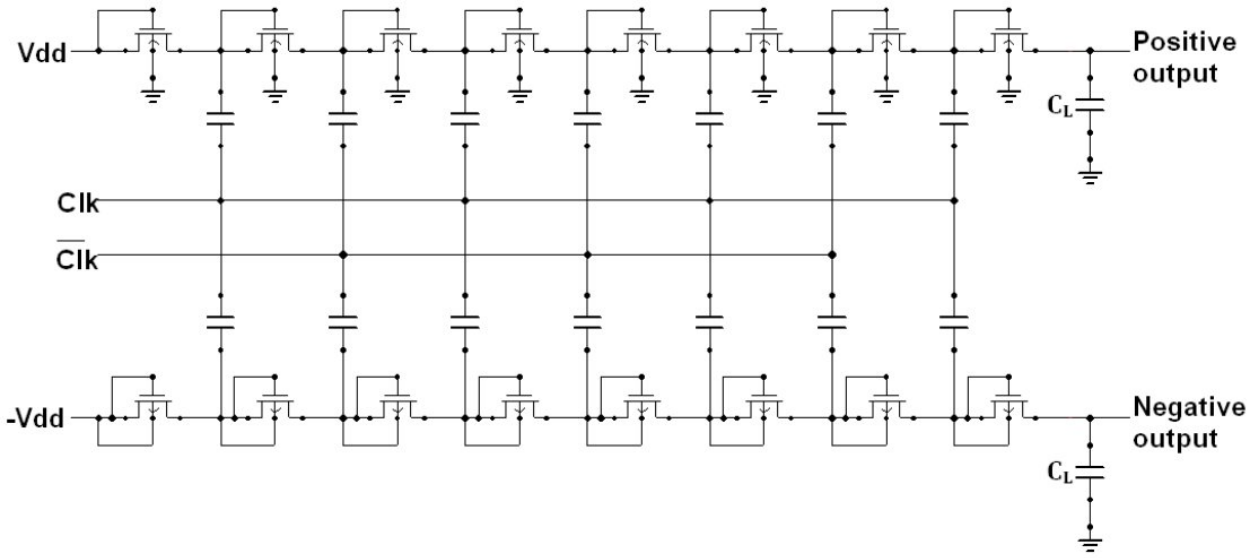

Vdd
Positive output
C_L
Clk
$\overline{Clk}$
-Vdd
Negative output
C_L

Figure 3

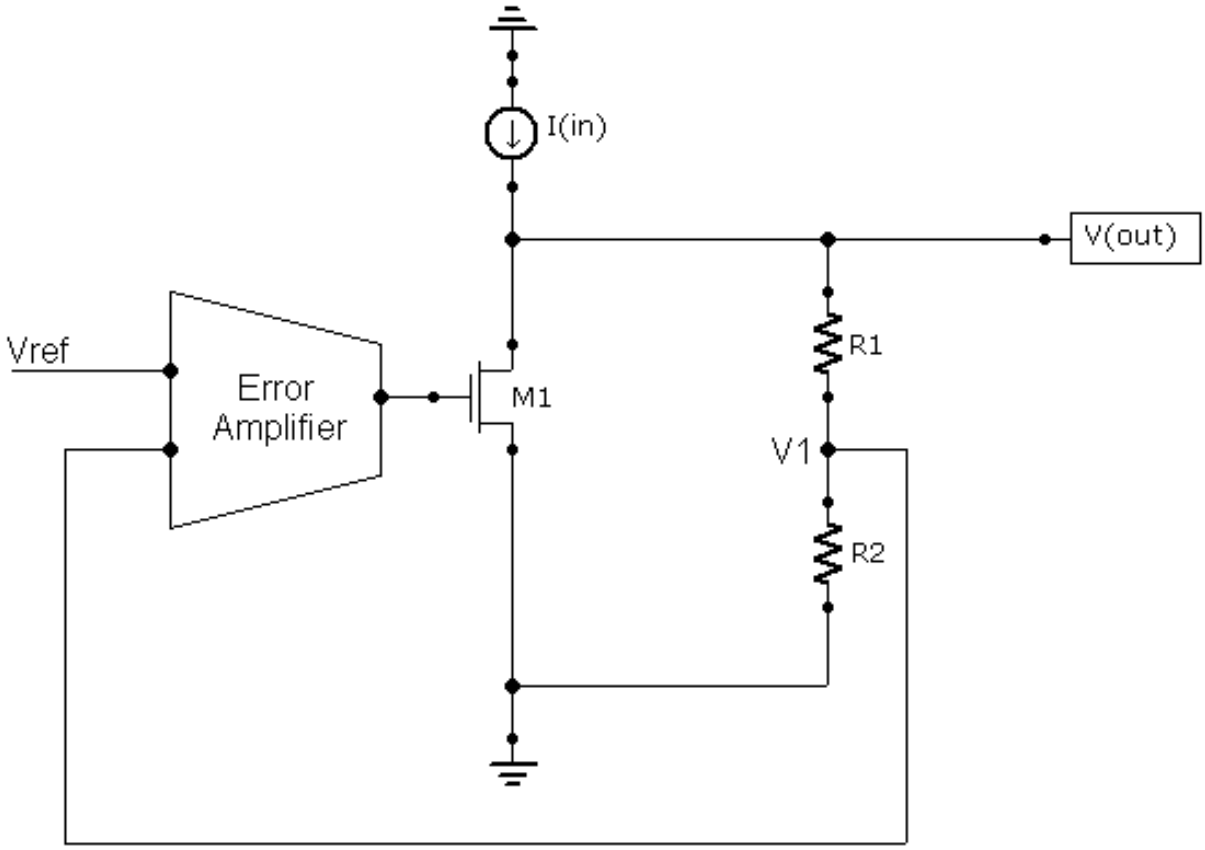
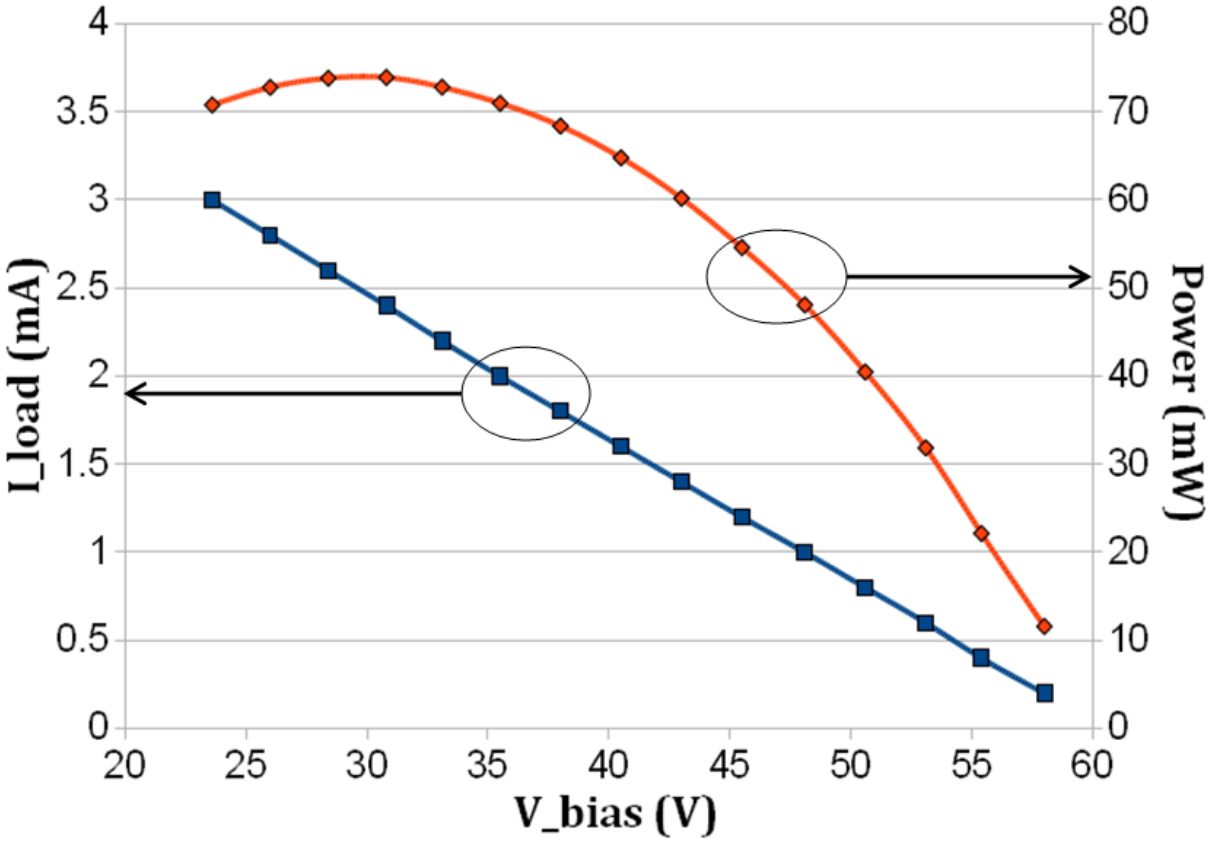


Figure 4


I_load (mA)
Power (mW)
V_bias (V)
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
80
20
25
30
35
40
45
50
55
60