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Local Secondary Control for Inverter-based Islanded Microgrids with Accurate Active-Power Sharing under High Load Conditions

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***Abstract*—Local secondary control has been successfully used to regulate the frequency of inverter-based islanded microgrids without using communications. In this scenario, noticeable steady-state deviations have been observed in active power sharing caused by the inherent clock drift of the digital processors that implement each inverter local control. This paper presents a control scheme that performs frequency regulation and improves the active power sharing under high load conditions, thus alleviating the impact of clock drifts in this situation. The study introduces a theoretical analysis that quantifies the steady-state deviations in active power sharing. It also includes a design procedure for the control parameters based on static and dynamic specifications. Experimental tests validate the expected features of the proposed control. The experimental setup is based on a laboratory microgrid equipped with three independent digital signal processors with different clock drifts.**

***Index Terms*—Inverter-based microgrids, islanded operation, frequency regulation, power sharing.**

I. Introduction

HIERARCHICAL control is widely used today to manage the operation of inverter-based islanded microgrids [1], [2]. This control policy is organized in several layers to meet different control objectives [3], [4]. The primary layer is responsible for the sharing of the load power. It is normally implemented using the well-known droop control method [5]. The secondary layer is responsible for the regulation of the microgrid frequency. Its purpose is to remove the frequency steady-state deviations introduced by the droop control method [5], [6]. The tertiary layer is responsible for the energy dispatching and power balance. Its target is to optimize operational costs and durability [7], [8].

Focusing on the use of the communication service, normally the primary layer is a control that uses only local measures while the tertiary layer is a communication-based control [8]. For the secondary layer, most of the control schemes use the communication service [9]-[14]. In centralized approaches, the secondary control is implemented in a central controller that calculates the corrective terms that compensate the frequency deviations and sends them to the inverters' control units [3], [9]. In distributed approaches, each local controller implements its own secondary layer using both local measures and data received from other controllers through the communication service. Distributed averaging and consensus are two examples of communication-based secondary control schemes [10], [11]. In both cases, the microgrid frequency is regulated by the cooperative action of the inverters [12], [13]. Droop-free distributed control is another communication-based control scheme for frequency regulation in microgrids [14]. This is an alternative implementation to the consensus algorithm in which the functions of the primary and secondary control are achieved without separating the control system in layers, thus flattering the hierarchical control structure. Both centralized and distributed control schemes based on communications have excellent performance. In fact, with these schemes, the power sharing and frequency regulation show insignificant steady-state errors.

However, in digital communication networks, messages suffer from delays and dropouts that can degrade the microgrid performance. This degradation has been reported in several studies, see for instance [15]-[18]. It is worth mentioning that the operation of the microgrid may become unstable when a certain percentage of dropouts is exceeded, e.g., see [18]. Even with these adverse effects, the communication service is today an important element in microgrids. But a tendency to reduce the use of communications in the control system of the microgrid is observed in some recent studies [19]-[23]. The idea is to implement several functionalities of the control system without data interchange between the local control units of the

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microgrid. This is inherently done in the primary layer by the droop control method. For the secondary layer, communication-less control schemes have been presented in [19]-[23]. Since they do not use the communication service, they are insensible to communication delays and dropouts. Moreover, with these control schemes, the security, confidentiality and integrity of the microgrid is improved due to the reduction of malicious cyberattacks [23]. The price to pay is a slight loss of quality in power sharing and frequency regulation, as reported in [20] and [21].

In addition to the communication constraints, another technological issue that affects the practical operation of inverter-based microgrids is the drift in the local controller clocks [24], [25]. Each inverter operates with its own digital processor and the clock used to generate the time signal of this processor differs from the time signals of the other processors due to the clock drifts. In the droop-based primary layer, the impact of clock drifts is nearly negligible, as shown in [25]. However, the effects in the secondary layer highly depend on the selected control algorithm. Using local integral controllers in the secondary layer, the steady-state operation of the microgrid tends to an unstable equilibrium point, as stated in [26]. Using the droop-free control scheme, the performance is good and the effects of clock drifts can be considered negligible when the control parameters are properly adjusted [27]. However, when a key control parameter is not carefully tuned, large errors in active power sharing appear. The local secondary control based on distributed low-pass filters (DLPF) analyzed in [28] exhibits a similar problem with power sharing. With this scheme, the difference in the active power supplied by the inverters is a constant value for all load conditions. Moreover, this value can be large in some circumstances, as discussed in detail in the next section. It is worth mentioning that the error in active power sharing represents a negative impact on the system performance during high load conditions. In this case, the active power supplied by the inverters is high and mismatches in power sharing may produce both excessive stress and poor thermal distribution in the inverters.

The source of the active power deviations is the different values of the line impedances when primary and secondary control layers are not implemented in the local control units, as shown in [18]. However, using the droop control in the primary layer, the different line impedances have no effect in power sharing, as demonstrated in [24] and [25]. The fact that the clock drifts cause active power deviations using different secondary control layers is revealed in [26]-[28]. In particular, in [27], it is verified experimentally that different clock drifts provoke different active power deviations.

Conversely, the effect of the clock drifts on the sharing of reactive power is negligible, as confirmed experimentally in [27]. The main reason for this is that: 1) the clock drifts cause a direct error only at the inverter operating frequencies (and indirectly at the active powers due to the coupling between frequency and active power through the droop-based control scheme) and 2) the coupling between active and reactive power through the power flow equations is low and, therefore, the errors in active power are not practically transferred to the reactive power. In view of this, the control schemes for voltage and reactive power are not included in this study. Interested readers can see [5] for a recent review of these control schemes.

This paper focuses on improving the performance of secondary control schemes that do not require communications for the control purposes. The local DLPF-based secondary control [20] is taken as a starting point for the study. The paper presents a new control algorithm that provides accurate active power sharing under high load conditions. And this feature is achieved even in real applications with the presence of different clock drifts in the digital signal processors implementing the local control. Thanks to this characteristic, the thermal load is distributed better along the system, which avoids the hot spots in the power inverters during high load conditions. In addition, the maximum injected currents coincide, which prevent excessive stress in the power switches and other passive components. For low load conditions, power sharing deviation is not a relevant problem since the current and power of the inverters are small and their differences will have no impact on the stress and thermal distribution of the inverters. From a theoretical point-of-view, the study includes a static analysis that quantifies the steady-state deviations in active power sharing. It also presents a design procedure for the control parameters including considerations based on static and dynamic specifications. Selected experimental tests validate the advantages and limitations of the proposed control scheme. The experimental tests were carried out in a laboratory microgrid equipped with three inverters driven by three digital signal processors, each one enabled with its own clock, thus reproducing real applications affected by distributed clock that inherently drift.

The rest of the paper is organized as follows. Section II presents the problem statement, including the description of the inverter-based microgrid and the practical limitations of the local DLPF-based secondary control. Section III proposes a control scheme that reduces the impact of clock drifts on the active power sharing under high load conditions. In addition, a theoretical study derives the particular features of the proposal using static and dynamic analytical tools. Section IV presents guidelines to design the parameters of the proposed control. Section V validates the theoretical results by experimental tests. Section VI presents a sensitivity analysis and a discussion on the results. Section VII concludes the study.

II. Problem Statement

This section presents the inverter-based islanded microgrid, reviews the standard local control scheme for the primary and secondary layers, and provides the problem formulation.

A. Inverter-based Islanded Microgrid

Fig. 1 shows a diagram of the laboratory three-phase microgrid considered in this study. Table I lists the nominal values of its components. This microgrid is tested to experimentally validate the features of the control proposed in next section.

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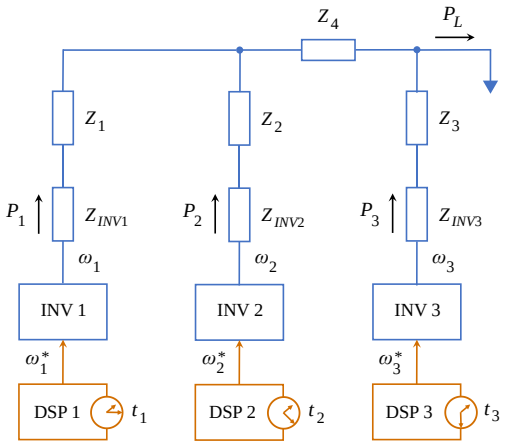

Fig. 1. Diagram of the inverter-based islanded microgrid.

TABLE I
NOMINAL VALUES OF THE MICROGRID COMPONENTS

Symbol	Quantity	Nominal value
n	Number of inverters	3
P_i^{max}	Maximum power of inverters	910 W
P_L^{max}	Maximum load power	2730 W
V_i	Phase voltage	110 Vrms
ω_0	Angular frequency	2π 60 rad/s
$Z_{INV.i}$	Output impedance of inverters	0 + j 3.77 Ω
Z_1	Line impedance 1	0.50 + j 1.13 Ω
Z_2	Line impedance 2	0.50 + j 0.38 Ω
Z_3	Line impedance 3	1.13 + j 0.23 Ω
Z_4	Line impedance 4	0 + j 0.30 Ω
d_1	Clock drift rate in DSP1	-1.69 ppm
d_2	Clock drift rate in DSP2	0
d_3	Clock drift rate in DSP3	2.81 ppm

The microgrid consists of three power inverters (INV i), which generate its internal current and voltage waveforms at the frequency ω_i and deliver the active power P_i to the load (P_L). The impedances Z_{INVi} and Z_i model the output impedances of the inverters and the line impedances of the distribution cables, respectively.

A digital signal processor (DSP i) controls the output of each inverter using only local measurements. The three processors have autonomous clocks that generate time t_i that differs between inverters ($t_i \neq t_j$) due to clock drifts. The local time t_i can be written as a function of the global time t as [24], [25]

$$t_i = (1 + d_i)t \tag{1}$$

where d_i is the clock drift rate of the i processor. Ideally, the clock drift rate is $d_i = 0$. In practice, all clocks have drifts with very small values (typically, several parts per million, ppm). Table I lists the measured clock drift rates of the three processors shown in Fig. 1 [28]. Note that the clock of the DSP 2 is chosen to represent the global time of the microgrid. This choice is made only to carry out the theoretical analysis of the system.

The reference frequency of each inverter ω_i^* is generated using the local time t_i. The power inverters force the local frequency ω_i to follow the reference frequency ω_i^* in order to regulate the frequency of the microgrid and supply the load cooperatively. As discussed next, active power steady-state errors are observed due to the clock drifts.

B. Control Objectives

The control objectives of the inverters shown in Fig. 1 are formulated in steady-state as follows:

1) To provide accurate power sharing (i.e., the power of the inverters must be proportional to its power rating while guaranteeing the supply of the load), which can be formulated as

$$P_{i,ss}^{id} = P_L \Big/ \sum_{j=1}^{n} \left(\frac{m_i}{m_j}\right). \tag{2}$$

In (2), $P_{i,ss}^{id}$ is the ideal power provided by each inverter in steady state. In this context, ideal power means the power supplied by each inverter assuming that the clock drift rate is zero, $d_i = 0$. Moreover, P_L is the load power and m_i and m_j are two parameters related to the rated power of the inverters. They will be formally defined in the following subsection.

2) To regulate the frequency of the microgrid in steady-state ω_{ss} to its nominal value ω_0, which can be formulated as

$$\omega_{ss} = \omega_0. \tag{3}$$

Due to clock drifts, the steady-state active power delivered by each inverter $P_{i,ss}$ is different to the ideal power $P_{i,ss}^{id}$. The difference between these two values depends on the control scheme used for the primary and secondary layers, as discussed in [25]-[28]. In addition, the steady-state microgrid frequency deviates from the nominal frequency [24]. These deviations are quantified by the active power and frequency steady-state errors as follows

$$e_{P_{i,ss}} = 100\frac{P_{i,ss} - P_{i,ss}^{id}}{P_i^{max}} \tag{4}$$

$$e_{f_{ss}} = \frac{\omega_{ss} - \omega_0}{2\pi} \tag{5}$$

where P_i^{max} is the maximum power of the INV i; see Table I.

C. Local Hierarchical Control without Communications

The hierarchical control without communications considered in this paper uses the droop method in the primary layer and the DLPF technique in the secondary layer. Fig. 2 shows a diagram of this standard control [20]. From Fig. 2, the reference frequency is generated as

$$\omega_i^*(t_i) = \omega_0 - m_i P_i(t_i) + \delta_i(t_i) \tag{6}$$

where ω_0 is the operating frequency of the inverter at no load (NL), m_i is the slope of the droop function and P_i is the averaged active power. This last variable is calculated using a low-pass filter LPF_P with cutoff frequency ω_P (the frequency sub-index P indicates primary layer)

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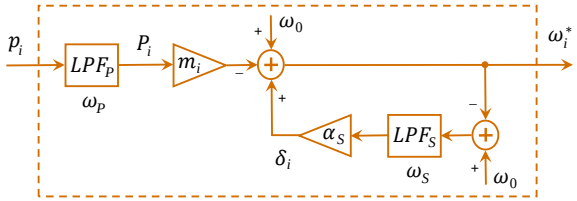

Fig. 2. Diagram of the local control without communications.

TABLE II
NOMINAL PARAMETER VALUES OF THE STANDARD CONTROL

Symbol	Quantity	Nominal value
m_i	Slope of the droop function	1 mrad/(Ws)
ω_P	Primary-layer cutoff frequency	2π rad/s
ω_S	Secondary-layer cutoff frequency	20π rad/s
α_S	Gain of the secondary layer	40

$$P_i(t_i) = \omega_P \int \left(p_i(t_i) - P_i(t_i)\right) dt_i \tag{7}$$

where the instantaneous active power p_i is the input of the filter. Additionally, $\delta_i(t_i)$ in (6) is the output of the secondary layer, as shown in Fig. 2, which is implemented using the DLPF technique as follows [20]

$$\delta_i(t_i) = \omega_S \int \left(\alpha_S(\omega_0 - \omega_i^*(t_i)) - \delta_i(t_i)\right) dt_i. \tag{8}$$

In (8), the input of the low-pass filter LPF_S is $\omega_0 - \omega_i^*$; see Fig. 2. Moreover, the control parameters α_S and ω_S are the gain and cutoff frequency of the filter, respectively. In this case, the frequency sub-index *S* indicates secondary layer.

It is possible to deactivate the secondary layer by setting $\alpha_S = 0$; see Fig. 2. Thus, the standard control in (6) operates only with the droop-based primary layer due to $\delta_i(t_i) = 0$.

Table II lists the nominal parameter values of the standard control. These values were designed following the guidelines reported in [3] for the primary layer (m_i and ω_P) and in [20] for the secondary layer (α_S and ω_S).

D. Problem Formulation

A procedure to determine the static characteristics of the standard control was presented in [28]. From this study, the steady-state errors in active power and frequency as a function of the clock drift rates can be written as:

$$e_{P_{i,ss}} = \omega_0(1+\alpha_S)\sum_{j=1}^{n}\left(\frac{d_i - d_j}{m_j}\right)\Big/\sum_{j=1}^{n}\left(\frac{m_i}{m_j}\right) \tag{9}$$

$$e_{f_{ss}} = \frac{-P_L}{2\pi(1+\alpha_S)}\Big/\sum_{j=1}^{n}\left(\frac{1}{m_j}\right). \tag{10}$$

The performance characteristics of the droop control can be derived using $\alpha_S = 0$ in (9) and (10). Fig. 3 illustrates them as a function of load using the parameters listed in Tables I and II. Note that the difference in the active power delivered by each inverter is negligible, which confirms that clock drifts have an insignificant effect on the droop-based power sharing, as announced in [25]. However, there is a large deviation in the microgrid frequency, which increases with load. In particular, the frequency deviation is 147 mHz at full load (FL). In real applications, this deviation is not enough to activate the under-frequency protection of the inverters, which is normally set at 600 mHz below the nominal frequency [5]. Consequently, the frequency deviation is not a relevant problem in the microgrids deployed to operate only in islanded mode. However, in those applications operating in both grid-connected and islanded mode, it is advised not to have large frequency deviations in islanded mode to facilitate a smooth transition to grid-connected mode [2].

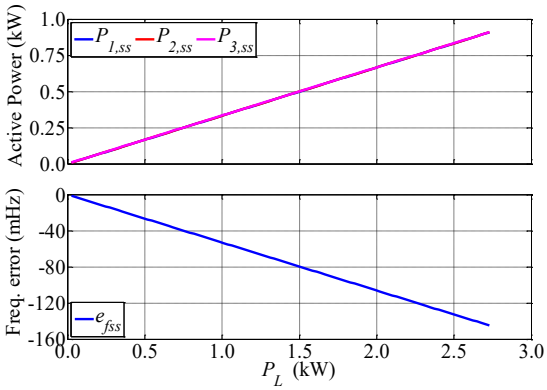

Fig. 3. Active powers and frequency errors in steady-state versus load for the droop control (i.e., the standard control with $\alpha_S = 0$).

Fig. 4 shows the active powers and the frequency errors as a function of load for the standard control. Two values of α_S are considered in this figure. With $\alpha_S = 40$ (nominal value), the error in the frequency is significantly reduced compared to the results of the droop control, as seen in Fig. 3(a). In fact, the frequency deviation at FL is only 3.5 mHz. With this value, the transition from islanded to grid-connected mode is greatly facilitated. The price to pay for this low frequency deviation is a deterioration in power sharing with a constant deviation of 4% for all load conditions. A second value of α_S higher than the nominal one is considered to observe the deterioration of power sharing produced when α_S is increased. With $\alpha_S = 160$, although the error in frequency becomes insignificant (0.9 mHz at FL), the error in active power is 16% for all the load range; see Fig. 4(b). This feature is particularly negative at high load conditions, when the practical consequences of the power deviation such as excessive stress and poor thermal management aggravate. Therefore, the problem of power sharing deviations produced by the clock drifts is more relevant in scenarios at high load conditions.

II. PROPOSED LOCAL SECONDARY CONTROL

The aim of this study is to introduce a local secondary control with accurate power sharing and good frequency regulation in high load conditions. This section presents the proposed control and an analysis that reveals its static and dynamic features.

A. Control Architecture

A new control scheme is derived starting from the standard control expressed in (6). Since the goal is to reduce the

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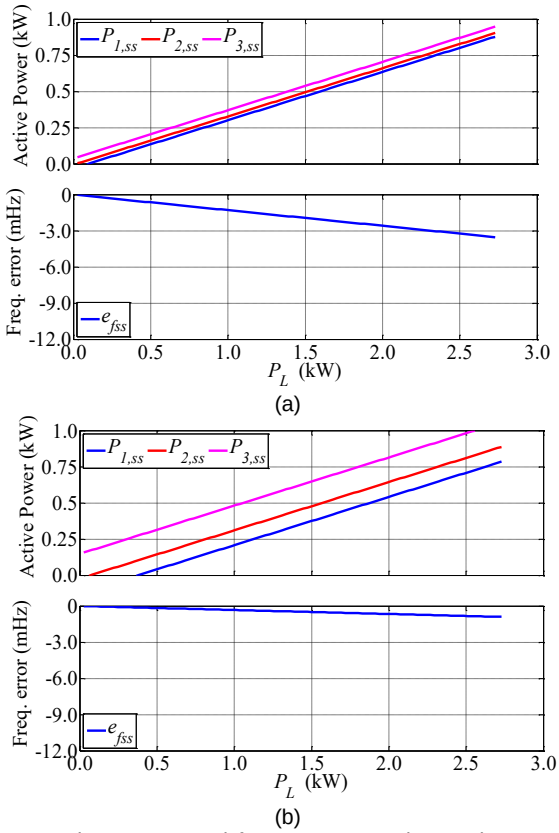

Fig. 4. Active powers and frequency errors in steady-state versus load for the standard control with (a) $\alpha_S = 40$ and (b) $\alpha_S = 160$.

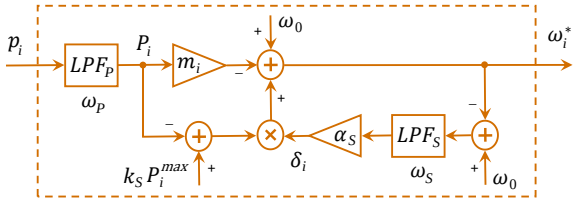

Fig. 5. Diagram of the proposed control.

deviations in power sharing, a new error equation for the active power is considered

$$e_{P_i} = k_S P_i^{max} - P_i(t_i) \tag{11}$$

where k_S is a control parameter. This error is zero at the desired active power according to the value of k_S. This property is used to obtain an accurate power sharing under high load conditions by including (11) in (6) and by properly setting the k_S parameter. The design of this parameter is presented in Section IV. In particular, the error term in (11) is multiplied by the output of the DLPF in (8), resulting in the new reference frequency, leading to

$$\omega_i^*(t_i) = \omega_0 - m_i P_i(t_i) + \delta_i(t_i)\left(k_S P_i^{max} - P_i(t_i)\right) \tag{12}$$

In (12), the averaged active power P_i and the output of the DLPF δ_i are calculated using (7) and (8), respectively. A diagram of the proposed control is shown in Fig. 5.

B. Static Characteristics

The static performance of the proposed control is

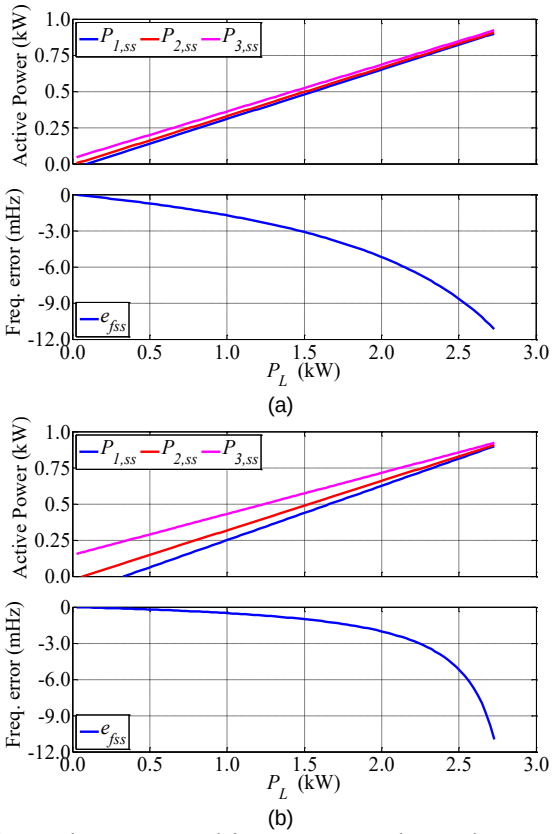

Fig. 6. Active powers and frequency errors in steady-state versus load for the proposed control with (a) $\alpha_S = 0.03$, $k_S = 1.41$ and (b) $\alpha_S = 0.16$, $k_S = 1.08$.

determined by the steady-state errors in active power and frequency. The error expressions are derived by applying the analysis procedure presented in [28] to (7), (8) and (12). The results are written as

$$e_{P_{i,ss}} = \omega_0\left(1 + \alpha_S\left(k_S P_i^{max} - P_{i,ss}^{id}\right)\right)\sum_{j=1}^{n}\left(\frac{d_i - d_j}{m_j}\right)\Big/\sum_{j=1}^{n}\left(\frac{m_i}{m_j}\right) \tag{13}$$

$$e_{f_{ss}} = \frac{-P_L}{2\pi\left(1 + \alpha_S\left(k_S P_i^{max} - P_{i,ss}^{ID}\right)\right)}\Big/\sum_{j=1}^{n}\left(\frac{1}{m_j}\right). \tag{14}$$

Fig. 6 shows the active powers and frequency errors using the parameters listed in Table I and in the figure caption. The proposed control has the ability to improve the power sharing as the load increases, reaching negligible errors at FL. The price to pay for this improvement in power sharing is a larger deviation in frequency compared to the standard control. Both accurate power sharing at FL and small frequency deviation are guaranteed by the design of the proposed control with the systematic procedure presented in Section IV.

C. Dynamic Characteristics

The phase margin and the control bandwidth are the metrics considered in this study to evaluate the dynamic performance of the proposed control. Below a procedure to derive the open loop transfer function $T_i(s)$ for the standard and the proposed control is presented. The dynamic characteristics are measured from this transfer function.

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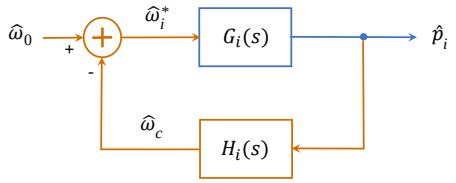

Fig. 7. Diagram of the small-signal model of an inverter with local hierarchical control.

TABLE III
IMPEDANCE SEEN FROM THE OUTPUT SIDE OF THE INVERTERS

Symbol	Quantity	Nominal value
$R_1 + j\omega_0 L_1$	Impedance seen at inverter 1	0.90 + j 7.02 Ω
$R_2 + j\omega_0 L_2$	Impedance seen at inverter 2	0.93 + j 6.45 Ω
$R_3 + j\omega_0 L_3$	Impedance seen at inverter 3	1.38 + j 6.55 Ω

Fig. 7 shows the small-signal model of an inverter with hierarchical control. The transfer functions $G_i(s)$ and $H_i(s)$ represent the small-signal models of the inverter and the control, respectively. In Fig. 7, the hat ^ denotes small-signal variables and s is the Laplace operator.

Small-signal models of droop-controlled inverters have been extensively studied in the literature for stability analysis [3], [10]. In particular, dynamic phasor modeling provides accurate models by preserving dynamics neglected by other approaches [29]. This study uses the dynamic phasor model reported in [30] for an inverter connected to a microgrid. The transfer function of the inverter $G_i(s) = \hat{p}_i(s)/\hat{\omega}_i^*(s)$ can be written as

$$G_i(s) = \frac{\omega_0 L_i V_i^2}{((L_i s + R_i)^2 + (\omega_0 L_i)^2)s} \tag{15}$$

where R_i and $\omega_0 L_i$ are the real and imaginary parts of the impedances seen from the output side of the inverters. These values are calculated from Fig. 1 and listed in Table III.

The digital processors that implement the local hierarchical control have individual clocks. Therefore, the transfer functions of the control system will rely on the drift rates of these clocks. These functions are derived as follows:

1) Write the model in the time domain as a function of the local clock that generate time t_i.
2) Rewrite the model in the time domain as a function of the global clock t using (1).
3) Write the model in the frequency domain using the Laplace transform.

From (7) and (8), the transfer function of the low-pass filters in the primary and secondary layers can be expressed as

$$LPF_P(s) = \frac{\hat{P}_i(s)}{\hat{p}_i(s)} = \frac{(1+d_i)\omega_P}{s + (1+d_i)\omega_P} \tag{16}$$

$$LPF_S(s) = \frac{\hat{\delta}_i(s)}{\hat{\omega}_0(s) - \hat{\omega}_i^*(s)} = \frac{\alpha_S(1+d_i)\omega_S}{s + (1+d_i)\omega_S}. \tag{17}$$

For the standard control, the reference frequency is obtained by inserting (17) in the frequency domain version of (6)

TABLE IV
PHASE MARGIN (°) AND CONTROL BANDWIDTH (RAD/S) USING DROOP, STANDARD AND PROPOSED CONTROL

Control	PM_1	PM_2	PM_3	BW_1	BW_2	BW_3
Droop	55.9	54.3	55.0	4.22	4.49	4.36
Standard	89.0	88.9	88.9	0.12	0.13	0.13
Prop. (NL)	89.0	88.9	88.9	0.13	0.14	0.13
Prop. (FL)	80.1	79.3	79.6	1.21	1.31	1.26

$$\hat{\omega}_i^*(s) = \hat{\omega}_0(s) - \frac{m_i LPF_P(s)}{1 + LPF_S(s)}\hat{p}_i(s). \tag{18}$$

From (18) and Fig. 7, the transfer function of the standard control $H_i^{st}(s)$ is identified as

$$H_i^{st}(s) = \frac{\hat{\omega}_c(s)}{\hat{p}_i(s)} = \frac{m_i LPF_P(s)}{1 + LPF_S(s)}. \tag{19}$$

Following a similar procedure for the proposed control and using (12) instead of (6), the transfer function $H_i^{pr}(s)$ can be written as

$$H_i^{pr}(s) = \frac{\hat{\omega}_c(s)}{\hat{p}_i(s)} = \frac{\left(m_i + \alpha_S(\omega_0 - \omega_{ss})\right)LPF_P(s)}{1 + \left(k_S P_i^{max} - P_{i,ss}\right)LPF_S(s)}. \tag{20}$$

The open-loop transfer function of the standard and proposed controls can finally be written as

$$T_i^{st}(s) = G_i(s)H_i^{st}(s) \tag{21}$$

$$T_i^{pr}(s) = G_i(s)H_i^{pr}(s). \tag{22}$$

From (21), the phase margin and the control bandwidth of the standard control are measured using the parameters listed in Tables I and II. The dynamic characteristics of the droop control can also be obtained using $\alpha_S = 0$ in (17). Table IV collects these measures for both control schemes. Note that the impact of clock drifts on the dynamic characteristics is negligible. This fact is clearly seen in Table IV where the measures of the three inverters show a very small deviation for each control. In addition, the phase margin increases and the control bandwidth decreases when α_S is changed from 0 to 40 and, therefore, it is expected to observe a slower transient response in the standard control compared to the droop control.

Fig. 8 shows the dynamic characteristics as a function of load for both control schemes. Note that the phase margin and the control bandwidth are constant, thus maintaining the dynamic properties for all load conditions.

Fig. 9 shows the phase margin and the control bandwidth for the proposed control. These measures are obtained from (22) using the parameters listed in Tables I and II (only m_i and ω_P). For low load conditions, the dynamic characteristics coincide with those obtained in the standard control; see also Table IV. Even more interesting is to observe that the control bandwidth improves as load increases (see Fig. 9), thus guaranteeing a faster transient response. Table IV shows that the control bandwidth is almost a decade larger at FL than at NL. This is an advantage of the proposed control, which is

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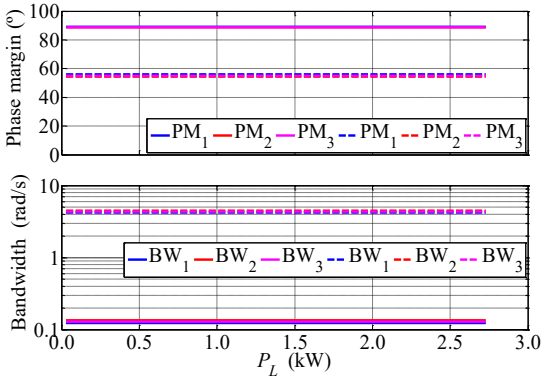

Fig. 8. Phase margin and control bandwidth versus load for the droop control (discontinuous lines) and the standard control (continuous lines).

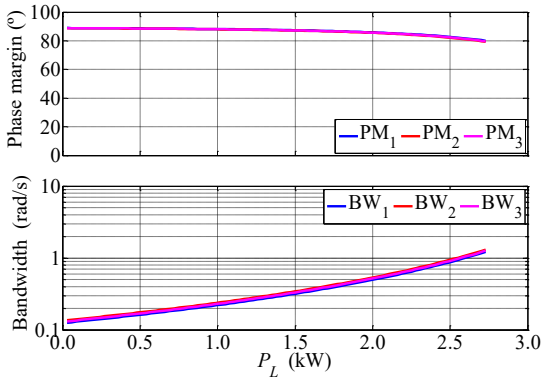

Fig. 9. Phase margin and control bandwidth versus load for the proposed control ($\alpha_S = 0.03$ and $k_S = 1.43$).

achieved at the price of slightly reducing the phase margin.

The above theoretical analysis shows that the phase margin of the three inverters shown in Fig. 1 is positive; see Table IV. This is true for all loading conditions (from NL to FL). As a consequence, the inverters present a stable operation for all the operating points of the microgrid. In Section V, the stability of the microgrid is validated experimentally.

III. Control Design

This section presents a systematic procedure to design the parameters of the proposed secondary control layer (α_S, k_S and ω_S); see Fig. 5. The parameters of the primary control layer (m_i and ω_P) were designed following the guidelines reported in [3]. The procedure is illustrated with a numerical example.

A. Design Specifications

Table V lists the design specifications of the proposed control and the values used in the numerical example. The maximum error in active power and frequency are the static specifications. In the proposed control, these maximum errors are obtained at NL and FL, respectively, as shown in Fig. 6.

The dynamic specifications are the desired phase margin and control bandwidth. To guarantee enough relative stability, the specified phase margin must be analyzed for all the load range conditions. The control bandwidth specification is provided for FL and it is set a decade above the bandwidth of the standard control.

TABLE V
Design Specifications of the Proposed Control

Symbol	Quantity	Nominal value
$e_{P_{i,NL}}^{max}$	Maximum error in active power	4% (at NL)
$e_{f_{ss}}^{max}$	Maximum error in frequency	12 mHz (at FL)
PM	Phase margin	Higher than 60 º
BW_C	Control bandwidth at full load	1.3 rad/s

TABLE VI
Solution to the Design Example of the Proposed Control

Symbol	Quantity	Nominal value
m_i	Slope of the droop function	1 mrad/(Ws)
ω_P	Primary-layer cutoff frequency	2π rad/s
ω_S	Secondary-layer cutoff frequency	20π rad/s
α_S	Gain of the secondary-layer filter	0.03 W^{-1}
k_S	Parameter of the secondary layer	1.43

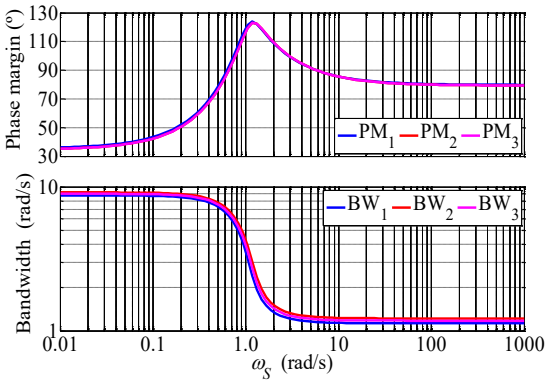

Fig. 10. Phase margin and control bandwidth vs ω_S for the proposed control ($\alpha_S = 0.03$ and $k_S = 1.43$).

B. Design Procedure

First, the parameters α_S and k_S are designed according to the specifications for the maximum errors in power and frequency. From (13) and (14), these errors can be written as

$$e_{P_{i,NL}}^{max} = \omega_0(1 + \alpha_S k_S P_i^{max}) \sum_{j=1}^{n} \left(\frac{d_i - d_j}{m_j}\right) \Big/ \sum_{j=1}^{n} \left(\frac{m_i}{m_j}\right) \quad (23)$$

$$e_{f_{ss}}^{max} = \frac{-P_L^{max}}{2\pi(1 + \alpha_S(k_S - 1)P_i^{max})} \Big/ \sum_{j=1}^{n} \left(\frac{1}{m_j}\right). \quad (24)$$

Note that the maximum error in power sharing takes place at NL (i.e., when $P_{i,ss}^{id} = 0$), as shown in Fig. 6. Conversely, the maximum deviation in frequency is obtained at FL (i.e., when $P_{i,ss}^{id} = P_i^{max}$). The values of α_S and k_S are calculated from (23) and (24) using the parameters shown in Tables I, II (only m_i and ω_P) and V. The results are listed in Table VI.

Second, the parameter ω_S is designed according to the dynamic specifications. Fig. 10 shows the phase margin and control bandwidth as a function of this parameter. Note that there is a wide range of values that meet the specifications. In particular, for ω_S > 5 rad/s, it is simultaneously achieved the scenario where the phase margin is higher than 60º and the control bandwidth is 1.3 rad/s. The value ω_S = 20π rad/s is chosen because it belongs to this range and coincides with the

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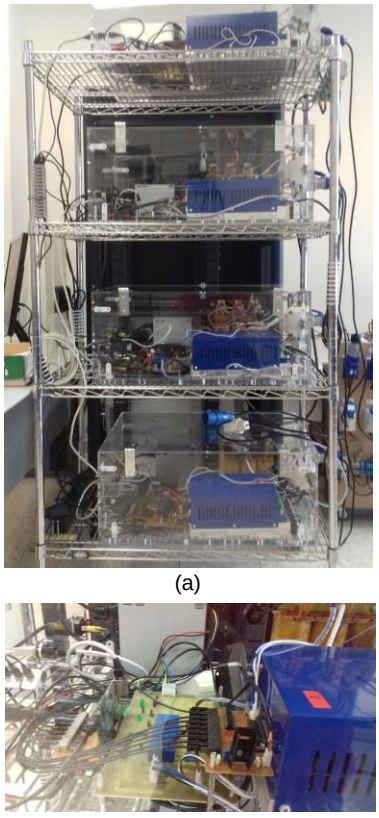

(a)

(b)

Fig. 11. Photo of the laboratory microgrid: (a) complete setup and (b) detail of the DSP card, sensing boards and three-phase inverter.

design of ω_S for the standard control [20]; see Table II.

From Fig. 10, it is worth mentioning that there is a range of values, 0.3 rad/s < ω_S < 5 rad/s, in which the control bandwidth is higher than 1.3 rad/s while the phase margin meets the specification. In this case, a faster transient response is expected. However, the design of ω_S inside this range causes undesired interactions between the operation of the primary and secondary control layers. Traditionally, to avoid these interactions, the secondary control bandwidth is designed lower than the primary control bandwidth [3], [4]. This is the control guideline used to specify the value of BW_C in Table V.

IV. Experimental Validation

This section validates the theoretical results with a selection of experimental tests that were conducted in the laboratory microgrid shown in Fig. 1.

A. Description of the Laboratory Microgrid

Fig. 11 shows a photo of the laboratory microgrid. In Fig. 11(a), the blue boxes are three-phase IBGT full-bridge inverters (Guasch, MTL-CBI0060F12IXHF) controlled by dual-core DSPs (TI, Concerto F28M36P63C). The control schemes shown in Fig. 2 and Fig. 5 were programmed in the DSPs with the control gain values listed in Tables II and VI. The inverters supply the load with the power delivered by a DC source (Amrel, SPS800-19) programmed at V_{DC} = 350 V. Fig. 11(b) shows a detail of a DSP card, sensing boards and a three-phase inverter. The nominal values of the setup, including microgrid voltage, line impedances and clock drift rates of the DSPs are listed in Table I. The measured results were exported from the DSPs to MATLAB© to achieve a high-quality representation of the figures with experimental results.

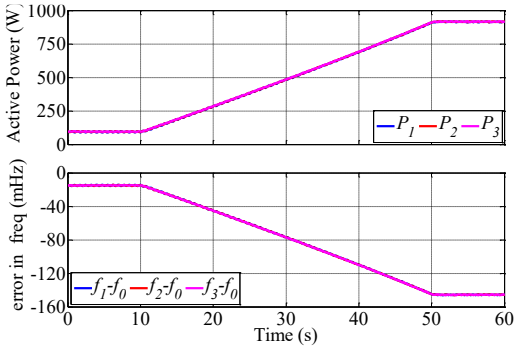

Fig. 12. Experimental active powers and frequency errors for soft load changes using the droop control.

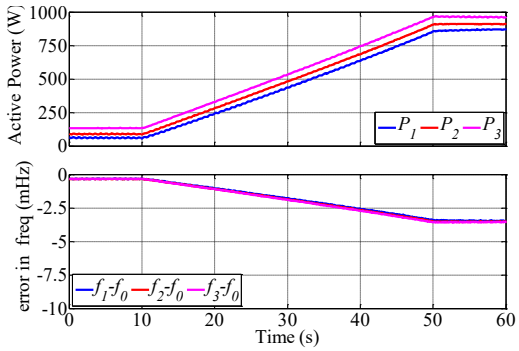

Fig. 13. Experimental active powers and frequency errors for soft load changes using the standard control.

B. Validation of the Static Characteristics

The first test consists on measuring the active powers and frequency errors when the load changes slowly from 10% to 100% of FL. Fig. 12 shows the results of the droop control. As predicted by the theoretical analysis, the impact of clock drifts on the active power is negligible in this control approach. However, the use of a secondary layer is necessary to avoid the large deviation in frequency at FL.

Fig. 13 shows the results of the standard control. In this case, the frequency errors are drastically reduced, with a maximum value of 3.2 mHz at FL. This frequency regulation improvement caused by the secondary layer magnifies the deviation in power sharing. In particular, the error in active powers are almost constant for all the load range, being its maximum value 5.9 %. Therefore, the impact of clock drifts is noticeable in the standard control and can be a relevant problem in power sharing under high load conditions.

This problem is solved by the proposed control, as shown in Fig. 14. Note that excellent power sharing is reached at high load conditions. In addition, the static specifications are met with a maximum error in active power of 3.9 % at NL and a maximum frequency deviation at FL of 9.3 mHz. Note that at NL the error in active power is similar to that obtained with the standard control. The reason is that the proposed control in

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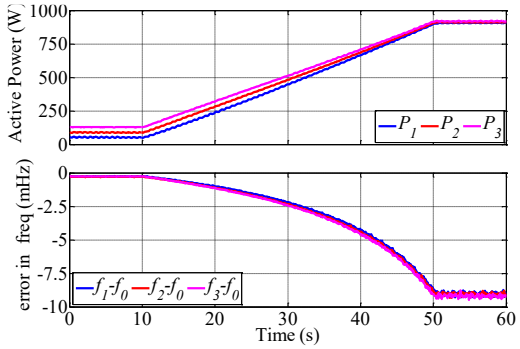

Fig. 14. Experimental active powers and frequency errors for soft load changes using the proposed control.

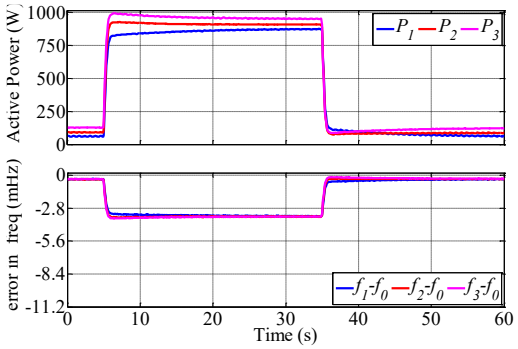

Fig. 15. Experimental active powers and frequency errors for abrupt load changes using the standard control.

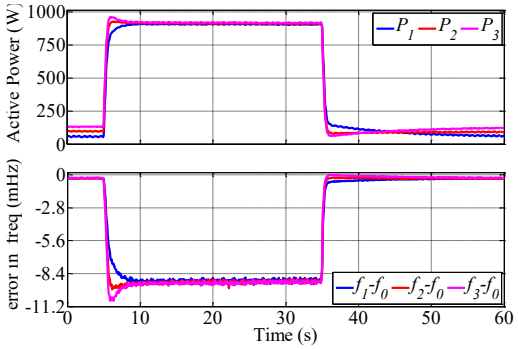

Fig. 16. Experimental active powers and frequency errors for abrupt load changes using the proposed control.

(12) exactly coincides with the standard control in (6) at NL. In other words, the error in (11) does not eliminate the power sharing deviations at NL. It is worth mentioning that this feature is not a relevant problem given that at low load conditions the inverter currents are small, thus the poor termal distribution has a insig-nificant impact on the inverters performance.

C. Validation of the Dynamic Characteristics

The second test involves changing the load abruptly during the experiment from 10% of FL to FL at t = 5 s and from FL to 10% of FL at t = 35 s.

Fig. 15 and 16 show the experimental results for the standard and the proposed control, respectively. As announced above, the transient response of the standard control does not rely on the load. The settling time is 15.2 s for both load changes. In the proposed control, this measure practically coincides with the load change from FL to 10 % of FL, as shown in Fig. 16. The most interesting point is the fast transient response that is achieved with the proposed control during the load change from 10 % of FL to FL with a settling time of only 5.1 s.

The static characteristics are confirmed by the results shown in Fig. 15 and 16. In the standard control, the deterioration in power sharing due to the clock drifts does not change for different load conditions. In the proposed control, the error in power sharing is negligible at FL while it nearly coincides with the error in the standard control at 10% of FL. The improvement in power sharing is reached at the price of a largest deviation in frequency. In practice, this maximum deviation is limited by a proper design of the control parameters. It is worth mentioning that the protection algorithms play an important role in the proposed control. If the power approaches its maximum value, then the frequency deviates exponentially, as shown in Fig. 6. Therefore, the protection must ensure that the maximum power is never exceeded.

V. Worst Case Analysis: Power Sharing at FL

The active power sharing at FL is the main point considered in this study. The proposed control clearly reduces the error in power sharing for the measured values of the clock drift rates, as verified experimentally. This section analyzes the deviations in the active power sharing at FL for the worst case. Recommendations on control design to reduce these deviations are also included.

A. Deviations on Active Power Sharing at FL

Theoretically, from (13), the error in active power sharing at FL is written as:

$$e_{P_{i,FL}} = \omega_0(1+\alpha_S(k_S-1)P_i^{max})\sum_{j=1}^{n}\left(\frac{d_i-d_j}{m_j}\right)\Big/\sum_{j=1}^{n}\left(\frac{m_i}{m_j}\right). \quad (25)$$

In practice, variations in clock drift rates d_i and d_j depend on technological, mechanical and environmental tolerances [31], that may be upper bounded by a given limit of $\pm d_{max}$. Environmental changes are caused by temperature, aging and mechanical effects (including shock, vibration and gravity). Normally, the dominant differences in clock drift rates are caused by these tolerances, especially in high-quality crystal oscillators such as temperature compensated and oven controlled devices [25], [31]. Assuming this type of oscillators, the maximum error in active power sharing at FL in terms of these tolerances can be written for the worst case as

$$e_{P_{i,FL}}^{max} = \omega_0(1+\alpha_S(k_S-1)P_i^{max})\frac{2(n-1)d_{max}}{n\,m_i}. \quad (26)$$

This expression is obtained by considering the worst case in which all clock drift rates d_i and d_j in (25) take the value d_{max} or $-d_{max}$. It is worth mentioning that the probability that these upper limit values are given at the same time for all processors in a practical scenario is extremely low.

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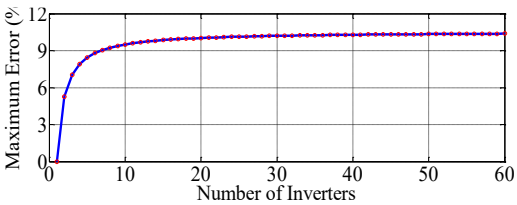

Fig. 17. Maximum error in active power sharing at FL using the upper limits of the clock drift rates for all inverters (d_{max} = 10 ppm).

B. Discussion

Fig. 17 shows the maximum error in active power sharing at FL using (26). Microgrids with a different number of inverters *n*, ranging from 1 to 60, is considered. From the figure, it can be observed that the error in power sharing is lower when the number of inverters is small. In addition, in large microgrids with many inverters, the inclusion of new ones does not significantly affect the load sharing error.

In any case, the most important remark about Fig. 17 is that the error in the worst case is high. This fact makes it necessary to adjust the parameters of the proposed control at the factory once the clock drift of the DSP has been measured for the current device. This is the main limitation of the proposed control.

VI. Conclusion

In this paper, the main contribution is the proposal of a new secondary control scheme that drastically reduces the active power sharing deviations in inverter-based microgrids under high-load conditions. The problem solved is relevant in real applications in which local controllers have separate processors with individual clock that inherently suffer from drift. The proposed solution modifies the standard communication-free control by introducing a new error term as a function of the active power, which improves the static and dynamic characteristics of the microgrid for high-load conditions.

A theoretical analysis has been carried out to quantify the steady-state deviations in power sharing as a function of the clock drift rates. In addition, the impact of clock drifts on phase margin and control bandwidth has been analyzed. From this study, a systematic procedure to design the parameters of the proposed control is presented. The theoretical results have been validated practically with experimental tests on a laboratory microgrid equipped with three digital signal processors. The sensitivity analysis shows that the maximum error in active power sharing at full load is high in the worst case scenario (when all the clock drift rates take the maximum value simultaneously). Although the probability of this scenario to occur is very low, it is the main limitation of the proposed control.

As a final remark, it is shown that the impact of clock drifts on the operation of inverter-based microgrids with separate processors can be high depending on the secondary control scheme implemented in the local controllers and the design of the given control parameters. This fact is observed in a microgrid equipped with processors with individual clock that inherently suffer from drift, even knowing that drift rates are as small as several ppm. An open topic for future research is the development of robust control schemes against both tolerance and temporal variations of clock drifts. The design of protection algorithms to limit frequency deviations in practical implementations can also be considered.

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