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Design of Broadband CNFET LNA Based on Extracted I-V Closed-Form Equation

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***Abstract*— A procedure of extracting a closed-form user-friendly I-V equation for short channel carbon nanotube field-effect transistors (CNFET) in the saturation region is presented by employing a relation between CNFET parameters meeting the experimental results. The methodology is based on the Stanford model and ballistic relation of one channel CNFET. In this regard, the ballistic relation is simplified to a closed-form I-V equation, and then, the parameters are estimated through the fitting algorithm by means of ICCAP and least square (LS) method, respectively, and the obtained equation is verified by the experimental results given in the literature. Additionally, an extended quantitative noise analysis is performed at the circuit level and the noise sources implemented in Verilog-A are added to the Stanford CNFET HSPICE model. Subsequently, with the accordance to the extracted I-V equation, a CNFET-based inductor-less broadband common-gate low noise amplifier (LNA) is designed theoretically and its results are confirmed in HSPICE based on the Stanford CNFET model, indicating a proper matching between analysis and simulation. The proposed CNFET-based LNA provides very high frequency bandwidth and also lower noise figure in comparison with its contemporary CMOS-based LNA, without any passive spiral inductor.**

***Index Terms*—Carbon nanotube (CNT), field-effect transistor (FET), short channel, closed-form I-V equation, Low noise amplifier (LNA), radio frequency (RF), noise figure (NF), nanoelectronics.**

I. Introduction

CARBON nanotubes (CNTs) have the same properties of conductors and semiconductors. They are utilized in the field-effect transistors (FETs) as an alternative to conventional channels to provide CNFET devices, being considered as promising devices that could be substituted for CMOS by continuing scaling trends in semiconductor technology in the future [1]. Despite the intensive researches on the CNFETs in digital circuits and applications [2]–[4], few works can be found on CNFET applications in analog and RF domain; some of them are limited to presenting the lumped model for CNFET structures as impedance matching components via metal contacts [5]; other studies have focused on the CNFET unity gain frequency, f_T, as a RF property which is given by $v_F/(2\pi L_g)$ for the Fermi velocity of v_F and gate length of L_g [6], and also have performed CNFET device level considerations [7]. Moreover, RF building blocks features such as noise, linearity, power, and bandwidth have been reviewed in [8], [9]. Since the mentioned works indicate that CNFET can be utilized in RF applications, a simplified user-friendly I-V equation according to CNFET parameters is required at the first step of analog/RF integrated circuit (IC) design. In particular, apart from our preliminary work [10], there exists no user-friendly I-V equation for CNFET as clear as MOSFET. In [11], [12], optimum analog CNFET-based circuit design is suggested; however, their design methods are just focused on sweeping the CNFET geometric design parameters. On the other hand, from experimental point of view, there are some experiments obtained from the fabricated CNFETs with the channel length of 350 nm - 1 μm in RF domain, which are categorized as long channel devices, and some noise analysis are performed [5], [13]. However, considering short channel devices with minimum size channel length is desirable to achieve the inherent capability of CNFETs in terms of noise and bandwidth in comparison with MOSFETs [14]. In overall, introducing a closed-form user-friendly I-V equation for short channel CNFET devices by employing a relation between CNFET parameters meeting the experimental results could be a primary requirement to have more details for CNFET-based RF IC design. Stanford CNFET model [15]–[18] provides a precise explanation of the electrical behavior of the intrinsic and additional doped CNTs. It has strong physical aspects such as transcapacitance network for intrinsic and doped CNTs, carrier scattering, parasitic capacitance, and screen effect. Apart from the mentioned features, it has a high accuracy with respect to the experimental results obtained from the fabricated CNFETs [18]. As well, it is notable that in the Stanford CNFET model, the transistor is considered as a short channel device with the channel length in the range of 10-100 nm in which the transport is quasi-ballistic. Additionally, a qualitative noise analysis is performed in [19] on short channel CNFETs based on the Stanford CNFET model.

As it is mentioned earlier, CNFET devices can be utilized in RF applications like low noise amplifiers (LNA), which are one of the essential blocks in receiver architectures. Moreover, the trend towards broadband LNAs in modern and future

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communication systems is due to covering multi-band frequencies, simultaneously, and reducing the total power by eliminating the extra components. Nevertheless, the design of broadband LNAs has conflicts in several aspects. One challenge is to achieve a low noise figure (NF) less than 3dB as well as maintaining impedance matching over several gigahertz bandwidth. Utilizing the CNFET technology in conjunction with RF circuit techniques makes it possible to meet suitable circumstances for designing broadband CNFET-based LNAs. In order that, a theoretical background like prior technologies is needed. I-V equation at this background aids designers to acquire predictable consideration about CNFET's behavior. This work aims to extract a closed-form I-V equation for short channel CNFETs through which the design of RF circuits like broadband CNFET-based LNA would be easier.

This paper is organized as follows. In section II, a closed-form I-V equation is extracted for short channel CNFETs in the saturation region based on the Stanford model and ballistic relation of one channel CNFET. After that and in section III, a quantitative noise analysis is performed at the circuit level for a short channel CNFET based on the Stanford model. The theoretical design of a CNFET-based broadband LNA is discussed, and then, its performance is compared to the CMOS-based LNA in sections IV and V, respectively. It is then followed by conclusion in section VI.

II. Closed-Form I-V Equation of the Uncorrelated Channel CNFET in the Saturation Region

A. Basis of CNFETs

A 3D view of CNFET is illustrated in Fig. 1 (a) in which its channels are formed by intrinsic semiconductors of carbon nanotubes. The geometric parameters D, W, N, and S indicate the diameter of the CNT, the transistor gate width, number of channels, and distance between centers of two adjacent CNTs, respectively. The relevance between these parameters is given by (1) [12]. Moreover, the parameter D has an inverse relation with the threshold voltage of CNTs, V_{th}, which is considered as half of the band gap energy, E_g, and expressed as (2) [20].

$$W = (N-1)S + D \tag{1}$$

$$V_{th} = \frac{E_g}{2q} = \frac{0.42}{D(nm)}(\mathrm{V}) \tag{2}$$

where q is the electron charge. If the chirality vector is assumed as $C_h = (n_1, n_2)$, the parameter D can be expressed as below [20]:

$$D = |C_h|/\pi = (a_c/\pi)\sqrt{n_1^2 + n_1 n_2 + n_2^2} \tag{3}$$

where a_c is the graphene lattice constant.

Fig. 1 (b) shows the cross-sectional view of the CNFET. The surface potential of the intrinsic channel, φ_S, is obtained by voltage dividing between the quantum capacitance per channel per unit length, C_q, given by (4), and the gate-channel electrostatic oxide capacitance per channel per unit length, C_{ox}, as (5) [20].

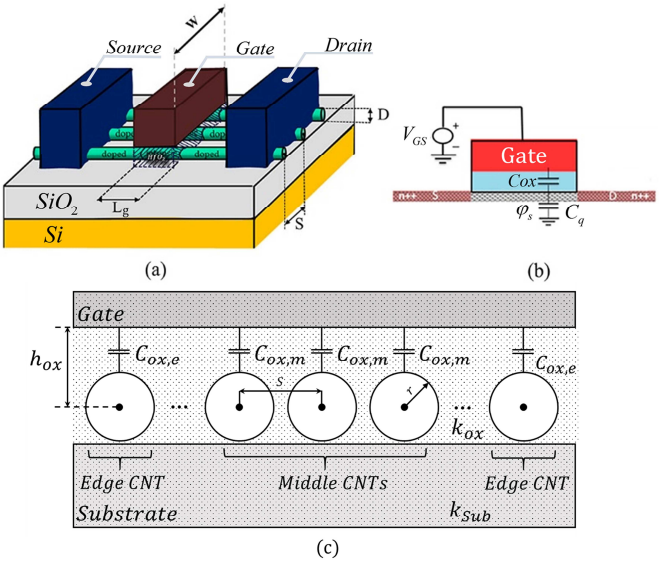

Fig. 1. CNFET: (a) 3D view, (b) cross-sectional view, and (c) front view of intrinsic CNTs.

$$C_q = \frac{2q^2}{h v_F} \tag{4}$$

$$\varphi_s = \frac{C_{ox}}{C_{ox} + C_q} V_{GS} = t V_{GS} \tag{5}$$

in which t, v_F, and V_{GS} are the dividing factor, Fermi velocity of the CNT carriers, and its gate-source voltage, respectively. As a matter of fact, due to the position of the intrinsic CNTs, the oxide capacitors, *i.e.* gate-channel capacitors, are separated to middle, $C_{ox,m}$, and edge, $C_{ox,e}$, capacitors, as shown in the Fig. 1 (c) [16], [18]. The relation between these two oxide capacitors can be expressed as below:

$$C_{ox,m} = C_{ox,e}(1 - \eta_c) \tag{6}$$

$$\eta_c = \frac{\ln\left(\frac{S^2 + 2(h_{ox} - r).[h_{ox} + \sqrt{h_{ox}^2 - r^2}]}{S^2 + 2(h_{ox} - r).[h_{ox} - \sqrt{h_{ox}^2 - r^2}]}\right)}{2[\cosh^{-1}(\frac{2h_{ox}}{D}) + \frac{k_{ox} - k_{Sub}}{k_{ox} + k_{Sub}} \ln(\frac{2h_{ox} + 2D}{3D})]} + \frac{\frac{k_{ox} - k_{Sub}}{k_{ox} + k_{Sub}} \ln(\frac{S^2 + (h_{ox} + D)^2}{S^2 + 9r^2}).\tanh(\frac{h_{ox} + r}{S - D})}{2[\cosh^{-1}(\frac{2h_{ox}}{D}) + \frac{k_{ox} - k_{Sub}}{k_{ox} + k_{Sub}} \ln(\frac{2h_{ox} + 2D}{3D})]} \tag{7}$$

where h_{ox}, k_{ox}, k_{Sub}, and r are the distance between the center of CNTs to the gate of the device, the gate oxide dielectric coefficient, the substrate dielectric coefficient, and the radius of the CNTs, respectively. The factor η_c shows the electrostatic effect of the adjacent channels on the middle channel which makes its capacitor to be different from the edge capacitor. However, in accordance with [16] and by assuming S greater than 20 nm, η_c is negligible. Therefore, the value of oxide capacitor per channel per unit length can be written as (8), in which ε_0 is vacuum permittivity.

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$$C_{ox} = C_{ox,m} = C_{ox,e} = \frac{2\pi k_{ox}\varepsilon_0}{\cosh^{-1}\left(2h_{ox}/\mathrm{D}\right)} \qquad S > 20nm \tag{8}$$

From electromagnetic point of view, the current of channels may be influenced by the adjacent channels because of the magnetic coupling between the near channels. It is feasible to specify these influences by calculating the magnetic field from nearest channel on target one, B, via the magnetic law, as (9).

$$B = \frac{\mu_0 I_c L_c}{2\pi S\sqrt{S^2 + L_c^{\,2}}} \tag{9}$$

where μ_0 and L_c are the permeability and half-length of each CNT, respectively. For a typical CNT, I_c is the DC drain-source current of each channel in the range of micro ampere, L_c and S are in the range of nanometer, giving the acquired B in the range of 10^{-4} T. Such a small magnetic field cannot influence the current of the target channel [21].

In the light of the electrostatic and electromagnetic effects, generally, CNFET channels can be classified as correlated and uncorrelated channels. Namely, the current of the uncorrelated channel is not influenced by the adjacent channels currents. Indeed, for S greater than 20 nm all channels have similar properties, *i.e.* η_c is approximately equal to zero. By contrast, for the correlated channels, S lower than 20 nm, the current of target channel is affected by other channels via the electrostatic capacitances and electromagnetic fields.

B. Description of the closed-form I-V equation

As mentioned in prior sections, the Stanford model does not provide any straightforward closed-form I-V equation for the design of CNFET devices. For instance, in the Stanford model level 2, by considering the charge conservation equations [17], I_D of the short channel CNFET with the drain-source voltage of V_{DS} in the saturation region is expressed as below:

$$I_D = \frac{\sqrt{3}a_C\pi V_\pi C_{ox}(V_{GS} - \varphi_S)}{h}\sum_{k_m}\sum_{k_l}\frac{k_l}{\sqrt{k_l^2 + k_m^2}} \times\left[1 + \frac{L_g}{\lambda_{op}}\frac{\sqrt{(E(k_m,k_l) - \hbar\Omega)^2 - E(k_m,0)^2}}{E(k_m,k_l) - \hbar\Omega}\left(1 + e^{\frac{E(k_m,k_l) - q\varphi_S + qV_{DS} - \hbar\Omega}{KT}}\right)\right]^{-1} \tag{10}$$

where V_π, $\hbar\Omega$, h, KT, and λ_{op} are the carbon π-π band energy, optical phonon-energy, Planck's constant, thermal energy, and optical phonon-scattering mean free path, respectively. The energy of states $E(k_m,k_l)$ is undeniable which is related to the wave number circumferential direction k_m and wave number current flow direction k_l. In this case, m and l signify the mth and lth discrete sub-band in circumferential and current flow directions, respectively [17].

Nevertheless, to provide a closed-form I-V relation, considering some simplifications are required. The ballistic relation of one channel CNFET current is as follows [22]:

$$I_D = \frac{4q}{h}KT\left[ln(1 + e^{(q\varphi_S - Eg/2)/KT}) - ln(1 + e^{(q\varphi_S - qV_{DS} - \mathrm{Eg}/2)/KT})\right] \tag{11}$$

For the saturation region, $V_{DS} > V_{GS} - V_{th}$, it is irrefutable that the positive portion is dominated. Therefore, the saturation current can be expressed as below:

$$I_D = \frac{4q}{h}KT\left[ln(1 + e^{(q\varphi_S - Eg/2)/KT})\right] \tag{12}$$

Due to the value of KT, which is lower than $(q\varphi_S\text{-}E_g/2)$, the term 1 in (10) is neglected in comparison to the exponential term. As a result, the I-V equation can be obtained by substituting (2), (4), and (5) in (12), as follows:

$$I_D \approx 2v_F\frac{C_{ox}C_q}{C_{ox} + C_q}\left(V_{GS} - V_{th}/t\right) = g_C\left(V_{GS} - V_{th}/t\right) \tag{13}$$

where g_c is the transconductance of each CNT. Therefore, the ideal I-V equation for the short channel CNFET with N uncorrelated channels can be written as below:

$$I_\mathrm{D} \approx Ng_C\left(V_\mathrm{GS} - V_{th}/t\right) \tag{14}$$

C. Validation of the closed-form I-V equation

Since the Stanford model is available for ballistic short channel CNFETs, in order to validate the obtained closed-form equation given by (14), an optimization and curve fitting algorithm is applied on the CNFET by targeting the Stanford model. For doing it, the estimated closed-form I-V formula output is compared with the target system output, Stanford model, and the generated error is used to adjust the estimated formula coefficients.

The relation between the drain saturation current, I, and gate-source voltage, v, of the transistor in the ballistic transport is as follows:

$$I = \alpha(\mathrm{v} - \mathrm{v}'_{th})^p \tag{15}$$

in which v'_{th} is the threshold voltage of CNFET. The exponent characteristic, p, must be between 1 and 1.5 [23]. There are three parameters to fit, p, α, and v'_{th}. The ICCAP software is used to fit these three parameters, simultaneously. First, the results provided by the Stanford model are imported to ICCAP as a measurement. Then a Verilog-A model involving Eq. (15) is implemented. ICCAP, coupled with Spectre performs simulations on the Verilog-A model, adjusts the parameters step by step in order to match the measurement. Fig. 2 illustrates the estimated parameter p versus N, D, and S which are swept in practical ranges. As it is obvious, the abundance of p reaches the maximum value where it is between 0.94 and 1. As a result, it is considered that p is approximately equal to 1. Therefore, (15) can be updated as below:

$$I = \alpha(\mathrm{v} - \mathrm{v}'_{th}) = \theta_1\mathrm{v} + \theta_0 \tag{16}$$

where v'_{th} and α are equal to θ_1 and $-\theta_0/\theta_1$, respectively.

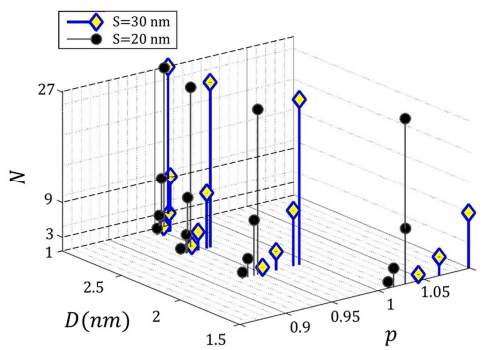

Fig. 2. Estimated parameter p for different N, D, and S

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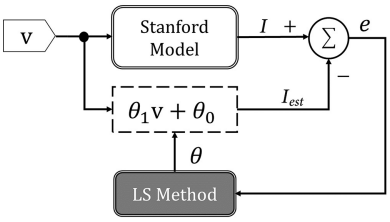

Fig. 3. Structure of the utilized system identifier.

As it can be seen, Eq. (16) is linear with respect to θ_0 and θ_1. Thus it can be identified by LS method. This structure is illustrated in Fig. 3, where the estimated current and error are denoted by I_{est} and e, respectively. Estimated coefficients vector, $\boldsymbol{\theta}$, containing θ_0 and θ_1, is achieved by using the LS method as below:

$$\boldsymbol{\theta} = V^{\dagger} I \tag{17}$$

where V represents the input matrix. Since the CNFET parameters are affected by geometric variations such as D, S, and N, changing one of the geometric parameters in each case for the input voltage from 0 to 2 V, while considering the others fixed, and extracting the drain current, the estimated coefficients vector is obtained via the LS method, as given in Table I and Fig. 4. It is noted that the drain voltage of the CNFET is tuned at the saturation region. As it is shown in Fig. 5, the estimated formula in (16) (dash line) has a good agreement with the target obtained from the Stanford model.

According to Fig. 5 (a), increasing N causes an increase in the drain current. If the number of channels becomes β times larger, the coefficient α will be increased by a factor of β, while v'_{th} will be constant (Fig. 4 (a)). The reason can be attributed to the parallel channels. On the other hand, for the variations of S greater than 20 nm, the drain current will be constant (Fig. 5 (b)). In addition, the coefficient α and v'_{th} will be constant, too.

In order to consider the effect of diameter on the drain current of CNFET, zigzag CNTs, i.e. CNTs with n_2=0 in (3), are considered. The increment of n_1 will cause to increase D and C_{ox} according to (3) and (8), respectively, and to decrease V_{th} based on (2), corresponding to the increment of coefficient α and reduction of v'_{th}, obtained in Figs. 4 (b) and 5 (c).

From the obtained results, it can be concluded that the coefficient α (transconductance) is proportional to the multiplication of the number of channels and the capacitance. Moreover, according to the transconductance unit, it is noticed that α is approximately equal to $NC_t\upsilon_{CNT}$ and the saturated drain current given by (16) can be updated as below:

$$I_D = NC_t\upsilon_{CNT}(V_{GS} - v'_{th}) \qquad V_{GS} \geq v'_{th} \tag{18}$$

in which, υ_{CNT} and C_t are the carrier velocity and equivalent capacitance per unit length of the CNTs, respectively. If it is assumed that $C_t^{-1} = C_q^{-1} + C_{ox}^{-1}$ and $v'_{th} = V_{th}/t$, an acceptable matching will be found between the I-V closed-form equations given by (18) and (14) for uncorrelated short channel CNFETs. In order to validate the accuracy of the proposed closed-form I-V equation for CNFET in the saturation region, it is compared with the experimental results of [24], as it is shown in Fig. 6, in which the obtained mean-square error is in the order of 10^{-14} A.

TABLE I
ESTIMATED COEFFICIENT

Case No.	N	S (nm)	D (nm)	α (A/V)	v'_{th} (V)
I. N_variation	1	20	1.5	3.64e-5	0.38
	3	20	1.5	1.08e-4	0.38
II. S_variation	3	20	1.5	1.08e-4	0.38
	3	30	1.5	1.08e-4	0.38
III. D_variation	1	20	2.8	5.37e-5	0.26
	1	20	1.5	3.64e-5	0.38

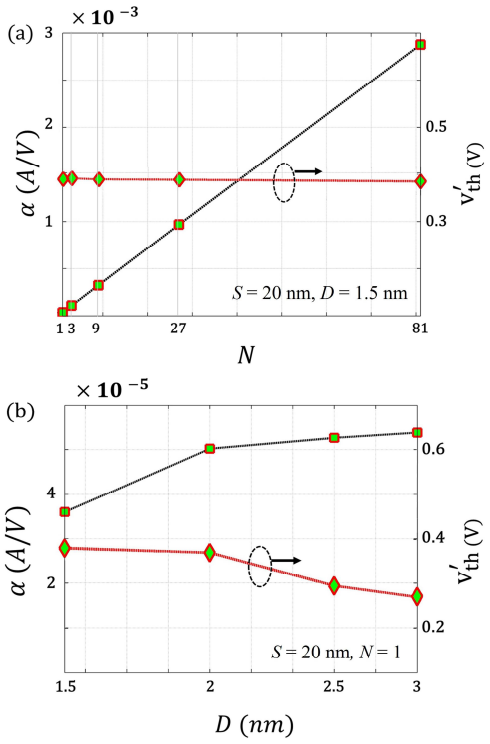

Fig. 4 Estimated coefficients α and v'_{th} for different, (a) N and (b) D.

III. OVERVIEW OF SHORT CHANNEL CNFET NOISE ANALYSIS

A qualitative noise analysis on a one channel CNFET based on the Stanford CNFET model is performed in [19]. However, one channel CNFET cannot afford the RF application requirements like current and power demands. Hence, it is needed that a multiple channel CNFET is considered from noise analysis point of view to satisfy these necessities. This section provides a noise analysis for the short channel CNFET with N channels based on the Stanford model by taking into account both the uncorrelated and correlated channels.

1. *Uncorrelated Channels*

As it is mentioned before, the CNFET channels are uncorrelated for S greater than 20 nm. In addition, two regions of saturation and triode are considered here.

A. Saturation Region

The saturation current in CNFETs is due to the invariance of carrier density while it appears in MOSFETs due to the pinch-off effect. Additionally, the short channel effect limiting the MOSFETs output resistance has no significant impact on the CNFETs. The simplified equivalent circuit of the CNFET

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based on the Stanford model is shown in Fig. 7 (a), where R_S and R_d represent the channel resistors at the source and drain regions, respectively, and r_o is the output resistance of the device which is near to 100 MΩ per channel [18], [25]. It should be noted that the contact resistor of source/drain metal electrode described in [18] is smaller than R_S/R_d. Furthermore, since the magnetic inductance is about four times smaller than the kinetic inductance, the magnetic inductance is ignored in the CNFET Stanford model. As a result, the contact resistors and magnetic inductance are not taken into account in the equivalent circuit. According to [18], the CNFET intrinsic channel, CNFET_L1, in conjunction with the drain and source regions, CNFET_L2, forms a one channel CNFET. The equivalent transconductance of the CNFET_L2 can be expressed as follows:

$$g_C = g_{\text{int}} / (1 + g_{\text{int}} R_S) \tag{19}$$

where g_c and g_{int} represent the CNFET_L2 and intrinsic transconductance, respectively. It is accepted that flicker and shot noises are the dominant noise sources in a short channel CNFET [19]. There are three main noise sources in the CNTFET_L2 consisting of the intrinsic channel equivalent noise (shot and flicker noises), and the doped channel drain/source region shot noises (Fig.7 (a)). However, the flicker noise is neglected at high frequencies because of its inverse relation with frequency. The equations of different noises per unit bandwidth can be expressed as below:

$$\overline{i_{n,\text{int}}^2} = 2qI_{D,L2}F + \frac{\alpha_H}{n}(I_{D,L2}^2 / f) \tag{20}$$

$$\overline{i_{n,R_S}^2} = 2qI_{D,L2}F_{dop} \tag{21}$$

$$\overline{i_{n,R_d}^2} = 2qI_{D,L2}F_{dop} \tag{22}$$

where $I_{D,L2}$, f, α_H, and n are the drain current of CNFET_L2, frequency, technology-dependent constant, and number of charge carriers in the semiconductor, respectively. Moreover, F_{dop} and F are doped and intrinsic channel's Fano factor, respectively. According to [19], α_H and F_{dop} are approximately equal to 10^{-4} and 0.3 by considering manufacturing results. On the other side, although there is no experimental results for intrinsic short channel shot noise, its theoritical model is widely reported in the litreture [26] in which F is between 0 and 1 for the saturation current and has a reverse relation to $I_{D,L2}$. By considering the high output impedance, the noise of R_d has no significant effect on the CNFET_L2 equivalent current noise, $i_{n,cht}$, shown in Fig. 7 (b). As a result, it can be expressed as below:

$$\overline{i_{n,cht}^2} = G_1\overline{i_{n,R_S}^2} + G_2\overline{i_{n,\text{int}}^2} \tag{23}$$

where G_1 and G_2 are the transfer gains which are equal to $(g_{int}R_s/(1+g_{int}R_S))^2$ and $(1/(1+g_{int}R_S))^2$, respectively.

The total current of the CNFET with N channels consists of the edge channels current, $I_{D,L2,e}$, and middle channels current, $I_{D,L2,m}$. Therefore, the equivalent noise includes two parts: edge channels noise, $i_{n,cht,e}$, and middle channels noise, $i_{n,cht,m}$, obtained by substituting edge Fano factor, F_e, edge intrinsic transconductance, $g_{int,e}$, and $I_{D,L2,e}$ as well as middle Fano factor, F_m, middle intrinsic transconductance, $g_{int,m}$, and $I_{D,L2,m}$

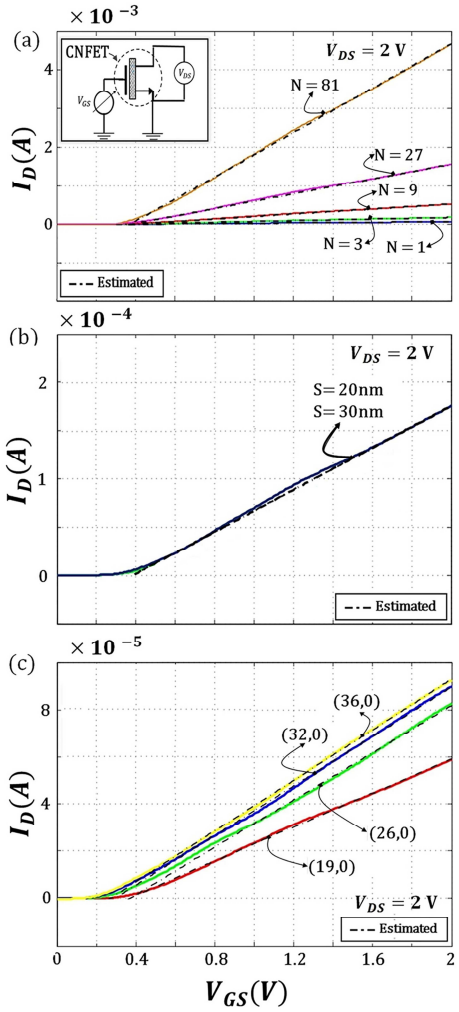

Fig. 5 Comparison between the estimated and Stanford model drain currents versus gate-source voltage of the CNFET for different (a) N (S=20 nm, D=1.5 nm), (b) S (D=1.5 nm, N=3), (c) D (S=20 nm, N=1).

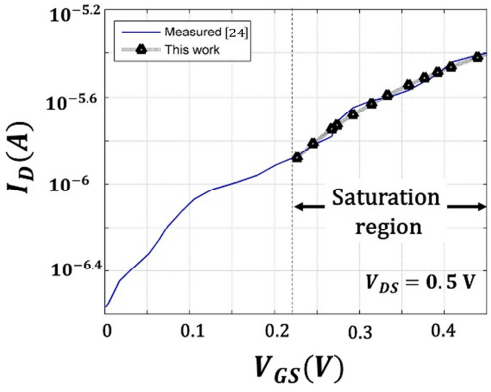

Fig. 6 Comparison between this work model and measurement results obtained from [24] (D=1.6 nm, N=1).

in Eqs. (20)-(23), respectively. As a result, total noise of the CNFET with N channels, $i_{n,tot}$, (Fig. 7 (c)), is equal to:

$$\overline{i_{n,tot}^2} = 2\overline{i_{n,cht,e}^2} + (N-2)\overline{i_{n,cht,m}^2} \tag{24}$$

However, for uncorrelated channels, $i_{n,cht,m}$ and $i_{n,cht,e}$ will be equal [10]. Therefore, total noise of the CNFET with N uncorrelated channels, $i_{n,tot,un}$, can be expressed as below:

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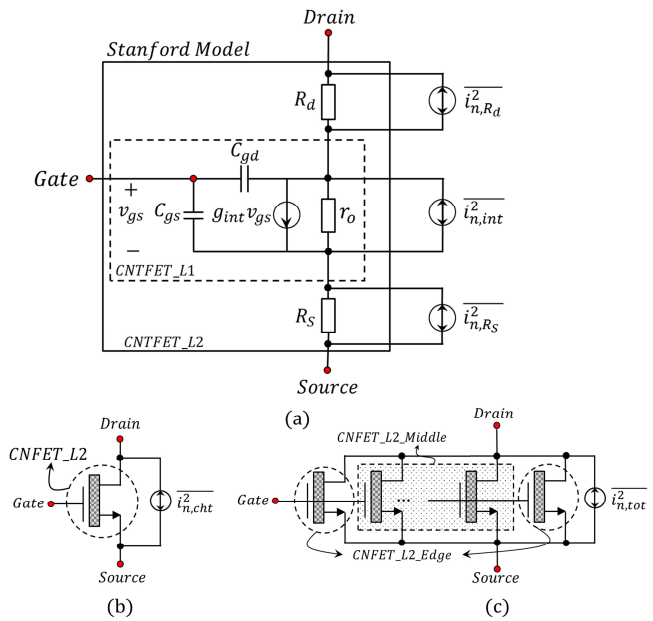

Fig. 7 (a) CNFET Small signal equivalent circuit and its internal noise current sources in the saturation region, (b) Equivalent compact noise source model considering the noise of CNFET_L2, (C) CNFET total noise sources with N channels.

$$\overline{i^2_{n,tot,un}} = N\overline{i^2_{n,cht}} \tag{25}$$

Substituting $I_{D,L2}=I_D/N$, where I_D is the current given by the closed-form I-V equation extracted in section II, and taking into account $q=KT/V_T$ (V_T is the thermal voltage), at high frequencies, (25) can be rewritten as below:

$$\overline{i^2_{n,tot,un}} = 4KTg_cNH_m \tag{26}$$

in which g_c is equal to $C_t v_{CNT}$ obtained from (14) and (18). In addition, the coefficient H_m is defined as below:

$$H_m = \left(\frac{V_{GS}-v'_{th}}{2V_T}\right)\left[\left(\frac{g_{int}R_s}{1+g_{int}R_s}\right)^2 F_{dop} + \left(\frac{1}{1+g_{int}R_s}\right)^2 F\right] \tag{27}$$

It is clear that H_m has a reverse relation to temperature, and hence, (26) is independent of temperature.

B. Triode Region

In the triode region, the intrinsic channel drain current has a linear behavior versus drain-source voltage. As a result, the intrinsic channel resistance R_{ds} will be decreased with respect to r_o. The CNFET small signal model based on the Stanford model in the triode region is shown in Fig. 8 [18]. The equivalent current noise can be calculated as below:

$$\begin{aligned}\overline{i^2_{n,cht}} = &\left[\frac{R_s}{R_d+R_{ds}+R_s}\right]^2\overline{i^2_{n,R_s}} + \left[\frac{R_{ds}}{R_d+R_{ds}+R_s}\right]^2\overline{i^2_{n,int}} \\ &+\left[\frac{R_d}{R_d+R_{ds}+R_s}\right]^2\overline{i^2_{n,R_d}}\end{aligned} \tag{28}$$

In addition, the total noise equation for N uncorrelated channels is as follows:

$$\overline{i^2_{n,cht}} = \frac{N}{(R_d+R_{ds}+R_s)^2}\left(R_s^2\overline{i^2_{n,R_s}} + R_{ds}^2\overline{i^2_{n,int}} + R_d^2\overline{i^2_{n,R_d}}\right) \tag{29}$$

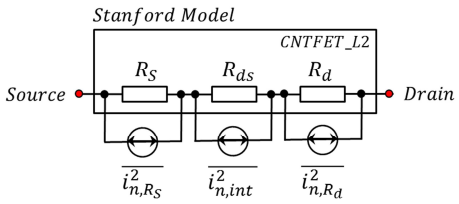

Fig. 8 CNFET Small-signal equivalent circuit and the internal noise current sources of the CNFET_L2 in the triode region.

If it is assumed that R_m is the total resistance of N uncorrelated channels of CNFET and by considering $R_{m,L2}$, the CNFET_L2 equivalent resistance, equal to $R_S+R_{ds}+R_d$ ($=NR_m$), $I_{D,L2}$ equal to I_D/N ($=V_{DS}/R_m$), and $q=KT/V_T$, and neglecting the flicker noise at high frequencies, (29) can be simplified as (30), in which, J_m is defined as (31).

$$\overline{i^2_{n,tot,un}} = 4KT\frac{1}{R_m}J_m \tag{30}$$

$$J_m = \frac{V_{DS}}{(2V_T)R_{m,L2}^2}\left[R_s^2F_{dop} + R_{ds}^2F + R_d^2F_{dop}\right] \tag{31}$$

For a similar reason, (30) has no temperature dependency due to the inverse relation between J_m and temperature.

2. Correlated Channels

The noise theoretical overview can be perused for correlated channels which their currents are influenced by neighboring channels current ($\eta_c \neq 0$). In this circumstances, by taking (6), (7), and (10) into account, the relation among $I_{D,L2,m}$ and $I_{D,L2,e}$ can be expressed as below:

$$I_{D,L2,m} = I_{D,L2,e}(1-\eta_c) \tag{32}$$

Because of this difference between the edge and middle channels current, F, G_1 and G_2 will change, too. With regards to (24) and by considering $G_{1,e}$, $G_{2,e}$ and $G_{1,m}$, $G_{2,m}$ as the transfer gains of edge and middle channels, respectively, and $\sigma=F_m-F_e$, $\Delta G_1=G_{1,m}-G_{1,e}$, and $\Delta G_2=G_{2,m}-G_{2,e}$, total noise of the CNFET with N correlated channels, $i_{n,tot,C}$, is achieved as (33).

$$\begin{aligned}\overline{i^2_{n,tot,C}} = &N\overline{i^2_{n,cht,e}} + (N-2)\eta_c\overline{i^2_{n,cht,e}} \\ &+2qI_{D,L2,e}(N-2)\left[(1-\eta_c)\sigma G_{2,e} + F_{dop}\Delta G_1 + F_e\Delta G_2 + \sigma\Delta G_2\right]\end{aligned} \tag{33}$$

As it is clear in (33), the correlated term of $i_{n,tot,C}$ corresponds to η_c, ΔG_1, ΔG_2, and σ. Hence, it is expected that (33) will become equal to (25) under uncorrelated situation when these factors proceed to zero.

IV. Broadband CNFET-Based LNA Design

LNA architectures are generally categorized to common-gate and common-source structures. The common-gate (CG) architecture demonstrates superior isolation and stability thanks to the lack of Miller effect of gate-drain capacitance, C_{gd}. In addition, due to its constant wideband input impedance, it can be considered as a good candidate for wide-band impedance matching, without using additional components, while preserving area consumption and avoiding from more resistance losses of on-chip inductors [27]. Beside the proper characteristics mentioned regarding the common-gate architecture, its noise performance is limited by the input

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matching condition due to fixing the device transconductance by the antenna output resistance. Therefore, noise reduction techniques are necessitated to be applied in order to improve the noise performance of CG LNAs for utilizing their wide bandwidth features [28]. There are some techniques to enhance the noise performance of the broadband LNAs (e.g., feedback and feedforward). The circuit noise is greatly dependent on the transconductance ratio of transistors (i.e., mismatch) in the feedforward techniques while this limitation is not significant in the feedback ones [29]. As a result, the negative feedback structure is used here to design the proposed broadband CNFET-based LNA.

The proposed broadband CNFET-based CG LNA topology is depicted in Fig. 9. It consists of two negative feedbacks which are applied by M_2 and M_3, while the signal is transferred towards the output by the common-gate transistor M_1. The common-source transistor M_2 boosts the transconductance of M_1. R_b sets the extra path to the power supply to compensate the difference in the transconductance of M_2 and M_3. Since, the total capacitance of the input device in the CNFET technology is very low over the bandwidth there is no need to any inductor over the large bandwidth such as 3 to 38 GHz. As a result, the resistor R_p is used here as the input terminal resistor instead of the conventional spiral inductors resulting in a broadband CNFET-based inductor-less CG LNA with reduced area. It is noticed that by carefully design of R_p, it is possible to reduce its noise effect. Moreover, transistor M_4, biased in triode region with equivalent resistance of R_L, provides an active load at the output terminal that used instead of conventional resistors to decrease the total noise. Finally, transistor M_5 buffers the output signal to provide a matching condition.

A. Input Impedance Matching

The in-band LNA impedance can be yield as (34):

$$Z_{in} = R_p \,||\, \frac{1+g_{m3}R_b(1+g_{m1}R_L)}{g_{m1}(1+g_{m3}R_b+g_{m2}R_b)} \,||\, \frac{1}{SC_{in}} \tag{34}$$

in which, C_{in} is due to the parasite capacitors at the input which is very low. g_{mi} denotes the total transconductance of transistor M_i which is equal to Ng_c for N uncorrelated channels. By assuming $g_{m3}R_b$ $(1+ g_{m1}R_L)$ and g_{m3} smaller than one and g_{m2}, respectively, and considering R_p at least 10 times than R_{Source} (source resistance), (34) can be simplified as:

$$Z_{in} = \frac{1}{g_{m1}(1+g_{m2}R_b)} \tag{35}$$

The input impedance Z_{in} should be equal to R_{source} for establishing the matching condition.

B. Gain and Bandwidth

As it is shown in Fig. 9, in terms of input impedance matching, the voltage gain from V_S to V_{out} can be calculated as follows:

$$A_V = \frac{g_{m1}R_L}{2}\left(\frac{g_{m2}+g_{m3}+1/R_b}{g_{m1}g_{m3}R_L+g_{m3}+1/R_b}\right) \tag{36}$$

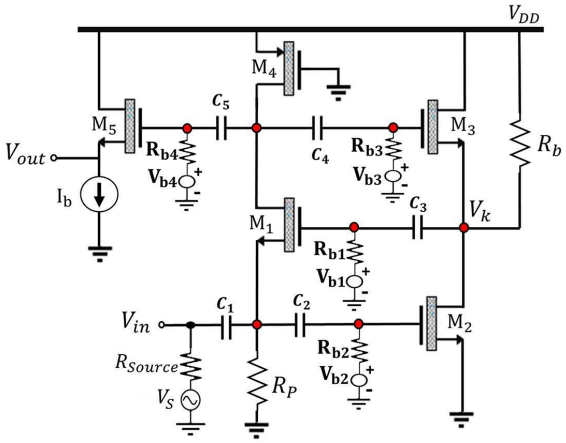

Fig. 9 Proposed broadband CNFET-based LNA topology.

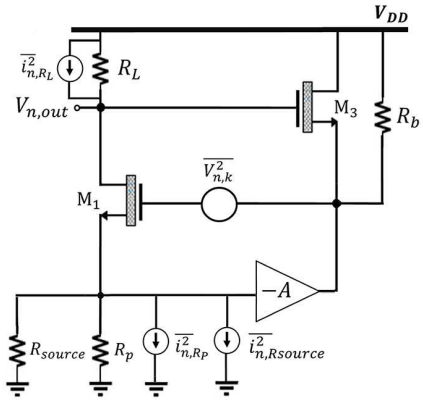

Fig. 10 Equivalent circuit with the noise sources.

According to the primary assumptions, (36) can be simplified as below:

$$A_V = \frac{1}{2}g_{m1}R_L(1+g_{m2}R_b) = \frac{R_L}{2R_{Source}} \tag{37}$$

Moreover, the bandwidth is equal to $1/(R_LC_P)$ in which C_P is the parasite capacitance at the drain of M_1. We expect a high bandwidth due to the quantum capacitors of the CNFET [17].

C. Noise Analysis

The circuit noise sources consist of the CNFETs channel noise and the thermal noise of resistors. To calculate the noise figure, the ratio of the total noise due to all noise sources and the noise due to the source resistance is needed.

The voltage gain V_k/V_{in} is calculated as below:

$$\frac{V_k}{V_{in}} = \frac{-g_{m2}+g_{m1}g_{m3}R_L}{1/R_b+g_{m3}(1+g_{m1}R_L)} = -g_{m2}R_b \tag{38}$$

Fig. 10 shows the equivalent circuit with its noise sources where the voltage gain A equals $g_{m2}R_b$ and the noises of M_1, M_2, M_3, and R_b are defined as an accumulated noise source $V_{n,k}$ at node k. In addition, the voltage gain $V_{n,out}/V_{n,k}$ can be calculated as follows:

$$\frac{V_{n,out}}{V_{n,k}} = \frac{-g_{m1}R_L}{g_{m1}R_{source}(1+A)+1} \tag{39}$$

Due to the matching condition, $R_{source}=(g_{m1}(1+A))^{-1}$, (39) is simplified as below:

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$$\frac{V_{n,out}}{V_{n,k}} = -g_{m1}\frac{R_L}{2} \tag{40}$$

The power spectral density of the noise components at the output of the first stage, the drain of M_1, within LNA's bandwidth can be obtained as follows:

$$\overline{V_{n,out}^2}\,|_{M1} = \left(\frac{\overline{i_{n,tot,un}^2}\,|_{M1}}{g_{m1}^{\ 2}}\right)\frac{(g_{m1}R_L)^2}{4} \tag{41}$$

$$\overline{V_{n,out}^2}\,|_{M2} = \left(\overline{i_{n,tot,un}^2}\,|_{M2}\ R_b^{\ 2}\right)\frac{(g_{m1}R_L)^2}{4} \tag{42}$$

$$\overline{V_{n,out}^2}\,|_{M3} = \left(\overline{i_{n,tot,un}^2}\,|_{M3}\ R_b^{\ 2}\right)\frac{(g_{m1}R_L)^2}{4} \tag{43}$$

$$\overline{V_{n,out}^2}\,|_{R_b} = (4KTR_b)\frac{(g_{m1}R_L)^2}{4} \tag{44}$$

$$\overline{V_{n,out}^2}\,|_{R_L} = 4KTJ_{m4}R_L \tag{45}$$

The thermal current noises of R_p and R_{source} are transferred to the output with the same power gain as follows:

$$\overline{V_{n,out}^2}\,|_{R_P} = \left(4KT\frac{1}{R_p}\right)\frac{R_L^{\ 2}}{4} \tag{46}$$

$$\overline{V_{n,out}^2}\,|_{R_{source}} = \left(4KT\frac{1}{R_{source}}\right)\frac{R_L^{\ 2}}{4} \tag{47}$$

Therefore, the noise figure is obtained as below:

$$\begin{aligned} NF &= 1 + \frac{\overline{V_{n,out}^2}\,|_{M1} + \overline{V_{n,out}^2}\,|_{M2} + \overline{V_{n,out}^2}\,|_{M3}}{\overline{V_{n,out}^2}\,|_{R_{source}}} \\ &+ \frac{\overline{V_{n,out}^2}\,|_{R_b} + \overline{V_{n,out}^2}\,|_{R_L} + \overline{V_{n,out}^2}\,|_{R_P}}{\overline{V_{n,out}^2}\,|_{R_{source}}} \\ &= 1 + \frac{H_{m1}}{(1+A)} + \frac{A^2H_{m2}}{g_{m2}R_{source}(1+A)^2} + \frac{A^2H_{m3}(g_{m3}/g_{m2})}{g_{m2}R_{source}(1+A)^2} \\ &+ \frac{R_b}{R_{source}(1+A)^2} + \frac{4J_{m4}R_{source}}{R_L} + \frac{R_{source}}{R_P} \end{aligned} \tag{48}$$

The circuit has been designed in a way that A or $g_{m2}R_b$ are much higher than one, thus the noise effects of M_1, M_2, M_3, and R_b on the noise figure would be insignificant. Moreover, the coefficients H_{m1}, H_{m2}, H_{m3}, and J_{m4} are less than one, and hence, they can reduce the noise figure. All in all, the most important noise sources are R_p and R_L which should be designed, accurately.

According to (20), there is a dependency among the intrinsic shot noise and F. On the other hand, NF is influenced by F. To determine this influence, the ratio of changes in NF (ΔNF) to the variations of F (ΔF) due to the circuit components M_1, M_2, M_3, and M_4 are expressed as (49):

$$\frac{\Delta NF}{\Delta F}\,|_{M_1} = \frac{V_{GS1} - \mathrm{v}'_{th1}}{2(1+A)(1+g_{\mathrm{int}1}R_{s1})^2V_T} \tag{49a}$$

$$\frac{\Delta NF}{\Delta F}\,|_{M_2} = \frac{A^2(V_{GS2} - \mathrm{v}'_{th2})}{2V_Tg_{m2}R_{source}(1+A)^2(1+g_{\mathrm{int}2}R_{s2})^2} \tag{49b}$$

$$\frac{\Delta NF}{\Delta F}\,|_{M_3} = \frac{A^2(g_{m3}/g_{m2})(V_{GS3} - \mathrm{v}'_{th3})}{2V_Tg_{m2}R_{source}(1+A)^2(1+g_{\mathrm{int}3}R_{s3})^2} \tag{49c}$$

$$\frac{\Delta NF}{\Delta F}\,|_{M_4} = \frac{4V_{DS4}R_{ds4}^{\ 2}R_{source}}{2V_TR_L(R_{m4,L2})^2} \tag{49d}$$

It is mentioned that, ΔNF is impressed a bit by ΔF in accord with the primary design assumptions expressed in this section.

V. Results

The broadband CNFET-based LNA is designed and characterized in HSPICE based on the 32 nm Stanford model [15] and 1 V power supply. Although the Stanford model is validated by experimental results [18], it has not any noise sources. As a result, its compact noise model presented in [19] is extended here for N channels CNFET and is taken into account via Veriloge-A for design of the LNA.

It is noted that, taking technological process into account for design parameters of CNFET devices is needed as practical aspects. Namely, although the CNT diameter variations and mispositioning of CNTs are considered as types of manufacturing process faults, the mechanism which is taken in [30] provides aligned arrays of CNTs perfectly while the diameters range from 0.5 to 3 nm within 10% standard deviations. In addition, although the diameter variations make unwanted metallic CNTs, they can be removed by thermocapillary resist as a promising approach [31]. Moreover, a majority of issues related to the fabrication process of CNFET has been solved and fabricated CNFETs are scaled down with minimum S equal to 4 nm [32]. On the other hand, increasing the CNTs density in the form of high performance CNFETs for the future electronics looks promising. For instance, the CNTs density is enlarged up to 45-55 CNTs/μm [33]. Due to these facts, it is significant to study the capability of systems designed in forthcoming technology. In this regard, the values of D, S, and CNTs density are set to 3 nm, 20 nm, and 51 CNTs/μm, respectively. The maximum transconductance per channel is reached by maximizing the practical diameter; hence, D is set to 3 nm. On the other hand, in order to have uncorrelated channels, S is set to 20 nm. As a result, the major design factor is the parameter N. In the design, we select the gate-source bias voltage; then the desired total current and transconductance can be obtained by selecting the proper N based on the acquired closed-form I-V equation. In this regard, the ratio of g_{m2}/g_{m3} is almost equal to N_2/N_3 in which N_2 and N_3 are the number of channels of the transistors M_2 and M_3, respectively. It is noted that N_2 is set to be considerably much greater than N_3. Alternatively, we set $g_{m3}R_b$=0.01 which is stemmed from R_b=40Ω and N_3=6. These terms lead us to reach our primary assumptions, i.e. $g_{m3}R_b(1+g_{m1}R_L) << 1$ and $g_{m3} << g_{m2}$. The design parameters and Stanford model technology configuration are listed in Tables II and III, respectively.

Fig. 11 illustrates $\Delta NF/\Delta F$ due to each component of the LNA. As it can be seen, small variation of F will not cause significant variation in ΔNF. For example, the variation of 0.1 for F will cause the maximum changes about 0.3 for $\Delta NF/\Delta F$. Thus, the ΔNF will be equal to 0.03 which cannot have a significant influence on the total NF.

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TABLE II
DESIGN PARAMETERS OF THE BROADBAND CNFET-BASED LNA

	CNFET Dimensions			Bias Sources		Operation Points (mA)		Cap. (pF)	Res. (Ω)
	N	S (nm)	D (nm)	Voltage (V)	Current (mA)	Simulation	Analytical		
M1	100	20	3	V_{b1} = 0.35	I_b = 2	I_{D1}= 0.216	I_{D1}= 0.218	C_1 = 5	R_P =500
M2	3100	20	3	V_{b2} = 0.3		I_{D2}= 14.4	I_{D2}=14.5	C_2 = 5	R_L =900
M3	6	20	3	V_{b3} = 0.8		I_{D3}= 0.038	I_{D3}= 0.036	C_3= 5	R_b=40
M4	23	20	3	V_{b4} = 0.3				C_4 = 5	
M5	450	20	3					C_5 = 5	

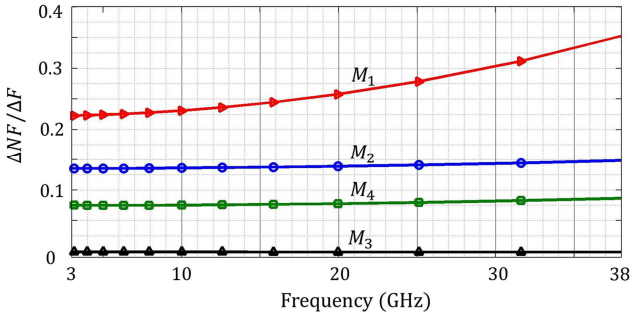

Fig. 11 The ratio of ΔNF to ΔF affected by each component of the LNA.

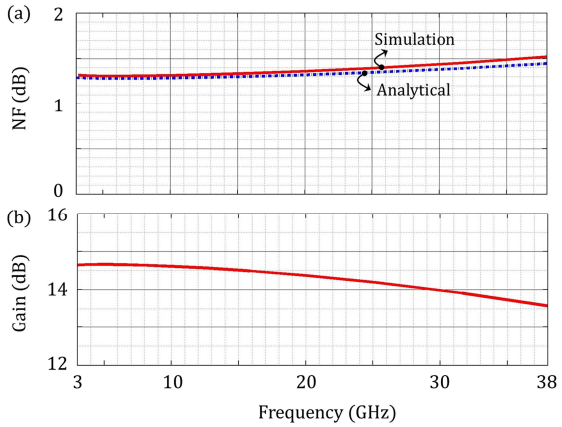

Fig. 12 Characterizations of the broadband CNFET-based LNA: (a) *NF*, and (b) Gain.

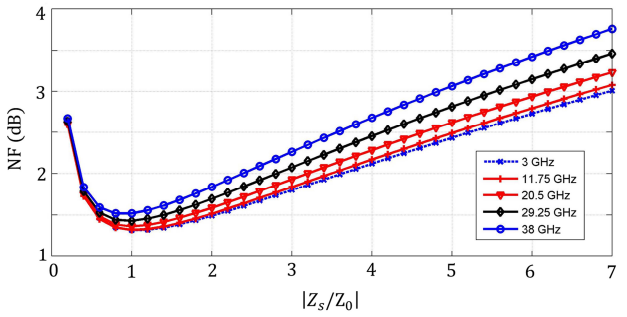

Fig. 13 Noise figure of the proposed LNA versus $|Z_s/Z_0|$.

The noise figure and gain of the LNA are shown in Fig. 12. Over the bandwidth (3 to 38 GHz); the noise figure is less than 1.5 dB and the gain equals 14.7 dB and drops just 1 dB over the entire bandwidth. In addition, there is an acceptable match between the analytical and simulation results. Fig. 13 shows the noise figure versus $|Z_s/Z_0|$ in which Z_s is the source impedance and Z_0 is equal to 50 Ω. As it is obvious, the optimum noise figure, NF_{min}, is acquired around the source impedance of 50 Ω, approximately.

TABLE III
TECHNOLOGY CONFIGURATION OF THE STANFORD MODEL

Parameters	Value
Chirality Vector	(38,0)
Power Supply	1 V
Gate Length	32 nm
Dielectric Constant	16
Doped Source Side Length	32 nm
Doped Drain Side Length	32 nm
Gate Dielectric Thickness	4 nm
Intrinsic CNT Mean Free Path	200 nm
Doped CNT Mean Free Path	12.5 nm
CNT Work Function	4.5 eV
Source/Drain Metal Contact Work Function	4.6 eV

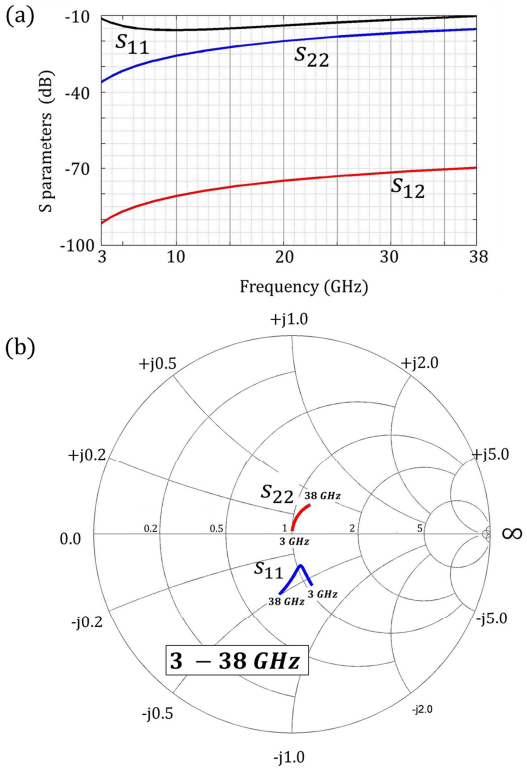

Fig. 14 Scattering parameters of the proposed broadband CNFET-based LNA: (a) S_{11}, S_{22}, and S_{12} and (b) Smith chart.

S_{11} and S_{22} are metrics of impedance matching with 50 Ω resistor at the input and output of the LNA, respectively. To make impedance matching at the output, a buffer is used which has insignificant effect on the gain while establishing a better matching. As it is illustrated in Fig. 14 (a), the paramet-

TABLE IV
PERFORMANCE OF THE BROADBAND CNFET-BASED LNA IN COMPARISON WITH OTHER WORKS

Ref.	[28]	[29]	[34]	This work
Technology	180 nm CMOS	180 nm CMOS	450 nm CNFET	32 nm CNFET
Data	Sim.	Exp.	Exp.	Sim.
Power supply(V)	1.8	1.8	2.5	1
P_{diss}(mW)	15.3	12.6	N.A.	16
IIP3(dBm)	-1.85	-0.7	-6	1.7
BW(GHz)	3-6	1.05-3.05	1-1.2	3-38
NF(dB)	3.5-3.6	2.6-3.1	8	0.4-1.3
S21(dB)	20.14-21	16.9	11	13.7-14.7
S11(dB)	< -11	< –10	< -10	< -10
S22(dB)	< -9	N.A.	< -18	< -15
Number of inductors	6	4	5	0
Total inductor	18.75 nH	N.A.	N.A.	0

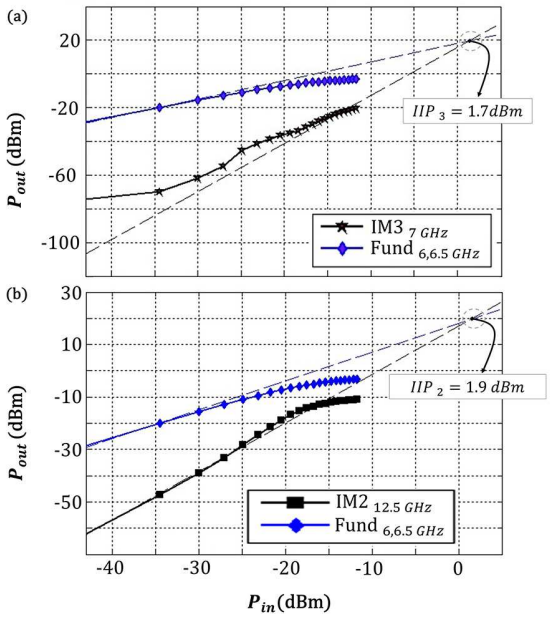

Fig. 15 Linearity characteristic of the broadband CNFET-based LNA: (a) IIP_3, and (b) IIP_2.

er at the entire frequency range, and hence, the system can be assumed as a unilateral device. As a result, the stability creteria can be obtained by checking $|S_{11}|$ and $|S_{22}|$. It is acceptable that in this circumstances, when $|S_{11}|$ and $|S_{22}|$ become less than 1, the system is likely unconditionally stable. Additionally, for taking the phase behaviour into account, S_{11} and S_{22} are displayed on the Smith chart (Fig. 14 (b)). These graphs are approximately located around the center of Smith chart where the reflection coefficient is zero.

The linearity parameters IIP_3 and IIP_2 of the proposed CNFET-based LNA are shown in Fig. 15. For this purpose, two frequencies of 6 GHz and 6.5 GHz are applied as the input signals of the LNA. As it can be seen, IIP_3 and IIP_2 of 1.7 dBm and 1.9 dBm have been reached.

In overall, Table IV lists the performance of the broadband CNFET-based LNA compared with recently published LNAs. The proposed circuit benefits from low *NF*, very high frequency range, and high linearity with moderate power consumption, while no passive spiral inductor has been utilized in its structure.

VI. CONCLUSION

This paper has presented the extraction of a closed-form I-V equation for short channel CNFETs in the saturation region based on the Stanford model and ballistic relation of one channel CNFET. After simplifying the ballistic relation to a closed-form I-V equation, the coefficients have been estimated by ICCAP and LS method. Furthermore, an extended quantitative noise analysis has been performed at the circuit level and the noise sources implemented in Verilog-A are added to the Stanford model. Afterward, a CNFET-based inductor-less broadband CG LNA is designed theoretically based upon the extracted I-V equation and its results confirmed in HSPICE based on the Stanford CNFET model indicate a proper matchnig between analysis and simulation.

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