Escola Tècnica Superior d'Enginyeria Industrial de Barcelona

DIGITAL CONTROL OF A RENEWABLE ENERGY RESOURCE INTERFACING THE DISTRIBUTION GRID

Master Final Thesis
Industrial Technologies Engineering

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Abstract

This project focuses on a power electronics unit composed by a boost converter and a three-phase inverter for use in a photovoltaic generation in grid-connected applications. The main aim is to build a setup with its software controller for educational purposes. To achieve this goal, a Digital Signal Controller of Texas Instruments has been used, which is in charge of the control. C code is employed for the controller, which generates the signals that rule the converters by doing measurements on key electrical variables and processing them according to the application objectives.

First of all, a complete theoretical analysis is made and a mathematical model of a system with a PV source the voltage level of which is boosted by a DC-DC boost convert and finally connected to the grid by a three-phase inverter.. This model is employed to design a suitable controller which is implemented on the DSC. To implement it, digital control and power electronics concepts are applied.

Once the digital controller is coded, the complete circuit is simulated with Typhoon HIL software, and simulations are carried out in a safe environment to ensure that controller works as desired. The goal of this activity is to check the suitability of the design in a safe environment, and study the system response with its similarities and differences with the modeled system.

Finally, the setup is prepared in the laboratory and experimental tests are carried out. The aim of the experimental tests is to show that controller works as desired and it can be used for educational purposes. Also, a study of the results is done to evaluate the performance of the controller. Each control loop is tested by applying steps on references variables and comparing the results with the theoretical values. These tests are carried on using different sampling and switching frequencies. MPPT algorithm is also tested to check if system can work permanently at MPP in different irradiance values.

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1. INTRODUCTION

1.1 Renewable Energy and Distributed Generation

Nowadays, the wide consumption of energy resources, most of which come from non-renewable sources of energy, presents the problem of finding new sources of energy that gradually replace non-renewable energy sources such as coal, oil or natural gas, the reserves of which may be exhausted in a near future. As a result of increasing environmental concerns, the use of green energy can be seen as a benefit to the global environment.

We could define renewable energies as those energies obtained from virtually inexhaustible natural sources, either because of the immense amount of energy they contain or because they are capable of regenerating by natural means.

Moreover, the development of populations far from central generation centers makes very interesting that the technology allows locating these sources of energy anywhere, without the need to create large infrastructures of transmission and distribution of electrical energy, due to the economic and environmental costs that these carry.

Thus, by bringing the generation points closer to the consumption points, the cost to supply the system, the energy losses, and the environmental impact are reduced, bringing an excellent solution for remote power needs. The paradigm that aims to solve this problem is the so-called distributed generation.

Renewable energies and their use in the system of distributed generation have the support of governments that try to favour their expansion. These policies also aim to regulate the generation and quality of service.

For these reasons, some sources of renewable energies such as photovoltaic solar energy provide an excellent solution for these problems, and therefore can be used for distributed power systems to offer electric power independently.

Industry efforts have focused increasingly on developing and building integrated photovoltaic and power plants for grid-connected applications. This field relies on a variety of manufacturing and installation industries for its development. These emerging renewable energy technologies, including solar energy, are still undergoing further development.

1.2 Photovoltaic Solar Energy

Photovoltaic solar energy is what the photovoltaic effect uses to generate energy, by the flow of electrons that a semiconductor material generates when the light strikes on him. This type of electricity generation is especially useful in places isolated to which the electricity does not arrive. However, its expansion as a source of power generation for the electrical network has been very fast during the last years, especially in countries like Germany.

The electricity generated by the photovoltaic (PV) systems can be either stored (using batteries) or used directly (stand-alone plant) by being fed into a large electricity grid powered by central generating plants (grid-connected or grid-tied plant). It can also be combined with one or many distributed/domestic electricity generators to feed into a small grid.

The solar cell is the element that converts photons from the sun into electricity. Solar cells are mainly junctions made of a semiconductor material. The energy of the photons, excite the electrons into solids up to higher energy states. The generated electrons (from the base) and holes (from the emitter) diffuse to the junction and are swept away by the electric field. These excited electrons generate a potential difference between the solar cell terminals.

The first silicon solar cell was reported in 1941, using melt grown junctions [1], with less than 1% of conversion efficiency. There is an evolution in 1954 [2], when the Bell lab discovered that silicon with some impurities was very sensitive to sunlight. Among the first applications was that of powering space satellites.

The excited electrons generate a potential difference or electromotive force between the solar cell terminals. The excited electrons quickly relax back to their ground state. However, the photovoltaic device is designed to pull the excited electrons out to feed an external circuit. The effectiveness of solar cell depends on the light absorbed by the materials so the surface is treated in order to reflect as little visible light as possible.

An individual solar cell provides low-voltage, thus it is needed to wire several cells to compose a photovoltaic module. This module needs weather-proof protections, mechanical connections, electrical power units, among other components to create a photovoltaic system.

Figure 1.1 shows a typical current-voltage curve (blue) and power-voltage curve (red). It is observed how it has a non-linear behavior. It can be defined by its V_{OC} (open-circuit voltage), I_{SC} (short-circuit current), and the MPP (maximum power point).

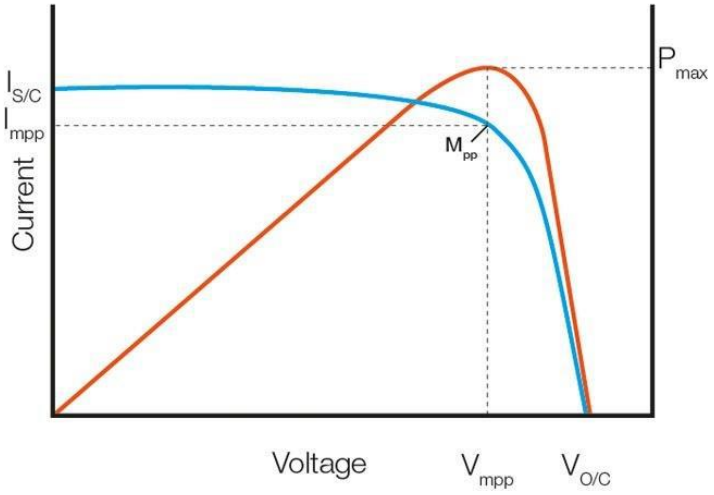

Figure 1.1: (I-V) curve and (P-V) curve of a solar cell *[3]*.

The efficiency of the solar panel improves as approaching to the MPP. For this reason, it is used an MPPT (maximum power point tracking), an algorithm that determines the panel operation voltage that allows maximum power output [4]. Therefore, MPPT is a key element to maximize the power production of a PV source.

Since PV source generates DC, to inject power into the grid it might be needed AC (e.g, grid-connected solar plant) which leads to a need of power electronics interface towards the grid. The power electronics converters are responsible for the energy conversion and for optimizing the energy transfer.

The system performance is managed by the power electronics interface by transferring safely the AC power into the grid. This power injection has to be stable and adapt to AC grid requirements.

1.3 Objectives

The main goal of the thesis is to model, simulate and implement a power electronics unit to interface a PV source with the AC grid. This is done by designing a controller that leads to an effective DC-AC energy conversion, synchronizes with the AC grid, and allows placing the working point on the MPP.

The first objective is modeling a system with a PV source the voltage level of which is boosted by a DC-DC boost convert and finally connected to the grid by a three-phase inverter. Also, it is necessary to do a study and model the modulation techniques to regulate the power converters. Once the system is modeled, the controller techniques are decided and mathematically designed with the needs of the system. Therefore, all control loops and MPPT algorithm are tuned.

The goal of simulating the system is to test controller performance and study the system response with its similarities and differences with the modeled system. Therefore, the objective is to match both mathematical and simulated performances, which means that modeling is done correctly and the controller is working as expected.

Finally, a very important objective is to be able to implement the controller in an experimental setup. With the material provided by the laboratory, the simulated system is built and can be tested. The goal of the tests is to demonstrate that the system works as desired. The algorithms are validated by comparing them with the results obtained from the modeling and simulations.

To carry on these tests in the laboratory without the need of external equipment, a PV source emulator has been used. This choice allows building a compact setup, which helps doing tests and giving multiple applications to it.

2. SYSTEM DESCRIPTION AND MODELING

This chapter provides an overview of the project and its structure. Once the system is introduced, the description and modeling of every part that has a role in the project are explained. PV source, boost converter, and three-phase inverter are described and modeled.

The modulation techniques used on each converter are introduced and the control strategy implemented is widely described considering parameters as grid filter, sampling and switching frequencies.

Figure 2.1 shows each element of the system, and how they are integrated. To be able to introduce the maximum power available from a PV source to the AC grid, this project considers using the following structures:

- PV source: it is the one in charge to generate electrical power with the energy from the sun. It is a non-linear DC source, its performance depends on many variables.
- Boost converter: although in this project it is used, it might not be necessary if the PV module is generating a voltage level high enough to be able to inject power into the AC grid. It is in charge of boosting the DC voltage from the PV source, in order to achieve the required DC voltage level for the three-phase inverter.
- Three-phase inverter: the aim of this converter is to generate AC current, which is injected on the three-phase AC grid.
- Grid filter: it is in charge of attenuating the switching frequency harmonics produced by the grid-connected inverter, i.e. filtering them.
- AC grid: it is modeled by a 4-quadrant source which in steady-state receives the power from the PV source and supplies it wherever of the grid it is needed.

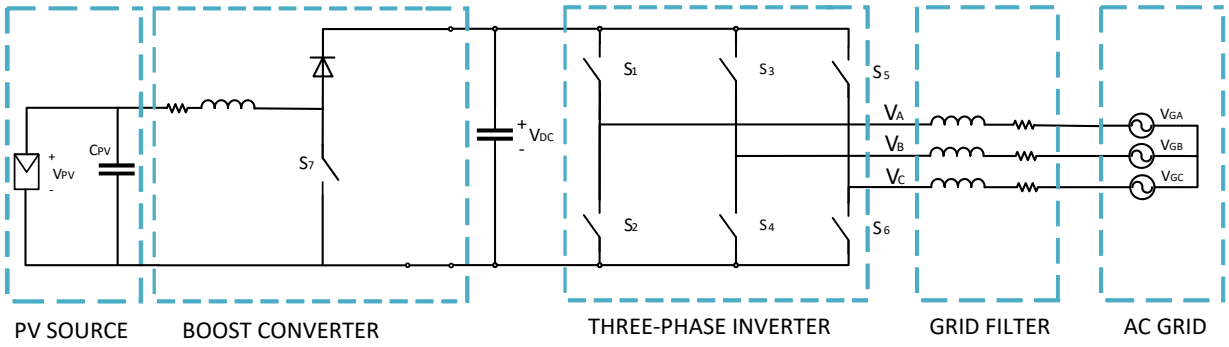

Figure 2.1: Electrical scheme of the experimental system.

The degrees of freedom for regulation come from the two converters used, composed of a total of seven switches. Therefore, on the control, it is assumed that AC grid and PV source are not controllable, as it is in a real system.

The overall control objective is to extract the maximum power that PV source can give, and with the maximum efficiency possible, inject it into the grid in good conditions. To carry out this strategy, PI controllers and closed loops are employed. Therefore, every part of the system must be modeled in order to carry on a stable and smart control.

2.1 Solar Cell Mathematical Model

The solar cell transforms the energy from the sun to electrical energy. This process can be represented by the equivalent electrical circuit [4] shown in Figure 2.2.

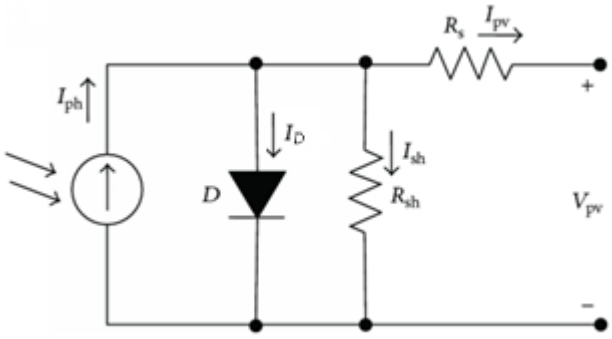

Figure 2.2: Equivalent electrical circuit of a PV source [4].

Where:

- I_{ph} is the photo current (source current). It depends on the irradiance (G) and the temperature (T).
- I_{sh} is the shunt resistance current. In an ideal solar cell, the shunt resistance could be considered equal to infinity.
- I_{pv} is the module current, which goes through the series resistance. This resistance could be considered equal to zero in an ideal solar cell.
- I_D is de diode current formed by the p-n junction of the cell.
- V_{pv} is the module voltage.

There is a relation between I_{pv} and V_{pv} which governs the behavior of the cell. This relation comes from the Kirchhoff's current law given by (2.1) [5].

$$I_{ph} = I_D + I_{sh} + I_{pv} \qquad \textit{Equation 2.1}$$

Where I_D and I_{sh} are given by (2.2) and (2.3).

$$I_D = I_o\left(e^{\frac{qI_{sh}R_S}{kT}} - 1\right) \qquad \textit{Equation 2.2}$$

$$I_{sh} = \frac{V_{pv}+I_{pv}R_S}{R_p} \qquad \textit{Equation 2.3}$$

Finally, the model is represented by the following equation (2.4).

$$I_{pv} = I_{ph} - I_o\left(e^{\frac{V_{pv}+I_{pv}R_S}{mV_T}} - 1\right) - \frac{V_{pv}+I_{pv}R_S}{R_p} \qquad \textit{Equation 2.4}$$

Where I_o is the reverse saturation current of the diode, V_T is the temperature voltage and T_{mod} is the module temperature. These are given by (2.5), (2.6) and (2.7), respectively.

$$I_o = C_o {T_{mod}}^3 e^{\frac{V_{gap}}{V_T}} \qquad \textit{Equation 2.5}$$

$$V_T = \frac{kT_{mod}}{q} \qquad \textit{Equation 2.6}$$

$$T_{mod} = T + \frac{c}{1000[\frac{W}{m^2}]}G \qquad \textit{Equation 2.7}$$

The solar cell is also characterized by its current-voltage curve and power-voltage curve. These curves determine the open circuit voltage and the short-circuit current, where no power is generated. The curves also determine the power, current and voltage at the point of maximum power.

In figure 2.3, the evolution of the current-voltage curve, as a function of the panel temperature or the solar irradiance can be observed.

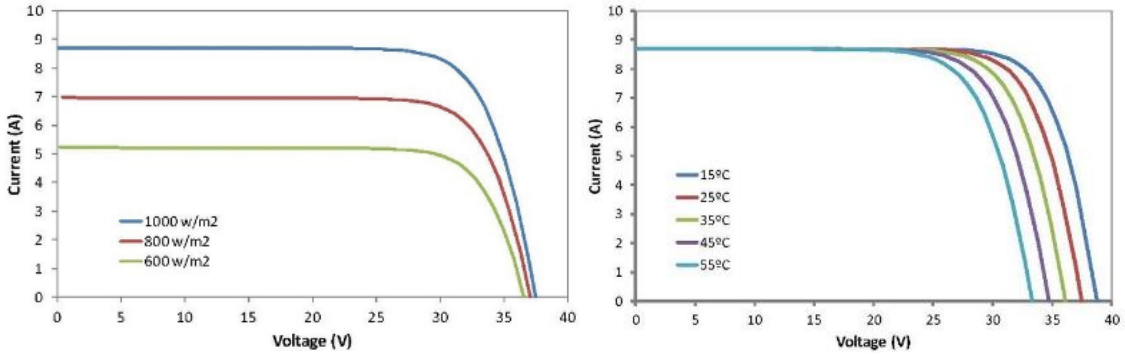

Figure 2.3: (I-V) curve under irradiance step (left) and under temperature step (right) [3].

The solar cell will have an efficiency determined by the power supplied by the dispositive divided by the power of the radiation incident upon it. The conditions under which efficiency is calculated must be carefully measured. The frequent conditions used are: irradiance 100mW/cm^2 and temperature 25°C [5].

2.1.1 Maximum Power Point Tracking (MPPT)

The MPPT is an algorithm which is the responsible for determining the panel operation voltage that allows maximum power output of the PV source. It has to work continually and be robust to changes in the environment, such as the temperature, irradiance or the load. With the appropriate use of this algorithm, extracted power from the module will be maximized.

To apply correctly the algorithm, measurements of I_{PV} y V_{PV} are needed. These variables will be the inputs of the calculation strategy to obtain the desired response. With the response, the algorithm will actuate on the DC/DC converter setting the V_{PV} required to maintain the maximum power point.

Different strategies exist. One of the most known and simplified strategy is called "Perturb and Observe" (P&O) [4]. The algorithm used to realize the MPPT strategy is shown in figure 2.4

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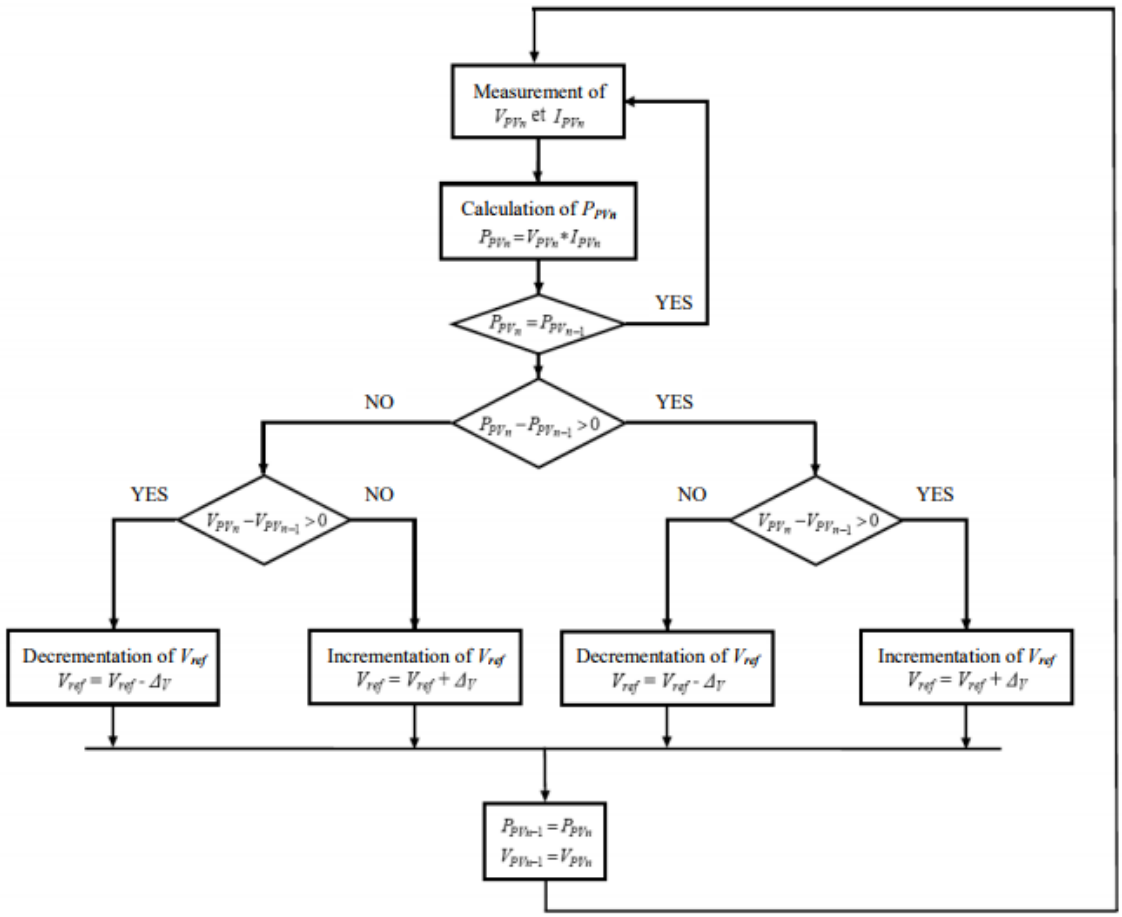

Figure 2.4: Block diagram of Perturb & Observe MPPT algorithm.

First, a perturbation is introduced in V_{PV} to notice the power variation which results from it by comparing the actual power with the power before the perturbation. The perturbation will be a fixed voltage step that can be either positive or negative. The value of the step must be studied as a big step will produce big oscillations and small step will slow down the algorithm. If a positive step of the voltage leads to a power increase, this means the obtained operating point is on the left of MPP, as shown in figure 2.5. Otherwise, the operating point is on the right of the MPP. Once the algorithm knows in which side of MPP is, a new perturbation of the required sign is generated.

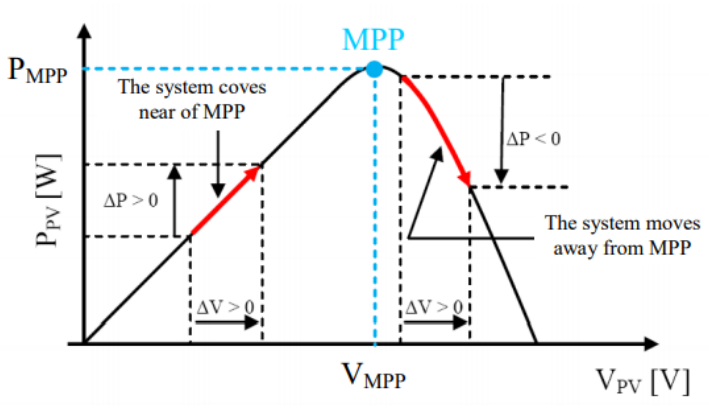

Figure 2.5: (P-V) curve of a solar cell with its Maximum Power Point.

Boost converter stage, which is described in the following chapter, will be regulated in order to modify Vpv in accordance with MPPT algorithm

2.2 Boost Converter

When it is needed to connect photovoltaic panels with the grid, it might be necessary to boost the output voltage of the panels to be able to introduce energy to the grid. With this purpose, it is interesting to use DC/DC converters which can help raising the voltage and also on keeping it stable. In this chapter, it is explained the boost converter that will be used in the system.

The Boost converter is a DC-DC step-up converter. Therefore, the output voltage will always be equal to or more than the input voltage. Its topology is shown in figure 2.6.

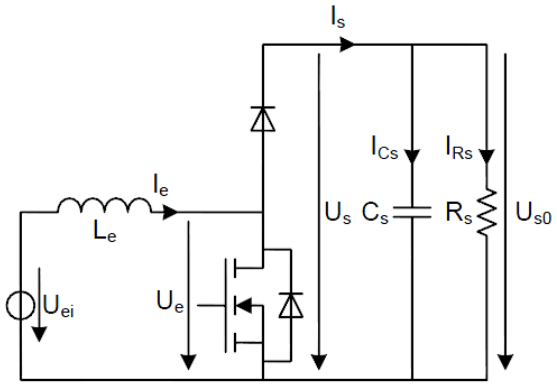

Figure 2.6: Electrical scheme of a boost converter [6].

When the switch is ON, the diode is OFF and inductor stores energy while capacitor releases stored energy supplying the load. When the switch is OFF, the diode is ON and the inductor releases while capacitor stores the energy. The average voltage over the inductor in one switching period must be zero as shown in (2.8).

$$\langle U_{Le} \rangle = \int_0^{T_s} V_L dt = 0 \qquad \textit{Equation 2.8}$$

Therefore the behavior of the boost converter is given by (2.9) and (2.10).

$$\langle U_{Le} \rangle = \frac{1}{T}\int_0^{DT} U_{ei} dt + \frac{1}{T}\int_{DT}^{T} (U_{ei} - U_{s0}) dt = U_{ei} D + (U_{ei} - U_{s0})(1 - D) = 0 \qquad \textit{Equation 2.9}$$

$$U_{s0} = U_{ei} \frac{1}{1-D} \qquad \textit{Equation 2.10}$$

To design properly the boost converter, some characteristics such as the input inductance, output capacitor, switching frequency and the duty cycle working range, are considered. This characteristic will give the inductor ripple and the output voltage, as shown in (2.11) and (2.12).

$$\Delta I_e = \frac{U_{ei}}{L_e f_s} D \qquad \textit{Equation 2.11}$$

$$\Delta U_{s0} = \frac{U_e}{R_s C_s f} \frac{D}{1-D} \qquad \textit{Equation 2.12}$$

2.2.1 Modulation Strategy

The used modulation technique is the Pulse-width modulation (PWM), which is a way of representing a signal as a pulse sequence. This modulation will be implemented by using a carrier signal and a reference signal. By modifying the value of the reference signal and fixing a frequency to the carrier signal, we can reach a different width of pulses as shown in figure 2.7.

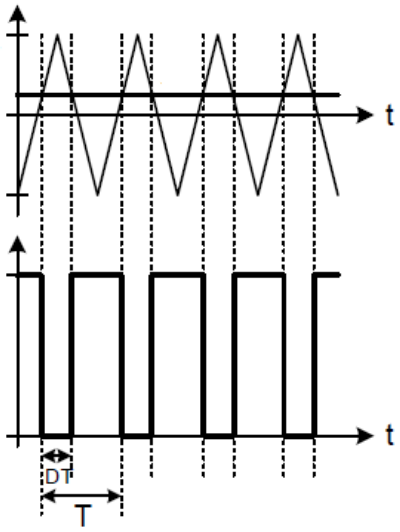

Figure 2.7: Carrier signal and comparator signal (up). Duty cycle (down).

The value of the reference signal is modified with the objective of carrying out the control. The goal of controlling the duty cycle of the boost converter is to extract the maximum power possible from the PV source, with the help of MPPT algorithm.

The boost converter is integrated into the system as shown in figure 2.1. The output of the converter is connected to the DC-link voltage and the input of the converter is connected to the PV source, through a capacitor.

2.3 Three-Phase Inverter

Once the PV source and boost converter are introduced, next step is the modeling of the three-phase inverter. As known, inversion is the process to change the DC input to an AC output with the desired current, voltage and frequency. There exists a wide variety of inverter topologies to inject power into the grid. In this project, the used inverter topology will be a two-level three-phase inverter.

This two-level three-phase grid connected inverter will be based on Insulated-Gate Bipolar Transistors (IGBT) which provides fast switching at a wide range of voltages. As the DC supply seen by the inverter is a voltage source (because of the DC-link capacitor), the DC-AC converter will be a Voltage Source Inverter (VSI), as shown in figure 2.8 [7].

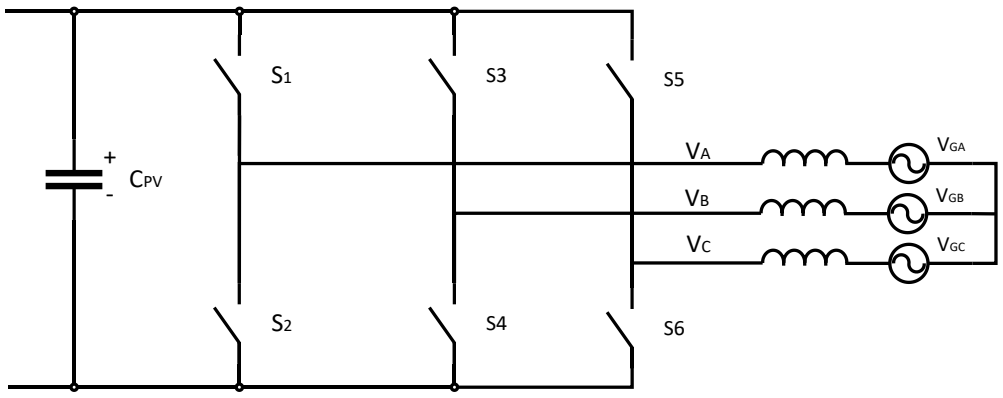

Figure 2.8: Scheme of a grid-connected VSI.

The main objective of the converter is to regulate energy exchange between the AC side and the DC side, by injecting to the grid the power extracted from the PV source

The DC side can be modeled as a voltage source or a current source connected to a shunt capacitor. The AC side is modeled as a three-phase AC voltage source connected to an RL filter which allows connecting to the inverter and reducing the harmonics injected into the grid.

Assuming that the L-filter is not ideal, and therefore it has an inductive and a resistive part (equal on each phase), the description of the system is given by (2.13).

$$V_A = Ri_A + L\frac{dI_A}{dt} + V_{GA}$$

$$V_B = Ri_B + L\frac{dI_B}{dt} + V_{GB} \qquad \textit{Equations 2.13}$$

$$V_C = Ri_C + L\frac{dI_C}{dt} + V_{GC}$$

In the following table 2.1, it is presented all the possible switching combinations and the voltages in each leg involved in every state, where 1 means upper switch is ON and lower switch is OFF, and 0 means the opposite. Switches in each leg are complementary, therefore only one switch of the same leg can be ON at each time, if not a short-circuit would occur.

	Leg_A	Leg_B	Leg_C	$V_{leg"A"}$	$V_{leg"B"}$	$V_{leg"C"}$
V_{000}	0	0	0	0	0	0
V_{100}	1	0	0	V_{DC}	0	0
V_{110}	1	1	0	V_{DC}	V_{DC}	0
V_{010}	0	1	0	0	V_{DC}	0
V_{011}	0	1	1	0	V_{DC}	V_{DC}
V_{001}	0	0	1	0	0	V_{DC}
V_{101}	1	0	1	V_{DC}	0	V_{DC}
V_{111}	1	1	1	V_{DC}	V_{DC}	V_{DC}

Table 2.1: Switching combinations for each space vector.

The VSC converter can apply the referenced voltages by modulating them using PWM. Multiple modulations technique exists in power converters. The modulation technique implemented is the SVPWM, which is explained below. To introduce SVPWM, Clarke and Park transformations must be described, as a key factor for carrying on the control.

2.3.1 Clarke Transform

Clarke transform is a useful tool for the analysis and modeling of three-phase electrical systems by transforming the three-phase system into a two-dimensional stationary reference frame [8]. It is normally used in balanced systems where the zero sequence component can be omitted to obtain the two-dimensional reference, as shown in (2.14), and its inverse is given by (2.15) [9].

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \qquad \textit{Equation 2.14}$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = {T_{\alpha\beta}}^{-1} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \qquad \textit{Equation 2.15}$$

This change of reference is due to a replace of the orthonormal base used as shown in figure 2.9 which allows to operate in a plane instead of a three-dimensional space, without any loss of information (in a three-wires system) [10].

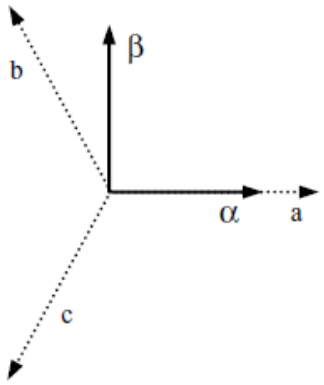

Figure 2.9: Vector diagram for Clarke transformation.

This transformation will be exact while the zero sequence component is equal to zero, if not a loss of information would take place. Zero sequence component can be omitted as it is assumed that following equation (2.16) is satisfied.

$$V_a + V_b + V_c = 0 \qquad \textit{Equation 2.16}$$

2.3.2 Park Transform

To take the maximum advantage from the Park transformation which will be applied on the current control, it might be interesting the implementation of a rotating reference frame, to simplify the analysis of the system and improve the control.

To change from a static reference frame to a rotating reference frame, the Park transformation is implemented. This new reference, known as *dq* reference, will rotate in the αβ reference frame at a certain frequency, as shown in figure 2.10.

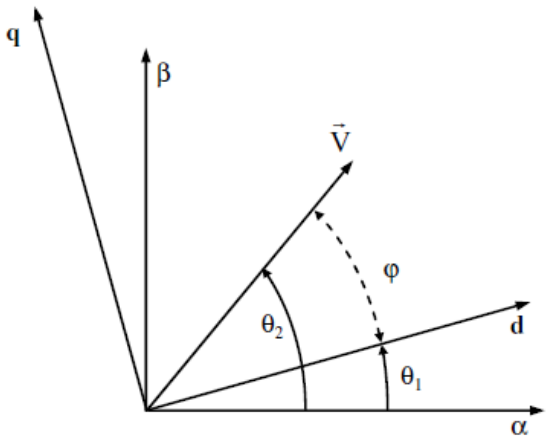

Figure 2.10: Vector diagrams for Park's transformation.

If the frequency of the rotating frame equals to the fundamental frequency of the three-phase system voltages, in the *dq* reference frame the angle and length of the voltage vector, will be constants, changing the AC system to a DC system [10].

The mathematical expression of this transformation is given by (2.17).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T_{dq} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \qquad \textit{Equation 2.17}$$

And its inverse, given by (2.18).

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = T_{dq} \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \qquad \textit{Equation 2.18}$$

Also, there is the possibility to express both transformations on one simple matrix transformation, as shown in equation (2.19) an its inverse in equation (2.20).

$$\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} cos\theta & -sin\theta \\ cos(\theta - \frac{2\pi}{3}) & -sin(\theta - \frac{2\pi}{3}) \\ cos(\theta + \frac{2\pi}{3}) & -sin(\theta + \frac{2\pi}{3}) \end{pmatrix} \begin{pmatrix} i_o \\ i_d \\ i_q \end{pmatrix} \qquad \textit{Equation 2.19}$$

$$\begin{pmatrix} i_o \\ i_d \\ i_q \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1/2 & 1/2 \\ cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ -sin(\theta - \frac{2\pi}{3}) & -sin(\theta + \frac{2\pi}{3}) \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \qquad \textit{Equation 2.20}$$

2.3.3 SVPWM Modulation Strategy

The space vector technique is a frequently used method to implement PWM in three-phase inverter control systems. It allows a more efficient use of DC link voltage by a harmonic injection mechanism.

The idea behind space vector modulation is to represent a three-phase voltage in the α β reference frame omitting zero-sequence component, using Clarke transformation. This representation is done by using a combination of switching states corresponding to the basic space vectors. On average, the superposition of these states in a modulation period will be equal to the desired voltage, as shown in figure 2.11 [8].

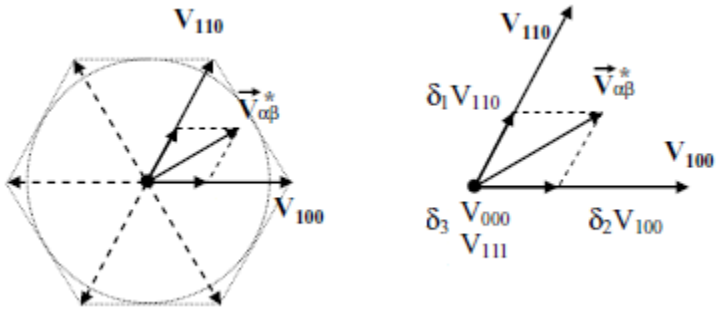

Figure 2.11 Voltage reference vector by superposition of inverter output vectors.

The desired vector is generated with the projection of the two closest states. Each state will be implemented in a fraction of the modulation period depending on the position of $V_{\alpha\beta}$ and its amplitude [11]. These fractions of time calculations are given by (2.21).

$$V_{\alpha\beta} \cdot T_s = V_{110} \cdot \delta_1 + V_{100} \cdot \delta_2 \qquad \textit{Equation 2.21}$$

If the application times are smaller than T_s the remaining time will be conferred to zero-space vectors as shown in (2.22) and (2.23).

$$V_{\alpha\beta} \cdot T_s = V_{110} \cdot \delta_1 + V_{100} \cdot \delta_2 + V_{111} \cdot \frac{\delta_3}{2} + V_{000} \cdot \frac{\delta_3}{2} \qquad \textit{Equation 2.22}$$

$$T_s = \delta_1 + \delta_2 + \delta_3 \qquad \textit{Equation 2.23}$$

The possible output voltage vector states given by a three-phase inverter are given by table 2.2.

	Leg_A	Leg_B	Leg_C	V_a	V_b	V_c
V_{000}	0	0	0	0	0	0
V_{100}	1	0	0	$2V_{DC}/3$	$-V_{DC}/3$	$-V_{DC}/3$
V_{110}	1	1	0	$V_{DC}/3$	$V_{DC}/3$	$-2V_{DC}/3$
V_{010}	0	1	0	$-V_{DC}/3$	$2V_{DC}/3$	$-V_{DC}/3$
V_{011}	0	1	1	$-2V_{DC}/3$	$V_{DC}/3$	$V_{DC}/3$
V_{001}	0	0	1	$-V_{DC}/3$	$-V_{DC}/3$	$2V_{DC}/3$
V_{101}	1	0	1	$V_{DC}/3$	$-2V_{DC}/3$	$V_{DC}/3$
V_{111}	1	1	1	0	0	0

Table 2.2: Ouput voltage vector on reference abc, for each possible estate.

Applying Clarke transformation shown in (2.24), it is obtained the value of the space vectors in the $\alpha\beta$ plane, which is given by (2.25).

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = T_{\alpha\beta}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \qquad \textit{Equation 2.24}$$

$$V_{\alpha\beta} = \frac{2}{3}V_{DC}e^{j\theta} = \frac{4}{3}\frac{V_{DC}}{2}e^{j\theta} \qquad \textit{Equation 2.25}$$

Which applied to each space vector after normalization of the space vectors with $\frac{V_{DC}}{2}$, results in (2.26):

$$V_{000} = V_{111} = 0$$

$$V_{100} = \frac{2}{3}V_{DC} = \frac{4}{3}$$

$$V_{110} = \frac{2}{3}V_{DC}e^{j\pi/3} = \frac{4}{3}e^{j\pi/3}$$

$$V_{010} = \frac{2}{3}V_{DC}e^{j2\pi/3} = \frac{4}{3}e^{j2\pi/3} \qquad \textit{Equations 2.26}$$

$$V_{011} = \frac{2}{3}V_{DC}e^{j3\pi/3} = \frac{4}{3}e^{j3\pi/3}$$

$$V_{001} = \frac{2}{3}V_{DC}e^{j4\pi/3} = \frac{4}{3}e^{j4\pi/3}$$

$$V_{101} = \frac{2}{3} V_{DC} e^{j5\pi/3} = \frac{4}{3} e^{j5\pi/3}$$

Therefore, using the expression presented in (2.21) it becomes easy to calculate the fraction period for each space vector, as shown in (2.27) and (2.28) [11].

$$\frac{4}{3} e^{j\theta} \cdot T_s = \frac{4}{3} e^{j\pi/3} \cdot \delta_1 + \frac{4}{3} \cdot \delta_2 \qquad \textit{Equation 2.27}$$

$$\begin{cases} \frac{4}{3} cos\,\theta = \frac{4}{3} cos\,\pi/3 \cdot \delta_1 + \frac{4}{3} \cdot \delta_2 \\ \frac{4}{3} sin\,\theta = \frac{4}{3} sin\,\pi/3 \cdot \delta_1 + 0 \cdot \delta_2 \end{cases} \qquad \textit{Equations 2.28}$$

The maximum amplitude of the rotating vector that can be generated by the inverter is represented by the inscribed circle in the $\alpha\beta$ plane. A vector partially outside the circle (overmodulation), will generate a sum of times greater than the modulation period, saturating the inverter and causing distortions in the output voltage when applying them.

This saturation level can be quantified with the modulation index, which is defined as (2.29) and (2.30).

$$M = \frac{V_m}{V_{DC}/2} \qquad \textit{Equation 2.29}$$

$$V_m = \frac{4}{3} \frac{V_{DC}}{2} cos\,\pi/6 = \frac{4}{3} \frac{\sqrt{3}}{2} \frac{V_{DC}}{2} = 1.1547 \frac{V_{DC}}{2} \qquad \textit{Equation 2.30}$$

Once the application times have been calculated, the next question is in which order in time should be applied this space vectors. On every modulation period will exist 4 different spaces vectors, which lead to multiple possible switching sequences.

In this project, the implemented sequence is the symmetrical switching sequence that allows minimizing the number of commutations and therefore the switching losses [12]. Symmetrical switching sequence imposes to start and finish with V_{000} and set in the middle of the sequence vector V_{111}. The order of the other two vectors is decided with the aim of reducing the number of commutations.

2.4 Control Strategy

As already introduced, the main goal of the control is to inject properly to the grid the power maximum power possible from a PV source. To achieve this goal, the controller must be stable and robust to changes and perturbations.

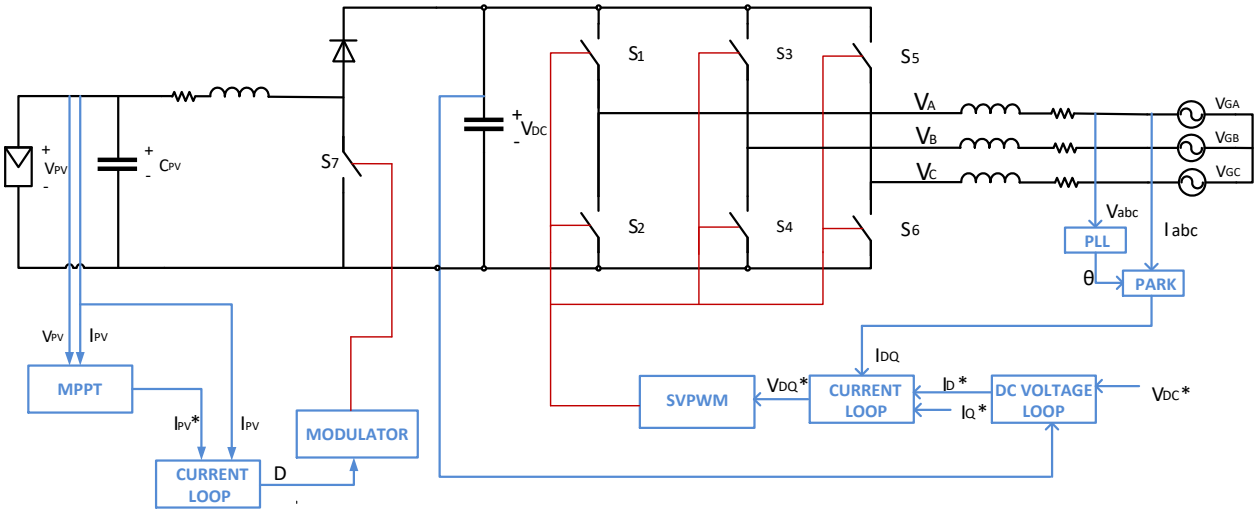

Figure 2.12: General control scheme of the system.

In figure 2.12, the general control scheme implemented on the controller is presented [13]. The controller will have a total of 4 loops, DC voltage loop, AC current loop, DC current loop, and the PLL loop. DC voltage and AC current loops will be in a cascade configuration, while the other two loops are working independently. Also, a total amount of 7 switches must be commanded to achieve the desired response.

Firstly, the AC side control will be described, starting from PLL loop. The controller will take advantage of the Clarke and Park transformations to operate in two variables instead of three. The VSI will control two electrical variables in *dq0* frame, in order to control separately the active and reactive power.

The control scheme of the inverter is based on a two-level cascaded control system. The lower level controller is the grid current control, which regulates the AC current injected into the grid in the *dq0* frame. This controller sends a reference of the voltages to the inverter and by generating an SVPWM sequence the desired AC current will be injected properly into the grid.

The higher level controller is in charge of regulating the DC-link voltage. The DC-link voltage controller generates a reference of AC current to inject on the grid, in order to maintain the power balance.

As the system is working in a rotating frame, the Phase Locked Loop (PLL) is needed to track the grid angle and achieve grid synchronization.

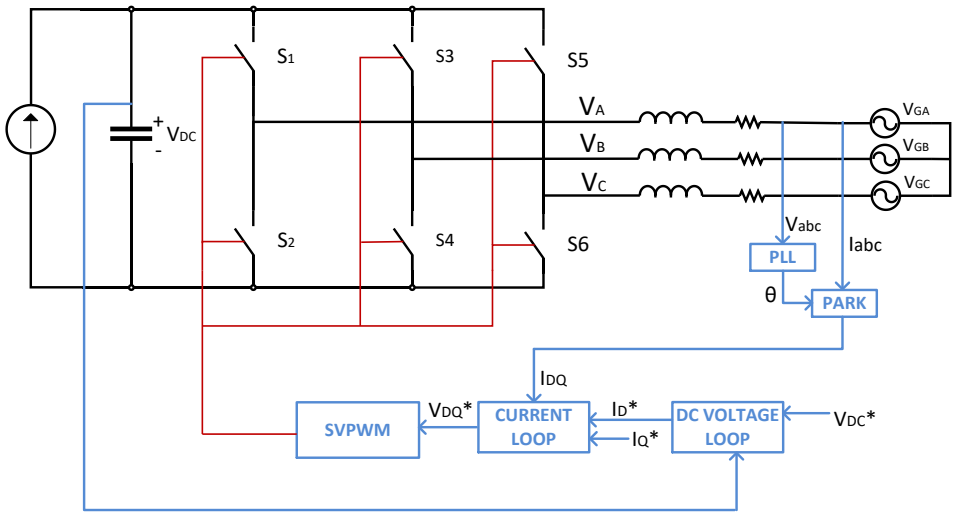

Figure 2.13: Control general scheme implemented on the AC side.

Figure 2.13 shows the control general scheme implemented on the AC side. While modeling the AC side, the source is represented as a DC current source, as this part of the control is developed afterward.

2.4.1 Phase Locked Loop

A phase-locked loop (PLL) is a closed-loop system in which an internal oscillator is controlled to keep the time of some external periodical signal by using the feedback loop [13]. It is a necessary tool for grid-connected power converters to work in harmony with the grid.

The PLL provides information about the phase-angle, frequency and amplitude of the magnitude of interest, in this case, the grid voltage. It must be robust against grid disturbances, as grid conditions are not constant. Moreover, it is useful compensating the delays introduced by the elements acting and sensing, just by advancing the phase-angle.

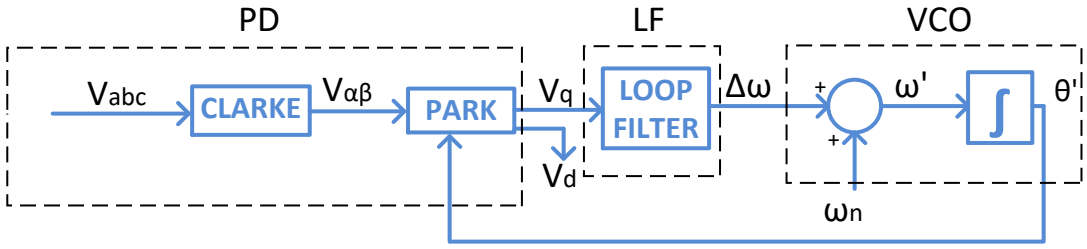

Figure 2.14: Block diagram of the PLL strategy used.

Figure 2.14 shows the block diagram of the PLL implemented. And it consists of three fundamental blocks:

- The phase detector (PD). This PD is based on a quadrature signal generator (QSG) and park transformation. The QSG consists of the Clarke transformation, and the input voltage is given by (2.31), and once QSG is applied, its output is given by (2.32).

$$\vec{v}_{abc} = V \begin{bmatrix} sin(\omega t + \phi) \\ sin(\omega t - \frac{2\pi}{3} + \phi) \\ sin(\omega t - \frac{4\pi}{3} + \phi) \end{bmatrix} \qquad \textit{Equation 2.31}$$

$$v_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V \begin{bmatrix} sin(\theta) \\ cos(\theta) \end{bmatrix} \qquad \textit{Equation 2.32}$$

By substituting (2.31) with the park transformation given by (2.33), it is obtained the output of the phase detector (2.34).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T_{dq} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta' & sin\theta' \\ -sin\theta' & cos\theta' \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad \textit{Equation 2.33}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} V \begin{bmatrix} sin(\theta - \theta') \\ -cos(\theta - \theta') \end{bmatrix} \quad \textit{Equation 2.34}$$

When the PLL is well locked$(\omega \approx \omega')$, the voltage vector will be free of oscillations.

- The loop filter (LF). This block is constituted by a PI controller and will drive its input to zero. In the presented case, the LF is placed on q-axis, aligning the grid voltage space vector with d-axis. The output of the LF is given by (2.35) [14].

$$\Delta\omega = \frac{2}{3} V \left(-sin\left(\theta - \theta^{'}\right)\right) * \left[K_p + \frac{K_i}{S}\right] \quad \textit{Equation 2.35}$$

The loop filter given by (2.35) will be implemented by the following equations.

$$IA_0 = K_i T_s V_{q1} + IA_1 \quad \textit{Equation 2.36}$$

$$\Delta\omega = K_p V_{q0} + IA_0 \quad \textit{Equation 2.37}$$

Where IA_0 is the actual Integral Action, IA_1 is the previous integral action, V_{q0} is the actual voltage, V_{q1} is the previous voltage and T_s is the update period.

- The Voltage Controller Oscillator (VGO). This block generates at its output an AC signal whose frequency is shifted with respect to a given central frequency. Its output is given by (2.38).

$$\theta' = \int (\omega_n + \Delta\omega) dt \quad \textit{Equation 2.38}$$

2.4.2 Current Loop Control

The grid current must be controlled in order to control active and reactive power exchange. This is done by sending a signal to the modulator which applying SVPWM, mentioned previously, will generate the appropriate voltage signal by driving the switches of the converter.

As mentioned, the AC voltage equations are given by (2.39). These equations can also be developed in αβ frame as shown in (2.40).

$$\begin{cases} V_A = Ri_A + L\frac{dI_A}{dt} + V_{GA} \\ V_B = Ri_B + L\frac{dI_B}{dt} + V_{GB} \\ V_C = Ri_C + L\frac{dI_C}{dt} + V_{GC} \end{cases}$$ *Equations 2.39*

$$\vec{V}_{\alpha\beta} = R\vec{i}_{\alpha\beta} + L\frac{d\vec{i}_{\alpha\beta}}{dt} + \vec{V}_{g\alpha\beta}$$ *Equation 2.40*

To be able to work with constants values, it is necessary to work on *dq* frame using park transformation. The obtained equations of the model in *dq* are presented as one complex equation in (2.41) or as two real equations with a coupling between them, shown in (2.42).

$$\vec{V}_{dq} = R\vec{i}_{dq} + L\frac{di_{dq}}{dt} + j\omega L\vec{i}_{dq} + \vec{V}_{gdq}$$ *Equation 2.41*

$$\begin{cases} \frac{di_d}{dt} - \omega i_q = \frac{1}{L}\left[-Ri_d - V_{gd} + V_d\right] \\ \frac{di_q}{dt} - \omega i_d = \frac{1}{L}\left[-Ri_q - V_{gq} + V_q\right] \end{cases}$$ *Equations 2.42*

To design the controller, an approach will be used decoupling and controlling both currents separately. The current loop of the PI controller is shown in figure 2.15 [13].

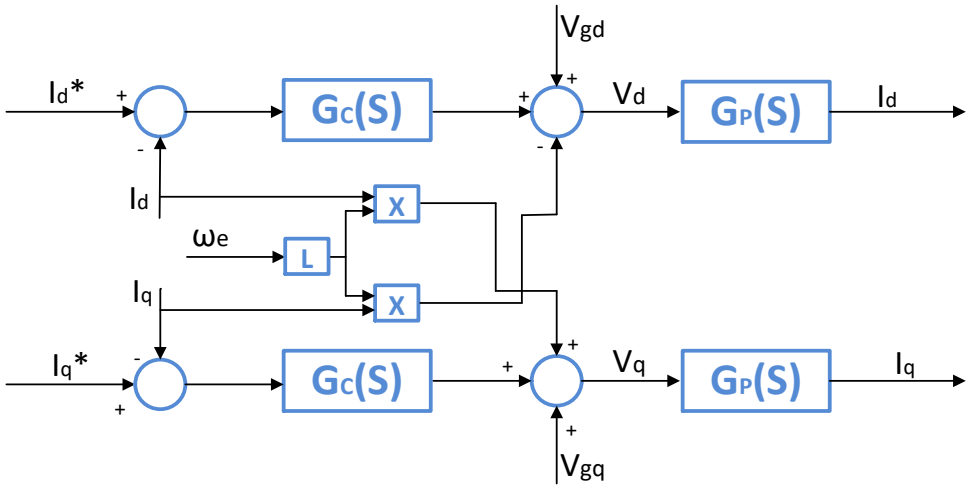

Figure 2.15: Block diagram of the current loop controller.

$G_c(s)$ is the transfer function of the controller and $G_p(s)$ is the transfer function of the filter in the Laplace domain, given by (2.43) and (2.44).

$$G_c(s) = k_p\left(1 + \frac{1}{sT_i}\right) \qquad \textit{Equation 2.43}$$

$$G_p(s) = \frac{1}{R+Ls} \qquad \textit{Equation 2.44}$$

2.4.3 Tuning Procedure of the PI Controller

PI (Proportional –Integral) controllers are probably the most common type of controllers in industrial power electronics. The PI controller may be implemented in either of two configurations: parallel or series [15], shown in figure 2.16.

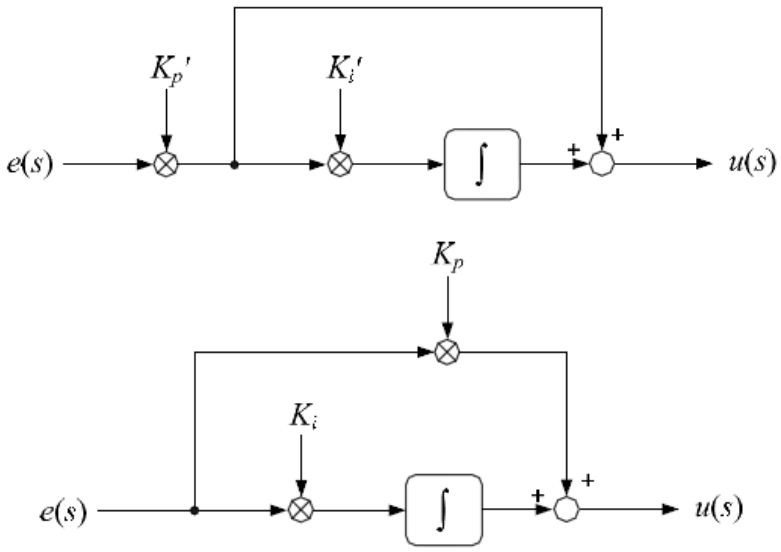

Figure 2.16: PI controller with parallel configuration (up)and series configuration (down).

Series configuration is the chosen method to implement. This configuration cannot be used in applications where zero proportional gain is required. As the controller is applied by a DSC, the controller will work on a discrete time, with a sampling period T_s. The behavior of the controller is given by the following equations.

$$U_p(k) = K_p e(k) \qquad \textit{Equation 2.45}$$

$$U_i(k) = U_i(k-1) + K_p \frac{T_s}{T_i} e(k) \qquad \textit{Equation 2.46}$$

$$U(k) = U_p(k) + U_i(k) \qquad \textit{Equation 2.47}$$

Tuning procedure of the PI controller is done by applying the Internal Model Control (IMC) method. Figure 2.17 shows the classical structure (above) with the IMC structure (below), where it is seen that IMC uses an internal model G*(s) in parallel with the controlled system G(s) [16].

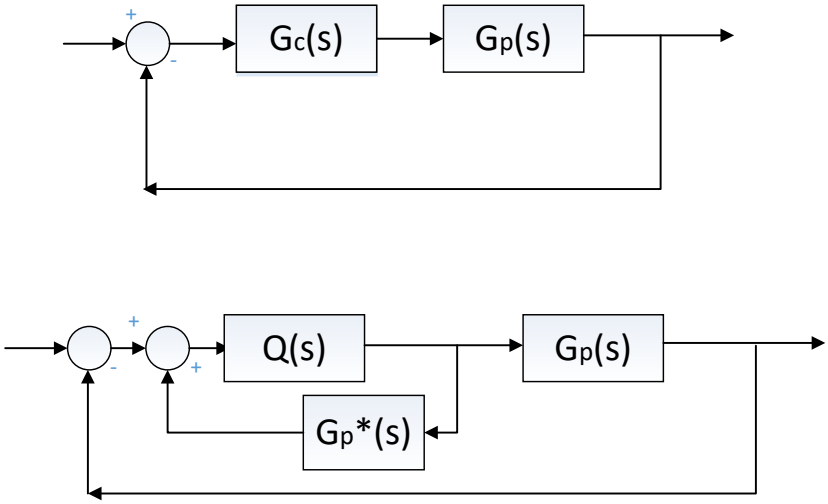

Figure 2.17 Classical control structure (up) and IMC structure (below).

As G(s) behaves as a first-order system, the controller Q(s) is defined as (2.48).

$$Q(s) = G_p(s)^{-1}L(s) \qquad \textit{Equation 2.48}$$

Where L(s) is a low-pass filter (2.49).

$$L(s) = \frac{\alpha}{s+\alpha}I \qquad \textit{Equation 2.49}$$

As a first-order system, the rise time will be related to α, the desired bandwidth. Applying these concepts, the equation of the controller is (2.50).

$$G_c(s) = \left[1 - Q(s){G_p}^*(s)\right]^{-1}Q(s) = \frac{Q(s)}{I - Q(s)\cdot G_p(s)^*} \qquad \textit{Equation 2.50}$$

To obtain a integral action, $\left[I - Q(s){G_p}^*(s)\right]^{-1}$ should be zero, so $Q(s){G_p}^*(s)$ should be equal to I. Unifying (2.48) and (2.50) it is obtained the equation of the controller $G_c(s)$(2.51) [16].

$$G_c(s) = \left[1 - \frac{\alpha}{s+\alpha}\right]^{-1} {G_p}^{-1}(s)\frac{\alpha}{s+\alpha} = \frac{\alpha}{s}{G_p}^{-1}(s) = \frac{\alpha}{s}[R + Ls] = \alpha L\left(1 + \frac{R}{sL}\right) \qquad \textit{Equation 2.51}$$

Comparing (2.51) with a standard PI controller (2.43), it is obtained the values of the gains needed to tune properly the controller (2.52).

$$Kp = \alpha L \;\; ; \;\; Ti = \frac{L}{R} \qquad \textit{Equation 2.52}$$

To select the closed-loop bandwidth, we must consider the sampling and switching frequencies. The goal of these frequencies is to make them as high enough so that the system performance does not degrade [16]. A good recommendation is to select a bandwidth at least 10 times lower than the sampling frequency (2.53), and the switching frequency should not be lower than half the sampling frequency (2.54).

$$\omega_s \geq 10\alpha \qquad \textit{Equation 2.53}$$

$$\omega_{sw} \geq 5\alpha \qquad \textit{Equation 2.54}$$

2.4.4 DC Voltage Loop Control

The DC voltage control is achieved by controlling the power exchanged by the converter with the grid. The transient conditions due to the change of power generated must be compensated by charging or discharging the capacitor of the DC link.

This control can be achieved through the grid current control, by applying a cascaded control. This involves an internal current loop and an outer DC voltage loop. The internal loop is designed to achieve short settling times and the outer loop is designed with the goal of stability, so it can be slower.

The behavior of the DC voltage is given by the instantaneous input-output power balance, as shown in (2.55).

$$\frac{3}{2}\left(V_{gd}i_d + V_{gq}i_q\right) = V_{dc}i_c + V_{dc}i_o = -V_{dc}C\frac{dV_{dc}}{dt} + V_{dc}i_o \qquad \textit{Equation 2.55}$$

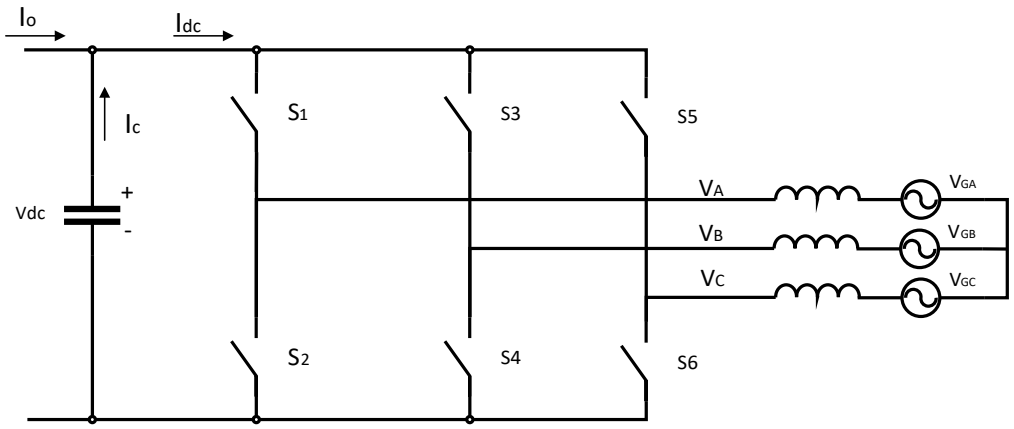

Figure 2.18 Scheme of a grid-connected VSI.

The objective is to find the transfer function of V_{dc} and i_d. Considering that the rotating frame is linealized with V_{gd}, the small-signal linearization leads to (2.56).

$$\frac{3}{2}\left((V_{gd}+\hat{v}_{gd})(i_d+\hat{\imath}_d)\right) = -(V_{dc}+\hat{v}_{dc})C\frac{d(V_{dc}+\hat{v}_{dc})}{dt} + (V_{dc}+\hat{v}_{dc})(i_o+\hat{\imath}_o) \quad \textit{Equation 2.56}$$

As the aim is to control $\hat{v}_{dc}$ and $\hat{\imath}_d$, the other pertubations have to be considered null, leading into (2.57) or (2.58) [13].

$$\frac{3}{2}\left((V_{gd}i_d + V_{gd}\hat{\imath}_d\right) = -V_{dc}C\frac{d\hat{v}_{dc}}{dt} + V_{dc}i_o + \hat{v}_{dc}i_o \quad \textit{Equation 2.57}$$

$$\left\{\begin{array}{c} \frac{3}{2}V_{gd}i_d = V_{dc}i_o \\ \frac{3}{2}V_{gd}\hat{\imath}_d = -V_{dc}C\frac{d\hat{v}_{dc}}{dt} + \hat{v}_{dc}i_o \end{array}\right\} \quad \textit{Equations 2.58}$$

Changing to Laplace domain and assuming $V_{dc} \approx \sqrt{3}V_{gd}$(DC link voltage cannot be lower than this value) in steady-state, lead to (2.59) and (2.60) [13].

$$\frac{\hat{v}_{dc}}{\hat{\imath}_d} = \frac{3}{2\sqrt{3}}\frac{{}^{V_{dc}}/_{i_o}}{(1-{}^{V_{dc}}/_{i_o}Cs)} \quad \textit{Equation 2.59}$$

$$K_p = \frac{C3\alpha}{2\sqrt{3}} \quad \textit{Equation 2.60}$$

The outer loop must be slower to guarantee the stability of the control. The bandwidth of the external loop will be designed with the following relation.

$$\alpha_{IL} \geq 10\alpha_{OL} \qquad \textit{Equation 2.61}$$

Where α_{IL} is the bandwidth of the inner loop, and α_{OL} is the bandwidth of the outer loop.

Although the system is a first order with no steady state error, any perturbation provokes steady-state error, which must be corrected using an integral action, using a PI controller.

This integral action has been designed experimentally, by testing different values and finding a solution that matches a low overshoot and a good correction of the offset. The chosen integral gain is proportional to the K_p and is given by (2.62).

$$T_i = \frac{200 * T_S}{K_p} \qquad \textit{Equation 2.62}$$

Once designed both loops, the final cascade control scheme is shown in figure 2.19.

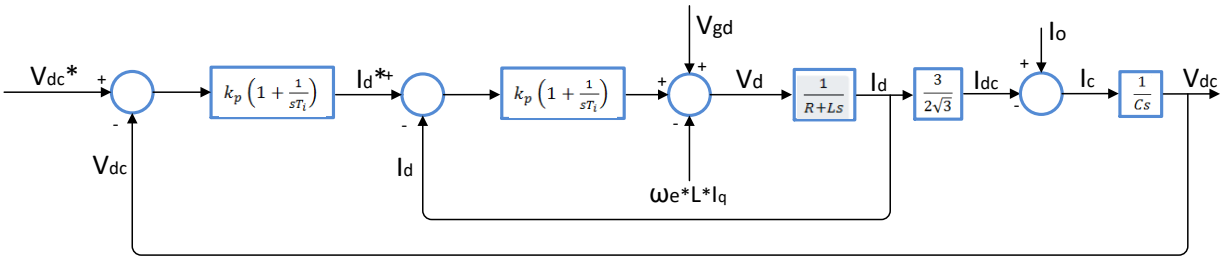

Figure 2.19: Block control scheme of the cascade control.

2.4.5 Boost Inductance Current Control

This control is a bit different from the previous ones, as its output is a dimensionless parameter, the duty cycle.

As already explained, the goal of the boost control is to extract the desired power from the DC source, in this case, a PV source. Most of the times, the desired power will be evidently the maximum power possible. This power is controlled through the current from the source, which results in a control scheme as shown in figure 2.20.

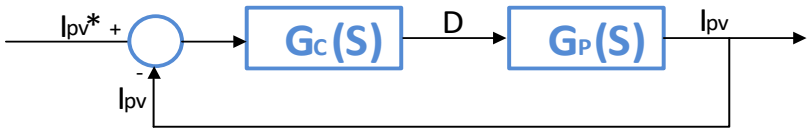

Figure 2.20: General block diagram of the Boost inductance control.

So the transfer function that must be found is the one that links the current with the duty cycle. To control the inductor current I_L, it is necessary to control its voltage. This relation is given by (2.63).

$$V_{L,B} = L_B \frac{dI_{L,B}}{dt} + R_B I_{L,B} \qquad \textit{Equation 2.63}$$

Using the Laplace transform.

$$V_{L,B} = L_B s I_{L,B} + R_B I_{L,B} \qquad \textit{Equation 2.64}$$

Where the average voltage across the inductance is zero, and it is given by (2.65). It must be assumed that the output voltage is constant, as the voltage loop is working as desired.

$$\int V_{L,B} dt = \int_0^{DT_s} V_{L,B} dt + \int_{DT_s}^{T_s} V_{L,B} dt = 0 \qquad \textit{Equation 2.65}$$

For a given period, from zero to DT_s, the switch is ON and diode is OFF, so the voltage across the inductance is equal to the DC source voltage.

For the same period, from DT_s to T_s, the switch is OFF and diode is ON. Then the voltage across the inductor is given by (2.66).

$$V_{L,B} = V_{PV} - V_{DC} \qquad \textit{Equation 2.66}$$

Then the average voltage is the following [9].

$$\int V_{L,B} dt = \frac{V_{PV} DT_s + V_{PV} T_s - V_{PV} DT_s - V_{DC} T_s + V_{DC} DT_s}{T_s} = V_{PV} + V_{DC}(D-1) \qquad \textit{Equation 2.67}$$

The plan transfer function is given by (2.68) and (2.69).

$$V_{L,B} = V_{PV} + V_{DC}(D-1) = (L_B s + R_B) I_{L,B} \qquad \textit{Equation 2.68}$$

$$I_{L,B} = \frac{V_{PV} - V_{DC} + V_{DC}D}{(L_B s + R_B)}$$ *Equation 2.69*

To design the controller, it must be considered that the parameter to control is D, so the terms that are multiplying D, will be seen as perturbations. The plant to control is given by (2.70).

$$\frac{I_{L,B}}{D} = \frac{V_{DC}}{(L_B s + R_B)}$$ *Equation 2.70*

Using the IMC method as in the AC grid current control, the transfer function of the controller is given by (2.71) [16].

$$G_c(s) = \left[1 - \frac{\alpha}{s+\alpha}\right]^{-1} {G_p}^{-1}(s)\frac{\alpha}{s+\alpha} = \frac{\alpha}{s}{G_p}^{-1}(s) = \frac{\alpha}{s}\left[\frac{R+Ls}{V_{DC}}\right] = \frac{\alpha L}{V_{DC}}\left(1 + \frac{R}{sL}\right)$$ *Equation 2.71*

Which results in the following PI gains.

$$Kp = \frac{\alpha L}{V_{DC}} \;\; ; \;\; Ti = \frac{L}{R}$$ *Equation 2.72*

As explained, the integral gain will be different on the implementation as it will be working on a discrete time domain, while the proportional gain is the same. The integral gain implemented in the controller is as shown in (2.73).

$$Ki_{DSP} = \frac{T_s}{Ti} = \frac{R}{Lf_s}$$ *Equation 2.73*

$$Kp_{DSP} = Kp$$ *Equation 2.74*

Finally, the control scheme of the controller and the plant is as shown in figure 2.21.

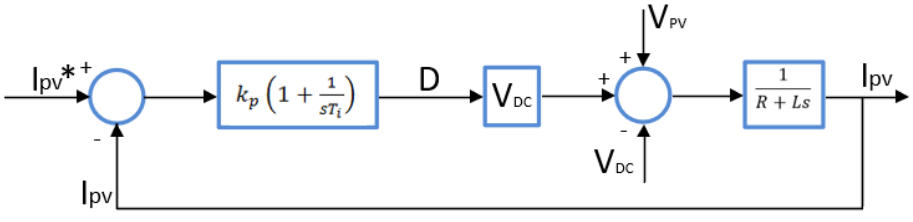

Figure 2.21: Block diagram of the Boost inductance current control.

3. GCC– REAL TIME HARDWARE IN THE LOOP SIMULATIONS

The project is implemented in two steps. The first one consists on using a Digital Signal Controller (DSC) and a Hardware in the loop (HIL), which is a safe environment in order to test all the controls. The second one, consist on using the same DSC acting on the LARA-100, the hardware containing the inverter and boost converter.

In this chapter, all these software and hardware related to the simulations implemented on the HIL is explained in detail. It is also presented the simulated circuit, with all its parameters and the simulation results.

In order to illustrate how the controller works and the performance of the DSC, the most important part of the code implemented is shown and explained.

3.1 Digital Signal Controller (DSC)

Microcontrollers are integrated chips that contain a processor core, memory, communication interface and peripherals like analog or digital inputs and outputs. Integrating these elements in one single chip has advantages as saving space, lower power consumption and higher reliability, which make microcontrollers a good solution for embedded systems.

On the other hand, a Digital Signal Processor (DSP) is a microprocessor within architecture specialized to operate with digital signal processing and fast operating capacity. Nowadays both microcontrollers and DSP can share some characteristics [17].

Therefore, a Digital Signal Controller (DSC) can be described as a combination of a Microcontroller and a DSP. DSC's advantages make them an excellent solution for a wide range of applications such as motor control, advanced power conversion, and power-sensitive applications.

For this project, a Texas Instrument DSC will be selected. The concrete model will be the TMS320F28335 of the Delfino series. This chip is sown in figure 3.1.

Figure 3.1: Texas Instrument TMS320F28335 controller [18].

Some of the key features of this DSC are a frequency time up to 150 MHz, Up to 18 PWM Outputs, 16 channels of 12-bit analog inputs and up to 88 individually programmable General Purpose Inputs/Outputs. The integrated development environment (IDE) used will be Code Composer Studio (CCS) [18].

Code Composer Studio (CCS) uses Eclipse software framework in addition to embedded debug capabilities from Texas Instruments, bringing to this software a suite of tools used to develop and debug embedded applications.

3.1.1 Enhanced Pulse Width Modulator (ePWM) Module

This peripheral module is a fundamental element in controlling power electronic systems by generating pulse width waveforms with minimal CPU intervention. Each ePWM module represents one PWM channel composed of two outputs: ePWMxA and ePWMxB, which are made available external to the device through the GPIO peripheral, as shown in figure 3.2. All the modules are chained together via a clock synchronization, which can be extended to the capture peripheral modules (eCAP). Each ePWM module can be configured to trigger an ADC start of conversion [18].

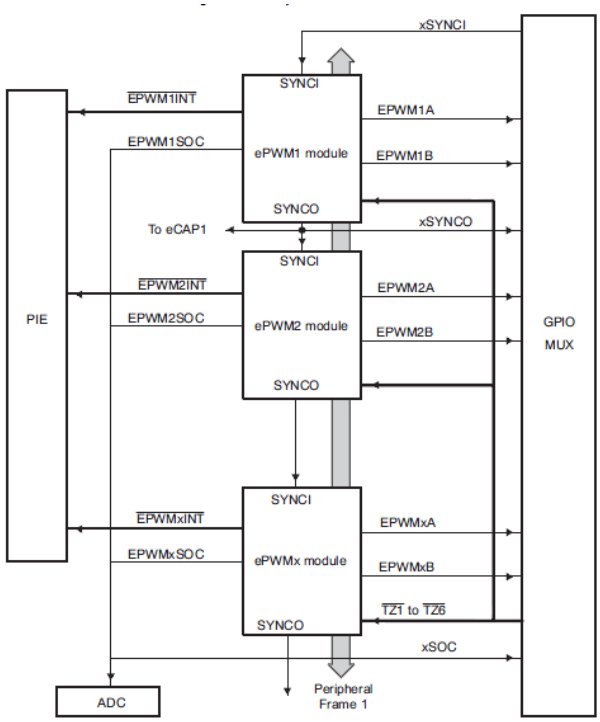

Figure 3.2: Connection between each ePWMx Module [18].

In every module, there is a time-base submodule that determines all of the event timing and can be configured to control the time-base counter (frequency of events), decide the count mode and prescale the CPU system clock.

There are three modes of operation:

- Up-Count Mode, where the counter starts from zero and increments until the period is reached.

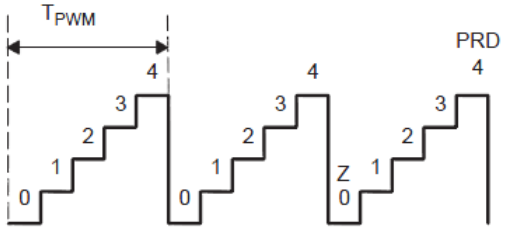

Figure 3.3: Time-Base Frequency and Period for Up-Count configuration [18].

- Down-Count Mode, where the counter starts from the period and decrements until zero is reached.

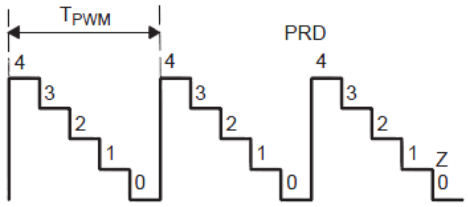

Figure 3.4: Time-Base Frequency and Period for Down-Count configuration [18].

- Up-Down-Count Mode, where counter starts from zero and increments until the period is reached. Then counter decrements until it reaches zero.

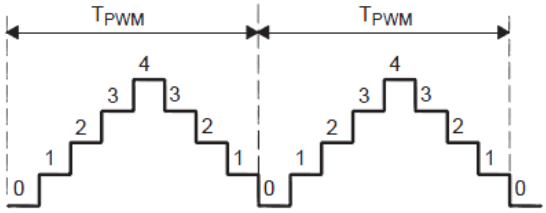

Figure 3.5: Time-Base Frequency and Period for Up-Down-Count configuration [18].

The Dead-Band submodule is used to generate a controlled dead-band between the two channels of an ePWM module. This submodule will be very useful in the generation of the SVPWM used for the three-phase inverter by inserting a small time period during which both leg switches receive OFF signal. For this purpose, the pair of outputs must be configured as active high, active low, active high complementary or active low complementary.

The dead-band submodule allows configuring independent values for rising-edge and falling-edge.

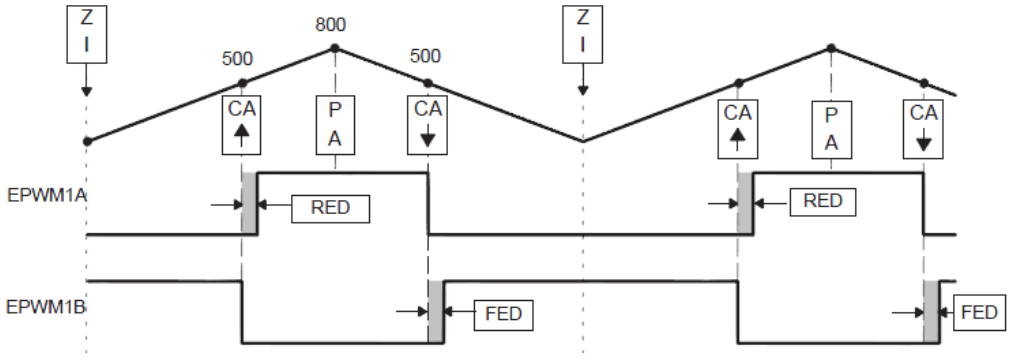

Figure 3.6: ePWM configuration for the inverter switches [18].

Figure 3.6 there is an example of a ePWM configuration for one leg of a three-phase inverter. This ePWM module has been configured Up-Down-Count mode until a value of 800. The compare value is set to 500 and there is a rising-edge dead-band and a falling-edge dead-band, both set to a value of 50. This module is configured as active high complementary.

3.1.2 Analog-to-Digital Converter (ADC) Module

The ADC module of TMS320F28335 has a 12-bit ADC with 16 channels configurable as two independent 8-channel modules [18]. Analog inputs analogue inputs are rated for signals in the range from 0V to 3V, and the digital value read by the DSC is given by (3.1).

$$Digital\ Value = 4095 * \frac{Input\ Voltage}{3} \qquad \textit{Equation 3.1}$$

Some ePWM modules will be used as triggers sources for the star-of-conversion (SOC) sequence. The analog MUX allows selecting any of the channel modules available. Figure 3.7 shows the block Diagram of the ADC Module.

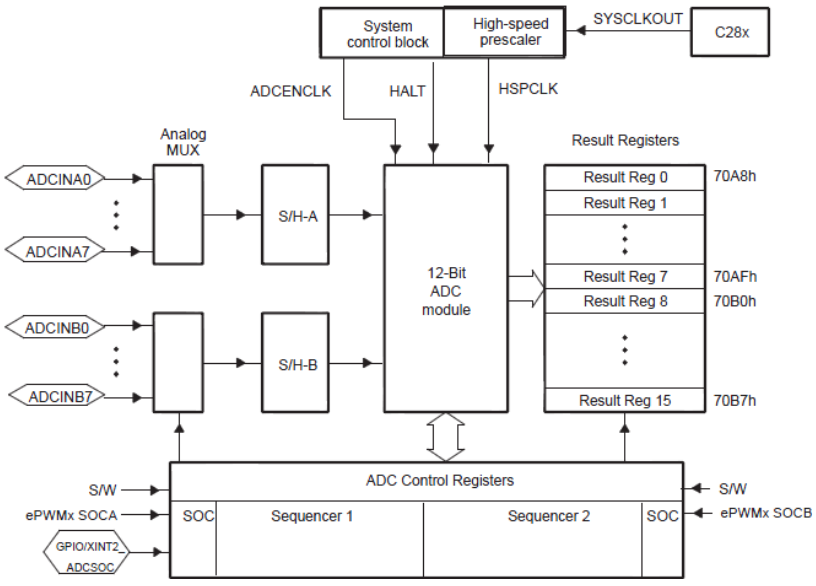

Figure 3.7: Block diagram of the ADC module [18].

Maximum sampling frequency runs at 12.5 MHz, and there can be up to 16 conversions in a single session. After the conversion, the digital value is stored in the appropriate result register.

3.2 Typhoon HIL

Controller Hardware in the Loop technology allows working in a safe environment, with no need of prototype, in order to test the controls for the power electronics systems studied.

HIL402 is the hardware-in-the-loop system used. It is a powerful tool which allows testing the code developed in a wide range of applications: solar and wind power generation, battery storage, power quality and motor drives. HIL402 has a 20 ns PWM resolution, in a closed loop with high-fidelity power stage with 1 MHz update rate [3].

A DSC interface board, specially built for C2000 family of Texas Instruments is integrated on the hardware. This interface provides a pin-to-pin compatible interface between Typhoon HIL emulators and C2000 control cards. Figure 3.8 shows the HIL402 with its interface board.

Figure 3.8: Typhoon HIL402 hardware.

Typhoon also provides a HIL software which is used to design the power electronics systems that will be tested. Figure 3.9 shows a schematic of an electrical system. This system will be compiled and ran by HIL402. Once the system is activated, the program coded will be compiled with Code Composer Studio and through the DSC interface board, the Texas Instrument controller will communicate to HIL402 and control the designed system.

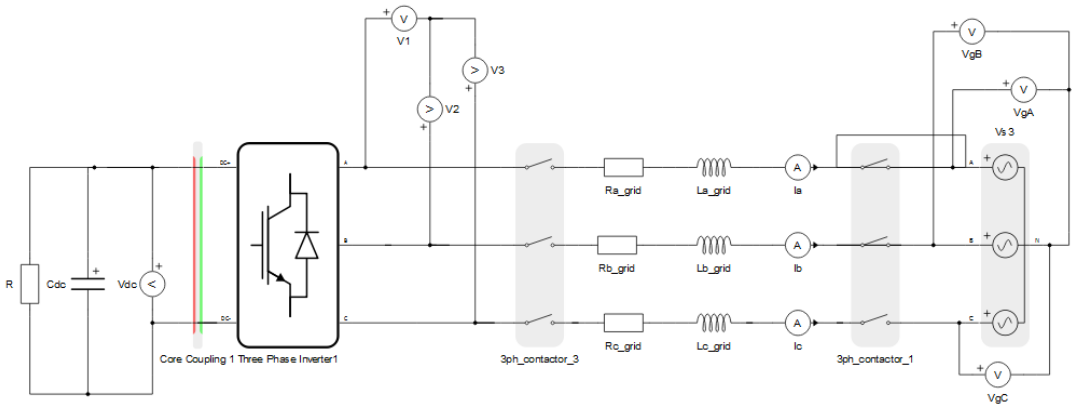

Figure 3.9: General scheme of the electrical simulated system.

One of the advantages of the used hardware is that although all connections are done, there is the option to use each HIL Digital and Analog Output or Input in the way it is wanted. This makes the experience of coding easier as the developer will be able to decide for example, which channel of the ADC will be used to read the DC link Voltage or which IGBT will be switched by EPWM-1. Figure 3.10 shows the relation between HIL's and DSC's pins.

Typhoon HIL Digital Output	DSP Digital Input	Typhoon HIL Digital Input	DSP Digital Output
DO1	GPIO-24 / EQEPA-2	DI1	GPIO-00/EPWM-1A
DO2	GPIO-25 / EQEPB-2	DI2	GPIO-02/EPWM-2A
DO3	GPIO-26 / EQEPI-2	DI3	GPIO-04/EPWM-3A
DO4	GPIO-20	DI4	GPIO-06/EPWM-4A
DO5	GPIO-21	DI5	GPIO-08/EPWM-5A
DO6	GPIO-22	DI6	GPIO-10/EPWM-6A
DO7	GPIO-23	DI7	GPIO-01/EPWM-1B
DO8	GPIO-27	DI8	GPIO-03/EPWM-2B
DO9	GPIO-32	DI9	GPIO-05/EPWM-3B
DO10	GPIO-33	DI10	GPIO-07/EPWM-4B
DO11	GPIO-48/40**	DI11	GPIO-09/EPWM-5B
DO12	GPIO-49/41**	DI12	GPIO-11/EPWM-6B
DO13	GPIO-60/44**	DI13	GPIO-14/EPWM-8A*
DO14	GPIO-61/45**	DI14	GPIO-12/EPWM-7A*
DO15	GPIO-62/46**	DI15	GPIO-15/EPWM-8B*
DO16	GPIO-63/47**	DI16	GPIO-13/EPWM-7B*

Typhoon HIL Analog Output	DSP Analog Input
AO1	ADCIN – A0
AO2	ADCIN – A1
AO3	ADCIN – A2
AO4	ADCIN – A3
AO5	ADCIN – A4
AO6	ADCIN – A5
AO7	ADCIN – A6
AO8	ADCIN – A7
AO9	ADCIN – B0
AO10	ADCIN – B1
AO11	ADCIN – B2
AO12	ADCIN – B3
AO13	ADCIN – B4
AO14	ADCIN – B5
AO15	ADCIN – B6
AO16	ADCIN – B7

Figure 3.10: Pins relation between typhoon HIL and TI's DSC [19].

To decide the proper relation between HIL's and DSC's pins, it should be taken in care the final purpose of the code, in order to make the schematic in HIL the maximum similar to the real system. The goal of the HIL will be that the developer is able to use the same code in the simulated system and in the real system, to take the maximum benefit of it.

3.3 Simulated Circuit

The circuit is firstly designed approaching it as much as possible to the set-up which is going to be tested. This tests allows to prove the control in a safe environment to study the response to different scenarios.

As is shown, the circuit is composed of all the elements studied before. A three-phase grid, with its voltage measurement, an RL filter with current measurement, three-phase inverter, and a capacitor in the DC part, with voltage and current measurement.

There is also the boost's IGBT, the filter composed by a resistance and an inductance, the source and a diode. Also, measurements like voltage and current on the PV source are added. The circuit is shown in figure 3.11.

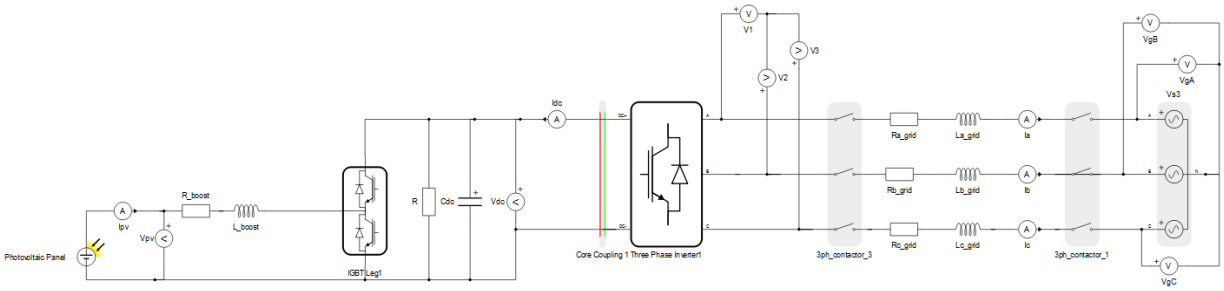

Figure 3.11: General electric scheme of the simulated circuit.

As the goal of this circuit is to study the response of the control before implementing it on LARA-100, more measurements than needed in practice have been used. Inverter voltage measurements and DC link current measurement will not be needed for practical experimentation.

The contactors and the Core coupling are also elements that are not needed for practical experimentation. Core coupling is a tool used by the software in order to separate the circuit into two dependent circuits to make easier the compilation of the design.

Finally, in table 3.1, it is presented the parameters used to build the simulated circuit.

Circuit Parameters	
Grid voltage (RMS)	V = 100 V
Grid frequency	F = 50 Hz
AC filter inductance	L = 19.23 mH
AC filter resistance	R = 1.6 Ω
Boost inductance	L = 35 mH
Boost resistance	R = 0.2 Ω

Table 3.1: Physical system parameters.

3.4 Program Implementation

Once the simulated system is built and the control is designed, it is time to code the desired control, using C language. The used DSC "TMS320F28335" has already been introduced, will be coded through Code Composer Studio (CCS) software.

The first tasks will be to code properly the PWM and ADC and after configuring these modules, the control loops will be coded. To carry out the project, it is used an example project given by the software named "Example_2833xGpioSetup". All the code will be developed from this initial project, which principal file is named "Main.c".

3.4.1 PWM Configuration

For the VSI, there are multiple ePWM modules that can be used, although the used ones will be ePWM1, ePWM2, and ePWM3 which are going to be configured.

- Switches T1 and T2 correspond to ePWM1a (GPIO0) and ePWM1b (GPIO1).
- Switches T3 and T4 correspond to ePWM2a (GPIO02) and ePWM2b (GPIO3).
- Switches T5 and T6 correspond to ePWM3a (GPIO4) and ePWM3b (GPIO5).

For the inverter switches, it is chosen the Up-Down-Count Mode, shown in figure 3.12.

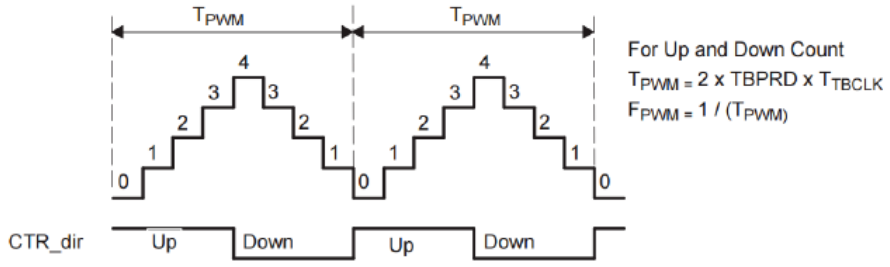

Figure 3.12: Up-Down-Count configuration for ePWM module [18].

Once the count mode is chosen, some parameters must be configured. Knowing the frequency of the DSC's clock is 150 [MHz] The desired switching frequency is set to 10 [kHz], the counter value (TBPRD) is given by (3.2).

$$TBPRD = \frac{f_{CLK}}{2*f_{sw}} = \frac{150000[kHz]}{2*10\ [kHz]} = 7500 \qquad \textit{Equation 3.2}$$

And the period is given by (3.3).

$$T_{PWM} = \frac{2*TBPRD}{f_{CLK}} = 1x10^{-4}\ [s] \qquad \textit{Equation 3.3}$$

Also, the dead-band must be configured in order to avoid a short-circuit. In figure 3.13 is seen that two dead-bands must be configured, RED and FED. The counter is set to 600, which equals to the value given by Equation 3.4.

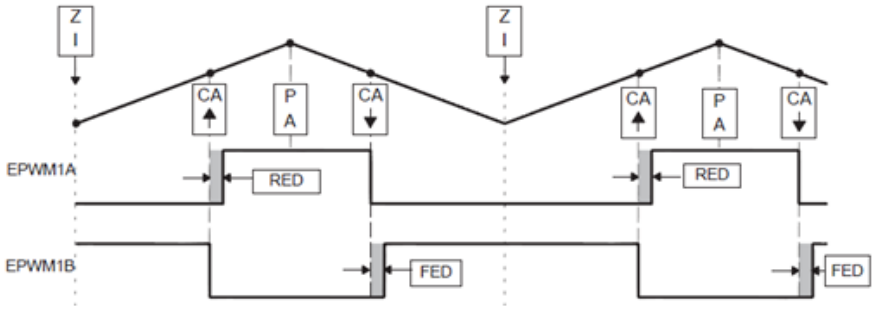

Figure 3.13: Inverter configuration of the ePWM module.

$$T_{DB} = \frac{DBcounter}{f_{CLK}} = \frac{600}{150000[kHz]} = 4x10^{-6}[s] \qquad \textit{Equation 3.4}$$

The pins involved in ePWM module must be configured firstly as outputs and then as part of the module to ensure they work under ePWM signal, with the following commands.

```
// set-up PWM GPIO as outputs
GpioCtrlRegs.GPADIR.bit.GPIO0 = 1;
GpioCtrlRegs.GPADIR.bit.GPIO1 = 1;
GpioCtrlRegs.GPADIR.bit.GPIO2 = 1;
GpioCtrlRegs.GPADIR.bit.GPIO3 = 1;
GpioCtrlRegs.GPADIR.bit.GPIO4 = 1;
GpioCtrlRegs.GPADIR.bit.GPIO5 = 1;
// set-up PWM GPIO as ePWM
GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;   // EPWM1A pin (T1 U)
GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 1;   // EPWM1B pin (T4 U)
GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1;   // EPWM2A pin (T2 V)
GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 1;   // EPWM2B pin (T5 V)
GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 1;   // EPWM3A pin (T3 W)
GpioCtrlRegs.GPAMUX1.bit.GPIO5 = 1;   // EPWM3B pin (T6 W)
```

Although the frequency is by default 10 [kHz], the variable "Fswitch", which is written in kHz, allows us to change it to any desired value. In the following images, it is shown the performance of the 6 PWM where input 1 and 7 corresponds to leg "A", input 2 and 8 to leg "B", and input 3 and 9 to leg "C". Figure 3.14 and 3.15 shows the PWM signals at 10 kHz and at 5 kHz, respectively, with a plot of 100μs per division.

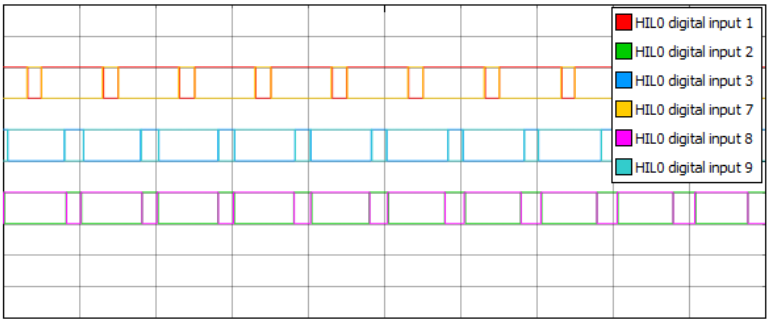

Figure 3.14: SVPWM signals simulated with f_s=10 kHz.

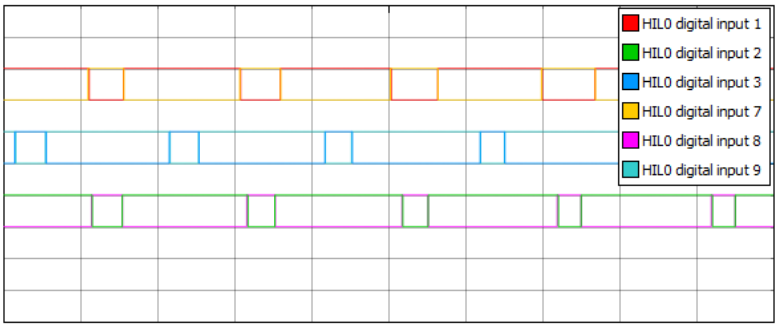

Figure 3.15: SVPWM signals simulated with f_s=5 kHz.

Also, the boost converter needs the configuration of one ePWM module, although in this case only one of the two pins related to ePWM will be used. The chosen PWM module is ePWM5 with a count-up configuration. Knowing the frequency of the DSC's clock is 150 [MHz] The desired switching frequency is set to 15 [kHz], the counter value (TBPRD) is given by (3.5).

$$\text{TBPRD} = \frac{\text{f}_{\text{CLK}}}{\text{f}_{\text{sw}}} = \frac{150000[\text{kHz}]}{15\ [\text{kHz}]} = 10000 \qquad \textit{Equation 3.5}$$

And the period is given by (3.6).

$$T_{PWM} = \frac{TBPRD}{f_{CLK}} = 6{,}66x10^{-5}\ [s] \qquad \textit{Equation 3.6}$$

The registers coded for both modules are the followings.

```
GpioCtrlRegs.GPAMUX1.bit.GPIO8 = 1;    // Typhoon
GpioCtrlRegs.GPADIR.bit.GPIO8 = 1;      // Set as output
// BOOST PWM //
EPwm5Regs.CMPA.half.CMPA=_IQmpy(10000,D); // 10kHz.
// END BOOST PWM //
```

3.4.2 ADC Configuration

The ADC module needs a trigger as a source for the star-of-conversion. There are multiple possible triggers. It has been decided to use ePWM6 module as trigger of the ADC, so we control fsample through this module. It is used a module independent of the switches with the aim of taking maximum advantage of the controller's bandwidth. The ADC is going to work at10 kHz. This is done with the following commands.

```
EPwm6Regs.ETSEL.bit.SOCAEN = 1;        // Enable SOC on A group
EPwm6Regs.ETSEL.bit.SOCASEL = 4;       // Select SOC from CPMA on up-count
EPwm6Regs.ETPS.bit.SOCAPRD = 1;        // Generate pulse on 1st event
```

At this point of the project, it is needed the measurements of AC inverter currents, DC link voltage, AC grid voltages, PV source voltage, and PV source current. Next step is to decide each scaling factor assuming that the values read by the ADC module are given by (3.7).

$$Digital\ Value = 4095 * \frac{Input\ Analog\ Voltage}{3} \qquad \textit{Equation 3.7}$$

The scaling factor can be set with HIL software, although it will be calibrated in order to make it identical to the experimentation circuit which will be presented in the next chapter.

- AC grid current. It has to be considered that the conversion is directly done by LARA-100 on the experimental circuit. An equation (3.8) is given in the datasheet to calculate approximately the scaling factor.

$$Range = 2 * 2.5 * 1.41 * I_N = 2 * 2.5 * 1.41 * 32\ [A] = 225.6[A] \qquad \textit{Equation 3.8}$$

As it is working with AC currents, the effective range is [-112.8, 112.8]. To be more accurate this value has been recalculated, obtaining a range of [-132.4, 132.4] which corresponds to [-1.5V, 1.5V]. The scaling factor obtained is 88.265 shown in (3.9).

$$Scaling\ factor = \frac{Range}{3} = \frac{132.4*2}{3} = 88.265 \qquad \textit{Equation 3.9}$$

The code implemented is the following one.

```
Iameas = _IQ11toIQ(AdcRegs.ADCRESULT0>>4)-_IQ11toIQ(AdcRegs.ADCRESULT5>>4);
Ibmeas = _IQ11toIQ(AdcRegs.ADCRESULT1>>4)-_IQ11toIQ(AdcRegs.ADCRESULT5>>4);
Icmeas = _IQ11toIQ(AdcRegs.ADCRESULT2>>4)-_IQ11toIQ(AdcRegs.ADCRESULT5>>4);

Ialara = _IQmpy(_IQ(88.265),Iameas)+_IQ(0.65);
Iblara = _IQmpy(_IQ(88.265),Ibmeas)+_IQ(0.2);
Iclara = _IQmpy(_IQ(88.265),Icmeas)+_IQ(0.1);
```

Where ADCRESULT5 is the offset of the current measurements.

- DC link voltage. This lecture will be a unipolar value as it is a DC voltage. For the experimental circuit, LARA-100 gives us a range that is [0V, 800V] which equals to [0V, 3V] in the ADC module. Therefore, the scaling factor is given by (3.10).

$$Scaling\ factor = \frac{Range}{Digital\ value} = \frac{800}{4095} = 0.19536 \qquad \textit{Equation 3.10}$$

And the code implemented is as follows.

```
Vdc = AdcRegs.ADCRESULT3>>4
Voltage= Vdc*0.19536; // 4095*0.19536 =800V
```

- AC grid voltages. This measurement is bipolar, and the range is [-800V, 800V] which equals to [-1.5V, 1.5V] in the ADC module. Therefore, the scaling factor is given by (3.11).

$$Scaling\ factor = \frac{Range}{Digital\ value} = \frac{1600}{4095} = 0.39072 \qquad \textit{Equation 3.11}$$

And the code implemented is as follows. Where empirically an offset of 32V has been set, to correct a deviation.

```
//  VOLTAGE GRID LECTURE //
Vared=AdcRegs.ADCRESULT7>>4;
Vbred=AdcRegs.ADCRESULT8>>4;
Vcred=AdcRegs.ADCRESULT9>>4;

Vax = (Vared*0.39072)-800+32;
Vbx = (Vbred*0.39072)-800+32;
Vcx = (Vcred*0.39072)-800+32;
```

- PV source voltage. Is a unipolar measurement although the range is [-800V, 800V] which equals to [-1.5V, 1.5V] in the ADC module. Therefore, the scaling factor is given by (3.12).

$$Scaling\ factor = \frac{Range}{Digital\ value} = \frac{1600}{4095} = 0.39072 \qquad \textit{Equation 3.12}$$

And the code implemented is as follows. Where empirically an offset of 32V has been set, to correct a deviation, exactly the same than in AC grid voltages.

```
//  PV VOLTAGE LECTURE //
Vpvmeas=AdcRegs.ADCRESULT10>>4
Vpv = (Vpvmeas*0.39072)-800+32;
```

- PV source current. The conversion is explained later in LA 25-NP chapter, and is coded as follows.

```
Ipvmeas=AdcRegs.ADCRESULT6>>4;
Ipv=(Ipvmeas-2047.5)/135.135;
```

The ratio value (135.135), is given by (3.13).

$$ratio_{DSP} = \frac{r_T * R}{range_{voltage}} * range_{DSP} = \frac{2*330}{1000*10} * 2047.5 = 135.135 \qquad \textit{Equation 3.13}$$

3.4.3 CLARKE and PARK Transforms

To success with the control, it is necessary to implement a correct Clarke and Park transformations. For this purpose, it is shown the commands used to implement them.

- Clarke transformation code.

```
ClarkeA=_IQmpy(_IQ(0.6666,clarke2A)-_IQmpy(_IQ(0.3333),clarke2B)-
_IQmpy(_IQ(0.3333),clarke2C);
ClarkeB=+_IQmpy(_IQ(0.57735027),clarke2B)-_IQmpy(_IQ(0.57735027),clarke2C)
```

- Park transformation code.

```
ParkD= _IQmpy(_IQ(Mycos0),ClarkeA)+_IQmpy(_IQ(Mysin0),ClarkeB);
ParkQ=-_IQmpy(_IQ(Mysin0),ClarkeA)+_IQmpy(_IQ(Mycos0),ClarkeB);
```

- Inverse Park transformation code.

```
IParkA=_IQmpy(-_IQ(Mycos0),IParkD)-_IQmpy(-_IQ(Mysin0),IParkQ);
IParkB=_IQmpy(-_IQ(Mysin0),IParkD)+_IQmpy(-_IQ(Mycos0),IParkQ);
```

3.4.4 SVPWM

To generate de SVPWM signals, a predefined module of the controlSUITE package called "SVGEN_DQ". This module calculates the appropriate duty ratios needed to generate a given stator reference voltage using SVPWM technique. The module's inputs are the inverter voltages in αβ frame, as shown in figure 3.16.

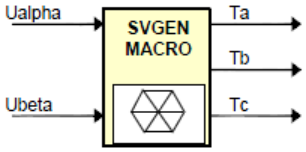

Figure 3.16: Block diagram of SVPWM module.

Firstly, it is necessary to obtain the inverter voltages signal in αβ frame, as the output of the cascade control gives these voltages in *dq* frame. Therefore, it is done the inverse park transformation with the following commands.

```
IParkA=_IQmpy(-_IQ(Mycos0),IParkD)-_IQmpy(-_IQ(Mysin0),IParkQ);
IParkB=_IQmpy(-_IQ(Mysin0),IParkD)+_IQmpy(-_IQ(Mycos0),IParkQ);
```

As the module works with the voltages in p.u., it is necessary to scale them using (3.14) and (3.15).

$$V_{\alpha\beta} = M\frac{V_{DC}}{2}e^{j\omega t} \qquad \textit{Equation 3.14}$$

$$V_{\alpha\beta_{p.u.}} = \frac{2V_{\alpha\beta}}{MV_{DC}} \qquad \textit{Equation 3.15}$$

The V_{dc} value is a constant changing value. To remove noise from its measurement, it is decided to pass it through a low-pass filter, whose function transfer in the Laplace domain is shown in figure 3.17.

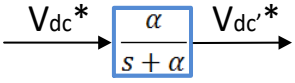

Figure 3.17: Block diagram of the low-pass filter.

Where α is the bandwidth of the filter. This bandwidth is set to the same value as the one in the outer voltage loop. This is coded in discrete time with the following equation (3.16).

$$y(z) = \frac{[a+b*z^{-1}]u(z)}{1+c*z^{-1}} \qquad \textit{Equation 3.16}$$

Finally, the implementation of the low-pass filter and the conversion to per unit is as follows.

```
//LOW-PASS FILTER //
Udc[0]=Voltage/1000;
Udc_filt[0]=Udc[0]*A_LPF[0]+Udc[1]*A_LPF[1]-B_LPF[1]*Udc_filt[1];
Udc_filt[1]=Udc_filt[0];
Udc[1]=Udc[0];
Ualpha= _IQmpy(IParkA,_IQ(1.739)); // 1.739= 2/1.15
Ubeta=  _IQmpy(IParkB,_IQ(1.739));
Ualpha1=_IQdiv(Ualpha,_IQ(Udc_filt[0]));
Ubeta1= _IQdiv(Ubeta,_IQ(Udc_filt[0]));
```

Next step is to call the space vector generator module, and reading the results. These results are given in per unit [-1, 1] and they must be adapted before implementing them to the ePWM module of the DSC. This is down by (3.17).

$$Compare = \frac{Counter}{2} * Compare_{p.u} + \frac{Counter}{2} \qquad \textit{Equation 3.17}$$

The commands implemented are the following ones.

```
svgen1.Ualpha = Ualpha1;
svgen1.Ubeta = Ubeta1;
SVGENDQ_MACRO (svgen1); // Call compute macro for svgen_dq1

lec1 = svgen1.Ta; // Access the outputs of svgen_dq1
lec2 = svgen1.Tb; // Access the outputs of svgen_dq1
lec3 = svgen1.Tc; // Access the outputs of svgen_dq1

EPwm1Regs.CMPA.half.CMPA =_IQmpy(HalfCounter,lec1)+ HalfCounter;
EPwm2Regs.CMPA.half.CMPA =_IQmpy(HalfCounter,lec2)+ HalfCounter;
EPwm3Regs.CMPA.half.CMPA =_IQmpy(HalfCounter,lec3)+ HalfCounter;
```

3.4.5 Controller

The code implemented to build the current controller is shown below:

```
//INNER LOOP: CURRENT CONTROL //
Kp_i=_IQ(Inductance*6.28318*Fsample/alfa);
Ki_i=_IQ(Resistance/(Inductance*Fsample*1000));

pid_iq.Ref = _IQ(Iqref);
pid_iq.Fdb = ParkQ;
pid_iq.Kp = Kp_i;
pid_iq.Ki = Ki_i;

PID_REG3_MACRO(pid_iq);

pid_id.Ref= pid_Vdc.Out;  // DC link bus control
pid_id.Fdb = ParkD;
pid_id.Kp = Kp_i;
pid_id.Ki = Ki_i;

PID_REG3_MACRO(pid_id);
// END CURRENT CONTROL//
```

As the controller is now working on a discrete domain, the gains must be redefined as shown on (3.18) and (3.19). The controller will work with [kV], what means that Kp‘ must be scaled.

$$Kp' = \frac{Kp}{10^3} = \frac{\alpha L}{10^3} = \frac{2\pi L f_S[Hz]}{10*10^3} = \frac{2\pi L f_S[kHz]}{10} \qquad \textit{Equation 3.18}$$

$$Ki' = T_s Ki = \frac{T_s}{T_i} = \frac{R}{Lf_s[Hz]} = \frac{R}{Lf_s[kHz]*10^3} \qquad \textit{Equation 3.19}$$

The PID is implemented using a predefined module of the controlSUITE package called "PID_REG3". This module gives us the output of the PI controller once the function is called and a reference and a feedback are given.

The code to implement the voltage controller is shown below:

```
//OUTER LOOP: Vdc CONTROL //
Kp_Vdc= _IQ(Capacitor*6.28318*Fs*Unitari2*1000/(alfa*alfa*1.1547))
Ki_Vdc= Kp_Vdc/500;

pid_Vdc.Ref = Vdcrefpu;
pid_Vdc.Fdb = Vdcpu;
pid_Vdc.Kp = Kp_Vdc;
pid_Vdc.Ki = Ki_Vdc;

PID_REG3_MACRO(pid_Vdc)
// END Vdc CONTROL //
```

Alfa is the attenuation of the bandwidth, which is set to 10. The outer loop must be slower than the inner loop, so the bandwidth will be smaller. The integral gain is tuned empirically as its only purpose is to correct static deviations.

It is also presented the code implemented on the Boost inductance current control. It has been used the module pid_reg3, as done on the other PI controllers.

```
// BOOST INDUCTANCE CONTROL //
Kp_Ipv= _IQ(L_boost*6.28318*10000/(14*Vdcref));
Ki_Ipv= _IQ(R_boost/(L_boost*Fs*1000));

pid_Ipv.Ref=Ipv_ref;
pid_Ipv.Fdb =_IQ(Ipv);
pid_Ipv.Kp = Kp_Ipv;
pid_Ipv.Ki = Ki_Ipv;

pid_Ipv.OutMin=_IQ(0);
pid_Ipv.OutMax=_IQ(0.6);

PID_REG3_MACRO(pid_Ipv);
D= pid_Ipv.Out;
// END BOOST INDUCTANCE CONTROL//
```

Finally, it is shown the code of the MPPT algorithm, which is done, following perturb and observe algorithm. These functions are called from the main loop, but are stored in another file.

```
void MPPT()

{

    if (cont3==Count_mppt)

         {

             if (P_mppt[0]>P_mppt[1])

             {

                 if (V_mppt[0]>V_mppt[1])

                 {

                     Ipvref=Ipvref-Step;

                 }else{

                     Ipvref=Ipvref+Step;

                      }

             }else{

                 if (V_mppt[0]>V_mppt[1])

                 {

                     Ipvref=Ipvref+Step;

                 }else{

                     Ipvref=Ipvref-Step;

                      }

             }

             cont3=0;

             V_mppt[1]=V_mppt[0];

             P_mppt[1]=P_mppt[0];

         }

}
```

Where Count_mppt, is a value calculated to determine the update frequency of the algorithm.

3.4.6 Program Sequence

Figure 3.18 shows a flowchart of the program's performance. Once the program is loaded, all the registers and variables are initialized and the modules are configured. Once the system is initialized, to continue running the program the variable StartOperation must be set to 1. This is done to be sure that all the registers have been successfully configured.

When StarOperation is set to 1, the program enters to the main loop, where the PLL and the voltage and current measurements start.

At this point, no actuation has been done to the power converter yet, and PID controllers are still unused. This is the moment to check that all the measurements are working correctly and that PLL is working properly.

When variable "Connect" is set to 1, inverter switches start to operate along with SVPWM and the PID controllers of AC current control and DC-link voltage control start its performance.

Finally, there is another variable to control the start of the boost converter switch, the Boost inductance current loop, and the MPPT algorithm. As shown in figure 3.18, the variable connect2, goes after the system is initialized and the PLL and the inverter control is working successfully.

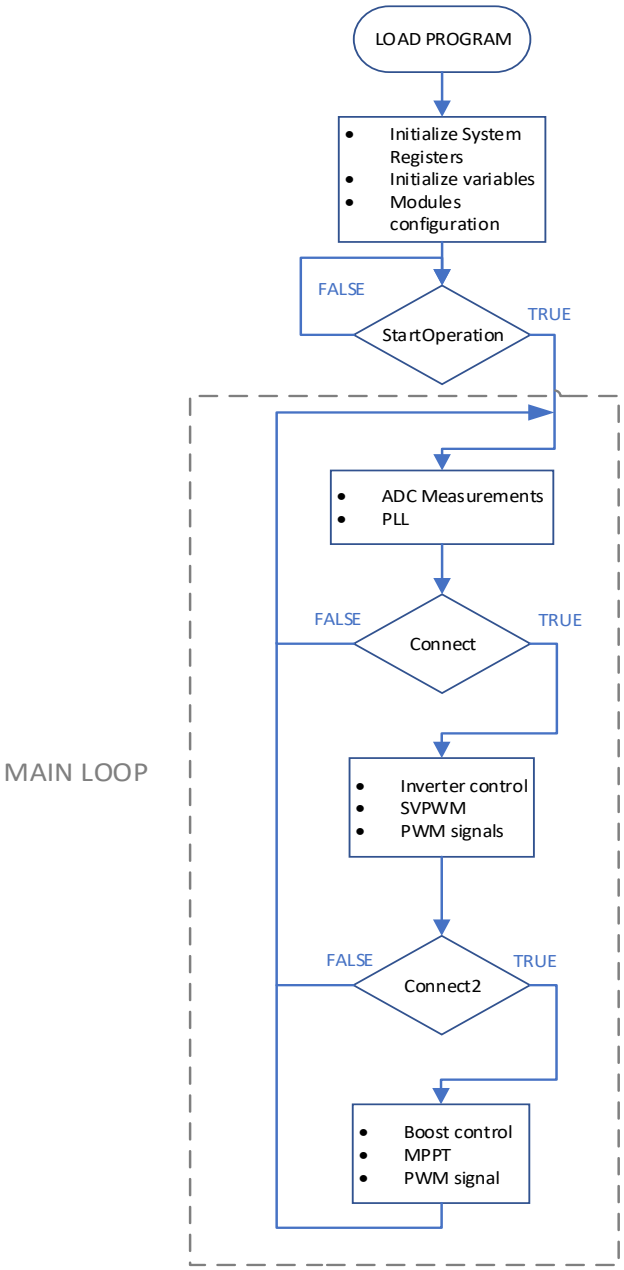

Figure 3.18: Block diagram of the program's sequence.

All variables "StartOperation", "Connect", and "Connect2" must be permanently set to 1 to ensure that loops are working as it is desired.

3.5 Results

This part of the chapter reflects the results evaluated on HIL simulations. The aim of this chapter is to verify the correct performance of the system and testing if the control has the desired response. It is tested the steady-state and the dynamic response of the main loops with changes on the grid frequency, and PV source conditions.

3.5.1 Current Loop

In order to test the current loop, step changes are applied in Iq while the inverter is switching. In this case, the switching frequency and the sampling frequency are equal, and three different frequencies are tested 10, 5 and 2 kHz. The success of the control is being evaluated in two ways. It must be seen that the AC grid current follows the reference fixed and that the step response has a time constant near to the designed one.

The time constant is the time for the system's step response to reach 63.2% of its final value [16]. The time constant owns a relation with the bandwidth which is given by (3.20). This relation will be a good tool to evaluate the control performance.

$$\tau = \frac{1}{2\pi f_{BW}} = \left(1 - \frac{1}{e}\right) * A_{step} \qquad \textit{Equation 3.20}$$

The bandwidth has been designed to be 14 times slower than the switching and sampling frequency, therefore in a system where fs = 10 kHz the frequency bandwidth is 714.29 Hz, and the desired time constant is given by (3.21).

$$\tau = \frac{1}{2\pi f_{BW}} = \frac{14}{2\pi * 10000} = 0.23\ ms \qquad \textit{Equation 3.21}$$

In figure 3.19, is difficult to appreciate the time constant of the control by viewing the current in *abc* frame, although it can be determined that the step reference amplitude change is properly followed, and the waveform is very near to a sinusoidal wave. In the right figure, appreciating that it is a 2ms division, it is evident that time constant is less than 1ms, although in every phase can be different depending on the instant phase.

To properly see the step response, it should be looked directly to variable Iq, which corresponds to the figure down. The time constant observed is near to the desired one, although it is appreciated some overshot and a second order system response.

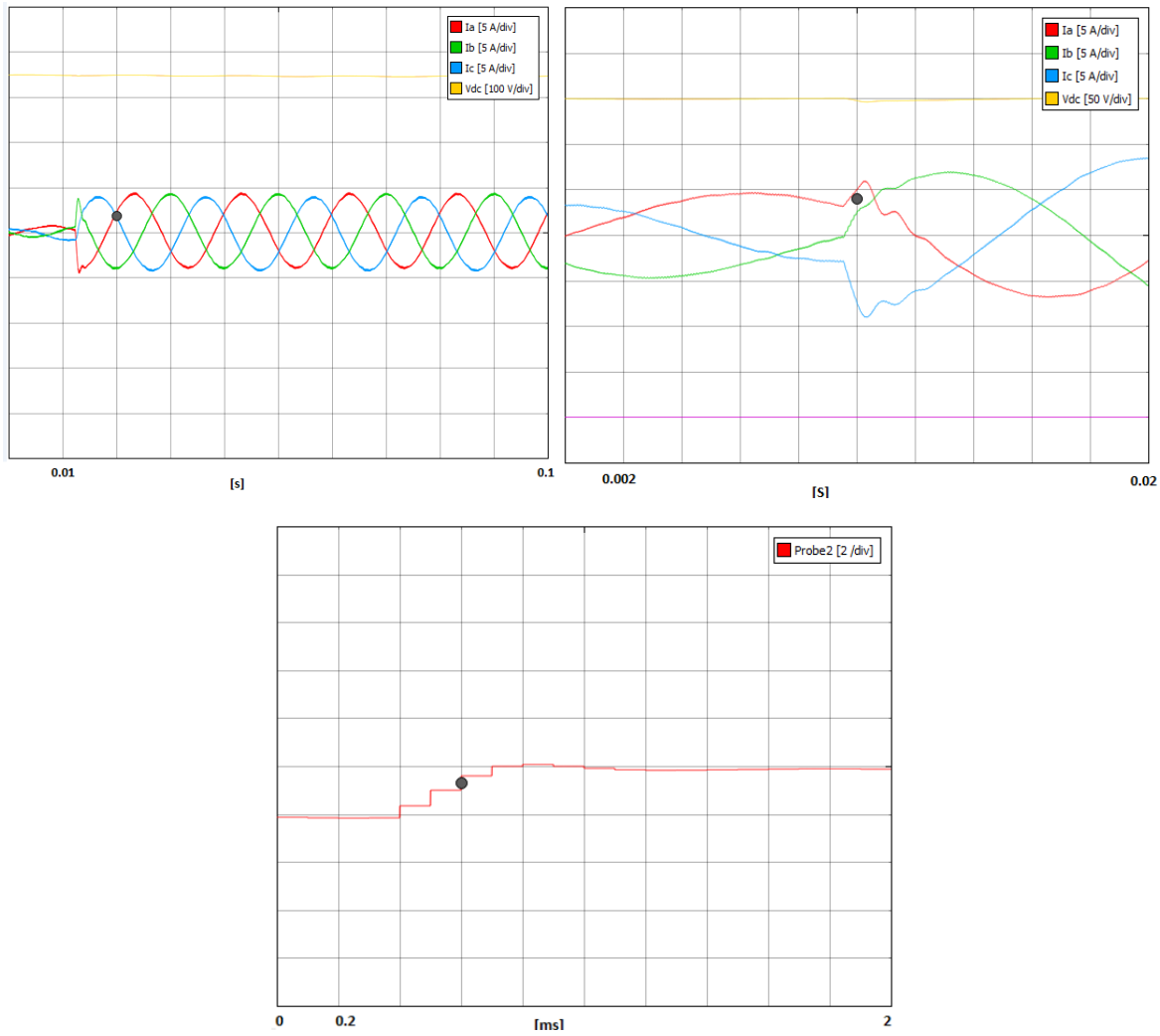

Figure 3.19: 4 Amps amplitude Step on Iq reference switching at 10 kHz.

The same test has been done with switching and sampling frequency set to 5 kHz. The time constant should be of 0.44 ms, and it is observed that this is achieved. It can be seen as the response is slower and the ripple starts to increment respect to the 10 kHz performance.

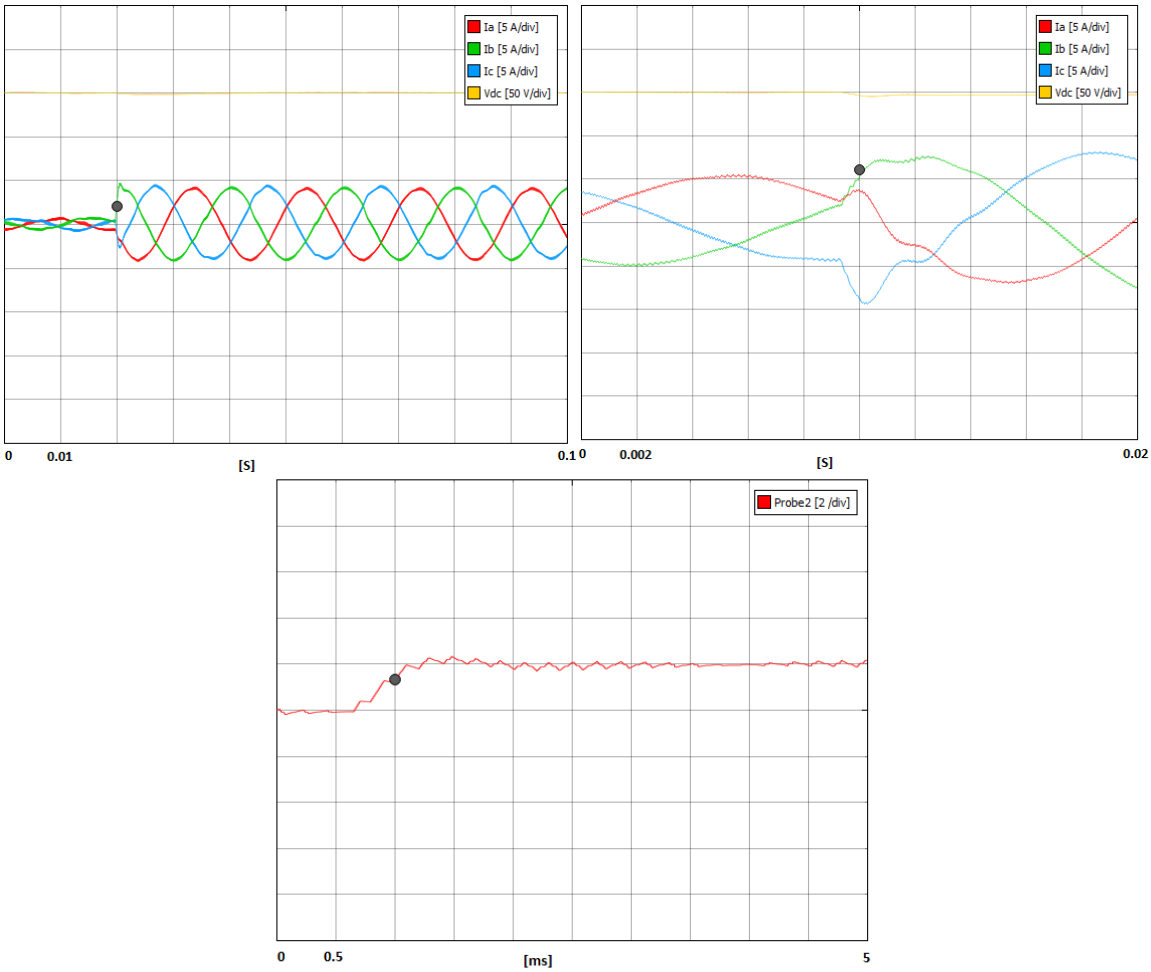

Figure 3.20: 4 Amps amplitude Step on Iq reference switching at 5 kHz.

Finally, the test has been done with the switching frequency set to 2 kHz. The time response expected for this test is given by (3.22), with a bandwidth 14 times slower than the inner loop.

$$\tau = \frac{1}{2\pi f_{BW}} = \frac{14}{2\pi * 2000} = 1.1\ ms \qquad \textit{Equation 3.22}$$

Observing Iq in figure 3.21 (below), it can be determined that the time constant is around 1 ms as expected. It is also remarkable the increase of the current ripple, in consequence of the decrease of the switching frequency.

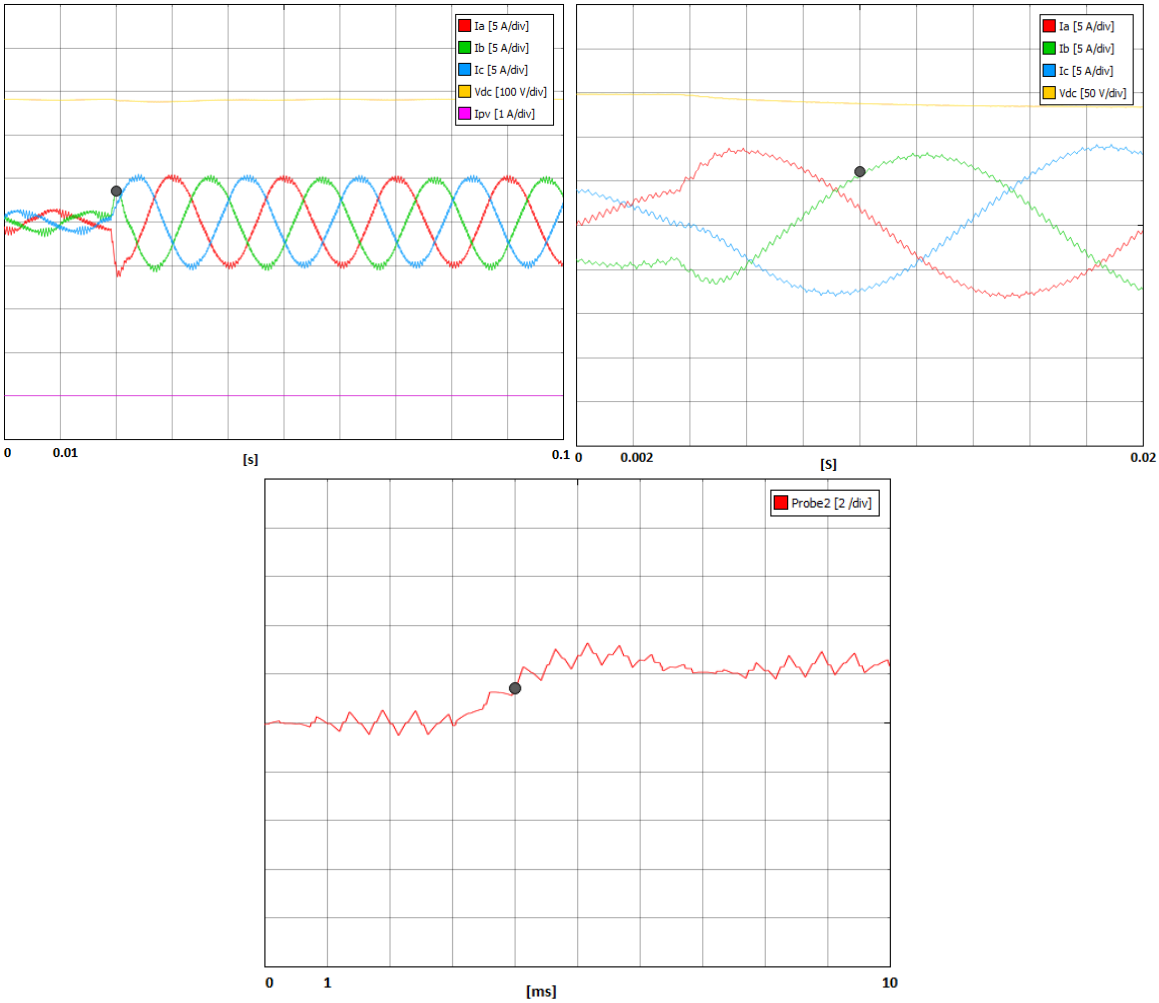

Figure 3.21: 4 Amps amplitude Step on Iq reference switching at 2 kHz.

Table 3.2 shows the simulated time constant at every tested switching frequency and the error respect the calculated ones. It is observed that the simulated time constants are lightly inferior to the expected ones, although it is considered that the values are positives.

Switching frequency [kHz]	Theoretical time constant [ms]	Simulated circuit time constant [ms]	Error [%]
10	0.22	0.2	9,1%
5	0.44	0.36	18 %
2	1.1	0.97	12%

Table 3.2: Comparison between theoritcal and simulated time constants on current loop.

Finally, figure 3.22 shows the current amplitude with three step changes and how the system follows properly the reference with stability in a large period of time.

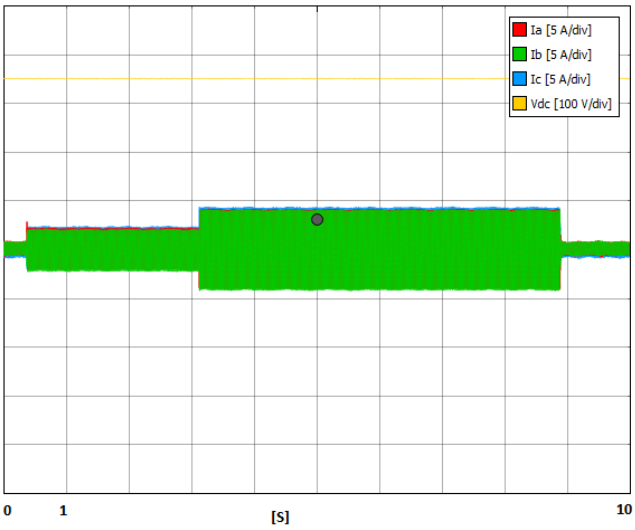

Figure 3.22: AC current grid amplitude variation under step changes.

3.5.2 Frequency and Grid Voltage Phase Steps

To prove the stability of the control, some tests have been done a changing the grid voltage phase or the grid voltage frequency to see the response of the system under grid changes. These tests are done with a switching frequency of 10 kHz.

Figure 3.23 shows the current and voltage control response to a 30 degrees step on grid voltage phase. A quick readjustment is done by the current loop with no overcurrent. Referring to voltage loop, it is observed a little perturbation on the DC-link voltage.

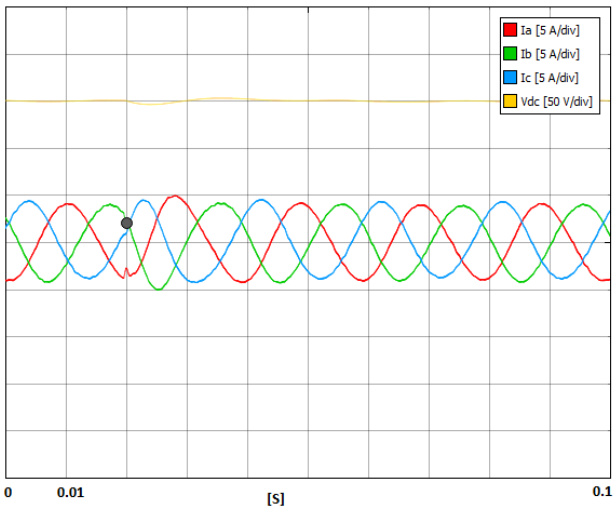

Figure 3.23: AC current and DC-link voltage under a 30º step change.

If the step is of 90 degrees, it is shown in figure 3.24, how the control achieves stability but there is overcurrent with peaks of 10 amps and also the DC-link voltage experiments a disturbance of, approximately, 20V. In a real system, the overvoltage would be easily assumed, although the overcurrent could be big enough to trip the system protections and stop its performance.

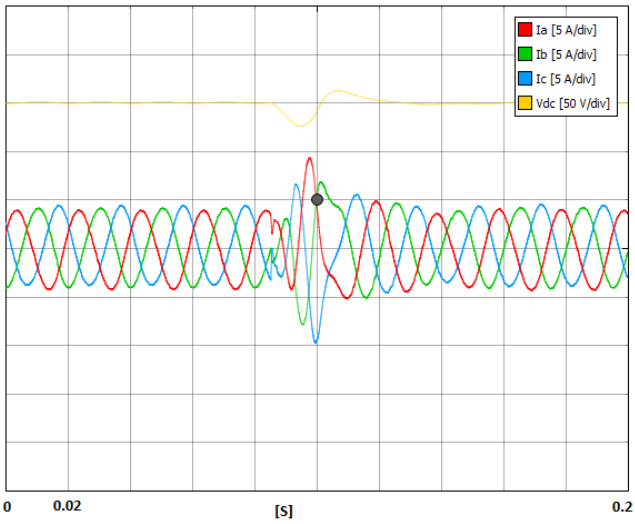

Figure 3.24: AC current and DC-link voltage under a 90º step change.

Finally, the same test has been carried on with a step of 180 degrees. It is shown that when the controller tries to correct the change, it becomes unstable. Although the system reaches the stability back again, in a real system the protections would have actuated and the system would stop.

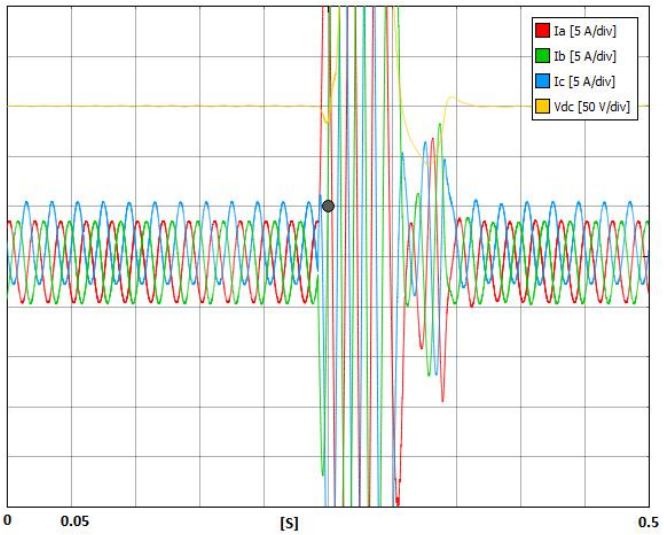

Figure 3.25: AC current and DC-link voltage under a 180º step change.

Therefore, it can be assumed by the simulations, that the system could be prepared to hold a step up to 90 degrees approximately, but it will probably lose control or make emerge system's protections with bigger steps on AC voltage phase.

The last test consists of a step on the grid frequency, changing from 50 Hz to 60 Hz. In this case, the PLL actuates fast by correcting the inverter current frequency with only a little perturbation observed, which is easily assumed by the system without carrying on problems on the control.

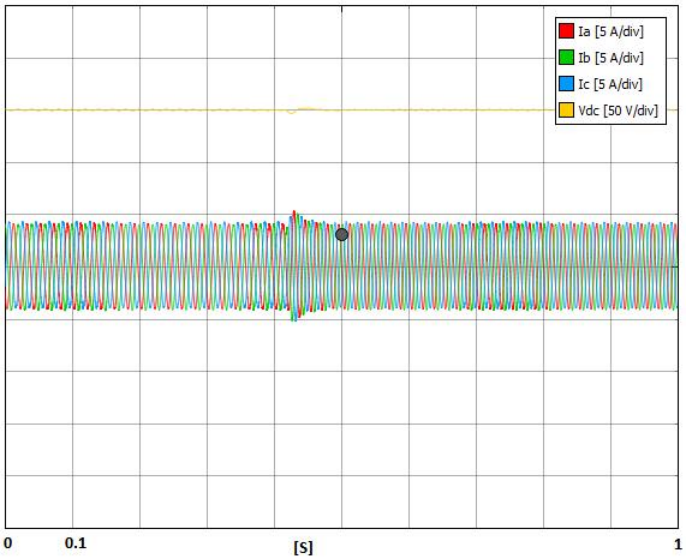

Figure 3.26: AC current and DC-link voltage under a grid frequency step from 50 Hz to 60 Hz.

3.5.3 Voltage Loop

Once IGBTs start to switch, a peak of current appears while the controllers start to actuate. Figure 3.27 shows the start of the controller and switches at 10, 5 and 2 kHz. The voltage reference is set to 280V in order to avoid a big step which could carry a high overcurrent. It is remarkable that as switching frequency decreases, the overcurrent and overvoltage increase. At 10 kHz it is observed a typical response to a first order system. While at 2 kHz, a 20 V overvoltage and a peak of current of 10 A appears.

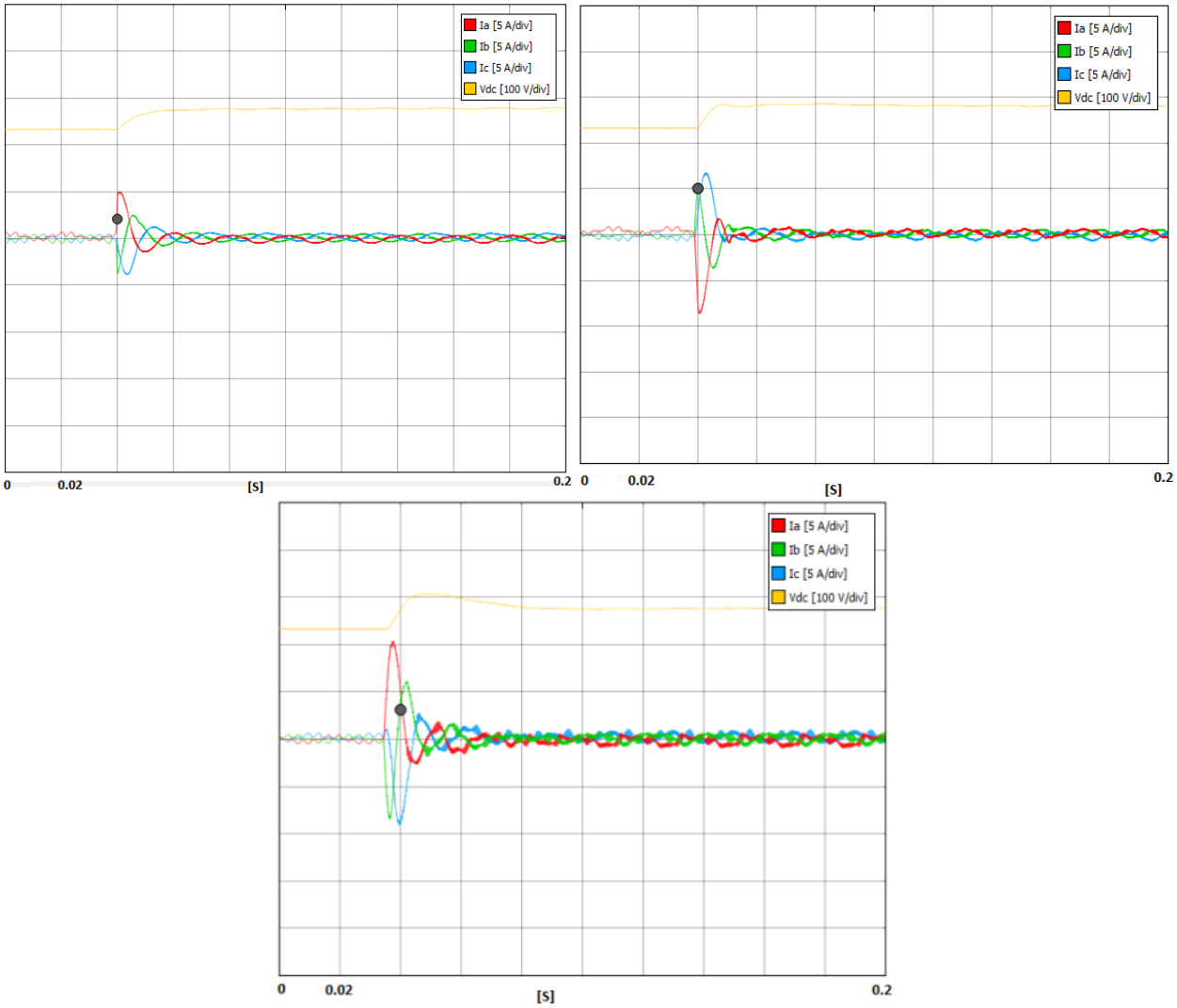

Figure 3.27: Performance on the start, switching at 10 kHz(Up-left),5 kHz(Up-right) and 2 kHz(down).

Switching frequency [kHz]	Simulated circuit overcurrent [A]	Simulated circuit overvoltage [V]
10	5	0
5	8	2
2	10.5	16

Table 3.3: Overcurrent and overvoltage at different switching frequencies.

To test the voltage loop, it is done by applying step changes of 50 V, specifically from 300 V to 350 V. It is designed to have a time constant given by (3.23), where is shown the time constant at 10 kHz.

$$\tau = \frac{1}{2\pi f_{BW}} = \frac{14*14}{2\pi*10000} = 3.12\ ms \qquad \textit{Equation 3.23}$$

Switching frequency [kHz]	Theoretical time constant [ms]	Simulated circuit time constant [ms]	Error [%]
10	3.12	6.61	111,85%
5	6.24	7.41	19.39 %
2	12.48	11.6	7.05%

Table 3.4: Comparison between theoretical and simulated time constants.

As it is seen in table 3.4, the error is decreasing with the bandwidth (proportional to switching frequency). This could be due to physical system limitations or because the controller enters into saturation and the response becomes slower.

Figure 3.28 shows the step response explained for each switching frequency. It results evident how the response becomes slowly as the switching frequency decreases, as expected.

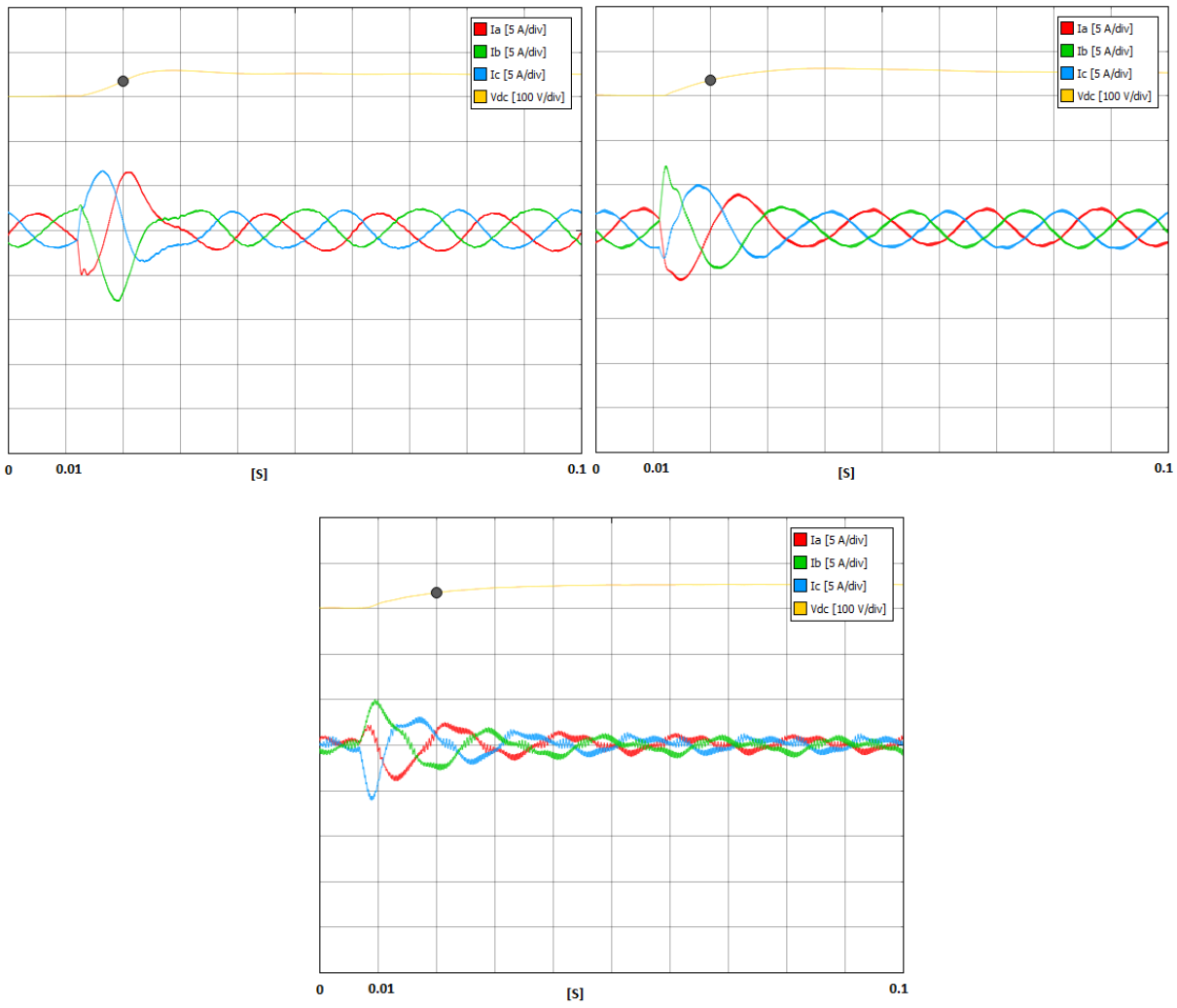

Figure 3.28: DC voltage step,, switching at 10 kHz(Up-left),5 kHz(Up-right) and 2 kHz(down).

Finally, figure 3.29 shows the response, in a large range of time, in order to show the stability of the control and that the systems follows all the changes of reference. It is also observed how every change carries an overcurrent due to the current loop action.

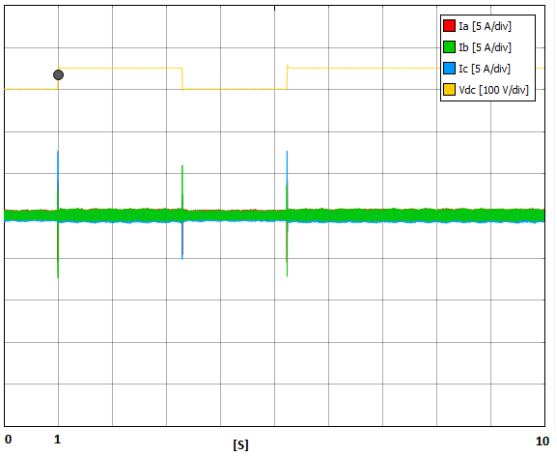

Figure 3.29: : DC voltage amplitude variation under step changes.

3.5.4 Boost Inductance Current Loop

To test the boost inductance current loop on the boost converter, a normal DC voltage source is used instead of using a PV source. This is done to be able to generate different references on the current, and not getting the reference from the MPPT algorithm.

As done with the other loops, the response will be compared to the theoretical time constant, to evaluate the performance of the controller. The boost inductance current loop is done with a bandwidth fourteen times lower than the sampling frequency, and its theoretical time constant at 10 kHz is given by (3.24).

$$\tau = \frac{1}{2\pi f_{BW}} = \frac{14}{2\pi * 10000} = 0.23\ m \qquad \textit{Equation 3.24}$$

Figure 3.30 shows the dynamic response to a step change of 1 A on the current reference at 10 kHz (left), and the same step at 5 kHz (right). At 10 kHz, it is appreciated a little overshoot, while at 5 kHz this overshot disappears and the response becomes slower. It is also appreciated the increase of the current ripple due to the decrease of the switching frequency.

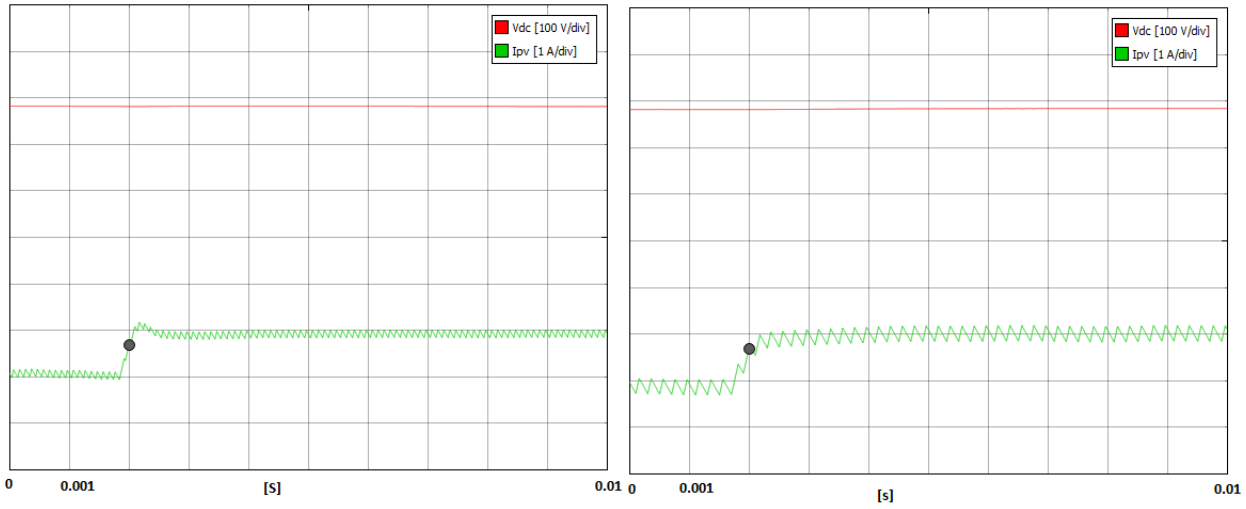

Figure 3.30: 1 A amplitude step to inductacance current switching at 10 kHz (left) and 5 kHz (right).

In table 3.5, it is compared the theoretical time constant with the simulated ones at both frequencies.

Switching frequency [kHz]	Theoretical time constant [ms]	Simulated circuit time constant [ms]	Error [%]
10	0.23	0.20	13%
5	0.46	0.32	26 %

Table 3.5: Comparison between theoretical and simulated time constants.

Finally, it is shown in figure 3.31, the behavior under continuous step changes at a large period of time.

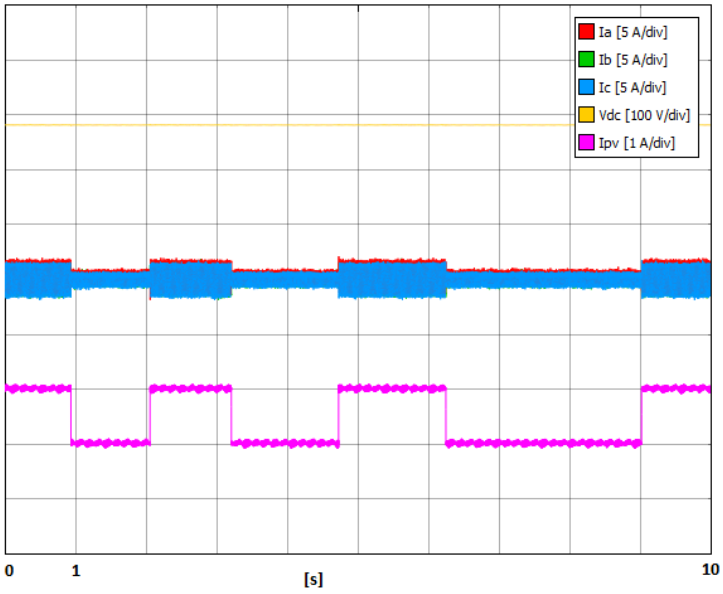

Figure 3.31: Inductance current amplitude variation under step changes.

3.5.5 MPPT

In this chapter, it is presented the performance of all the system simulated and experimental, with all its modules working, including the MPPT algorithm. Figure 3.32 shows the characteristic curve of the solar panel emulated on the simulations. With an open circuit voltage of approximately 225 V and a short-circuit current of 4.1 A. Its maximum power point is located on 3.84 A and 182.30 V, developing a maximum power of 700.08 W.

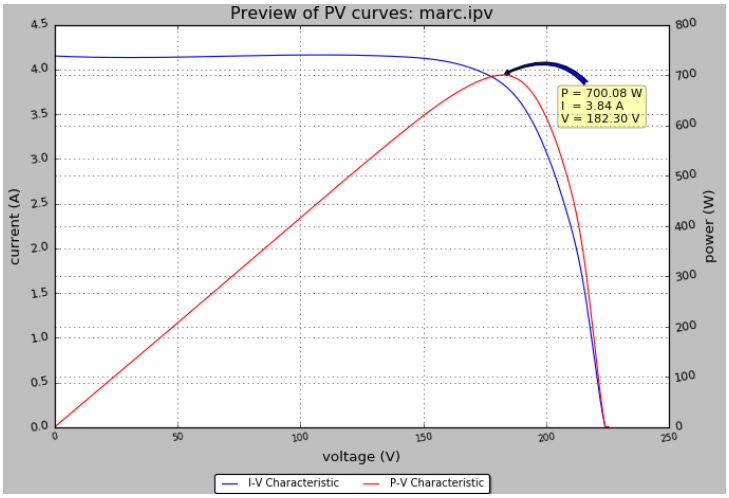

Figure 3.32: I-V and P-V curve characteristic of the simulated PV source.

With this model of PV source, it has been tested the algorithm with a step on the current of 0.05A and an update frequency of the algorithm of 200 Hz.

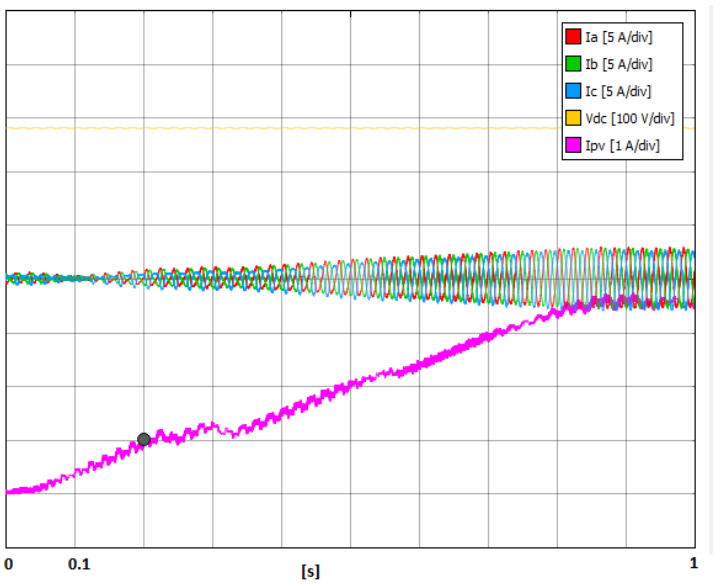

Figure 3.33: Evolution of the system due to MPPT algorithm performance.

As it is observed at figure 3.33, the MPPT algorithm takes around 0.85 seconds to achieve the maximum power point, this time could be reduced or increased by increasing or reducing the step or the update frequency (the two degrees of freedom that allows our MPPT). So it has been tuned with the aim of achieving a compromise between speed and fluctuations.

It is also observed how the inverter current increases proportionally to the PV source current, in order to extract the maximum power. The voltage loop grants that while all this exchange of power is taking place, the DC-link voltage maintains its level stable as expected.

4. GCC – EXPERIMENTAL RESULTS

Once the control software is verified and tested in the simulations, experimental test setup is organized in the laboratory.

In this chapter, the devices and the way in which they are interconnected to form the whole setup are explained in detail. Setup is built around LARA-100, which will be the main device. The controller is implemented in the same DSC used to simulate the system.

Finally, the performance and the results extracted from the tests are presented and evaluated.

4.1 LARA-100

LARA-100 is a platform designed for Power Electronics control development, research and education, which allows being re-configured and re-used according to the present needs. It interfaces with popular controllers such as Texas Instruments C2000 series. The parts of LARA-100 can be summarized as shown in figure 4.1.

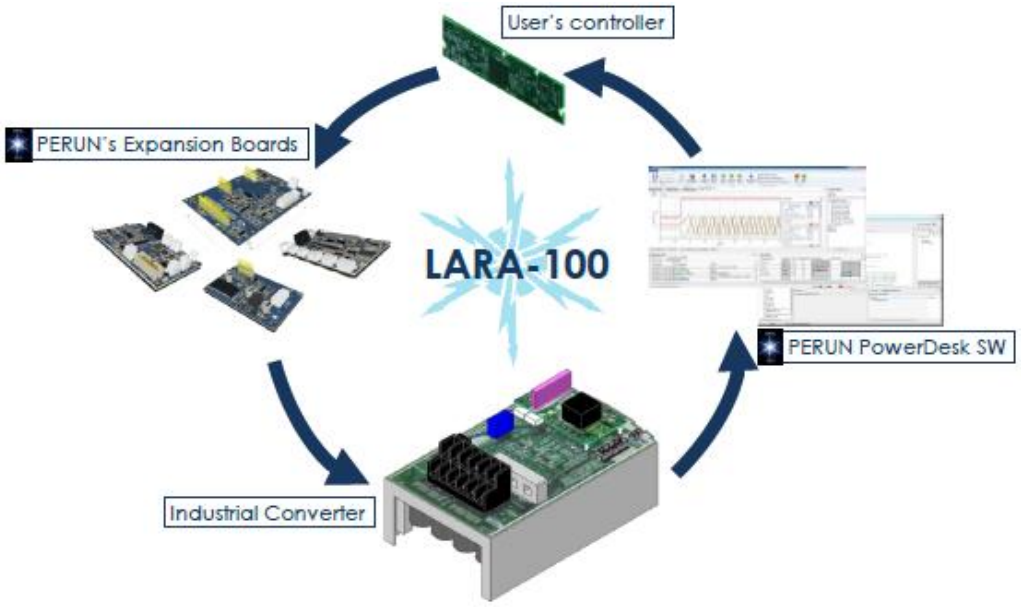

Figure 4.1: LARA-100 main components [20].

The hardware contains an industrial converter and LARA-100 PowerBox. This PowerBox includes all the expansion boards and PERUN PowerDesk (its software).

4.1.1 Expansion Boards

LARA-100 Expansion Boards are:

- LARA-100 Motherboard. It is the main board interfacing power electronics stage and the controller. The role of this board is to extend system's functionalities by hosting the other expansion boards. It also provides a USB interface, a UART connection, and an on-board XDS100 JTGA programmer/debugger. The Pinout of the board is placed in the annex.

Figure 4.2: LARA-100 Motherboard [20].

- LARA-100 Application Boards. There are different types of boards depending if the user considers motor drive applications or grid-connected applications. In this case, the application board used is the one shown in figure 4.3.

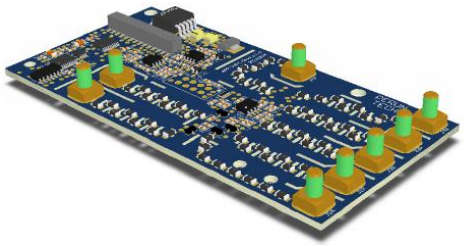

Figure 4.3: LARA-100 Application board [20].

This board serves as a transducer of four differential voltages, from a range of -800V to 800V, into microcontroller fitted voltage levels (0V to 3V). They may be used for either AC voltages or unipolar voltages.

- LARA-100 Communication Boards. These boards are solutions to form complex systems like smart-grids, connecting different platforms through Ethernet, CAN or RS-485. This configuration of this board is shown in figure 4.4.

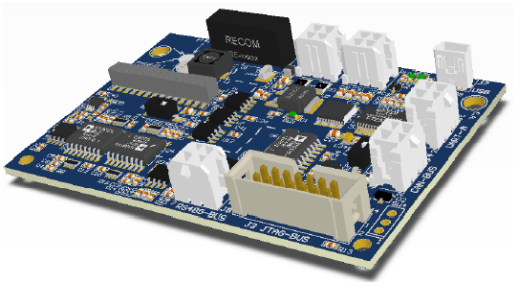

Figure 4.4: LARA-100 Communication boards [20].

As said, different types of communication and connectivity are contained in this board such as CAN, RS-485, UART, and USB. All these communication interfaces are designed for operation in especially-harsh environments.

- LARA-100 General Purpose Input Output (GPIO) Boards. This board includes all sort of digital and analog input and output circuitries. It allows interfacing 6 digital inputs, 6 digital outputs, 3 analog inputs and 3 analog outputs.

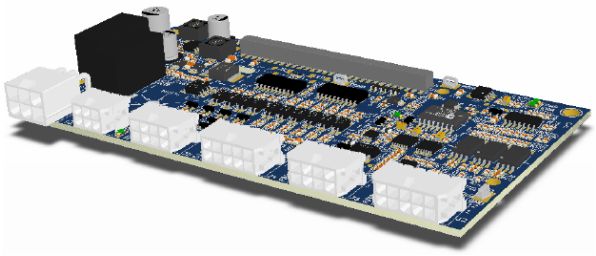

Figure 4.5: LARA-100 General Purpose Input Output board [20].

4.1.2 LARA-100 Power Stage

Power Stage is built in order to support different applications. It is possible to operate as different converters such as single-phase or three-phase inverter, buck, boost, etc. Its electrical scheme is shown in figure 4.6.

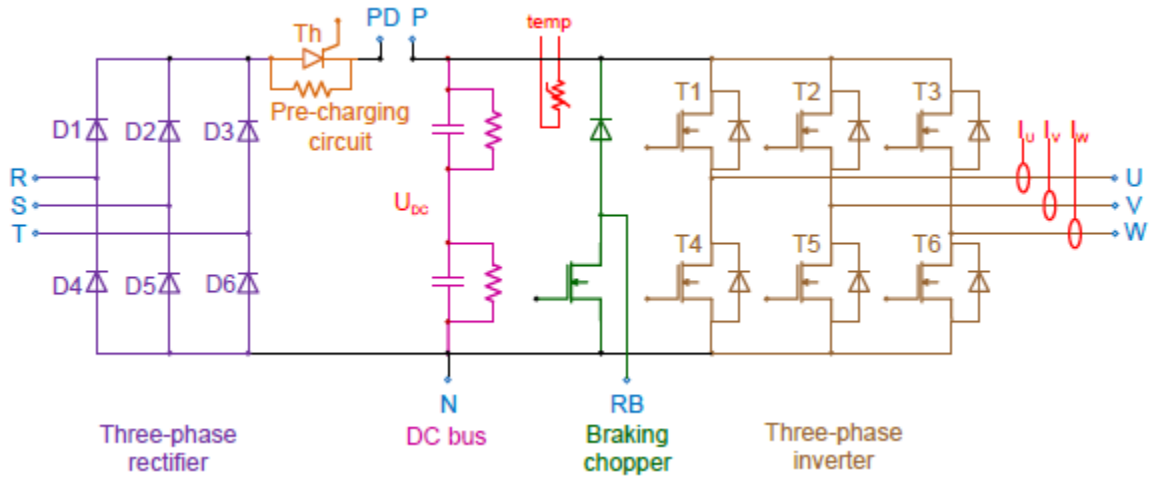

Figure 4.6: Electrical scheme of LARA-100 power stage [20].

LARA-100 Power Stage contains a three-phase rectifier, pre-charging circuit, DC bus, braking chopper and three-phase inverter. It also includes an interface with measurements like the inverter output currents and DC-link voltage.

4.1.3 PERUN PowerDesk

PERUN PowerDesk is the software that allows debugging, profiling and monitoring LARA-100 performance or any DSC-driven processor device. It has a wide range of functionalities, such as advanced digital oscilloscope and provides direct access to device memory. Figure 4.7 shows the Main Window of the software with its tools.

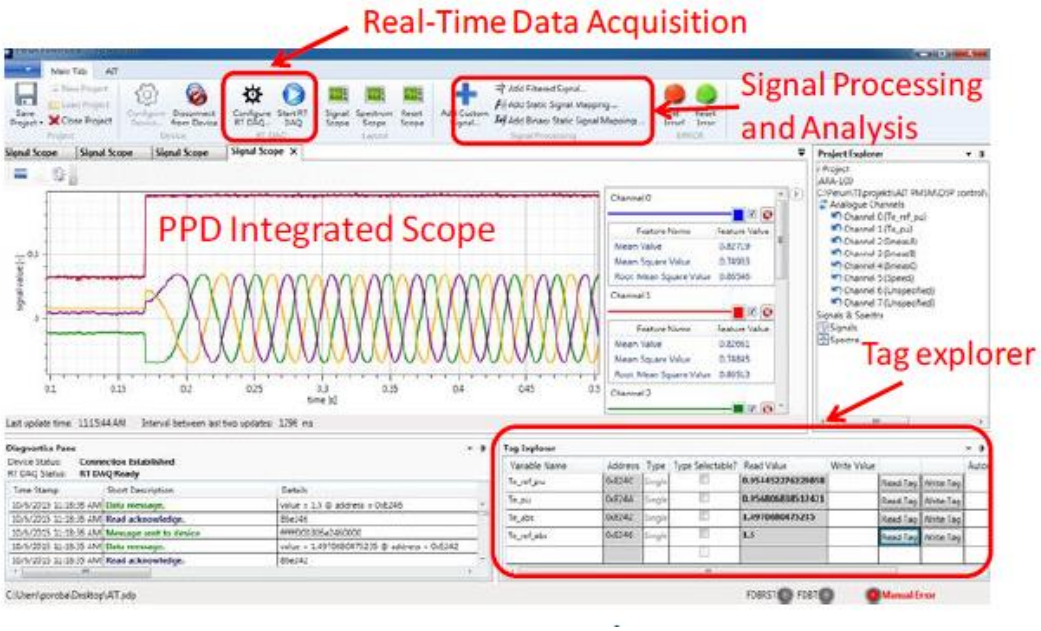

Figure 4.7: Main window of PERUN PowerDesk software [21].

PowerDesk also offers a Tag Explorer with access (read or write) to all variables and parameters defined by the user and signal processing and data visualization components. All these tools help the user to design new control algorithm. It makes possible to access LARA-100 with languages such as python or platforms like MATLAB/Simulink.

4.2 Grid Simulator

Grid simulator from Regatron is a full 4-quadrant system operation with programmable parameters. It is possible to variy frequency, phase angle, amplitude, to make step changes and impose harmonics. Its power ratings are 50 kVA and it is a successful tool for application fields like testing solar inverter equipment.

Figure 4.8: Full 4-Quadrant grid simulation system [22].

Regatron is supplied with a software which is used to run the system and the protections, to make the environment safe. The software allows programming and offers data acquisition, storage, and documentation.

4.3 Delta Elektronika DC Power Supply

To emulate the PV panel and be able to work in the laboratory, a delta elektronika DC power supply is employed. It is a two-quadrant power supply which confers the possibility to program its performance with an Ethernet interface. The used model is SM 660-AR-11, which has the ranges shown in table 4.1. Delta is protected against all overload and short circuit conditions.

SM 660-AR-11	**0 – 330 V**	**0 – 11 A**
	0 – 660 V	0 – 5.5 A

Table 4.1: SM 660-AR-11 voltage and current ranges.

To simulate a photovoltaic I-V curve, an interface module "INT MOD SIM" is used [23]. This module communicates with its software via Ethernet, which is shown in figure 4.9.

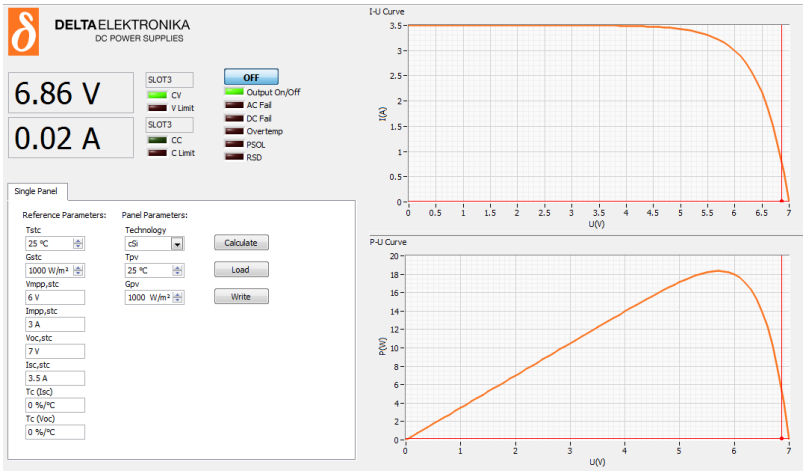

Figure 4.9: Main window of Delta Elektronikia software.

The simulation interface software allows generating an I-V curve, in an easy way by adjusting the reference parameters as desired. It also allows seeing the point of the curve where the source is working, what makes this application very suitable for testing MPPT algorithms.

4.4 Experimental Test Setup

The circuit has been built with five principal elements. Each element has the role shown in figure 4.10, where is presented every device with its role in the setup.

- LARA-100. Includes the inverter, boost converter switch, DC-link with its capacitor, and electronic boards (including DSC).
- Transformer. A transformer has been used to perform as an RL filter between inverter and grid.
- Regatron. It is used as an AC source simulating the grid.
- Inductance. An external inductance is needed to complete the boost converter.
- Delta. It is used as a PV source emulator.

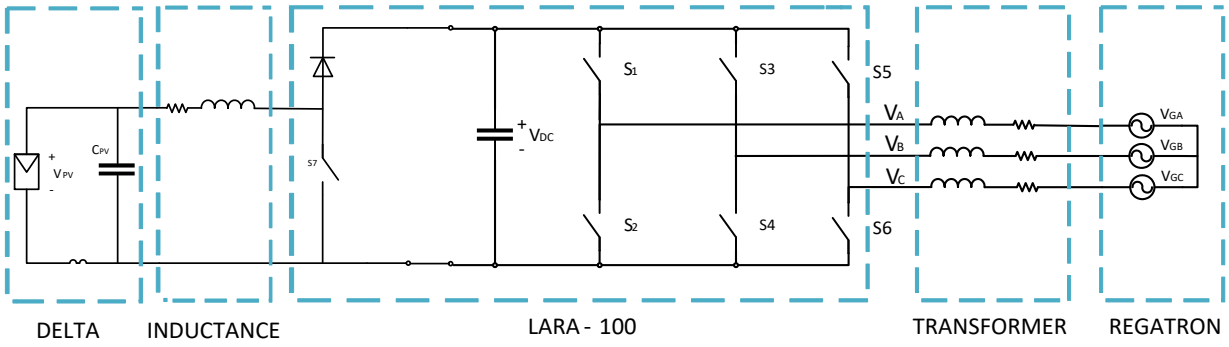

Figure 4.10: Relation with the electrical circuit and the elements used.

One of the aims of the project is to achieve a system integrated as much as possible, for this reason, instead of using an external boost converter or using a second LARA-100, it has been decided to use the braking chopper switch and the diode in its leg as part of the boost converter. The braking chopper is placed in LARA-100 as shown in figure 4.6.

Figure 4.11 shows the setup with all its devices. Regatron, Delta, LARA-100, transformer, and boost inductance are shown among other devices used as Oscilloscope or a laptop. All connections are done and also all the needed measurements are wired to test the setup. All these connections are explained in the following section.

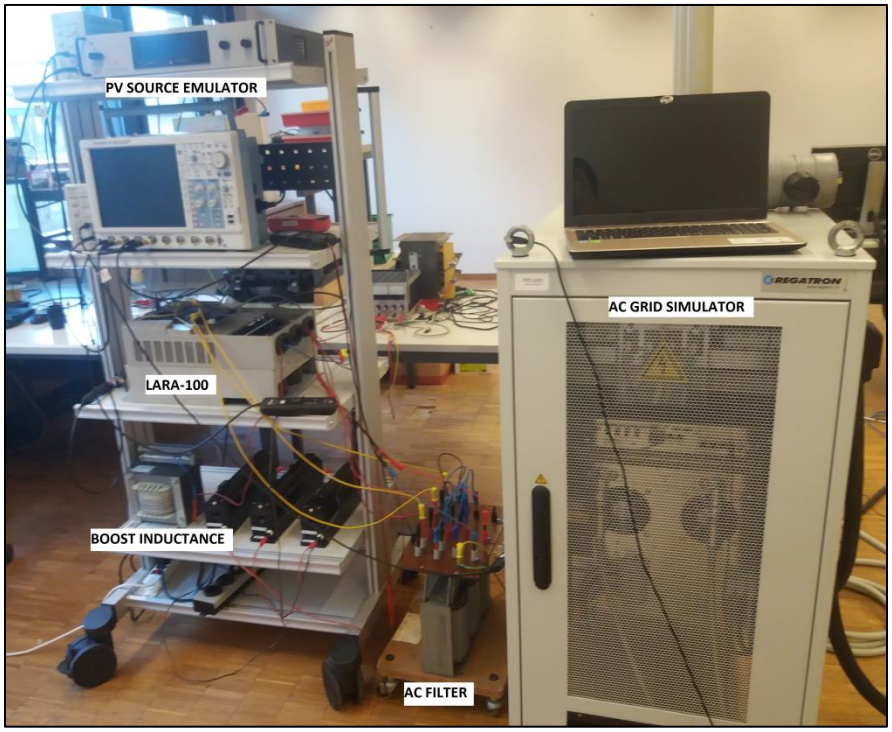

Figure 4.11: Experimental setup tested in the laboratory.

Circuit parameters remain equal to the simulated ones, as these were designed to match the experimental system.

4.4.1 System Modifications

LARA-100 uses GPIO34 to switch the braking chopper IGBT, but on HIL there is not the option to use this PIN. The adopted solution is to use different modules although both will be configured the same way.

GPIO34 is not configurable as an ePWM output, but it can be configured as an enhanced Capture input/output. This module is essentially used for Speed measurements of rotating machinery, elapsed time measurements between position sensor pulses, between other applications.

Although it is not its principal use, eCAP module can be used to build a single-channel PWM generator. The counter operates in count-up mode and the CAP1 and CAP2 registers become the active period and compare registers, respectively. In the other hand, CAP3 and CAP4 registers become the period and capture shadow registers, respectively. So this module can be used to modulate the boost converter. The signal is shown in figure 4.12.

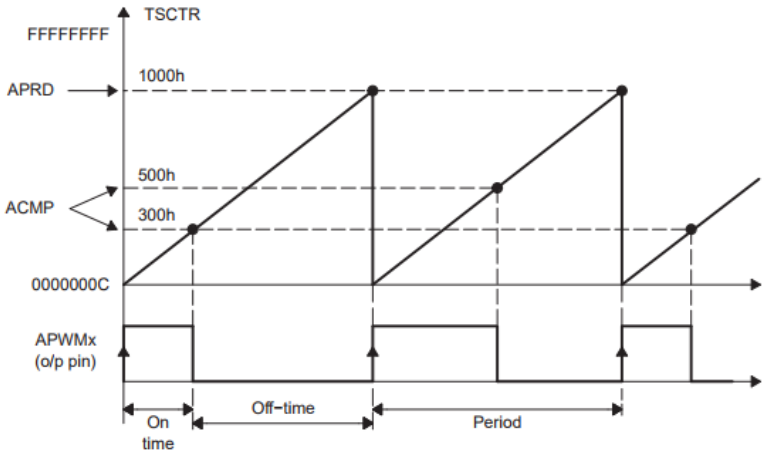

Figure 4.12: PWM signals of eCAP module [18].

And it is coded as follows.

```
GpioCtrlRegs.GPADIR.bit.GPIO34 = 1;        // Set as output
GpioCtrlRegs.GPBMUX1.bit.GPIO34= 1;    // BOOST SWITCH as APWM
ECap1Regs.CAP2=_IQmpy(10000,D); //10kHz.
```

4.4.2 LARA-100 Connections

As shown in figure 4.6, AC current and DC link voltage measurements are already wired, so it is not necessary to do any change. Connections U, V, W will be wired with the three-phase output of the transformer.

Connections P (positive) and N (neutral) will be wired with a resistor in parallel with the capacitor. Inductance's output is wired with RB connection to form the boost converter. Connections RST are not used.

AC grid voltages generated by grid simulator are measured directly. LARA-100 offers GPIO board, where there is the possibility to carry out these connections. Each phase is wired to pins J1P, J2P and J3P. As GPIO board carries out the transduced differential voltage between the pair of pins (for example J1P and J1N), J1N, J2N and J3N will be interconnected and wired with the neutral in the input of the transformer.

GPIO board is in charge to carry the measurements to the controller board using analog input channels ADCIN-B0, ADCIN-B1, and ADCIN-B2, respectively.

Finally, pins J4P will be used to measure the PV voltage, using ADCIN-B3 analog input channel.

4.4.3 Transformer Connections

The transformer has a 1:1 turns ratio and is used as a filter, so it is not wanted a phase displacement or a change of voltage values. To avoid a change of phase angle, both sides of the transformer will be connected with a star configuration.

The nominal values of the used transformer are the following ones.

$$S_N = 3\ [kVA] = \sqrt{3} * 380 * I_N\ ;\ I_N = 4.56\ A \qquad \textit{Equation 4.1}$$

To reach a ratio equal to 1, it is necessary to connect in series the 2 inputs. This is done as shown in figure 4.13.

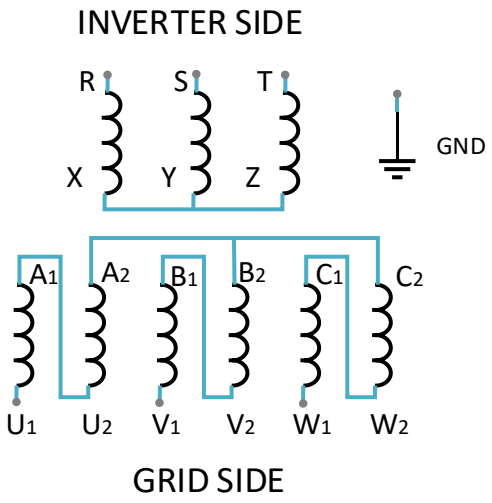

Figure 4.13: Transformer connections.

Although the characteristics of the transformer are given, a short-circuit test is done to ensure that the values are accurate. Firstly, it is calculated de nominal current of the transformer with (4.2).

$$P_N = 3\ [KVA] = \sqrt{3} * 380 * I_N \qquad \textit{Equation 4.2}$$

$$I_N = 4.56\ [A] \qquad \textit{Equation 4.3}$$

The test is done by applying an AC voltage to the transformer's grid side and short-circuiting the inverter side, as shown in figure 4.14.

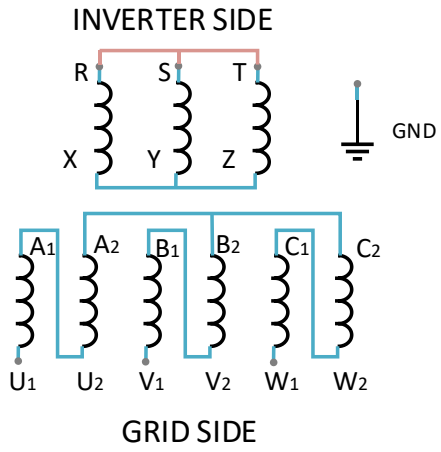

Figure 4.14: Transfomer connections on a short-circuit test.

With a digital multimeter, the resistor part of the transformer is calculated, and the iron losses in the transformer can be taken as negligible here.

Applying a phase voltage of 20 [V], it is measured a phase current of 3.2 [A]. It is important to work below the nominal current of the transformer to ensure its behavior is the expected. With all this, the results are as follows.

$$Z_{cc} = \frac{U}{\sqrt{3} I_N} = \frac{\sqrt{3}*20}{\sqrt{3}*3.2} = 6.25\ [\Omega] \qquad \textit{Equation 4.4}$$

$$Z_{cc}(\%) = \frac{\sqrt{3}*20}{380} * 100 = 9{,}12\% \qquad \textit{Equation 4.5}$$

$$Rx = 1.6\ [\Omega] \qquad \textit{Equation 4.6}$$

$$Z_{cc} = \sqrt{1.6^2 + (X^2)} \qquad \textit{Equation 4.7}$$

$$L = \frac{\sqrt{{Z_{cc}}^2 - 1.6^2}}{\omega} = 0.0192314\ [H] = 19.23[mH] \qquad \textit{Equation 4.8}$$

4.4.4 Grid simulator Connections

Wiring Grid simulator consists of connecting each phase of grid simulator output with each phase of transformer's input. For safety, earth connection is also wired with transformer's earth connection. On the grid side, it is connected to three-phase grid.

4.4.5 Current Transducer

LARA-100 doesn't offer the possibility to read current on the application board as it has been done with the AC and DC voltages. To satisfy the need of measuring PV output current, the solution adopted is to use an external current transducer in addition to the GPIO board.

This board offers a voltage analog input whose range is (-10V, 10V), and its input signal is isolated and conditioned to 0-3V for the controller board. The concrete connector is J2, which has the distribution shown in figure 4.15.

Figure 4.15: Pin distribution of J2 connector [20].

On the other hand, the chosen current transducer is LA 25-NP, from LEM [24]. This current transducer uses the Hall Effect and has multiple connections to generate different ratios of conversion. The characteristics of the used configuration are shown in table 4.2.

Ratio	2/10000
Primary nominal current	12 A
Primary maximum current	18 A
Nominal Output current	24 mA
Measuring resistance	330 Ω

Table 4.2 : LA 25-NP parameters.

The goal is to use the maximum of the range that offers LARA-100 GPIO board. With the shown characteristics, the range used is given by (4.9) and (4.10).

$$Nominal\ output\ voltage = I_N * r_T * R = \frac{12*2*330}{1000} = 7.92\ V \qquad \textit{Equation 4.9}$$

$$Maximum\ output\ voltage = I_{max} * r_T * R = \frac{18*2*330}{1000} = 11.88V \qquad \textit{Equation 4.10}$$

The maximum output voltage allowed by the transducer is bigger than the maximum voltage allowed by GPIO board, this would be a problem, but device's protections ensure that the system will not reach currents of 18A.

The current transducer needs also a power supply of -15 V and 15V, which can be taken from the same connector on GPIO board. Therefore, a total amount of 3 wires will be placed between the current transducer and LARA-100 board.

4.5 Results

The aim of this section is to show how the system is executed and present the results obtained from it. To prove its performance some tests have been done following the conditions on the previous simulations in order to carry on a comparison.

4.5.1 Run Experimental System

To be able to communicate with the DSC, it is necessary to charge the DC-link capacitor. LARA-100 boards run when the DC-link voltage reaches approximately 200 V. This is done by the AC side, connecting the inverter to the grid and applying voltage steps from 0 VAC to 100 VAC in RMS. At this point, the inverter is working as a three-phase rectifier charging the capacitor. The value of DC-link voltage is given by (4.11)

$$V_{OUT} = \frac{3\sqrt{3}}{\pi} V_m = \frac{3\sqrt{3}}{\pi} \sqrt{2} V_{RMS} = 233.9\ V \qquad \textit{Equation 4.11}$$

Figure 4.16 shows the typical current waveform of a rectifier, the grid phase voltage, and the DC-link voltage at it steady-state before running the control.

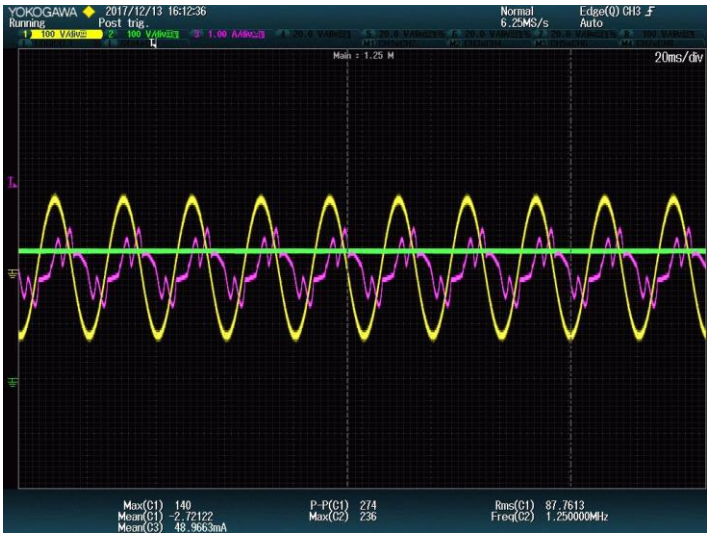

Figure 4.16: three-phase rectifier charging DC-link voltage. DC-link voltage (green), AC current phase A (purple), AC line-to-line voltage (yellow) (20ms/div).

Once the DC-link achieves the 200 V, LARA-100 starts to supply power to the motherboard, and the program can be turned over to the DSC. Before activating the inverter switches, it is proved that all measurements are working correctly and the PLL has synchronized with the grid satisfactorily.

4.5.2 Inrush Current

When electrical equipment is first turned on, a large current flow which exceeds the steady-state current value, it is called inrush current. The charge of the DC-link capacitor of LARA-100 will induce inrush current, which must be considered as it can damage electrical systems. The system sees the discharged capacitor as a short-circuit, the amount of inrush current into the capacitor is determined by (4.12) [25].

$$I_{INRUSH} = C\frac{dV}{dt} \qquad \textit{Equation 4.12}$$

To avoid a high inrush current, one possible solution is to carry on a "soft-start", this is the reason why the grid voltage is reached using steps of 20 VAC. Figure 4.17 shows one of these steps on grid voltage. It is observed how the DC-link voltage charges (green line) and while it is charging, an inrush current appears with a peak of approximately 8 A. If a high step was done on the grid voltage, the Regatron or LARA-100 protections would actuate as a consequence of an overcurrent error.

Figure 4.17: Inrush current caused by a 20 VAC step. DC-link voltage (green), AC current phase A (purple), AC line-to-line voltage (yellow) (20ms/div).

4.5.3 PLL

PLL loop must be able to synchronize with the grid at frequencies around 50 Hz. To test if this synchronization is effective, it is tested the three-phase inverter at 50 Hz and 60 Hz. The load in parallel with the DC-link capacitor has been removed in order to see the grid and inverter voltage at the same phase.

Figure 4.18: PLL synchronization at 50Hz (left) and 60 Hz (right). Line-to-line inverter voltage (blue),line-to-line gird voltage (green), and AC current phase A (purple) (10ms/div).

Figure 4.18, shows how inverter line-to-line voltage is at the same phase tan grid line-to-line voltage. Therefore, PLL is able to synchronize the inverter voltage at 50 Hz and 60 Hz. It is seen how DC-link voltage is set to 300 V and how AC current is around zero, as system is not connected to any load.

Synchronization is reached before switching,and can be observed by looking at grid voltage measurements in *dq* reference frame. A properly use of PLL leads into a V_q near 0 V and V_d given by the following equation.

$$V_d = \sqrt{2} * V_{phase(RMS)} = 141.42\ V \qquad \textit{Equation 4.13}$$

Figure 4.19 shows grid voltage measurements in dq frame in kV. It is seen how V_d is 141.5 V, near to the value shown in equation 4.13. Also, V_q is 0.33 V which means that PLL is well locked.

Expression	Type	Value
(x)= VParkD	long	0.1415035129 (Q-Value(24))
(x)= VParkQ	long	-0.0003300309181 (Q-Value(24))

Figure 4.19: V_{dq} variables measurements in Code Composer Studio in kV.

4.5.4 Current Loop

Using the same methodology as in the simulation tests, step changes in *Iq* reference are applied. Switching frequency and the sampling frequency are equal, and the same three different frequencies are tested 10, 5 and 2 kHz.

Using the same bandwidth as in the simulations, and for a frequency of 10 kHz, the desired time constant has a value of 0.22 ms.

A step amplitude change to the *Iq* reference variable on the experimental system, in this case, a 2 A amplitude step, has been done and the results are shown in figure 4.20, where the waveform corresponds to phase A current. It is seen that the shape of the of the current improves with its amplitude. This is presumably because low order harmonics are induced due to the saturation of the grid inductance. Also the time constant is clearly less than 1 ms, as expected.

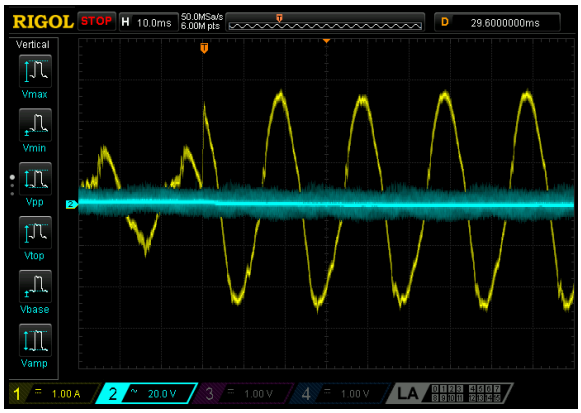

Figure 4.20: 2 A amplitude Step on Iq reference switching at 10 kHz. DC-link voltage (blue), AC current phase A (yellow) (10ms/div).

The same test has been done with the switching and sampling frequency set to 5 kHz. The time constant should be of 0.44 ms, although it is difficult to determine. It is seen that the response is slower and the ripple starts to increment, particularly on the peak. It can be determined that the current loop works satisfactorily at 5 kHz as shown in figure 4.21.

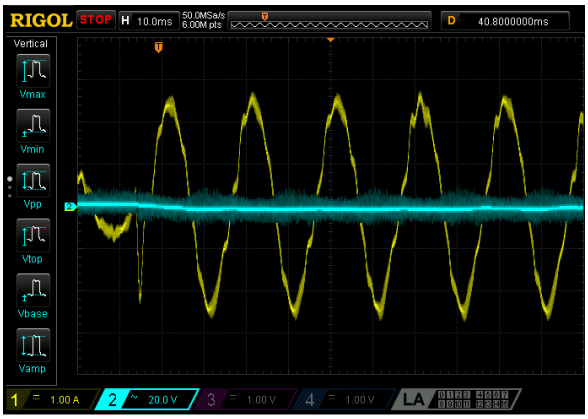

Figure 4.21: 2 A amplitude Step on Iq reference switching at 5 kHz. DC-link voltage (blue), AC current phase A (yellow) (10ms/div).

Finally, the test has been done with the sampling frequency set to 2 kHz. Although LARA-100 and the controller work properly with the inverter switches working at 2 kHz, it noticeable that the current wave is moving away from a sinusoidal wave, because of the low switching frequency.

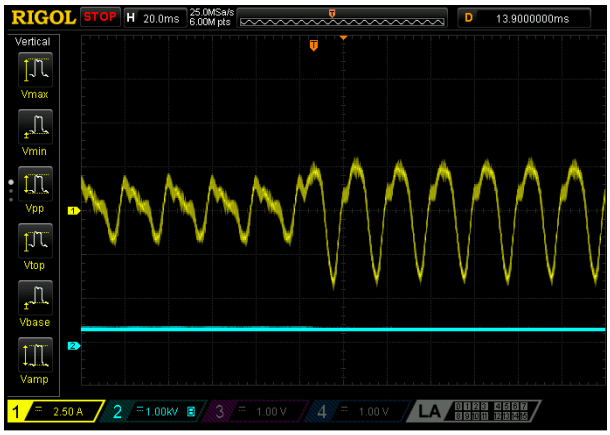

Figure 4.22: 2 A amplitude Step on Iq reference switching at 2 kHz. DC-link voltage (blue), AC current phase A (yellow) (20ms/div).

4.5.5 Voltage Loop

Figure 4.23 shows the start of the controller and operation at 10, 5 and 2 kHz. A small step is done on the voltage reference when starting the performance, as a large peak of current appears when the converter starts switching which could activate the system's protections. Therefore, the voltage reference is firstly set to 280V in order to avoid a big step which could carry a high overcurrent.

It is observed a typical response to a first-order system in the three frequencies. Also, it can be observed the typical current waveform of a three-phase rectifier before the IGBTs start to switch.

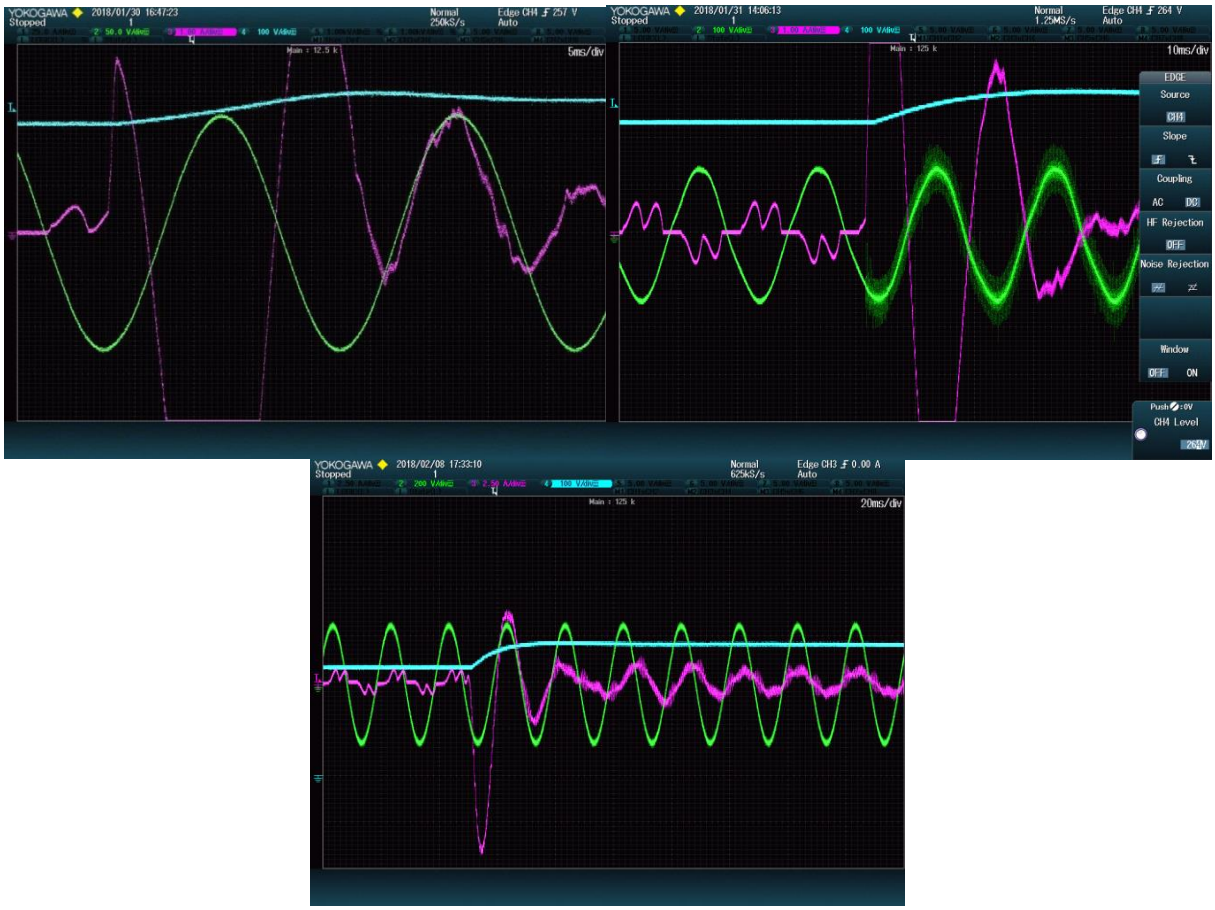

Figure 4.23: VSI start at 10 kHz (up-left) (5ms/div),5 kHz (up-right) (10ms/div), and 2 kHz (down) (20ms/div). DC-link voltage (blue), AC current phase A (purple), AC line-to-neutral voltage (green).

Figure 4.24 shows the response of the system to a 50 V step on the DC-link voltage reference at 10, 5, and 2 kHz. As in the previous test, a typical first-order system response is seen although, at 10 kHz, a little overshoot is detected.

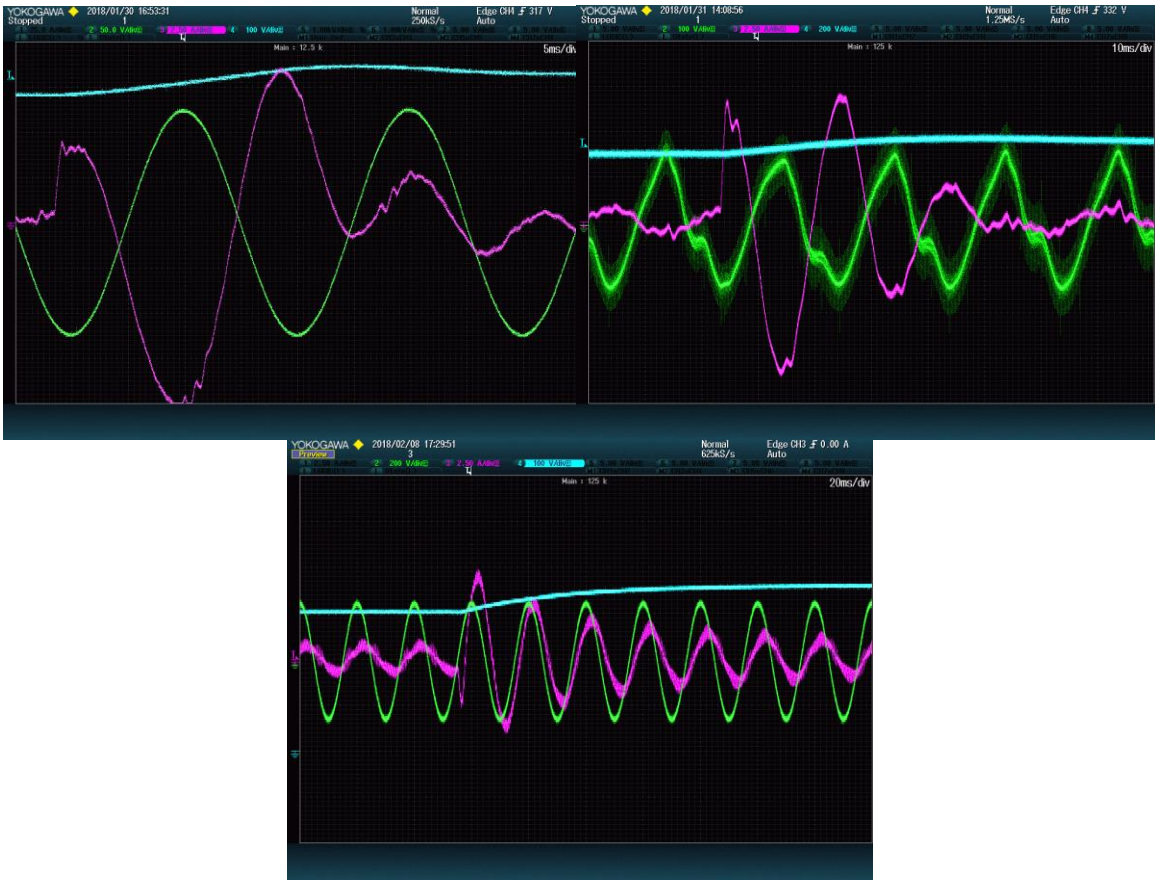

Figure 4.24: 50 V step at 10 kHz (up-left) (5ms/div),5 kHz (up-right) (10ms/div), and 2 kHz (down) (20ms/div). DC-link voltage (blue), AC current phase A (purple), AC line-to-neutral voltage (green).

Table 4.3 shows the time constants comparison for each working frequency. It is seen that experimental circuit time constants become slower than the simulated ones, although the results are acceptable. This could be caused by the difference between real system parameters and simulated system parameters.

Switching frequency [kHz]	Theoretically time constant [ms]	Simulated circuit time constant [ms]	Experimental circuit time constant [ms]
10	3.12	6.61	8
5	6.24	7.41	11
2	12.48	11.6	21

Table 4.3: Comparison of time constants on voltage loop.

4.5.6 Boost Inductance Current Loop

In order to test the boost inductance current loop, Delta power supply has been configured as a voltage source, instead of a PV source. This will allow generating different references on the current without using the MPPT algorithm. The aim of these tests is to evaluate the time response of the boost inductance current loop. These tests are only carried on at 10 kHz and 5 kHz.

Figure 4.25 shows a 1 A step on the boost inductance current reference sampling at 10 kHz. It is seen that the response is fast (clearly less than 1 ms) and how I_a (purple) and V_a (green) are in the same phase, as only active power is introduced to the grid. Also a little overshoot, very similar to the simulated one, is appreciated which is quickly damped.

Figure 4.25: 1 A step at boost inductance current reference at 10 kHz. DC-link voltage (blue), AC current phase A (purple), AC line-to-neutral voltage (green), Boost inductance current (yellow) (2ms/div).

It is observed how in the process of changing the boost inductance current reference, DC-link voltage control (blue) is able to keep stable the voltage level.

Figure 4.26, shows the same dynamic response switching and sampling at 5 kHz. The overshoot appreciated at 10 kHz disappears and the response becomes slower. It is also appreciated how the DC-link voltage keeps stable under this step reference.

Figure 4.26: 1 A step at boost inductance current reference at 5 kHz. DC-link voltage (blue), AC current phase A (purple), AC line-to-neutral voltage (green), Boost inductance current (yellow) (5ms/div).

Table 4.4 compares the theoretical time constant with the simulated and the experimental ones at both frequencies. The experimental time constants have been empirically calculated and its results might not be exact, although it is seen that all the values converge satisfactorily.

Switching frequency [kHz]	Theoretical time constant [ms]	Simulated circuit time constant [ms]	Experimental circuit time constant [ms]
10	0.23	0.20	0.2
5	0.46	0.32	0.5

Table 4.4 : Comparison between time constants on boost inductance current loop.

4.5.7 MPPT

Finally, the whole control with the MPPT algorithm is tested. The goal of this chapter is to show that the controller is able to extract the maximum power from the PV source by tracing correctly the MPP of the PV source curve.

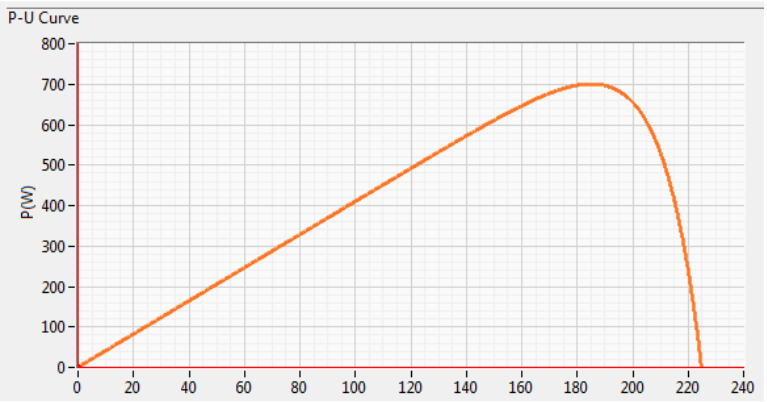

Figure 4.27: P-V curve emulated by Delta power supply.

Figure 4.27 shows the characteristic curve (P-V) of the solar panel emulated by Delta elektronika power supply. The PV source has been designed with the aim of being similar to the simulated one. Table 4.5 shows the parameters of the PV source curve.

PV source Parameters	
Vmpp	182.3 V
Impp	3.84 A
Voc	225 V
Isc	4.1 A
Maximum Power	700.08 W

Table 4.5: Reference PV source parameters.

The coded MPPT algorithm is defined by two parameters, the step of current reference and the update frequency, which are set to 0.05 A and 200 Hz respectively. It is important to find an optimal relation between these parameters to make the algorithm fast enough without causing disturbances.

Figure 4.28 shows the system sampling at 10 kHz once the MPPT algorithm starts to work. It is seen how the boost inductance current goes from 0 A to 3.8 A in approximately 0.7 s. The inverter current on phase A amplitude increases in order to extract the PV source power.

Figure 4.28: System response to MPPT algorithm sampling at 10 kHz. Line-to-line inverter voltage (blue), AC current phase A (purple), grid line-to-line voltage (green), Boost inductance current (yellow) (500 ms/div).

Also, to check the controller performance, it is tested the MPPT algorithm under irradiance steps, as shown in figure 4.29. It is seen that boost inductance current changes (due to the solar irradiance step) and this leads into a change on AC current injected into the grid. All this changes doesn't affect the DC-link voltage, which maintains its value at 300 V due to voltage loop control.

Figure 4.29: MPPT algorithm under irradiance steps, sampling at 10 kHz. Line-to-line inverter voltage (blue), AC current phase A (purple), grid line-to-line voltage (green), Boost inductance current (yellow) (1 s/div).

Figure 4.30 shows the same case from Delta's software point of view. Both curves are shown in which is appreciated that the maximum power is correctly traced. Also in the current and voltage measurements are shown on the right side of the screen, which match with the maximum power values.

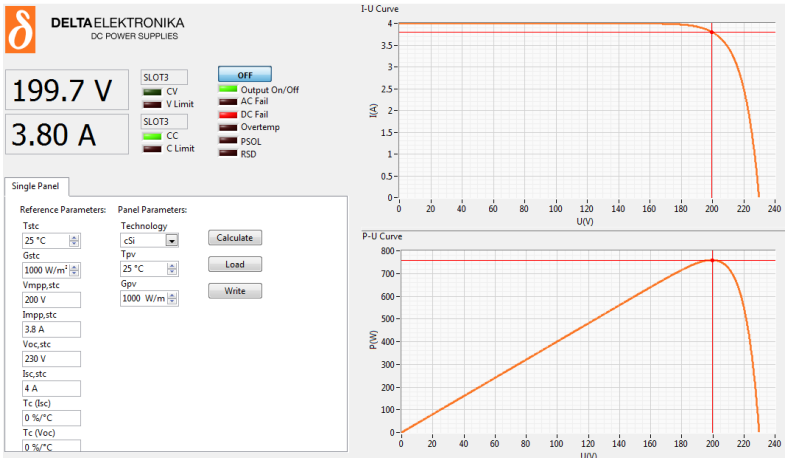

Figure 4.30: Delta software power point tracing during the controller performance at 10 kHz.

Also, MPPT algorithm has been tested with sampling frequency at 5 kHz but keeping boost switching frequency at 15 kHz as seen in figure 4.31. It is seen how MPPT algorithm becomes less effective and a little disturbance is detected as sampling frequency is reduced, although it keeps the system working on the MPP.

Figure 4.31: System response to MPPT algorithm sampling at 5 kHz. DC-link voltage (blue), AC current phase A (purple), AC line-to-neutral voltage (green), Boost inductance current (yellow) (10 ms/div).

Finally, figure 4.32 shows the delta software performance. Values remain near to the MPP although algorithm oscillations around this point become noticeable.

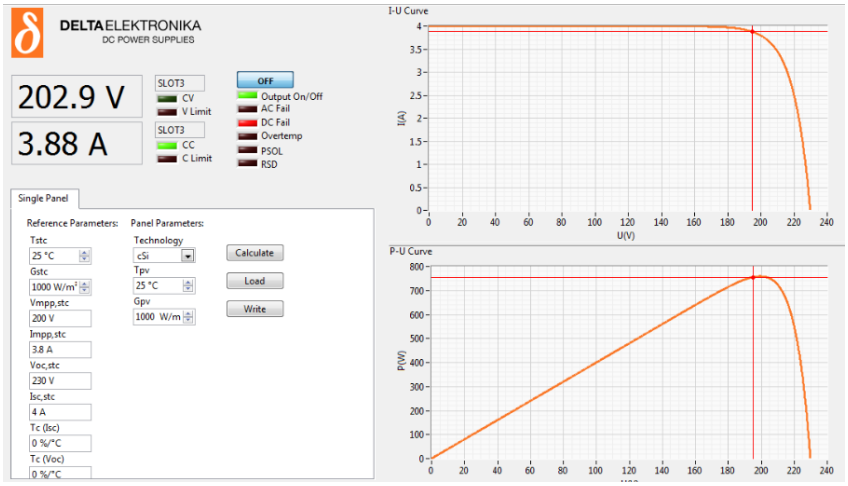

Figure 4.32: Delta software power point tracing during the controller performance at 5 kHz.

4.5.8 Results Conclusion

In a general way, it can be assumed that the controller achieved the goals as the experimental system works as desired and is capable of extracting the maximum power from the PV source and injecting it into the three-phase grid. This ensures that main loops are working and modulation is well implemented.

All loops have been compared with its mathematical model, and with the results extracted, it is seen that there is an assumable difference between them, as the time constants of the different loops are of the same order the modelled ones. The difference between them is due to different reasons. The experimental system is never completely known, physical parameters are calculated or given by datasheets, but are tied to an uncertainty which is not considered. Also, some parameters of the system such as losses are neglected in the modelling of the system, as it is considered that their effect upon the system is low.

Also, testing the experimental system at different switching and sampling frequencies allows to show that results are correct in all the working frequencies, and therefore, makes the results extracted more valid.

By the other hand, on voltage loop it is seen that at high switching frequencies the response is slower than the expected one. This can be due to a physical saturation on the transformer or a digital saturation on the controller; as if sampling frequency is slower the time constant gets closer to the theoretical one.

Conclusion

This thesis was proposed with the purpose of designing and implementing a power electronics unit interfacing a photovoltaic source with the three-phase grid, to verify experimentally the control theories proposed. For educational purposes, it has been checked that HIL helps in the development of the experimental setup, and that both system provide the same results.

The software and hardware used, allowed to implement an accurate control and therefore, efficient results have been obtained which allowed to evaluate them. A study of the experimental and the simulations results have been done to draw general conclusions. It can be assumed that the project achieved adequately the goals established.

To implement the prototype, the flow of energy through-out the system has been studied in order to be able to extract the maximum power from the photovoltaic generator at the different working conditions. All the control loops work in accordance with its mathematical model to generate the control signals necessaries to inject a three-phase sinusoidal current into the grid. Therefore, the behaviour of both simulations and experimental tests match the expectations.

Finally, the desired knowledge to implement the project has been achieved. The project has been very helpful to acquire knowledge beyond the master studies carried out. This thesis has allowed extending learning in power electronics, digital control, and electrical devices, among others.

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