Design of Low-Power Transmitter and Receiver Front End

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ABSTRACT OF THE
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This thesis focuses on the design of "RF front-end blocks" for the transmitter and receiver. The blocks include the low noise amplifier (LNA) and mixer down-conversion at the receiving side, while the power amplifier includes the pre-driver circuit, and mixer up-conversion at the transmitter side. All of the blocks were designed in a 65nm design kit. The basics of these RF blocks are first described in chapters two to four. After that, the general principle of operations is then described and different topologies are discussed. In chapter 5 the proposed design is discussed. The proposed design is composed of a differential IDCS narrow band LNA, with a passive down-conversion mixer on the receiving side, designed for bluetooth low energy (BLE) applications, that operates at 2.4 GHz with a 1.2 V supply voltage. The overall conversion gain at the receiving side was found to be greater than 13 dB with a double side band noise figure of 8.3 dB having a 1 dB compression point of -11.8 dB, and with IIP3 of -2.06 dBm having a power consumption of 251 μwatts. On the transmission side, a power amplifier with a pre-driver circuit and a passive up-conversion mixer has been designed to operate at a 1.2 V supply at the frequency of operation 2.4 GHz, having overall gain of 24 dB with maximum power added efficiency of 34% when using maximum output power of 11 dBm. The Cadence virtuoso design kit was used for simulation. Additionally, the layout considerations were discussed, followed by presentation of the post-layout results and graphs, and, finally, some conclusions have been drawn.

Keywords: RF Front End, LNA,Mixer, Power amplifier

Preface

First of all I wish to Thank Almighty ALLAH, for blessing me with everything and giving me courage at every stage of my life. I want to express special gratitude to my supervisor Professor Kari Halonen, for his guidance and support during this whole work, and my instructor Dr Shailesh Singh Chouhan for his precious guidance and motivation. Without their help I would never have been able to complete this work.

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Last but not least, I would like to dedicate this work to my family, my Mother Asfa Javed, Father Muhammad Aslam Javed and brother Owais Javed who always supported me during good and bad times, and always prayed for me; without their encouragement and support, I would never have reached the stage of life I am at now.

Otaniemi, 28.05.2018

Muhammad Annus Javed

Contents

Symbols and Abbreviations

Abbreviations

ANT	Area Network Technology
AC	Alternating Current
dBm	Decibel Refrence to Milliwatts
BER	Bit-Error Rate
BLE	Bluetooth Low Energy
CMOS	Complementry Metal Oxide Semiconductor
DC	Direct Current
DE	Drain Efficiency
DRC	Design Rule Check
IDCS	Inductive Degeneration Common Source
IF	Intermediate Frequency
IoT	Internet of Things
ISM	Industrial Scientific and Medical
LNA	Low Noise Amplifier
LO	Local Oscillator
LVS	Layout vs Schematic
MEMS	Micro Electromechanical System
NF	Noise Figure
NMOS	N-channel Metal Oxide Semi-conductor
PA	Power Amplifier
PAE	Power Added Efficiency
PMOS	P-channel Metal Oxide Semi-conductor
RC	Resistor Capacitor
RF	Radio Frequency
RFC	RF Choke
RLC	Resistor Inductor Capacitor
RMS	Root Mean Square
SB	Single Balanced
SOC	System on Chip
SNR	Signal to Noise Ratio
UNII	Unliscensed National Information Infrastructure
WLAN	Wireless Local Area Network
ZCS	Zero-Current Switching
ZDS	Zero-derivative Switching
ZVS	Zero-Voltage Switching

Symbols

A_v	Voltage Gain
C_{gs}	Gate to Source Capacitance
C_{gd}	Gate to Drain Capacitance
C_P	Parasitic Capacitance
C_{DB}	Drain to Bulk Capacitance
C_{SB}	Substrate to Bulk Capacitance
f_{RF}	RF frequency
f_T	Transit Frequency
F	Noise Factor
g_m	Transconductance of Transistor
G	Gain
G_m	Transconductance
$\overline{i_n^2}$	Noise Current
i_o	Output current
I_D	Drain current
I_{out}	Output Current
L_S	Source Inductor
L_G	Gate Inductor
L_D	Drain Inductor
N_A	Noise Power reffered to output
P_{in}	Input Power
P_{out}	Output Power
P_{avgout}	Average output Power
Q_{in}	Quality Factor
$R_{FullLoad}$	Full Load Resistance
R_f	Feedback Resistance
R_L	Load Resistance
R_S	Source Resistance
S_{11}	Input Scattering
$\overline{V_n^2}$	Noise Voltage
V_{DD}	Supply Voltage
V_{RF}	RF Voltage
V_{in}	Input Voltage
V_{out}	Output Voltage
V_{GS}	Gate-to-Source Voltage
V_{TH}	Threshold Voltage
X_L	Inductor impedance
Y	Admittance
Z_{RE}	Real Impedance
Z_{in}	Input Impedance
Z_O	Output Impedance
ω_o	Resonance Frequency
ω_{LO}	LO frequency
ω_{RF}	RF Frequency
η_{dmax}	Maximum Efficiency
γ	excess noise coefficient

1 Introduction

1.1 Motivation

In this modern era of technology and development, the importance of electronic devices can never be neglected because they have become a part of daily life. At the same time, the radio frequency and wireless market has dimensions beyond human imagination. This has resulted in challenges for the designers of integrated circuits. During the past decades, various standards for wireless communication have been introduced for short distance and long distance communication, and multi-standard wireless devices accommodate different standards into only a single chip called a System on Chip (SOC).

The Bluetooth standard was introduced to connect appliances, such as computers, cell phones, printers and TV by using the Industrial Scientific and Medical (ISM) band. Moreover, the widespread use of the Internet around the globe led to the development of the Wireless Local Area Network (WLAN) which has been introduced in the ISM and the Unlicensed National Information Infrastructure (UNII) band for high data rates in wireless communication. The technologies were specifically designed for sensor-based short range devices for data transfer. The two main requirements for designing such devices are the miniaturization of the devices and low power consumption. This has culminated in the remarkable development in sensor electronics and the Internet of Things (IoT) applications, as well as short range devices. The miniaturization of circuits and the reduction in cost are now possible due to the advancements in Complementary Metal Oxide Semiconductor (CMOS) and Micro Electro Mechanical Systems (MEMS) processes. However, the power consumption has yet to be scaled down to such an extent; therefore, minimum power consumption still needs to be fullfilled. Hence, reduced power consumption of these devices has become a widely researched topic within the field of integrated circuits.

1.2 Research Goals

Ultra-Low Power short range Radio Frequency (RF) devices have great potential for low power consumption through design and innovation. Therefore, it is a hot and relatively new topic of research in the design of the Integrated Circuit (IC) in comparison to traditional RF IC design. In order to realize this, several low-power radio standards have been introduced, such as Bluetooth Low Energy (BLE), Zigbee and Area Network Technology (ANT).

Transceivers with minimal power consumption are the key requirement for achieving portability. Within the transceiver, the element consuming the most power is the RF block. A transceiver consists of a transmitter and a receiver. The RF front-end blocks of a transmitter consist of a power amplifier and a mixer, and a Low Noise Amplifier (LNA) with a mixer on the receiver side. As the baseband signal functions

at a low frequency, it needs to be translated to a higher frequency for transmission. Therefore, an up-conversion mixer will be needed in order to translate the baseband signals to a higher frequency. Next, the signals need to be transmitted, but, at the same time, the signal strength should be strong in order to reach the desired distance after transmission from the antenna. Hence, a power amplifier is required which will amplify the signal strength. Additionally, the output impedance of the power amplifier must be matched with the antenna in order to transfer maximum power and to avoid signal loss caused by scattering.

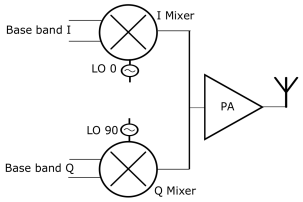


Figure 1: Transmitter RF Front End

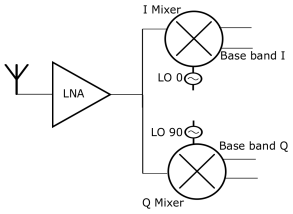


Figure 2: Receiver RF Front End

As the strength of the signal is known to be very weak, the LNA should therefore have gain and the lowest noise in the receiving chain because the noise of the LNA dominates in the receiver. Similarly, the mixer in the receiving chain should have low noise and high linearity. Therefore, the design architecture choices are based on different parameters, such as cost, power dissipation, complexity and other constraints required by the system, in order to fulfill the requirements of the communication system. The aim of the thesis is to design receiver and transmitter RF front-end blocks with ultra-low power consumption which will be implemented in CMOS 65nm technology for the BLE standard. Basically, four blocks are designed which follow the BLE standard. The blocks that are designed are discussed in the following chapters.

1.3 Specification for Bluetooth Low Energy

In this section we will review the specification for Bluetooth low energy and examine the calculation of front-end parameters.

1.3.1 Noise

The first step to design a Bluetooth Low Energy (BLE) receiver is to determine the noise figure specification allowed by the standard. BLE operates in the ISM band

between 2400-2483.5 MHz. The number of channels are 40 which have a channel spacing of 2 MHz, while the bandwidth of each channel is 1 MHz. The maximum Bit Error Rate (BER) in BLE is 10^{-3}, which has to be translated into minimum $SNR_{out,min}$ of 12 dB. BLE provides a sensitivity level of -70 dBm. In order to have a safety margin, it is necessary to take this into account due to non-idealities by calculating the minimum noise figure $SNR_{out,min}$ to be 12 dB as follows:

$$NoiseFigure = S_{in}|_{dBm} + IL - N_s|_{dBm} - SNR_{out,min}|_{dB} \quad (1)$$
$$= -80dBm - 2dB - (-114dBm) - 12dB = 20dB \quad (2)$$

Where $S_{in}|_{dBm}$ is the sensitivity level for BLE, $N_s|_{dBm} = 10log(kTB)$ is the in-band noise source depending on the Boltzmann constant and absolute Temperature (300K) as well as the signal Bandwidth(B), while IL is the insertion loss. With a 20 dB noise figure, the noise floor is given by [2]:

$$NoiseFloor = N_s|_{dBm} + NF = -114 + 20 = -94dBm \quad (3)$$

1.3.2 Linearity

After the noise figure, the other most important figure of merit for a receiver and transmitter in BLE is the linearity; how linear our system should be in order to qualify for the specification of Bluetooth Low Energy. The Inter-modulation test defines the linearity in terms of the intermodulation products IP3 and IP2. According to [2], the sum of the IM3 product and the $SNR_{out,min}$ must be lower than the sum of the sensitivity and the margin to have a signal to noise ratio larger than the minimum allowed. Therefore, the minimum IIP3 for the entire chain of the receiver is given by [1]:

$$IIP3 = \frac{1}{2}(3P_{int} - IM3) = \frac{1}{2}(3P_{int} - N_{floor} - Margin) \quad (4)$$
$$= \frac{1}{2}(3 * (-50) - (-94) - 6) = -31dBm \quad (5)$$

1.4 Thesis Overview

Chapter 1 provides brief overview of the Bluetooth Low Energy specification as well as the motivation behind this research work. Low Noise Ampifier topologies and an overview of the theoretical background of these topologies are reported in chapter 2. Chapter 3 provides a review of active and passive mixer topologies. Chapter 4 offers a brief description of power amplifier topologies. In chapter 5 implementation of the designed blocks with post-layout simulation results, as well as an overview of the layout considerations for the designed blocks is presented. Finally, the thesis including the main results of the blocks are summarized in chapter 6.

2 Low Noise Amplifier

The overall performance of the receiver is directly affected by the performance of the first active device. The signals received by the antenna are possibly weak, an amplifier is therefore needed to amplify those received signals. There are certain performance parameters which must be fulfilled by this amplifier. Typically this amplifier should amplify the received signal while ideally not adding any further noise to the signal. In practice, however, there is always some noise present. That's why the added noise should be the minimum as possible. Hence this kind of amplifier was named the low noise amplifier (LNA). The main design parameters in the LNA are the gain, noise figure and linearity. Linearity is also a crucial parameter in modern digital systems because the peak to average ratio of the RF signals is usually high. Therefore to reduce the intermodulation products in the wireless receiver, a high linear LNA is required [6]. In this chapter we will focus on the general performance parameters as well as different topologies which are taken into account while designing an LNA.

2.0.1 Noise Figure

The noise figure defines the noise performance of a device. As a signal passes through a receiver, noise is added causing the signal to noise ratio to decrease. An initial estimation of the noise provides a firm basis for the design and selection of LNA topology and receiver architecture. The noise factor is given by:

$$NoiseFactor = \frac{SNR_{OUT}}{SNR_{IN}} \tag{6}$$

while the noise figure is given by:

$$NoiseFigure = 10log(NoiseFactor) \tag{7}$$

The noise figure of an LNA should be as small as possible because it defines the noise figure of the receiver chain. According to the Friis equation, the noise factor of the entire receiver chain, when the devices are connected in cascade, is given by:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + ... + \frac{F_n - 1}{G_1 G_2 G_3 G_4 ..... G_{n-1}} \tag{8}$$

Due to this, the choice of topology is limited because from the above equation we can deduce that, for an LNA with a low noise figure only one device should contribute the noise, usually the input transistor. Therefore the source followers and common emmiters cannot be used to design an LNA [1].

2.0.2 Gain

Another parameter of the LNA which needs to be considered during design is the gain. As seen in the Friis equation (8) from the previous section, at least a moderate

gain is necessary in order to minimize the noise figure of the subsequent stages. However at the same time there is a tradeoff present between the noise figure, gain and linearity of the device. This is because a considerable high gain will decrease the noise figure of the subsequent stages while it will decrease the linearity at the same time. The power consumption must also be considered while designing the LNA as it also needs a trade off.

2.0.3 Linearity

As the LNA is the first block in the receiver chain it should be linear so that it can have high sensitivity as well as the capability to suppress interference. Mostly the LNA does not limit the linearity of the receiver; the baseband amplifier or the filter tend to limit the overall input of IP_3 or P_{1dB}. However it becomes critical in full-duplex systems as well as in the Wideband receivers which may receive a large number of strong interference signals [1].

2.0.4 Input Matching

The LNA interacts with the outer world through an antenna. Therefore its input must be perfectly matched with the impedance of the antenna for maximum power transfer to minimize losses.

2.1 Common Source Stage with Resistive Feedback

One of the topologies used in LNA design is the resistive feedback topology. In this topology, a PMOS current source is connected with a common source transistor with resistive feedback. This is shown in Figure 3.

In this figure the resistor R_f transfers the current to the input (gate of M1 transistor) by sensing the output voltage. M2 acts as a current source. The input impedance needs to be matched with the Rs. The circuit topology is valid as long as the transit frequency f_T of the transistor is higher than the frequency of operation. The transit frequency ω_T of a MOSFET is given as:

$$\omega_T = 2 * \pi * f_T = \frac{g_m}{C_{gs} + C_{gd}} \approx \frac{g_m}{C_{gs}} \tag{9}$$

Therefore the transconductance and the gate-to-source capacitance of the transistor are important in this topology for defining the frequency band of operation. Since the feedback resistance R_f contains no bias current, this topology does not therefore suffer from any trade off between the gain and supply voltages, which is in contrast to a resistively loaded common source stage. As the transistor M1 acts as a diode connected due to the feedback resistor, the transconductance of the M1 is therefore the chosen inverse of the source resistance and is given by:

$$g_{m1} = \frac{1}{R_S} \tag{10}$$

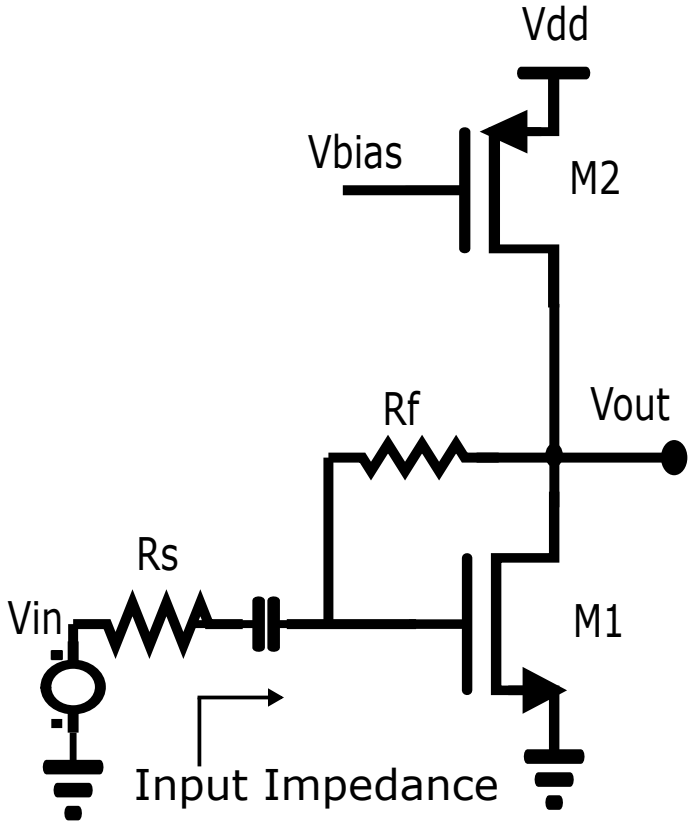


Figure 3: Resistive Feedback LNA

The voltage across the resistor R_f is given by:

$$V_{R_f} = g_{m1} V_{in} R_f \tag{11}$$

Therefore the output voltage is given by:

$$V_{out} = V_{in} - g_{m1} V_{in} R_f \tag{12}$$

$$\frac{V_{out}}{V_{in}} = 1 - g_{m1} R_f \tag{13}$$

$$= 1 - \frac{R_f}{R_S} \tag{14}$$

The voltage gain is given by:

$$A_v = \frac{1}{2}(1 - \frac{R_f}{R_S}) \approx -\frac{R_f}{R_S} \tag{15}$$

This is because the noise of the source impedance is multiplied by the gain of the LNA. This topology has a relatively high noise figure while referred to the input. The noise figure of this topology is given by:

$$NF \approx 1 + 4\frac{R_S}{Rf} + \gamma + \gamma g_{m2} R_S. \tag{16}$$

Even if we assume the term $4\frac{R_S}{Rf} + \gamma + \gamma g_{m2} R_S$ to be much less than 1, where γ is the "excess noise coefficient", still the noise figure will exceed 3dB [1]. Due to a high noise figure, the wide-band specification and high-power consumption of this topology, it is not suitable for the design and specification.

2.2 Common Gate LNA

Another topology which is widely used in LNA design is the so-called common gate topology. The basic common gate topology is shown in Figure 4. In comparison to narrow band applications, common gate topology is a more favorable choice for wide-band applications due to simple input matching. This is because the input impedance is dependent inversely on the transconductance (g_m) of the transistor when the body effect and channel length are neglected. The input impedance of a common gate LNA is set by the aspect ratio of the transistors and the current flowing through it. The input will be matched when $\frac{1}{g_m}$ becomes equal to the termination impedance Z_o for the desired frequency of operation. Typically, single-ended Z_o is 50Ω and, therefore, g_m of approximately 20 mS is required [3]. A single transistor can be used only because reverse isolation can be achieved as there is no Miller effect present in this topology. Therefore, input impedance matching and load can be designed separately [3]. If we ignore the channel length modulation, then the input impedance of Figure 4 is given by:

$$g_m = \frac{1}{R_S} = \frac{1}{50\Omega} \tag{17}$$

Another issue for the common gate LNA is the input matching, which is dependent on the input and output impedance, and is given as:

$$S_{11} = \mid \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \mid \tag{18}$$

For a good matching, the usual practice is to Select S_{11} to be less than -10dB. The equivalent circuit model of the common gate LNA is given in Figure 5. From the equivalent circuit, the gain of the LNA is obtained as [52]:

$$Y = \frac{i_o}{v_s} = \frac{g_m v_{gs}}{v_s} = g_m \frac{Z_i}{R_S + Z_i} \tag{19}$$

$$Y = \frac{g_m}{1 + R_S(g_m + j\omega C_{gs})} \tag{20}$$

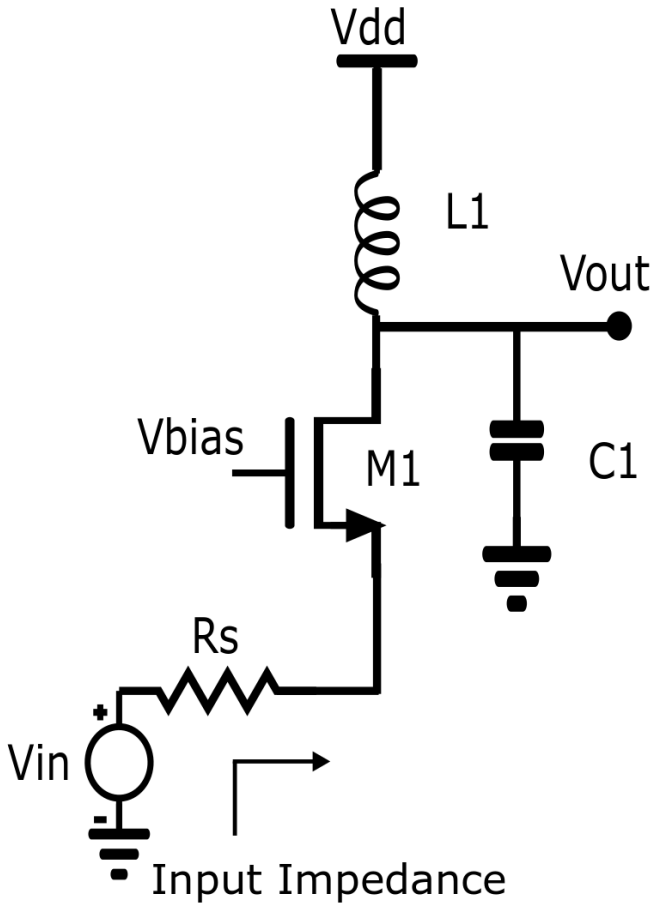


Figure 4: Common Gate LNA

$$Gain = |Y|^2 = \frac{i_o i_o*}{v_s v_s*} = \frac{g_m}{(1+g_m R_s)^2 + (\omega R_s C_{gs})^2} \tag{21}$$

Here we will only consider the channel noise of the transistor for the noise factor. The noise power added by the circuit is referred to as the output $N_A = 4kT\gamma g_{do}$, where g_{do} is the output admittance. Similarly, the noise at the input is given as: $N_i = 4kT\gamma R_s$, where R_s is the series resistance.

Now the noise factor of the circuit can be calculated as [52]:

$$F = 1 + \frac{N_A}{Gain\dot{N}_i} \tag{22}$$

$$F = 1 + \frac{4kT\gamma g_d o}{\frac{g_m}{(1+g_m R_s)^2+(\omega R_s C_{gs})^2} 4kTR_s} \tag{23}$$

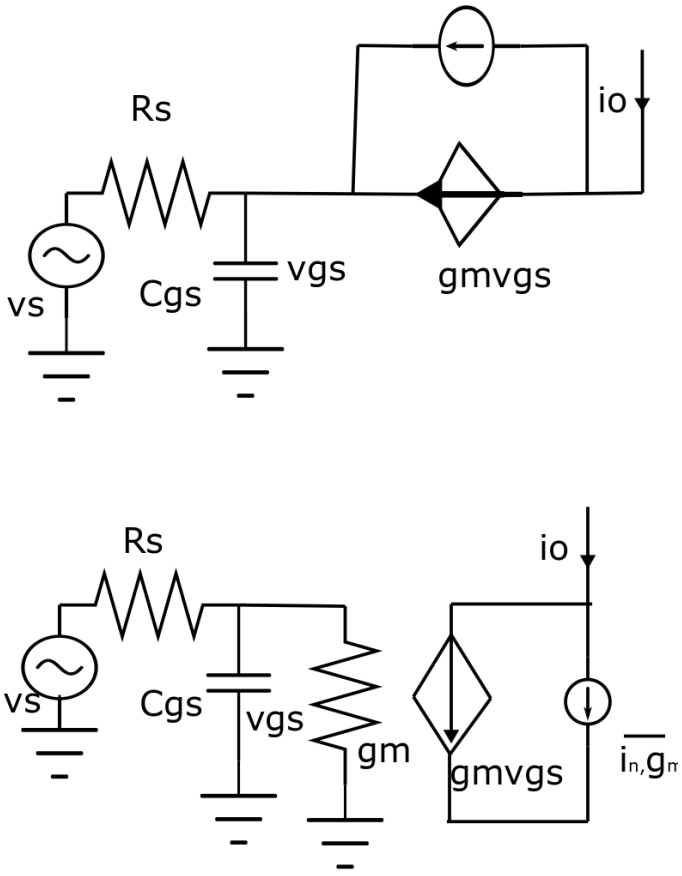


Figure 5: Equivalent Common Gate LNA

$$= 1 + \frac{\gamma}{g_m R_s}((1 + g_m R_s)^2 + \gamma g_m R_s(\frac{\omega}{\omega_T})^2) \tag{24}$$

When the input is matched, the transconductance of M1 is $g_m = \frac{1}{R_S}$, and Equation 24 will become:

$$F = 1 + 4\gamma + \gamma(\frac{\omega}{\omega_T})^2 \tag{25}$$

Considering the case when $\gamma(\frac{\omega}{\omega_T})^2 << 1 + \gamma$, the noise figure will still be greater than 3 dB due to the transconductance, which should be $\frac{1}{R_S}$ for the input matching.

2.3 Inductor Degeneration Common Source LNA

This topology is the favorable topology for narrow-band applications, and has been widely used. In a common source amplifier usually the input impedance is capacitive

due to the gate-to-source capacitance of the input transistor which needs to be matched with 50Ω impedance.

One way to match the input impedance is by using the resistive termination topology in a common source amplifier. However this will induce thermal noise due to resistive termination. However inductively degeneration topology can be employed to provide 50Ω input matching without adding resistive noise. Inductive degeneration common source (IDCS) topology is shown in Figure 6.

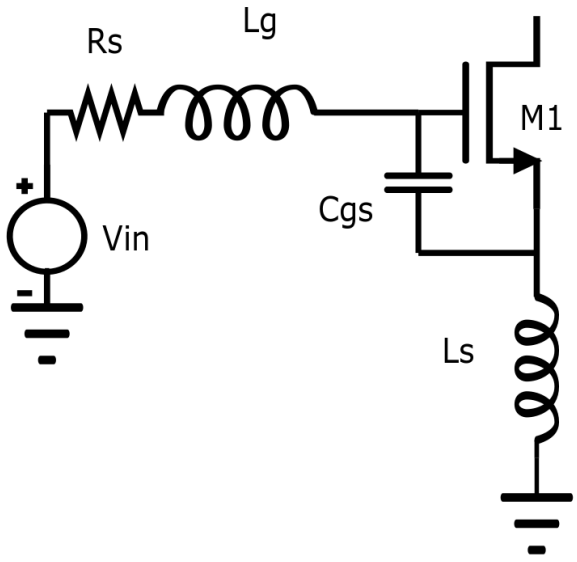


Figure 6: Inductively Degenerated LNA

From Figure 6 the small signal equivalent circuit is shown in Figure 7.
According to Kirchoff's Voltage Law the input voltage is given by:

$$V_{in} = I_{in}X_{Lg} + I_{in}X_{Cgs} + (I_{in} + g_m V_{gs})X_{LS} \tag{26}$$

From Equation 26 the input impedance impedance is calculated to be:

$$\frac{V_{in}}{I_{in}} = Z_{in} = X_{Lg} + X_{Cgs} + X_{LS} + g_m X_{LS} X_{Cgs} \tag{27}$$

$$Z_{in} = S(L_g + L_S) + \frac{1}{SC_{gs}} + \frac{g_m L_S}{C_{gs}} \tag{28}$$

where $X_{Lg}, X_{Cgs}, X_{LS}, I_{in}$ are the impedance of the gate inductor the impedance of the gate-to-source capacitor, the impedance of the source inductor and the input current respectively. For input matching at the desired frequency, the term $\frac{g_m L_S}{C_{gs}}$ must be equal to 50Ω and the imaginary term must be equal to zero. Therefore, to calculate the desired frequency equating the imaginary part of Equation 29 to zero:

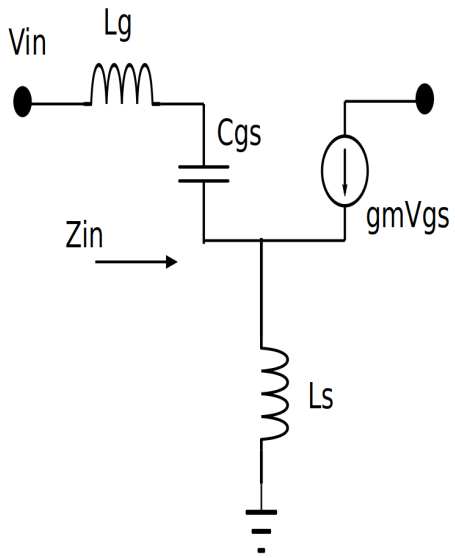


Figure 7: Equivalent Input Impedance of IDCS LNA

$$S(L_g + L_S) + \frac{1}{SC_{gs}} = 0 \tag{29}$$

$$j\omega(L_g + L_S) + \frac{1}{j\omega C_{gs}} = 0 \tag{30}$$

$$\omega = \frac{1}{\sqrt{C_{gs}(L_g + L_S)}} \tag{31}$$

The values of transconductance g_m, source inductor L_S, and the gate-to-source capacitance C_{gs} are varied to set the input impedance to 50Ω while the L_g, L_S and C_{gs} form a tank and are tuned to the frequency of operation, thus providing better matching without creating thermal noise.

From Equation 29 we can observe that the input of this topology behaves like an RLC circuit, therefore the quality factor can be given as:

$$Q_s = \frac{\omega L}{R} = \frac{1}{\omega RC} \tag{32}$$

$$Q_{in} = \frac{1}{\omega(R_s + \frac{g_m L_s}{C_{gs}})C_{gs}} \tag{33}$$

From Equation 33, $R_s = \frac{g_m L_S}{C_{gs}}$ when the input impedance is matched. In the absence of gate noise, as well as ignoring the Miller effect, V_{gs} in terms of input quality factor is given as [53].

$$V_{gs} = Q_{in} V_{in} \tag{34}$$

Transconductance is given as [53]:

$$g_m = \frac{I_{out}}{V_{gs}} \tag{35}$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{V_{gs} g_m}{V_{in}} = Q_{in} g_m \tag{36}$$

$$G_m = \frac{Q_{in}}{g_m} \tag{37}$$

The gain is given as:

$$Gain = -G_m R_L = -Q_{in} g_m R_L \tag{38}$$

Now calculating the noise figure considering that the input is matched, the real term in Equation 29 will therefore be equal to the input source impedance R_S. For the sake of simplicity, we consider only the transistor channel noise and source noise and ignore the pad capacitances and cascode transistor noise. Therefore the noise figure is given by [53]:

$$NF = 1 + \frac{\overline{V^2_{nM1,out}}}{\overline{V^2_{nRs,out}}} \tag{39}$$

Where $\overline{V^2_{nM1,out}}$ and $\overline{V^2_{nRs,out}}$ are the noise voltage of the transistor M1 and the input source respectively. The noise current of the transistor M1 is given by:

$$\overline{i^2_{nM1}} = 4kT\gamma g_m \Delta\omega \tag{40}$$

where $\Delta\omega$ is the bandwidth. And the output noise due to the input source resistance is given as:

$$\overline{V^2_{nRs,out}} = \overline{V^2_{nRs}} R_L^2 G_m^2 \tag{41}$$

where $\overline{V^2_{nRs}} = 4kTR_s\Delta\omega$. Now substituting all the values in Equation 39 we obtain:

$$NF = 1 + \frac{\overline{i^2_{nM1} R_L^2}}{\overline{V^2_{nRs}} R_L^2 Q_{in}^2 g_m^2} \tag{42}$$

Substituting the values of $\overline{i^2_{nM1}}, \overline{V^2_{nRs}} and Q_{in}$, we obtain a noise figure as:

$$NF = 1 + g_m R_s \gamma (\frac{\omega}{\omega_T})^2 \tag{43}$$

where ω is the frequency of operation and ω_T is the transient frequency of M1.An inductive load attached to the common source stage introduces a negative resistance

due to the feedback through C_{gd}. Therefore a cascode transistor is added in order to suppress this effect [1], as shown in Figure 8. Now the voltage gain will be equal to the product of the circuit's transconductance and the load resistance [1]. The gain can be increased by increasing the transconductance; supposing that the inductor losses are represented by resistance R1, then the voltage gain will be given as [1]:

$$\frac{V_{out}}{V_{in}} = \frac{\omega_T}{2\omega}\frac{R1}{R_S} \tag{44}$$

In case of ideal inductance the parallel losses R1 will become infinite. Therefore the gain will also become infinite. However if the losses are modeled by series resistance then the R1 will be 0 in case of ideal inductance and the gain equation will be derived accordingly for that case. A single-ended cascode IDCS LNA is shown in Figure 8.

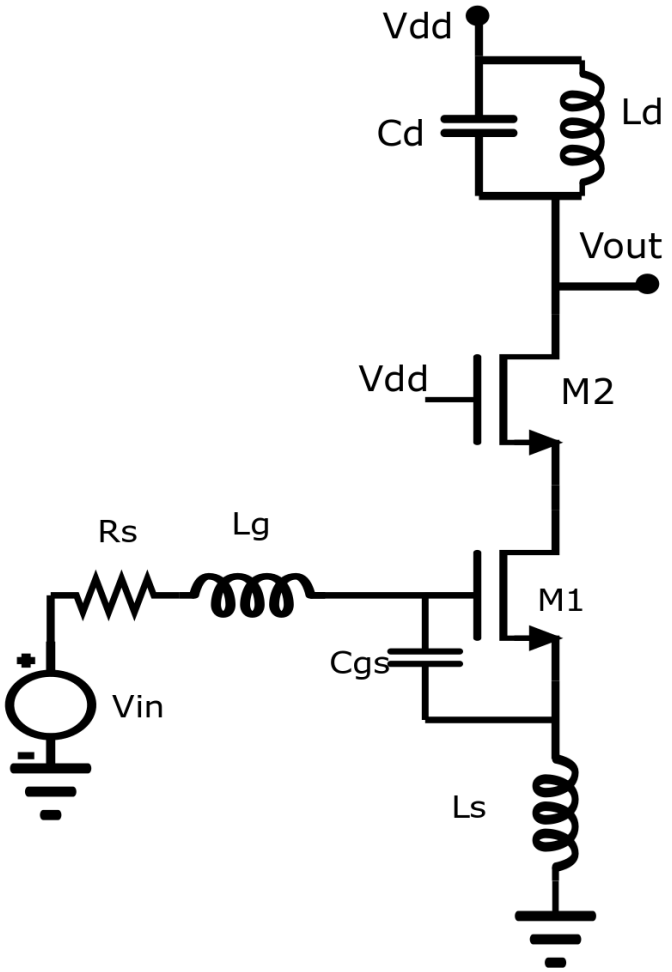


Figure 8: Cascode inductively Degenerated LNA

This topology can therefore be considered for the design of our circuit, the further design of which will be discussed in the following chapter.

3 Mixer

A mixer is a frequency translation device used in many radio frequency applications. A mixer basically consists of 3 ports: 1) a high-frequency port which is an RF port, 2) a local oscillator (LO) port and 3) an intermediate frequency (IF)/Baseband port. The translation of frequency generates two new signals which have frequencies equal to the sum and difference of the input frequencies. The simplest mixer can be a simple switch turning ON and OFF with the local oscillator frequency thus converting the RF signal to baseband for receiving, or simple multiplication of the RF signal with LO and vice-versa for transmission as shown in Figure 9:

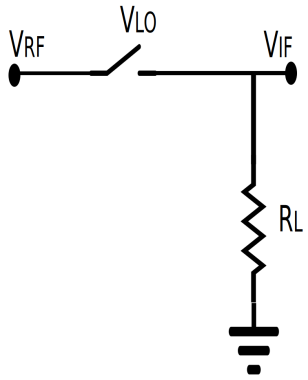


Figure 9: Basic Mixer with ideal switch

From Figure 9 it is clear that the switching in the mixer plays a critical role in frequency translation. Thus the switch should be fast enough so that it can perform frequency translation. Transistors are therefore the most convenient option to implement in the design of the mixer. The Gilbert's cell mixer is one popular topology among RF mixers, that are based on switches. Switching mixers are preferred in frequencies below than millimeter wave as switching mixers are slightly easier to design and produce less spurs [7]. While designing mixers, the following performance parameters must be considered: noise, linearity and gain, as well as port-to-port feed through. The multiplication of two frequencies can be simply given by the multiplication of two cosine signals, and is given by:

$$x(t)_{RF} = Acos(\omega_{RF}t) \tag{45}$$

$$x2(t)_{LO} = Bcos(\omega_{LO}t) \tag{46}$$

$$x(t)_{RF} * x2(t)_{LO} = \frac{AB}{2}[cos(\omega_{RF} - \omega_{LO})t + cos(\omega_{RF} + \omega_{LO})t] \tag{47}$$

As can be seen from the above equation, the mixer produces two output sum and difference frequencies. For the receiver, only the difference is selected while for the transmitter side only the sum is selected. In this section the major focus has been put on describing the topology of the Gilbert mixer, and its pros and cons are briefly overviewed.

3.0.1 Noise and Linearity

The noise of the mixer input produces a great influence on the performance of the system. While considering the receiver, as a mixer is a frequency translation device, therefore more noise means more corruption in the received signal, so the system design should be done in such a manner that the noise of the mixer is minimized and is not be able to affect the overall performance of the receiver. This could be acheived by increasing the gain of the LNA so that the noise of the mixer is divided by the gain of the LNA and should be minimized, as seen in Equation 8. Therefore the design is done in such a manner that the linearity of the mixer should be maximized while keeping the noise figure as low as possible. The noise figure of a noise-less mixer is 3dB [1]; if the desired signal after down conversion resides on only one side of the LO frequency then the noise figure is known as a "Single Sideband Noise Figure". If, on the other hand, the input signal resides on both sides of the LO frequency, then the noise figure will be a "Double Sideband Noise Figure". In an up-conversion mixer, the noise figure is not as critical in the transmitter as in receiver, however, the linearity is specified by the type of modulation.

3.0.2 Gain

The gain of the mixer is another parameter which needs to be considered during the design process. The gain of the mixer is basically the voltage conversion gain. The voltage conversion gain of a down-conversion mixer is the ratio of the rms voltage of the IF signal to the rms voltage of the RF signal [1].

3.0.3 Port-to-Port Feedthrough

The architecture of the front end defines the feedthrough effect of the ports on system performance. With regard to the direct conversion receiver, the LO-IF feed through in down conversion is benign because the IF filter suppresses it [1].However LO-RF feedthrough is undesirable because of the offsets in baseband and LO radiation from the antenna, but this depends upon several factors such as circuit design and matching etc.

3.1 Single and Double Balanced Mixers

A mixer is known as "single balanced mixer" when only the LO port of the mixer is balanced. This configuration provides twice the gain of the simple mixer as depicted in Figure 9. The single-balanced (SB) configuration provides differential outputs at the IF/Baseband port therefore making it easy for subsequent processing despite having a single-ended RF input at the receiving side. In the case of a double-balanced mixer, both LO and RF inputs are balanced. A single-ended RF input can also be applied here while grounding the other input, but it will increase the input referred noise. Single-balanced mixers provide better performance compared to single-switch mixers because of the balanced LO port.

In an SB mixer, LO-RF feedthrough disappears at ω_{LO} if the design is symmetric. However the LO-IF feedthrough is still a problem in single-balanced mixers. To solve this problem, double-balanced topology was designed, in which two single-balanced mixers are connected in such a manner that the LO output feedthrough signals cancel each other.

In a double-balanced mixer, the LO signal should be a perfectly square wave in order to avoid overlap time as well as to ensure abrupt switching; otherwise a gradual change in LO wave form will lead to a short instant of time at which all transistors are ON. This means that all transistors will treat the RF signal as common mode for that instant of time resulting in a waste of the input signal. At high frequency, however, the LO wave is not a perfect square. It resembles a sine wave. Therefore in order to minimize overlap time, the amplitude of the LO is chosen relatively large to ensure minimum overlap time. The principle schematics of a single-balanced mixer and a double-balanced mixer are depicted in Figures 10 and 11.

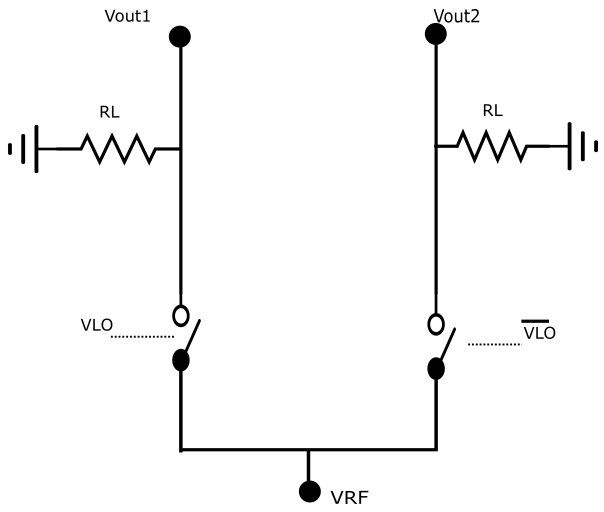


Figure 10: Single-Balanced passive Mixer [1]

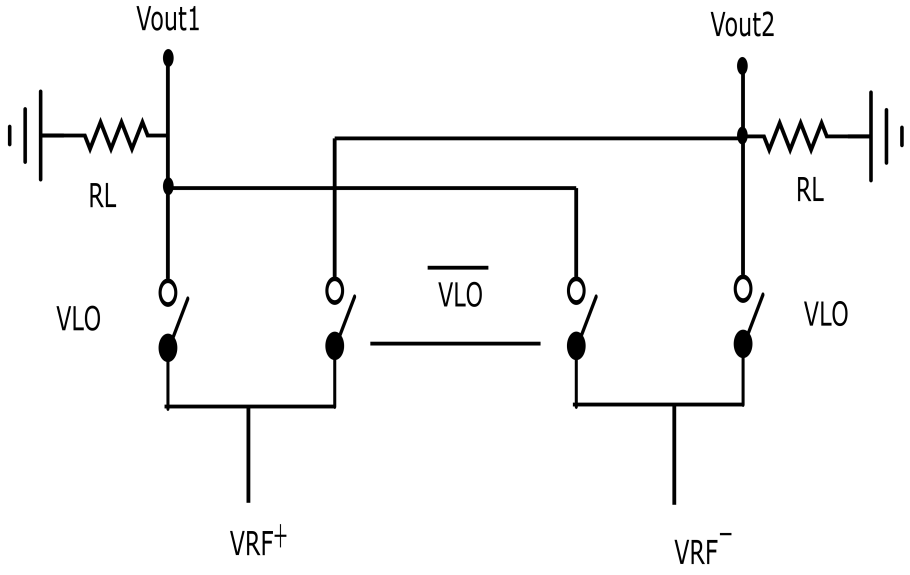


Figure 11: Double-Balanced Passive Mixer [1]

3.2 Passive Mixers

The main difference between active and passive mixers is that the passive mixers do not consume power, thus they provide loss while active mixers consume power to provide gain. Therefore to cover up the noise of passive mixers the gain of the previous stages must be high. Yet when considering linearity, passive mixers have better performance compared to active mixers. In practice, for proper switching, passive mixers require a full rail LO signal [11]. A double-balanced passive mixer is depicted in Figure 12. Passive mixers are biased near the threshold region. Parasitic capacitances at the output of the transconductance stage are charged and discharged at the rate of the LO [13].

In this topology the NMOS transistors behave as switches. At any time instant, two of the switches are turned ON while the other two remain OFF. Theoretically the conversion gain of an ideal double-balanced passive mixer is given by [12]:

$$20log\frac{2}{\pi} = -3.9dB \tag{48}$$

The above value can be achieved when ideal switches are employed. However, in practice, this value is even lower.

An important advantage of passive mixers is that they carry no DC currents theoretically, thus no current means no flicker noise in ideal cases. In practice, they also contain some flicker noise as discussed in [18], but it is still remarkably lower than in active mixers. This makes passive mixers a favorable choice for direct conversion receivers.

The noise of mixers can be further minimized by increasing transistor width.

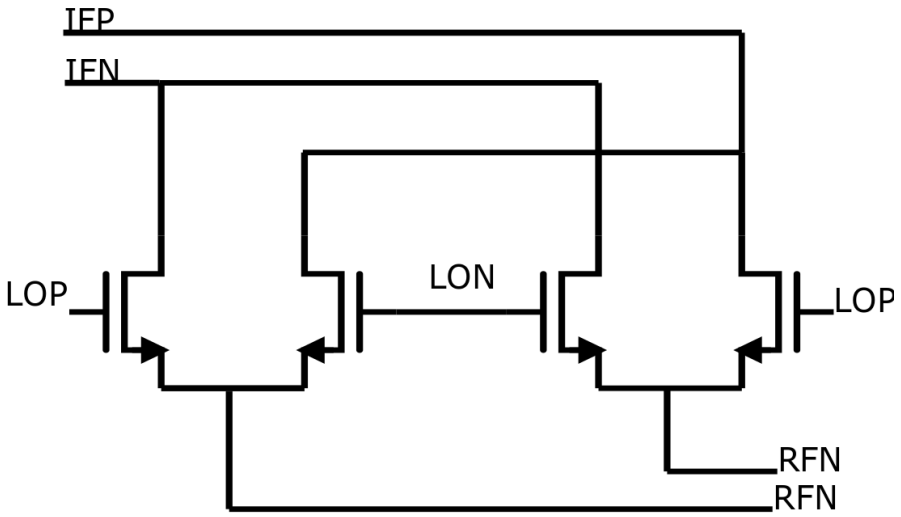


Figure 12: Double-Balanced Passive Down-Conversion Mixer

However increasing device size will increase gate capacitance that will require high LO power, thus the choice of transistor dimensions needs to be optimized while designing the passive mixer The input referred noise of a passive mixer is determined by first finding the output noise power density of the mixer and then dividing the result by the square of the conversion gain. For the double-balanced topology the input referred noise is given by [1]:

$$\overline{V_{n,in}^2} = 2\pi^2 kTR_{on} \tag{49}$$

From Equation 49, it is clear that noise directly depends upon the on-resistance of the device. So decreasing the on-resistance will decrease the noise.

3.3 Active Mixers

Active mixers consume power in contrast to passive mixers, giving them their own advantages and disadvantages. Active mixers have the advantage of conversion gain and a low LO power requirement at the cost of low linearity and a high noise figure in comparison with passive mixers [14]. While considering active mixers, the Gilbert cell topology is prominent in a direct conversion receiver because of its high gain, low LO-RF feedthrough and high isolation performance [16]. The Gilbert Mixer was first proposed by Barrie Gilbert in the mid 1960s [24].

A double-balanced Gilbert mixer in CMOS is depicted in Figure 13. An active mixer can also be of single-balanced topology as shown in Figure 14.

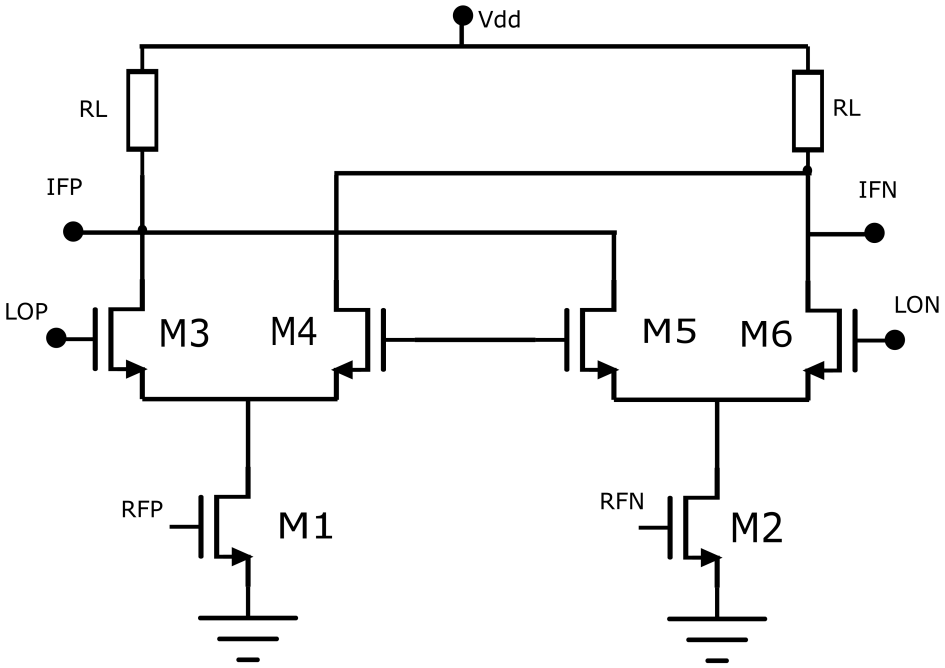


Figure 13: Double Balanced Active Down-Conversion Mixer

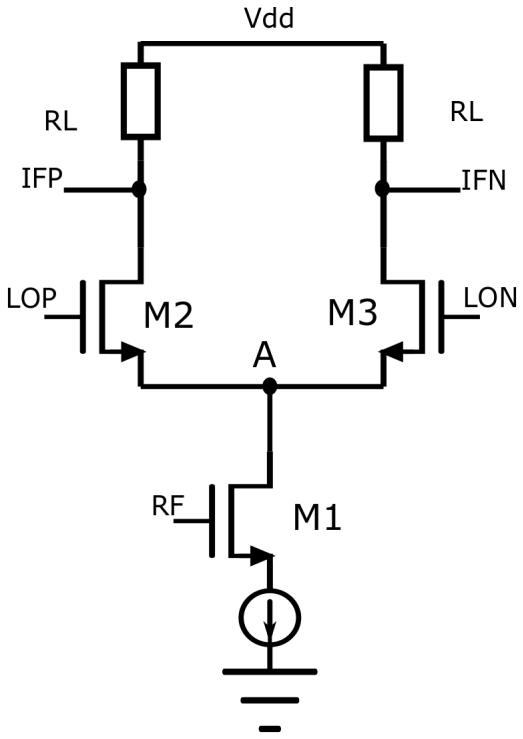


Figure 14: Single Balanced Active Down-Conversion Mixer

An active mixer first performs switching by voltage to current conversion, and then again by converting the current to voltage after frequency translation, thus acheiving the converison gain. In the single-balanced topology shown in Figure 14, M1 converts the RF signal to a current, then the transistors (M2,M3) forming a switching pair, steer the current to the load RL, and then this current is converted to voltage. The voltage conversion gain is given by [1]:

$$\frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} g_m R_L \tag{50}$$

The transconductance of input transistor M1 is dependent upon the current flowing through the transistor and is given by [1]:

$$g_m = \frac{2I_D}{(V_{GS1} - V_{TH1})} \tag{51}$$

Also the load resistance value R_L is limited by the voltage head room. The linearity requirement suggests that the swiches which run with the LO should operate in an active region. Low supply voltage thus degrades the gain of active mixers. Another factor which is responsible for decreasing mixer gain is the capacitance seen at node A in Figure 14. When considering one half of the LO cycle during which M2 is ON and M3 is OFF, this capacitance is expressed as:

$$C_P = C_{DB1} + C_{gs2} + C_{gs3} + C_{SB2} + C_{SB3} \tag{52}$$

This capacitance causes the RF current to split at node A between C_P and $\frac{1}{g_{m2}}$ causing a decrease in gain by a factor of $\frac{g_{m2}}{sC_p+g_{m2}}$[1]. For the double-balanced topology, the conversion gain is half the value of the single-balanced mixer.

Non abrupt switching of LO port transistors (M2, M3 Figure 14), increases noise in the active mixers. The noise components of interest in the mixer shift to the IF range after down-conversion. The input referred noise in double-balanced mixers is half the value of the noise in single-balanced mixers. With a symmetrical structure the flicker noise of the RF port does not appear at the output, however, the flicker noise of the LO port still appears. The flicker noise for the active down-conversion mixer is given by [1]:

$$V_{n,out}(f)|_{k=0} = \frac{I_{SS}R_D}{\pi V_{p,LO}} V_{n,2}(f) \tag{53}$$

Where $V_{n,out}(f)$, I_{SS}, R_D, $V_{p,LO}$, $V_{n,2}$ are the output noise, current passing through switching transistors, load resistance, peak voltage of the LO and the noise of M2 seen in Figure 14 respectively. The above equation shows that the flicker noise is scaled by a factor of $\frac{I_{SS}R_D}{\pi V_{p,LO}}$. Thus the flicker noise is directly dependent upon the bias current of the active mixers [1].

In active mixers, the overdrive voltage of the RF input transistor primarily determines the linearity. IP3 increases directly with the overdrive voltage of the transistor. This can be seen from the following equations [1]:

$$IP_3 \alpha V_{GS} - V_{TH} \tag{54}$$

$$\overline{V_{n,in}^2} = \frac{4kT\gamma}{g_m} = \frac{4kT\gamma}{2I_D}(V_{GS} - V_{TH}) \tag{55}$$

Similarly, noise is also dependent on the overdrive voltage which can also be seen from Equation (55). The linearity of Gilbert cell mixers can be increased. Several methods have been presented, for instance, gain control in [15], current bleeding in [19], folded switching in [20, 21], and different techniques for biasing LO and RF switches, as in [22, 23]. But these methods employ the use of on-chip inductors resulting in a large die area and high power consumption, which are undesirable in accordance with the low-power design principle.

4 Power Amplifier

One of the power hungry building blocks of an RF transmitter is the power amplifier (PA). Power amplifier design is therefore a critical task. There are certain figures of merit which must be considered when a power amplifier is designed. These are:

- Power Added Efficiency
- Drain Efficiency
- Maximum Output Power
- Linearity

An important parameter in the power amplifier is the efficiency, which affects directly the talktime of handheld devices. The efficiency of the power amplifier is defined in terms of power added efficiency and drain efficiency. Power added efficiency is the ratio of the difference of input power with the output power to the total dc power consumption, and is given by [25]:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{56}$$

where P_{OUT}, P_{IN} and P_{DC} are the output signal power, input power and dc power respectively at the desired frequency. While drain efficiency is the ratio of the output signal power at the desired frequency to the DC power consumption and is given by:

$$DE = \frac{P_{OUT}}{P_{DC}} \tag{57}$$

PAE is used to determine the efficieny of the PA between the linear and saturated regions, making it possible to find the optimal point where the amplifier can maximize the transference of input power to output power [26].

The output power for the power amplifier is defined as the active power delivered to the load at the desired frequency [28]. The antenna provides a 50 ohm resistance. Therefore the output impedance of the power amplifier should be properly matched with this 50Ω impedance to minimize scattering and loss of power. The average output power of a PA at the desired frequency is given as:

$$P_{avgout} = \frac{V_{out}^2}{2R_L} \tag{58}$$

where V_{out} is the amplitude of the output voltage, R_L is the load resistance and P_{avgout} is the output power.

There are several ways to classify power amplifiers; however when considering linearity, power amplifiers can be classified into two groups [27]:

- Linear power amplifier
- Non-linear power amplifiers or switching power amplifiers

In a linear power amplifier there is a linear relationship between the input and output signals. Linearity is important, especially for such modulation schemes in which the envelopes are not constant. Therefore, the PA should be linear enough so that the information should not be lost [25]. Linear amplifiers include class A, class B, class AB and class C. The general architecture of these classes is the same, however they differ in biasing. The general architecture of a single-stage PA is shown in Figure 15.

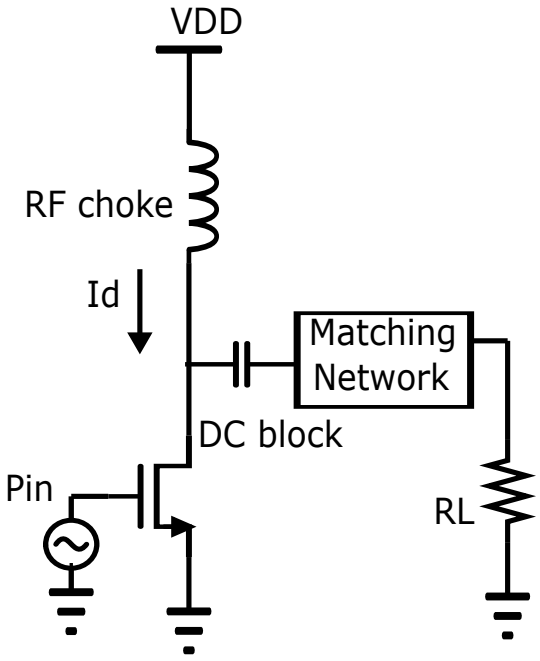


Figure 15: General Single-Stage Power Amplifier Model [28]

Study of non-linear amplifiers reveals that they provide more efficiency than linear amplifiers [1]. Non-linear amplifers are further classified into class C,class D, class E and class F.

4.1 Class A Amplifiers

Class A amplifiers are the most linear amplifiers compared to all the other amplifier classes. In class A the amplifier transistors remain ON for a full operation cycle and the operation is linear. The biasing point is chosen higher so that the device does not turn OFF at any instant of the signal cycle. When the device operating point does not change significantly then the device is said to be linear [28].

The CMOS transistor must operate in the active region, and thus its drain current is given by the square law:

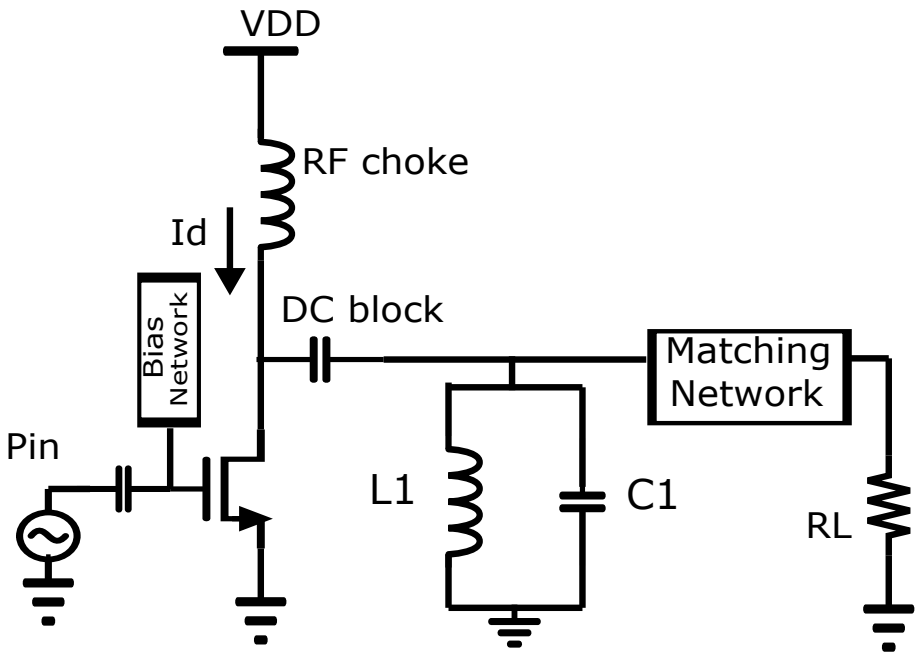


Figure 16: Class A power Amplifier [26]

$$I_D = \frac{1}{2}K_n(\frac{W}{L})(V_{GS} - V_{TH})^2 \tag{59}$$

For the narrow-band class A amplifiers, the parallel resonant in Figure 16 is used to suppress the undesired harmonics. The linearity of class A amplifiers is very good in comparison to other classes. However, when considering efficiency this is not the case. The theoretical maximum efficiency of class A amplifiers is 50 %. Considering a sinusuoidal input waveform, the output power can be given as:

$$P_{out} = \frac{V_{out}^2}{2R_L} \tag{60}$$

Therefore, the drain efficiency is given by:

$$\eta_d = \frac{P_{out}}{P_{DC}} \tag{61}$$

When the maximum power is delivered to the output, the maximum drain efficiency will occur at the same time because the load is constant. When the input transistor is completely turned OFF then the maximum output voltage will occur, because the supply current will flow completely into the load, and assuming that the load is completely matched without any loss. Hence the inductor will behave like an RFC(RF Choke) at the desired frequency, and, therefore, the maximum output voltage will be V_{DD}. The maximum drain efficiency can be calculated as [26]:

$$\eta_d(max) = \frac{\frac{V_{omax}^2}{2R_L}}{V_{DD}I_{DC}} \times 100\% \tag{62}$$

$$= \frac{1}{2}\frac{V_{omax}^2}{V_{DD}^2} \times 100\% \tag{63}$$

$$\eta_d(max) = 50\% \tag{64}$$

4.2 Class B Amplifers

Class B amplifiers provide higher efficiency than class A amplifiers, however, the linearity is lower. The efficiency of class B amplifiers can be increased by changing the bias point of the input transistor, which in turn decreases the conduction angle of the power amplifier. Since the transitor does not remain ON for the whole signal period, the input transistor should be biased near the threshold voltage, so that it can switch to active and cut-off regions instantly thus conducting for half of the signal period. Typically, the circuit topology for a class B amplifier is the same as for class A amplifiers. The difference between these two classes is the biasing point of the input transistors. The maximum efficiency of class B amplifiers can be given as [29]:

$$\eta_d = \frac{P_O}{P_{DC}} \tag{65}$$

The output power will be the same in both class A and B amplifiers, but the DC power will be given as [29]:

$$P_{DC} = \frac{V_{DD}^2}{\frac{\pi}{2}R_L} \tag{66}$$

Hence the maximum effciency can be given as:

$$\eta_{dmax} = \frac{\frac{V_{OMAX}^2}{2R_L}}{\frac{V_{OMAX}V_{DD}}{\frac{\pi}{2}}} \times 100 \tag{67}$$

$$\tag{68}$$

At the maximum output voltage $V_{OMAX} = V_{DD}$, the maximum drain effciency of a class B amplifier will be [29]:

$$\eta_{dmax} = \frac{\pi}{4}\frac{V_{DD}}{V_{DD}} \times 100 \tag{69}$$

$$\eta_{dmax} = \frac{\pi}{4} \times 100 \approx 78.5\% \tag{70}$$

The drawback of this toplogy is that the turn-off period of the input transitor results in undesired harmonics at the output, therefore a high quality resonant circuit is required in order to suppress these harmonics [26]. The inductance and capacitance values can be calculated as [26]:

$$L_o = \frac{R}{Q_L \omega_o} \tag{71}$$

$$C_o = \frac{Q_L}{R\dot{\omega}_o} \tag{72}$$

where L_o, C_o are the inductance and capacitance values of the tank circuit, Q_L is the quality of the resonant circuit at the desired frequency, and R is the optimized value for the desired output power before matching [26].

4.3 Class AB Amplifiers

In Class AB amplifiers the input transistors are biased in between class A and B amplifiers, having a conduction angle between 180 to 360 degrees, thus providing an efficiency ranging from 50% to 78.5%, allowing designers to make a trade off between efficiency and linearity.

4.4 Class C Amplifiers

In this class the input transitor is biased in such a way that it mostly operates in the cut-off region having a conduction angle below 180 degrees. These amplifiers are able to provide a theoretical efficiency range between 78.5% to 100% while degrading linearity.

4.5 Class D Amplifiers

The class D RF amplifier concept was first described by Baxandall in 1960 [29], and since then named as one of the amplifiers that theoretically offer the highest efficiency of 100%. The reason for the high efficiency of a class D amplifier is due to the fact that the active devices are operated as switches in a push-pull fashion. The output of class D amplifiers is a digital pulse. This however means that this amplifier can be implemented for only constant envelope input, and this is the main limitation of class D amplifiers. Class D amplifiers are implemented using switched-mode techniques, and have gained a lot of attention, especially for high-frequency operations. A class D amplifier is shown in Figures 17 and 18.

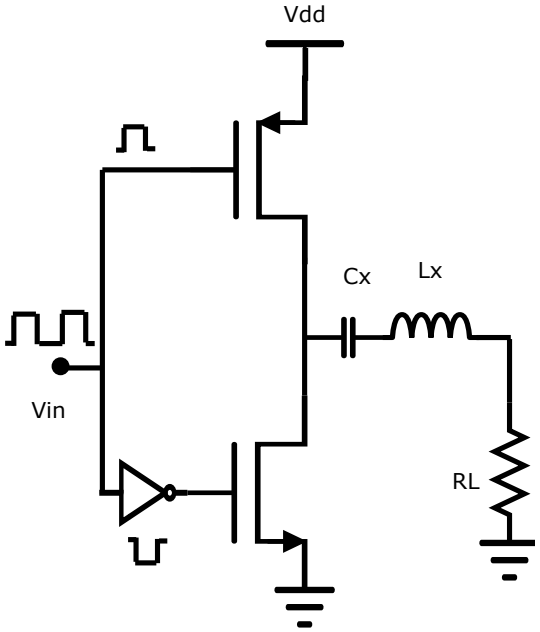


Figure 17: Class D voltage-mode power amplifier [26]

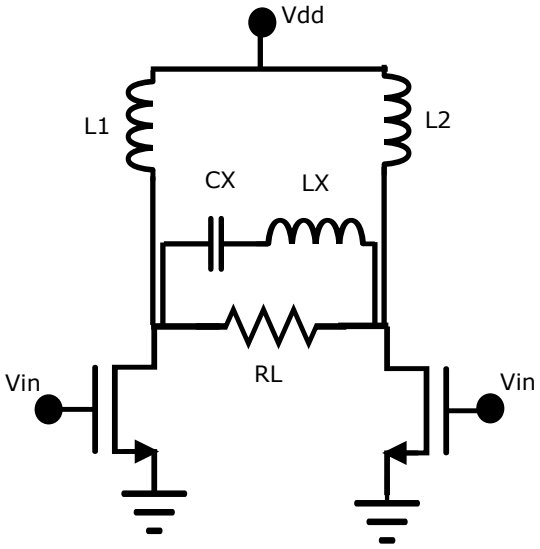


Figure 18: Class D current-mode power amplifier [26]

A class D amplifier can be operated in one of two possible modes:

- Voltage Mode
- Current Mode

Voltage switching class D amplifiers usually consist of a series resonant circuit as shown in Figure 17. If the quality of the resonant circuit is high, then the voltage across the switching pair will be a square wave while the current from the switching

devices will be a half sinosuidal wave. The resonant circuit will provide the full sinosuidal current.

In current-mode class D amplifiers the opposite occurs. These amplifiers consist of a parallel resonant circuit as shown in Figure 18. The current through the switching pairs is a square wave and the voltage across the switches is a half sinusoidal wave, while the voltage across the resonant circuit is full depending upon the high quality factor of the tank circuit.

The impedance of the resonant circuit is capacitive below the frequency of operation while highly inductive above the frequency of operation. Voltage-mode operation cannot be used at high frequency because of the losses due to transistor parasitics. However, the current-mode class D amplifier can be used at high frequency. A current mode class D amplifier incorporates a zero-voltage switching technique as discussed in [32, 34]. Further explanation of zero-voltage switching will be given in the next section of this chapter.

4.6 Class E Amplifiers

Another class of non-linear amplifiers are class E amplifiers. The way this class differs from the previous class D amplifier is that this class contain only a single transistor. The Class E amplifier was proposed by Sokal in 1975 [35]. Class E amplifiers comprise a switching transistor and a passive load network, having a maximum theoretical efficiency of 100%. Class E amplifiers also operate in one of two modes.

- Zero-Voltage Switching(ZVS)
- Zero-Current Switching (ZCS)

The basic circuit of a class E amplifier is shown in Figure 19.

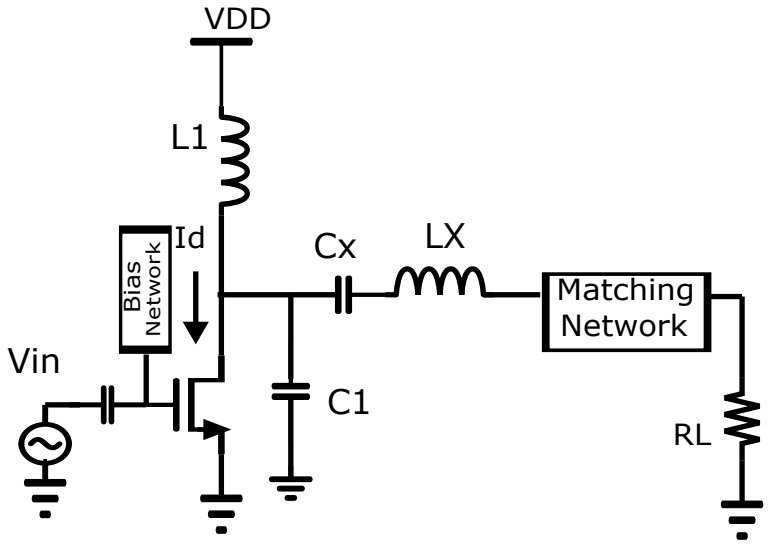


Figure 19: Class E power amplifier model

Where L1 acts as the DC feed inductor or as an RF choke. Capacitance C1 is used when the topology operates in zero-voltage switching mode. In zero-current switching, the absence of C1 causes the abrupt switching, which results in a sudden voltage drop in the transistor giving lower efficiency [26]. Zero-voltage switching is therefore more preferable in cases where the switching occurs due to a gradual voltage change. C1 decreases power dissipation in the transistor when operating in zero-voltage switching mode [37]. Cx and Lx forms the tuning circuit in Figure 19. The quality of this tuning circuit defines the performance of the power amplifier [26].

4.7 Class F Amplifiers

Non-linear amplifiers also include class F amplifiers which differ from class E amplifiers in such a way that they have no need for a fast switching driver signal. Due to the usage of large switches in class E amplifiers, class E amplifiers produce hindrance with scaling down technology [37]. For this reason, this class has gained much popularity in low-power designs. Class F amplifiers employ harmonic control techniques, in which even and odd harmonics see either an open or short circuit respectively or vice versa, so that only the fundamental harmonic will appear in the load, and undesired harmonics can be terminated [26]. The square wave will appear at the output if the odd harmonics see an open circuit caused by the filter blocks. A parallel resonant circuit tuned at the desired frequency, and an n number of series LC tank circuits tuned to an n number of odd harmonics, defines the load network. The output current will appear as a square wave when the open circuit is chosen for even harmonics. The principal circuit diagram of a class F amplifier is shown in Figure 20.

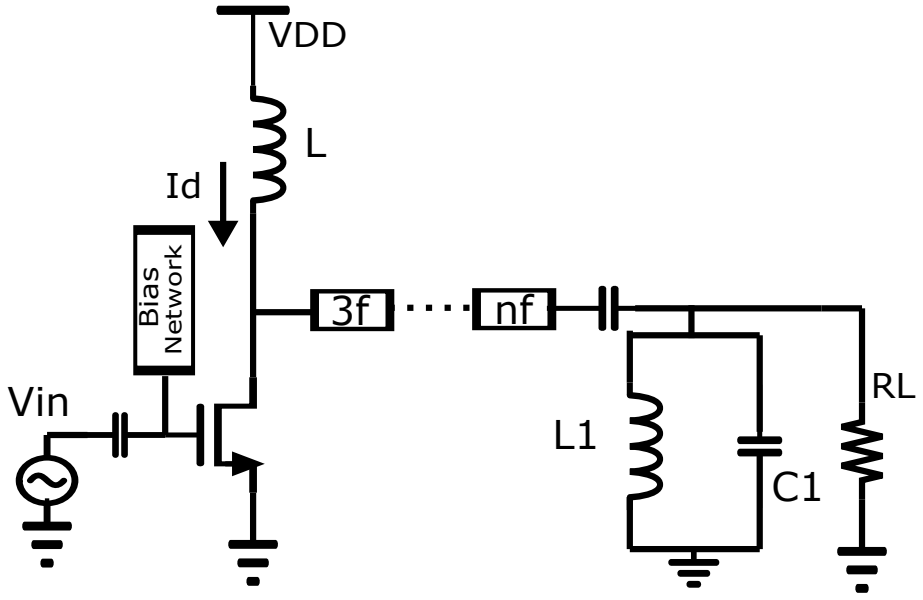


Figure 20: Class F power amplifier model [26]

5 Description of Design

This section explains the steps and procedure to design all the blocks for the receiver and transmitter of the RF front end. As discussed before, the blocks are designed to be implemented for BLE applications for which the frequency of operation is 2.4 GHz. The receiver bandwidth should be 80 MHz from 2.4 GHz to 2.48 GHz. All of the designed blocks were implemented in a 65nm technology using Cadence Virtuoso software. The Spectre simulator was used for the circuit simulations.

5.1 LNA Design

As discussed in chapter 2, IDCS LNA topology is considered as a better choice for a narrow band LNA. Therefore this topology was selected in the design.

The first step in designing the LNA is to match the input impedance of the LNA with the source. Therefore tradional methods of matching the input of an IDCS LNA are employed here. As discussed previously, the input impedance of the IDCS LNA is dominated by capacitive reactance, determined by the gate-to-source capacitance of the input transistors. Due to this, matching with the 50Ω resistive impedance is a difficult task without adding any resistive noise. To overcome this problem, both gate and source inductances are used to provide real input matching of 50 ohms without adding extra noise.

To obtain an estimate of the gate capacitance as well as the threshold voltage of the transistors, the Cadence manual was consulted.

For the matching of the input stage of the LNA, Equation 28 was used, in order to get the first order estimation. Hence, the third term in Equation 28 is the real input impedance as given below:

$$Z_{in,RE} = \frac{g_m L_s}{C_g s} \tag{73}$$

This expression was used to match the input with the real 50 ohms while Equation 31 was used to match at the desired frequency of 2.4 GHz. Thus, the values of g_m, L_S and C_{GS} were tuned to obtain the impedance of 50 ohms; for a low-power design, the LNA is biased in the subthreshold region [38]. After that, the values of the source degeneration inductor (L_S), the gate-to-source capacitance C_{GS} of the input transistor and the gate series inductance (L_G) were selected in order to match the input. According to the discussion in section 2.3, (L_S) contributes significantly the input impedance, while $L_S + L_G$ resonates with C_{GS}. As discussed earlier, for the proper input matching the maximum transit frequency of NMOS transistor f_T is decreased using the following dependency:

$$\frac{g_m}{C_{GS}} \approx \omega_T = 2\pi f_T \tag{74}$$

The 65nm technology used for the design of this project has the $f_T \approx 160$ GHz. Therefore the matching can be done by adding an external gate-to-source capacitance

C_{GS} to the input transistor [1]. In practice, the bonding wire often acts as a source degeneration inductor but its typical value is relatively large, around 1-2 nH and it increases the input resistance $\approx L_s\omega_T$ if f_T is not decreased. Therefore a C_{GS} value of around 56 fF is added from the gate-to-source of the input transistor to decrease the f_T. The gate inductance L_g value also needs to be calculated for the operation frequency 2.4 GHz, according to Equation 31:

$$\omega^2 = \frac{1}{C_{gs}(L_S + L_g)} \tag{75}$$

L_g is realized as off-chip, therefore the effect of pad capacitance and bonding wire inductance were also considered in the design. After including pad capacitance and the bonding wire, the input of the LNA appears as in Figure 21.

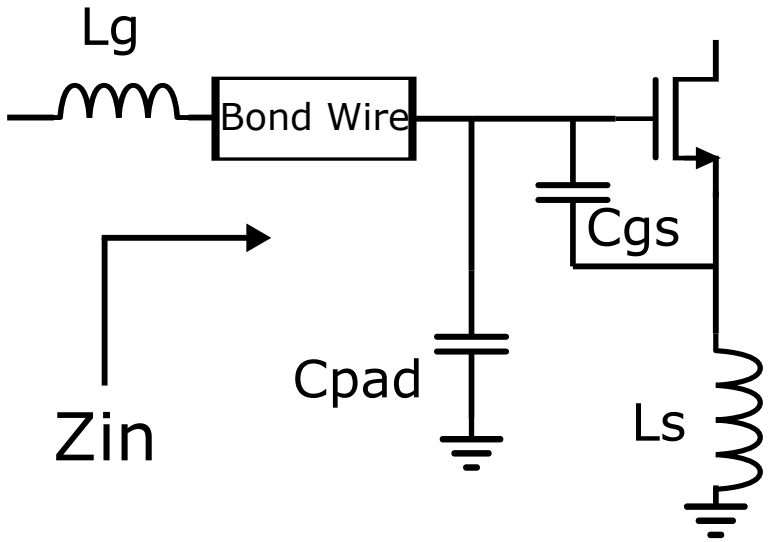


Figure 21: Input Impedance IDCS LNA

According to the Cadence 65nm technology manual, the typical value of pad capacitance is 400 fF. Therefore in the simulations, 400 fF capacitor is added to the input of the LNA. The bonding wire also causes inductance.

As a rule of thumb a bonding wire with a diameter of 25 μm has an inductance of 1 nH / mm per unit length. A more accurate estimation is given by [39]:

$$L_{BondWire} = 5.08 \times 10^{(} - 3) \times Length \times (ln(4 \times Length/Diameter) - 1) \tag{76}$$

The bonding wire contains capacitance and resistance as well, therefore the bonding wire is modeled as shown in Figure 22.

The simulation is performed using all the real components in the design. The parasitics of the real components increase the noise figure of the design. A differential topology for the LNA is implemented in the design because of common-mode rejection and immunity to supply noise. For a low-power design, the LNA is biased in the subthreshold region, i.e the V_{GS} remains slightly less than V_T. Hence, for the input

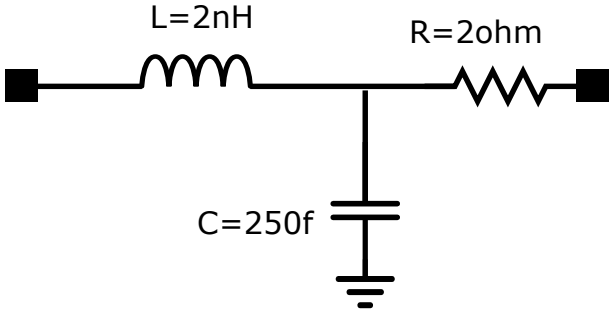


Figure 22: Model of Bonding wire

transistor the relationship between the drain current I_D and V_{GS} in this region is given by [41, 42]:

$$I_D = \frac{W}{L} I_{Do} e^{q\frac{V_{GS}}{nKT}} \tag{77}$$

From which the transconductance is calculated to be [42]:

$$g_m \approx \frac{I_D}{V_{GS}} \tag{78}$$

Using these equations the device size was estimated and then further optimized for best performance. The reason for using IDCS LNA is that the common source LNA produces a negative resistance from output to input due to the feedback capacitance from the drain to the gate of the input transistor. Therefore a cascode device is added in order to avoid this effect. The dimensions of this cascode device were made equal to the input transistor. The load of the cascode LNA contains an LC tank circuit which oscillates at the desired frequency of operation. From Equation 38, the gain of the IDCS depends upon the load resistance as well as the transconductance and quality factor. Therefore the gain of the LNA is achieved by optimizing the values of both load resistance and transconductance.

All of the components in the design are real components. Therefore the inductor model in the design contains parasitics. The inductor implemented is modeled as shown in Figure 23.

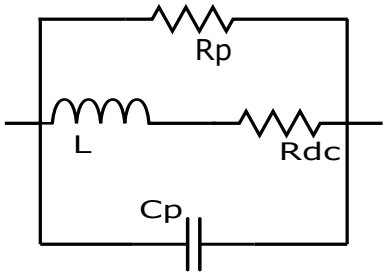


Figure 23: Inductor modeling

where R_P, R_{DC}, C_P and L are the parallel resistance, DC series resistance, parallel

capacitance, and inductance respectively. Instead of using saperate single inductors at each branch of the differential LNA, a differential inductor is used in the design in order to minimize the size of the chip area. The gate inductance was realized as off-chip, and for the simulations the S-parameter file of the inductor supplied by the CoilCraft company was used. The simulated differential inductor degeneration common-source LNA is depicted in Figure 24.

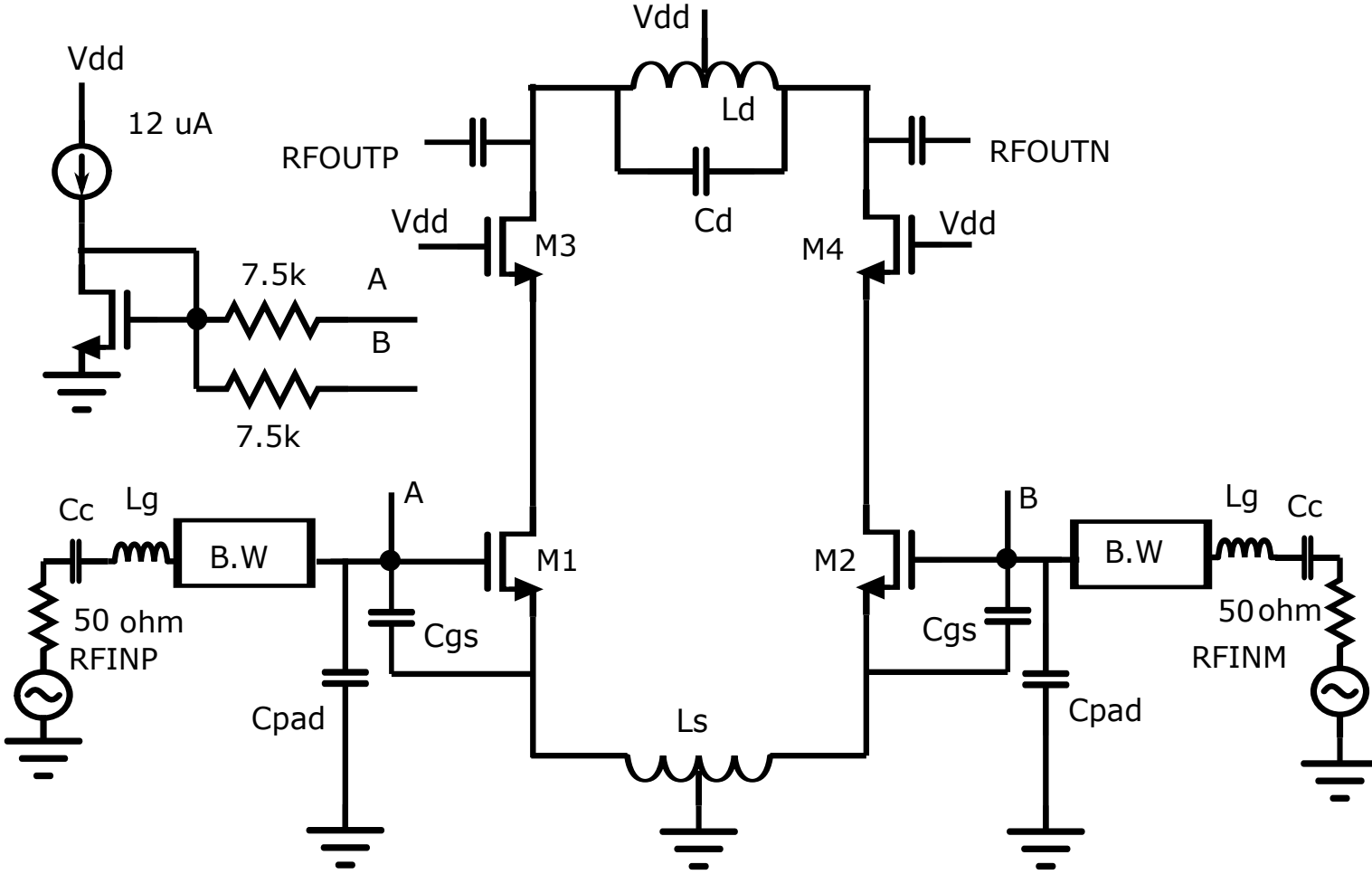


Figure 24: Inductor degeneration LNA implemented design

The final values for the devices are shown in Table 1 as follows.

Table 1: Components values

Component Names	Component Values
$M1 - M4$	$\frac{5.1\mu}{0.07\mu}$
C_{gs}	56 fF
L_S	2 nH
L_D	11.2 nH
L_G	4.7 nH
C_D	260 fF
C_c	10 pF
C_{pad}	400 fF
Biasing Transistor	$\frac{1.1\mu}{0.07\mu}$

After post layout simulation of the designed low noise amplifier, the following peformance parameter results were obtained.

The input scattering S_{11} of the LNA for the whole bandwidth from 2.4 GHz to 2.48 GHz was found to be below -10 dB as shown in Figure 25:

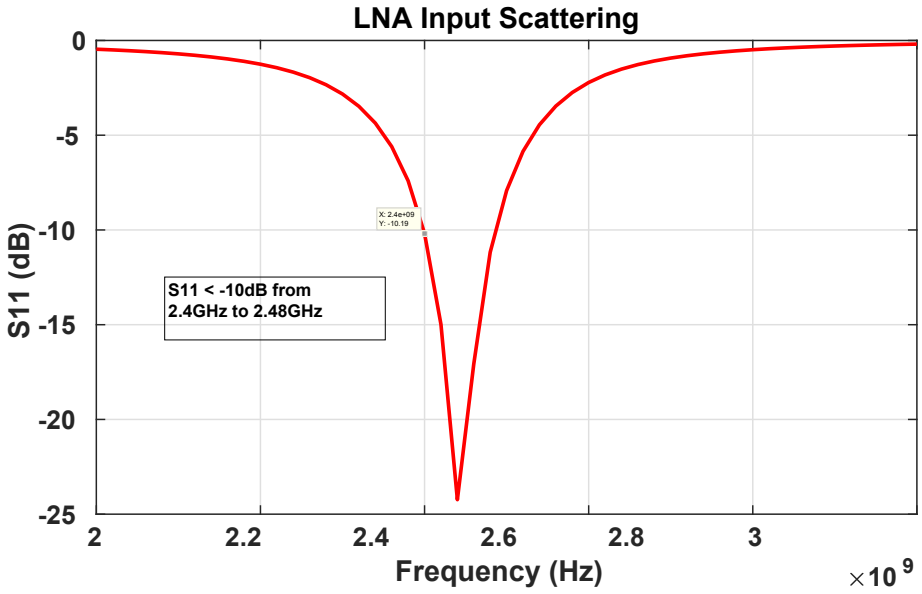


Figure 25: Input scattering

The gain of the LNA was found to be above 16 dB for the whole bandwidth while achieving the gain of 17.2 dB at 2.4 GHz as shown in Figure 26.

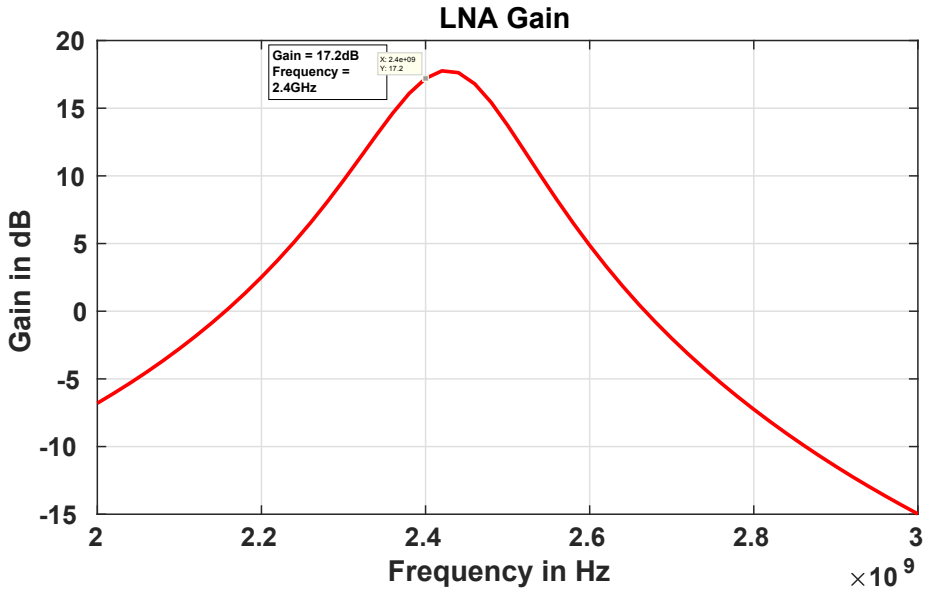


Figure 26: Differential LNA gain

After the input scattering and gain, the noise figure of the LNA was simulated and is 7.3 dB for the whole bandwidth 2.4 GHz to 2.48 GHz, while achieving a noise figure of 7.267 dB at 2.4 GHz. The noise figure graph for the LNA is shown in Figure 27.

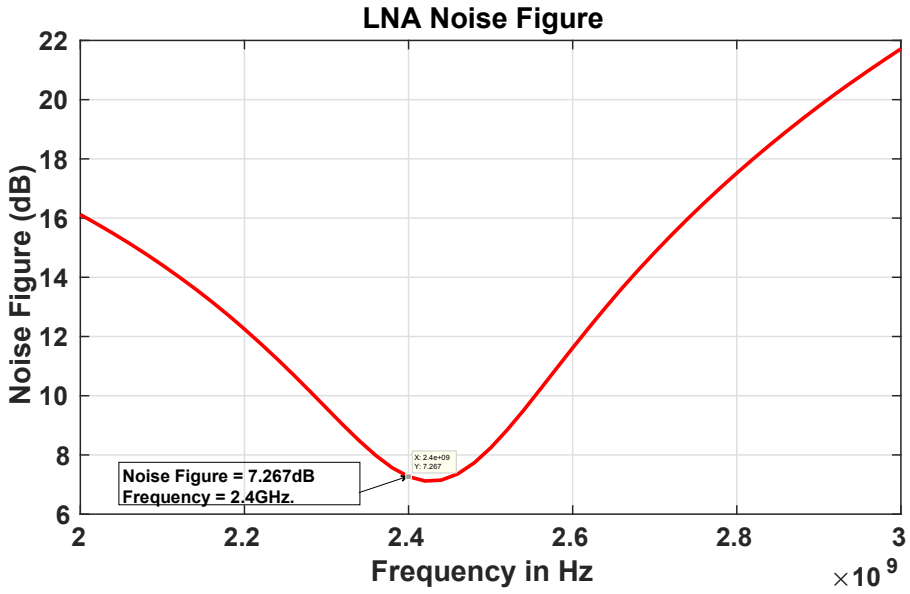


Figure 27: LNA noise figure

The linearity of LNA was determined by 1 dB compression point and IIP3 simulations. The 1 dB compression point and IIP3 simulation results for the designed LNA are shown in Figures 28 and 29 respectively. The 1 dB compression point is -10.394 dBm and IIP3 is -8.23 dBm.

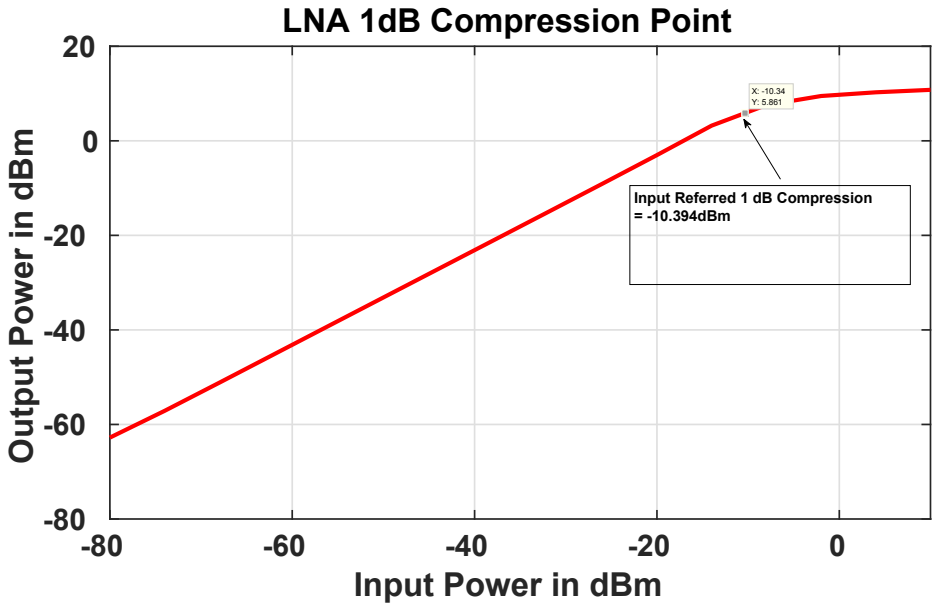


Figure 28: LNA 1 dB compression point

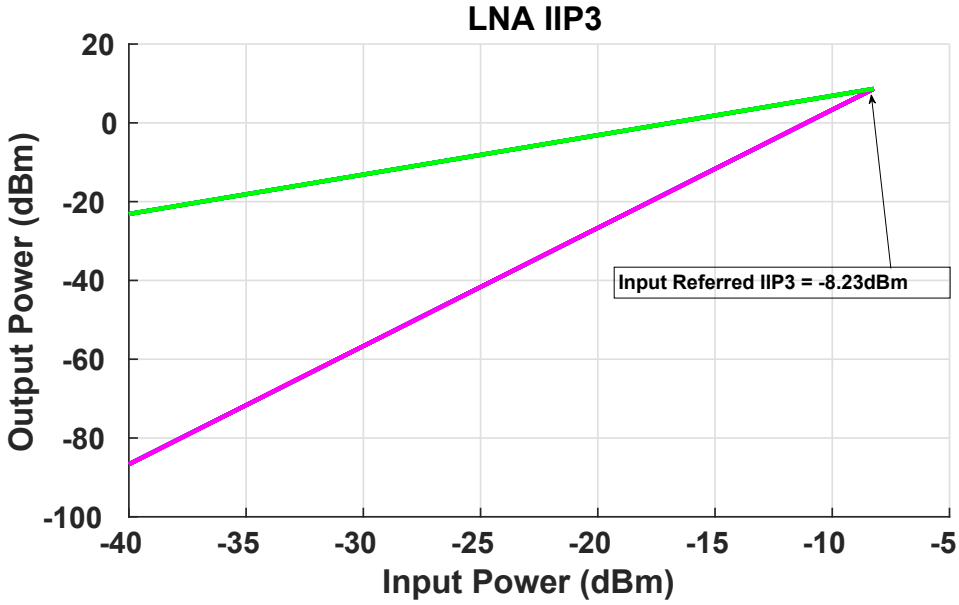


Figure 29: LNA IIP3

The post-layout simulation results for the LNA are collected in Table 2.

Table 2: LNA Post-Layout Simulation Results

Parameters	**Values**
S_{11}	$<$ -10 dB(2.4 GHz to 2.48 GHz)
Voltage Gain	17.26 dB @ 2.4 GHz
Noise Figure	7.3 dB
1 dB Compression Point	-10.394 dBm
IIP3	-8.23 dBm

5.2 Down-Conversion Mixer Design

The designed receiver included also a mixer, the design of which is described next. Passive mixers provide good linearity as compared to active mixers as discussed previously in chapter 3. Also, passive mixers do not consume power. For these main reasons a passive mixer is implemented in the design of our down-conversion mixer.

Since the output of the LNA is differential, a double-balanced passive mixer was implemented. A DC block capacitor is placed between the output of the LNA and the input of the mixer so that there is no DC current flow through the mixer, thus allowing only an AC signal to pass through the mixer. As the passive mixer presents a capacitive load to the LNA, the LNA was therefore tuned in such a manner that L_D oscillates with C_D as well as the capacitance of the mixer. The design of a mixer involves the selection of optimized dimensions of the switching transistors. The device dimensions are optimized through simulations. The dimensions of the switching-transistors are made large so that the on-resistance of the mixer is reduced.

Wide switching transistors have low on-resistance, but at the same time, they also possess high gate capacitance. Due to this, the device size was optimized in order to not to elevate too greatly the input capacitance of the switching transistors. As discussed earlier in chapter 3, a mixer requires abrupt switching. To ensure abrupt switching, an LO waveform must be a square wave, but at high frequency, LO wave forms resemble sinusoids. Therefore a large amplitude LO wave is choosen to ensure a minimum overlap time. Flicker noise in mixers is responsible for a high noise figure, which is mainly dependent on the DC bias current. To ensure no DC current flows through the mixer, a DC block capacitor was placed after the LNA to block the DC current from the LNA to the mixer. A double sideband noise figure was calculated for the implemented design because of direct conversion topology. The implemented design of the down-conversion mixer is shown in Figure 30.

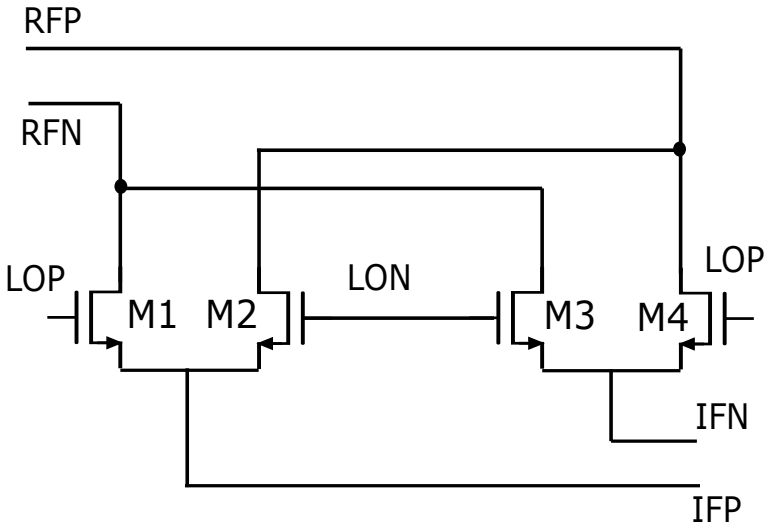


Figure 30: Double-Balanced Passive Down-Conversion Mixer

When considering the LO port, it will see the gate capacitance of the mixer switches. The IF port will see the high impedance input node of the baseband amplifier. Hence by keeping that in mind, a very high value resistance was placed at the output of the IF port to have a common-mode voltage of 0.6 i.e ($\frac{V_{DD}}{2}$) at the output of the mixer. The switching transistors (M1-M4) perform mixing operations, and because no DC current flows through the switches, the consumption of power is therefore low. The post layout simulation results of the mixer are collected in Table 3.

Table 3: Mixer Simulations

Simulation Results	
f_{RF}	2.4 GHz
f_{LO}	2.4 GHz
$M1 - M4$	$\frac{5.1\mu}{0.07\mu}$
Power Consumption	0
Mixer Conversion Gain	-1.32 dB
Noise Figure dsb	11.86 dB
1dB Compression Point	2.68 dBm
IIP3	24 dBm

5.3 Receiver Front End

Finally, the LNA and mixer were simulated together as a complete receiver for both the I and Q branches. In order to avoid cross talk between the I and Q signals, a 25% duty cycle LO wave was applied to the input of the LO port of the mixer. The post-layout simulation results of the receiver are collected in Table 4.

Table 4: Post Layout Simulation Results of Receiver

Simulation Results	
Supply Voltage	$1.2V$
f_{RF}	2.4 GHz
f_{LO}	2.4 GHz
Current Consumption	$209.2\mu A$
DC power Consumption	251.04 μwatts
S_{11} LNA	$<$ -10 dB
Conversion Gain of Receiver	$>$ 13 dB
1 dB Compression Point Overall	-11.8 dBm
Noise Figure Double Side band	8.3 dB
IIP3 of Receiver	-2.06495 dBm

The conversion gain of the receiver front end is shown in Figure 31. The conversion gain of the whole bandwidth was found to be greater than 13 dB. Figure 32 shows the 1 dB compression point for the overall receiver RF front end. A 1 dB compression point was found to be -11.8 dBm. The noise figure was also simulated for the RF front end. Figure 33 shows the double sideband noise figure of the RF front end of the receiver. The noise figure for the whole band was found to be 8.3 dB.

Figure 34 shows the overall IIP3 for the receiver front end. The overall IIP3 for the receiver was found to be -2.06 dBm. The receiver therefore satisfied the required specifications for BLE. Moreover, the noise figure specifications for the BLE are 20 dB; in our simulations the noise figure was 8.3 dB, which is well within the requirements of the specification. Similarly the IIP3 specification for the whole receiver is -31 dBm, however, the RF front end has an IIP3 of only -2.06 dBm which is also within the specified limits.

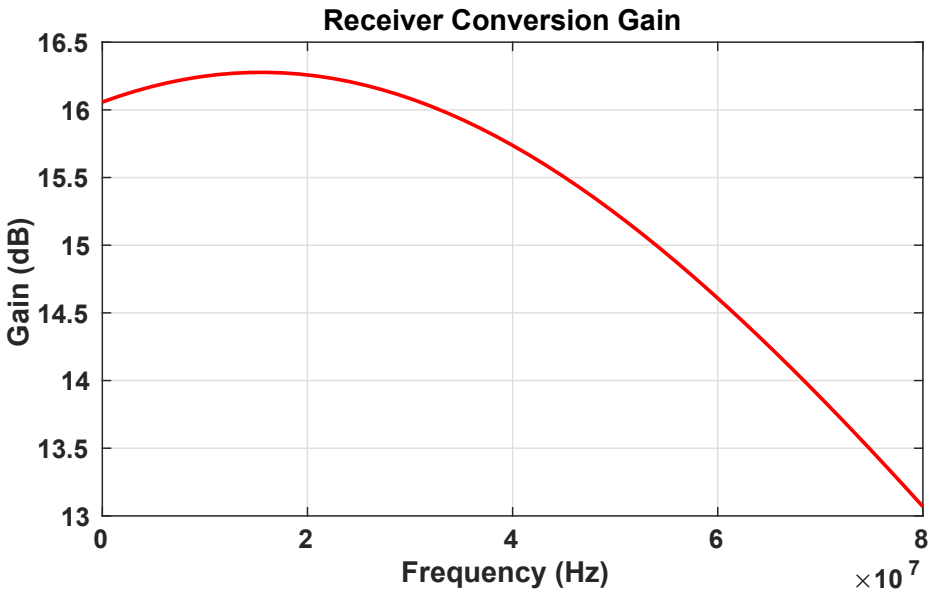


Figure 31: Receiver conversion gain

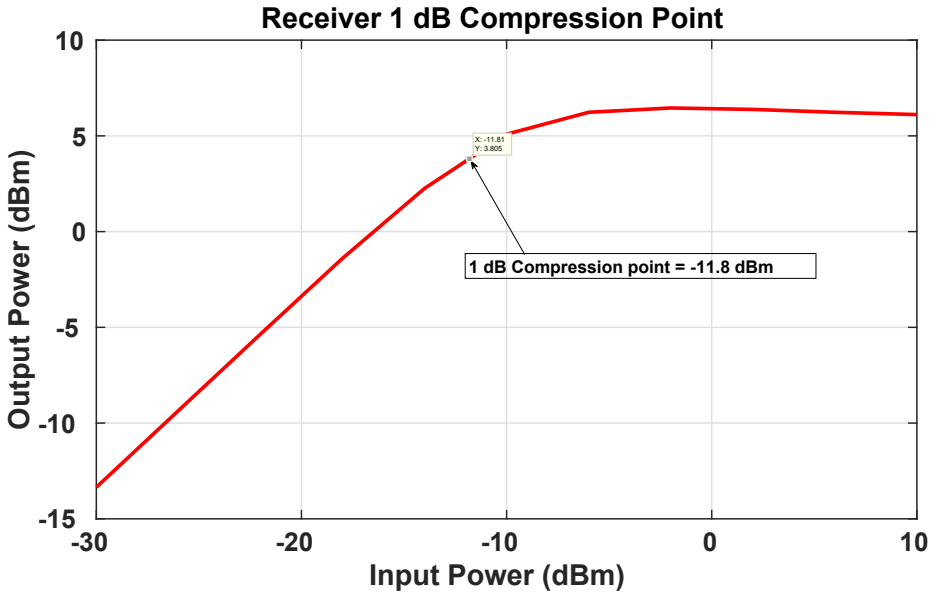


Figure 32: Receiver 1-dB compression point

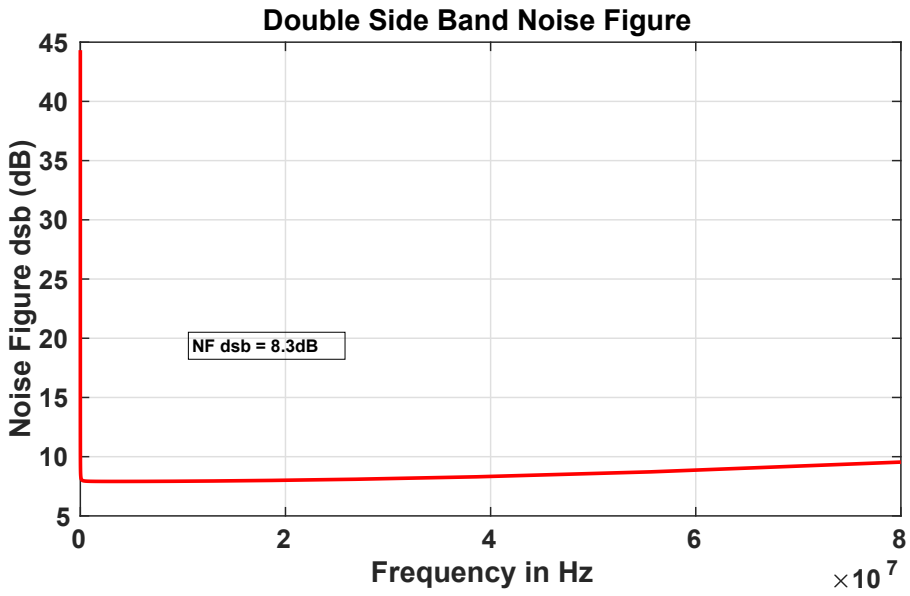


Figure 33: Double sideband noise figure

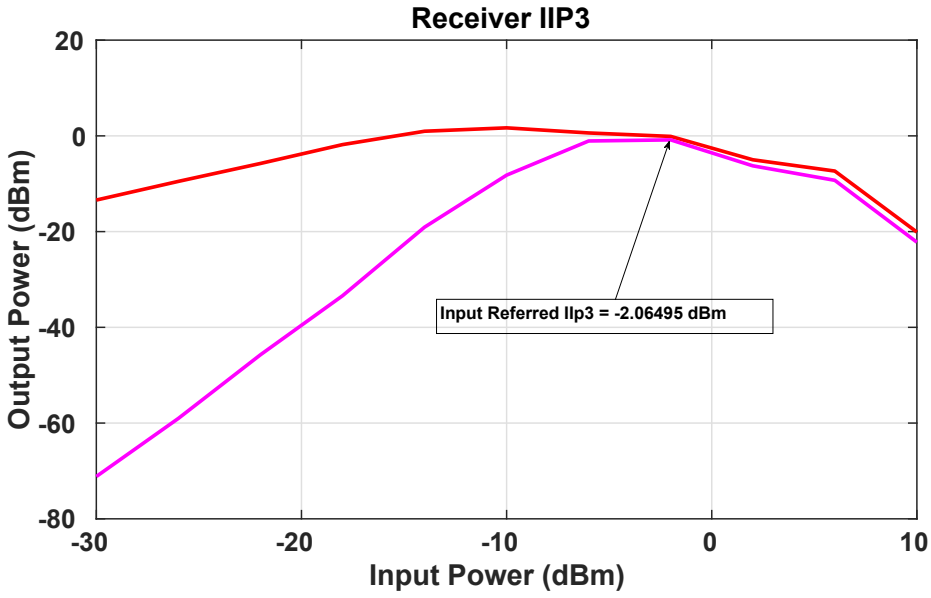


Figure 34: IIP-3 of receiver

5.4 Power Amplifier Design

The transmitter design consists of the up-conversion mixer and a power amplifier. The power amplifier is the most crucial block while considering transmission. Its performance enables efficient data transmission. As it deals with high power, power consumption is therefore high in this block. Design of a class E power amplifier is discussed in this section. The power amplifier block comprises two blocks, the driver stage and the ouput stage, as shown in Figure 35.

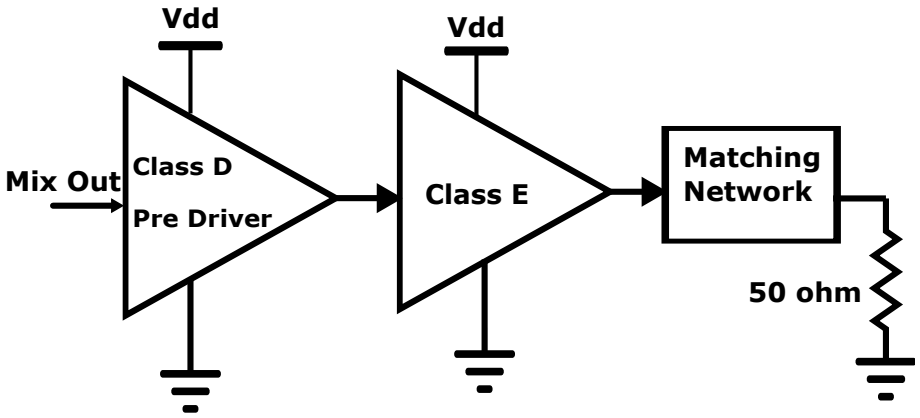


Figure 35: Complete PA chain

Because of high efficiency and simplicity in design, class E power amplifier topology was selected. The implemented class E power amplifier is shown in Figure 36.

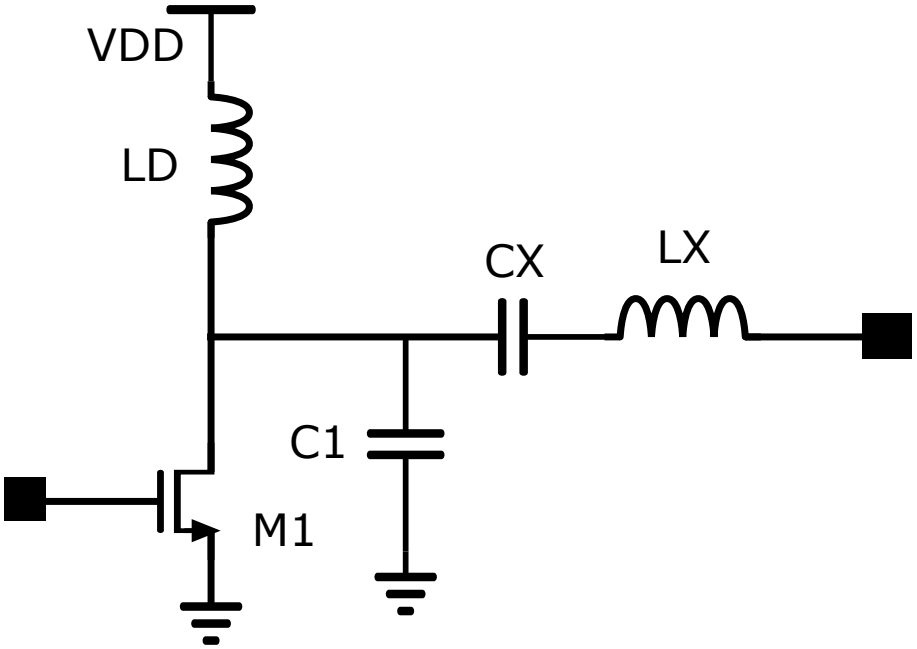


Figure 36: Class E power amplifier

As seen in Figure 36, the PA is composed of several components, L_D behaves as finite DC-feed inductance, L_X and C_X behave as an LC resonator which resonates

Table 5: Power Amplifier Component values

Component Values	
Supply Voltage	1.2 V
L_D	3.620 nH
C_1	694.8 fF
C_X	1.01 pF
L_X	1.338 nH
M_1	$\frac{50\mu}{0.06\mu}$

at the frequency of operation i.e 2.4 GHz. M1 acts as a switch which turns ON and OFF at the input frequency. L_X and C_X allow only the signal current at 2.4 GHz to pass through the load. This reactance will be either capacitive or inductive at other frequencies depending upon the values of L_X and C_X. C1 ensures that when the switch M1 turns OFF, voltage across it still remains at some low value such that the drain current becomes zero. The Component values of the power amplifier are shown in Table 5.

As discussed in chapter 4, there are two practical implementations for this class E amplifier which are ZVS and ZCS. Both of them use zero-derivative switching (ZDS), in which the switch turns OFF with zero current and turns ON with zero voltage, so that there must be no overlapping current and voltage wave forms. The power amplifier is composed of two stages, the input and output stages. The output stage will mainly define the efficiency of the power amplifier.

In a class E amplifier, L_D can be used as either an RFC or a DC-feed inductor, but according to [44], using L_D as a DC feed inductor gives the advantage of a low value inductor, which saves the chip area. A small DC-feed inductance is effective when DC voltage and load resistance are specified and high output power is needed.

For topology based on DC-feed inductance, the output power depends upon the quality factor of the LC tank circuit. The output power will increase if the quality factor is large and decrease when the quality factor is small.

Table 6: Specifications For PA

Specifications	**Value**
Supply Voltage	1.2 V
f_{RF}	2.4 GHz
P_{output}	-6 dBm to 4 dBm
R_L	50Ω

In Table 6, the specification for the power amplifier is shown, the maximum output power specification being 4 dBm. However, the designed power amplifier has a maximum output power of 11 dBm, to compensate the losses contained in the output matching network and the off-chip balun. The component values for the design were calculated using the design equations from [45, 46, 47, 26]. Now the values of full load resistance, inductance L_D and capacitance C1 were calculated using the following equations [26]:

$$R_{FullLoad} = K_P \times \frac{V_{DD}^2}{P_{out}} \tag{79}$$

$$L_D = K_L \times \frac{R_{FullLoad}}{\omega_o} \tag{80}$$

$$C_1 = K_C \times \frac{1}{\omega_o R_{FullLoad}} \tag{81}$$

The values of K_P, K_C and K_L were found from the graph [26], given in Figure 37.

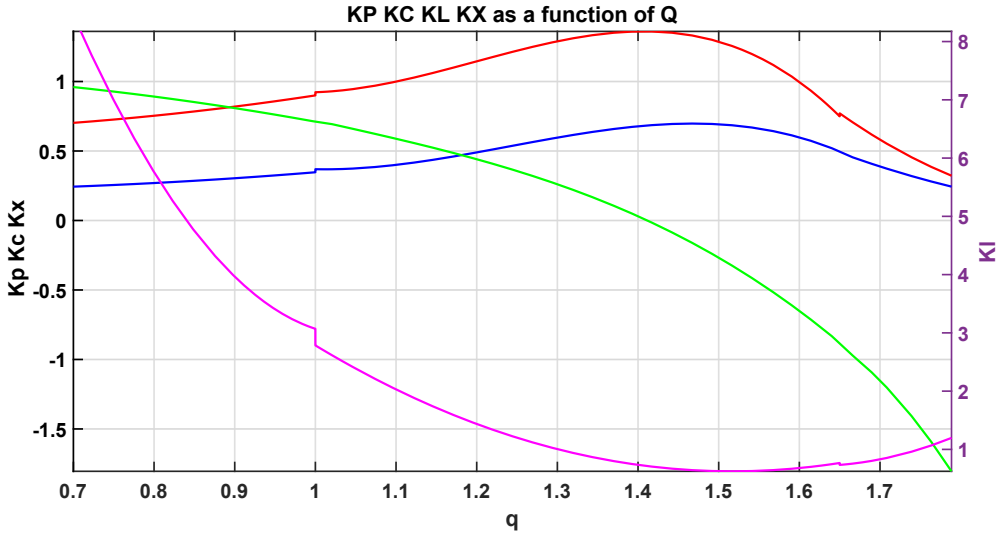


Figure 37: K_P, K_C, K_L and K_X as a function of quality factor of DC-feed inductance

However the inductor L_D will resonate with C1 as well as with the parasitic capacitance of M1. The dimensions of the input transistor will play an important role in the performance. The transistor posses some on-resistance, which can be minimized by making the width of the transistor wider. However the use of larger transistor dimensions will also result in high parasitic capacitance, leading to trade off in the performance.

As can be seen from the on-resistance equation given in [48], the on-resistance is inversely proportional to the current. Therefore, the current should be increased to minimize the on-resistance.

$$R_{on} = \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}(1 - \frac{7}{9}\lambda V_{DD}) \tag{82}$$

The gate length of the transistor should be as small as possible, therefore the minimum length allowed by the technology is selected. First assuming that the transistor is in saturation, the width of the transistor can then be calculated using Equation 83, given in [49]:

$$W = \frac{I_D \times 2L}{Kn(V_{gs} - Vth)^2} \approx 200\mu \tag{83}$$

The values of L_X and C_X were simply calculated as follows:

$$L_X = \frac{QR_{Fullload}}{\omega_o} \tag{84}$$

$$C_X = \frac{1}{Q\omega_o R_{FullLoad}} \tag{85}$$

A post-layout simulation for the power amplifier was performed. The power amplifier efficiency was determined in terms of power added efficiency and drain efficiency. Output matching for the power amplifier was also simulated and the output power was determined. The results that were obtained are shown in Table 7.

Table 7: Power Amplifier Simulation Results

Specifications	**Value**
Output Power	11 dBm
Drain Efficiency	34%
Power Added Efficiency	34%
S_{22}	< -15 dB

Figure 38 shows the output power for the power amplifier. The maximum output power was found to be 11 dB at the input power of -5 dBm.

The drain efficiency was also simulated for the power amplifier. Figure 39 shows the drain efficiency of the power amplifier. The maximum drain efficiency was found to be 36% at the input power level of 0 dBm.

Figure 40 shows the simulation result of the power added efficiency for the power amplifier. The maximum power added efficiency was found to be 34% at the input power level of -5 dBm.

Figure 41 shows the output scattering (S_{22}) of the power amplifier. The ouput scattering for the band of interest, was found to be below -15 dB.

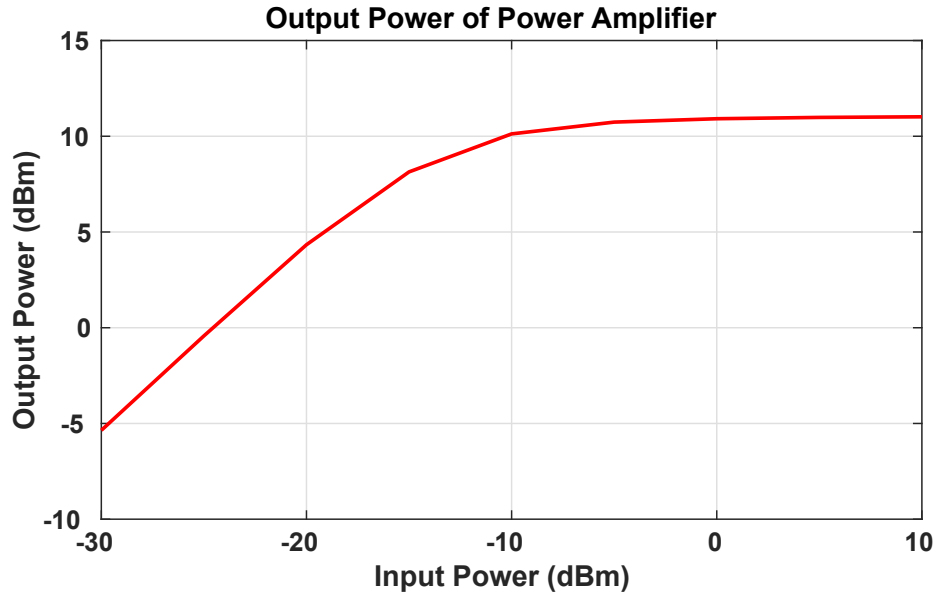


Figure 38: Output power of power amplifier

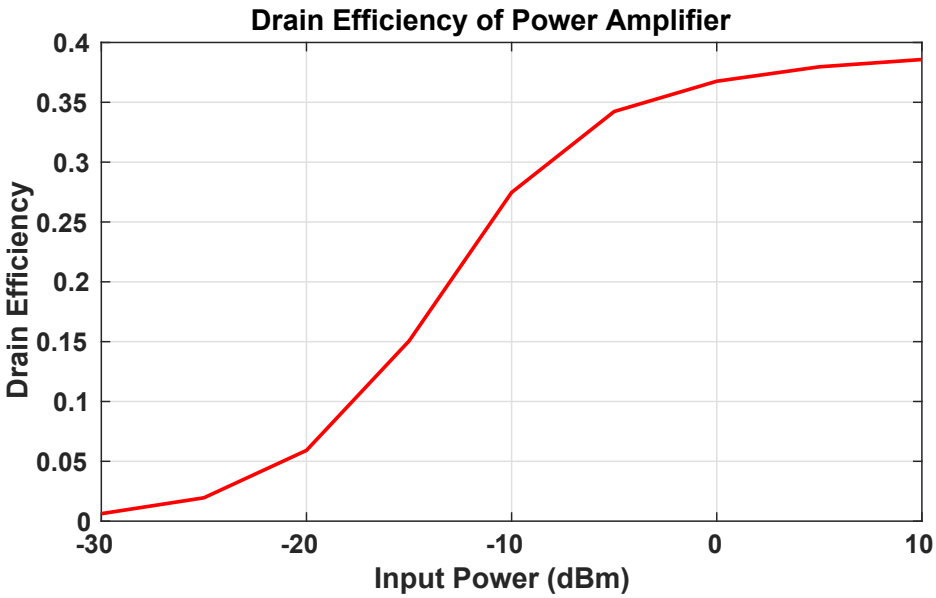


Figure 39: Drain efficiency of power amplifier

5.4.1 Driver Stage

The design procedure of the pre-driver circuit is described in this section. The design of the pre-driver stage should be done carefully, because it directly affects the performance of the whole power amplifier.

A resistive feedback inverter topology is used as the pre-driver amplifier. The RC time constants at the input and output nodes define the bandwidth of this topology [50]. The operating bandwidth depends upon the parasitic capacitance of the CMOS transistors. The implemented design is shown in Figure 42.

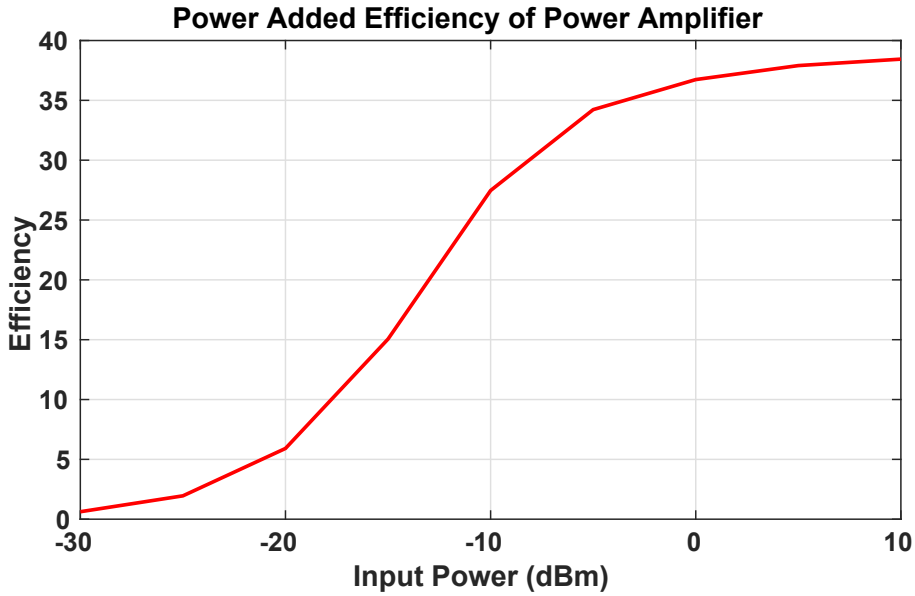


Figure 40: Power added efficiency of power amplifier

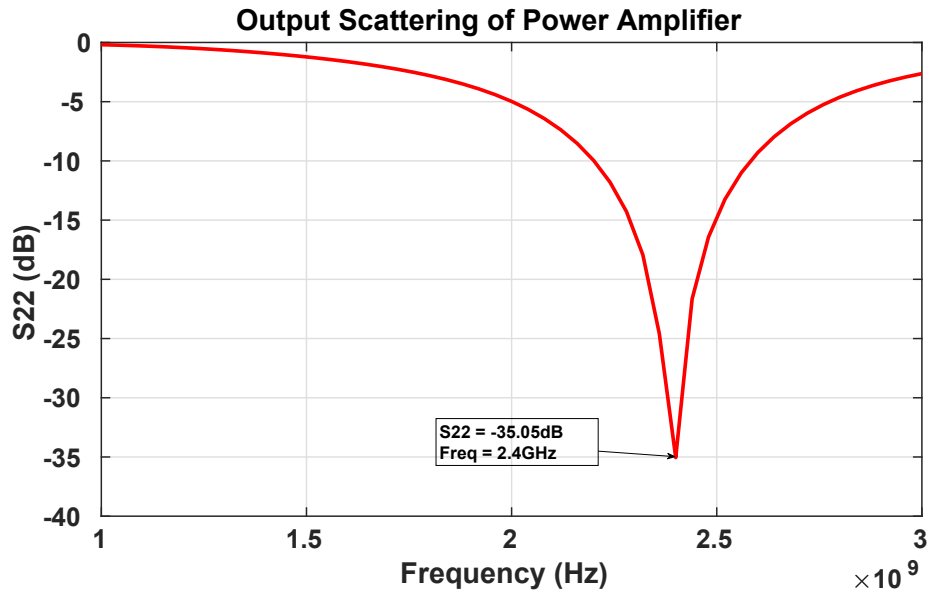


Figure 41: S_{22} of power amplifier

In this circuit, the inverter acts as a non-linear amplifier because of the feedback resistor R_f. The R_f biases the inverter to the point of equal drain current. Therefore the DC operating point will be settled to $\frac{V_{DD}}{2}$.

Several driver amplifier stages are required to drive the power amplifier because of large gate capacitance. The dimensions of the inverter were designed by first simulating a chain of inverters containing two inverters driving the input impedance of the class E amplifier. The W/L ratio was determined so that it would yield a symmetric design as well as keep the propagation delay within an affordable range.

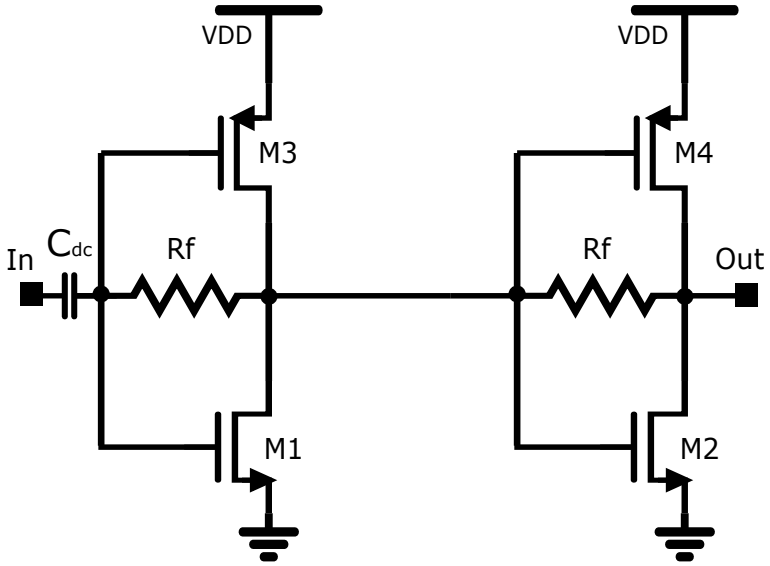


Figure 42: Driver stage for PA

To make the rise and fall time of the inverter the same, the width of the PMOS transistor was made 2.5 times larger than the width of the NMOS transistor. In order to drive the input impedance of the PA, the next inverting stage was made two times larger than the previous one. The dimensions of the transistors are shown in Table 8.

Table 8: Components Parameters of Pre-driver

Specifications	**Value**
Supply Voltage	1.2 V
R_f	7.5 $k\Omega$
$M1$	$\frac{16\mu}{0.06\mu}$
$M2$	$\frac{32\mu}{0.06\mu}$
$M3$	$\frac{40\mu}{0.06\mu}$
$M4$	$\frac{80\mu}{0.06\mu}$

Transient analysis simulation was performed to check the waveform of the predriver input and output, where Figure 43 shows the transient waveforms for the input and output. The pink waveform is the input wave form having a peak-to-peak voltage of 200 mV and the red colored waveform is the output of the pre-driver. We can see from the figure that the pre-driver has amplified the input waveform as well as converted it to a square wave with a peak voltage of 1.2 V.

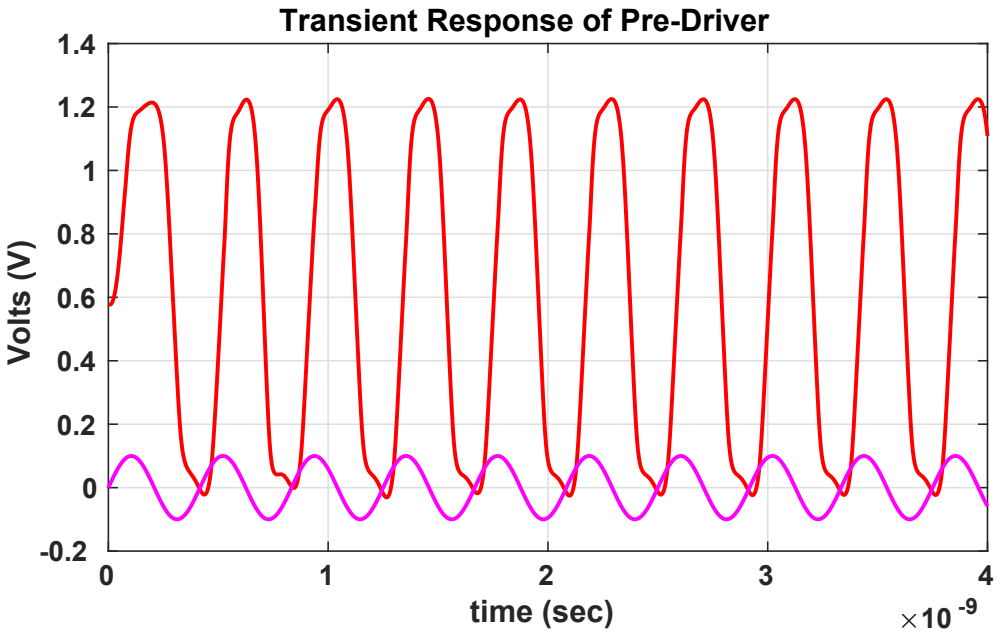


Figure 43: Transient response of pre-driver

5.5 Up-Conversion Mixer Design

The designed transmitter included also a mixer, the design of which is described next. For transmission the baseband signal needs to be up-converted to RF frequencies. An up-conversion mixer translates the signal from the baseband to RF frequency for transmission. Several mixer topologies can be implemented for up-conversion. The double-balanced passive topology has been widely implemented in several designs because the baseband signals are mostly in differential form. However in this design, the baseband signals are single ended. Therefore, a single-balanced passive mixer is implemented as the up-conversion mixer in this circuit design. The designed mixer is shown in Figure 44.

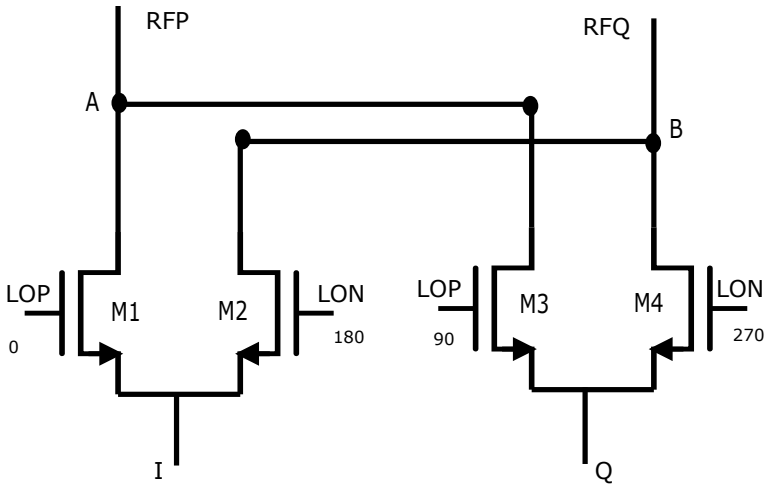


Figure 44: Up-conversion mixer

As the designing of a mixer is a challenging task, several simulations were therefore performed to achieve the expected results. The dimensions of the switching transistors were optimized to minimize the conversion loss. The dimensions of the designed mixer is shown in Table 9. Since the output of the baseband signal is single-ended i.e I and Q, they are combined at nodes A and B into two signals. The switches M1-M4 sample the IF current with the frequency of the LO, while those currents are summed up at nodes A and B, thus combining the I and Q signals. Wider switches are implemented to minimize loss. Ideal LO waveforms were applied to simulate the mixer. Usually an LO buffer is implemented in an up-conversion mixer to avoid the pulling effect.

To avoid cross talk between the I and Q signals, a 25% duty cycle was applied at the LO port. Passive mixers provide good linearity as compared to active ones. M1-M4 operate in the triode region, when the LO signal is high. Theoretically a passive mixer does not contain any DC-power. To ensure that no DC current flows through the mixer, DC block capacitors were placed between the mixer and the pre-driver amplifier. The post-layout simulation results are shown next.

Figure 45 shows the conversion gain of the mixer. Since the mixer is passive, therefore it provides loss. The mixer loss is 5.1 dB as shown in Figure 45.

Table 9: Mixer Performance

Specifications	Value
F_{LO}	2.4 GHz
$M1 - M4$	$\frac{8\mu}{0.06\mu}$
F_{IF}	250 K
1 dB Compression Point	-5.013 dBm
$IIP3$	0.352 dBm
Mixer Conversion Gain	-5.15 dB

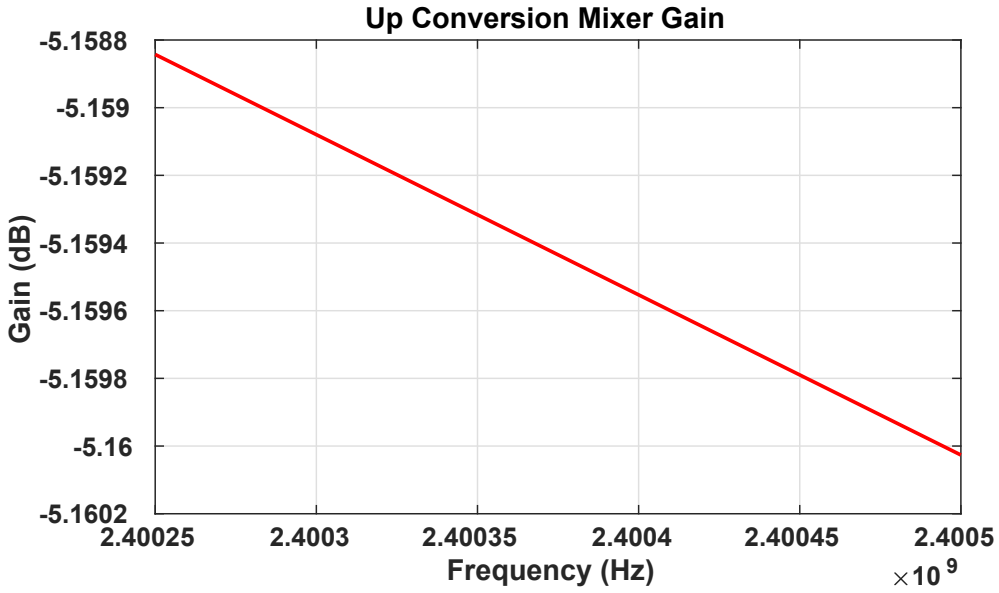


Figure 45: Up-conversion mixer gain

A 1 dB compression point for the up-conversion mixer is shown in Figure 46. The 1 dB compression point is -5.103 dBm.

Figure 47 shows the IIp3 value for the up-conversion mixer. The IIp3 value for the up-conversion mixer is 0 dBm.

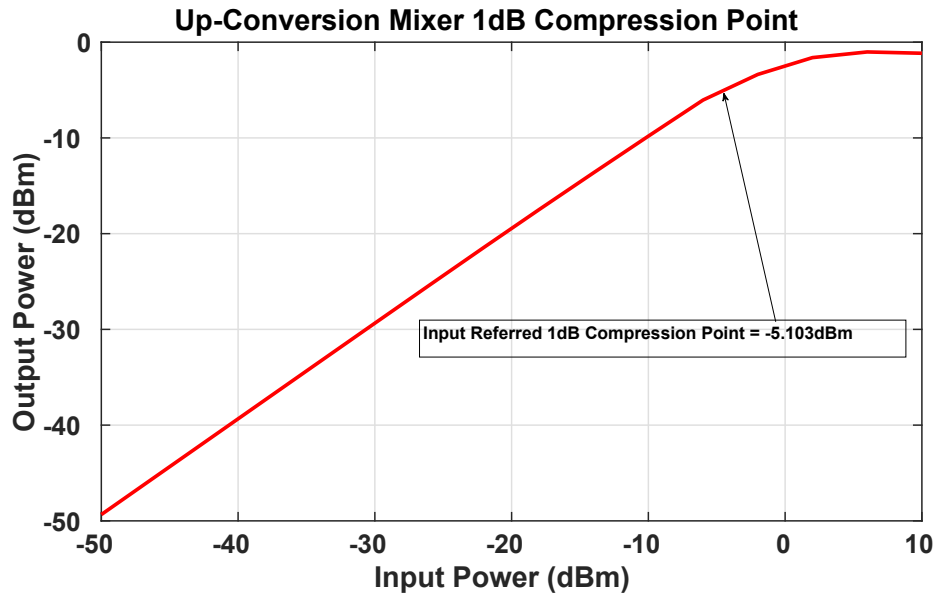


Figure 46: Up-conversion mixer 1 dB compression point

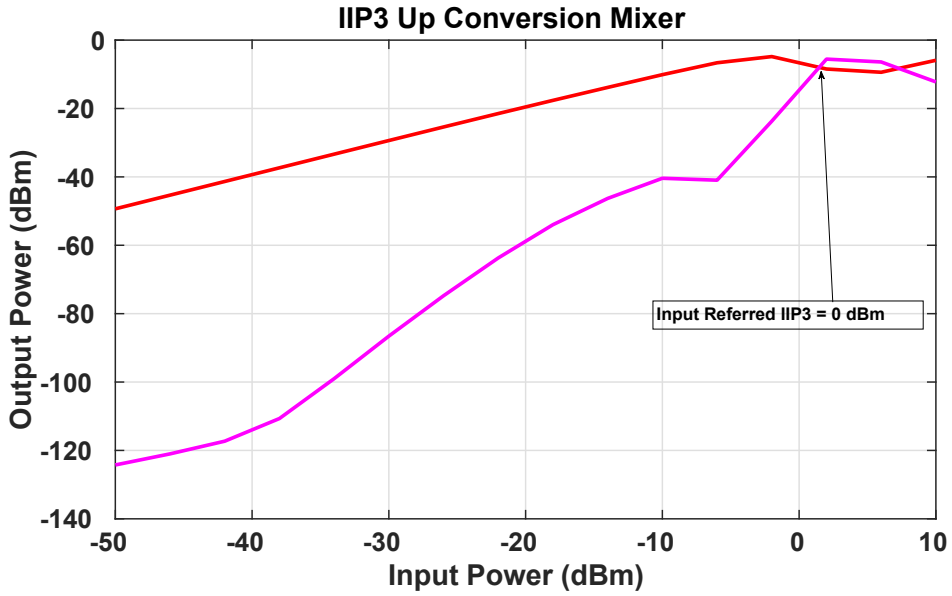


Figure 47: Up-conversion mixer IIP3

5.6 Transmitter Front End

Finally, the mixer, driver and power amplifier were connected together to form the transmitter. The performance of this transmitter was then characterized by simulations. The overall gain for the blocks was found. Transient analysis was additionally performed to find the spectral view of the final signal, which is shown in Figures 48 and 49 respectively. The simulated performance of the transmitter is collected in Table 10.

Table 10: Transmitter Performance

Specifications	**Value**
Supply Voltage	1.2 V
Maximum Output Power	11 dBm
Maximum Drain Efficiency	34%
Maximum Power Added Efficiency	34%
Output Scattering	$<$ -15 dB
Overall Transmitter Gain	24 dB
Power Consumption	1.4 mwatts

The transmitter gain is found to be 24.8 dB as shown in Figure 48.

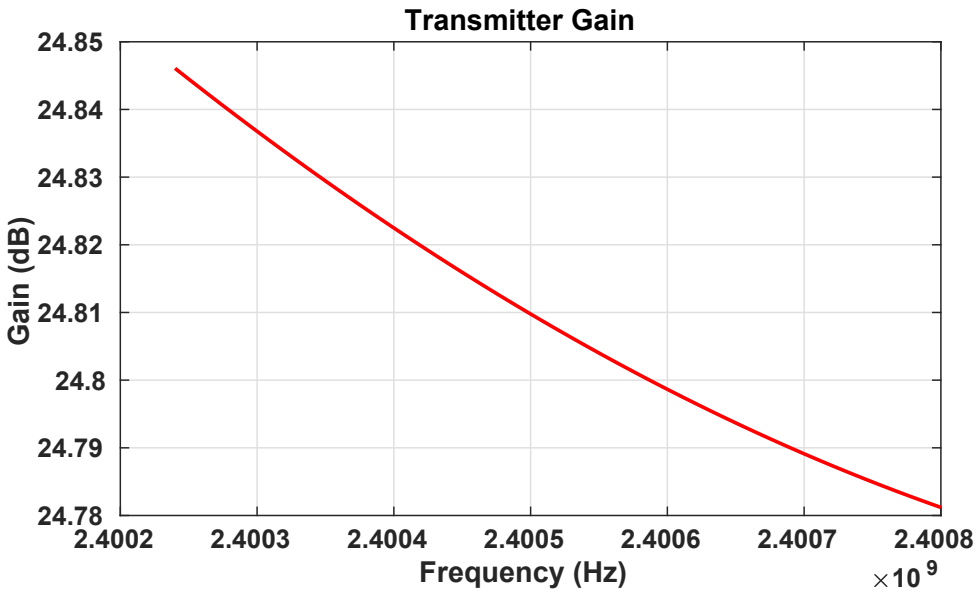


Figure 48: Overall transmitter gain

Figure 49 shows the spectral view of the transmitter chain. As can be seen, there are harmonics present out of the band as well; this is because class E amplifiers are

quite non-linear and exhibits a trade off between the efficiency and harmonic content. For a low harmonic the quality factor of the output tuning network should be high, and here the quality factor of the tuning circuit is not high enough to filter the harmonics. However the peak value of the harmonics is not high enough to interfere with the other signals.

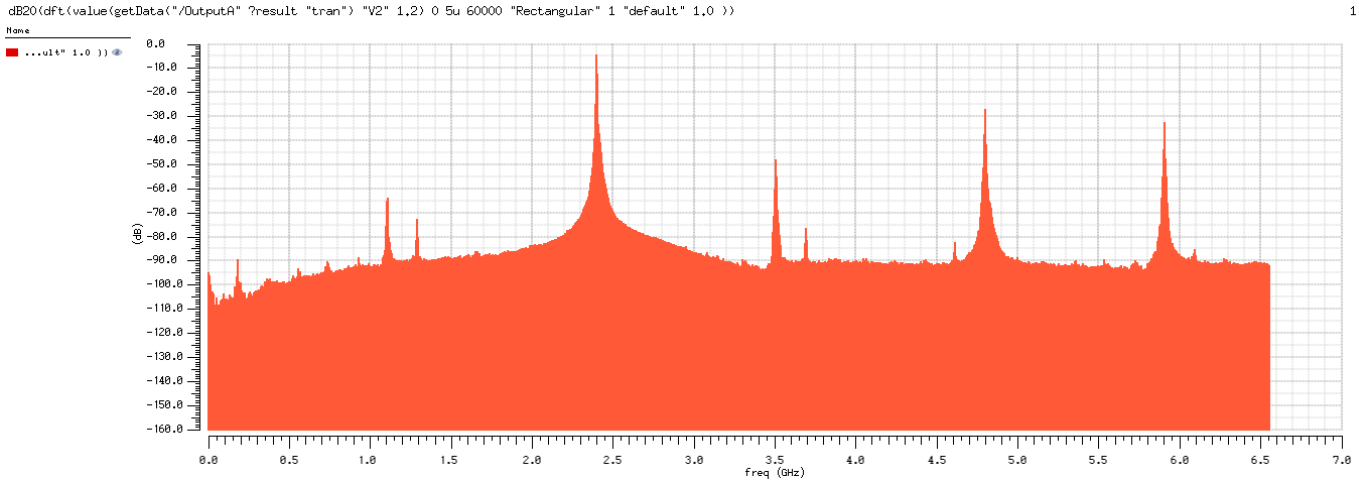


Figure 49: Spectral view

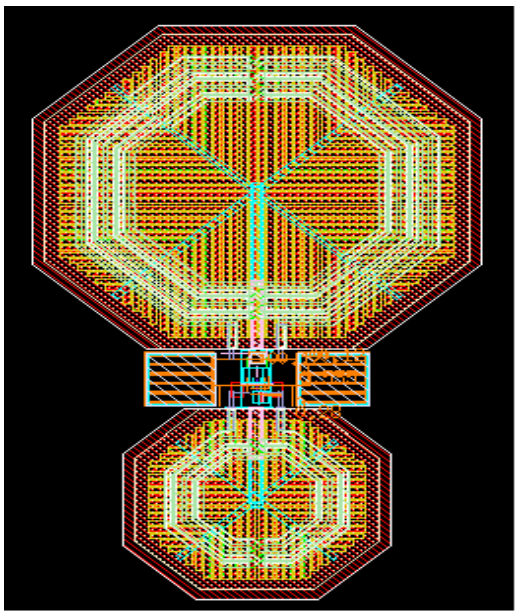
5.7 Layout Consideration

In this chapter layout design considerations of the circuit are discussed. Virtuoso layout editor software was used to design the layout. When considering layout, a few considerations were taken into account, which alter the performance of the design. Therefore to minimize these effects the following steps were taken into account:

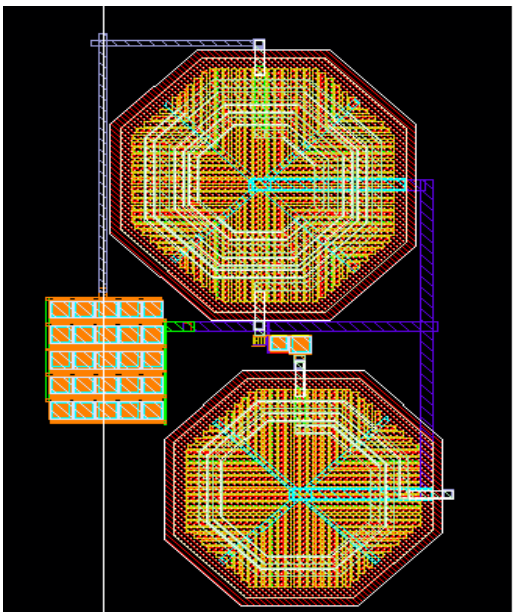
- *Symmetry*: Matching transistors, especially in the case of input differential transistors, symmetry is considered during the design.
- *Neighborhood*: In order to minimize offset, the neighborhood of the differential transistors was kept as similar as possible.
- *Orientation*: Orientation of the transistors was done in such a manner that matched transistors were arranged in either horizontal or vertical arrangement.
- *Metal Routes*: All even and odd metal layers were used to consider either vertical or horizontal routing or vice versa to manage the layout.
- *Vias*: Multiple vias was inserted to minimize the resistance and to increase the reliability.
- *Supply lines*: Wider width for materials were used for power supply lines to minimize resistance.

Common centroid topology was applied to minimize the mismatching and offset. To ensure the design according to the design kit rules, continuous checking of the design rule check (DRC) was performed. After completion of the layout, a layout vs schematic (LVS) was performed to ensure that the designed layout is in accordance with the schematic design. After all of these steps, Calibre View (RC) extraction of the design was performed to estimate the parasitic effects of the layout, and after the extraction, simulation was once again performed. The layout of the final circuit design is shown in Figure 50. The area consumed by the LNA and mixer combined was found to be $524.51\mu \times 311.84\mu$. While the area of the PA, pre-driver and mixer was found to be $552.63\mu \times 333.95\mu$, $82.525\mu \times 90.425\mu$ and $8.25\mu \times 5.55\mu$ respectively.

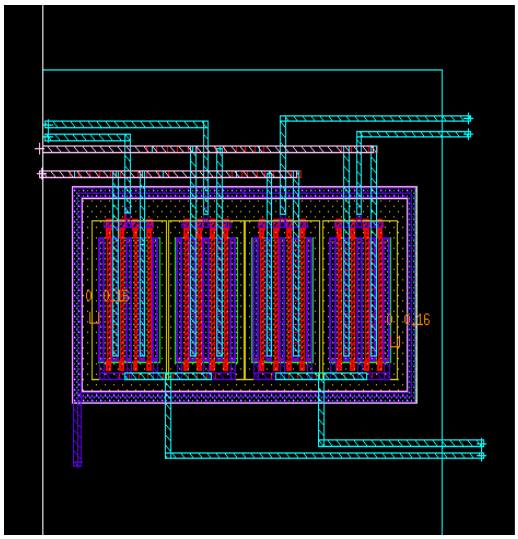
Because of the large dimension of the inductors, the other components are not very clearly visible in the picture. After the design of the layout, the post layout simulations were performed, and these have already been discussed in the previous section.



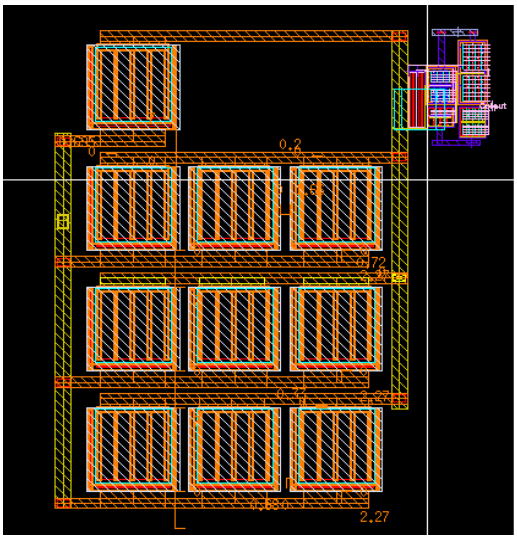
(a) LNA and Mixer together



(b) Power Amplifier



(c) Mixer Up-conversion



(d) Pre-Driver

Figure 50: Layout design

6 Conclusion

The design and analysis of low power transmitter and receiver RF front-end blocks, for Bluetooth low energy applications, in 65nm technology, has been presented in this thesis. The designed RF front-end blocks were a low noise amplifier (LNA), a down-conversion mixer, a power amplifier (PA), a driver amplifier and an up-conversion mixer for the 2.4 GHz to 2.48 GHz frequency band.

All of the blocks were designed using CMOS transistors. The performance parameters of the LNA, such as the gain and noise figure linearity input matching, have been analyzed. A gain of more than 16 dB was achieved, with a noise figure of 7.3 dB and input matching less than -10 dB for the band of interest. A down-conversion mixer was discussed from a theoretical point of view as well as an implemented design which was analyzed. The down-conversion mixer was also simulated, and the gain, linearity and noise figure performance parameters were all analyzed. The LNA and the mixer were connected together to form a receiver. The performance of the receiver was analyzed. The conversion gain of the receiver was found to be greater than 13 dB for the whole band, while having a double-side band noise figure of 8.3 dB. The IIp3 of the receiver was found to be -2.036 dBm. The dc power consumption of receiver is 251.04 μwatts.

At the transmission side a power amplifier, driver amplifier and an up-conversion mixer have all been implemented in this thesis. The performance parameters of each of these blocks were analyzed. The power amplifier provides a maximum output power of 11 dBm at an input power level of -5 dBm. The power added efficiency was found to be 34%, while output matching S_{22} was below -10 dB for the whole band of interest. An up-conversion mixer provided a loss of 5 dB. The IIP3 of the up-conversion mixer was found to be 0 dBm. After designing the mixer and power amplifier, the whole transmitter chain was simulated by connecting these blocks together. The overall transmission gain was found to be 24 dB. The dc power consumption of transmitter is 1.4 mwatts.

The layout procedure has also been explained, and keypoints which were considered during layout design have also been explained. Parasitic extraction for the layout design has been performed. A design rule check (DRC) and layout vs schematic (LVS) were also performed for the designed blocks.

Regarding the future enhancements of the design, there is the need for a real oscillator to complete the whole RF blocks since ideal oscillator waveforms were used in the design simulations. A real oscillator, as well as baseband stages, will therefore need to be designed for the processing of the down-converted signal in order to complete the system.

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