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TECHNICAL PAPER

Focussed ion beam based fabrication of micro-electro-mechanical resonators

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Abstract A simple and fast process to fabricate micro-electro-mechanical (MEM) resonators with deep sub-micron transduction gaps in thin SOI is presented. The proposed process is realized on both 350 nm and 1.5 μm thin silicon-on-insulator (SOI) substrates, evaluating the possibilities for MEMS devices on thin SOI for future co-integration with CMOS circuitry on a single chip. Through the combination of conventional UV-lithography and focused ion beam (FIB) milling the process needs only two lithography steps, achieving ~100 nm gaps, thus ensuring an effective transduction. Different FIB parameters and etching parameters and their effect on the process are reported.

1 Introduction

Silicon micro-electro-mechanical (MEM) resonators have shown performances comparable to those of quartz resonators (Kaajakari et al. 2003; Yu-Wei et al. 2004) but they offer the advantage of higher levels of integration in electronic circuits. The research effort for these devices is currently focused on rather thick layers combined with deep sub-micron gaps (also referred to as nanogaps), as this allows reduction of the resonator's equivalent resistance (Kaajakari et al. 2003). Different fabrication processes have been proposed to create nanogap resonators in thick SOI (Ciressan et al. 2007; Pourkamali and Ayazi 2004), achieving good resonator performance. Thin SOI substrate is needed in order to enable a co-integration of MEMS and CMOS on a single chip, where the CMOS part can benefit from low leakage and high-speed, potentially offered by the SOI substrate. The fabrication of MEM resonators is therefore evaluated on such thin substrates to explore the possibilities for future co-integration. For this purpose, we propose a rapid prototyping fabrication process that offers the possibility to reduce the gap dimensions below 100 nm using focused ion beam (FIB).

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2 Device description and fabrication

2.1 Design

The design used in this process is mainly concentrating on square resonators with support in all four corners, resonating in a bulk lateral mode, and double clamped beams and tuning forks, resonating in a flexural in plane mode. Simple design allows achieving a high mechanical stability of the resulting resonators, especially in the 350 nm thin substrate. The square shaped bulk lateral resonators are designed to vibrate in a Lamé mode, as indicated with the dashed line in Fig. 1. The design is simulated with ANSYS® finite element method to take the release holes into account. With the given electrode configuration, it is also possible to excite a square extensional mode, where all four sides are moving in phase. The excitation and readout of the resonance is done electrostatically, with either two or three electrodes. The gap dimension is important, as it influences directly the motional resistance and the DC bias needed to excite the resonator. To simplify the FIB milling step, all designs were composed only of straight lines, as our FIB equipment did not allow creating rounded shapes easily.

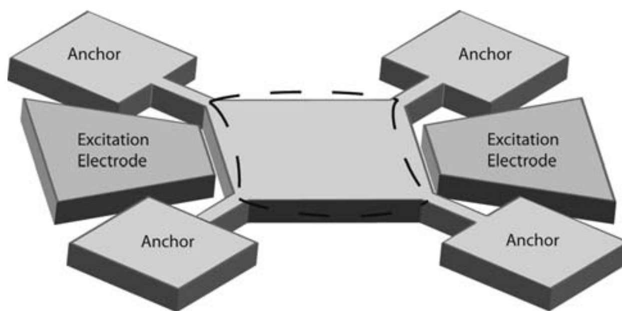

Fig. 1 Schematic view of a resonator with capacitive detection, the *dashed line* indicates the designed resonance mode (Lamé-mode)

2.2 Processflow

Two types of wafers were used: thin SOI wafers with a device layer of 340 and 400 nm buried oxide thickness and thicker SOI wafers having a device layer of 1.5 and 3 µm of buried oxide were used. The SOI wafers are heavily doped n-type to achieve good electrical contact. A dry thermal oxide of 300 nm is grown on top, which will serve as stop layer for the FIB milling and as hardmask for the silicon etching. This oxidation step reduces the SOI device layer thickness by approximately 150 nm to the final thickness of 200 nm and 1.35 µm, respectively. Patterning of the resonator structures is based upon a combination of standard UV lithography with a resolution of 800 nm and subsequent FIB milling of the photoresist to create sub 100 nm openings, with the goal of fabricating single crystalline silicon resonators and electrodes with a single mask step. A 500 nm thin photoresist (Shipley, S1805) is coated on the wafer and patterned by UV lithography (Fig. 1a). The resist is then locally milled away to create gaps in the order of 50–100 nm (Figs. 2b, 3). As it can be seen in Fig. 3a, the FIB milling is optimized to stop the Ga+-ions in the silicon dioxide layer and avoid Ga-contamination of the SOI device layer. This is important in order to avoid local masking effects that can occur during the reactive ion etching (RIE) and to keep the option for additional electrical functionality without gallium contamination. Reactive ion etching is used to transfer the patterns created by UV-lithography and FIB into the silicon dioxide hard mask in a single etch step. For the following silicon etch, different etch processes are evaluated (Fig. 1 c): the 1.35 µm thick SOI is etched with a high aspect ratio SHARP process (Ciressan et al 2007), while for the 200 nm thin SOI, two different etch processes (chlorine or fluorine chemistry) are compared with respect to their possible influence on the gap size. After patterning the silicon, the oxide hardmask is removed with a short BHF 7:1 etch. AlSi 1% is sputter deposited onto a two-layer

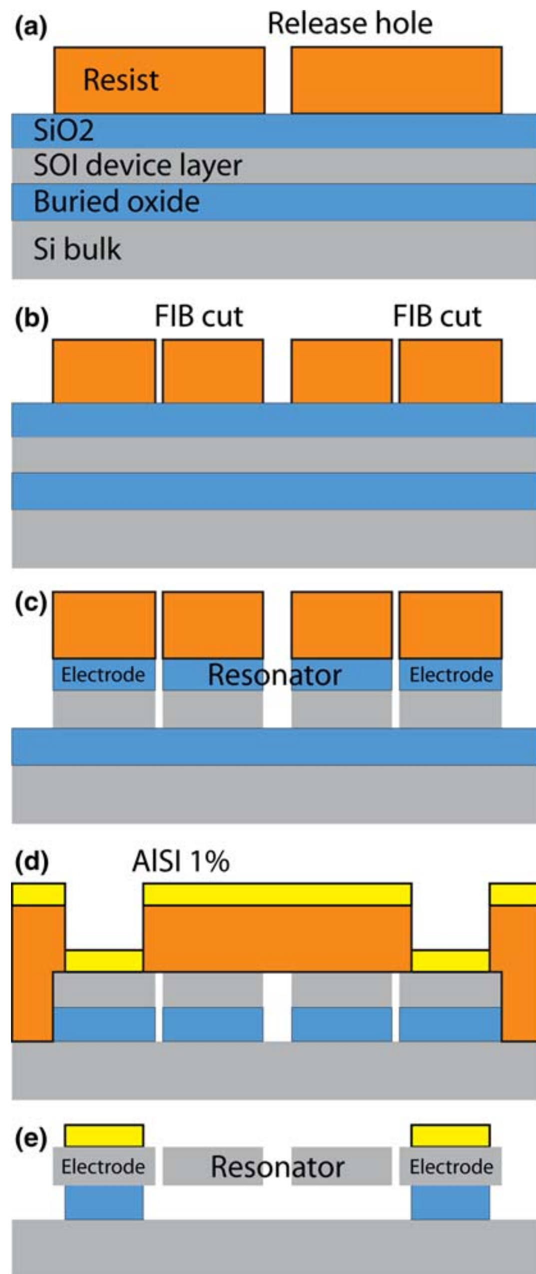

Fig. 2 Schematic of the process to create MEMS resonators with only two levels of photolithography. **a** UV lithography is done on a SOI wafer and **b** nano-size features are added through FIB milling. **c** SiO_2 and Si etching procedures are used to transfer the structure into the SOI device layer. **d** The metallization is done with a lift-off process and **e** the resonators are finally released and dried

lift-off resist (Microchem LOR5 A; Shipley S1813) to create the contacts on the pads (Fig. 1d). Annealing of the metal layer is done at 425°C. Finally the resonators are released using silox (pad etch) to etch away the buried oxide under the resonator (Fig. 1e) without etching the metal layer, followed by a CO_2 supercritical drying step.

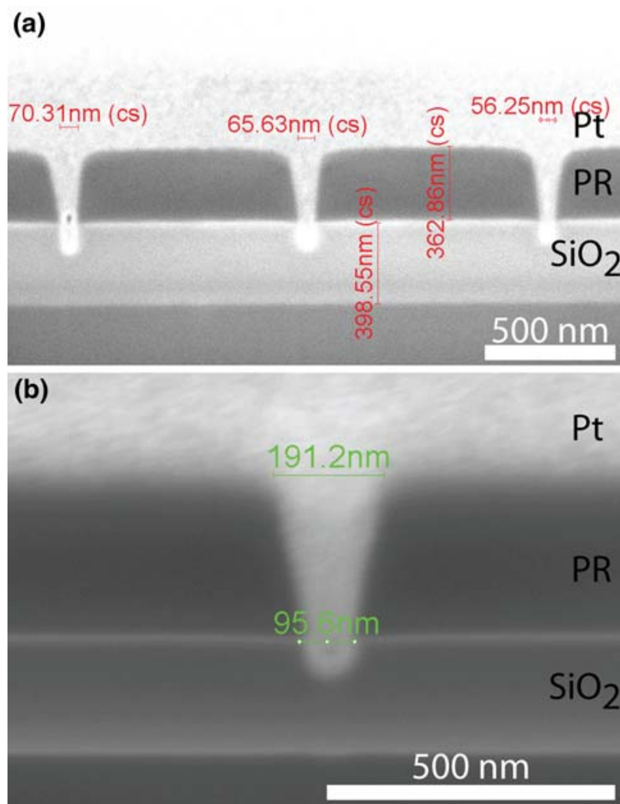

Fig. 3 Cross-section of a FIB milling test on SiO_2 layer. **a** Testing of three different equivalent depths (700, 800 and 900 nm from *right* to *left*) without H_2O enhancement. **b** The etching with H_2O enhancement results slightly larger opening at a shorter equivalent depth of 500 nm

3 Focussed ion beam milling

The combination of the appropriate FIB milling parameters together with a suitable etch process is a key element for rapid prototyping of nanostructures. This approach is interesting for validation of new nanogap MEMS devices, but has its limitations for high throughput applications. Ga+-Ion milling with and without H_2O enhancement (Stark et al. 1995) is tested on a FEI Nova 600 Nanolab, a SEM/FIB dualbeam system which is also equipped with a gas injection system (GIS).

Preliminary tests are done to determine ideal tradeoff between beam current and resulting size of the nanogaps in the resist. The theoretical minimal beam diameter is depending on the beam current and a smaller current is therefore promising a narrower gap, but a small current is also increasing the milling time and therefore slowing down the whole process. For our experiments, a tradeoff between time and resolution found with a Ga-ion current of 50 pA at 30 keV acceleration voltage (theoretical beam diameter of 19 nm) is used throughout all experiments.

Once the milling current is fixed, the milling time is adjusted to stop precisely in the silicon dioxide layer to avoid Ga contamination of the silicon layer. On the FEI dualbeam machine interface, time is automatically calculated as a function of surface and depth (milling volume), therefore timescales are indicated as an equivalent depth for a single line (beam overlap is 50%, dwelling time is 1 µs).

SRIM (http://www.srim.org/) simulation of Ga+ ions in a silicon-dioxide layer results in a stopping range of 27 nm and shows that all ions stop within approximately 60 nm. It seems therefore safe to stop the ion milling within the first 100 nm, to assure gallium free silicon in the device layer. The result of a milling test for equivalent depth of 700, 800 and 900 nm (in silicon) is shown in Fig. 3a, where 800 nm is suitable for the process.

3.1 FIB milling with H_2O

The GIS enables the use of different gases for either deposition or etching. A selective carbon milling (with Magnesium sulfate heptahydrate gas injection) process is compared to the conventional milling technique. The effect of the selective carbon milling seems to depend upon the product of the sputtered material and H_2O. The result is an increased milling efficiency of Ga+-ions on carbon containing materials (thus polymers also) and at the same time a reduction of the milling efficiency on SiO_2. With this technique and an ion beam current of 50 pA the equivalent depth could be reduced to 500 nm. The aspect ratio of the H_2O enhanced milling is reduced, as can be seen in Fig. 3b, compared to the FIB milling described above.

3.2 Charging and edge effects

Charging is a difficulty in this process, as the Ga+-ion beam tends to drift away from its initial position during the milling. This drift is time and current dependent and can be influenced by the milling parameters, but not fully canceled. To stop the drift motion, a strong electron current from a separate electron gun is used, with the disadvantage of disabling the in situ observation theoretically offered by the dual beam machine.

Two types of problems occur at the photoresist edge. The photoresist sidewall has an angle of approximately 45° (in a cross-section), making it virtually impossible to align the nanogaps precisely and leaving residual structures along the gap to air interface (Fig. 4a). Such structures or small overlaps of the designed gaps with the sidewall lead to shortcuts between the resonator and the electrodes. To reduce this problem, small circles or triangles are added on the resist edge. A second effect also appears at the outer end of the milled nanogaps. As can be seen on the Fig. 4b, the gap is narrowing towards the end, but this effect is also

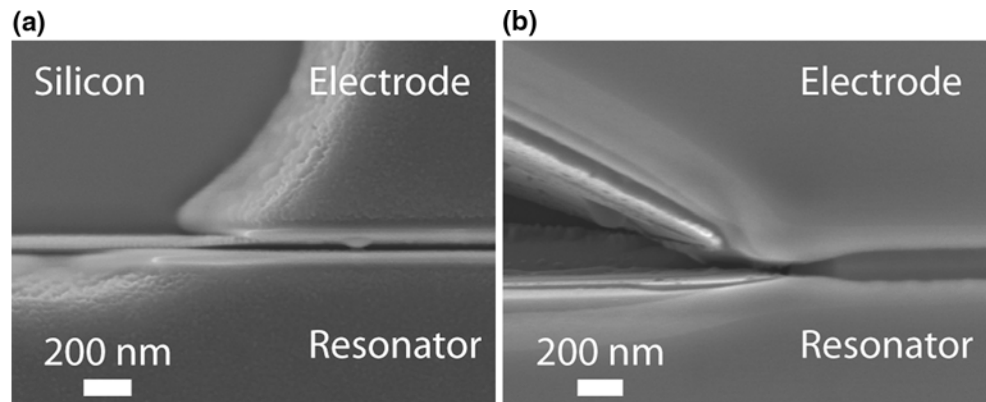

Fig. 4 *Top view* of a nanogaps after silicon dioxide etching without (**a**) and with an added *triangle* (**b**)

reduced, although not completely avoided, with the added structures.

These two problems do not occur with the H_2O enhanced FIB milling. In fact, due to the reduced thickness at the edge of the resist, this type of milling results in a slightly increased gap dimension with a smooth transition between the gap and the open area.

4 Nanogap etching

The transfer of the photoresist mask into the silicon dioxide is done using SF_6 based SiO_2 dry etching process, with a selectivity of 1:1 and an etch speed of 280 nm/min. This etch step does not show any dependence on the Ga ion concentration in the SiO_2 layer.

Two etch processes are compared to qualify the transfer of the SiO_2 hard mask into 200 nm thin silicon. A fluorine (SF_6) based silicon RIE etch (Si etch rate of 1 µm/min, selectivity 20:1 on SiO_2) is compared to chlorine (Cl_2) based ICP etch (Si etch rate of 0.35 µm/min, selectivity 1:1 on SiO_2). The combination of a conventional FIB milling and high selectivity fluorine etch process results in very small gaps, but a cross-section reveals that this process suffers from a rather large notching problem (Fig. 5a). The gap is much wider than expected over half of the resonator layer.

The chlorine etching process is successfully used to transfer larger gaps, created by H_2O enhanced FIB, into to the SOI device layer. A cross section showing the gap profile is shown in Fig. 5b. Gaps with widths of clearly less than 100 nm and almost vertical sidewalls are created with this process. The resulting thin SOI MEM resonator with nanogaps is shown in Fig. 6.

To etch the trenches into the 1.35 µm thick silicon, the high aspect ratio, high selectivity SHARP process is successfully employed. A cross section of a fabricated gap is shown in Fig. 5c, revealing the possibility to create ~50 nm gaps. Due to the narrowing of the gap at the edge

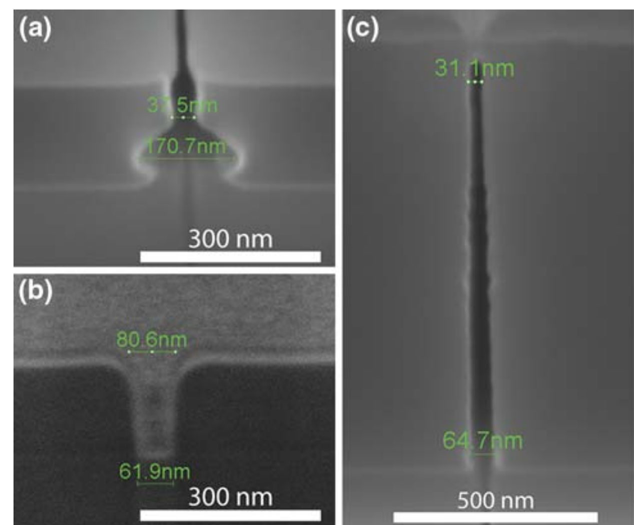

Fig. 5 Nanogaps created with **a** FIB without enhancement and fluorine etching. **b** H_2O enhanced FIB and chlorine etching in 200 nm thin SOI. **c** shows a cross section of a gap created by FIB without enhancement and SHARP process etching

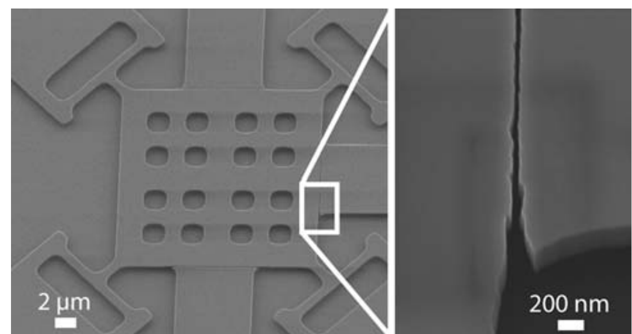

Fig. 6 Bulk lateral resonator with side length L = 20 µm (designed freq: 162 MHz) and nano-gap (< 100 nm) detection fabricated with the proposed FIB prototyping process

(Fig. 4b) combined with the high selectivity, the gaps tend to be closed (shortcut between the resonator and the electrode) at the end of the gap for such small dimensions.

Gaps of approximately 100 nm or more are not limited by this narrowing problem and result in functional resonators.

5 Conclusion

We have successfully demonstrated a rapid FIB prototyping process for fabricating deep sub-micron gap (31–65 nm in the best case) MEM resonators in 200 nm and 1.35 μm thin SOI with only two mask levels. The impact of two different FIB milling processes combined with two different silicon etches are investigated, to optimize the fabrication of 100 nm gaps in thin silicon.

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