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Programmable Switched Capacitor Finite Impulse Response Filter with Circular Memory Implemented in CMOS 0.18 μm Technology

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Abstract This paper presents a programmable multi-mode finite impulse response (FIR) filter implemented as switched capacitor (SC) technique in CMOS 0.18 μm technology. Intended application of the described circuit is in analog base-band filtering in GSM/WCDMA systems. The proposed filter features a regular structure that allows for elimination of some parasitic capacitances, thus significantly improving the filtering accuracy. Due to its modularity that allows for dividing the circuit into two separate sections, the circuit can be easily reconfigured to work as either infinite impulse response (IIR) or as finite impulse (FIR) filter. One of the key components that allows for this multi-mode operation is the proposed programmable and ultra low power multiphase clock circuit. The 24-taps filter for the sampling frequency of 30 MHz dissipates power of 4.5 mW from a 1.8 V supply.

Keywords Baseband filtering · WCDMA · GSM · Switched capacitor technique (SC) · Finite impulse response (FIR) filter · Programmable filter

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1 Introduction

From third-generation (3G) cellular and ultra-wideband (UWB) to future cognitive radios, ubiquitous wireless connectivity is changing our life daily. This relentless drive towards wireless connectivity is reflected in the integration of multiple radios and wireless standards on a single silicon chip. To stay competitive and meet very demanding integration challenges designers are exploring numerous design techniques such as body biasing, digital RF architectures, high efficiency amplifiers, and advanced power management, just to name a few [1].

One research area that is relatively unexplored is signal processing partitioning among analog and digital signal processing functions of the CMOS radio. The prevailing RF transceiver architectures rely on directly converting extracted base-band signals using high resolution analog to digital converters (ADCs) so subsequent filtering can be performed using digital signal processing (DSP). We are exploring an alternative scenario where some analog signal processing is performed prior to the ADC conversion.

The issue of analog versus digital signal processing has been discussed in a literature for a number of years [2, 3]. The general conclusions stemming from that research seem to be the following: analog signal processing can be more computationally efficient for situations where signal to noise ratio (SNR) is below 60–70 dB [4, 5]. In the explored system architecture analog filtering is performed after the final RF/IF mixing operation but prior to the ADC conversion. The new system partitioning eases implementation complexity for ADC and DSP blocks. In fact, lower required ADC resolution in this case leads to significant saving in the ADC power dissipation that are larger than the power dissipation of the additional analog filtering block.

Different filtering techniques are widely described in the literature. Filters can operate in continuous or discrete time

domain and with analog or digital signals. Finite impulse response (FIR) filters offer numerous advantages such as linear phase and stability. They are typically used in filtering of discrete time signals, although they can also operate in continuous time domain using the continuous time delay lines [6].

Analog FIR filters can be implemented as switched capacitor (SC) or switched current (SI) filters. They are typically more power and chip area efficient compared to the digital implementations especially in applications that do not require a very high attenuation. Switched capacitor finite impulse response (SC FIR) filter topology is one of the most attractive techniques to realize analog filters. The advantages of SC FIR technique come from the fact that filter coefficients are not dependent on the absolute values of capacitors capacitance but only their ratios. The capacitor ratios are precisely controlled and a precision better than 0.1% is possible with careful layout.

2 Analog Base-band Filtering for WCDMA/GSM

The third-generation (3G) cellular phone systems, like wide-band CDMA (WCDMA), are being introduced to markets around the world. At the same time there is a huge installed infrastructure of the second-generation systems like GSM, some of which have been recently upgraded with extended data capability in the form of EDGE (Enhanced Data for GSM Evolution) technology. Clearly hardware that can service multiple systems is required. Integrated Circuits that can accommodate multiple standards using the smallest die area and power are in high demand.

There are two typical architectures for RF receive path [2]: IF (super heterodyne) and direct conversion. In the direct conversion architecture, shown in Fig. 1, filtering and signal amplification takes place at DC, where gain is easier to achieve with low power and the filtering can be accomplished with on-chip resistors and capacitors instead

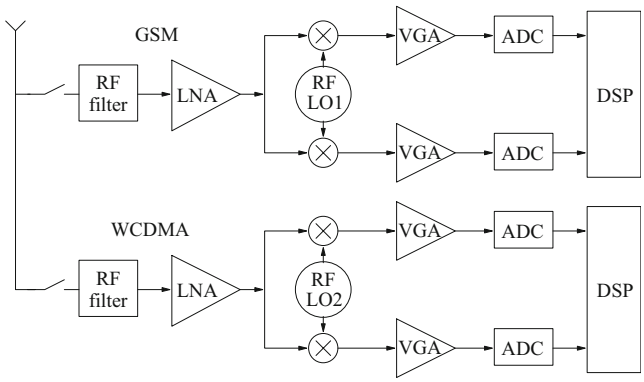


Figure 1 Traditional direct conversion architecture for GSM/WCDMA.

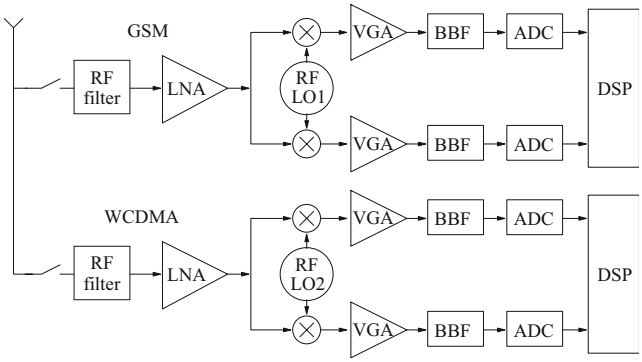


Figure 2 Direct conversion architecture for GSM/WCDMA using combined analog and digital base-band filtering.

of the expensive and bulky SAW filters. For these reasons the direct conversion architecture is gaining popularity although challenges like local oscillator (LO) leakage to the antenna present severe implementation constraints.

To service multiple standards a multiple channel receiver typically needs to contain a dedicated RF front end for each standard due to stringent noise and linearity requirements. However, base-band filtering that can be shared among various standards is feasible. Traditionally, base-band filtering is performed in a digital domain after the ADC conversion (Fig. 1). We are exploring an alternative solution, shown in Fig. 2, where the partial filtering is performed in analog domain by the additional base-band filter (BBF) [3, 4].

In the alternative solution the requirements for the analog to digital converter (ADC) are greatly reduced. As a result a simpler ADC with low resolution (6–8 bits) coupled with the analog base-band filter (BBF) can offer a competitive solution to the high resolution ADC (8–10 bits) required in the traditional digital filtering scheme. In particular, we are anticipating that the total power dissipated would be lower when using analog base-band filtering. In this paper we are presenting the analog programmable base-band filter realized using Finite Impulse Response (FIR) Switched Capacitor (SC) filter topology while the development of the low power 8-bit ADC converter is reported elsewhere [7].

GSM uses Gaussian-MSK modulation with a spectral efficiency of 1.3 bit/Hz providing bit rate of 270 kb/s using the channel bandwidth of 200 kHz. WCDMA uses quadrature-phase-shift-keying (QPSK) modulation and a spreading code that increases the signal bandwidth (variable from 8 to 384 kHz) to 3.84 MHz. At the receiver, the de-spreading process uses the same code applied in the transmitter to recover the original spectrum of the data signal. As a result of the system requirements the base-band filter 3 dB bandwidth is set at 100 kHz for GSM and at 2 MHz for WCDMA.

In multi-standard systems, base-band signals vary widely in terms of signal level and bandwidth, so reconfigurable

filters are needed. A filtering stage with variable bandwidth can be realized by varying values of capacitors, resistors, and transconductors using digital control. In literature many examples of programmable multi-mode base-band filters have been described [8], [9], and [10], propose channel select filters for dual-band applications, while [11], [12] and [13] extend the filter programmability for multiple standard applications.

This paper presents design and optimization of the finite impulse response (FIR) filters realized in switched capacitor (SC) technique for GSM/WCDMA systems that offers superior performance characteristics compared to other solutions presented in the literature.

3 SC FIR Filter Design Considerations

A general block diagram for an FIR filter is shown in Fig. 3. The filter of order N contains a delay line that stores N samples of the input signal, $x(n)$, which passing this memory structure are in following clock cycles multiplied by $N+1$ coefficients, h_i, and finally summed, thus producing the output samples, $y(n)$.

The FIR filter shown in Fig. 3 can be realized in SC technique using different architectures that differ in structure of the corresponding building blocks. The main trade-offs between architectures are: power dissipation versus sampling frequency and chip area vs. possible stopband attenuation and the power dissipation [14]. In SC FIR filters power dissipation depends on number of operational amplifiers (OAs), that differ between particular architectures, but also on the OA's structure [15–17]. For example, in the Gillingham [14] and the rotator [18] structures each delay element (T) contains one OA, which means that a total number of OAs depends on the filter order, N. On the other hand, in the parallel structure [16, 19], only one operational amplifier is used, independently on the filter order. There are also the intermediate solutions, e.g. the family of the even-odd structures [16, 14], in which particular delay elements, still containing only one OA, allow for storing of more than one sample.

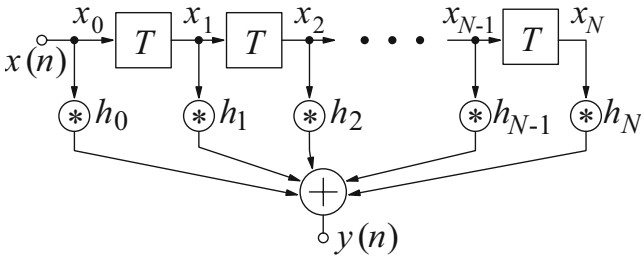


Figure 3 Block diagram of a finite impulse response (FIR) filter with three blocks: a delay line (T), filter coefficients (h_i), and a summing circuit [20]; x_i means $x(n-i)$.

The additional trade-off exists between the filter accuracy, that depends on a total number of re-writing operations of a single sample in the filter structure, and the complexity of the logic circuitry that controls the filter. Each re-writing operation of the analog signal introduces an error that accumulates at the end of the delay line, thus limiting the filtering accuracy [14]. The logic circuitry has additionally influence on both the chip area and the overall power dissipation. According to this criteria SC FIR filters can be divided into two groups.

The first group contains the Gillingham and the even–odd delay line structures, which feature a low logic (clock) complexity at the expense of limited filtering accuracy [14]. The Gillingham structure is controlled using a simple 2-phase clock but suffers from the highest number of re-writing operations between all SC FIR filters, equal in this case to $2(N+1)$. In the even–odd structures, on the other hand, number of re-writing operations is at least 3 times smaller than in the Gillingham structure but is still dependent on the filter order. The clock generator is in this case more complex than in the Gillingham structure but number of clock phases does not depend on the filter order [14]. Both these structures have been fabricated in CMOS 0.8 μm technology for the application in the GSM base-band filtering, and compared in detail in [14]. In case of the even–odd filter the measured stop-band attenuation was higher by about 17 dB than in case of the Gillingham structure, as expected.

The second group contains filters that use different types of circular analog delay lines, in which particular samples remain in fixed positions as long as they are replaced by new samples after N clock phases. To this group belong the rotator structure, the circular memory structure, proposed in this paper, and the parallel structure. In the last of these structures each filter coefficient contains many capacitors, which significantly increases the chip area making this filter suitable for small orders only [16, 19]. The common feature of all filters belonging to this group is a small number of re-writing operations, usually less than 4, which additionally does not depend on the filter order. On the other hand, these filters suffer from a very complex multiphase clock generator, in which number of clock phases increases with the filter order.

Taking into account all described criterions, particular SC FIR filters have been compared in Table 1 in terms of the power dissipation, the accuracy (number of re-writing operations per a single sample) and the chip area. The circular-memory filter proposed in this paper has been also included for comparison.

The issue that becomes important in design of SC FIR filters is a direct correlation between the chip area and the

Table 1 General performance comparison between particular groups of SC FIR filter architectures.

Structure	Power consumption (No. of OA)	Accuracy (No. of rewriting operations)	Chip area for $N>10$	Ref.
Gillingham	Large (N+1)	Small (2N+1)	Small	[14]
Even–odd	Medium (≈0.66,N+1)	Medium (≈0.66N+1)	Medium	[14]
Rotator	Large (N+2)	High (3)	Medium	[16, 18]
Parallel	Medium (1)	High (2)	Ultra large	[16, 19]
Circular	Small (N+2)	Very high (3)	Small-to-medium	[29, 20]

filter accuracy. In SC FIR filters coefficients are realized as capacitors, whose capacitance is directly proportional to these coefficients. The coefficient capacitors (CC) typically are realized as an array of small unity capacitors (UC) connected in parallel [16]. In such implementations theoretical values of the coefficients must be rounded to the nearest UC, which limits the attenuation in the stop-band of the frequency response. This problem can be solved in several ways. One of them relies on increasing the number of UCs in each CC, which allows for decreasing the rounding errors. This approach has limited usage in practice. The problem is that UCs can not be too small, because of influence of parasitic capacitances of connecting paths. In this situation increasing the number of UCs increases also the value of each CC. As CCs loads delay elements in the delay line, therefore the largest CC determines the overall power dissipation of the filter. The sum of all CCs is critical as well. Value of the capacitor that is placed in the feedback of the output OA is equal to the sum of all CCs in the filter, and when CCs are large it indirectly puts high demands on the output OA in case when high sampling frequencies are required. Due to all these constrains SC FIR filters reported in literature usually were designed with relatively small numbers of taps, for applications in which selectivity that is bellow 30 dB is sufficient, or for applications that require small sampling frequencies. In the proposed filter another method has been used [14]. The designed filter with 24 taps can work as a single structure or, if necessary, be divided into two shorter sections connected in series. The spread between coefficients in each of these sections is low (15:1), but as transmittances of both sections are multiplied one by the other, the resultant filter coefficients have larger spread, which allows for relatively large attenuations in the range up to 52–65 dB. This approach enables using larger UCs and operation with relatively high sampling frequencies.

3.1 Example Implementations of Analog FIR Filters

Example reported analog FIR filter implementations, in both the SC and the switched currents (SI) techniques, have been compared in Table 2. For meaningful comparison the following Figure of Merit (FOM) has been defined as the

Table 2 Comparison of various implementations of analog FIR filters.

Case	Ref.	Type of structure	f_S [MHz]	P [mW]	Process	No. of taps	Atten. [dB]	V_{DD} [V]	FOM [samplestaps/nJ]
#1	[19]	Parallel	80	136	0.35 µm	15 (4)	45	2.5	2.35
#2	[32]	Parallel	10	10	0.35 µm	4	35	2.8	4
#3	[21]	Parallel	72	23	90 nm	4	30	1	12.52
#4	[33]	Parallel	200	19.5	0.35 µm	4	32	3.3	41.03
#5a	[14]	even–odd	2	16	0.8 µm	32	57	3	4
#5b	[14]	Gillingham	2	19	0.8 µm	32	41	3	3.37
#6	[23]	Rotator	0.1	230	3 µm	32	35	5	0.01
#7	[24]	Rotator	200	507	0.6 µm	9	–	5	3.55
#8	[25]	Rotator	160	200	0.8 µm	5	50	5	4
#9	[22]	Rotator	170	70	1.2 µm	9	–	3.3	21.86
#10	[34]	Circular	100	5mW/tap	no data	–	–	–	20
#11	[27]	Circular	20	70	0.8 µm	15	35	5	4.29
#12	[28]	Circular	1	48	0.8 µm	4	20	3	0.08
#13	This work	Circular (WCDMA)	30	4.5	0.18 µm	24	65	1.8	102.86
#14	This work	Circular (GSM)	1	0.5	0.18 µm	24	55	1	48

sampling frequency multiplied by the number of taps per power dissipation [20] (Fig. 4):

$$\mathrm{FOM} = \frac{\mathrm{No\_of\_taps}\, f_s}{P}\,[\mathrm{samples\,taps/nj}] \quad (1)$$

This diagram shows that in general classification parallel structures offer the best FOM between previously reported analog FIR filters, but usually feature small number of taps and low attenuation. Rotator structures, on the other hand, usually reach the best FOM when comparing filters realized in the same process. Furthermore, these structures in older technologies offer comparable parameters to, for example, parallel structures realized in newer technologies [21, 22]. This is possible, as although the number of OAs in rotator structures is larger than in the parallel structures, but these OAs dissipate very low power.

The previously reported circular memory filters offer worse parameters than rotator structures. The main reason of this is large power dissipated in the logic circuitry due to rotation of multi-bit coefficients in the ring memory structure. Number of memory cells that are switched over after calculation each output sample is equal to 2 $n(N+1)$, in which n is the number of bits in each of CCs. Factor '2' is necessary as each bit requires two cells to enable fast parallel reprogramming of all CCs in a single clock step. Our proposed circular-memory SC FIR filter due to special circuit solutions offers better FOM attaining better general performance [20]. Although the number of memory cells in described solution is large i.e. 240 for 24 taps and 5-bits per each CC, the power efficient logic circuitry has been used that allows for significant power saving.

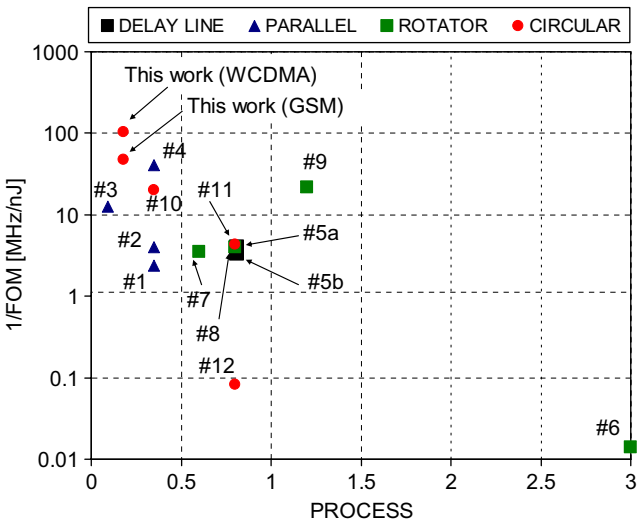


Figure 4 Performance comparison between different analog FIR filters listed in Table 2 as a function of process.

4 The Proposed Circular Memory SC FIR Filter Structure

4.1 Circular Memory vs. Rotator Structure

The SC FIR rotator structure has been initially proposed by Tsividis [18] and then implemented several times in different technologies [22–25]. The circular memory FIR filters so far were implemented only in SI technique, which in comparison to SC technique offers smaller accuracy [26]. For example, the SI FIR circular memory filters described in [27] and [28] allow for attenuation that is equal to 35 and 20 dB only. In this paper we propose the circular memory filter implemented in the SC technique as this approach takes advantage from the circular memory approach, which is kind of rotating structure, while simultaneously offering a better performance.

The rotator and the proposed circular memory SC FIR filters, shown in Fig. 5, use an equal analog circular delay line. The signal samples stored in particular cells of this block are copied to an array of programmable CCs, which in each of these structures is controlled using other logic circuit. In the rotator structure each filter coefficient remains in the same CC whole the time, while a delaying effect is realized using a rotator switch, which in different clock phases connects particular delay elements to different CCs [18]. In the circular memory structure the rotator switch has been removed and each delay element is permanently connected to only one CC. In this approach filter coefficients are cyclically moved between CCs, thus realizing the delaying effect.

The rotator switch introduces a number of connecting paths between the delay line and the summing circuit, which is equal to the square of the number of the filter taps i.e. to $(N+1)^2$. In the circular memory structure, on the other hand, number of such connections has been significantly reduced and is now equal to the number of the filter taps only i.e. to $(N+1)$. For example, in designed filter this means 24 connections only in comparison to 576 in rotator structure. This is one of the main advantages of proposed filter, which simplifies the circuit structure and allows for significant saving of the chip area, which for filter with 24 taps is equal to about 40% of total filter area.

The rotator switch is the source of other concerns. One of the problems is that particular connections cross each other, which results in many extra parasitic capacitances affecting the performance of the filter [14]. Another problem is that particular connections are of different length. The resistance of paths is in this case of less importance, as SC filters work in the voltage mode and the resistance has only influence on time constants of charging the CCs. The more important are different values of parasitic capacitances of connecting paths, which are source

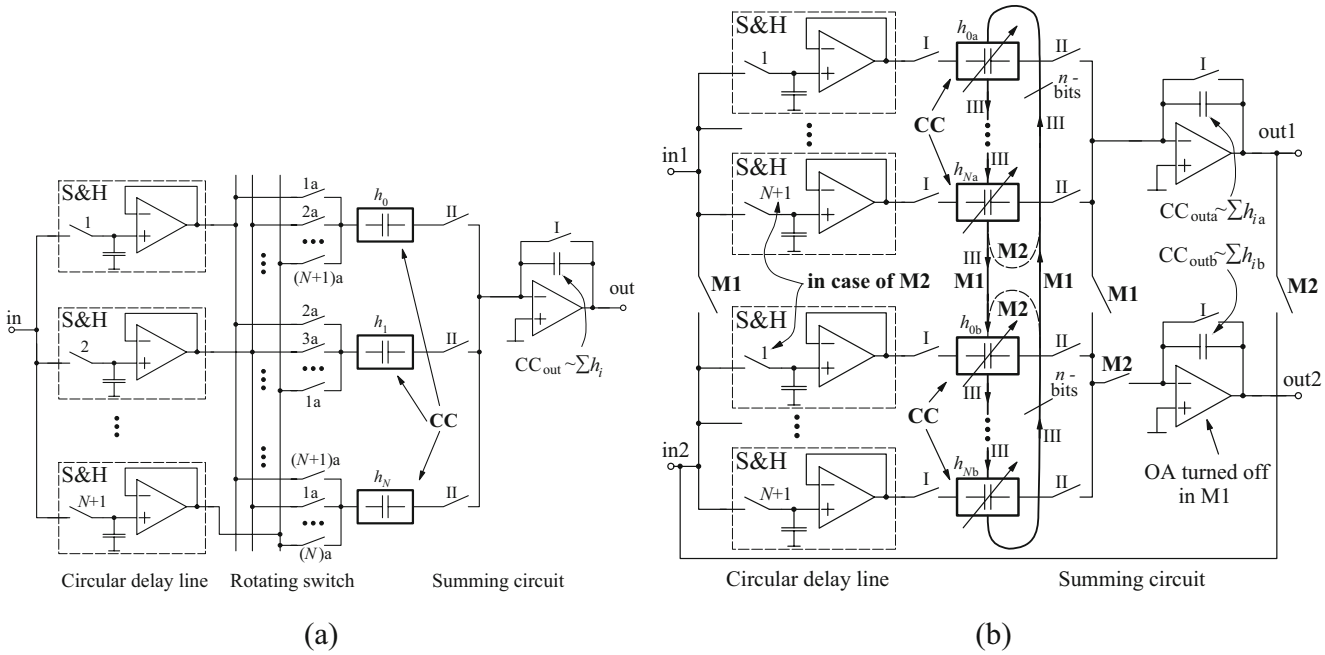


Figure 5 Simplified electrical diagram of the SC FIR: **a** rotator structure and **b** programmable 2-stages circular memory structure [20].

of different charge injection errors in each of CCs that diminishes the accuracy of the filter.

One of the disadvantages of the rotator structure is also a more complex clock generator, as half of all clock phases are used to control the rotator switch. The clock signals for the rotator and the circular memory filters are shown in Fig. 6. The number of clock phases in the rotator structure is about four times higher than the number of filter taps, whereas in circular memory filter the number of clock phases is only two times higher than number of filter taps [29]. For circular memory FIR filter with 24 taps this means elimination of 48 clock phases which simplifies the clock circuit and allows for elimination of many signal paths and saving of the chip area.

Taking into account all described aspects, the circular memory filter structure is more suitable for longer filters and therefore has been chosen for implementation of the base-band WCDMA/GSM filter.

4.2 Implementation of Programmable Filter Coefficients

Filter coefficients in the proposed filter are realized as multi-segment capacitors programmed using the n-bits words, as shown in Fig. 7. The absolute value of the coefficient is programmed using n-1 LSBs, while the n'th bit (MSB) controls the sign of the coefficient using the circuit shown in Fig. 7b. For an example case of n=5 filter coefficients can be programmed in the range between −15 and 15.

One of the problems related to implementation of the positive and the negative coefficients is that the positive coefficient, shown in Fig. 7a, is a parasitic sensitive structure [30]. This effect is especially important in CMOS technologies, e.g. AMS, in which poly-poly capacitors are using and the top plate parasitic capacitance can have a value as high as 10–15% of the capacitor value. The parasitic capacitances must be carefully compensated otherwise the precision of the filter is diminished. The attractiveness of SC FIR filters increases when implemented in the technologies, in which metal-to-metal (MiM) capacitors are available. Such capacitors feature relatively small top plate parasitic capacitances to the substrate, which in the CMOS TSMC 0.18 μm technology are equal to 1% of the capacitors values.

The proposed programmable filter features an additional technique that minimizes the effect of the top plate parasitic capacitances. The compensation techniques that may be found in literature [16, 30] are useful when capacitors have constant values e.g. in nonprogrammable filters. In this case

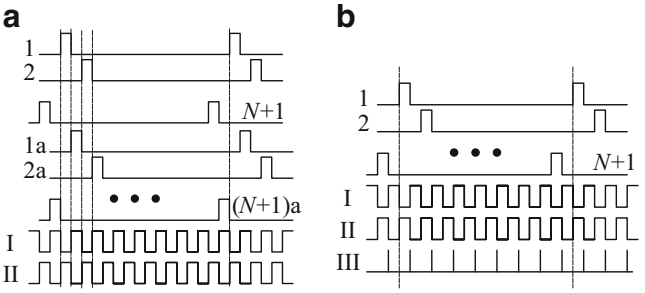


Figure 6 Illustrative clock diagram for the filter of second order N=2 for **a** the rotator structure and **b** the circular memory structure [29].

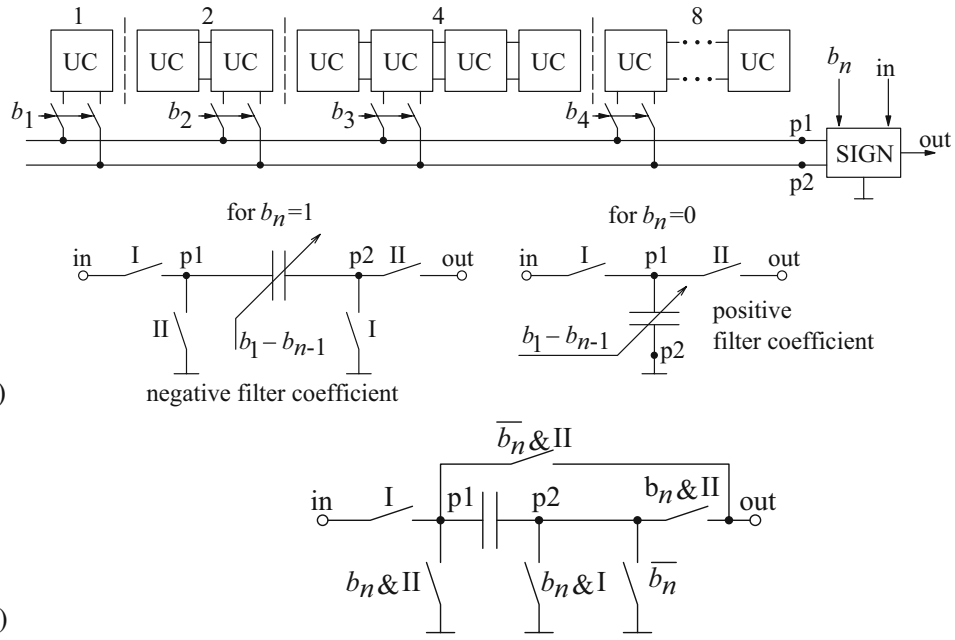


Figure 7 The scheme of the programmable CC: **a** The general structure, in which bits b_1–b_{n-1} turn on particular CCs' sections, **b** the circuit that controls sign of the coefficient [29].

compensation must be done before the filter is manufactured. In programmable structures this effect becomes insignificant as frequency response of the filter is in this case designed after the chip has been manufactured. In this situation it is possible to take the influence of parasitic capacitances into consideration and design coefficients in the proper way. For example, assuming the top plate parasitic capacitance introduces an error of 10%, the positive coefficients should be designed in such a way to have values that are equal to about 90% of desired theoretical values—parasitic capacitances increase values of the coefficients. If the measurement tests prove the assumption of 10% is incorrect, the coefficients can be redesigned and reprogrammed in the structure for other error values. After several iterations the real error values can be found, which can be then used as some correction factors.

The important is that values of designed coefficients are constant when the filter is working. The only things which do change are places of particular coefficients in the array of CCs, which have exactly the same structure, so this does not affect the filter performance.

5 Application of our Proposed Circular Memory Filter in Base-band GSM/WCDMA Filtering

The proposed circular-memory FIR filter with 24-taps has been used in application of a programmable base-band filter suitable for both the WCDMA and the GSM standards. To minimize the spread between the CCs our filter has been divided into two sections, 11th order (12 taps) each, connected in series (mode M2 in Fig. 5b).

Specification of the WCDMA baseband filter is shown in Fig. 8 (curve A). It is worth noting that the similar specification has the baseband filter used in the GSM standard, but in this case all frequencies must be scaled down 20 times. In case of not divided structure (mode M1) to satisfy this specification, the example filter coefficients after rounding have the following values:

$$h_i = \left\{ \begin{array}{l} \mathbf{1},\ 4,\ 6,\ -3,\ -32,\ -73,\ -91,\ -37,\ 114,\ 331,\ 527,\ \mathbf{606}, \\ 527,\ 331,\ 114,\ -37,\ -91,\ -73,\ -32,\ -3,\ 6,\ 4,\ \mathbf{1},\ 0 \end{array} \right\}, for\ i = 0, ..., 23 \quad (2)$$

The resultant frequency response is in this case shown in Fig. 8 (curve B). This filter is difficult to implement owing to the large spread between coefficients that exceeds 600.

When the filter is divided into sections, the spread between CCs does not exceed 15 and CCs may be programmed using 5 bits only. The filter coefficients in both sections are listed in Table 3. The CCs are small enough to allow for relatively high sampling frequencies and for low power dissipation. This technique allows for significant reduction of the chip area, which is equal to about 90% for the array of CCs and 80% for entire filter.

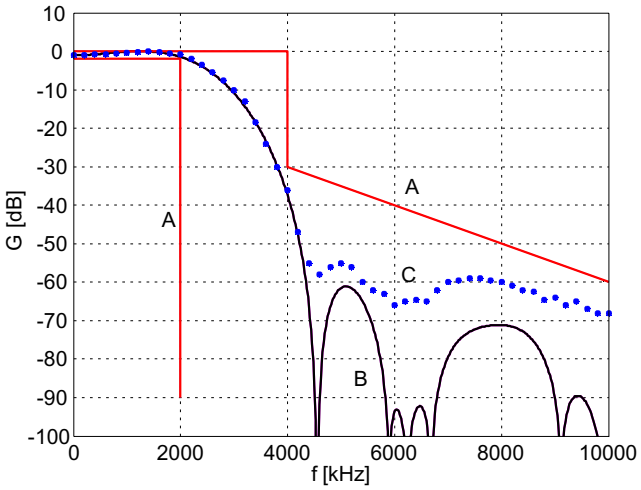


Figure 8 Implementation of the WCDMA base-band filter: *A* filter specification, *B* theoretical frequency response, *C* simulated frequency response. Sampling frequency is equal to 20 MHz in this case [20].

This filter has been implemented in TSMC CMOS 0.18 µm standard process and verified in HSPICE simulations. One of advantages of SC FIR filters that is very useful in this application is that the output signal is already sampled and has constant values within the period that is equal to the half of the sampling period ($1/f_S$), as illustrated in Fig. 9. Such signal can be used directly by subsequent ADC without additional sample and hold element. The example output signals illustrated in Fig. 9 are for the sampling frequency of 20 MHz and the input signal frequency equal to 300 kHz (passband) and to 6250 kHz (stopband) respectively, for small values of the input signal. Designed filter operates correctly also for sampling frequencies up to 30 MHz.

The simulated frequency response of designed filter is shown in Fig. 8 (curve C) for WCDMA standard. The presented results are for 1.8 V supply. The attained

Table 3 Implementation of the baseband GSM/WCDMA filter in programmable circular memory filter.

Section 1	Section 1—binary	Section 2	Section 2—binary
−1	1000**1**	−1	1000**1**
−2	1001**0**	−2	1001**0**
−1	**1**000**1**	−1	**1**000**1**
4	00**1**00	3	0001**1**
10	0**1**0**1**0	9	0**1**00**1**
15	0**1**1**1**1	13	0**1**1**0**1
15	0**1**1**1**1	13	0**1**1**0**1
10	0**1**0**1**0	9	0**1**00**1**
4	00**1**00	3	0001**1**
−1	**1**000**1**	−1	**1**000**1**
−2	1001**0**	−2	1001**0**
−1	1000**1**	−1	1000**1**

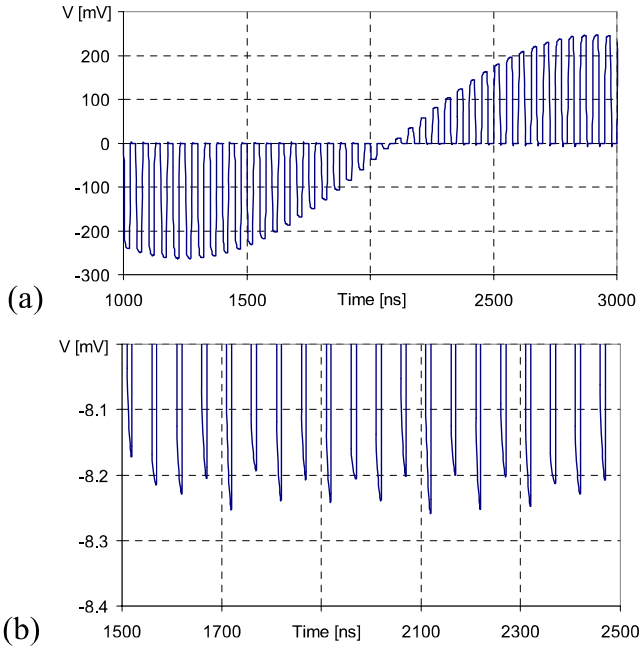


Figure 9 Filter output signal in the WCDMA mode for: **a** passband—f_S=20 MHz, f_{IN}=300 kHz, **b** stopband—f_S=20 MHz, f_{IN}=6250 kHz.

attenuation in the stopband is smaller than theoretical (curve B) due to different nonidealities, but filter still meets the required specification with sufficient margin of at least 10 dB.

The advantage of proposed solution is that the frequency response is easily scalable by adjustment of the sampling frequency only. This feature is not available e.g. in active RC filters, as scaling of the cut-off frequency requires in this case changing the values of the capacitors. The proposed filter in both the GSM and the WCDMA standards uses exactly the same coefficients and reprogramming is in this case not required. In the WCDMA mode f_S is equal to 20 MHz, while in the GSM mode f_S is scaled down to 1 MHz.

The proposed filter is also very flexible in terms of the power dissipation. In case when the filter operates with low sampling frequencies, the power dissipation can be reduced by decreasing the supply voltage, as shown in Fig. 10 for selected values of f_S. The best FOM has been reached for medium supply voltages but the energy varies only moderately in entire range.

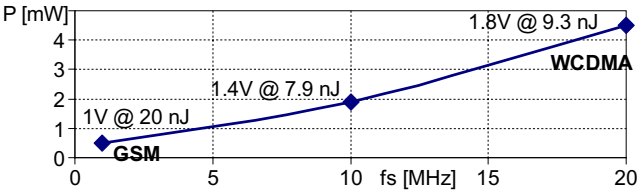


Figure 10 Power dissipation vs. sampling frequency in proposed filter.

6 Power Efficient Digital Memory and Clock Generator Used in Our Proposed SC FIR Circular Memory Filter

One of the encountered implementation problems was large power dissipation in the control logic circuitry when this block was realized using D-flip flops (DFF). To enable low power operation a simpler and more power efficient memory block, shown in Fig. 11, has been proposed. This memory has been realized using gate-to-source parasitic capacitances in NOT gates, which are connected as a ring. Number of such rings in the filter is equal to the resolution of the CC, i.e. 5 in designed filter, plus one additional ring that serves as a clock generator [20]. The advantage of this solution results from the fact that the CMOS NOT gate dissipates much smaller power than the DFF, only when switching between two logical states, while a DFF dissipates power even when the input logical value does not change.

The filter contains additionally the off-line memory realized as 25 blocks, each containing 6 DFFs. This memory is programmed sequentially using external signals. During this operation particular blocks are addressed using 5 addressing lines and programmed using 6 data lines. After this operation is finished the ring memory is programmed in one step using the PROG signal. To program the frequency response of the filter only 24 blocks are required. The 25th block is used for different control signals.

To illustrate this operation, let us consider, for example, the frequency response of the first section of designed baseband filter. The second column in Table 3 contains the binary representation of the filter coefficients. Each memory ring after programming contains bits from a given position in the coefficients. For example, the first ring contains all LSBs i.e. {101001100101}, while the 5th ring contains all the MSBs i.e. {111000000111}. When particular bits change their positions during the filter operation only several NOT gates change the logical state. For example, in the 5th ring only two NOT gates change the state and dissipate power i.e. between the 00…0 and the 11..1 sequences. As a result, the total power dissipated in this memory block is proportional to the number of places (marked using the bold font), in which bits change their values, not to the total number of elements. In both sections of our filter this is only 42 places comparing to the total number of 240 memory cells. This means a reduction of the power dissipation in the digital block by about 80–90%, which is now equal to only 100 μW for the sampling frequency of 20 MHz.

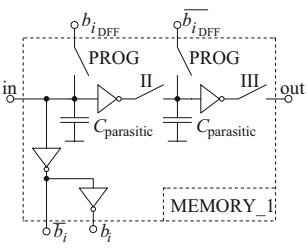
6.1 Programmable Clock Generator

The programmable clock generator is realized using one additional memory ring, programmed in the same way as the memory block described above. This clock can easily be programmed to perform for example one 24 phase clock generator or two independent generators, each with 12 phases. Theoretically it is also possible to obtain other patterns e.g. four independent generators, each containing 6 phases, but this mode is not using in the proposed filter. In the first case, i.e. for 24 phases, only 1 bit in the ring is equal to 1 {100000000000000000000000}, whereas in the second case 2 bits are equal to 1 {100000000000100000000000}. In case of four clock generators the bit sequence would be: {100000100000100000100000}. In the second case the clock simple divides the filter into two independent blocks (with equal length) that can be used in different ways as described in the next section. This clock generator consumes very low power, which is equal to power dissipation of couple NOT gates only.

7 Different Configurations of the Proposed Circular Memory Filter

Due to very regular structure the proposed filter can be easily reconfigured in different ways, in order to address various applications. In this section we present several possible configurations.

Both sections of the designed filter can be used as independent filters, for example, as a programmable quadrature mirror filter bank (QMF). Such filter bank consists of two filters, i.e. the low-pass filter with the transfer function G, and the high-pass filter whose transfer function H is the quadrature mirror image of G with respect to the normalized frequency equal to $\pi/2$. The filter bank can be used, for example, in multistage discrete wavelet transform (DWT) [31].



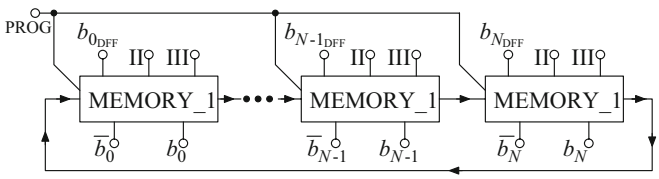


Figure 11 Ring digital memory, controlled by a 2-phases clock generator (II, III) used in proposed circular memory SC FIR filter structure [20].

Another way of utilizing the filter is to connect both sections in series. This connectivity allows for increasing the effective spread between filter coefficients without enlarging the chip area. This mode has been used in described WCDMA/GSM baseband filtration.

In yet another example, illustrated in Fig. 12, both sections have been used to realize the infinite impulse response (IIR) filter. In this case one section is using as the nominator while the second one as the denominator of the transfer function of the IIR filter. The main advantage of IIR filters is that they allow for obtaining parameters similar to those of FIR filters but using the smaller number of the filter taps.

The proposed filter in the IIR mode operates as follows: The clock phase "II" overlaps phases 1, 2, 3,…, N+1, as shown in Fig. 6b. In these phases the input samples are written to the delay line of the first section. At the same time the output samples occur at the output of the first section (out1) and are immediately stored in the delay line of the second section. In this way the output samples (out1) are sums of the filter input samples (in1) multiplied by coefficients $h_{i\mathrm{a}}$ as well as previously calculated output samples (in2) multiplied by coefficients $h_{i\mathrm{b}}$. The proposed filter working in the IIR configuration is shown in Fig. 12 and can be described using the following differential equation:

$$\begin{aligned} y(n) = {} & x(n)h_{0\mathrm{a}} + x(n-1)h_{1\mathrm{a}} + \ldots + x(n-N)h_{N\mathrm{a}} \\ & + y(n-1)h_{0\mathrm{b}} + y(n-2)h_{1\mathrm{b}} + \ldots \\ & + y(n-N-1)h_{N\mathrm{b}} \end{aligned} \tag{3}$$

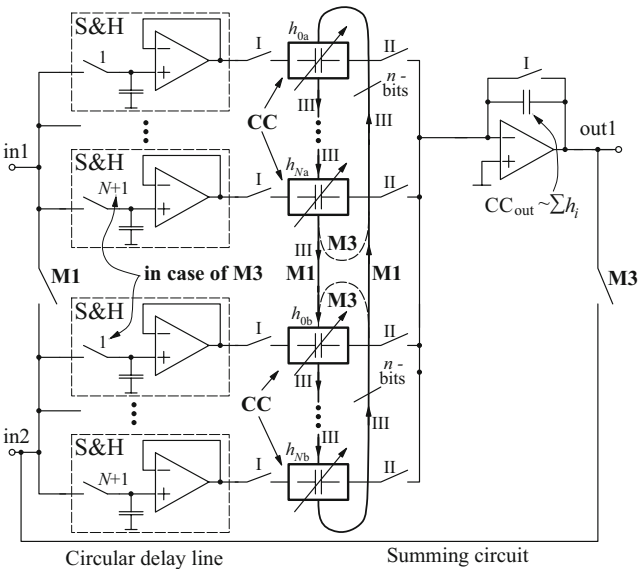


Figure 12 Proposed circular memory structure used as an infinite impulse response (IIR) filter (switches m2 are closed and m1 are opened) [35].

Table 4 Summary of the proposed SC FIR filter's performance.

Parameter	WCDMA	GSM
Voltage supply	1.8 V	1 V
Sampling rate	20 MHz	1 MHz
Passband (3 dB)	2 MHz	100 kHz
Power dissipation	4.5 mW	500 μW
Energy per sample	9 nJ	20 nJ
Attenuation (HSPICE)	65 dB	52 dB
Process	TSMC CMOS 0.18 μm	
Die area	540×330 μm (1.78 mm^2)	
Number of filter taps	24	

Resultant filter transmittance H(z) that is the transmittance of the IIR filter is therefore given as:

$$H(z) = \frac{h_{0\mathrm{a}} + h_{1\mathrm{a}}z^{-1} + \ldots + h_{N\mathrm{a}}z^{-N}}{1 - (h_{0\mathrm{b}}z^{-1} + h_{1\mathrm{b}}z^{-2} + \ldots + h_{N\mathrm{b}}z^{-N-1})} \tag{4}$$

8 Conclusions

A new analog SC FIR filter with circular memory has been implemented in CMOS 0.18 μm technology. The new structure is a significantly modified SC FIR rotator filter described theoretically in [16, 18] and designed earlier by authors in CMOS 0.35 μm technology [29].

The proposed filter features several advantages in comparison to other SC FIR filters: substantial reduction of the chip area (by about 50%), simplification of the clock generator (number of clock phases reduced by half), and increased precision. The increase in filter precision is possible due to small number of re-writing operations and due to elimination of substantial number of parasitic capacitances. In the designed filter with 24-taps the number of the critical parasitic capacitances in the analog part has been reduced by almost 600. As a result the attenuation in the stop-band of the frequency response is larger by about 15 dB.

The proposed filter can operate in different modes, which increases the area of potential applications of this circuit. It can work in the 'one-section' or in the 'two-sections' modes. In the second case both sections can be used separately e.g. in the filter bank, or as the IIR filter or can be connected in series, which enables increasing the attenuation in the stop-band of the frequency response in comparison to the 'one-section' mode.

The proposed filter has a programmable structure. In described implementation the coefficient capacitors (CC) can be programmed in the range between −15 and 15. Value of the unity capacitor (UC) used in CCs has been determined experimentally and values of 30 fF have been

used. For the sampling frequency equal to 20 MHz (WCDMA mode) the filter dissipates 4.5 mW from 1.8 V voltage supply. Adjusting this voltage in the range between 1 and 1.8 V allows for controlling the power dissipation and the maximum sampling frequency. For an example supply voltage of 1 V the maximum sampling frequency is equal to 1 MHz, which is sufficient e.g. in the GSM mode. In this case the filter dissipates power of 500 μW (Table 4).

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