Appl Phys A (2010) 100: 287–296
DOI 10.1007/s00339-010-5802-1

Applied Physics A
Materials Science & Processing

Growth study of indium-catalyzed silicon nanowires by plasma enhanced chemical vapor deposition

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Received: 19 February 2010 / Accepted: 26 May 2010 / Published online: 11 June 2010

Abstract Indium was used as a catalyst for the synthesis of silicon nanowires in a plasma enhanced chemical vapor deposition reactor. In order to foster the catalytic activity of indium, the indium droplets had to be exposed to a hydrogen plasma prior to nanowire growth in a silane plasma. The structure of the nanowires was investigated as a function of the growth conditions by electron microscopy and Raman spectroscopy. The nanowires were found to crystallize along the <111>, <112> or <001> growth direction. When growing on the <112> and <111> directions, they revealed a similar crystal quality and the presence of a high density of twins along the {111} planes. The high density and periodicity of these twins lead to the formation of hexagonal domains inside the cubic structure. The corresponding Raman signature was found to be a peak at 495 cm^{-1}, in agreement with previous studies. Finally, electron energy loss spectroscopy indicates an occasional migration of indium during growth.

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1 Introduction

Nanotechnology and nanowires (NWs) have attracted great interest in the last decade, as they provide the ideal frame to study one-dimensional phenomena and to fabricate novel and/or better performing devices [1–7]. Among all the materials synthesized in the form of nanowires, semiconductors such as silicon have attracted attention due to their potential role in significantly improving the performance of electronic devices [8, 9]. Additionally, silicon nanowires with very small diameters, less than 5 nm, are expected to have a direct band gap, which would enable silicon to participate in devices as optical emitters [10, 11].

To date, the most successful method to fabricate nanowires has been the vapor–liquid–solid (VLS) method, in which a metal catalyst locally assists the decomposition of the growth precursors and thereby drives the nucleation and growth of the nanowires. This method enables the control of the nanowire diameter and position as they are governed by the size and location of the catalyst drops [12–14]. In the last few years, a good understanding of the growth mechanisms has been achieved [15–18]. The most commonly used catalyst has been gold. However, when incorporated in the lattice, gold introduces deep-level traps that significantly alter the electronic and optical properties of a semiconductor [19, 20]. It is for this reason that alternative metals to gold have been investigated for the synthesis of semiconductor

nanowires [21–30]. There are three main types of alternative catalysts, depending on: (i) if they form a eutectic with a high concentration of silicon (>10%), (ii) if they form a eutectic with nearly zero concentration of silicon or (iii) if growth proceeds through the formation of a silicide. A review of the differences in the growth mechanisms can be found in the work by Schmidt et al. [21]. Indium belongs to the second type, which implies a more challenging growth process. For the synthesis of silicon nanowires, the use of indium has certain advantages: (i) the low temperature of the Si–In eutectic and (ii) the shallow ionization energy of indium incorporated in a silicon lattice, so that it acts as a p-type dopant if it becomes incorporated in the nanowire during growth. In recent years, there has been some controversy with respect of gold's capability or not to incorporate in the nanowire crystal lattice [31–36]. However, some studies have shown that the use of an alternative catalyst can improve the optical and electronic properties of silicon nanowires. Indeed, photoluminescence (PL) was only obtained when gold was not used as a catalyst [37]. Other studies indicate that PL is only obtained after etching the gold and annealing the nanowires under oxygen ambient for a controlled oxidation [38].

In this work, we present a detailed study of the conditions leading to the growth of silicon nanowires by using indium as a catalyst. After presenting the experimental methods in Sect. 2, the structural analysis by high resolution transmission electron microscopy (HRTEM) and micro Raman spectroscopy are shown in Sect. 3. The results will be discussed in Sect. 4. Finally, a conclusion will be given in Sect. 5.

2 Experimental details

The silicon nanowires were obtained in a plasma enhanced chemical vapor deposition (PECVD) system. The PECVD chamber is a vertical cold wall reactor, consisting of an evacuated stainless steel vessel, in which the plasma is generated by two heated electrodes, whose temperatures can be chosen independently. The samples are placed on the bottom electrode. The process gases available were SiH_4 and H_2, whose fluxes were controlled by two mass-flow controllers, with maximum flow capacities of 10 and 200 sccm, respectively. A butterfly valve between the reactor chamber and the pumping system enables the control of the pressure in the growth chamber in an independent manner.

The substrates were (001)-oriented silicon or thermally oxidized (001) silicon wafers (with one-micron-thick SiO_2). For simplicity, in the following we will refer to these as Si and SiO_2 substrates. The wafers were cleaned by rinsing in acetone for 10 min, followed by methanol for 10 min and then cleaved. In order to remove the native oxide and to obtain a hydrogen-terminated surface, prior to indium deposition, the p-type Si <001> was etched with a 10:1 buffered 40% HF solution for 10 min and then flushed by nitrogen. The p-type Si <100> coated with 1000 nm of thermal oxide was dipped for 3 s in undiluted buffered 40% HF, in order to ensure a clean surface, and then flushed by nitrogen. The indium thin films of thicknesses 2, 5 and 10 nm were deposited by electron-beam evaporation from a 99.99% purity source.

In order to ensure a reducing environment, the whole growth process was performed in hydrogen ambient, under a flow of 100 sccm at a pressure of 1.0 Torr. Low plasma power conditions were used, in order to avoid ion bombardment [39]. Before starting the synthesis process, the substrate temperature was increased to 400°C under a 5-W hydrogen plasma. This treatment reduces the oxidized surface of the indium and allows the formation of droplets, which are catalytically active for the SiH_4 molecules and related ions and radicals produced by the plasma (i.e. SiH_3). Once the substrate has been treated, the plasma is briefly switched off to enable the introduction of 5 sccm SiH_4 and let the substrate reach the growth temperature without non-catalytic decomposition of the precursor gas. In these conditions, the silane partial pressure lies between 0.12 and 0.14 Torr. Once the growth temperature is reached, the low plasma power conditions are again activated, with a power of 3 W. We observed that the existence of the plasma was necessary for the growth of nanowires [26]. In this study, the growth temperature and the growth time have been varied between 500 and 600°C and 1 and 30 min, respectively. The temperature of the RF electrode was kept at 380°C for all growth processes.

The samples' surface morphology after the annealing process was investigated by atomic force microscopy (AFM). The morphology and the structure of the grown nanowires were investigated by scanning electron microscopy (SEM), transmission electron microscopy (TEM), scanning transmission electron microscopy (STEM) in high angular annular dark field (HAADF) or Z-contrast mode and Raman spectroscopy. The localized chemical analysis at nanoscale was studied by electron energy loss spectroscopy (EELS).

Raman spectroscopy was performed at room temperature, using a 50× microscope objective in backscattering geometry. The excitation wavelength was the 514.5-nm line of an Ar^+ laser. The calibrated incident power on the sample was always 0.5 mW (corresponding to a power density of 58 kW/cm^2). The scattered light was collected by an XY Raman Dilor triple spectrometer with a multichannel charge coupled device detector.

3 Results

The use of indium as a catalyst for the VLS growth of group-IV nanowires is challenging because of: (i) the relatively fast

oxidation of indium to indium oxide, which inhibits the capability of indium as a catalyst and (ii) the low solubility of the group-IV elements in liquid indium. Recently, germanium nanowires were obtained [27]. The nanowires were obtained by CVD without the use of a hydrogen plasma. In particular, it was demonstrated that annealing at relatively high temperature (600°C) and hydrogen pressure (30 Torr) was a necessary condition for the nucleation of nanowires. Indeed, molecular hydrogen decomposes preferentially at high pressures and temperatures [40]. This means that such a treatment could reduce the indium oxide to indium, thereby enabling its catalytic activity. Germanium nanowires were also obtained at relatively high pressures, which guaranteed that the indium was not re-oxidized during the synthesis process. We have realized similar studies for the CVD growth of silicon nanowires with indium as catalyst. We explored numerous annealing and growth conditions, from 500 to 700°C, and gas pressures between 0.75 and 350 Torr. The nucleation of silicon nanostructures/wires could be observed sporadically in some edges of the substrate and never homogeneously on the whole surface. We believe that this results from a combination of the slow catalytic activity of indium in decomposing silane (which may be slower than in the case of germane) and the lower solubility of silicon in indium, in comparison to germanium.

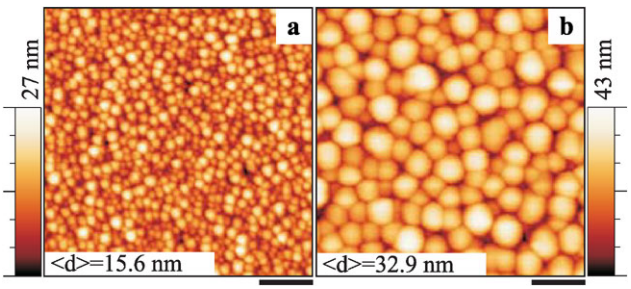

Fig. 1 AFM measurements (500 × 500 nm^2) of the sample surfaces after the annealing process, performed in hydrogen plasma from room temperature up to 400°C. On a Si <100> substrate coated with 1000 nm of thermal oxide were deposited 2 nm of indium (**a**) and 10 nm of indium (**b**). Scale bars are 100 nm

3.1 Nucleation

It is widely accepted that the size and dispersion of the catalyst on the substrate at the initial stages of growth define the nucleation of the nanowires [41, 42]. We have thus investigated the sample surface prior to growth, after the annealing process involving the exposure to hydrogen plasma at 400°C. AFM images of the samples with 2 and 10 nm of indium on SiO_2 substrates are presented in Fig. 1. Several AFM scans performed on different positions on each sample confirmed the surface homogeneity. From the measurements, the droplet size distribution was calculated. As can be deduced from Fig. 1, the sample surfaces are covered by homogeneously distributed indium droplets. The droplet size increases with the thickness of the indium layer deposited from 15.6 ± 9.9 nm to 32.9 ± 16.8 nm, for respectively 2- and 10-nm indium thicknesses. The relatively large dispersion in the droplet size can be explained by a weak coarsening effect. Here we would like to point out that similar studies realized on gallium thin films did not show the same tendency. In that case, the droplet size decreased with increasing gallium thickness, and the average diameter was in all cases larger than 19.0 ± 1.0 nm.

The nucleation and initial stages of growth of the nanowires were investigated by monitoring the morphology as a function of time. For that, growths at 600°C with different durations were realized under identical conditions. The growth times were 1, 5, 15 and 30 min. Scanning electron micrographs of the samples are shown in Fig. 2a–d, while the evolution of the nanowire length is presented in Fig. 2e.

As shown in Fig. 2a, the growth of the nanowires has started after 1 min of plasma, pointing to a relatively short incubation time [43]. The nanowire lengths are about 131.8 ± 22.9 nm and 151.8 ± 24.3 nm, for indium layers of 2 nm and 5 nm, respectively. For substrates with 10 nm

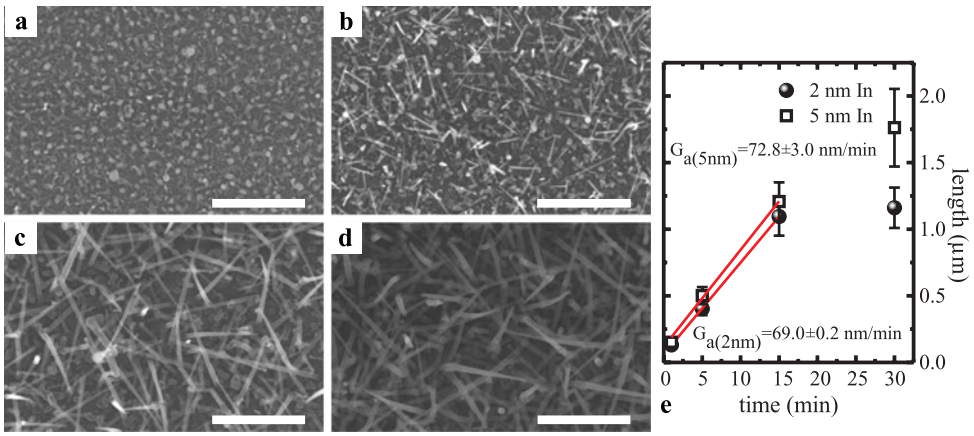

Fig. 2 Top-view SEM images of indium-catalyzed silicon nanowires grown at 600°C for 1 min (**a**), 5 min (**b**), 15 min (**c**) and 30 min (**d**). A 5-nm-thick indium layer was deposited on a Si <001> substrate. The growth rates calculated for silicon nanowires catalyzed by 2 nm (*black spheres*) and 5 nm (*open squares*) of indium are presented in (**e**), where the average length of the nanowires is plotted as a function of time, and the *red lines* are the linear fits. Scale bars: 1 μm

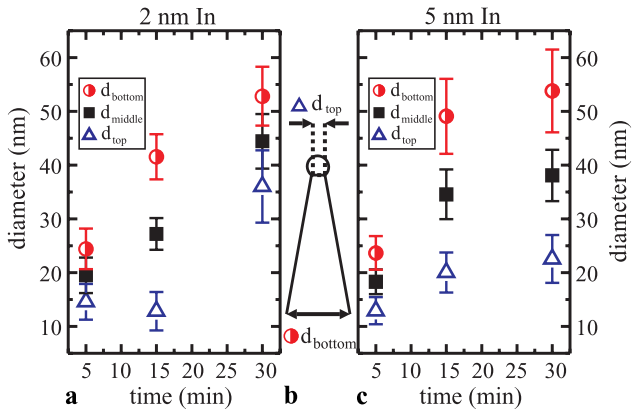

Fig. 3 (**a**) Dependence on the growth time of the top and the bottom diameters, depicted as *open triangles* and *half-filled circles*, for growth with 2 nm of indium. The middle diameter, defined as the average of the previous two, is also shown as *filled squares*. (**b**) Sketch of a tapered nanowire, where the top and bottom diameters are defined. (**c**) The same dependence as in (**a**) for growth with 5 nm of indium. The increase in the diameter at the top of the wire at 30 min in the case of the 2-nm In layer is due to the change from conical to cylindrical shape of the wire (see the text)

of indium we found that very few nanowires nucleated after 1 min of growth, making a reliable statistic difficult. This is a straightforward consequence of the dependence of the incubation time on the droplet size [43]. At longer growth times, the length of the nanowires increases at a constant rate. However, the dispersion in the nanowire length increases with the growth time. In Fig. 2e the length, as averaged between 60 nanowires, is plotted as a function of the growth time. By fitting the average length as a function of time at $T_{\text{growth}} = 600°\text{C}$, we find growth rates of 69.0 ± 0.2 nm/min and 72.8 ± 3.0 nm/min for growths realized respectively with 2 and 5 nm of In—the growth rate has been estimated by fitting the data up to 15 min. As shown in Fig. 2e, for growth realized with 2 nm of indium, the growth rate of the nanowires does not remain constant; the length of the nanowires saturates at a growth time of about 30 min. This phenomenon has already been observed and reported in the past [44, 45] and it has been attributed to the presence of a temperature gradient in the growth chamber, due to its geometry. Indeed, in our case the chamber is not heated homogeneously as may be the case in standard chemical vapor deposition systems—which are usually tube furnaces. The sample is heated directly from the sample holder. This means that, as soon as nanowires start to stick out of the substrate, a temperature gradient may appear, and the catalyst temperature decreases. As the decomposition of the silane at the catalyst surface might be temperature activated, the decomposition rate might decrease as the catalyst temperature decreases. A second reason which could explain the saturation in the growth rate could be the consumption or the evaporation of the catalyst droplet. In order to clarify this, a statistical analysis of the evolution of the nanowire morphology has been carried out. This is presented in Fig. 3. The nanowire diameter has been measured in two different positions: at the interface between the nanowire and the catalyst droplets (for simplicity denominated as *top diameter,* d_{top}) and at the interface between the nanowire and the substrate (*bottom diameter,* d_{bottom}). For further clarity, the schematic drawing of a tapered nanowire and the nomenclature is schematically shown in Fig. 3b. Each point in Fig. 3a corresponds to the average diameter of 20 nanowires grown at 600°C from 2-nm-thick indium layers. The average top diameter after 5 min of growth is 14.6 ± 3.3 nm, which corresponds well with the droplet size after the annealing. The average bottom diameter is larger: 24.4 ± 3.8 nm. Nanowires grown for 15 min exhibit the same average top diameter, while the bottom diameter has increased to 41.6 nm. This suggests that tapering increases with time, but not at the expense of the droplet consumption. Nanowires grown for 30 min seem to exhibit larger top and bottom diameters, respectively 36.0 ± 6.7 nm and 52.8 ± 5.5 nm. Here it is worth noting that we observe a sharp decrease in the growth rate by 30 min of growth. This leads to a second effect, namely a reduction in the tapering of the nanowires; in other words, the nanowire geometry evolves from cylindrical. The tapering factor, defined as $k = (d_{\text{bottom}} - d_{\text{top}})/L$, where L is the nanowire length, decreases by 50% for growth times between 5 min and 30 min. This analysis definitely proves that the tapering of the nanowires is caused by side-wall deposition. For comparison, nanowires grown from 5 nm of indium present a weaker decrease in the axial growth rate after 30 min of growth. The evolution of the nanowire dimensions is plotted in Fig. 3c. In this case, we observe that the tapering stays approximately constant as a function of time, the top diameter slightly increasing. This clearly shows that the radial growth becomes dominant when the nanowire axial growth stops.

Even though the sharp decrease in the axial growth rate could be explained by a temperature gradient in the growth chamber, which results in a reduction of the reactions occurring at the catalyst level [44, 45], we think that a more plausible explanation is the disappearance of the indium droplet at the top of the nanowire either by evaporation or by diffusion. The possible catalyst droplet consumption due to diffusion along the nanowire side wall has been studied by means of EEL spectroscopy. The EELS analysis presented in Fig. 4, together with STEM Bright Field (BF) and HAADF micrographs, shows clearly the agglomeration of indium along the wire. However, we should note here that the presence of catalyst clusters along the side wall has been found only sporadically in a few wires. The same effect was found when gallium was used as catalyst.

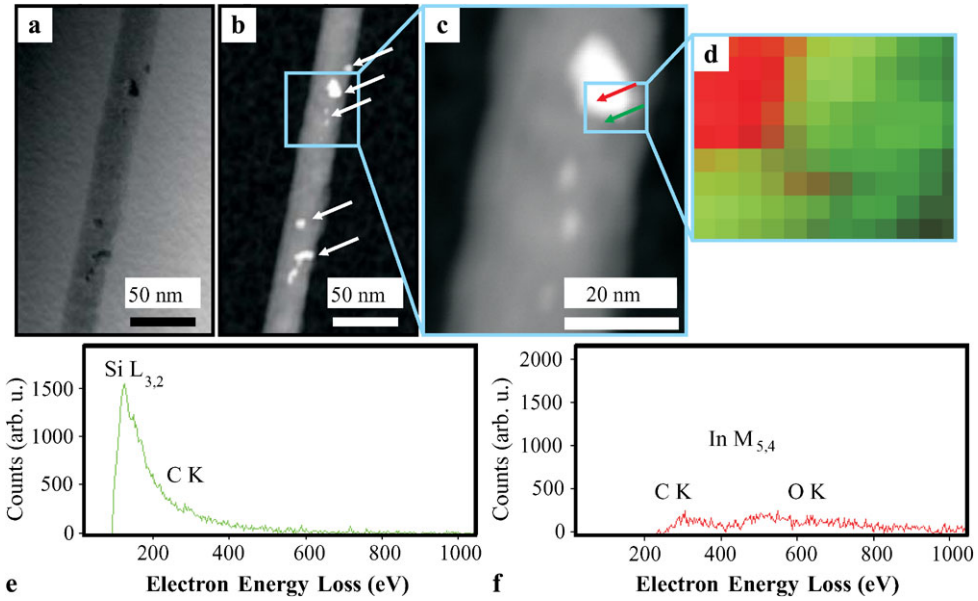

Fig. 4 (**a**) STEM BF and (**b**) HAADF images of a Si NW where the indium oxide segregation along the nanowire side wall has occurred. The indium has oxidized after the growth process, upon exposure of the sample in air. (**c**) HAADF image of an indium oxide aggregate along the nanowire surface. (**d**) Multiple linear least-square (MLLS) fitting performed to the spectrum image obtained from the highlighted region in (**c**), taking the background-subtracted EEL spectra obtained at the highlighted points in (**c**) and displayed in (**e**) and (**f**) as reference spectra. The image presented in (**d**) is a silicon (*green*) and indium oxide (*red*) distribution map

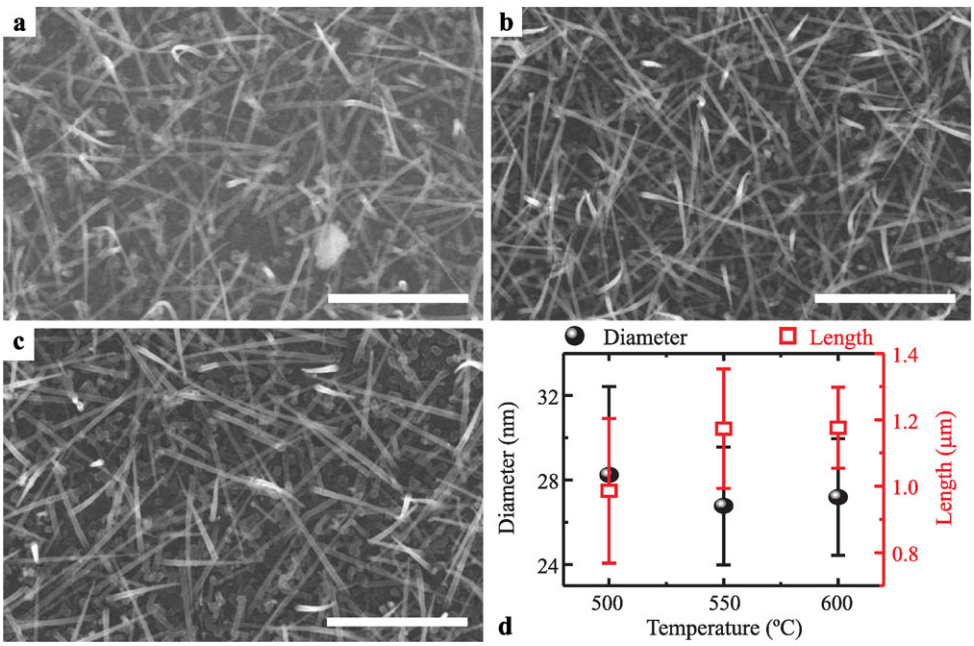

Fig. 5 SEM micrographs of indium-catalyzed silicon nanowires grown for 15 min at 500°C (**a**), 550°C (**b**) and 600°C (**c**). The thickness of the indium layer is 2 nm, and the substrate is Si <001>. Scale bars: 1 µm. (**d**) Temperature dependence of the average diameter and length of the nanowire grown for 15 min on a Si <001> substrate on which a 2-nm-thick indium layer was deposited. Error bars represent the diameter and length dispersion as measured by SEM

3.2 Morphology, structure and temperature dependence

In order to find the optimum conditions for the synthesis of the silicon nanowires, nanowires were grown at 500°C, 550°C and 600°C and the morphology and structure analyzed by ex situ measurements. Representative scanning electron micrographs of nanowires grown for 15 min from 2 nm of indium deposited on a Si <001> substrate are shown in Fig. 5a–c.

Interestingly, even if the growth has been realized on a crystalline substrate, the nanowires do not show any clear preferential orientation. This is surprising, as it has been shown in the past that the use of reducing conditions fosters the epitaxy with the substrate [46, 47].

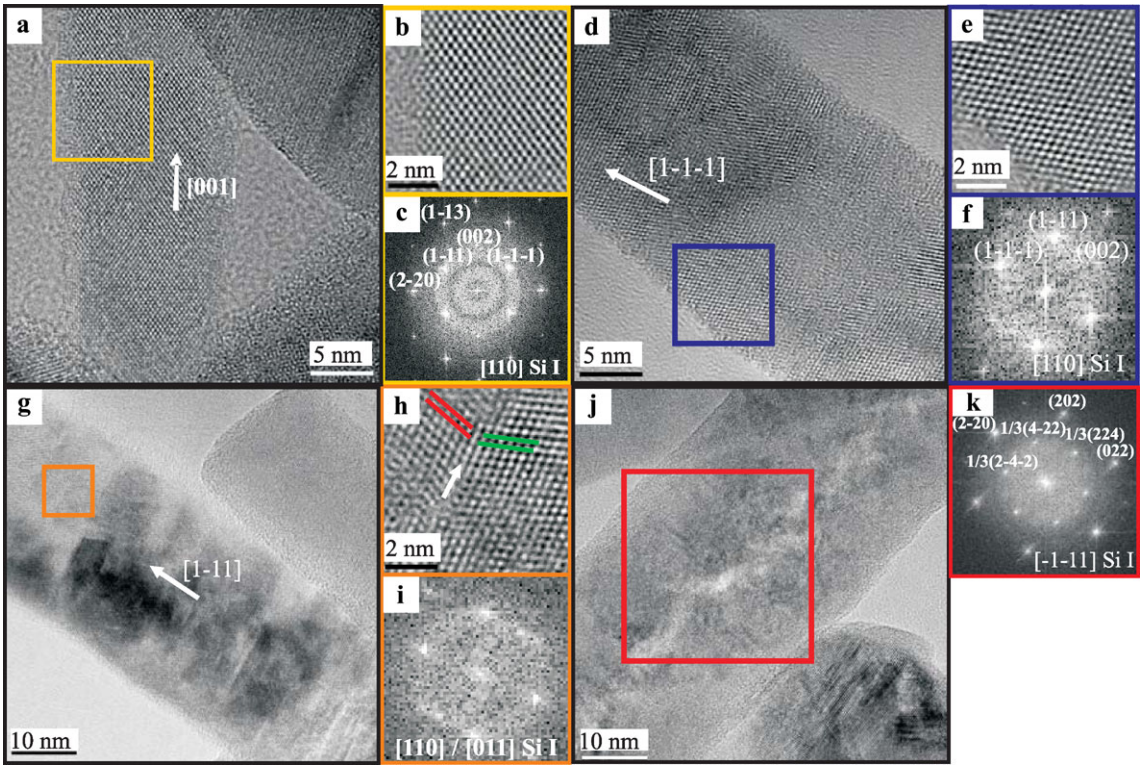

Fig. 6 (**a**) High-resolution transmission electron micrograph of a nanowire grown at 600°C. It has a diameter of 12 nm, is grown along the [001] direction and presents cubic structure with high crystalline purity without any defects, as shown by the HRTEM detail (**b**) and the power spectrum (**c**). (**d**) High-resolution TEM image of a nanowire grown along the [1–1–1] direction at 600°C, which has a diameter of 21 nm. This nanowire crystallized in the diamond cubic phase without the presence of twins, as shown by the HRTEM detail (**e**) and the power spectrum (**f**). (**g**) HRTEM image of a nanowire grown at 600°C along the [1–11] direction, crystallized in the cubic Si I polytype and with a diameter of 28 nm. It presents transversal or lamellar twinning along the growth direction, as shown by the HRTEM detail (**h**) and the power spectrum (**i**). (**j**) Nanowire grown at 600°C along the {112}-type axes with a diameter of 36 nm. This wire presents longitudinal twins on the {111} planes parallel to the growth axis. Panel (**k**) presents a power spectrum of the red squared zone in (**j**). All the nanowires presented here were grown using 2 nm of indium on Si <001> substrate

A high density of nanowires is obtained at the three temperatures. The wires present a tapered shape, some of them being bent or kinked. The density of the nanowires on the surface increases with the temperature, while the bending slightly decreases. The size distribution as a function of temperature has been deduced by SEM measurements on 20 nanowires grown from 2 nm of indium for 15 min and it is shown in Fig. 5d. In this case the middle diameter, defined as $d_m = (d_{bottom} + d_{top})/2$, has been considered. Differently from what happened when gallium is used as catalyst, the nanowire diameter stays approximately constant, decreasing with increasing growth temperature from about 28 nm at 500°C to about 27 nm at 600°C. The dispersion is quite narrow for all the growth temperatures investigated, being always less than 5 nm.

HRTEM has been used for the analysis of the structure and growth direction as a function of the growth temperature and nanowire diameter. The nanowires crystallized in the cubic structure, presenting in some cases a very high crystal quality and in others a high concentration of twins along the {111} planes. A clear dependence of the growth direction with regard to the growth temperature and/or on the diameter is not observed. Typical HRTEM micrographs of the nanowires are shown in Fig. 6. At high and low growth temperatures, all nanowires presented a growth axis parallel either to the <111> or the <112> direction. Surprisingly, in the sample grown at 550°C, only nanowires growing along the <112> direction have been found. One should also note that some nanowires with a diameter close to 10 nm presented a growth axis along the <001> direction, which has not been observed before in unconstrained growth [48, 49].

We did not find any effect of the indium thickness on the morphology or structure of the nanowires. For completeness, in Fig. 7, SEM micrographs corresponding to nanowires grown from different indium layer thicknesses on Si and SiO_2 substrates are shown.

A detailed HRTEM study of numerous nanowires reveals the presence of twin defects on the {111} planes. The density of these defects increases for the lowest growth temperatures. For those nanowires growing along the <112> di-

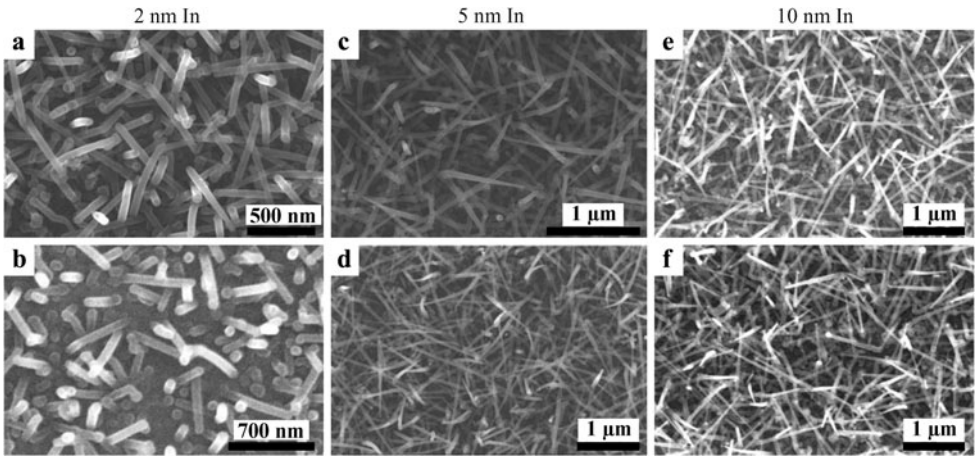

Fig. 7 SEM images of indium-catalyzed silicon nanowires. The thickness of the indium layer is 2 nm on Si substrate (**a**) and on SiO_2 substrate (**b**); 5 nm on Si substrate (**c**) and on SiO_2 substrate (**d**); 10 nm on Si substrate (**e**) and on SiO_2 substrate (**f**). All the samples were grown at 600°C for 30 min, under low plasma power conditions

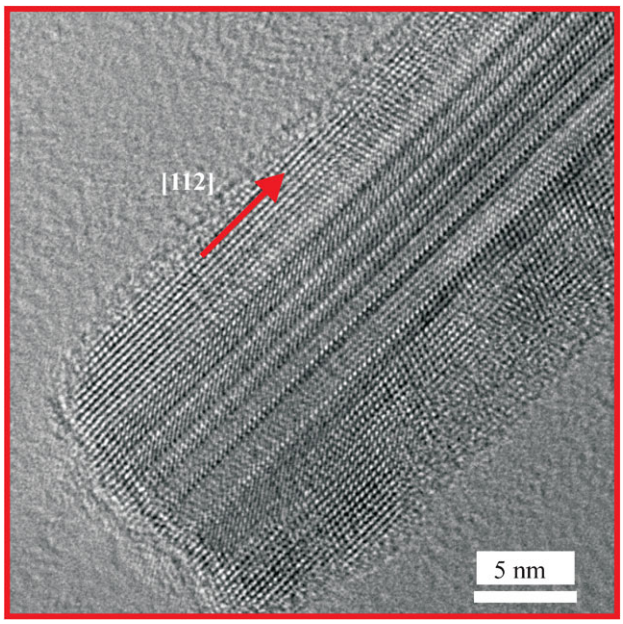

Fig. 8 Silicon nanowire grown at 550°C from 2 nm of indium on Si <001> substrate, along the {112}-type axes. It presents several axial twins on the {111} planes parallel to the growth axis, leading to formation of hexagonal monolayers inside the cubic structure

rection, the twins appear along the nanowire length. This type of twins is denominated axial twins, as reported in the past [50–53]. The twin itself corresponds to a 180° rotation along the [111] axis. Each twin is equivalent to the formation of a monolayer of hexagonal silicon (Si-IV). As has been demonstrated, the occurrence of a high density of multiple twin defects in the cubic structure can sometimes cause the formation of hexagonal phase in local areas [53–55]. An example is given in Fig. 8. The same phenomenon was observed in gallium-catalyzed silicon nanowires [26].

3.3 Raman spectroscopy

In order to investigate the structure of the nanowires on a larger ensemble than with HRTEM, Raman spectroscopy was used. Raman spectroscopy is a non-destructive technique which gives extremely detailed information on the structure of materials. As was recently shown, it is very sensitive to structural defects such as the presence of dense stacking faults or twins [46, 56].

Raman measurements on bundles of wires grown at 500°C, 550°C and 600°C were performed. The results are presented in Fig. 9a. All the Raman spectra present a narrow silicon peak, indicating the high crystal quality of the silicon nanowires. The peak is however slightly down shifted with respect to the bulk Si TO/LO mode at 519–520 cm^{-1}. The shift of about 2 cm^{-1} could be due to the small size of the nanowires defining a short Raman correlation length – as no strain could be measured with HRTEM. Heating of the sample can be excluded, since the typical asymmetric broadening related to a heating effect is not present and special care was taken to use excitation powers below which heating is observed.

In addition to the peak related to the TO/LO phonon, the presence of an additional peak at about 498 cm^{-1} can be observed for all the samples. Moreover, we have realized a deconvolution of the spectra with multiple Lorentzians. This has shown the presence of a further peak, at about 516 cm^{-1}. Figure 9b shows an example of the multiple Lorentzian fit. The existence of these peaks has been explained by the presence of the highly twinned domains and hexagonal phase in nanowires [51, 52, 57, 58]. The position of the band at 498 cm^{-1} coincides with the energy of the phonon dispersion of silicon in the L point. Indeed, the length of the unit cell of the hexagonal phase in the [111] direction is half of the cell of the diamond (cubic) phase. For this reason the phonon dispersion can be approximated by folding the one of the hexagonal structure from the Γ to the L point. This operation leads to the appearance of the band at 495 cm^{-1} at

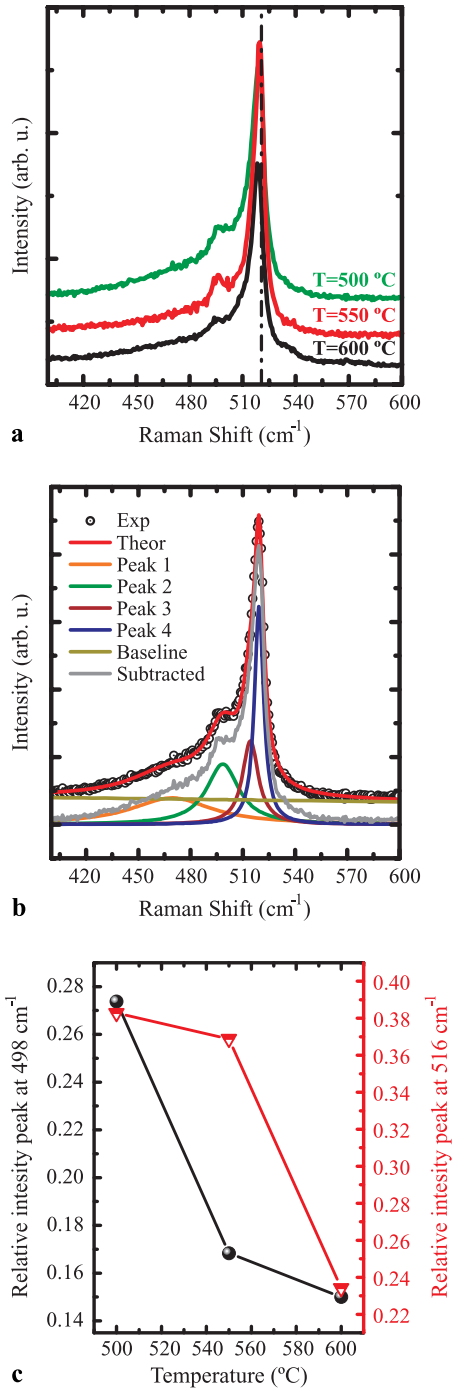

Fig. 9 (**a**) Raman spectra of indium-catalyzed nanowires grown at different temperatures. The nanowires were grown from 2 nm of indium deposited on Si <001> substrate. (**b**) Raman spectrum of the sample grown at 500°C (*open circles*) with individual Lorentzian contributions deconvoluted (*solid lines*). (**c**) Relative intensity of the modes at 498 and 516 cm^{-1} as a function of the temperature. The intensity has been calculated with respect to the TO/LO one for each temperature

the origin of the Brillouin zone. Such band folding has also been observed in the past in SiC, GaN and GaAs systems [56, 59, 60]. Furthermore, the bands at 495 and 517 cm^{-1} have been assigned recently to the E_{2g} and A_{1g} modes, respectively, of the 2H structure, by direct comparison of TEM analysis and Raman studies in Ref. [50].

One should point out that the intensity of these modes around 498 cm^{-1} is relatively low, with respect to the TO/LO mode. This is due to the fact that the twinned regions present only a small percentage of the nanowires. Here, Raman spectroscopy shows its full potential. Indeed, it is highly time and resources consuming to realize HRTEM on a large number of nanowires. On the contrary, Raman spectroscopy can be realized across a grown sample, thereby analyzing the homogeneity in the structure of the nanowires. By measuring several regions of the grown samples, we find that the structure of the nanowires from one run is homogeneous. We have plotted in Fig. 9c the relative intensity of the bands at 498 and 517 cm^{-1}, calculated with respect to the intensity of the TO/LO mode for each synthesis temperature. The intensity of the twin-related bands is higher at the lowest temperatures, in good agreement with the TEM analysis, which has shown an increase in the defect density with decreasing temperature.

Finally, we would like to compare the measurements with previous Raman results obtained on gallium-catalyzed nanowires [255]. There, a peak with extremely low intensity appeared at 495 cm^{-1} in the samples grown at low temperature. The preferential growth direction of these nanowires was <112>, coinciding with the existence of high-density twins along the {111} planes.

4 Discussion

In order to further understand the necessity of using reducing conditions for the nanowire growth, we investigated the capacity of indium to oxidize when exposed to air. For that, the composition of indium droplets at the top of the nanowires was measured by EELS and HRTEM. The TEM micrograph of an analyzed nanowire is shown in Fig. 10a together with the multiple linear least-square fitting of an EELS mapping performed on the highlighted region in (a) (Fig. 10d). The EEL spectra taken at the nanowire core and droplet are shown in Fig. 10b and c. At the nanowire core, silicon is the only element detected—besides the carbon coming from the TEM grid. At the nanowire tip, silicon is not detected any more and a mixture of indium and oxygen is found. In Fig. 10e, the TEM micrograph of a second nanowire is shown. In this case, the structures at the droplet peak and nanowire are analyzed by electron diffraction, which are shown in Fig. 10f and g. The core of the nanowire corresponds to silicon crystallized under diamond structure, while the nanowire tip corresponds to single-crystalline In_2O_3. This analysis demonstrates that the whole indium droplet has oxidized. From this, we deduce

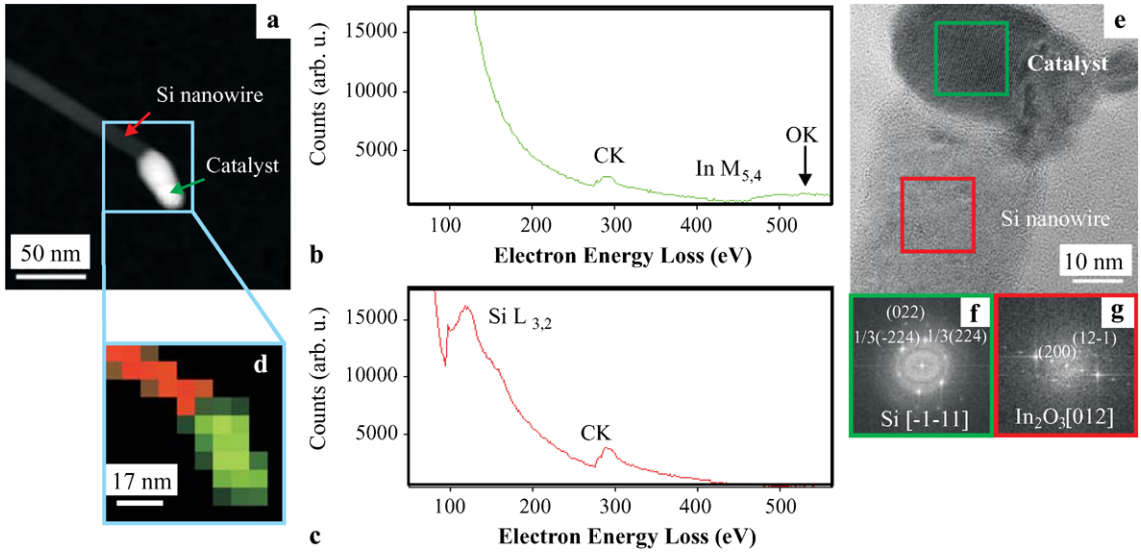

Fig. 10 (**a**) HAADF image of a Si NW grown at 500°C from 2 nm of indium. (**b**) and (**c**) EEL spectra obtained on the catalyst and on the nanowire, respectively, at the positions indicated in (**a**). (**d**) MLLS fitting performed to the spectrum image obtained from the highlighted region in (**a**), taking the spectra displayed in (**b**) and (**c**) as reference spectra, so that it gives a Si (*red*) and In_2O_3 (*green*) distribution map. (**e**) HRTEM image of a Si NW grown at 550°C from 2 nm of indium, and FFTs corresponding to the nanowire (**f**) and the catalyst (**g**)

that the use of conditions with a high density of atomic hydrogen must be key for the reduction of the indium layer deposited prior to the nanowire synthesis. We have found that the annealing under hydrogen plasma is key for the successful synthesis of nanowires with indium as a catalyst.

5 Conclusion

We have presented a study of the synthesis of silicon nanowires by using indium as a catalyst. The use of a hydrogen-rich plasma during the annealing prior to growth has shown to be key for the successful nanowire growth. The appearance of lamellar and axial twins has been demonstrated by HRTEM and Raman spectroscopy. Synthesis at the lowest temperature (500°C) leads to nanowires with the lowest defect density. This study represents a further step towards the use of alternative catalysts for the synthesis of nanowires.

Acknowledgements The authors would like to kindly thank G. Abstreiter and M. Bichler for their experimental support. This research was supported by a Marie Curie Excellence Grant 'SENFED' and the DFG excellence cluster Nanosystems Initiative Munich.

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