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TECHNICAL PAPER

Fabrication of silicon-on-insulator MEM resonators with deep sub-micron transduction gaps

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Abstract The paper proposes and validates a low-cost technological process for the realization of monocrystalline micro-electro-mechanical (MEM) resonators with deep sub-micron transduction gaps, on silicon-on-insulator (SOI) substrates. The MEM resonators are designed to work as bulk lateral resonators (BLR) in which the resonance of a suspended mass is excited and detected by lateral electrodes. For MEM BLRs, nano-scaled gaps (<200 nm) are essential to reduce the motional resistance in the order of few kΩ as well as to avoid the use of large DC applied voltages. Only standard optical lithography with 1 μm resolution and IC-compatible processing steps are employed to obtain 100–200 nm wide gaps with very high aspect-ratios of more than [40:1], allowing the fabrication of high Q resonators for MHz to GHz operating frequency range.

1 Introduction

Latest developments in the field of RF devices and systems show increased interest concerning the miniaturization and integration of the resonator element into the reference oscillator (Nguyen and Howe 1999; Nguyen 2004; Bannon et al. 2000). A large part of the efforts are focusing on silicon or SOI MEM resonators which promise to be a viable alternative to stable but bulky quartz crystals, due to their remarkably miniaturized sizes which allow high integration levels (Wang et al. 2000, 2003; Quévy et al. 2003; Pourkamali and Ayazi 2003; Xie et al. 2003; Kaajakari et al. 2004).

In order to extend the operating frequencies domain in the tens of MHz–GHz range, the resonator size, so also the actuation area is decreasing, and it becomes challenging to maintain acceptable resonator impedance (R_m) and power levels. The motional resistance, R_m, of a MEM BLR is proportional to: $\frac{g^4}{h^2 \times w^2}$, where g is the width, h the depth and w the length of the transduction gap. Therefore, in order to meet the specifications for practical applications, it is essential to decrease the gap width, while maximizing the trench aspect ratio (h/g) as much as possible. For this reason, gaps in the 100–200 nm range, with aspect ratios as high as [40:1] are targeted.

2 Process flow

The cross-sections from Fig. 1 summarizes the fabrication sequence.

The starting material is SOI substrate, with a Si layer thickness of 1.5 and 3 μm buried oxide (BOX). The initial step consists of a 0.5 μm tetra-ethyl-oxysilane (TEOS) deposition, followed by patterning and etching of the first mask, which will define the MEM resonating structure. A polysilicon layer with a thickness of less than 100 nm, which will serve as gap-spacer, is then deposited. At this processing step, the cross-section looks as in Fig. 1a. Next a second TEOS layer is

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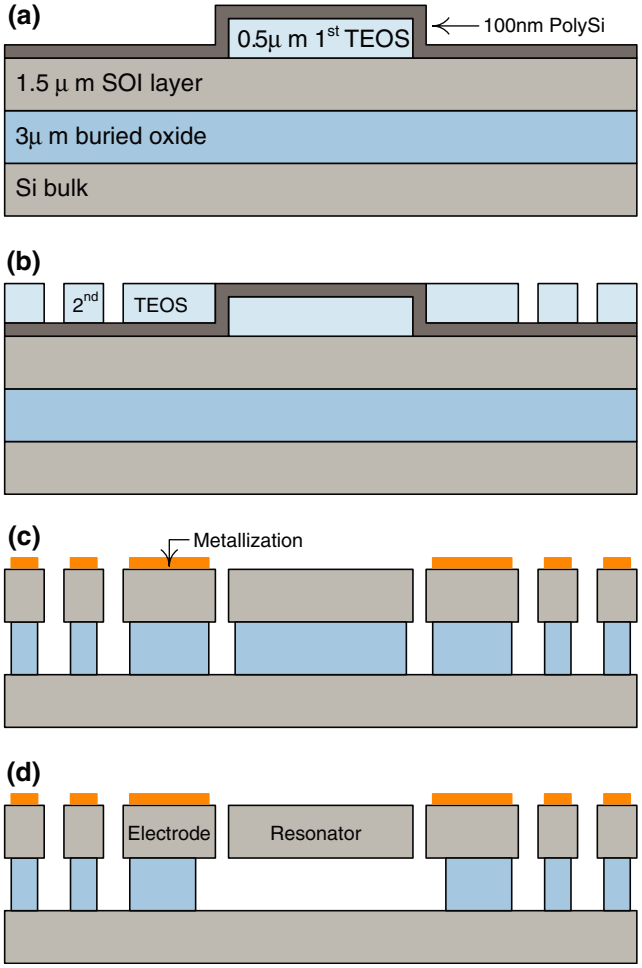

Fig. 1 Process flow main steps

deposited, followed by a combination of chemical mechanical polishing (CMP) and wet etch in order to expose the polysilicon layer. A second photolithography step and a dry SiO_2 etch will define the resonator's electrodes. At this stage, as shown in Fig. 1b, the hard-mask which will be used to etch the Si MEM resonator is complete. The structure is then etched with a low-frequency pulsed plasma inductive-coupled-plasma reactive-ion-etch (ICP-RIE) in order to avoid Si notching at the BOX interface, and the mask oxide is removed in buffered hydrofluoric acid (BHF). Subsequently, using a third mask, the undoped polysilicon is removed from the contact area, and metal is plated. Figure 1c illustrates the process at this step. At last, the structure is released in BHF as depicted in Fig. 1d.

3 Nano-gap mask formation

The deep sub-micron openings in the TEOS hard mask which are used to etch the nano-gaps are obtained by depositing and then selectively removing a very thin polysilicon spacer layer. The PolySi LPCVD has a good uniformity; therefore the in-wafer nano-gap mask opening variation is smaller than ±5%.

It is very important that after patterning the first mask, the TEOS sidewalls are very smooth and vertical. Otherwise, the polysilicon gap spacer which is following exactly the shape of the structure will be tilted and the plasma would not have directional access to the SOI layer when etching the resonators. For this reason, a high quality first photolithography step is essential, as well as a selective, smooth oxide dry-etch recipe.

A second oxide is then deposited above the polysilicon, and then etched back with a combination of CMP and wet etch, until the spacer layer is uncovered. It is important that the polysilicon layer is not damaged at this stage, because later on it will be used to protect the oxide underneath, while patterning the electrodes, sealing ring and contact pads. The CMP speed is highly dependent on the pattern density and size, the general rule being that some wide, high-density patterns planarize the slowest and narrow, isolated features planarize the fastest. Therefore, in some areas, the polysilicon layer will be exposed faster and it will start to erode. Since the layer thickness is of 100 nm or less, there is a high risk of punching through the polysilicon in the areas with a less dense pattern. This problem can be avoided by stopping the CMP before reaching the polysilicon layer, and by finishing the oxide back-etch with a short BHF step.

Special attention must be paid to the second oxide deposition. At first, LPCVD low temperature oxide (LTO) has been tested, and the electrodes were etched using BHF. The SEM images taken at this point (Fig. 2a) revealed that voids were formed during LTO deposition, which were etched faster in BHF, generating an uneven shape in the hard mask at the electrode corner in contact with the polysilicon spacer. For this reason, as shown in Fig. 2b, after etching the gaps, the trench interface with an open area was very rough, a strong skirting effect being observed.

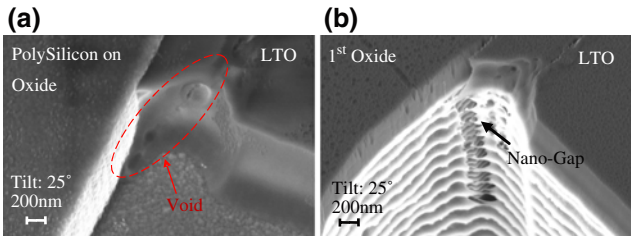

Fig. 2 SEM pictures showing voids in the LTO layer after patterning the electrodes (**a**) and after etching the gap (**b**)

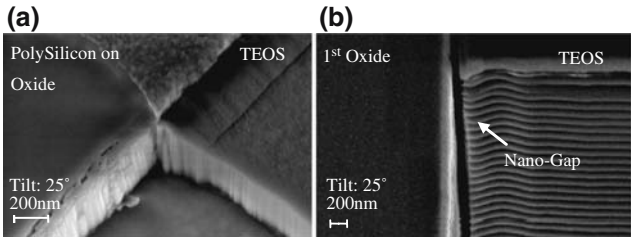

Fig. 3 SEM pictures of the improved process, showing the hard mask after patterning the electrodes with a dry plasma etch (**a**) and the etched nano-gap (**b**)

In order to solve this difficulty, the process flow was changed by replacing the LTO with LPCVD TEOS, which has better step-coverage and higher density, and by etching the electrodes with a selective C_4F_8 plasma etch instead of wet BHF-etch. The results obtained with the improved process are shown in Fig. 3.

4 Nano-gap etch

One of the most critical steps of the process is the deep sub-micron gap etch. Two different techniques have been evaluated, a continuous etch-process, and the super high aspect ratio process (SHARP), developed at Alcatel Vacuum Technology (Puech et al. 2003).

The continuous process uses a mix of etching (SF_6) and passivating (C_4F_8) gases, and due to the directional ion bombardment, the passivation layer is removed at much higher rate from the bottom of the trench, exposing it to the etch. The process has the advantage of generating smooth walls, but it proved to be very sensitive to the angle of the hard-mask openings, caused by the first photolithography step, as shown in Fig. 4.

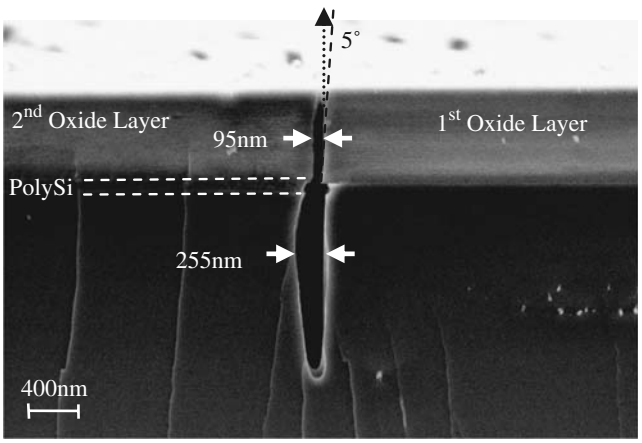

Fig. 4 SEM picture of a nano-gap etched using the continuous process

In the picture above we can see that as the ions which are reaching the substrate are not coming under a 90° but a slightly smaller angle, one of the trench walls is bowed, noticeably increasing the gap-width.

Better results were obtained starting from the SHARP process, based on the Bosch technique, which uses alternating etching and passivating steps to achieve high aspect ratio trenches in silicon. The Bosch process has its limitations, among which we can mention the scalloping-induced wall roughness, the large undercut and the aspect ratio limited to maximum [30:1]. When used for etching deep sub-micron trenches, all these effects become critical, being a major limiting factor. The main improvements of the SHARP process include: (a) fast-switching of the etching and passivating steps to reduce the wall roughness, (b) raising the platen power and decreasing the pressure for a longer mean free path, (c) adding an O_2 plasma step for better polymer removal and (d) decreasing the substrate temperature for a higher mask selectivity.

Figure 5 shows the SEM picture of a 200 nm wide and 7.5 μm deep gap etched with this technique. Aspect ratios of [40:1] and low scalloping, thus smooth vertical walls have been demonstrated, although aspect ratios as high as [60:1] can be obtained. The limiting factor for the achieved trench depth was the etch selectivity between the silicon and the oxide hard-mask. For further tests regarding the maximum achievable aspect ratio, thicker oxide hard-mask should be used.

4.1 Notching effect

Deep reactive ion etch (DRIE) processes may have different silicon etch-rates due to loading effects as aspect-ratio-dependent-etch (ARDE) or the general

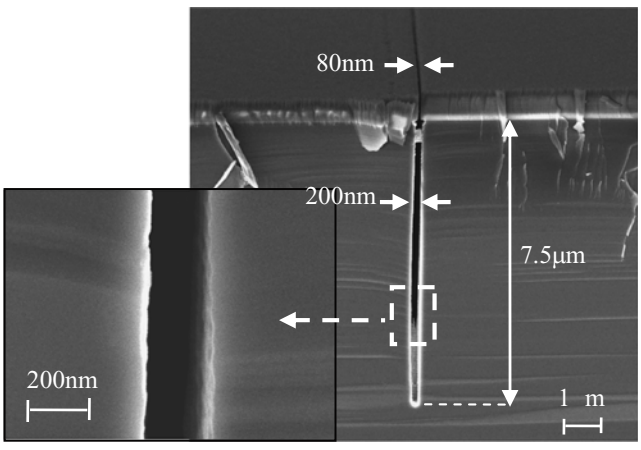

Fig. 5 SEM picture of a 200 nm wide and 7.5 μm deep trench, etched with a SHARP-based process

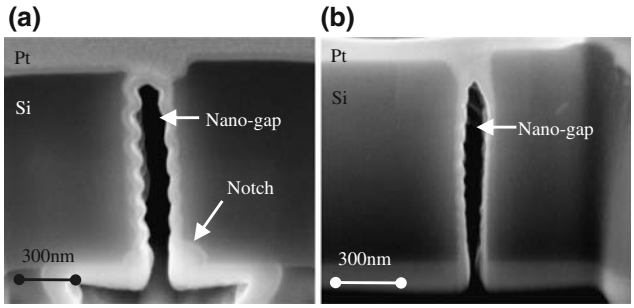

Fig. 6 FIB cross-sections of fully etched nano-gaps showing **a** notching and **b** notch-free profile obtained with an Adixen AMS 200 DSE etcher. The lighter-colored material is the platinum protection deposited with the FIB

loading effect by which edges of the wafer etch faster than the center. The same applies to the SHARP process, the etch-rate being more than two times lower in the nano-gap area than in the large openings. For this reason, wide opened spaces on the wafer will be overetched by as much as 150% until the nano-gaps are completely opened.

At the same time, plasma etching of silicon over an insulator layer can result in a notching problem at the silicon/insulator interface, due to trapped charges in the insulator, as it can be seen in Fig. 6a. The notch size is proportional to the etch time, so large overetch of the big openings results in significant notching effect.

This effect can be removed by using a low frequency pulsed substrate polarization, which allows the ions to escape, preventing the charge accumulation. We have used an Adixen AMS 200 DSE etcher and a typical notch-free result is shown in Fig. 6b.

4.2 Skirting effect

One additional phenomenon related to the DRIE processes, which can cause a short between the electrodes and the resonating structure, is the so called ''skirting effect''. Due to over-passivation, the etch fails to entirely remove the silicon at the interface between narrow trenches and larger openings, producing a result as shown in Fig. 7.

Since the skirting effect cannot be solved by modifying the process parameters without affecting the selectivity of the etch, the undercut and the gap profile, a special anti-skirting design was needed. The design uses a smooth transition between the trench and the open area, as shown in Fig. 8.

From the pictures above we can see that the anti-skirting design solves the problem completely, no skirting being observed for gaps of up to 10 μm deep.

The final critical step of the process is the resonator release and oxide mask removal, by wet etching the

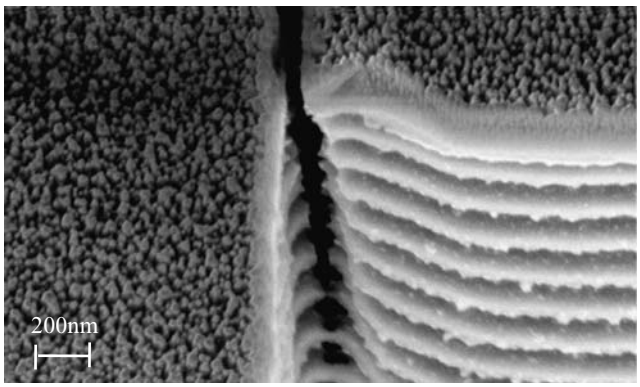

Fig. 7 SEM picture of the nano-gap interface with a large opening, showing an extreme case of skirting

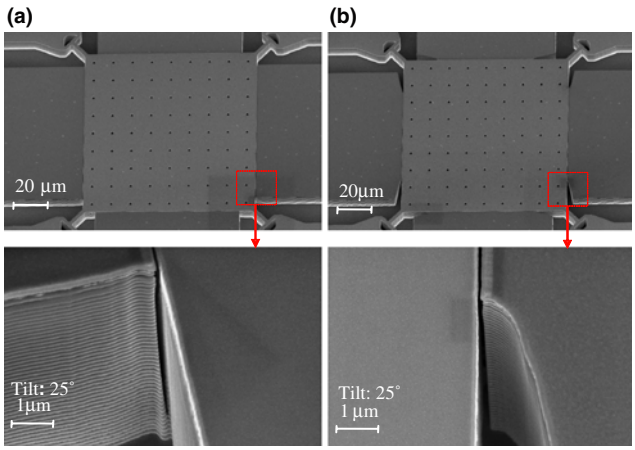

Fig. 8 SEM pictures of MEM resonators and nano-gaps without (**a**) and with (**b**) anti-skirting design

oxide. First tests have shown that most of the structures can be successfully released with BHF and air-dried although some of the less stiff structures suffer from release-related stiction (see Fig. 9). In the future, supercritical drying needs to be used in order to entirely solve the stiction problem.

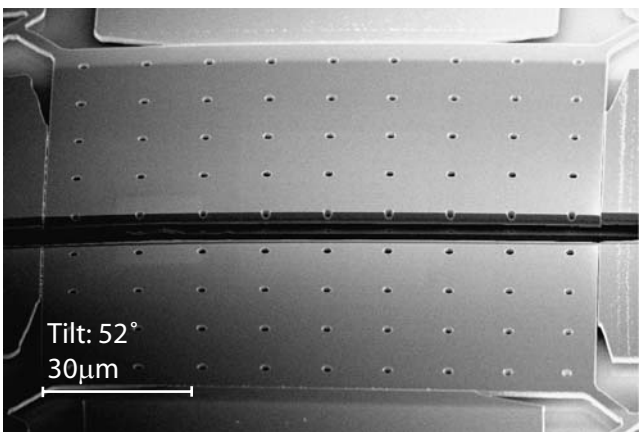

Fig. 9 FIB cut through a released resonator

5 Conclusions

A fabrication process for realizing mono-crystalline MEM resonators with deep sub-micron transduction gaps on SOI substrates has been developed and validated. Gaps of less than 200 nm were obtained, using only standard optical lithography with 1 μm resolution. Aspect ratios as high as [40:1] were demonstrated, using an optimized, notch-free dry etch process based on Alcatel Vacuum Technology's SHARP. An anti-skirting design has been proposed and validated for gap depths of up to 10 μm, allowing the fabrication of MEM resonators with low impedance levels, without the need of high DC voltages, functioning in the hundreds of MHz–GHz range.

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