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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Física, realizada sob a orientação científica do Professor Doutor Nikolai Andreevitch Sobolev, Professor Associado do Departamento de Física da Universidade de Aveiro, e do Professor Doutor José Carlos Esteves Duarte Pedro, Professor Catedrático do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro

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Abstract

In this MSc Thesis we evaluate the channel current characteristics of a GaN High Electron Mobility Transistor (GaN HEMT) for its potential memristive characterisics. Using a Matlab implementation of the SRH physics model and several experimental pulsed I/V and sinusoidal excitation data, we demonstrate that GaN HEMT channels affected by deep level traps can indeed display the two fundamental memristive criteria: (i) A pinched hysteretic trajectory in the i_{DS}/v_{DS} phase plane when the device is excited by a sinusoidal stimulus, and (ii) a hysteresis area that is monotonic and vanishes for increasingly higher frequencies.

Resumo

Nesta dissertação de Mestrado nós avaliamos as características da corrente do canal de um GaN High Electron Mobility Transistor (GaN HEMT) pelas suas características memristivas. Utilizando uma implementação do modelo físico de SRH em Matlab e diversas medidas experimentais pulsadas I-V e resultados de excitação sinusoidal, nós demonstramos que o canal de um GaN HEMT afectado por traps de níveis profundos pode, de facto, apresentar as duas características fundamentais do critério de memristividade: (i) Uma trajectória com histerese comprimida no espaço de fase i_{DS}/v_{DS} quando o dispositivo é excitado por um estímulo sinusoidal, e (ii) uma histerese cuja área é monotónica e desvanece para frequências cada vez maiores.

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List of Abbreviations and Acronyms

GaN Gallium Nitride. 1, 2, 3

HEMTs High Electron Mobility Transistors. 1, 2, 3

GaAs Gallium Arsenide. 1

MESFETs Metal-Semiconductor Field-Effect Transistors. 1

Si Silicon. 1

LDMOS Laterally Diffused Metal-Oxide-Semiconductor. 1

RF Radio-Frequency. 1, 2

I-V curve Current-Voltage Characteristic. 1

DC Direct Current. 1

HEMT High Electron Mobility Transistor. 1

IC Integrated Circuits. 2

HP Hewlett-Packard. 2

ReRAM Resistive Random Access Memory. 2

AlN Alluminium Nitride. 3

n-GaN n-type Gallium Nitride. 3

MIS Metal-Insulator-Semiconductor. 3

SRH Shockley-Read-Hall. 3, 10

HJFETs Heterojunction Field-Effect Transitors. 6, 8, 9

BG Backgate Terminal. 6, 7, 9

AWG Arbitrary Waveform Generator. 29

DUT Device Under Test. 29

Chapter 1

Introduction

1.1 Problem Statement

GaN HEMTs are currently ubiquitous in the field of radio frequency power amplifiers. They surpassed GaAs MESFETs with higher output power and lower capacitance per unit size, and Si LDMOS transistors with maximum operating frequencies [8], [9]. However, contrary to GaAs and Si, heteropitaxial growth of GaN has still much to improve. In fact, problems that were solved for these materials, particularly carrier-trapping defects, are currently unsolved and strongly affecting GaN technology [10].

Carrier-trapping effects generate complex behaviour in microwave field-effect transistors which severely alters their radio-frequency performance. A variety of outputs has been linked to trapping, particularly knee walk-out, RF dispersion and kink of the I-V curve. In literature, all these are commonly abbreviate to current collapse [11], broadly defined as "the recoverable decrease in drain current induced by the exposure to high electric field" [12], or, as the large signal current dispersion between DC and RF [13].

Two distinctive mechanisms have been identified as precursors of current collapse: dynamic on-resistance and variation of the threshold voltage. Evidences show a strong correlation between these mechanisms and the trap sites on the HEMT structure. For instance, surface traps increase the on-resistance, which is a clear disadvantage for power devices since their parasitic resistance should be negligible. Buffer and substrate traps are related to shifts in the threshold voltage (or self-biasing) [12]. It is also common to address these effects by the terminal voltage that induce them, for instance, gate voltage variations are thought to change the charge in surface states. Thus, the increase of on-resistance is labelled as gate-lag. Likewise, drain-voltage variations are related to shifts in the threshold voltage, originating the drain-lag designation. Currently, gate-lag is nearly extinct due to the effectiveness of high quality passivation and gate field plating to suppress the manifestation of surface traps. On the other hand, drain-lag is a problem still unsolved [8]. Throughout this work, we will exclusively be concerned with the drain-lag phenomena. Figure 1.1 illustrates this effect using a square pulse excitation on a FET polarized above the threshold voltage.

The emergence of the term *lag* is associated to a particular effect of trapping, namely the slow current transient once the voltage is changed. To better understand this concept, suppose we are analysing a HEMT, in the steady-state, polarized with $(V_{GS}, V_{DS}) = (0, 1)$ V. To visualize the drain-lag effect, we apply a step pulse of $(0, 20)$ V as demonstrated in Fig. 1.1. Previous studies tell us that after a few nanoseconds, most traps

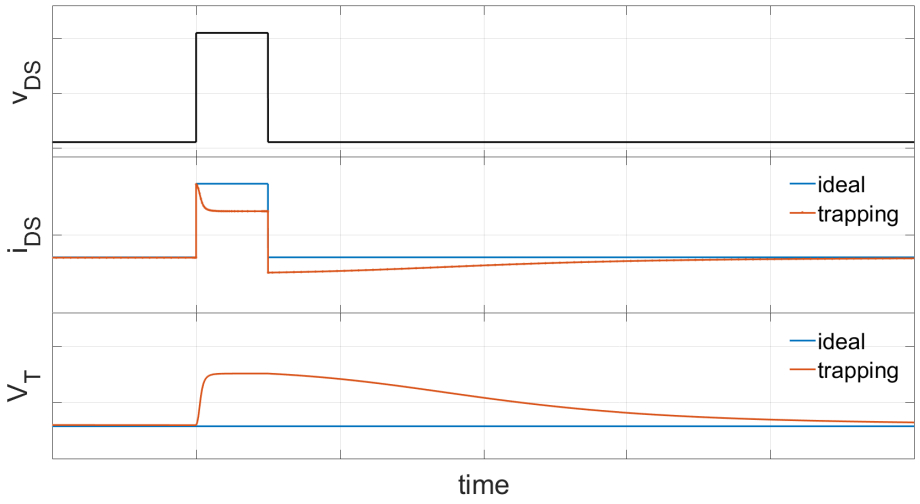

Figure 1.1: Simulation of the drain-lag effect for a square pulse of V_{DS}. The model used in this simulation is based on the self-backgating and Shockley-Read-Hall statistics. It will be explained later.

will be filled (respective to the 20 V state), which in consequence causes the current to collapse. Looking careful at Fig. 1.1 one sees evidence of this steep current overshoot at the rising-voltage edge. This phenomena is so fast in modern devices that it passes unnoticed for conventional measurement techniques [2].

Already in the steady-state, we now step down the drain voltage to the initial $(0, 1)$ V. The new drain current value will not be the same as the one we began with. Now, the device is affected by the 20 V drain-induced trapping, and the current recovery will be limited by the detrapping process, known to linger from nanoseconds up to seconds [10]. Remember that these devices are made to operate in the RF spectrum, which means this process is considered very slow.

This simple example captures the fundamental aspect of drain-lag and helps us understand two crucial concepts: asymmetric time constants and slow current transients. They pose serious problems for many applications, as gain variation in broad band amplifiers and decreased phase margin in digital IC [2]. Yet, these characteristics are also clear evidences of memory [3].

So, one question arises: Can we find an application for drain-lag in GaN-HEMTs? And if so, can we prove it?

1.2 State-of-the-art

In 2008, HP claimed it had found the memristor. This argued result triggered a widespread search for new memristors, mostly because of there many promising applications. We can highlight perhaps the most interesting ones, namely neuromorphing computing and ReRAM devices [14].

As we will see later on, memristors are defined by a particular set of simple conditions that we expect to find in GaN-HEMTs affected by trapping. Establishing this link could provide a new incentive to the exploration of other applications for GaN HEMTs.

We see two possible approaches to prove that GaN HEMTs are memristors. In the first option, we could use physical models to simulate trapping in these devices and observe the memristor characteristics. We found no evidence of previous studies trying to do what we propose. However, there is a lot of research on models we could and will base our work upon. In the second option, we could measure the macroscopic behavior of GaN HEMTs and verify the memristor characteristics. We found little evidence of research on this topic. Perhaps the most similar work was found in [15] where it is shown evidences of reproducible bipolar resistive switching in AlN/n-GaN MIS. Given our position in this unexplored topic, we will dedicate this section to the research done on the origin of memory effects in HEMTs and to the memristor definition. Each model presented in the following sections are extensive, so we will direct the reader's attention to the key concepts of each one, in order to provide us with the required tools to understand the theoretical basis and new developments in this field.

1.2.1 Shockley-Read-Hall Model

It is known that the origin of drain-lag has to do with charge-carrier trapping by deep-level traps. One of the most reliable theoretical work that describes this class of defects is the SRH model. In fact, the following models dedicated to the explanation of drain-lag in HEMTs are all based on the SRH model. Thus, it is essential to understand this theory's core.

The SRH model (or statistics) is a phenomenological model based on the Fermi-Dirac statistics, that explains recombination of holes and electrons, the hole-electron pair generation and charge trapping as a trap-assisted process in semiconductors. It happens that certain crystal defects form levels in the bandgap with activation energies considerably higher than those of the typical shallow donors or acceptors. These deep-levels are expected to capture and emit both electrons and holes at low rates, resulting in charge-trapping and in some circumstances, in charge recombination [1]. Notice that shallow defects also capture and emit charge carriers, however, these processes are so fast that we are not able to distinguish them at a macroscopic level, and thus they are not relevant for this discussion.

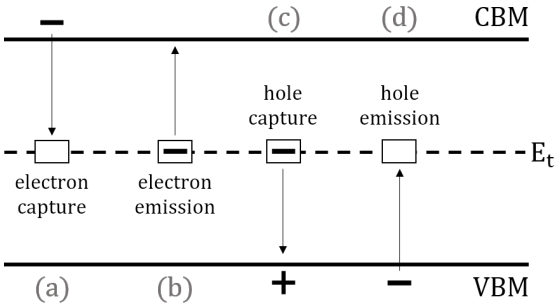

Figure 1.2: Schematic representation of the 4 basic processes involved in the SRH model for an acceptor-like center. Electron capture: a free electron is captured by a neutral trap; electron emission: a negative charged trap emits an electron to the conduction band; hole capture: a negative charged trap emits an electron to the valence band, or from another perspective, the trap captures a hole from the valence band; hole emission: the neutral trap captures an electron from the valence band (or emits a hole to the valence band). Adapted from [1].

The simplest SRH model assumes that each trap has two possible states, separated by an electronic charge unit. Fig. 1.2 shows the 4 basic processes likely to happen on a trap with a neutral and a negative state, mimicking the behaviour of an acceptor. Notice that other types of traps are also possible. For instance, trap-states can switch between neutral and positive (donor-like) or even between -1 and -2 charge states.

There are several approximations made in this model that are worth mentioning. For instance, it is assumed that the trap level in the bandgap is discrete and unique. This is not accurate because the combination of defects in the crystal lattice creates their own narrow bands, and so the charge capture is mostly made by the more energetic states of these bands, followed by a relaxation period of the particle to the ground-state. However, because this relaxation period is very short, from a macroscopic perspective, the trap is considered always to be in the ground-state [1]. Another approximation, that is used to obtain the simplest SRH model, is to assume a single trap level. In reality, actual devices have different defects that induce discrete bands separated by forbidden states, thus creating multiple trapping levels, and consequently numerous time constants [16]. This last approximation is not indispensable for our study but help us simplify the model we will use.

The distribution function of a trap center, f_t, follows a sigmoid curve equivalent to a modified Fermi-Dirac function whose Schrödinger equation's eigenvalue is replaced by an effective energy level, in this case the defect energy E_t. These variables are related by

$$f_t = \frac{1}{1 + \frac{1}{g} exp^{\frac{E_t - F}{k_B T}}} \tag{1.1}$$

where F stands for the Fermi level in thermal equilibrium, k_B is the Boltzmann's constant and T the system's temperature. A degeneracy factor, g, is added to account for additional spin states: $g_n = 2$ for electrons in the conduction band and $g_p = 4$ for holes in the valence band [17]. This function ranges between zero, when the trap is empty, and one, when it is full.

The processes of capture and emission can then be described by the rate of variation of the occupancy ratio, seen in eq. 1.1, as

$$\frac{df_t}{dt} = nc_n(1 - f_t) - e_n f_t - c_p f_t + e_p(1 - f_t). \tag{1.2}$$

The terms on the right side of the equation, from left to right, correspond to process (a), followed by (b), (c) and finally (d), explicit in Fig. 1.2. n and p are the concentrations of free electrons and free holes. The electron-emission rate e_n and the hole-emission rate e_p are related to the electron-capture coefficient c_n and to the hole-capture coefficient c_p as: $e_n = n_1 c_n$ and $e_p = p_1 c_p$, where $c_n = \sigma_n v_{thn}$, $c_p = \sigma_p v_{thp}$. The origin of n_1 and p_1 is explained below. σ_n and σ_p are the electron-capture and hole-capture cross-sections of the traps. v_{thn} and v_{thp} are the electron and hole thermal velocities. N_c and N_v are the effective density of states in the conduction and valence band. E_c, E_v and E_t are the energy levels for the conduction band minimum, valence band maximum and deep-level trap.

To help the reader familiarise with eq. 1.2 let us analyse its first term. As we said, it represents process (a), i.e. the capture of an electron from the conduction band. Assuming some constant capture coefficient, this term states that a larger concentration of free electrons in the conduction band, n, incentives a higher rate of capture. Likewise, a higher probability of a trap being empty, $1 - f_t$, also results in a higher rate of capture. The second term, describing process (b) - the emission of a trapped electron to the conduction band - is now just dependent on the occupancy ratio of a trap. Some [10] consider an additional factor, $1 - n/N_c$, that represents the probability of unoccupied states in the conduction band that are able to collect the emitted electron. However, we can safely assume $n/N_c \ll 1$ for a general case. The other two remaining terms of eq. 1.2 have the same interpretation that we made for the first two, but now considering the hole as the charge intermediary between the deep-level trap and the valence band.

The present discussion is limited to the non-degenerate case ($|E_{c,v} - F| > 3k_B T$) or diluted electron concentration $n, p \ll N_{c,v} \sim 10^{19} cm^{-3}$. Therefore, we can approximate the Fermi-Dirac distribution of free charge carriers in their respective band to a Maxwell-Boltzmann distribution, where n and p are expressed as

$$n = N_c \, exp\left(\frac{F - E_c}{k_B T}\right),$$

$$p = N_v \, exp\left(\frac{E_v - F}{k_B T}\right). \tag{1.3}$$

For thermal equilibrium, $\left(\frac{dn}{dt}\right)_{SRH} = (b) - (a) = 0$ and $\left(\frac{dp}{dt}\right)_{SRH} = (d) - (c) = 0$. From these, we can obtain a new relation for the emission rate coefficients, using eq. 1.2, as

$$\begin{aligned}
\frac{e_{ne}}{c_{ne}} &= \frac{1}{g_n}\, n_e\, exp\left(\frac{E_t - F}{k_B T}\right) = \frac{1}{g_n}\, N_c\, exp\left(\frac{E_t - E_c}{k_B T}\right) = n_1, \\
\frac{e_{pe}}{c_{pe}} &= \frac{1}{g_p}\, p_e\, exp\left(\frac{F - E_t}{k_B T}\right) = \frac{1}{g_p}\, N_v\, exp\left(\frac{E_v - E_t}{k_B T}\right) = p_1,
\end{aligned} \tag{1.4}$$

where the subscript e is used to denote the quantities respective to equilibrium. Notice that, n_1 (and p_1) represent the concentration of electrons in the conduction band (and holes in the valence band) as if the Fermi level coincided with the SRH center level, times the degeneracy factor.

As mentioned above, the procedure used to relate the capture with the emission coefficients is valid when the system is in thermal equilibrium. In fact, experimental studies regarding traps in SiO_2 suggest that the existence of strong electric fields can cause a decrease in the cross-section values of neutral traps by an order of magnitude [18], thus altering the capture coefficient and consequently its relation with the emission coefficient. Nevertheless, for small deviations from the steady-sate one can apply the following approximations [19],

$$\begin{aligned}
\frac{e_{ne}}{c_{ne}} &\doteq \frac{e_n}{c_n} = n_1, \\
\frac{e_{pe}}{c_{pe}} &\doteq \frac{e_p}{c_p} = p_1.
\end{aligned} \tag{1.5}$$

These approximations will prove to be indispensable for the development of the next models.

We now close the topic of the SRH model and introduce the pioneering work of Kunihiro and Ohno, as they were the first ones, that we are aware, to relate the SRH model with the drain-lag effect seen in HJFETs.

1.2.2 Kunihiro and Ohno Model

The entire mathematical construction of the Kunihiro and Ohno model begins with eq. 1.2. Based on experimental evidences, only electron traps are considered here, thus the last two terms of the equation are neglected. A succeeding paper from the same group deals with the case of hole traps [20]. Furthermore, it was assumed at the time that traps are located in the interface between the epitaxial layer and the substrate. Also, and very important, they assumed that the captured charge comes from the channel. From here, they idealized the epitaxial layer as a parallel plated capacitance in parallel with a resistor, whose terminals correspond to a channel's portion and the interface, just as represented in Fig. 1.3. The pseudo-terminal created by the traps is named the Backgate terminal (BG). This is one of the key concepts developed in the Kunihiro and Ohno model and will be fundamental to our work.

At steady-state, the capture and emission occur at the same rate which means $df_t/dt = 0$. Thus, the trapped charge remains constant and, consequently, the BG voltage, designated as V_B, will also remain constant. On the other hand, a change in the occupancy ratio entails a variation of the amount of trapped charge, and inevitably a $\Delta V_B \neq 0$. According to the previous assumption, where the epitaxial layer is deemed as a capacitance, these relations come naturally as a first order dependence described as

$$\Delta V_B = \frac{y_B}{\epsilon_s} \Delta Q_B, \tag{1.6}$$

$$\Delta Q_B = -eN_{DD}\Delta f_t, \tag{1.7}$$

where y_B and ϵ_s are the thickness and permittivity of the epitaxial layer, respectively, N_{DD} is the sheet trap density and e is the elementary charge.

Assuming a non-degenerate regime, one can describe the concentration of free electrons in the BG by a Maxwell-Boltzmann distribution deviated from the steady-state, n_0, as

$$n = n_0 \exp\left(\frac{e\Delta V_B}{k_B T}\right). \tag{1.8}$$

This is the same to consider the variation of the Fermi-level in the material when excited as $\Delta F = e\Delta V_B$.

Substituting eqs. 1.6, 1.7 and 1.8 into eq. 1.2 we obtain the state equation

$$\frac{d\Delta f_t}{dt} = \omega_0 f_{t0}\left(1 - f_{t0} - \Delta f_t\right)\left\{\exp\left(\frac{-e^2 N_{DD} y_B \Delta f_t}{\epsilon_s k_B T}\right) - 1\right\} - \omega_0 \Delta f_t, \tag{1.9}$$

where f_{t0} is the occupancy ratio at the steady-state defined as

$$f_{t0} = \frac{n_0 c_n}{e_n + n_0 c_n} \tag{1.10}$$

and ω_0 is the characteristic frequency of the system defined as

$$\omega_0 = e_n + n_0 c_n. \tag{1.11}$$

Before moving on, we need to address an important approximation made by Kunihiro and Ohno that goes unmentioned in the original paper. In fact, the result they arrived at is different from the one we achieved in eq. 1.9, following their exact steps. The difference lies in the first term of the right side of the equation, where they obtained $\omega_0 f_{t0}\left(1 - f_{t0}\right)(...)$, while we get $\omega_0 f_{t0}\left(1 - f_{t0} - \Delta f_t\right)(...)$. This means, they considered the contribution of Δf_t in the sum, $1 - f_t - \Delta f_t$, vanishingly small, which is in our understanding valid only when the deviation from the steady-state is very small. Since this is the same approximation made when deriving the emission coefficients from the SRH model, we consider their approximation valid, and apply it for the following calculations, which will allow us to reach their result.

For now, eq. 1.9 is still somewhat enigmatic, however, we can replace the trap parameters by the following circuit parameters:

$$J_{SB} = eN_{DD}\omega_0 f_{t0}(1 - f_{t0}), \tag{1.12}$$

describing the current density and

$$R_B C_B = \omega_0^{-1}, \tag{1.13}$$

where R_B is a resistance predicted by the SRH model (implemented in the equivalent circuit, see Fig.1.4) and C_B comes naturally as

$$C_B = \frac{\epsilon_s}{y_B}. \tag{1.14}$$

From here it is extracted the elegant circuit equation, achieved by Kunihiro and Ohno, describing the trapping mechanism in HJFETs, as

$$\frac{d\Delta Q_B}{dt} = -J_{SB}\left\{exp\left(\frac{e\Delta Q_B}{C_B k_B T}\right) - 1\right\} - \frac{\Delta Q_B}{R_B C_B}. \tag{1.15}$$

The first term of the right side of eq. 1.15 adopts the equivalent form of a current through a diode, describing the capture mechanism, while the second term depicts a current through a resistor, describing the emission mechanism. This difference between the mathematical representation of both processes direct us to the asymmetric time constants mentioned in section 1.1.

The next imposing question is, how an external excitation will influence V_B. In other words, what is the driving signal of the state equation, that is responsible for the dynamic system's forcing response. We know that it has to be dependent on the drain voltage variation, since this is the parameter that they defended as responsible for the trap charging in real devices. However, in their paper, Kunihiro and Ohno state that ΔV_B - the input variable of the state equation - is directly proportional to Δv_{DS} (a variation of the drain to source voltage) at high frequencies and DC, whose proportionality constants are, respectively,

$$\alpha = \frac{C_{BD}}{C_{BD} + C_{SB}},$$
$$\beta = \frac{R_{SD}}{R_{SD} + R_{BD}}, \tag{1.16}$$

but say nothing on the remaining frequency bandwidth. Therefore, we are left to what seems to be just the dynamical system's natural response describing the entire trapping mechanism. We are, consequently, unable to simulate the traps' occupancy variation, when some external potential is applied to the device. The authors materialized this system in an equivalent circuit, consisting of a capacitance, describing the traps ability to store charge, in series with a diode in parallel with a resistor, obtained by the state

equation. The remaining components of the equivalent circuit pictured in Fig. 1.4 results from the initial assumptions made by the authors.

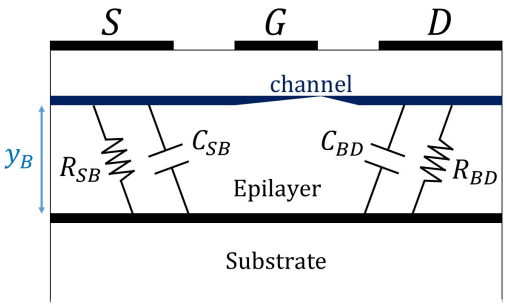

Figure 1.3: Schematic diagram of substrate parasitic elements in a HJFET. y_B is the distance between the channel and the pseudo-backgate. Redrawn from [2].

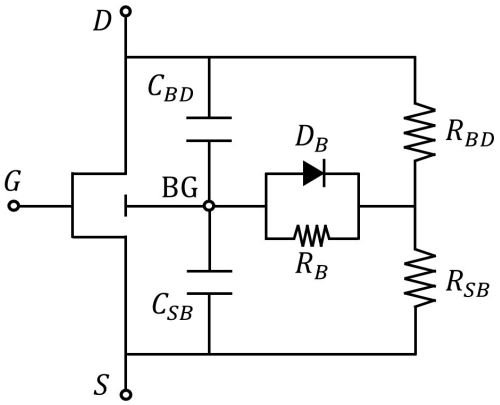

Figure 1.4: Equivalent circuit model with pseudo-backgate terminal. Redrawn from [2].

Despite this apparent inaccuracy of the Kunihiro and Ohno model, some concepts are and were worth exploring. The circuit of Fig. 1.4 has been replicated in more recent articles under the equivalent form of Fig. 1.5, obtained by calculating the Thévenin equivalent. The advantage of this circuit lies in the simplicity on which one can impose two different time constants, mimicking the trapping and detrapping difference, in modern HEMT models.

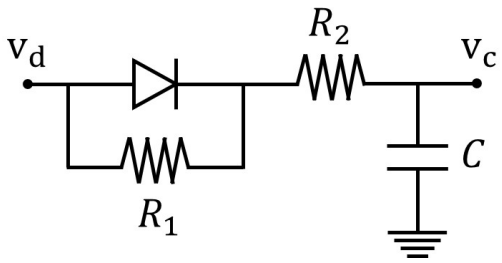

Figure 1.5: Trapping equivalent circuit. Redrawn from [3].

In Fig. 1.5, v_C is equivalent to the Backgate potential, and v_d represents the drain potential.

It remains to know, how the BG voltage will influence the macroscopic behaviour of the HJFETs. At the time, many defended the idea that the trapped charge below the channel acts as a virtual-gate that reduces the gate potential, known as "self-backgating" [2]. The latter, can be mathematically described by a shift to the transistor's threshold voltage, like

$$V_{th} = V_{th0} - \gamma V_B, \tag{1.17}$$

where V_{th0} is the threshold voltage without the BG and γ is a Backgate-transconductance parameter. Fig. 1.6 shows the consequence of a threshold shift for the drain current.

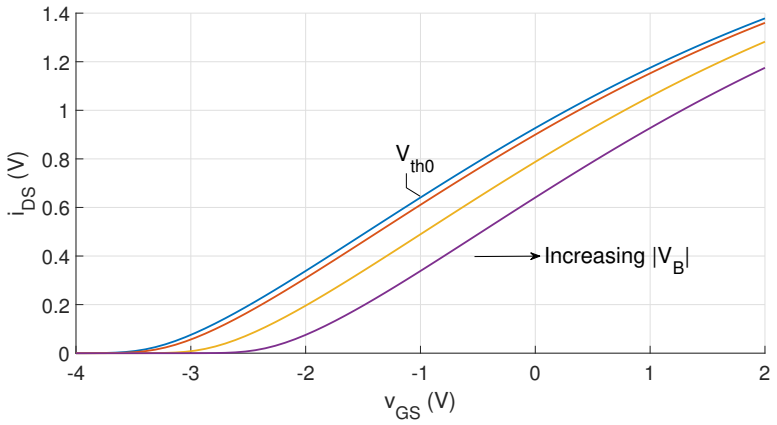

Figure 1.6: Simulation of the threshold variation for increasing $|V_B|$ @ $v_{DS} = 10$ V. The parameters used in this simulation are from a different work, so the values obtained here are just a crude approximation.

Currently there is no widely accepted theory in the literature, that we are aware, regarding the exact nature of traps, their location in the device and the origin of the charge that fills them. On this basis, the next model presents a more general approach to the trapping mechanism, making no assumption regarding the trap's position. Furthermore, the state equation of the next model is much more explicit, making us able to distinguish the natural from the forcing response of the dynamical system, which will allow us to apply this next model in our simulations.

1.2.3 The Rathmell and Parker Model

The proposed model of Rathmell and Parker begins from a completely general approach to trapping in semiconductors. It could be described as a particular case of the SRH model.

The same notation used in section 1.2.1 is applied next. Let N_t be the concentration of traps (cm^{-3}) in the material, so that $n_t = f_t N_t$ is the concentration of trapped electrons and $p_t = (1 - f_t)N_t$ is the concentration of trapped holes. This notation is only valid for thermal equilibrium where the same Fermi level describes both electron and hole concentrations. As assigned in Fig. 1.2, processes (a) and (b) are more likely to occur when the trap level is closer to the conduction band, $E_c - E_t < E_t - E_v$. Here, the steady-state distribution is dominated by the balance between the electron capture and emission processes. Thus, it is considered as possible states of the SRH centers, either neutral or positive (denominated as donor-like trap). Hence, the trapped charge by the

SRH centers is treated in terms of trapped holes,

$$\frac{dp_t}{dt} = (b) - (a) + (c) - (d) \approx (b) - (a) = c_n(N_t - p_t)n_1 - c_n p_t n$$

$$= c_n \left[(N_t - p_t) N_c exp\left(\frac{E_t - E_c}{k_B T} \right) - p_t N_c exp\left(\frac{F - E_c}{k_B T} \right) \right]$$

$$= \omega_{0n} \left[(N_t - p_t) - p_t exp\left(\frac{F - E_t}{k_B T} \right) \right], \tag{1.18}$$

where

$$\omega_{0n} = c_n N_c exp\left(\frac{E_t - E_c}{k_B T} \right). \tag{1.19}$$

The exactly same reasoning is applied to the case where the trap level is closer to the valence band (denominated as acceptor-like trap). The dominant processes here are (c) and (d); thus, the rate of trapped charge is given in terms of trapped electrons, like

$$\frac{dn_t}{dt} = \omega_{0p} \left[(N_t - n_t) - n_t exp\left(\frac{E_t - F}{k_B T} \right) \right], \tag{1.20}$$

where

$$\omega_{0p} = c_p N_v exp\left(\frac{E_v - E_t}{k_B T} \right). \tag{1.21}$$

Notice that ω_0 has units of frequency and both $E_v - E_t$ and $E_t - E_c$ represent an activation energy, i.e. a required energy-leap to ionize the trap. Knowing that N_v and N_c are proportional to $T^{3/2}$ [21] and that v_{th} is proportional to $\sqrt{T}$ [17], we can generalize eqs. 1.19 and 1.21 as

$$\omega_0(T) = BT^2 exp\left(-\frac{E_{act}}{k_B T} \right) \tag{1.22}$$

where B is a proportionality constant. As we can see, eq. 1.22 has the form of a modified Arrhenius equation, typically used to describe occupancy rates of crystal vacancies. If we compare eqs. 1.19 or 1.21 with the eqs. 1.5, it becomes clear that $\omega_0(s^{-1})$ is the emission rate coefficient. Which also means, that its inverse will be the emission time-constant, $\tau_e = \frac{1}{\omega_0}$. Given the relation between the temperature and the emission process, we say that the emission mechanism in SRH centers is thermally activated, meaning that thermal fluctuations induce charge emission from the traps. This temperature-emission relation, described in eq. 1.22, is the basis for several techniques, like deep level transient spectroscopy [22] or dynamic transconductance measurements [23], dedicated to the extraction of the trap parameters, namely, the capture cross-section and the activation energy.

It is worth noting that, ω_0 grows exponentially with the position of the deep-level trap in the energy spectrum, depicted by E_t. This means, that the emission-related term, $\omega_{0n}(N_t - p_t)$, for the donor-like case (we could infer the same for an acceptor-like trap), will also follow this dependence with the trap energy-level position. As a consequence,

larger energy intervals between the conduction band minimum and the deep-level trap will result in (exponentially) lower emission rates, and consequently (exponentially) larger emission time-constants. On the other hand, if we analyse the capture-related term, $\omega_{0n} p_t \exp\left(\frac{F-E_t}{k_B T}\right)$, we can see that the product, $\omega_{0n} \times \exp\left(\frac{F-E_t}{k_B T}\right)$ will eliminate the E_t dependence, since this term disappears from the exponential argument. This is curious, because implies that the capture time-constants of shallow and deep-levels should be practically alike, assuming the same conditions and a similar capture coefficient. Such, comes with a profound revelation because, nowadays, we can achieve gigahertz signals in doped semiconductors - containing shallow impurities - without any trapping manifestation. This indicates, that the capture and emission processes, in these devices, must occur faster than nanoseconds to pass unnoticed. A direct consequence of this is that the capture transient illustrated in Fig. 1.1 is not real, in the sense that we can not measure it with modern equipment, instead we are only able to see the steady-state of the system after the drain potential is raised.

Note that the previous reasoning is based on rough estimates, serving as a conceptual framework to understand the extent of time asymmetry between the two processes and the importance of detrapping, at deep-levels, to observe memory effects. This asymmetry was also visible in the Kunihiro and Ohno model derivation of the trapping process, described as a diode in parallel with a resistor. So, it becomes now visible, that this concept which we emphasize in this work, emerges naturally from the SRH model. This is relevant because it corroborates the idea of GaN HEMTs hosting deep-level traps, and because it helps us understand the underlying phenomena during these devices' operation.

Now, just as made in the Kunihiro and Ohno model derivation, it is found a motivation to these equations by applying an analogy between the physical phenomena and electronic components. Assuming that SRH centers behave like capacitances, we can obtain a proportional relation between the trap charge and the trap potential expressed as

$$\begin{aligned} q n_t &= C_{nt} v_{nt}, \\ q p_t &= C_{pt} v_{pt}, \end{aligned} \tag{1.23}$$

where $C_{(n,p)t}$ is the trap capacitance. Also, the time derivative of the trapped charge, described by eqs. 1.18 and 1.20, is directly proportional to the time derivative of the trap potential. Therefore, we can generalize our notation and obtain

$$i_t = C_t \omega_0 \left[V_0 - v_t - v_t \exp\left(\frac{e V_I}{k_B T}\right) \right] \tag{1.24}$$

where V_0 is the maximum capacitance potential and V_I is a behavioural equation (that will be defined latter on) that relates the Fermi level with an external potential. Strictly speaking, these SRH centers behave not as capacitances but as transcapacitances, since the charging and discharging processes depend on both v_t and V_I. According to Rathmell and Parker [4], the trapping equivalent circuit emerges naturally from eq. 1.24 as

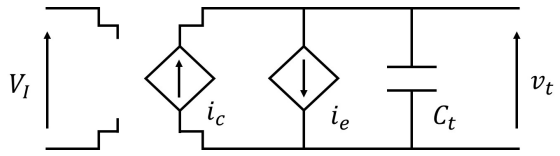

Figure 1.7: Trapping equivalent circuit. Redrawn from [4].

where the total trap current is given by the sum of the capture current and the emission current, defined respectively as

$$i_c = C_t \omega_0 v_t \exp\left(\frac{eV_I}{k_B T}\right) \tag{1.25}$$

$$i_e = C_t \omega_0 v_t \left(V_0 - v_t\right) \tag{1.26}$$

To conclude this derivation, eq. 1.24 can be re-written, considering the direct proportionality between the current and the time derivative of the voltage across a capacitance, as

$$\frac{dv_t}{dt} = \omega_0 \left[V_0 - v_t - v_t \exp\left(\frac{eV_I}{k_B T}\right)\right]. \tag{1.27}$$

Eq. 1.27 is the general representation of the dynamical system that describes the trapping mechanism, whose forcing response is dictated by the driving variable V_I. When $V_I = 0$, the Fermi-level overlaps the trap deep-level, which means there is an approximately 50% chance (we must also take the degeneracy factor into consideration) of the trap being filled. When $V_I > 0$, the capture rate increases, which is expected given the fact that the Fermi-level is now above the trap level. Depending on the defect type, the polarity of v_t will change. In the case of a donor trap, $0 \leq v_t \leq V_0$, and for an acceptor, $V_0 \leq v_t \leq 0$. For both cases, when the trap is completely full, then $v_t = 0$.

To finish the state-of-the-art we now explain the general description of a memristor and its unique characteristics.

1.2.4 Memristor

The study of two-terminal electronic devices typically starts with the measure of a finite number of admissible signal pairs in the $(v(t), i(t))$ plane to infer an approximation of the device constitutive relation - collection of all admissible signal pairs. Over time, three passive devices have been found whose constitutive relations were a linear relation between the (v, i), $\left(v, \frac{di}{dt}\right)$ and $\left(\frac{dv}{dt}, i\right)$ pairs. Due to their valuable linear behavior under certain operation domains, these devices, namely, the resistor, the inductor and the capacitor were widespread in countless applications laying the foundations of electronics [24].

Introducing two fundamental circuit variables, namely, $q(t) = \int_{-\infty}^{t} i(\tau)d\tau$ and $\phi(t) = \int_{-\infty}^{t} v(\tau)d\tau$, commonly known as charge and flux (these variables do not need to be

associated to a physical meaning, like the charge on a capacitor or the magnetic flux on a coil) we can re-describe the inductor and the capacitor pair as (ϕ, i) and (v, q), accordingly. The resistor pair remains (v, i) and the pairs (q, i) and (ϕ, v) are not considered constitutive relations [25] since both elements of each pair describe the same physical quantity.

We are seeing here that, by using four variables, we can describe the three key elements of electronics. But, a pair that constitutes a possible constitutive relation remains unassigned. Based on a preoccupation for completeness, Leon Chua presented to the world in his renown paper of 1971, a fourth passive element described by the (ϕ, q) pair, and coined it as memristor, a contraction of memory with resistor [26]. Defined as a two-terminal device, its constitutive relation is $M(\phi, q) = 0$ in the $\phi - q$ plane.

The memristor equation is commonly derived by an axiomatic approach, that we will present next. Let

$$\varphi = f(q). \tag{1.28}$$

Applying the derivative chain rule, we obtain

$$\frac{d\varphi}{dt} = \frac{df(q)}{dq}\,\frac{dq}{dt}. \tag{1.29}$$

Remembering the charge and flux definition presented above, eq. 1.29 leads to

$$v = \frac{d\varphi}{dq} i. \tag{1.30}$$

If the constitutive relation in the $\phi - q$ plane is a straight line with slope equal to M (called memristance), then our memristor is said to be linear, and eq. 1.30 is simply Ohm's law, $v = M\,i$. This means we are not able to distinguish a linear memristor from a resistor, which is not very interesting. On the other hand, if the slope is dependent on q, then the memristor is said to be charge-controlled and the constitutive relation assumes the form

$$\varphi = \hat{\varphi}(q) \tag{1.31}$$

equivalent to

$$v = M(q)\, i$$

$$M(q) \triangleq \frac{\hat{\varphi}}{dq}. \tag{1.32}$$

Eq. 1.32 can be interpreted as a charge-controlled memristor that behaves as a linear resistor, whose resistance depends on an instantaneous charge value that "remembers" past events of input current $\left(q = \int_{-\infty}^{t} i(\tau) d\tau\right)$ [24].

One can also analyse the memductance, contraction of memory and conductance, when describing a flux-controlled memristor, whose constitutive relation can be expressed as

$$i = G(\varphi)\, v. \tag{1.33}$$

A later work of Leon Chua [27] generalized the memristor definition to memristive systems and devices. In its simplest form, one can state that a one-port memristive system is a special case of the general class of dynamical systems, defined as

$$\dot{\mathbf{x}} = f\left(\mathbf{x}, u, t\right) \tag{1.34}$$

$$y = g\left(\mathbf{x}, u, t\right)\, u \tag{1.35}$$

where u and y are the input and output of the system, respectively, and $\mathbf{x}$ denotes the state of the system. The function $f : \Re^n \times \Re \times \Re \mapsto \Re^n$ is a continuous n-dimensional vector function and $g : \Re^n \times \Re \times \Re \mapsto \Re$ is a continuous scalar function. It is assumed that the state equation (eq. 1.34) has a unique solution for any initial state $x_0 \in \Re^n$.

Memristive systems possess two distinctive features that separated them from a broader class of dynamical systems, as Leon Chua demonstrates in [27]. One of them is the pinched characteristic of the I-V curve at the origin, i.e. when $u = 0$ then $y = 0$ regardless of the system state, $\mathbf{x}$. This can be easily proven considering that $g\left(\mathbf{x}, 0, t\right) \neq \infty$. Thus, $g\left(\mathbf{x}, 0, t\right) \times 0 = 0$ is always true for any memristive system. The second signature of these systems is the dependence of the hysteresis lobe area on the frequency of some input periodic signal. It can be shown that above a certain frequency, the lobe area decreases monotonically for increasingly higher frequencies until it vanishes. To prove this, let us consider a time-invariant memristive system that is bounded-input bounded-state stable, and we excite it with a periodic signal of frequency ω. From this and the continuity of the function f, we can express, for any bounded input, eq. 1.34 as a Fourier series, described by

$$f(x, u) = \alpha_0 + \sum_{\substack{k=-N \\ k\neq 0}}^{N} \exp\left(jk\omega t\right) \alpha_k, \tag{1.36}$$

where N is some integer, α_0 and α_k are the Fourier components. Substituting eq. 1.36 in eq. 1.34 we obtain

$$x(t) = x(t_0) + \int_{t_0}^{t} f\left(x\left(\tau\right), u\left(\tau\right)\right) d\tau$$

$$= x_0 + \alpha_0(t - t_0) + \sum_{\substack{k=-N \\ k\neq 0}}^{N} \frac{\exp(jkwt) - \exp(jkwt_0)}{jkw}\alpha_k. \tag{1.37}$$

Since $x(t)$ is bounded, as we imposed on the beginning of this derivation, then $\alpha_0 = 0$, otherwise, this function would grow indefinitely over time. The numerator of the third term of the right side of eq. 1.37 is also bounded (its maximum possible value is $2\alpha_k$). Hence, if we increase the frequency of excitation up to infinity, this fraction will tend to zero, due to the denominator indefinite growth, and, consequently, $x(t)$ will tend to x_0. This means, that the amplitude of oscillation of the state variable, for a memristive

system under periodic excitation with increasingly higher frequency, will decrease to zero, up to the point where the state variable remains constant. Since the double-value Lissajous figure property (hysteresis) is a consequence of the state variable variation, then, as we increase the frequency, after some critical value, we will observe a reduction of the hysteresis lobe area [27]. Fig. 1.8 illustrates both fingerprints of a memristive device.

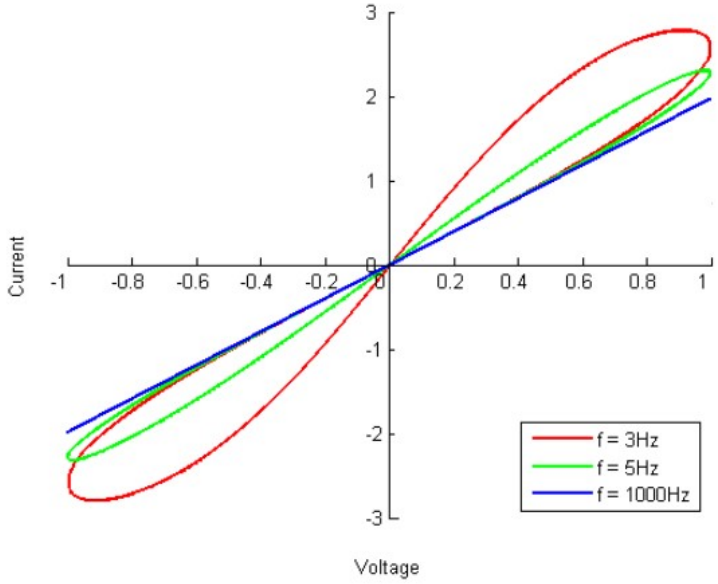

Figure 1.8: Illustration of a typical memristor I-V curve. Obtained from [5].

1.3 Objective

As mentioned in the previous section, the objective of our MSc thesis is to prove that GaN HEMTs are memristive systems. In short, any system is said to be memristive if it presents the two following fingerprints [28],[29]:

- When driven by a periodic signal that passes through zero, the device must exhibit a pinched hysteresis loop in the voltage-current plane, assuming the response is periodic;
- Starting from some critical frequency, the hysteresis lobe area should decrease monotonically as the excitation frequency increases;

In this framework two goals are set, particularly, (i) to prove physically and (ii) experimentally that the GaN HEMT channel affected by drain-lag can be described as a memductance, whose state variable is the trap potential.

1.4 Synopsis

Our contribution to this field of research is divided in two distinct parts: the first, in chapter 2, is dedicated to the numerical simulation of the models presented in the state-of-the-art, to infer about the influence of deep-level traps in a modern behavioural model of GaN HEMTs; in the second, chapter 3, we observe and measure the memristive characteristics, proving the influence of deep-level traps, using a commercial GaN HEMT, with focus on the observation of hysteresis and pinching at the origin of the I-V curves.

Chapter 2

Dynamic Model

The dynamic behavior seen in GaN HEMTs - drain lag - is thought to be mainly caused by trapping effects. Inspired by this phenomena, we will construct a dynamic model, where the drain to source voltage, v_{DS}, is the input; the drain to source current, i_{DS}, is the output; and the space-state will be defined by a single variable, related with the trapping potential.

We begin this chapter by defining and analysing our state variable, starting from the Rathmell and Parker model described in sec. 1.2.3.

2.1 Trapping Voltage

Given the purpose of this work, the trap potential described in eq. 1.27 is not an adequate way to describe the state variable. According to the Rathmell and Parker model, the trap potential is zero when the trap is full and V_0 when entirely empty. These potential limits are a consequence of our conception of charge in SRH centers, given that we consider them as either donors or acceptors. This implies that the charge capture acts as a process to neutralize the trap (impurity). Apart from the counter-intuitive notion - the trap potential decreases with charge capture - this variable takes into account the nature of the trap (donor-like or acceptor-like). Therefore, we introduce a new variable, designated as effective trap potential, v_T, defined as

$$v_T = |V_0 - v_t|. \tag{2.1}$$

The effective trap potential is zero when the trap is empty and maximum, with some positive scalar, when the trap is full, and allow us to ignore the trap nature. This is relevant because it removes the responsibility of assuming something we have no conclusive evidence of.

The equation of motion of the effective trap potential is

$$\frac{dv_T}{dt} = \omega_0 \left[-v_T + (V_0 - v_T) \exp\left(\frac{eV_I}{k_B T}\right) \right]. \tag{2.2}$$

Where V_I is a linear function of the gate and drain potential [30]

$$V_I = k + k_g v_{GS} + k_d v_{DS} \tag{2.3}$$

where k, k_g and k_d are parameters of the system. Depending on the type and location of the traps, these parameters will have different signs and amplitudes. By manipulating

their values, we are able to control how the terminal potentials will influence the capture rate. As we mentioned in the beginning of this work, gate-voltage variations no longer cause gate-lag in modern devices, therefore we set $k_g = 0$. On the contrary, when v_{DS} increases, so must the capture rate in order to represent the drain-lag phenomena, therefore $k_d > 0$. Lastly, the choice of k was made under the assumption that, for $v_{DS} = 0$, the traps should be mostly empty, hence $k < 0$.

Commonly, memristive systems are studied using bipolar periodic signals [29]. However, since we wish to compare these simulations with real measurements, we should use similar inputs for both cases. Due to the structure of HEMTs, we must be very careful when applying negative voltages to the drain terminal, otherwise we risk damaging the device, as we will see in the next chapter. In theory, we just need a signal that passes through zero, to observe the pinched characteristic at the origin, and that is periodic, within a reasonable range of frequencies, to achieve a visible hysteresis. Therefore, we use an input signal described as

$$v_{DS} = \frac{A}{2} + \frac{A}{2} \sin(2\pi f t) + V_{DSmin} \tag{2.4}$$

where V_{DSmin} is the minimum v_{DS} voltage (a slightly negative value), A is a constant related to the amplitude of oscillation and to the average voltage, f is the frequency of excitation and t the time vector.

The initial condition, at which we start our integration, is very important because it will influence the transient response and, consequently, its accuracy, relevant when we compare these simulations with real measurements. Notice that selecting the value of $v_T(t = 0)$ in our simulations is the virtual equivalent to set the quiescent value of v_{DS} on a real setup. We can assume this because the only external parameter, that we are considering able to be able to change the trap state, is the drain to source voltage. Further, any constant voltage applied results in some constant trap state. As a matter of fact, we can establish a map between these two variables $-v_T(t = 0) \mapsto v_{DSQ}-$ by comparing eq. 2.2 with the equation of motion of the circuit illustrated in Fig. 2.1.

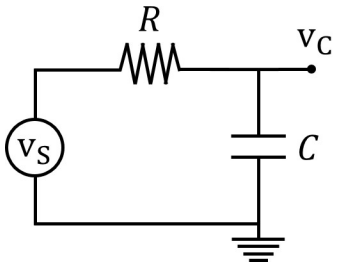

Figure 2.1: An auxiliary circuit whose dynamic can be compared to the Rathmell and Parker model.

The equation of motion of the auxiliary circuit is

$$\frac{dv_C}{dt} = \frac{v_S}{RC} - \frac{v_C}{RC}. \tag{2.5}$$

Comparing the terms of eq. 2.5 with the corresponding ones of eq. 2.2, we obtain the relations

$$\frac{1}{RC} \iff \omega_0 \left[1 + \exp\left(\frac{eV_I}{k_B T}\right)\right], \tag{2.6}$$

$$\frac{v_S}{RC} \iff \omega_0 V_0 \exp\left(\frac{eV_I}{k_B T}\right). \tag{2.7}$$

This comparison is helpful, because we know that the DC solution of the auxiliary circuit is reached when the capacitor is fully charged, $v_C = v_S$, being controlled by the time constant RC. Therefore, we can infer that the DC solution of our system will be

$$v_{T_{DC}} = \frac{V_0}{1 + \exp\left(\frac{-eV_I}{k_B T}\right)}, \tag{2.8}$$

and that the system's characteristic frequency is defined in eq. 2.6. Notably, the system's time-constant depends inversely with the exponential of V_I, which means that, as we increase V_I, the system reaches the DC regime much faster. With eq. 2.8, we are able to set the initial condition of our dynamic system for any v_{DSQ} of our choice.

Eq. 2.2 is an inhomogeneous first-order ordinary differential equation with very distinct time constants, that can be efficiently solved using MATLAB's function ode23s, a low order method to solve stiff differential equations. The solution is shown in Fig. 2.2 for several input-signal frequencies, described by eq. 2.4, using the parameters of table 2.1. The vertical axis represents the effective trap potential, and the horizontal axis, the time vector. The plot in Fig. 2.2 has its time vector normalized to compare the impact of the frequency on the curve shape.

Table 2.1: Parameters used in our simulation.

$A(V)$	$V_{DSmin}(V)$	$E_{act}(V)$	$V_0(V)$	$k(V)$	k_g	k_d	$T(K)$	$B(s^{-1}K^{-2})$
15	-1	0.5	1	-0.1	0	1.5×10^{-2}	300	4×10^6

From our simulations, two effects stand out: the amplitude of the oscillation decreases with frequency (see Fig. 2.2 and Fig. 2.3); and the amount of completed cycles during the transient response increases with frequency (see Fig. 2.3). Both can be understood as an outcome of fast trapping and slow detrapping. For instance, when we increase the input frequency, the emitted and captured charge per cycle decreases. Nevertheless, the capture is always the dominant process. As a consequence, the liquid charging per cycle is always positive, until it reaches the steady-state. After that, the amplitude of oscillation is such that the captured charge is equal to the emitted charge.

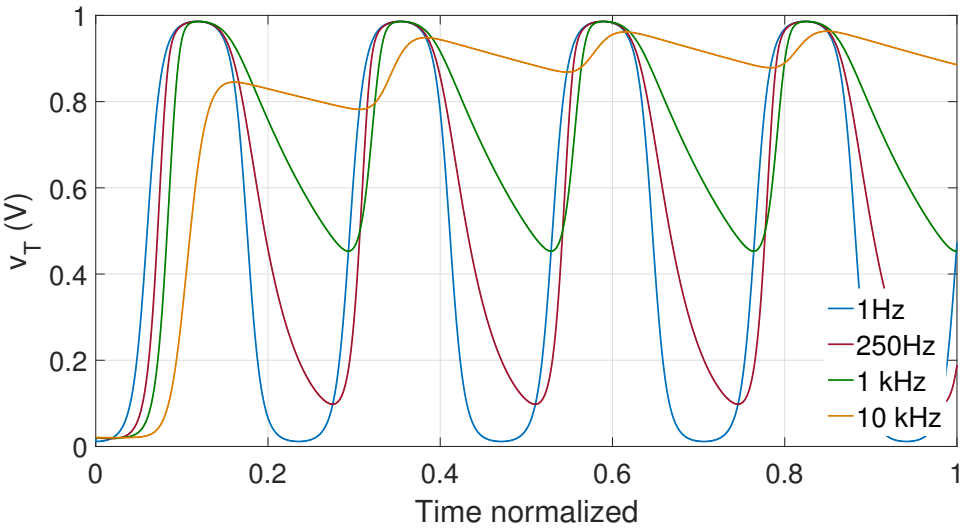

Figure 2.2: Numerical integration solution of eq. 2.2, @$v_{DSQ} = 0$.

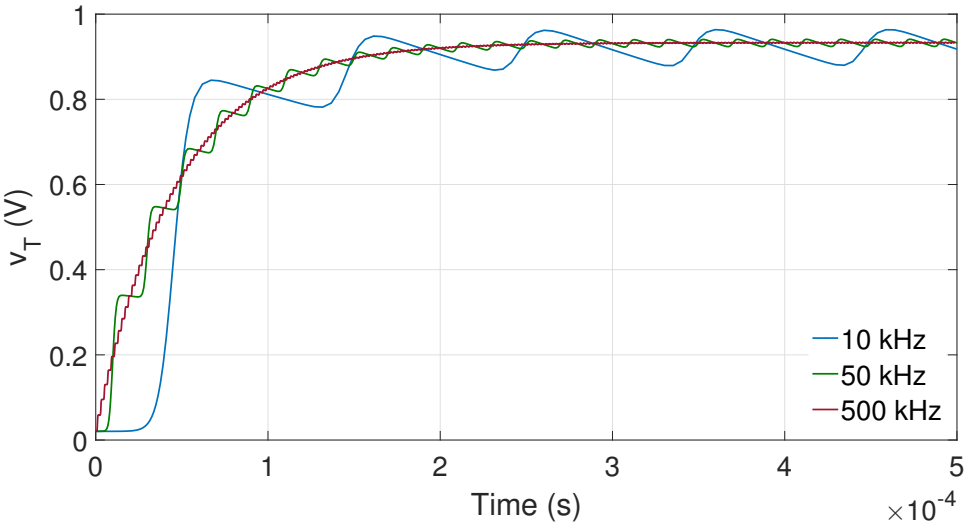

Figure 2.3: Transient behavior of our system for high frequencies, @$v_{DSQ} = 0$.

Another interesting point, more easily noticed in Fig. 2.2, is the transformation of the input signal. When we excite this system with a sine wave, it responds with an asymmetrical curve format. When the slope is positive, then the capture process dominates and the curve becomes more steep. On the other hand, when the slope becomes negative, the emission process dominates and the curve flattens. The slope in this case represents the rate of change of the trap potential, hence, we expect two different slopes respective to the growth direction of v_T, to represent the distinct rates associated to the capture and emission mechanism.

To conclude this section, we remark that, for increasingly higher frequencies, the amplitude of oscillation decreases, up to the point where it vanishes, better illustrated in Fig. 2.3. This property appears to be in line with the predicted features of a memristive system, as we saw before.

2.2 Nonlinear Device Model

To simulate a typical GaN HEMT, we use a nonlinear model, whose development was made considering the strong nonlinearities of these devices, like the triode to saturation zone transition, the current cut-off, the gate-channel diode conduction and the gate-channel breakdown [6]. The drain to source current is described in this model as

$$i_{DS}(t) = \frac{\beta v_{GS3}^2}{1 + \frac{v_{GS3}^{p_{lin}}}{V_L}} [1 + \lambda |v_{DS}(t)|] \tanh\left(\frac{\alpha_D}{v_{GS3}^{p_{sat}}} v_{DS}(t)\right) \tag{2.9}$$

where v_{GS3} acts as an intermediary to the v_{GS} function, defined as

$$v_{GS3}(v_{GS2}) = VST \ln\left[1 + \exp\left(\frac{v_{GS2}}{VST}\right)\right] \tag{2.10}$$

and

$$v_{GS2} = v_{GS1} - \frac{1}{2}\left(v_{GS1} + \sqrt{(v_{GS1} - VK)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2}\right) \tag{2.11}$$

where v_{GS1} is the FET's effective gate potential $-$ v_{GS} translated by the threshold voltage V_T $-$ defined as

$$v_{GS1}(v_{GS}) = v_{GS}(t) - V_T. \tag{2.12}$$

The $i_{DS}(v_{DS})$ dependence, pictured by the Curtice hyperbolic tangent function, simulates the transition from triode to the saturation region. An additional linear factor, λ, is added to account for the non null G_{ds} in saturation. The module (in $|v_{DS}(t)|$) was added to contemplate the symmetric property of the HEMT when $v_{DS} < 0$. The argument of the hyperbolic tangent has a scaling factor to reproduce the displacement of the knee voltage with v_{GS}[6].

Table 2.2: Parameters adapted from [6].

$\beta(A\,V^{-2})$	$VST(V)$	$VK(V)$	$\Delta(V)$	$V_L(V)$	$\lambda(V^{-1})$	$\alpha_D\left(V^{p_{sat}-1}\right)$	p_{sat}	p_{lin}
0.40	0.15	4	5	1.35	0.0056	0.40	-0.62	1

It remains now to bridge the gap between this model and the trap potential. We attain this by implementing the idea introduced by Kunihiro and Ohno, namely the backgate potential. We use an updated version of their work, particularly developed to model GaN HEMTs' operation, which we call the Threshold function.

2.3 The Threshold Function

The empirical relation between the threshold voltage and the effective trap potential, explored in [7], is modelled as

$$V_T[v_T(t)] = V_{T0} + \frac{1}{2}A_{V_T}\left\{1 + \tanh\left[K_{V_T}\left(v_T(t) - V_{V_T}\right)\right]\right\} \tag{2.13}$$

where V_{T0} is the expected threshold voltage when all traps are empty. A_{V_T}, K_{V_T} and V_{V_T} are parameters of our system.

Now, we can introduce eq. 2.13 into eq. 2.12 and re-write our dynamic system as a parametric function of the instantaneous values of v_{GS} and v_{DS}, whose threshold voltage coefficient is a function of the trap state [8],

$$i_{DS}(t) = f\{v_{GS}(t), v_{DS}(t), V_T[v_T(t)]\}. \tag{2.14}$$

Table 2.3: Parameters adapted from [7].

$V_{T0}(V)$	$A_{V_T}(V)$	$K_{V_T}(V^{-1})$	$V_{V_T}(V)$
-3.616628	3	1	2

2.4 Simulations

All simulations were made using the specified parameters in tables 2.1, 2.2 and 2.3. We tested five different frequencies, with some of them being on the same order of magnitude as the ones we will apply in our experimental work. We intend, with these simulations, firstly, to observe the memristive properties originated from the trapping manifestation and secondly, to set a reference point, that can help guiding us during the analysis of the experimental results. This is very important because, in a real device, there will be several non-related trapping effects, that are embedded in the measured output response,

and could be responsible for a part of the observed memory effects. Therefore, it is of great interest to us, to understand the I-V curves' distortion originated exclusively by trapping.

We begin by representing the ideal curve of our model whose threshold voltage is fixed at V_{T0}, in black, together with the first five periods of the output of a 1 kHz sine wave, in Fig. 2.4. The arrows point to the direction that v_{DS} is varying. The blue arrows indicate a transient regime and the black ones, the steady-state.

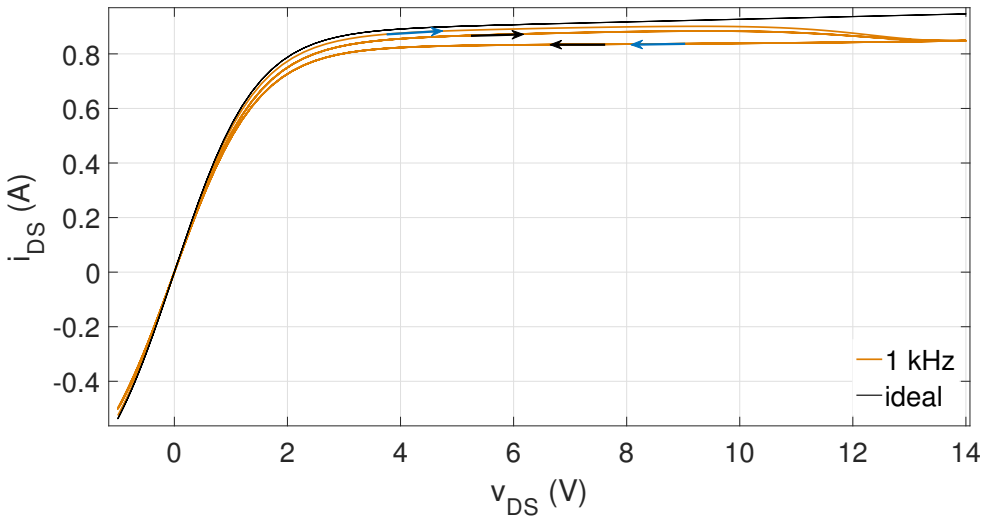

Figure 2.4: Simulation of the ideal case and the drain signal at 1 kHz, @$v_{DSQ} = 0$.

The first cycle presents the largest hysteresis lobe area. After that, we can infer that the system reached the steady-state, proved by the overlap of the four remaining cycles. According to our previous results - relating the impact of the frequency on v_T - we can expect that for higher frequencies we will observe additional lobes, a consequence of the extra cycles during the transient response of the system. This can indeed be observed in Fig. 2.5.

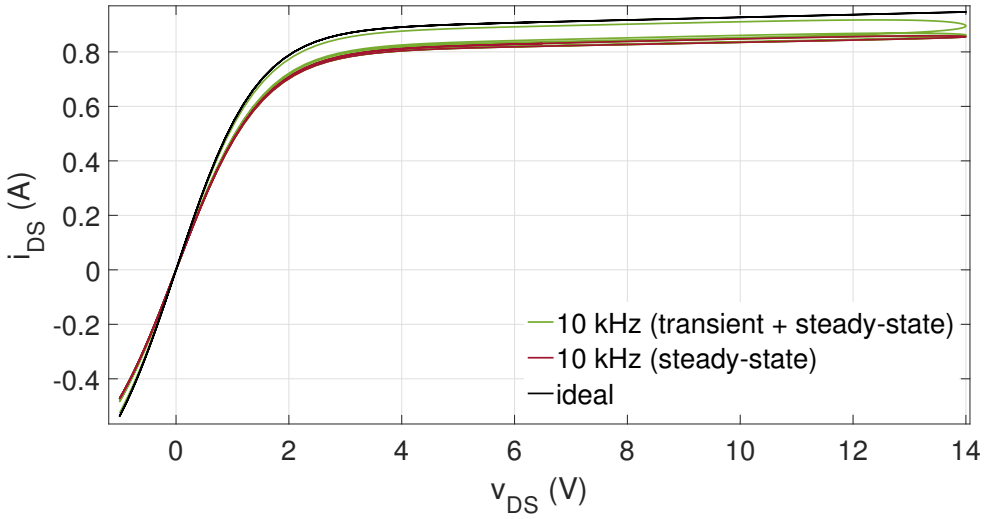

Figure 2.5: Simulation of the ideal case and the drain signal at 10 kHz, @$v_{DSQ} = 0$.

The effect of a different choice on the initial condition becomes visible when we compare $v_{DSQ} = 15$ V, pictured in Fig. 2.6, with $v_{DSQ} = 0$ V, illustrated in Fig. 2.5. Notice that we are able to significantly reduce the effect of the transient response just by starting with a higher v_{DSQ}, in this case equal to the maximum value of the input signal. This can be compared to a real device whose traps begin already pre-charged. In this case, the system experiences current collapse from the beginning, which, in turn, results in a quasi-static output signal. This phenomena will be further explored in the next chapter.

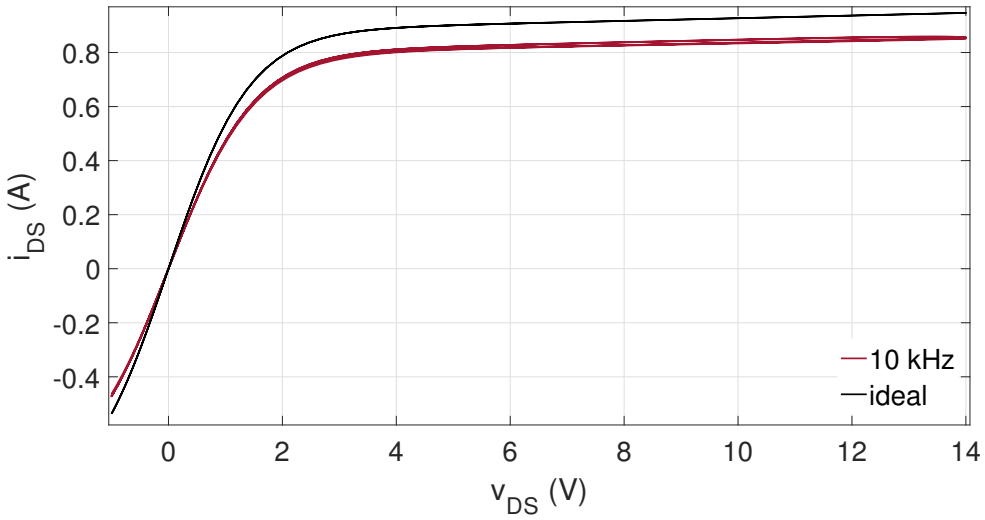

Figure 2.6: Simulation of the ideal case and the drain signal at 10 kHz, @$v_{DSQ} = 15$.

On the other hand, if we reduce the frequency below 1 kHz, we observe that the hysteresis lobe area reduces, up to the point it completely closes at 1 Hz. For this frequency, the capture and emission time-constants are much faster than the rate of change of v_{DS}.

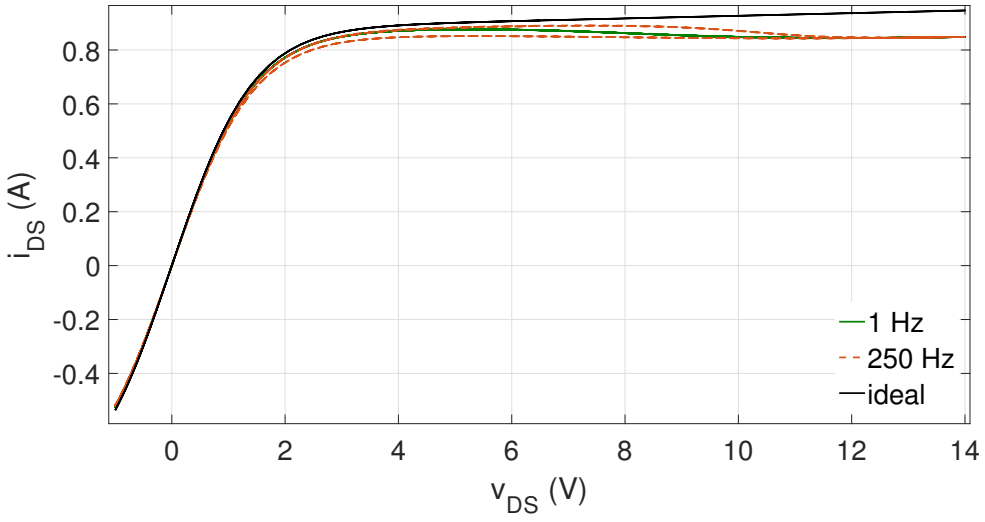

Figure 2.7: Simulation of the ideal case and the drain signal at 1 and 250 Hz, @$v_{DSQ} = 0$.

To conclude, we can see that all curves are indeed pinched at the origin. In fact, we can prove it, as we will demonstrate in the next section. Furthermore, it was demonstrated in this study that the state variable amplitude of oscillation for a periodic input decreases with frequency until it vanishes. This will manifest in the hysteresis lobe as a reduction of the area, which is expected from a memristive system.

2.5 Memristive Fingerprint

Let us now take a different approach to our model and analyse it from an analytical perspective. We begin by describing our system in the general form, assuming a constant v_{GS},

$$\begin{aligned} \dot{v}_T &= f\left(v_T, v_{DS}\right), \\ i_{DS} &= g\left(v_T, v_{DS}\right) v_{DS}, \end{aligned} \tag{2.15}$$

where the meductance is defined as

$$g\left(v_T, v_{DS}\right) = \frac{\frac{\beta v_{GS3}^2}{v_{plin}^p} \left[1 + \lambda |v_{DS}(t)|\right] \tanh\left(\frac{\alpha_D}{v_{psat}^p} v_{DS}(t)\right)}{1 + \frac{v_{GS3}}{V_L}} \Bigg/ v_{DS}. \tag{2.16}$$

According to the definition, the system must obey the condition $i_{DS}(v_T, 0) = 0$. This is the equivalent to say it must be pinched in the origin ($i_{DS} = 0, v_{DS} = 0$).

Since the memductance is indeterminate for $v_{DS} = 0$, which may compromise the previous condition, we must determine its value when $v_{DS} \to 0$, and find if it is bounded or not. For that, we apply L'Hopital's rule to the memductance definition, and arrive at a condition that must be verified, so that we can prove that $(i_{DS} = 0, v_{DS} = 0)$ belongs to our system, expressed as

$$\frac{di_{DS}(v_T, v_{DS})}{dv_{DS}}|_{v_{DS}=0} = \frac{\delta i_{DS}(v_T, v_{DS})}{\delta v_{DS}}|_{v_{DS}=0} + \frac{\delta i_{DS}(v_T, v_{DS})}{\delta v_T} \frac{dv_T}{dv_{DS}}|_{v_{DS}=0} \neq \infty, \quad (2.17)$$

which can be simplified to

$$\frac{di_{DS}(v_T, v_{DS})}{dv_{DS}}|_{v_{DS}=0} = \frac{\beta\, \alpha_D\, v_{GS3}^{2-p_{sat}}}{1 + \frac{v_{GS3}^{p_{lin}}}{V_L}}. \quad (2.18)$$

This means that the memductance is well defined in the origin, thus obeying the memristive definition.

We conclude this chapter by saying that our simulations and mathematical demonstrations prove that the model developed in this work possess the two fingerprints of memristive systems. Furthermore, a deeper understanding of the dynamical properties of GaN HEMTs was attained with the simulations made.

Chapter 3

Experimental Realization

In this chapter we completely change our approach towards the proof of memristivity in GaN HEMTs. We are now interested to pass from theory to experiment and prove that real devices possess memristive properties due to trapping.

An extensive calibration procedure was perfected throughout this work, revealing to be essential in order to understand our results. Given the importance of the calibration procedure, a deep analysis will be made on this topic. Additionally, due to the limitations of our equipment, plus the existence of additional effects on the device under test (DUT), we carefully optimize our input signal.

From previous experimental work done by our group, we estimate that most trapping happens around nanoseconds and most detrapping in milliseconds. Furthermore, we know that trapping effects are more pronounced at high voltages, most probably due to higher trap voltages reached, which in turn leads to increasing current collapse. Because of all this, we require input signals that are simultaneously fast and high: enough to distinguish different time constants and to observe clear evidences of memory.

Large power devices have large power dissipation, which means that a DC bias voltage would inevitably result in unwanted thermal effects, including damage on the device. In fact, fortuitous tests taken during our work suggest that GaN HEMTs change their intrinsic properties when subjected to high current peaks. Therefore, it is common practice to study these devices in high power conditions using pulsed measurements. The reason is that physical devices have non-zero heat capacity, so, raising the current to large values during short periods of time, proves to be insufficient to reach critical temperatures. Hence, one is able to study the large signal response of the transistor without burning it. On the other hand, since physical devices do not possess infinite thermal conductivity, they must be turn off for long periods of time to cool down. The ratio between the active time and off time for one period is designated as duty cycle. In our case, we will use 1% duty cycle for all tests. Pulsed measurements also provide us with the ability to study our DUT in iso-thermal and iso-dynamic conditions [31].

3.1 Setup Description

To create fast and high voltage pulses we use a power amplifier pulser head, called from now on just by Pulser, that amplifies the output signal of an AWG and feeds the DUT with the required power. A less powerful version of the main Pulser is used on the gate, also connected to the arbitrary waveform generator (AWG). The calibration of

both pulsers is done simultaneously using a set of predefined pulses. These are loaded into the AWG, amplified by the pulsers and read by a digital oscilloscope, using two probes, each connected to the output of each pulser. Additionally, a bias tee is employed between each pulser and the correspondent transistor's terminal, required to obtain stable impedances at high frequencies. Fig. 3.1 is a photography of our equipment in the typical configuration used for most measurements. The voltage probe does not show up for the purpose of clarity, but it is always attached directly to the HEMT fixture after the Bias Tee. This topology was originally designed for iso-dynamic and iso-thermal characterization of RF PAs, but it turned out to be also a useful topology for our work.

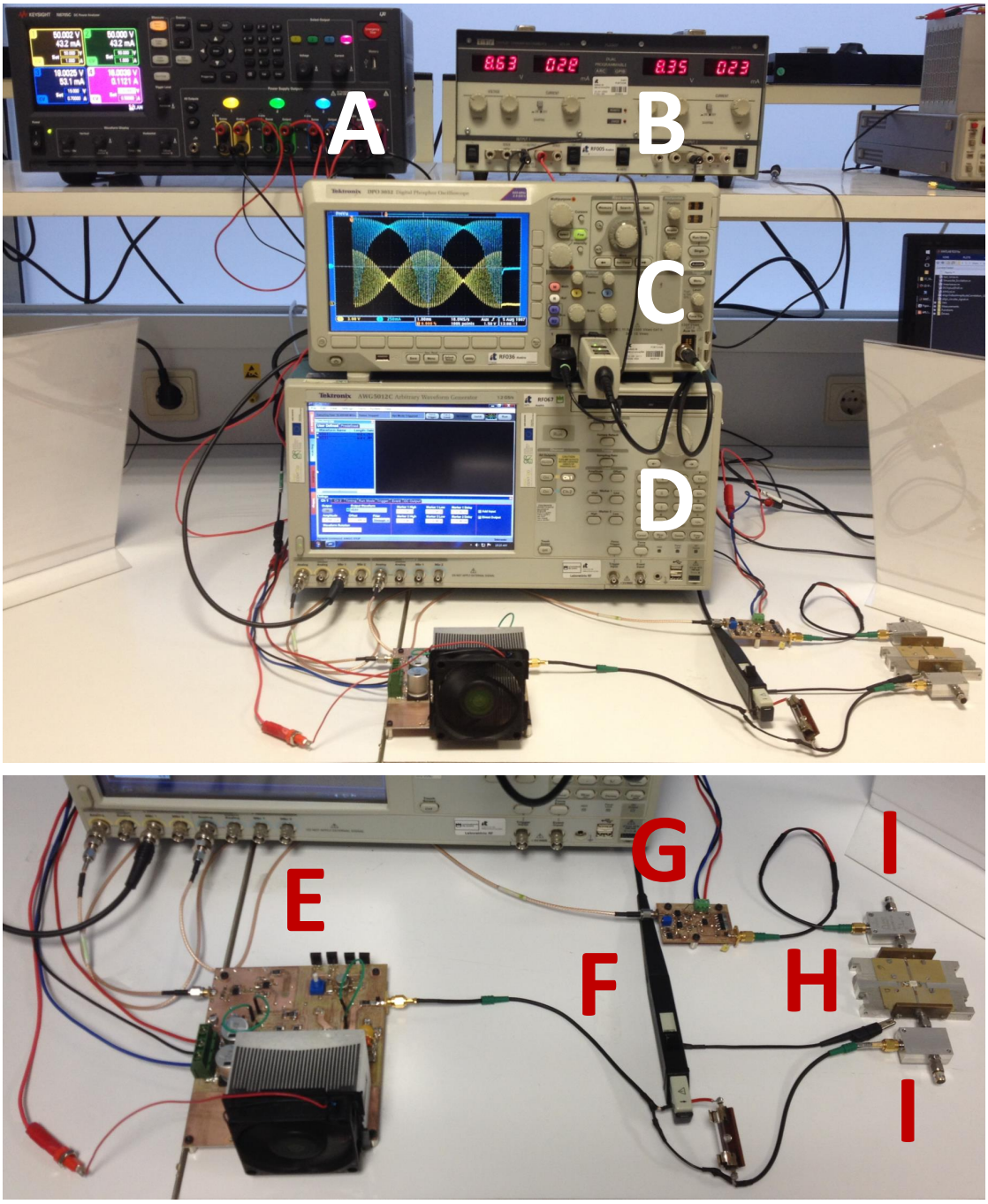

Figure 3.1: Setup. Above, view of the entire equipment used. Below, approximation on the pulsers, transistor and probe. A - N6705C DC Power Analyzer; B - PL320QMD DC Power Supply; C - Tektronix DPO3052 500 MHz, 2-Ch Digital Phosphor Oscilloscope; D - AWG5012C Arbitrary Waveform Generator; E - Drain Pulser; F - TCP0030A Current Probe; G - Gate Pulser; H - CGH27015 GaN HEMT from Cree and fixture; I - 8860SMF2-06 RF Bias Tee.

3.2 Input Signal

The structure of the input signal is very important to obtain good results. Like in the simulations we made, our excitation signal will also be a sine wave with the difference of now being preceded by a square pulse, designated as pre-pulse. Fig. 3.2 represents the general form of the optimized input signal, that we will employ in all our measurements.

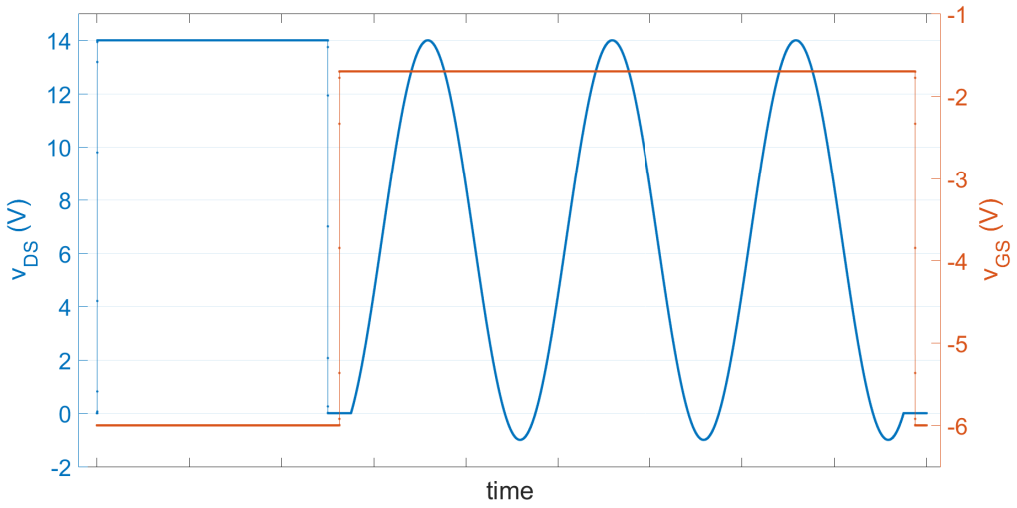

Figure 3.2: Representation of a general input signal.

The input signal is composed by two signals: the drain pulse and the gate pulse.

3.2.1 Drain pulse

The drain pulse is divided in two distinct components, namely, the pre-pulse and the drain signal, separated by short period where $v_{DS} = 0$.

The pre-pulse is a long square pulse applied to the drain terminal while the transistor is in the off state - the gate potential is below the threshold voltage. The pre-pulse inspiration comes from the method of double-pulsing [8] and is used to pre-charge the traps. We do with this technique the same we did when we selected the initial effective trap voltage in the simulation framework, discussed in chapter 2, namely, we impose an initial trap state to study the transient response of the dynamic system.

We know that the pre-pulse width, amplitude and even the time spacing between this and the drain signal are powerful parameters that, when changed, can tell us a lot about the trapping mechanism. In fact, previous studies led by our group, revealed that spanning the pre-pulse width, for a fixed amplitude, results in different trap states measured in the output signal, suggesting multiple capture time constants. Likewise, changing the

time spacing, with $v_{DS} = 0$, between the two parts of the v_{DS} pulse (pre-pulse + drain signal), for a fixed pre-pulse width and amplitude, changes the trap state measured in the output signal, most probably due to the variation of the time of effective detrapping. Thus, we can also infer about the detrapping time constants from this.

As we mentioned before, detrapping is much slower than trapping, which means that, after the pre-pulse charges all the corresponding traps for the applied drain voltage, the system will remain iso-dynamic during the drain signal for a short period of time, as long as v_{DS} does not surpass the pre-pulse amplitude - this would imply additional trapping. Even considering the possibility of short emission time constants, we can safely ignore this premiss, given that it constitutes a small fraction of the emission process. This concept will be useful during the analyses of our results.

For the purpose of this thesis, every pre-pulse will have a fixed width of 5 ms. This guarantees that all time constants associated to the capture process are satisfied. Remember that we wish to see clear evidences of drain-lag, so it is important to maximize the amount of trapping. After the pre-pulse, we apply the effective signal on v_{DS}, specifically, a sinusoidal wave limited between -1 V and 14 V. Contrarily to our simulations, we now apply negative values to the drain, meant to create clear evidences of a I-V curve pinched at the origin. It is important to notice that, when we apply negative values to v_{DS}, we must consider the existence of a structure equivalent to a Schottky diode between the gate terminal (anode) and the drain terminal (cathode). In GaN HEMTs, this diode has a maximum forward voltage around $\sim 1.8V$ [32]. Meaning that, if $v_{GS} - v_{DS} > 1.8$ V, then we will observe current flowing through the diode, which in turn results in potentially destructive gate currents. An additional problem must be contemplated that can be better understood by the following example. Suppose we polarize the gate with $v_{GS} = -1.7$ V, then, according to the previous condition, we can safely apply a drain voltage down to -3.5 V minimum. However, the HEMT structure is approximately symmetric, which means, there is no real difference between the drain and the source terminal. Thus, if we keep the source grounded and set $v_{DS} = -3$ V, then our transistor becomes polarized to $-1.7 - (-3) = 1.3$ V. This happens because the terminal with lower voltage becomes the source, thus, the previous source terminal converts into the drain terminal and vice-versa. Due to the large periods we are using, on the order of μs, currents generated by this polarization would certainly destroy the transistor by surpassing the critical temperatures. Therefore, with all these in mind, we conclude that $v_{DS} = -1$ V is the safe minimum, that allows the I-V curve a clear passage through the origin without compromising the device integrity.

As visible by Fig. 3.2, we only use three full periods because they showed to be enough to reach the steady-state of the device. Three frequencies will be preselected to excite our device, namely 250 Hz, 1 kHz and 10 kHz. Lower frequencies would result in unwanted thermal effects, while higher frequencies have similar outputs to the one observed at 10 kHz. Finally, we use a function of our oscilloscope to average 16 times the voltage and current samples for each frequency, in order to increase the signal-to-noise ratio.

3.2.2 Gate pulse

After the pre-pulse, a fast rising square pulse is applied to the gate terminal, with rise and fall times around $300ns$. When the pulse amplitude surpasses the threshold voltage of the GaN HEMT (a depletion mode transistor), ≈ -2.7 V, the device changes to the on-state, and current starts flowing if $v_{DS} \neq 0$. Here, the time spacing between the pre-pulse and the drain signal gains a new purpose. While $v_{DS} = 0$ we can safely step up v_{GS} without causing any pre-pulse current. Additionally, we must also consider the transient of our equipment when dropping from high voltages to zero in microseconds. It was seen that the recovery time of the Pulser and oscilloscope, after the pre-pulse application, is close to $30\mu s$. This transient affects particularly the starting point of the drain signal, causing it to deviate from zero.

After the drain signal, it is of critical importance that we end the gate pulse with $v_{DS} = 0$ to avoid inductance-induced voltage peaks. In order to understand the origin of these peaks it is, perhaps, more helpful to imagine the counter case, where v_{GS} is dropped while $v_{DS} \neq 0$. The problem lies in the presence of a bias tee preceding the transistor, particularly, the DC path of the bias tee, essentially made by an inductive element. When we drop abruptly the gate voltage, cutting-off the transistor, the existing current will cease very fast, which in turn, causes a voltage peak at the DUT's drain, proportional to the current time derivative. The major consequence of this peak is the possible infliction of damage to the transistor and the additional charging of the traps with unknown voltage amplitudes for unknown times, that may persist until the next active period of the input signal. Therefore, the gate pulse will be wider than the drain signal, allowing the device's current to discharge slowly through the bias tee inductance. This circuit element is also the motive why we imposed the drain signal starting from zero, otherwise, we would get fast variations of current, which would be responsible for voltage peaks that opposed the applied v_{DS}.

The gate quiescent value was set to $v_{GSQ} = -6$ V and the square pulse amplitude to -1.7 V. It was observed that higher amplitudes led to current pulses that exceeded the Pulser's ability to maintained them for the required time. Furthermore, high currents generate temperature rises that obscure the trapping effects. On the opposite side, lower gate potentials cause the conduction regime of the HEMT to switch from saturation to sub-threshold, while v_{DS} increases. We were able to visualize it due to the inflexion of the I-V curve at mid drain signal. This was seen as a clear example of the threshold voltage shift as trapping occurs. Despite the elegance of this effect it is relevant for this work, so no simulations are presented showing it.

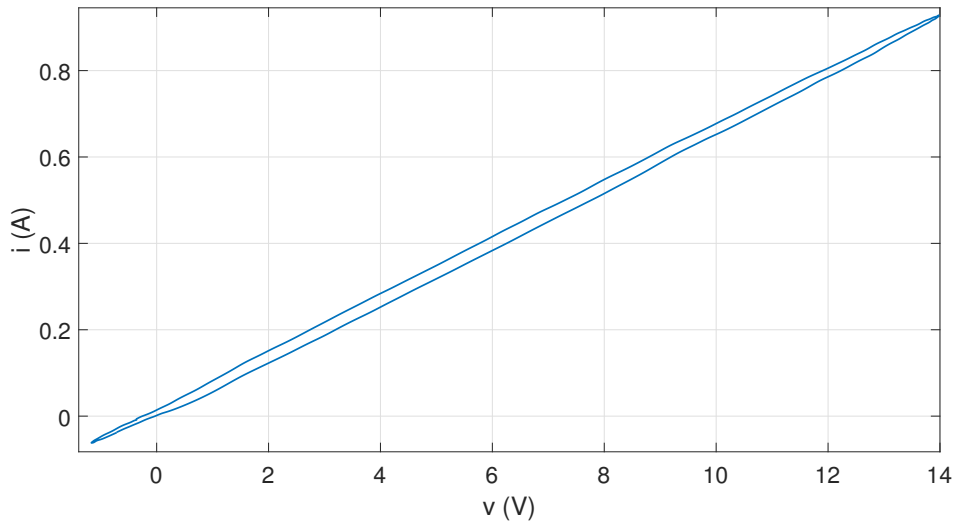

Figure 3.3: Confirmation of the delay present at our setup using a 15Ω resistor excited with at 750 Hz.

3.3 Calibration Procedure

Let us remember our initial purpose: Does the device exhibit a pinched hysteresis loop in the voltage-current plane? And does the hysteresis lobe area decreases monotonically as the excitation frequency increase?

Before we answer this question, we need to be completely sure that what we are measuring is exclusively effects of the transistor and there is no accountable influence from our setup. Such, can only be achieved with a rigorous calibration. We start our investigation by understanding possible sources of error, and one effect appear as critical, namely, time lag (or delay) between the current and the voltage measurement equipment (known as skew). The main concern respective to this problem is the alteration of the DUT's I-V curve hysteresis. A possible way to demonstrate the existence of this problem is the measurement of an I-V curve from a linear static system, like a resistor, with negligible reactance and thermal effects, for our range of input signals. Ideally, the I-V curve should be a straight line passing through the origin, whose slope equals the resistance. However, as our tests confirm it (see Fig. 3.3), there will be a visible hysteresis due to a $\sim 10^{-7}s$ delay between the voltage and current measurement. Obviously, given the goals of this work, this experimental error destroy the credibility of our measurements. Thus, we must begin by understand the sources of this problem, and then establish a strategy to eliminate it.

Time lag results from multiple components, but only three are considered relevant, enough to induce a measurable deviation, namely the two probes and the oscilloscope. We note that, for the applied frequencies, our cables are innocuous. We use two probes,

one measuring v_{DS} and the other i_D. The first has the possibility to manually tune the input capacitance, which we fix it to what we considered the most adequate position (we used a calibration square pulse from the oscilloscope). Relatively to the oscilloscope, we select the most appropriated scale for the time, voltage and current, given the expected sample values of the transistor, for each frequency set. Once the scale is selected, it remains constant during the measurements. This is critical because, when switching scales there occurs internal changes on the oscilloscope's hardware, which in turn introduces different offsets and delays. On the other hand, the oscilloscope is able to impose an artificial delay between the two channels to compensate the external skew. Since the range of this delay is insufficient to account for the ones we are seeing, we pin this compensation in the recommended value, proposed by the oscilloscope. Note that, so far, we only assure that each source of delay remains invariant between measurements of each frequency set.

3.3.1 Delay Correction

After we steady every source of delay, by unchanging any related controllable parameter, we apply the input signal to a resistor, that will be from now a reference element. From the voltage and current samples, measured on the resistor, we compute the correlation between them. In short, we applied successive shifts to one of the vectors, in our case the current (but it could also be the voltage), until the algorithm reaches the correlation minimum by an iterative process. The final amount of shifted points on one vector sample, relatively to the other, corresponds to a accurate approximation of the delay (multiplied by the sampling rate), imposed by our setup.

We found that the delay was frequency dependent, particularly, it was seen that the delay, measured in the same resistor and oscilloscope settings, decreased with frequency. This is a serious concern because GaN HEMTs are highly nonlinear systems, hence, when we apply a periodic signal to it, like a sine wave, harmonics will be generated. To understand this concept, let us analyse eq. 2.9 considering a constant v_{GS}, which can be readily simplified to $i_{DS} = C \tanh(\alpha\, v_{DS})$ where C and α are constants. Also, remember that, we are exciting our system with a sinusoidal signal and $\sin(x)^n$ can be simplified to something that contains the $\sin(nx)$ term. So, if we expand i_{DS} in a Taylor series, and we can ignore the constant so we just have to deal with the hyperbolic tangent, we will get $\tanh(x) = x - \frac{x^3}{3} + \frac{2x^5}{15} + (...)$. It becomes now visible that all odd harmonics are generated $(\sin(x) + \sin(3x) + \sin(5x) + (...))$ when we excite the transistor with a sinusoidal input. Furthermore, we can also consider the case where v_{GD} changes, that happens when we apply negative values to v_{DS}, and, consequently, additional harmonics are generated.

It is now clear that the output vector sample of our transistor will contemplate several frequencies, besides the frequency of excitation (or fundamental frequency), each of them affected by a different delay. For instance, if we were going to study the transistor response at 10 kHz, we must calculate the delay, in a resistor, for 10, 20, 30, 40 and 50

kHz. More than fifth order corrections becomes irrelevant since the generated harmonics have their amplitudes quickly reduced for higher orders. Fig. 3.4 shows the phase delay calculated for each scale of the oscilloscope settled accordingly to the frequency group, namely 250 Hz to 1250 Hz, 1 kHz to 5 kHz and 10 kHz to 50 kHz. Phase delay is defined as the product of the delay with frequency, and is plotted instead because this is the variable we will be using in our correction method.

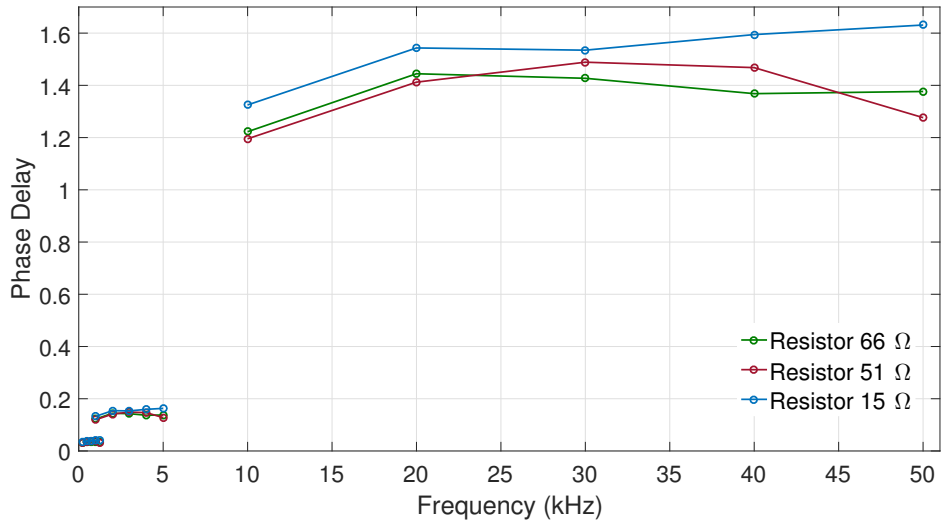

Figure 3.4: Phase delay (degrees) in function of the frequency for three different resistors, at three different oscilloscope scales.

After the calculation of every relevant delay value, we execute a MATLAB implementation to adjust the transistor's output vector sample. The method applied to correct the delay manifestation was developed on an *ad hoc* basis, whose key idea is to apply a phase delay correction to the output vector sample in the frequency domain. Two distinct steps are needed to support this calculation. First, we transform the i_{DS} vector to the frequency domain, represented with $\hat{i}_{DS}(f)$, using the Fast Fourier Transform algorithm. The frequency domain is limited from $-f_s$ to $+f_s$, with f_s being the frequency of sampling (dependent on the oscilloscope scale). Second, we create a phase delay vector, θ, with the same size of $\hat{i}_{DS}(f)$ resultant from a linear interpolation of the measured phase delay points. The following conditions were imposed: $\theta\left(f_s/2\right) = -\theta\left(-f_s/2\right) = \theta\left(f_5\right)$, where f_5 is the fifth harmonic frequency of the group, and $\theta(0) = 0$ represents the absence of phase delay at DC regime ($f = 0$). This method can be mathematically expressed as

$$i_{DS}\left(t - \theta/f\right) = \mathfrak{F}^{-1}\left[\hat{i}_{DS}(f)\, \exp\left(-i2\pi\theta\right)\right] \tag{3.1}$$

Thus, we are now able to make the appropriated correction, taking into account most frequencies generated by the transistor.

A secondary test was made, where we apply the correlation minimum algorithm directly to the transistor output vector samples. We observe that the resulting I-V curve maintained, in some areas visible hysteresis lobes. This is most probably an indication of multiple time constants.

3.3.2 Final Thoughts on the Calibration Procedure

Let us recap how far we got. Until now we presented the setup. We described in detail the optimized input signal, very important to differentiate the transistor's response from the setup limitation footprints (like the Pulser's transient). And we discovered, confirmed and found ways to correct the major source of error in the setup, namely, the delay. Nevertheless, we must still acknowledge the physical limitations of our oscilloscope, particularly its precision. Our tests show that, when excited with a sine wave limited from -1 V to 14 V, our transistor response ranges, approximately, from -1 A up to 1 A. The oscilloscope is set to 3 V and 250 mA per division (for a total of 10 divisions) in order to accommodate the entire signal - a lower scale would obscure part of the signal. Given the 8 bit vertical resolution of the oscilloscope, we will have $3 \times 10 \div 2^8 \approx 120$ mV of voltage precision and $0.250 \times 10 \div 2^8 \approx 10$ mA of current precision. We must remember, though, that the 16 averages applied to these results improve their accuracy. On the other hand, averaging is only useful at reducing the effect of random errors. We suspect that the oscilloscope we used may apply an unknown interpolation to our points, that could cause small ripples to the output curves. Additionally, our assumption of resistors to be completely linear and static may be compromised by the presence of a small curvature in the I-V curve, that also contributes to the propagation of errors. Considering the additional error associated to the delay correction, we are confronted with the complex task of knowing the factual confidence interval of our measured values. We can say, with certainty, that the lower bound of precision is the oscilloscope's precision. Knowing the upper value would require an extensive investigation work, that we were not able to produce for now.

In the next section we will present our results. All of the curves were corrected to account for the delay.

3.4 Results and Discussion

Once the calibration was carefully made, we move on to the measurements on a CGH27015 GaN HEMT on silicon carbide from Cree.

Every figure has a legend that contemplates all the obtained curves. Playing with different combinations allow us to infer information about the impact of trapping and temperature on the device. Also, we choose to display the entire legend, to provide a more clear idea of our line of thought to the reader. The bold sections in the legend represent the curves that are currently visible in that plot. The legend sections which

end in "(+ prepulse)" represent the signals preceded by a 14 V pre-pulse. All the remaining ones are preceded by a 0 V pre-pulse, which is the same to say that there is no pre-pulse. Furthermore, the 1st, 2nd and 3rd period designation are used to differentiate the first, second and third period in our drain signal (see section 3.2.1), each of them resulting in a single closed I-V curve. Lastly, we introduce here the upper and lower arch designations when referring to the I-V curve sections where v_{DS} is increasing and decreasing, respectively. They are featured by arrows indicating the growth direction.

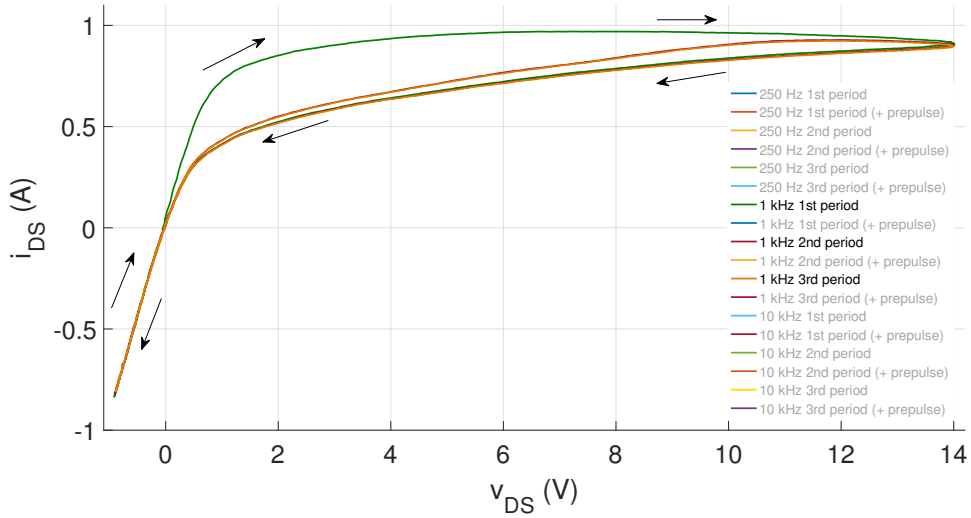

Figure 3.5: Three periods of a 1 kHz v_{DS} signal.

Fig. 3.5 plots the entire drain signal (all three periods) at 1 kHz, with no pre-pulse. The initial trap state corresponds to $V_{DSQ} = 0$, which, according to our model, is the same to assume $v_T(t = 0) \approx 0$. Also, since there is no current flowing during the pre-pulse, we presume a constant temperature in that interval. We can infer from this plot that the system is able to reach the steady-state at 1 kHz nearly after one period. Furthermore, this device is clearly affected by a combination of trapping and temperature (with unknown weights), visible by the hysteresis and the current decrease at high v_{DS}. As we said, we are interested to see here if the trap potential can, or not, be considered as a state variable in a memristive system. Thus, our next move is meant to distinguish the trapping from thermal effects.

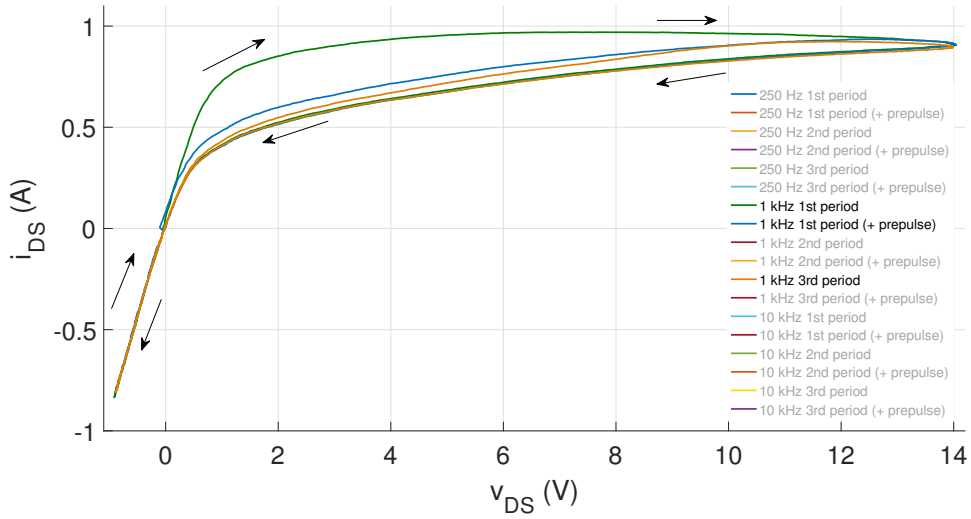

Figure 3.6: Effect of the pre-pulse on a 1 kHz v_{DS} signal.

Fig. 3.6 illustrates the influence of a 14 V pre-pulse, by plotting simultaneously a signal with and without pre-pulse. The first period of the signal preceded by a 14 V pre-pulse begins much more severely affected. Since the initial temperature is the same for both cases (there is no current flowing in the pre-pulse, and consequently no power dissipation), then, this difference can only be justified by the existence of, what it seems, strong trapping effects.

It is curious to observe that the application of a pre-pulse does not impose the steady-state faster then the case with no pre-pulse. This is confirmed by the difference between the upper arch of the first period preceded by a pre-pulse and the upper arch of the third period. The most probable reason has to do with the temperature rise after three periods of current flowing. This is responsible for increasing the average temperature and therefore decrease the channel conductivity. So, when referring to the steady-state we must assume constant average temperature and trapping/detrapping ratio.

Based on these two figures, we can now trace an ansatz model to help us predict the next curves and validate our theory, to distinguish trapping from temperature. Let us then begin by supposing we are increasing v_{DS} from zero, without any pre-pulse. Given the fast capture process, mostly happening at the nanosecond time scale, as we increase v_{DS}, in the kHz order, the traps will appear to fill instantaneously, which causes the effective trap potential to increase at the same time as v_{DS}. That is why, for the frequencies we are using, it is expected that all upper arcs of the first period for all frequencies will overlap initially. Fig. 3.7 illustrates this idea. However, by the end near the v_{DS} maximum (high i_{DS}), the lower frequency signals will suffer a larger current drop, decreasing as the frequency increases. This is expected because lower frequencies signals dissipate for longer periods of time and, consequently, suffer more severely thermal effects.

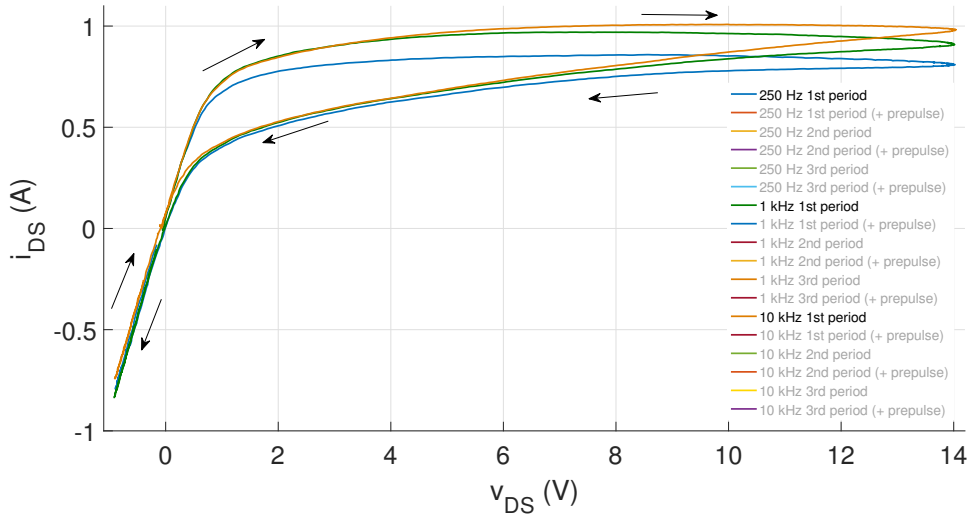

Figure 3.7: First periods of 250 Hz, 1 kHz and 10 kHz v_{DS} signals.

Continuing our model, we now analyse the case when v_{DS} decreases, looking at the lower arcs. In this situation the trap potential will not follow the same rate of variation of v_{DS}. In fact, as we saw before, the time-constants associated to detrapping are very slow, so, the current will adopt the values correspondent to the present applied v_{DS}, but with the effective gate potential still shifted by the trap potential resultant from higher v_{DS} values. To clarify, let us see what happens when we apply a signal that changes so fast that the traps are unable to discharge significantly.

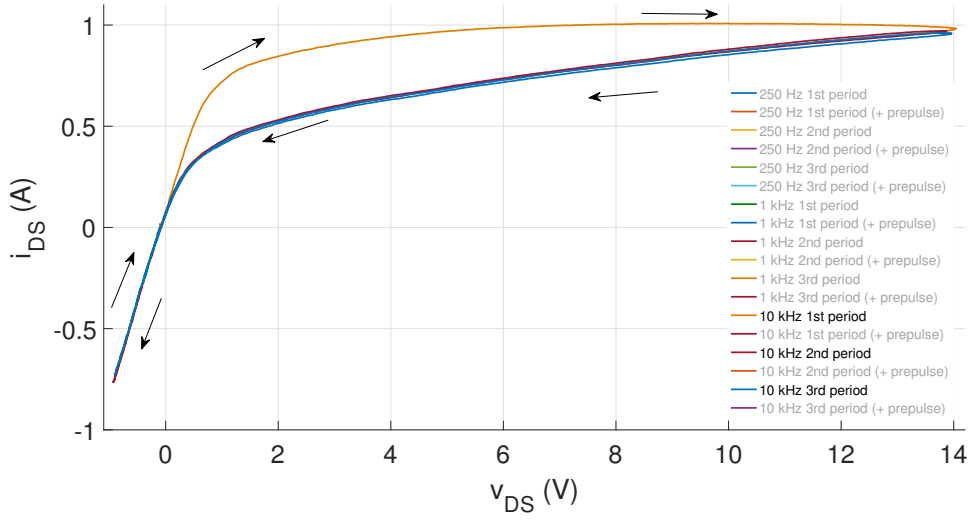

Figure 3.8: Three periods of a 10 kHz v_{DS} signal.

As visible by Fig. 3.8, after the first period of a 10 kHz signal, the hysteresis is practically gone. The only difference between the second and third period is a slight deviation of the third period curve downwards, most probably due to temperature rise. This allow us to infer for now that most detrapping occurs in a time interval much longer than $50\mu s$ (half a period of 10 kHz). So, if we change to a 250 Hz excitation, we have a better chance to observe the detrapping manifestation more clearly.

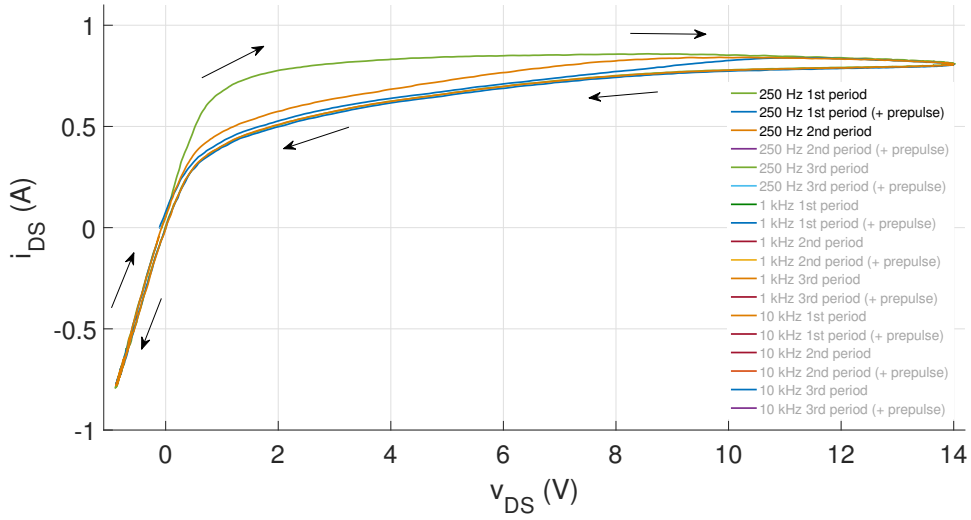

Figure 3.9: First periods of a 250 Hz v_{DS} signal.

Figure 3.9 show us a different phenomenon than the one presented in Fig. 3.6. Now, the upper arch of the first period preceded by a pre-pulse is below the upper arch of the second period curve (already at the steady-state). From this we can deduce that, after the first period preceded by a pre-pulse achieves the maximum value and starts decreasing down to zero, it takes less than 2 milliseconds (half a period of 250 kHz) for some significant detrapping to happen.

From these results we show that we were able to distinguish clear evidences of drain-lag from temperature effects. We saw that a sufficiently high frequency leads to the reduction of the hysteresis lobe area, almost to the point of a single curve for this level of precision, thus corroborating one of the memristor's fingerprint.

Let us now direct our attention to the question of whether the curves do pinch or not at the origin. As previously calculated, we are mainly limited by the oscilloscope's precision, particularly, 120 mV and 10 mA. That said, accordingly to Fig. 3.10, with focus on the inset plot, we can confirm that our curves pass through the origin, for this level of precision.

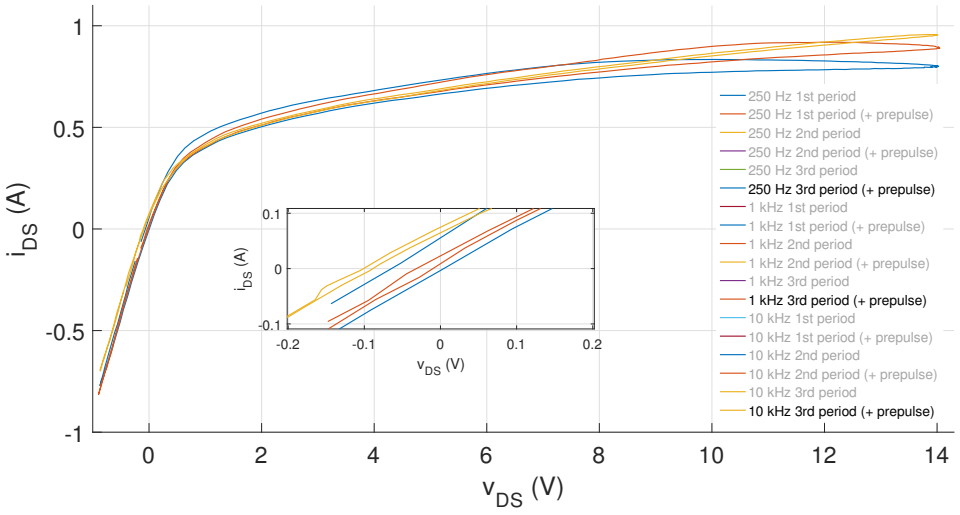

Figure 3.10: Steady-state for 250 Hz, 1 kHz and 10 kHz v_{DS} signals. Inset shows the zoom-in around the origin.

Chapter 4

Conclusions

In this work we demonstrate, using physical models and corroborating them with experimental results, that GaN HEMTs can be deemed as memristive devices. Nevertheless, this declaration has some serious uncertainties that one should meditate upon. One of those, and perhaps the most relevant, is the validation of the I-V curve passage through the origin. To understand our concern, let us consider that throughout this work we defended the idea that the nature of traps in GaN HEMTs is, as we know, an unclear subject with several different theories presented in the literature. This perspective imposed a more direct focus on an empirical model to simulate drain-lag, allowing us to simplify our work. However, there is indeed one theory that has been gaining relevance in recent years, which is the idea that traps are located in the buffer layer and result from the introduction of acceptors, like carbon or iron, designed to prevent punch-through and current leakage through the buffer [11], [12], [23], [33], [34], [35], [36], [37], [38]. This seems to corroborate the concept of a virtual gate below the channel, that causes channel depletion as the amount of captured charge increases. However, this also poses a serious question for our work, namely, what is the origin of the trapped charges. As you recall, the Kunihiro and Ohno model defended the idea that traps capture and emit charge directly from and to the channel, as illustrated in Fig. 1.3 (despite they considered the traps' location in the interface between the substrate and epitaxial layer). If this is true, then there is the possibility that $(i_{DS} = 0, v_{DS} = 0)$ does not belong to the I-V curves of a GaN HEMT, because some detrapping may still happen while $v_{DS} = 0$, determining that charge-carriers flow from and to the channel and thus contribute to $i_D(v_{DS} = 0) \neq 0$. On the contrary, the Rathmell and Parker model considers that traps act as transcapacitances, which means that the drain voltage will not act directly upon them and, consequently, the drain current does not contemplate the charge flowing from and to the traps. This model is very convenient for us, because it prevents an $i_{DS} \neq 0$ when $v_{DS} = 0$, at least due to trapping. On the other hand, this model assumes that the trapping time constant is controlled by the Fermi level, which in turn is respective to the semiconductor hosting the traps. It seems unlikely that the charges captured by the traps present in the buffer layer come directly from the traps vicinities, because, if they did, then this layer would remain electrically neutral, and no potential would exist to cause the channel's depletion. All these points lead us to question the validity of the GaN HEMT's I-V curves crossing the origin, and, consequently, if these devices can be deemed as memristive.

Near the conclusion of this work, we found a state-of-the-art paper, at the time unpublished [39], that made an approach very similar to ours, regarding the modelling of trapping. Particularly, they start from the Rathmell and Parker model to obtain also

an effective trap potential, and use it to create a new nonlinear model to simulate GaN HEMTs. They, however, consider also the temperature as a state-variable. Nevertheless, several similarities were found between our works, which makes this paper a good complement to our work (and possibly vice-versa).

4.0.1 Future Work

We saw, in our experimental results, that completely separating thermal from trapping effects is quite difficult, if not impossible. Further, temperature variation in this type of devices is inescapable and strongly influences their response. In fact, thermal effects generate complex behaviour. For instance, they cause current to drop, due to the rise of the channel's resistance, while, at the same time, contribute to the increase of charge emission, which, as a consequence, reduces the current collapse. Therefore, the exclusion of temperature as a state variable is a probable source of error, that undermines our ability to accurately predict the real device behavior. Therefore, we propose, as future work, to consider the temperature as an additional state variable in a more complete dynamical system. The other major problem, already mentioned in the previous chapter, is the precision of measurements. Specifically, what is the DC offset in our samples and, more importantly, what is the real precision of the current and voltage measurement, when $v_{DS} \to 0$. These are two serious problems, that are interconnected, and obscure our ability to attest with confidence the passage of the GaN HEMT I-V curves through the origin. Therefore, we propose, as future work, foremost an increase of calibration samples to improve our correction precision, and if possible an improvement of our measurement techniques and equipment.

The technological application of GaN HEMTs as potential memory devices is at this stage unforeseeable. A possible application would be as non-volatile memory, since the memory depth of GaN HEMTs is limited by the detrapping time constants (around milliseconds). On the other hand, we are dealing with an analogue memory device, in opposition to the typical resistive-switching-based devices, which directs us to analogue computation. An additional factor, and perhaps the most important one, that must be weighted before any final decision, is the potential monetary outcome. GaN HEMTs are considerably more expensive then the typical memristor samples made of chromium, tin or tungsten [40]. Therefore, we propose as future work an analysis of the new GaN HEMTs' applications and a market study to understand at which level can they be profitable.

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