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Analysis and Comparison of dc/dc Topologies in Partial Power Processing Configuration for Energy Storage Systems

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***Abstract*—This paper presents an analysis and comparison of dc/dc switched-mode power supplies (SMPS) for energy storage systems in partial power processing (PPP) configuration. The advantage of this configuration is that the SMPS only processes the partial power resulting from the voltage difference between the source and the energy storage element, thus allowing for a reduction of the converter power rating. Selection of an appropriate topology for a given system configuration is the key factor in achieving high efficiency power conversion. An analysis and comparison of dc/dc topologies based on component stress factor (CSF) is performed to determine the optimal solution for the evaluated application. Based on the results of the CSF analysis, a dc/dc converter is designed, built and tested. Experimental results prove the feasibility of the PPP configuration with a reduction of the 80% of the power rating compared to the traditional interconnection, which implies a reduction in cost, weight and an increase in efficiency.**

Keywords—Converter; dc-dc; partial power converter; partial power processing; electrolyzer cells; energy storage systems.

I. INTRODUCTION

Energy storage elements are indispensable components in renewable energy systems due to the intermittent nature of the energy source [1], [2]. They are as well essential in smart grids in order to balance the energy production and demand [3], and also in stand-alone structures to provide energy in remote locations, where cabling is challenging and expensive. Switched-mode power supplies (SMPS) play an important role in the integration of energy storage elements to provide high efficiency energy conversion [4].

Nowadays, different energy storage technologies are available, such as electrochemical (batteries), thermal (molten salt), mechanical (pumped hydro, compressed air, flywheels), chemical (hydrogen based energy storage), etc. More than 95% of the global energy storage capacity is represented by pumped hydro plants [2], which is a mature technology and allows to store large quantities of energy with high efficiency over a long time. However, it is not suited for distributed generation and have relatively low energy density. Electrochemical energy storage is an emerging technology, which has had significant advances in the last two decades both from technical and cost perspective. It provides high flexibility in terms of energy and power capacity. Nevertheless, batteries lifecycle is limited and there are environmental and safety concerns. Hydrogen energy storage systems have also attracted research interest in the last years [5]. The advantages of hydrogen is that it can be locally produced, it offers high energy density, long term scalable storage and low enviromental impact. However, the cost of the initial investment is high and there are safety considerations.

II. SYSTEM ANALYSIS AND SPECIFICATIONS

The application under analysis is an energy storage system based on alkaline electrolyzer cells (EC), nevertheless, the system configuration can as well be applied to battery charge systems. The traditional way of interconnecting the elements is shown in Fig. 1 (a), where the load, in this case the EC stack, is connected at the output of a dc/dc converter. In this configuration the converter must be rated at the full power of the EC stack. Figure 1 (b) shows the block diagram of the partial power processing (PPP) configuration, where the EC stack is connected in series with the dc bus (V_{dc}) and the dc/dc converter creating a voltage divider. Therefore, in this arrangement, the input of the SMPS (V_{in}) is set by the voltage difference between the dc bus and the EC stack (V_{dc} - V_{EC}), thus, the dc/dc converter only process the differential power between the dc bus and the EC. Figure 2 shows the electrolyzer stack voltage as a function of the current and Table I presents the specifications of the system in PPP configuration. As it can be observed, in PPP arrangement the maximum input power processed by the converter is P_{in} = 733 W, compared to the traditional parallel connection, where the converter would have been rated at the maximum EC power, in this case P_{EC} = 3456 W. Therefore, a reduction of nearly 80% of the required power of the dc/dc converter is achieved, which considerably helps reducing the cost and weight, as well as increasing the power density and efficiency of the system.

The idea of the series connection of source and load originated in the spacecraft technology for photovoltaic applications [6]. The proposed configuration, called series connected boost unit (SCBU), showed numerous advantages compared to the traditional interconnection. High efficiency and high power density can be achieved because the dc/dc converter only processes a fraction of the total power of the system, which results in small, lightweight and low cost power supplies, which in space implementations are extremely important.

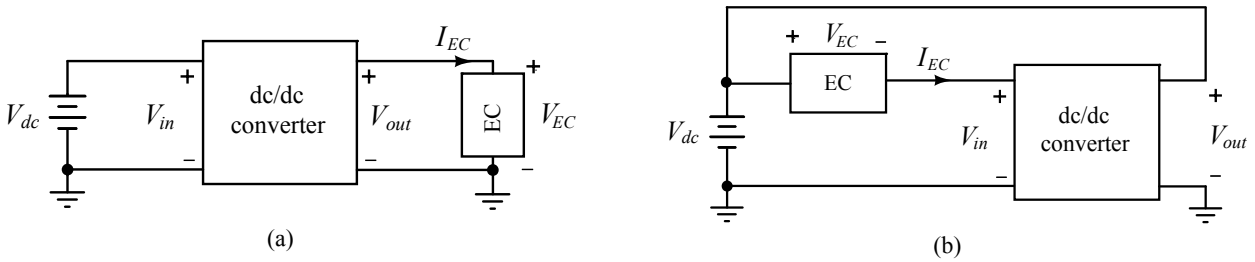

Fig. 1. Block diagram of the traditional parallel connection (a) and (b) partial power processing configuration (PPP).

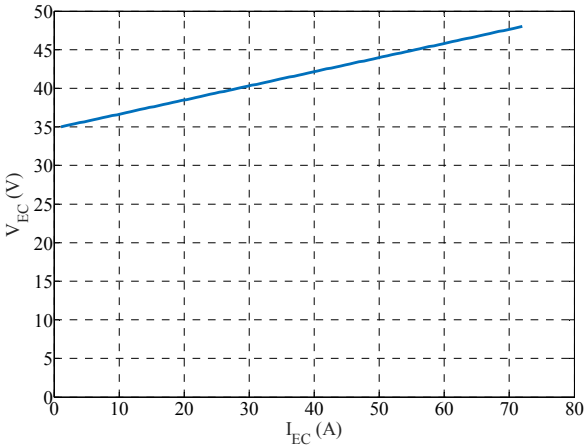

Fig. 2. Electrolyzer stack voltage (V_{EC}) as a function of the current (I_{EC}).

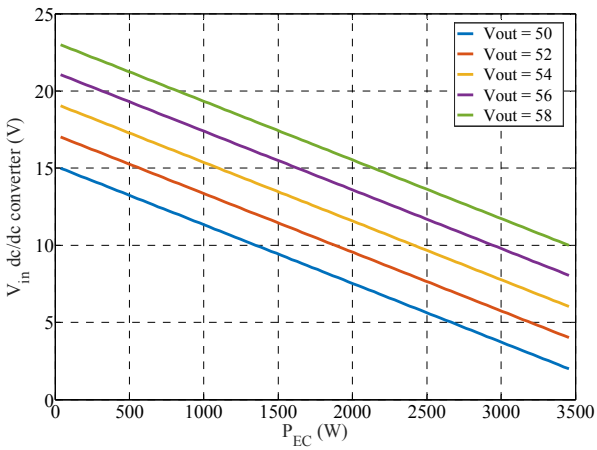

Fig. 3. PPP configuration dc/dc converter input voltage (V_{in}) as a function of the EC power (P_{EC}) for different output voltages.

TABLE I
PPP CONFIGURATION SYSTEM SPECIFICATIONS

V_{dc}	50 to 58 V
V_{EC}	35 - 48 V
I_{EC}	1 - 72 A
P_{EC}	3456 W
$V_{in} = V_{dc} - V_{EC}$	2 to 23 V
$P_{in} = V_{in} \cdot I_{EC}$	733 W
V_{out}	50 to 58 V

Depending on the requirements of the application, the series connection of source and load can be performed at the input (input-series-output-parallel ISOP) or at the output of the dc/dc converter (input-parallel-output-series IPOS) [7], where IPOS structure is used in a battery storage system.

Figure 3 and Fig. 4 show the input voltage and input power of the dc/dc converter in PPP configuration, respectively, as a function of the power of the EC, for different values of the output voltage. As it can be observed, the PPP configuration has the disadvantage of presenting a large variation of the converter input voltage, which requires the selected topology to operate efficiently within a wide input to output voltage range. It is important to notice that the point at which the converter power is maximum, will not correspond with the maximum EC, as the characteristic electrolyzer stack curve will make the voltage at the input of the converter decrease as the power increases. It is also important to observe that the system should be designed so the amount of power processed by

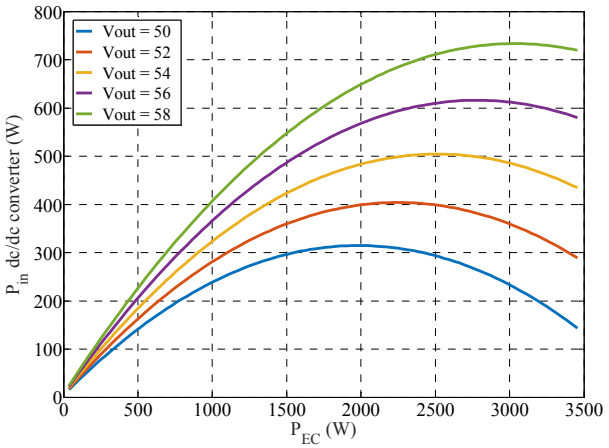

Fig. 4. PPP configuration dc/dc converter input power (P_{in}) as a function of the EC power (P_{EC}) for different output voltages.

the converter tends to zero, thus reducing the losses inserted in the system. Therefore, maximizing the efficiency of the direct power flow, which corresponds to the path to charge the EC, will minimize the power processed by the dc/dc converter and maximize the efficiency of the system.

III. COMPONENT STRESS FACTOR (CSF) ANALYSIS

The topology selection is a key factor in achieving high efficiency, since it will determine the performance of the overall system. From the system specifications it can be observed that the power stage presents a large input/output

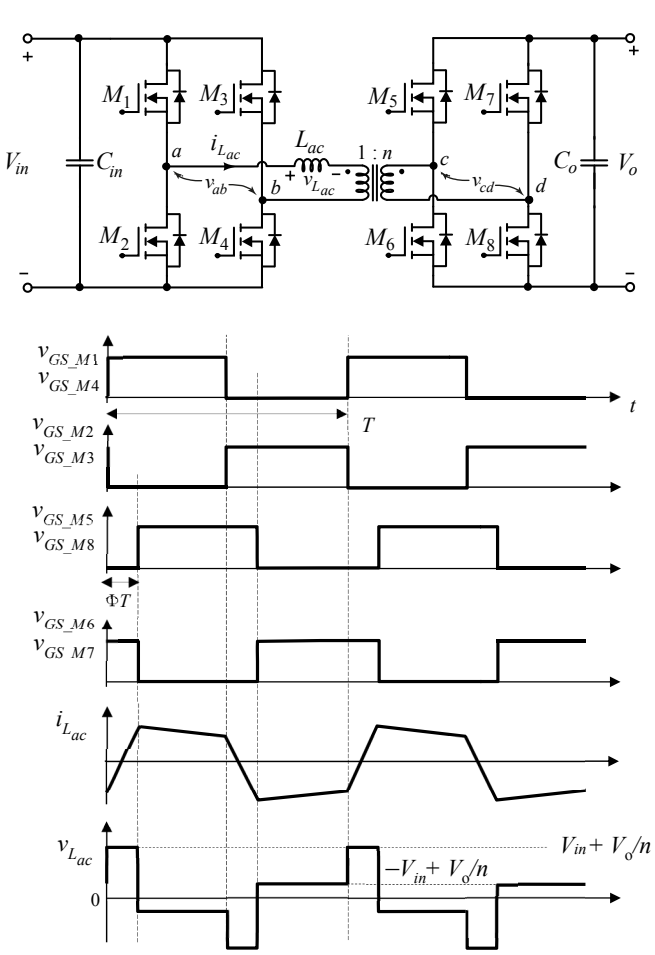

Fig. 5. Dual Active Bridge (DAB) topology and key operating waveforms, top and bottom, respectively.

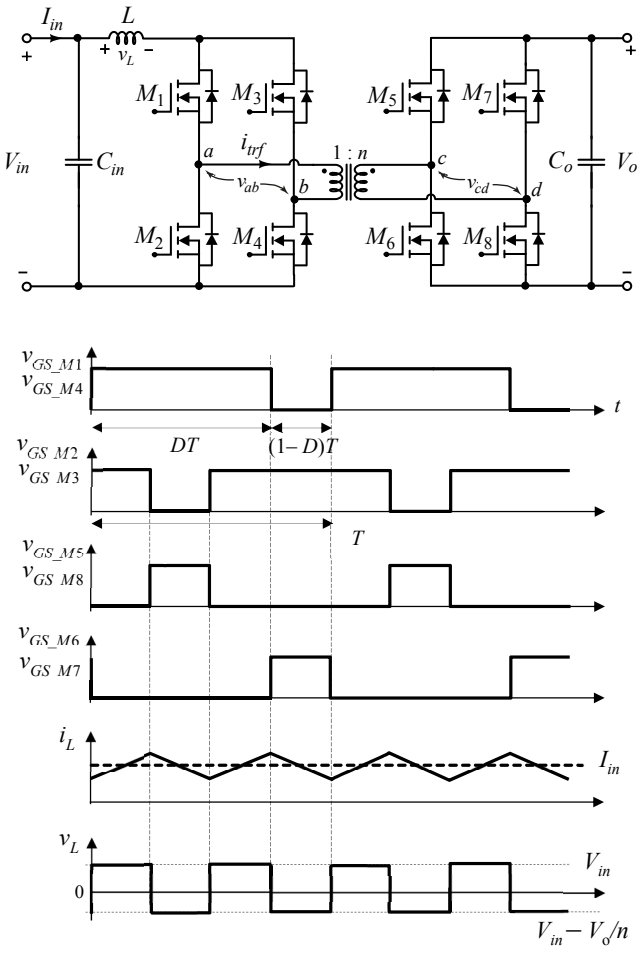

Fig. 6. Isolated Full Bridge Boost (IFBB) topology and key operating waveforms, top and bottom, respectively.

voltage variation. The challenge is to select a topology that can provide high power conversion efficiency over the whole operating range.

An analysis and review of high efficiency bidirectional dc/dc converters with high voltage gain is performed [8]. Based on the analysis and the system specifications, the topology selection is narrowed down to two candidate topologies: dual active bridge (DAB) and isolated full bridge boost (IFBB) converter. The selection is performed based on complexity in terms of number of active switches, passive components and control. These components will affect the efficiency, cost and reliability of the entire system. Both, DAB and IFBB topologies, have been proved to achieve high efficiency [9], [10], with a reduced component number (low complexity). Figure 5 and Fig. 6 show the schematic of the DAB and IFBB topologies and their operating waveforms, respectively. As it can be observed, both converters present the same number of active switches and passive components. In the DAB the power is delivered to the output through an ac inductor, whose charge and discharge is controlled with the phase-shift angle of the half bridge switching legs. In the IFBB converter, the control parameter is the duty cycle of the primary switches and the input inductor is the component that transfers the energy to the output port.

The analysis of the DAB and IFBB topologies is performed based on component stress factor (CSF) [11]. CSF is a derivation of the component load factors approach (CLF) [12]. CLF is a numerical method, which is calculated based on the components voltage and current stress and normalized to the processed power (volt-amp/watt figure), which makes the calculation dimensionless.

The approach of the CSF analysis is based on the assumption that the evaluated topologies have the same amount of resources: silicon for semiconductors, magnetic material and copper for windings and capacitor volume for energy storage/filter components. A weighing factor is applied to distribute the resources within the topology. The result of the CSF analysis provides an effective way to evaluate the losses in the individual components of the circuit, and consequently, an estimation of the converter performance. Therefore, the analysis gives a quantitative measure to compare the performance of different topologies for a specific application [13], [14].

The CSF method adopts two assumptions in order to simplify the calculations, i. e., the power losses in the converter are neglected (efficiency 100%) and the inductors are large enough to have no ripple current (square waveform).

The stress factor is calculated independently for each component: semiconductors (SCSF), windings (WCSF) and capacitors (CCSF), as shown in (1), (2), (3), respectively. The CSF is related to the power dissipated in the component. In the semiconductors, the conduction losses are calculated with the squared root mean square (rms) current through the device multiplied by the channel on-resistance of the switch. For a given die size, the channel on-resistance is proportional to the voltage rating to the power of 2.5 [15], higher voltage rating will result in a longer channel with smaller cross section. Taking the rated voltage squared gives a good approximation to relate the maximum voltage and the channel on-resistance. Therefore, SCSF is calculated with the breakdown voltage squared, times the rms current squared, and normalized to the square of the processed power, to provide a dimensionless quantity.

Regarding the calculation of the stress factor of magnetic components, to perform a fair comparison, each topology should have the same amount of copper volume, and hence, the same winding area. The windings losses in magnetic components are calculated with the rms current squared, times the winding resistance. The winding resistance is related to the number of turns and the cross-sectional area of the copper. The voltage applied to the windings is proportional to the number of turns. Therefore, the resistance will increase with the square of the number of turns, which is proportional to the voltage squared. The WCSF is then computed as the maximum voltage applied to the windings squared, multiplied by the rms current squared (2). The maximum voltage applied to the winding is calculated as the average voltage applied to the winding over a period, as shown in (4).

The stress factor of capacitors is determined by the resistive losses due to the equivalent series resistance (ESR). The ESR is related to the capacitor volume, and the volume is proportional to the energy storage capacity, thus, the CCSF is calculated with the squared maximum voltage and the rms current as presented in (3).

$$SCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{\max}^{\,2} \cdot I_{rms}^{\,2}}{P_{in}^{\,2}} \tag{1}$$

$$WCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{\max\_avg}^{\,2} \cdot I_{rms}^{\,2}}{P_{in}^{\,2}} \tag{2}$$

$$CCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{\max}^{\,2} \cdot I_{rms}^{\,2}}{P_{in}^{\,2}} \tag{3}$$

$$V_{\max\_avg} = \sum_i D_i \cdot |V_i| \tag{4}$$

The distribution of the resources is implemented by the term $\sum_j W_j \Big/ W_i$, which represents the weighting factor for component *i*, where $\sum_j W_j$ is the sum of the individual weights of all components of the same type and W_i is the weight assigned to the component *i*. In the first iteration, the resources are distributed equally. Based on the results, the weight distribution can be adjusted. As a result, the component with higher CSF can be assigned with a larger amount of the resource in order to reduce the stress factor.

Once the stress factor for each component is calculated, the total CSF is computed as the sum of component stress factors of the same type as in shown in (5).

$$\begin{cases} SCSF = \sum_i SCSF_i \\ WCSF = \sum_i WCSF_i \\ CCSF = \sum_i SCSF_i \end{cases} \tag{5}$$

From the procedure of the CSF calculation, it can be observed that the analysis accounts for the conduction losses in switches, magnetic components and capacitors. However, it does not consider the switching losses in the semiconductors and the magnetic core losses. From the system specifications presented in Table I, the application under analysis is a low voltage, high current application, therefore, the conduction losses in the semiconductors will dominate over the switching losses. Regarding the magnetic components, the core losses are a function of the magnetic material, the volts-seconds, the peak to peak ac flux density and the switching frequency. As discussed before, the system is characterized by a low input voltage to the dc/dc converter, and the switching frequency is limited to 50 kHz. Therefore, the CSF approach is considered a valid method to compare the topologies for the application under analysis.

Figure 7 (a) to (f) shows the results of the CSF analysis for the DAB and the IFBB topologies for semiconductors (SCSF), windings (WCSF) and capacitors (CCSF), respectively. The graphs show the stress factor values as a function of the power of the EC for different values of the output voltage. The CSFs are normalized to the maximum stress value, which occurs in the DAB topology. At low power levels the DAB converter present very high CSF in semiconductors, winding and capacitors compared to the IFBB topology. This is due to the fact that the DAB topology presents a large rms circulating reactive current. At low power levels the rms current is very large compared to the processed power, which results in large CSF values. As the power of the electrolyzer stack increases, the ratio of the rms current to the processed power is reduced and thus, the CSF. In the IFBB converter the highest CSF occurs at the maximum EC power level (maximum EC current) and minimum output voltage. As it can be observed from the SCSF, the DAB presents a minima for the different output voltages, which corresponds to the point where the converter reactive current is minimized. The IFBB presents higher stress as the input to output voltage transformation ratio is increased, which is an expected result from boost derived topologies. The DAB therefore, shows a reduced SCSF compare to the IFBB, but only in a small range of the operating region. However, the WCSF for the DAB is significantly worse than that of the IFBB in all the operating range due to the increased voltage stress in the magnetic components and the alternating current nature in the resonant inductor.

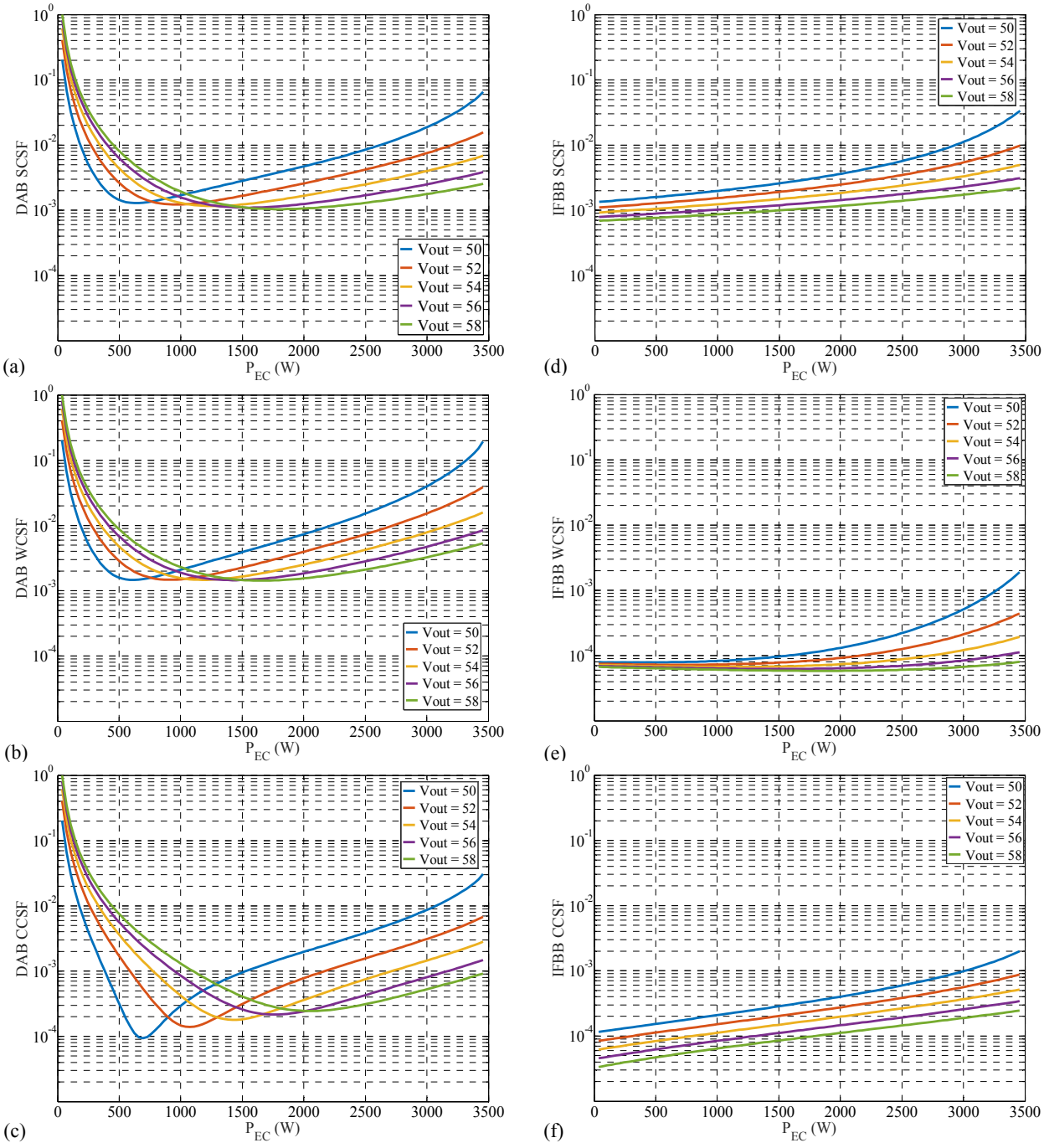

Fig. 7. CSF analysis of DAB: (a) SCSF, (b) WCSF and (c) CCSF; and IFBB converter: (d) SCSF, (e) WCSF and (f) CCSF, as a function of the EC power (P_{EC}) for different output voltages (V_{out}).

Based on the results of the CSF analysis, the IFBB converter is the selected topology to implement the energy storage system in PPP configuration.

IV. IFBB Design & Experimental Results

A prototype of the IFBB is designed and constructed. A printed circuit board (PCB) with 4 layers is designed with special attention to minimize the ac current loops. Due to the high current application, 140 µm (4 oz) PCB copper thickness is used in order to minimize the resistive losses. The main converter components are listed in Table II. The design is based on Silicon (Si) MOSFETs with low R_{DS} on-resistance in order to reduce the conduction losses. DirectFET technology from Infineon is selected, which provides low package inductance and maximized thermal transfer due to copper drain clip. The high rms current on the IFBB primary side, which is around $I_{rms\_prim\_MOS}$ = 40 A, will cause high conduction losses, therefore, primary MOSFETs with very low on-resistance are selected, R_{DS} = 0.34 mΩ at V_{GS} = 10 V. The maximum rms current on the secondary side is $I_{rms\_sec\_MOS}$ = 15 A, which allows to select devices with higher on-resistance than in the primary side. The converter switching frequency is f_{sw} = 50 kHz, to limit the switching losses. The magnetic design for the inductor and the transformer is based on planar cores. Planar magnetics offers low profile structure with high surface

TABLE II
PPP IFBB CONVERTER COMPONENTS

$M_1 \sim M_4$	IRL7472L1
$M_5 \sim M_8$	AUIRF7759L2
ISO gate drivers	SI8235AB-D-IS1
Transformer	1:2, EILP43/10/28, Ferrite N87
Inductor	2.3 µH, EILP43/10/28, Ferrite N87
Capacitors C_{in}	20 x 10 µF 50V X7R
Capacitors C_{out}	20 x 10 µF 100V X7S
Current sensor	ACS770LCB-100B
Switching frequency	f_{sw} = 50 kHz
Digital controller	TMS320F2808 DSP

area and good thermal characteristics. Moreover, it helps implementing interleaving techniques to achieve low leakage inductance and ac resistance [10]. The inductor is manufactured in a 6 layers PCB with 210 µm (6 oz.) copper thickness. Two PCB are stack in parallel in order to reduce the dc resistance. The transformer is manufactured in an 8 layers PCB with 210 µm (6 oz.) copper thickness with a turns ratio of 1:2. The primary winding (P) is formed by two turns in parallel, which are fully interleaved with four turns of the secondary winding (S), in a structure $\frac{P}{2}/S/\frac{P}{2}/S/\frac{P}{2}/S/\frac{P}{2}/S$. Full interleaving winding technique is implemented in order to reduce the transformer leakage inductance. Achieving a low leakage inductance is critical in full bridge boost configurations without snubbers, because the energy stored in the leakage inductance will cause an overshoot in the primary MOSFETs. Full interleaving technique also helps reducing the ac resistance as the magneto motive force (mmf) is always equal to 1[10]. The measured transformer leakage inductance is L_{lk} = 19.4 nH.

The control law is implemented in a digital signal processor (DSP) TMS320F2808 from Texas Instruments. The reading of the inductor current is performed with a high precision Hall effect current sensor, which inserts an extremely low resistance of R_{sens} = 0.1 mΩ.

Figure 8 shows the experimental prototype of the IFBB converter. The primary and secondary MOSFETs are placed on the bottom side of the PCB, in order to transfer the heat to the heat sink through an isolated gap pad material with a thermal conductivity of 4.0 W/mK.

For the experimental test of the IFBB in PPP configuration, the behavior of the EC stack is simulated with an electronic load in series with a power resistor. The electronic load is configured as a constant voltage source and will set the starting point of the characteristic V-I curve shown in Fig. 3. The power resistor (R = 0.185 Ω) connected in series, will provide the slope of the V-I curve as the I_{EC} current increases.

Figure 9 shows the steady state waveforms of the IFBB converter. Figure 9 (a) shows the converter operating at V_{dc} = 50 V, V_{EC} = 38 V, I_{EC} = 13 A, V_{in} = 12 V, P_{EC} = 594 W, P_{conv} = 156 W. In this conditions, the duty cycle D is approx. 75%. Figure 9 (b) shows the IFBB converter waveforms at the system maximum power level, thus, the electrolyzer stack is charging at the maximum current. The

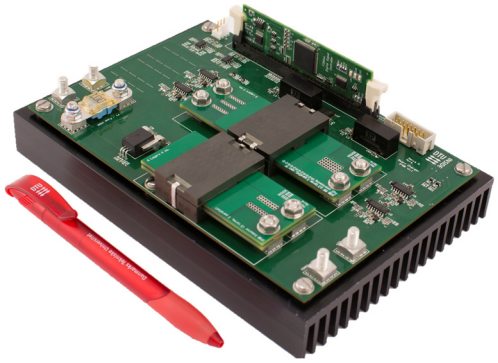

Fig. 8. Experimental prototype of the IFBB converter.

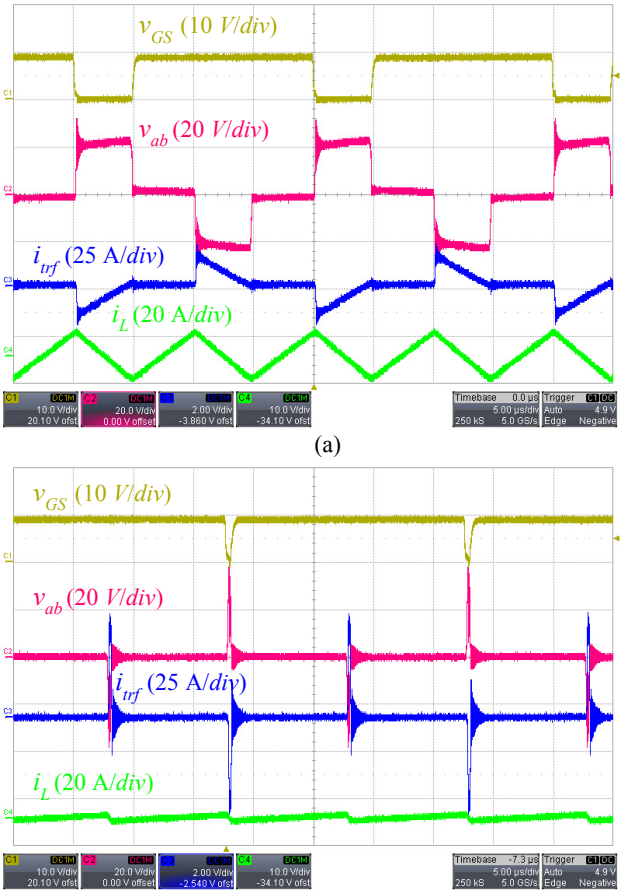

Fig. 9. IFBB operating waveforms, from top to bottom: primary gate-to-source voltage (10 V/div); voltage across the transformer primary side (20 V/div); transformer secondary side ac current (25 A/div) Rogowski coil (20 mV/A); inductor ac current (20 A/div) Rogowski coil (100 mV/A). Time scale 5 µs/div.

converter operating conditions are V_{dc} = 50 V, V_{EC} = 48 V, I_{EC} = 72 A, V_{in} = 2 V, P_{EC} = 3456 W, P_{conv} = 144 W and the converter's duty cycle is maximum D = 99 %. As it can be observed the inductor current ripple reduces as the input voltage of the converter decreases. However, the peak current on the transformer secondary side increases due to the reduced conducting time of the secondary MOSFETs.

Figure 10 shows an enlarged portion of the steady state waveforms when the converter operates at maximum duty cycle (Fig. 9 (b)). As it can be observed, the voltage across the transformer does not clamp, which indicates that there is no avalanche mode operation of the MOSFETs primary

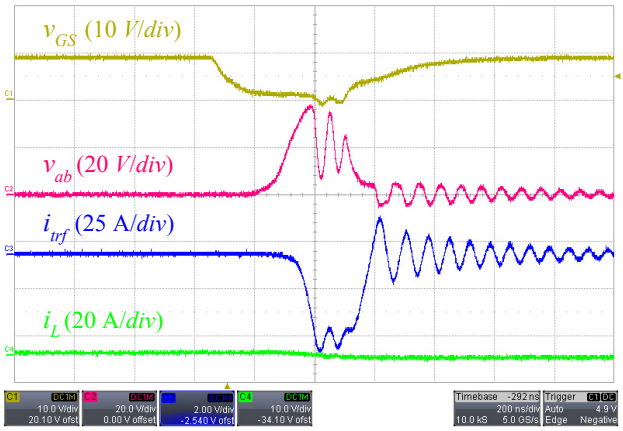

Fig. 10. Enlarged IFBB operating waveforms from top to bottom: primary gate-to-source voltage (10 V/div); voltage across the transformer primary side (20 V/div); transformer secondary side ac current (25 A/div) Rogowski coil (20 mV/A); inductor current ac (20 A/div) Rogowski coil (100 mV/A). Time scale 200 ns/div.

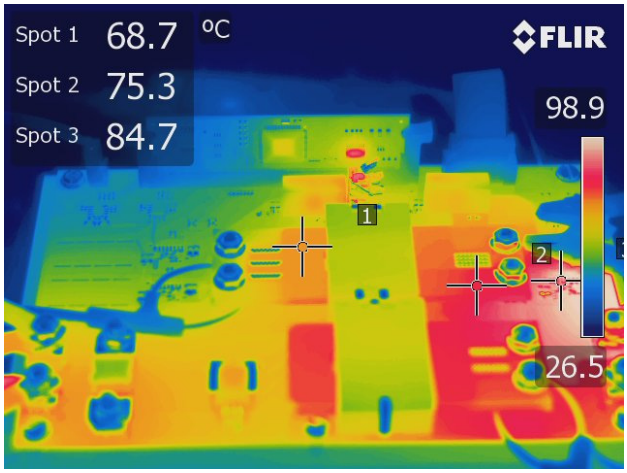

Fig. 11. Thermal image of the IFBB converter in PPP configuration operating at the EC maximum power P_{EC}=3456 W.

side. This proves the low leakage inductance design of the transformer, therefore, no snubber components are required. Fig. 11 presents a thermal image of the IFFB converter operating at the worst conditions, which are minimum input voltage and maximum input current, while the system is working at the maximum power level P_{EC} = 3456 W. The thermal image shows a maximum temperature of 98.9 °C. As the input voltage decreases, the converter current stress on the secondary side reduces, while it increases on the primary side, therefore, the highest temperature appears at the converter primary side.

V. Conclusion

This paper presents an analytical comparison of dc/dc topologies in PPP configuration for energy storage systems. Selecting the most appropriate topology for a specific application is crucial in achieving high efficiency. Although the two analyzed converters present the same number of active switches and passive components, the CSF analysis shows a big difference of the converters' performance for the given configuration. Based on the analysis, an IFBB converter is designed and tested. Experimental results shows that in PPP configuration, the converter can handle the maximum system power level, with a reduction of 80% of the power rating compared to traditional load connection. Therefore, the proposed PPP configuration for energy storage systems achieves a large reduction of the converter size, weight and price.

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