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Published in:
Proceedings of 2018 International Power Electronics Conference

Link to article, DOI:
10.23919/IPEC.2018.8507536

Publication date:
2018

Document Version
Peer reviewed version

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Citation (APA):
Sun, B., Zhang, Z., & Andersen, M. A. E. (2018). Review of Resonant Gate Driver in Power Conversion. In Proceedings of 2018 International Power Electronics Conference (pp. 607-613). IEEE. DOI: 10.23919/IPEC.2018.8507536

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Review of Resonant Gate Driver in Power Conversion

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***Abstract*-Resonant gate driver is a vital trend of research topic along with the development of high electron mobility transistor (HEMT). Compared with conventional gate driver, resonant gate driver achieves much lower power dissipation during switching transient and widely viewed as one essential technique for high frequency power conversion. This paper provides a state-of-art review and thorough comparison of different resonant gate driver topologies. Case study of two representative topologies is carried out. Application of resonant gate driver in Gallium Nitride (GaN) HEMT is discussed.**

Keywords— Resonant gate driver, GaN HEMT, power conversion.

I. Introduction

GaN HEMT is widely considered as a promising candidate for the next generation of power transistor [1]. Compared with Silicon MOSFET, GaN HEMT has a higher semiconductor band gap, which leads to lower on-resistance, lower leakage current and higher operating temperature [2-5]. All these salient features enable the GaN HEMT's application in high frequency power conversion. Benefit from fast switching capability, GaN HEMT based high frequency converter can effectively achieve volume reduction and high power density integration [6].

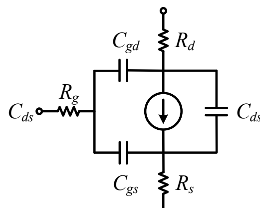

Fig. 1. Equivalent circuit of transistor.

Efficiency is the chief consideration in power converter design. For high frequency switching application, transistor parasitic capacitor and loop impedance will result in considerate power loss. Equivalent circuit of the transistor is shown as Fig. 1 [7]. Two major sources of power loss during the switching process are: transistor switching loss and gating loss [8]. Switching loss is related to the transistor output capacitor (C_{oss}=C_{DS}+C_{GD}) [9]. Soft-switching techniques has been widely investigated for decades to minimize this part of energy dissipation [10]. Gating loss is related to transistor's input capacitor (C_{iss}=C_{GS}+C_{GD}). Charging and discharging process of transistor C_{iss} during switching transient lead to energy dissipated in the gate loop impedance, which is also known as CV^2 loss. Equation for CV^2 loss calculation is given as (1):

$$P_{Gate} = V_G \cdot Q_G \cdot f_s = V_G^2 \cdot C_{iss} \cdot f_s \tag{1}$$

, where Q_G is the total gate charge, f_s is the switching frequency and V_G is the gate voltage [11]. Furthermore, loss dissipation on the gate driver transistor also contributes to the overall gate driver loss.

For conventional gate driver, CV^2 loss is totally dissipated in gate loop impedance during the switching transient. According to (1), gating loss is proportional to the transistor switching frequency, which highly deteriorates the converter efficiency in high frequency application [12]. Resonant gate driver is introduced to recycle this part of energy. With resonant tank added in the gating path, part of the gate energy can be recycled and gating loss is significantly reduced [13].

In this paper, review of resonant gate driver topologies is given in section II. In section III, case study of two representative resonant gate driver is carried out. Detailed analysis of gating performance and loss evaluation is given according to the simulation results. Section IV concludes the paper.

II. Review Of Resonant Gate Driver

Conventional gate driver is the push-pull (totem pole) topology, shown in Fig. 2(a). PMOS and NMOS are in series configured as half bridge structure to generate square wave gate signal [14]. Full-bridge configuration is aiming to provide negative gate voltage for the transistor effectively gated-off, which is shown in Fig. 2(b). All kinds of resonant gate driver design are based on these two fundamental topologies. Difference lays in the resonant tank design and control strategy.

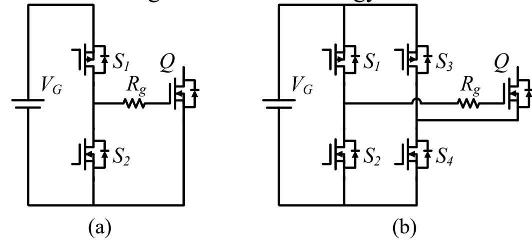

Fig. 2. Conventional gate driver. (a) Half-bridge configuration (b) Full-bridge configuration

One criterion to classify resonant gate drivers is the initial inductor current [15]. For zero initial inductor

current topology, gate charging process is simultaneous with the charging process of resonant inductor. For non-zero initial inductor current topologies, gate charging is initialed with a start-up current, which helps to shorten the switching transient. Different resonant gate driver topologies are classified and reviewed according to this criterion in this paper.

A. Zero initial inductor current gate driver

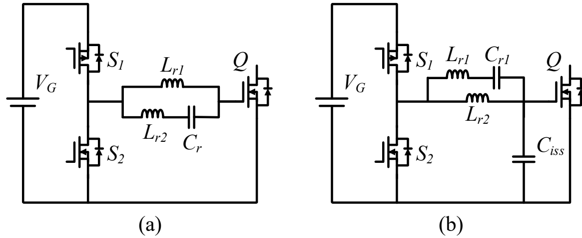

Fig. 3. Multi-resonant tank topology. (a) External resonant tank (b) Parasitic included resonant tank

A multi-resonant gate driver designed for Class-E power amplifier is proposed in [16], which is shown as Fig.3 (a). The resonant tank, L_{r1}, L_{r1} and C_r, are designed to pass through 1st and 3rd harmonic component. A quasi-square gate signal is generated for efficiency consideration. Gate transistors S_1 and S_2 both operate at soft switching, which further helps to minimize the gate driver loss. For Si MOSFET (FDMC86248) in a 32W Class-E amplifier operating at 20MHz, gating loss is reported to be lowered from 1.8W to 720mW, compared with the hard gating method by gate driver IC (LM5114).

Further research into this idea for GaN HEMT application is carried out in [17], which is shown as Fig.3 (b). Input capacitor of GaN HEMT is considered as part of the resonant tank. The proposed gate driver is tested to drive GaN-HEMT (TPH3066PS) based 13.56MHz Class-E inverter. Gating loss is reported to be lowered from 880mW to 800mW compared with the conventional totem pole gate driver.

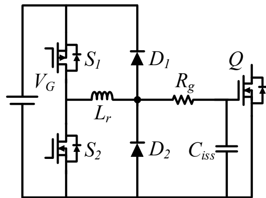

Fig. 4. Efficient power recovery topology.

Resonant gate driver topology with efficient power recovery is first proposed in [11], which is shown as Fig. 4. Resonant inductor L_r is connected to the totem pole output, where freewheeling diodes D1 and D2 are installed to provide returned current path for excessive energy recovery. The proposed topology is tested based on MOSFET switching at 500kHz. Gating loss is reported to be 209mW, which reduces 55% of the conventional loss. This topology is further researched in [18] to be applied for GaN HEMT. Gating loss is reported to be 198mW in a 10MHz IC design simulation. Application of this topology in driving e-mode GaN transistor (EPC2001) is researched in [19]. During 10MHz operation, gating loss is reported be 200mW, compared with 450mW consumed by conventional gate driver.

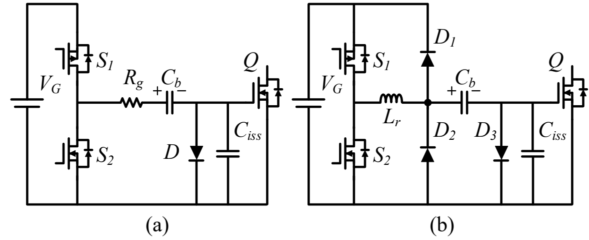

Fig. 5. Negative gate voltage topology. (a) Resonant tank included (b) Freewheeling diodes included

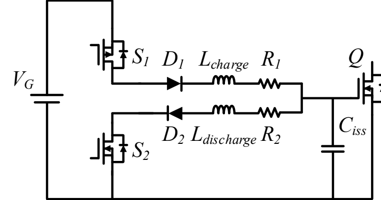

Fig. 6. Separate gate path topology.

Resonant gate driver with negative voltage driving capability is proposed in [20], which is shown as Fig.5 (a). Capacitor C_b and diode D_3 are installed in the gate path to provide negative driving voltage. A normally-on GaN transistor is fabricated in this paper to be applied in a 5.67W Class-E power amplifier operating at 13.56MHz. Based on the similar idea, energy recovery resonant gate driver with negative gate voltage is given in [21] and [22], which is shown as Fig.5 (b).

The resonant gate driver topology with controllable slew rate is proposed in [23] and further explored in [24] to fit for GaN HEMT application, which is shown as Fig. 6. The totem pole output is separated into charging and discharging path, where different resonant inductor are installed to provide asymmetric output. The topology is tested to drive the 600V commercial GaN HEMT. With 200V applied on the transistor, the gating loss is reported to steadily rise from 250mW to 1.04W, when switching frequency rises from 200kHz to 1MHz.

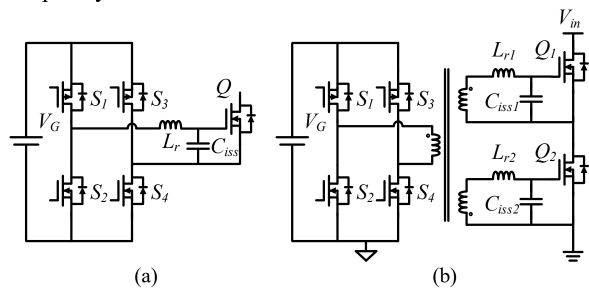

Fig. 7. Full bridge resonant gate driver. (a) For single transistor (b) For half bridge module

A full bridge configured resonant gate driver is proposed in [25], which is shown as Fig.7 (a). The proposed gate driver is tested in a 360kHz and 1kW MOSFET inverter, which helps to realize the overall efficiency of 99.1%. Compared with the conventional gate driver, gating loss is reported to be lowered from 9.3W to 0.9W. A further research of this topology is carried out in [26], which is shown as Fig.7 (b). Transformer with two secondary windings is integrated in

the gate driver to provide half-bridge driving capability. Converter overall efficiency is reported to be improved by 0.5% for 500kHz, 1kW full bridge inverter.

B. Non-zero initial inductor current gate driver

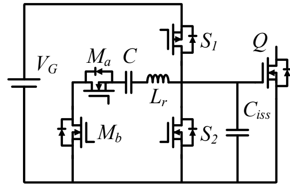

Fig. 8. Pulse resonant gate driver.

A pulse resonant gate driver, with online controllable slew rate, is proposed in [27], shown as Fig. 8. The basic idea is to generate initialized current to charge or discharge the gate capacitor C_{iss}. M_a and M_b are ancillary switches, which is in reverse series connection to provide separate path for charging and discharging *LC* resonant tank. Both driving switches pair and ancillary switches pair operate in complementary conduction mode, where phase shift control is utilized to control the slew rate. PSPICE simulation result is given for 12V 1MHz switching condition. Switching loss is reported to be 330mW when rise/fall time is 25ns and 420mW when rise/fall time is 20ns.

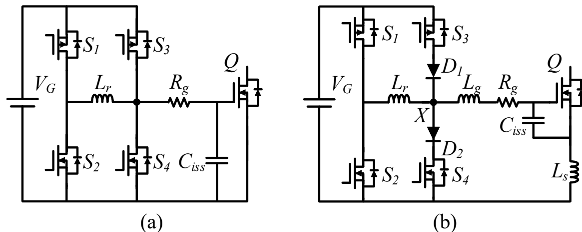

Fig. 9. Gate power recovery topology. (a) Two totem pole topology (b) Gate impedance insensitive topology

The resonant gate driver with power recovery capability is proposed in [28], shown as Fig.9 (a). A small resonant inductor is connected between two totem pole transistor pairs. Excessive inductor stored energy is returned to the line voltage source V_G and power MOSFET *Q* is charged with a non-zero initial current. 6.5% overall efficiency improvement is reported to be achieved in a 1MHz 12V Boost converter. The same idea is studied in [29] to provide dual-channel output, which is reported to reduce the gating loss by 67% compared with conventional non-resonant gate driver. A further research into this topology is given in [15], shown as Fig.9 (b). Schottkey diodes D1 and D2 are installed to recovery excessive gate power as well as clamp the gate voltage during this process, which helps the resonant tank design less sensitive to the parasitic component on the gate path.

Self-oscillating resonant gate driver is one special category in this classification. Different from totem pole based gate driver, additional gate transistor is not needed in the design. Drain source voltage of the transistor is fed back to the resonant tank and thus a close loop is formed to maintain self-oscillating. As a result, volume of the gate driver can be minimized to achieve high power density. Furthermore, switching frequency of the gate signal is no longer limited by the gate transistors, which can be largely increased to meet for very-high-frequency application.

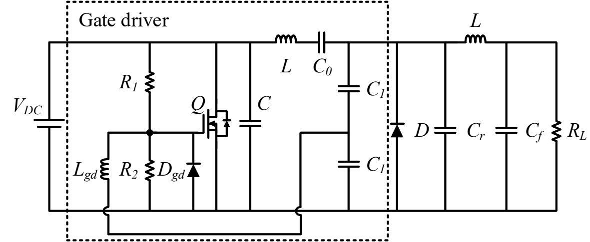

Fig. 10. Self-oscillating resonant gate driver.

One application of self-oscillating gate driver is researched in [30]. A VHF Class E DC-DC converter is built to operate in the whole VHF band width from 30MHz to 300MHz. Self-oscillating gate driver is utilized in the Class-E inverter part, which is shown as Fig. 10. Gating loss is reported to be 290.4mW and switching loss is reported to be 933.7mW at 100MHz according to the simulation result based on transistor MRF6V2010NR1. Other application of self-oscillating resonant gate driver can be found in [31] for Class-Φ2 inverter application and [32] for boost converter application.

The salient drawback of the self-oscillating gate driver is that impedance matching must be considered in the converter output. The inverter output must be followed by a rectifier stage designed accordingly to generate the desired self-oscillating gate signal [30]-[32]. As a result, application of self-oscillating gate driver is limited to DC-DC converter design, which is widely adopted in the audio amplifier.

III. CASE STUDY

A. Summary of literature review

From literature review in the last chapter, several conclusions can be made:

1) General idea for resonant gate driver is the construction of resonant tank.

2) General idea for resonant gate driver with negative voltage driving capability is the resonant capacitor in series installed to gate path.

3) Controllable slew rate is one popular research topic, which is generally achieved by separate gate path or phase shift control scheme.

4) Efficient power recovery is one popular research topic, which is generally achieved by additional diodes or ancillary switches to provide current returned path.

5) Additional gate transistors are essential for non-zero initial inductor current gate driver.

6) Self-oscillating gate driver requires impedance match which is optimal for VHF DC-DC converter design.

Several problems need further research include:

1) Different topologies are researched in different application circumstances. A general evaluation method for resonant gate driver is absent.

2) In many researches, only overall efficiency improvement of the converter is given to validate the feasibility of the proposed topology. Detailed loss analysis is essential.

3) Many topologies are researched based on the application in conventional silicon MOSFET. Performance in the GaN HEMT application need to be further evaluated.

B. Case Analysis

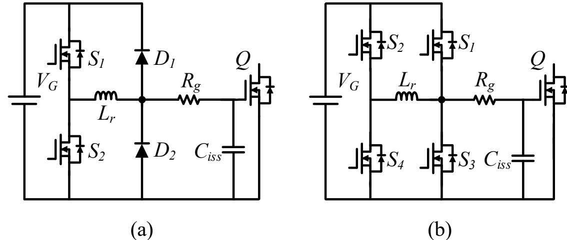

Fig. 11. Gate driver topologies. (a) Case A (b) Case B

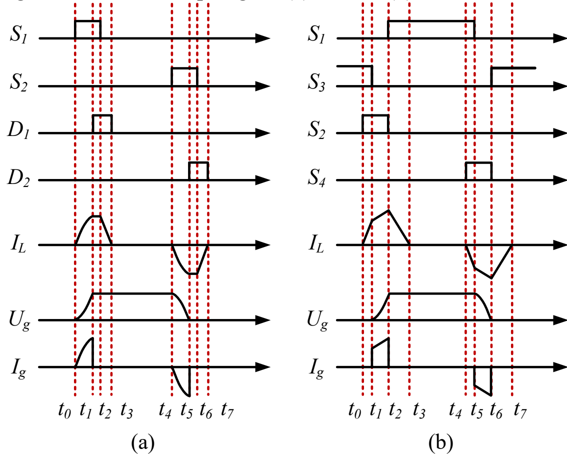

Fig. 12. Ideal waveform. (a) Case A (b) Case B

According to analysis above, case study of two resonant gate drivers is carried out. Case A is the zero initial inductor topology proposed in [11] and Case B is the non-zero initial inductor current topology proposed in [28]. Two topologies are similar in structure and both topologies implement the idea of energy recovery, which is optimal for comparison. Topologies of Case A and Case B are shown in Fig. 11.

The ideal operating waveform of two topologies is shown in Fig. 12. For intuitive comparison, all the transistors in both topology are selected as n-mos. Topology of Case A is composed of a conventional totem pole, a resonant inductor and two schottkey diodes. Input capacitor of Q is charged during $t_0 \sim t_1$, along with charging of the resonant inductor. Energy recovery takes place during $t_2 \sim t_3$ and the conventionally wasted energy is returned to the gate voltage source via the path of S_2 body diode, L_r and D_1. In Case B, two schottkey diodes are replaced with another totem pole. Accordingly, the resonant inductor is pre-charged via the path of S_2, L_r and S_3. After that, the inductor current charges the input capacitor of Q during $t_1 \sim t_2$. Energy recovery takes place during $t_2 \sim t_3$ via the path of S_4 body diode, L_r and S_1.

According to the analysis above, gate energy can be recycled in both Case A and Case B, via a similar conduction path. The extra totem pole in Case B provides a pre-charging stage of the resonant inductor and thus results in fast gate charging/discharging capability. Shortened switching transient of the driven transistor shall reduce the switching loss and further improve the power conversion efficiency.

C. Test Benchmark Specification

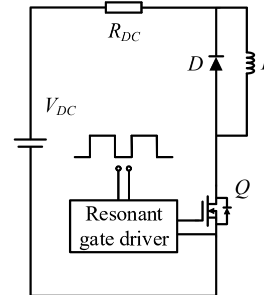

Fig. 13. Resonant gate driver characterization circuit.

The general method for transistor loss characterization is double pulse tester, which is widely adopted in [33]-[35]. However, in case of resonant gate driver, the first pulse, which is conventionally used for current forming, will interfere with the charging state of the resonant inductor and thus cannot be directly applied. As a result, based on the idea of conventional double pulse tester, topology for resonant gate driver characterization is proposed in this paper, which is shown in Fig. 13. Repetitive gate signal with fixed duty ratio is generated by the resonant gate driver. Resistor R_{DC} is installed in the power loop to adjust the switching current of the driven transistor. Schottkey diode is installed in parallel to the inductor L to provide a circulating current path during the transistor Q gated off

TABLE I
PARAMETERS OF DRIVEN TRANSISTOR

	IPW60R045CP	GS66516B
Type	MOSFET	GaN HEMT
V_{DS}	650V	650V
I_D	60A	60A
Q_g	150nC	12.1nC
V_{GS}	±20V	-10V to +7V

Conventional totem pole gate driver and resonant gate driver in both cases are tested. Transistor Q is selected as MOSFET and GaN HEMT respectively to evaluate the loss of two resonant gate drivers. Parameters of each transistor are shown in Table I. Two transistors have the same power rate. Benefit from the wide band gap characteristic of GaN HEMT, GS66516 enjoys a much smaller gate charge (Q_g) and lower gate voltage (V_{GS}). Transistor in gate driver is selected as IRF7309N for both cases. Resonant inductor in Case A and Case B are designed according to the design rules specified in each paper. Calculation equation from Case A and Case B are shown in (2) and (3) respectively:

$$L_R \le \frac{1}{C_G} \times \left(\frac{2 \times t_{rise}}{\pi} \right)^2 \tag{2}$$

$$L_R = \frac{V_{cc} t_{rise}}{Q_G} \times \left(\frac{t_{rise}}{4} + t_d \right) \tag{3}$$

, where t_{rise} represents the gate voltage rising time ($t_0 \sim t_1$ in Case A and $t_1 \sim t_2$ in Case B) and t_d represents the inductor pre-charging time ($t_0 \sim t_1$ in Case B).

D. Simulation results

1) Gate waveform

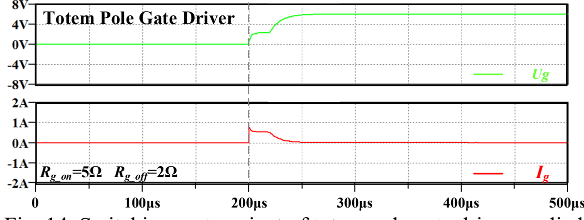

Fig. 14. Switching on transient of totem pole gate driver applied in GaN HEMT.

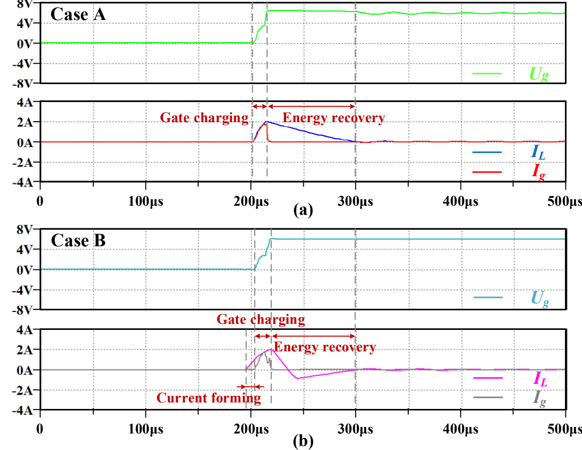

Fig. 15. Switching on transient of resonant gate driver applied in GaN HEMT. (a) Case A (b) Case B

Both of the two resonant gate drivers are originally proposed for silicon MOSFET application. As a result, gate waveform will be given for their GaN HEMT application. Simulation is carried out in LTSpice and transistor models are obtained from each manufacturer. Switching frequency is 100 kHz. As a comparison, simulation results of the conventional totem pole gate driver is given in Fig. 14.

Gate waveform of two resonant gate drivers applied for GaN HEMT is given in Fig. 15. U_g is the gate voltage and both of the two cases show good gate driving capability in GaN HMET application. I_L and I_g are the resonant inductor current and gate charging current respectively. The gate charging current rises along with the resonant inductor current in Case A. While in Case B, there is a current forming stage in the resonant inductor before the gate capacitor is charged. Also, there's a noticeable current ringing in the resonant inductor during energy recovery for Gate B application, which is resulted from the oscillation of resonant inductor and the parasitic capacitor of gate transistors. From simulation results, it can be concluded that resonant gate drivers from both Case A and Case B show well capability in GaN HEMT application. Waveform validates the energy recovery process researched in two cases.

2) Gate charging capability

In conventional totem pole gate driver, gate charging current is controlled by the gate resistor. Gate-on resistor is 5 Ω and gate-off resistor is 2 Ω, which is the typical value specified in GS66516B application note from the manufacturer. For resonant gate driver, gate charging current is related to the resonant inductor. In Case A, the gate charging speed is solely determined by the time constant of the resonant tank (L_r and C_{iss}). In Case B, the gate charging speed is determined by the resonant inductor current as well as the gate charging time. As a result, benefit from the two extra gate transistors, resonant gate driver in Case B can achieve online changeable slew rate.

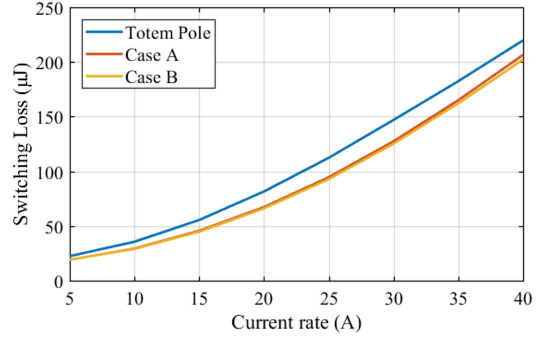

Fig. 16. Switching loss characterization.

From the simulation result, it should be noted that the peak gate charging current of conventional totem pole gate driver is less than 1A and decays quickly. For resonant gate driver, the peak gate current is around 1.9A in two cases. A faster gate charging speed will result in a faster transistor switching transient, which will thus lead to a lower switching loss in the driven transistor. To validate the analysis, loss characterization of GaN HEMT is carried out in simulation, which is shown in Fig. 16. Conventional totem pole gate driver and resonant gate drivers in two cases are tested respectively to obtain the switching loss. GS66516B is tested to switch at fixed drain-source voltage (V_{ds}=400V) and a large range of source current (I_{ds}=5A~40A). According to the simulation results, switching loss characterization is pretty identical in Case A and Case B, which is resulted from the similar gate charging current. Compared with conventional totem pole gate driver, there's a noticeable reduction of switching loss when resonant gate driver is applied. At 40A source current, switching loss can be reduced by 7.7% compared with conventional totem pole gate driver.

3) Gating loss evaluation

TABLE II
GATE LOSS ANALYSIS IN SILICON MOSFET APPLICATION

	Totem pole	Case A	Case B
Gating loss	2.86 μJ	1.62 μJ	1.37 μJ
Gate driver E_{sw}	0.29 μJ	0.37 μJ	0.51 μJ
Overall gate driver loss	3.15 μJ	1.99μJ	1.88 μJ

One salient advantage of resonant gate driver is the reduction of gating loss. The overall gate driver loss can be categorized into two parts: the driven transistor gating loss and the gate transistor switching loss (E_{sw}). Gate loss analysis in Silicon MOSFET application is shown in TABLE II. Compared with the conventional totem pole gate driver, gating loss is significantly reduced by 44.4% and 52.1% in Case A and Case B respectively. On the

other hand, extra components in resonant gate driver introduces additional gate driver E_{sw} in both cases. The overall gate driver loss is reduced by 36.8% and 40.3% in Case A and Case B respectively.

TABLE III
GATE LOSS ANALYSIS IN GAN HEMT APPLICATION

	Totem pole	Case A	Case B
Gating loss	55.4nJ	25.4nJ	23.4nJ
Gate driver E_{sw}	98.7nJ	102.94nJ	113.1nJ
Overall gate driver loss	154.1nJ	128.34nJ	136.5nJ

Gate loss analysis in GaN HEMT application is shown in TABLE III. Benefit from small input capacitor, GaN HEMT has a much lower gating loss compared with its Silicon MOSFET counterpart. Resonant gate driver in Case A and Case B reduces 54.2% and 57.8% of the conventional gating loss respectively. It should be noted that gate driver switching loss is the majority of overall gate driver loss in the case of GaN HEMT application. As a result, the overall gate driver efficiency is merely improved by 16.7% in Case A and 11.4% in Case B.

IV. CONCLUSIONS

In this paper, a thorough review of resonant gate driver for switching application is given. Two general categories, zero initial inductor current topology and non-zero initial inductor current topology, are analyzed and compared in details. According the case study, several conclusions can be made:

(1) Both of the two categories of resonant gate driver can effectively reduce the gating loss in Silicon MOSFET and GaN HMET application.

(2) Resonant gate driver is capable of forming large gate charging current, which helps to reduce the switching loss of driven transistor.

(3) For the zero initial inductor current category, topology and control is rather simple, which is highly reliable and capable of integrating the commercial half bridge gate driver.

(4) For the non-zero initial inductor current category, gating loss can be further reduced. Gate charging current is online changeable with the extra gate transistors. However, complicated controller design limits its application in the multi-transistor topologies.

(5) Reduction of overall loss in resonant gate driver is not evident for GaN HEMT application. Switching loss of the transistors in gate driver contributes to the majority of gate driver loss.

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