Waller, W. M., Gajda, M., Pandey, S., Donkers, J. J. T. M., Calton, D., Croon, J., ... Kuball, M. (2017). Control of Buffer-Induced Current Collapse in AlGaN/GaN HEMTs Using $SiN_X$ Deposition. *IEEE Transactions on Electron Devices*, *64*(10), 4044-4049. [8013764]. https://doi.org/10.1109/TED.2017.2738669

Peer reviewed version

# Control of Buffer Induced Current Collapse in AlGaN/GaN HEMTs Using $SiN_x$ Deposition

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***Abstract*— The stoichiometry of LPCVD $SiN_x$ surface passivation is shown to change vertical conductivity at the top of the epitaxial stack in GaN-on-Si power HEMTs. This changes the charge stored in the carbon doped GaN layer during high voltage operation, and allows direct control of buffer-related current collapse in HEMTs. Substrate bias ramps are used to identify the changes in C:GaN charge trapping and vertical leakage. Channel length dependence indicates a lateral conductivity in the C:GaN with a localized increase in vertical conductivity under the Ohmic contacts. An optimum $SiN_x$ recipe is identified which simultaneously delivers low current-collapse and low drain leakage.**

***Index Terms*— AlGaN/GaN HEMT, buffer trapping, passivation.**

## I. Introduction

The low on-resistance and high breakdown voltages that can be realized using GaN high electron mobility transistor technology have generated much interest for power applications. However, dynamic on-resistance is still a problem for maximizing the potential of this technology. This "current collapse" problem is due to negative charge trapping in the device when it is held in the high voltage off-state. This charge then persists in the on-state partially depleting the channel, reducing carrier concentration and mobility [1]. The location of this trapped charge has been reported as being above the channel [2] and below the channel in the carbon-doped GaN layer (C:GaN) [3]. Previous work has shown several ways to control increased dynamic on-resistance such as introducing fieldplates [4], making changes to the $SiN_x$ deposition process [5,6] and changing GaN epitaxial growth [7,8]. Until now these two trapping locations were thought to be independently controlled, however this work demonstrates that changes to the bulk C:GaN layer trapping can be caused by modifying the surface passivation process [9]. Specifically, changing the stoichiometry of low pressure chemical vapor deposition (LPCVD) $SiN_x$ increases vertical conductivity of the GaN located below the 2DEG channel and results in completely different charge trapping below the 2DEG, both vertically and laterally. Modifying the LPCVD $SiN_x$ has already been shown to cause changes to surface trapping, leakage and fieldplate pinch off voltages and a detailed analysis of these properties can be found in [10]. In addition to these surface changes we demonstrate here its impact upon the epitaxial conductivity and consequently the buffer contribution to current collapse. We focus on the changes to charge storage below the channel and demonstrate that optimization of the $SiN_x$ stoichiometry can deliver low buffer induced current-collapse. The results described here are entirely consistent with a "leaky dielectric" model for buffer induced current-collapse. [11]

## II. Devices and Measurements

GaN-on-Si wafers were grown with nominally identical epitaxy and have been described in detail in another publication [10]. These wafers had a strain relief layer, a carbon doped GaN layer, an unintentionally doped GaN channel, a 20nm AlGaN layer and a 3nm GaN cap making a total epitaxial thickness of ~5µm. The difference between these wafers is the subsequent 70nm of LPCVD $SiN_x$ grown to passivate the surface, the stoichiometry of this layer was varied by changing the dichlorosilane (DCS) to $NH_3$ ratio during growth. Four representative wafers have been chosen to show the range of

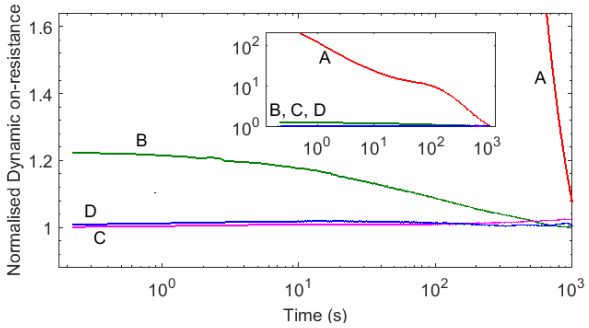


Fig. 1. Normalised Dynamic on-resistance measured on MISHEMTs fabricated on wafer A to wafer D after a stress condition of $V_D = 100V V_G = -15V$ held for 1000s. On condition is $V_D = 1V, V_G = 0V$, current is plotted against time-after-switching. Inset is a log-log scale plot (same axes) to show the extent of current collapse in wafer A.

Manuscript received July XX, 2016; revised July XX, 2016; accepted February XX, 2016. Date of publication July XX, 2016; date of current version February XX, 2016 …

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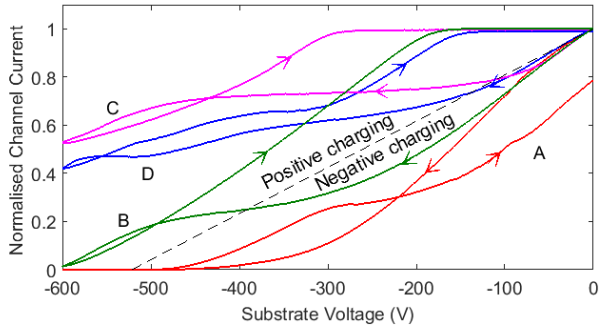


Fig. 2. Normalised channel current measured on 35µm TLM structures as the Si substrate is swept to -600V and back. This is an equivalent vertical electric field to normal MISHEMT operating condition of positive voltage applied to the drain. Wafer A shows negative charge storage and current collapse, wafers B-D show positive charge storage. Wafers C&D do not pinch-off. Expected capacitively coupled behavior is depicted as dashed line.

behavior. The $SiN_x$ varies from stoichiometric $Si_3N_4$ on wafer A to a Si-rich $SiN_x$ on wafer D.

MISHEMTs were then fabricated and had a gate width of 100µm and a threshold of -11±0.5V. These devices also had full fieldplate structures consisting of a gate wing and two

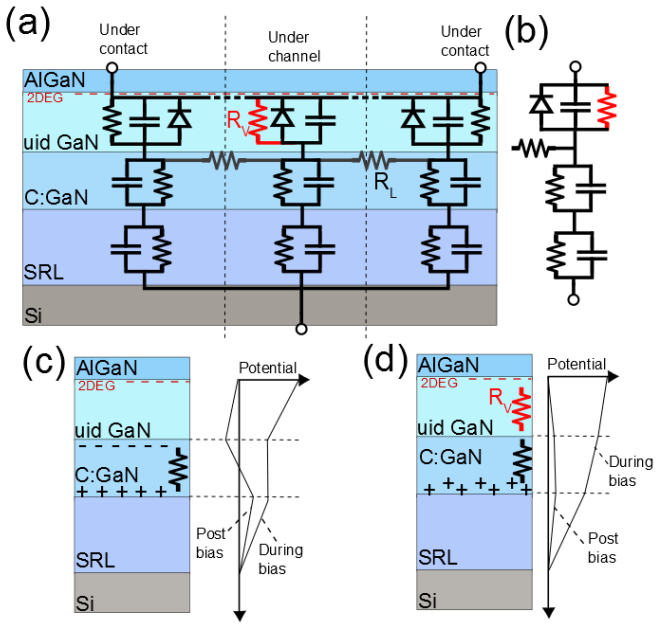


Fig. 3. (a) Lumped element equivalent circuit of epitaxial stack. The diode behavior of the uid GaN layer is due to the pin junction between the n-type channel and the p-type C:GaN. The vertical conduction path, $R_V$, is changed between the wafers. (b) 1D simplification of model. (c) Location of charge when C:GaN is the least resistive layer, this leads to current collapse. (d) Location of charge when uid-GaN is the least resistive layer, this leads to positive charge storage, this can exit the stack due the forward biased diode.

subsequent fieldplates at thicknesses of 70nm, 370nm and 670nm respectively. Full details of this fieldplate structure and threshold voltages are outlined in [10]. These devices were used to measure current collapse. For measuring the impact of substrate bias ramps TLM structures were used with a width of 100µm and a range of contact spacings. A number of specially fabricated HEMT devices with a Schottky sense contact placed at different positions in the channel were used to measure

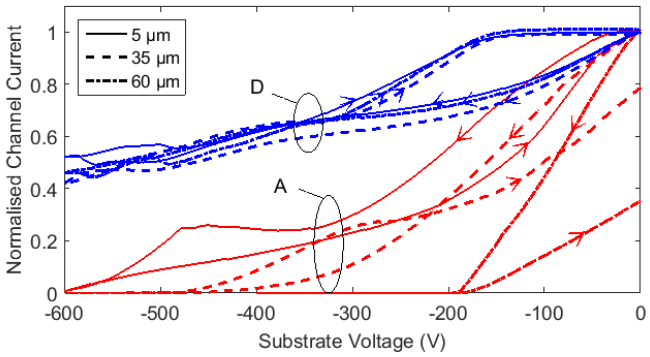


Fig. 4. Normalised channel current for wafers A&D measured on fresh TLM structures of different spacing. There is minimal variation between the measurements for wafer D, wafer A has a strong gap dependence.

channel potential [10,12]. Forcing a small forward-bias current across this extra contact measures the potential at that position.

## III. Results and Discussion

### A. Dynamic $R_{ON}$ Measurement

Normalized dynamic Ron measured on MISHEMTs fabricated on wafers A to D are shown in Fig. 1. This is after a stress condition of $V_D = 100$V, $V_G = -15$V held for 1000s. ON-state is $V_D = 1$V, $V_G = 0$V. $V_D$ =100V has been chosen for the OFF-state stress as this is close to the peak dynamic Ron seen on these types of devices. [13] Wafer A exhibits significant current collapse and wafer C and D have almost none. Wafer B corresponds to close to optimum with a low off-state drain leakage (shown in [10]) and low current-collapse. This measurement, on its own, does not distinguish between trapping above and below the channel. A full study of surface effects is found in [10] and shows only a small surface contribution to current collapse. The focus of this paper is trapping below the 2DEG.

### B. Substrate Ramp

To investigate the contribution to this current collapse from trapping below the 2DEG, the substrate bias ramp technique was used. Prior to 2DEG pinch-off, this technique is surface-insensitive and probes only the region of the device below the channel as the 2DEG screens the surface from the electric field induced by a substrate bias. The technique is especially sensitive to changes in the resistivity of the UiD (Unintentionally Doped) channel and C:GaN [14,15]. Interpretation is discussed in more detail in [11, 16-18]. TLM structures with a contact gap of 35 µm were used and the substrate was swept to −600V and back to 0V at 9.2V/s while a source to drain voltage of 1V was applied. The normalized drain current measured on the different wafers is plotted in Fig. 2. The dashed line indicates predicted channel current as the Si substrate acts as a back-gate and pinches the device off at −520V. This assumes that the epitaxial stack behaves like a dielectric and there is no charging, hence the stack behaves like a perfect capacitor with capacitance $\varepsilon/d$ for a dielectric

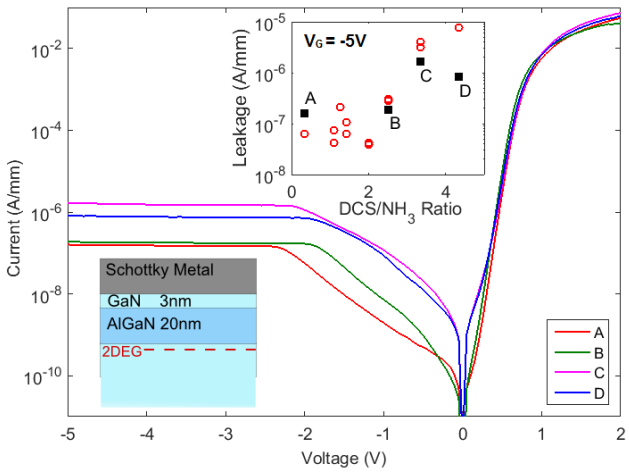


Fig. 5. Schottky diode forward and reverse bias characteristics. Shows change in conductivity in reverse bias that is linked to DCS/$NH_3$ fraction. This indicates a change in vertical conductivity through the AlGaN barrier layer. Inset (top) is plot of leakage at $V_G$ = -5V for a larger set of wafers showing that results follow a trend. Inset (bottom) is cross section of Schottky junction.

constant of $\varepsilon = 10.4$ [19] and thicknesses, $d$. It also assumes a constant mobility. Any deviation above the line indicates positive charge storage (weighted towards charge at the top of the stack), and deviation below the line indicates negative charging. The highly surprising result is that Fig. 2 demonstrates that the previously identically-grown epitaxy has been modified by the different passivations. Wafer A shows negative charge storage after the ramped stress leading to a reduced 2DEG current. In contrast wafers B-D recover quickly to the initial state. For wafers C & D there is no negative charge storage at any point in the ramp, with wafer B showing some negative charge storage at moderate bias. Wafer C has the highest positive charge during a ramp, this is consistent with following measurements and represents statistical variation between wafers. These results probe the vertical transport and are consistent with Fig. 1. A full description of charge trapping in the HEMT will also depend on the horizontal transport.

The C:GaN layer is known to be weakly p-type, [20, 21] so to understand the charge storage in this layer we must consider the vertical structure of the device [15-18]. Figure 3 depicts a simple circuit model of the different layers of the device. The difference between the wafers can be explained if the leakage through the UID GaN layer is modified. The charge stored in the C:GaN layer is dictated by the relative resistances of the

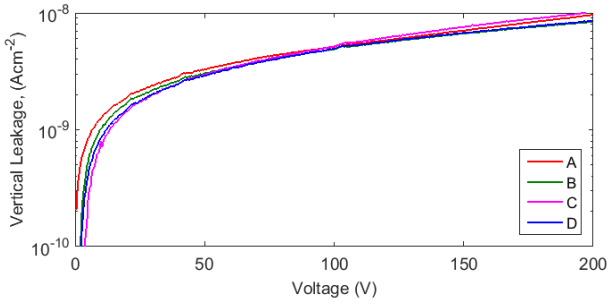


Fig. 6. Vertical leakage under isolated $1.4\times10^{-3}$cm$^2$ CTLM contact on wafers, there is very little difference between the vertical leakages, this suggests any changes to the vertical conductivity in the wafers is confined to near the surface.

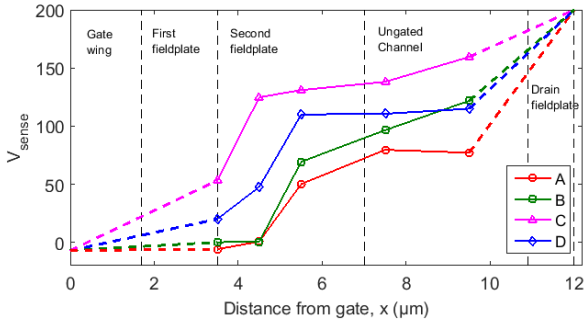


Fig. 7. Potential measured in channel at different positions between the gate and drain while device is held in off-state ($V_D$ = 200V, $V_G$ = -7V). Lines are extrapolated to gate and drain potentials. Potential is dropped more near the drain for wafer A and more near the gate for wafers C&D.

different layers of the stack, depicted in Fig 3(c)&(d). If the upper part of the stack is leaky, indicated by the resistor marked $R_V$ in Figs. 3(a)&(b) then positive charge is stored in the C:GaN layer when under bias. If the UID GaN is highly resistive then charge redistribution can occur in the C:GaN (Fig. 3(c)), or net negative charging if the SRL layer is more leaky. The diode in Fig. 3 is due to the p-i-n junction between the weakly p-type C:GaN [20, 21], intrinsic UID-GaN and effectively n-type 2DEG. The source of positive charge in the case of Fig. 3(d) could be from a band-to-band variable-range-hopping conduction process [22].

In this 1D model, wafers C and D up to -500V and wafer B above -200V would correspond to Fig. 3(d), where leakage through the UID GaN layer allows positive charge to accumulate in the C:GaN layer, this leakage must be of the order of 50nA/cm$^2$ at this sweep rate to avoid changes in 2DEG density. Wafer B in the range −50 to −200V would correspond to Fig. 3(c), suggesting no leakage through the UID GaN and charge redistribution in the C:GaN layer causing a small current-collapse. Wafer A is more complicated and is discussed below.

To investigate the mechanism of this change in resistance, further substrate bias measurements were made with different TLM spacing. Only two wafers have been shown for clarity in Fig. 4. Wafer D has no TLM spacing dependence, suggesting that the leakage path between the 2DEG and the C:GaN inferred in the previous section exists for the entire source to drain region, and the stack behaves as in the 1D model of Fig 3(b). This behavior was also seen in wafers B and C (not shown). By contrast, wafer A has strong TLM gap dependence. A large spacing of 60 μm leads to significant current collapse and a voltage of only around -200V is needed to deplete the channel, whereas when performed on a small spacing of 5 μm the channel does not deplete until -600V and the reduction in channel current after the bias ramp is minimal. This indicates the presence of vertical conduction under the Ohmic contacts down to the C:GaN (as discussed in [15,18]), preventing the accumulation of negative charge under the contacts. To explain this spacing dependence the lateral charge transport in the C:GaN layer, $R_L$, must be highly resistive as otherwise the area under the channel would be at the same potential as the area under the contact, hence a 1D model of the device is not sufficient. Wafer A behaves as in Fig 3(a) with highly resistive

$R_V$ and $R_L$.

### C. Schottky Response

Forward and reverse bias characteristics on Schottky diodes were measured and are shown in Fig. 5 together with a schematic of the device where fieldplates and passivation have been omitted. This leakage is predominantly vertical, we have deduced this from leakage scaling with device area (not shown). When reverse biased and at small forward biases the leakage is linked to $SiN_x$ type. The second inset shows how the reverse bias leakage at $V_G$=-5V on wafers A-D follow a trend against $SiN_x$ type from a larger batch of wafers. This increase in conduction is consistent with an increase in vertical conductivity through the AlGaN barrier. As discussed in the previous section, substrate bias measurements in Figs. 2&4 demonstrate a change in vertical epitaxial conductivity through the uid-GaN linked to LPCVD $SiN_x$ type. We therefore arrive at the conclusion that changing the passivation stoichiometry must increase conductivity of the epitaxy nearest to the surface, both the AlGaN and the UiD-GaN. Wafer C has consistently shown slightly higher leakage than wafer D indicating some manufacturing variation.

### D. Vertical Leakage

Vertical leakage through the entire epitaxial stack was measured. Fig. 6 depicts this current and there is no significant difference in vertical leakage between the wafers. There are two possibilities to reconcile this observation with the previous sections. First, any changes to the vertical conductivity in the wafers are primarily confined to near the surface and only affect charge redistribution in the top part of the stack. Alternatively the leakage seen in Fig. 6 through the entire stack may be dominated by preferential widely spaced leakage paths [16] which dominate over the small changes in leakage inferred from substrate ramps and which extend over the entire surface of the device.

### E. Lateral Potential Distribution

The lateral distribution of charges in the C:GaN layer will impact not only current collapse in a device but also the electric field distribution in the channel [12,13]. Fig. 7 depicts the channel potential measured in off-state HEMTs ($V_D$ = 200V $V_G$ = -7V) using Schottky sense-contact devices. Some of the variation in potential between wafers can be attributed to fieldplate dielectric leakage [10]. However, there is a clear trend linked to the vertical conductivity at the surface of the epitaxy, inferred from substrate sweeps (Fig.2) and Schottky leakage measurements (Fig. 5). Wafers with high vertical conductivity (C & D) have a stronger electric field near the gate edge, whereas wafer A with low vertical conductivity has a much higher field at the drain edge.

### F. Suggestions for a Physical Mechanism

A change in vertical conductivity at the surface of the epitaxy linked to LPCVD SiNx stoichiometry has been consistently observed. This processing step is therefore critical for determining the magnitude of buffer-trapping related current collapse on the wafer and the off-state electric field distribution in the channel.

The change to diffusivity of ions through this $SiN_x$ blocking layer is a plausible cause and is a concept well understood from Si technologies [23]. It is known that a change in growth conditions modifies the growth morphology and internal stress of the $SiN_x$ layer [24, 25, 10], the stoichiometric $Si_3N_4$ will have less voids and therefore will have the highest ion blocking ability. It would then be in various high temperature processing steps such as the Ohmic anneal or further $SiN_x$ deposition that ion diffusion could occur.

A possible ion candidate would be H+ due to its high mobility in GaN [26] and its abundance during processing. These ions would be attracted to negatively charged threading dislocations due to their trapping of electrons [27], this could change their electrical conductivity and hence the vertical conductivity in the surface epitaxy.

An alternative picture would be diffusion of nitrogen out of the epitaxy, it has been shown that nitrogen can diffuse from the surface leaving vacancies which increase leakage [28]. Future work should investigate the mechanism for this observed increase in vertical conductivity in these devices. Secondary Ion Mass Spectroscopy, (SIMS), was unable to discern any significant differences between the wafers, this is not surprising if the mechanism is hydrogen decoration of dislocations or nitrogen vacancies. Hydrogen can only be detected above 0.1% atomic percent and this measurement is averaged over the entire beam area. Nitrogen vacancies are not detectable either.

## IV. Conclusion

Bulk-trapping related dynamic on-resistance (current collapse) is suppressed by changing the stoichiometry of LPCVD $SiN_x$ passivation after epitaxial growth. Substrate bias ramps have been used to show that the current collapse is suppressed by an increase in vertical leakage in the upper part of the buffer.

The highly surprising conclusion is that changes to the surface passivation can result in changes to the carrier transport in the bulk of the epitaxial buffer.

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