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Effect of Logic Family on Radiated Emissions from Digital Circuits

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***Abstract*—Radiated emissions were measured for simple digital circuits designed to operate with various logic families. Emissions in the near and far field were found to depend both on the circuit layout and the choice of logic family. However, the difference in peak emissions between any two logic families was found to be independent of circuit layout. The greatest difference in peak emissions was between high-speed 74ACT logic and low-speed 4000 CMOS logic devices, with a mean value of approximately 20 dB. Emissions from a more complex circuit were compared with the measurements on simple loop circuits. Test circuits were used to measure the propagation delay, the rise and fall times, the maximum operating frequency and the transient switching currents between two successive logic gates for each logic family. Empirical formulas have been derived that relate relative peak emissions to these switching parameters. It is hoped that these will assist designers to assess the effect of choice of logic family on electromagnetic compatibility.**

***Index Terms*— Digital circuits, electromagnetic compatibility, electromagnetic interference, logic circuits, radiated emissions.**

I. Introduction

Digital circuits are a source of broad-band electromagnetic radiation due to the harmonic content of pulsed waveforms with fast transitions. The level of this radiation depends on several factors including choice of components, clock frequency, circuit layout, and shielding. However, the relative importance of these factors is often not adequately quantified. In this paper, we consider the effect of choice of logic family. Our aims are to compare the radiated emissions from circuits using commonly available logic families and to investigate how the results correlate with some important switching parameters of the logic devices.

The work described forms part of a project to identify those aspects of electronic design that are critical to the electromagnetic compatibility (EMC) of equipment. Quantitative knowledge of EMC factors will enable designers to make effective decisions at an early stage in the design process. If designers are able to compare the relative merits of different methods of achieving EMC (e.g., using a slow-logic family or a circuit board with a ground plane), then they will be able to optimize their designs rather than be forced to apply more counter measures than may be necessary. The ultimate goal of our work is to reduce the problem of designing for EMC to an "EMC equation"

$$\text{'EMC'} = \sum_i G_i \tag{1}$$

and a "cost equation"

$$\text{'cost'} = \sum_i c(G_i) \tag{2}$$

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where G_i are the contributions to EMC from various design factors (e.g., layout, shielding, or choice of components) and $c(G_i)$ are the costs of implementing them. The aim of the designer would then be to minimize $\Sigma_i\ c(G_i)$ while obtaining a sufficient level of $\Sigma_i\ G_i$.

A. Radiation from Digital Circuits

It is known that clock signals are often the major source of RF radiation from digital circuits [1], [2]. The waveforms of these signals are approximately trapezoidal with finite rise and fall times.

In the frequency domain, a periodic train of pulses has a line or comb spectrum. The frequencies are harmonics of the clock frequency, while the envelope of the spectrum is the Fourier transform of the pulse shape. If the pulse is trapezoidal with rise time τ_r and fall time τ_f, then the magnitude of the coefficient of the nth harmonic $|c_n|$ is given by

$$|c_n| = \frac{A}{\pi n}\left|\frac{\sin(\pi n\tau_r/T)}{\pi n\tau_r/T}\,e^{j\pi n\tau/T} - \frac{\sin(\pi n\tau_f/T)}{\pi n\tau_f/T}\,e^{-j\pi n\tau/T}\right| \tag{3}$$

where A is the amplitude, T the period, and τ the pulse width [3]. If the pulse is symmetrical then $\tau_r = \tau_f$ and (3) simplifies to

$$|c_n| = 2A\,\frac{\tau}{T}\left|\frac{\sin(\pi n\tau/T)}{\pi n\tau/T}\right|\left|\frac{\sin(\pi n\tau_r/T)}{\pi n\tau_r/T}\right|. \tag{4}$$

The value of $|c_n|$ tends to fall with frequency at a rate of 20 dB per decade at frequencies above $1/\pi\tau$ and at 40 dB per decade at frequencies above $1/\pi\tau_r$.

Digital circuits are able to radiate when the signal and power tracks connecting integrated circuits (IC's) act as an antenna. The radiation from a circuit, therefore, depends both on the harmonic content of the signal and on the efficiency of the antenna. The latter rises with frequency until the size of the circuit becomes comparable to the wavelength of the radiation. Combined with the falloff of $|c_n|$ with frequency, this often leads to the peak radiated emission occurring at a frequency of several hundred megahertz. In this work, we are particularly concerned with peak radiation because this is of great importance as to whether a product complies with EMC legislation.

In the literature on radiation from digital circuits, there has been considerable work on the effects of layout and grounding, but comparatively little on the choice of logic family. White *et al.* [1] have estimated relative values of radiation as the product of gate current and operating bandwidth, but it is not clear whether these refer to peak or total radiation and the values are not supported by measurements. Koga *et al.* [4] have compared the emissions from three transistor–transistor logic (TTL) and two complementary metal-oxide-semiconductor (CMOS) families using a small loop antenna at 50 mm from the circuit. However, they have measured the total noise power rather than the peak harmonic and, unfortunately, the bandwidth of the noise detector is not stated. From the graphs that they have presented, the noise power from the highest and lowest emitters (74AC and 74ALS) appears to differ by a factor of approximately 3.2 (5 dB). Bush [2] has compared the spectra of a clock circuit with two different oscillator modules whose rise times were 1 and 5 ns. The difference in peak radiated emissions was approximately 12 dB. Turner [5] has presented spectra from identical circuits with three different logic families, measured on a test site at 3 m. From the graphs that are presented it can be seen that the peak emission from the circuit with 74F logic is 10 dB greater than that

TABLE I
LOGIC FAMILIES THAT WERE INVESTIGATED

Technology	family	τ_{pd} (ns)	P_d at 1 MHz (mW/gate)
TTL	74LS	10	2
	74ALS	4	1.3
	74F	3.5	5.4
CMOS	4000B	50	0.3
	74HC	9	0.5
	74HCT	9	0.5
	74ACT	3	0.5

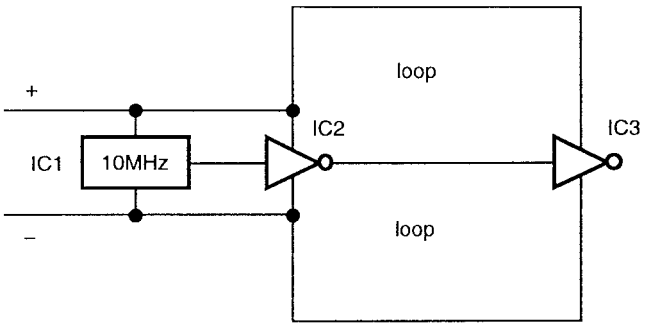


Fig. 1. Circuit for emissions testing.

with 74HCT logic and 12 dB greater than that with 74LS logic. In this paper, we present the first systematic study of the differences in emission due to logic family using circuits with various layout and grounding schemes.

II. CIRCUITS FOR EMISSIONS TESTING

A. Logic Families

Most logic IC's are available in several compatible families, each with its own power requirements and speed. Table I lists the three TTL and four CMOS families that were investigated, giving typical propagation delays τ_{pd} and power dissipation P_d when operated at 1 MHz [6].

B. Circuits

A set of simple circuits were designed for emissions testing. They consisted of a logic inverter driving either a second inverter or a passive load with a 10-MHz signal. They were battery operated so that the radiation would be solely from the printed circuit board (PCB) and not from cables. Fig. 1 is a diagram of a test circuit. IC1 is a 10-MHz oscillator module. IC2 and IC3 are either 74 × 04 or 4069 logic inverters where x is one of the families listed in Table I. All the IC's are decoupled with 100-nF ceramic capacitors. A second test circuit was also used in which IC3 was replaced by a passive load between the output of IC2 and ground.

The circuits were laid out on PCB's with IC1 as close as possible to IC2 and the tracks between IC2 and IC3 forming large radiating loops. Fig. 2 shows the three layouts that were used. In Fig. 2(a) the load Z was 390 Ω. Note that Fig. 2(c) can be configured to

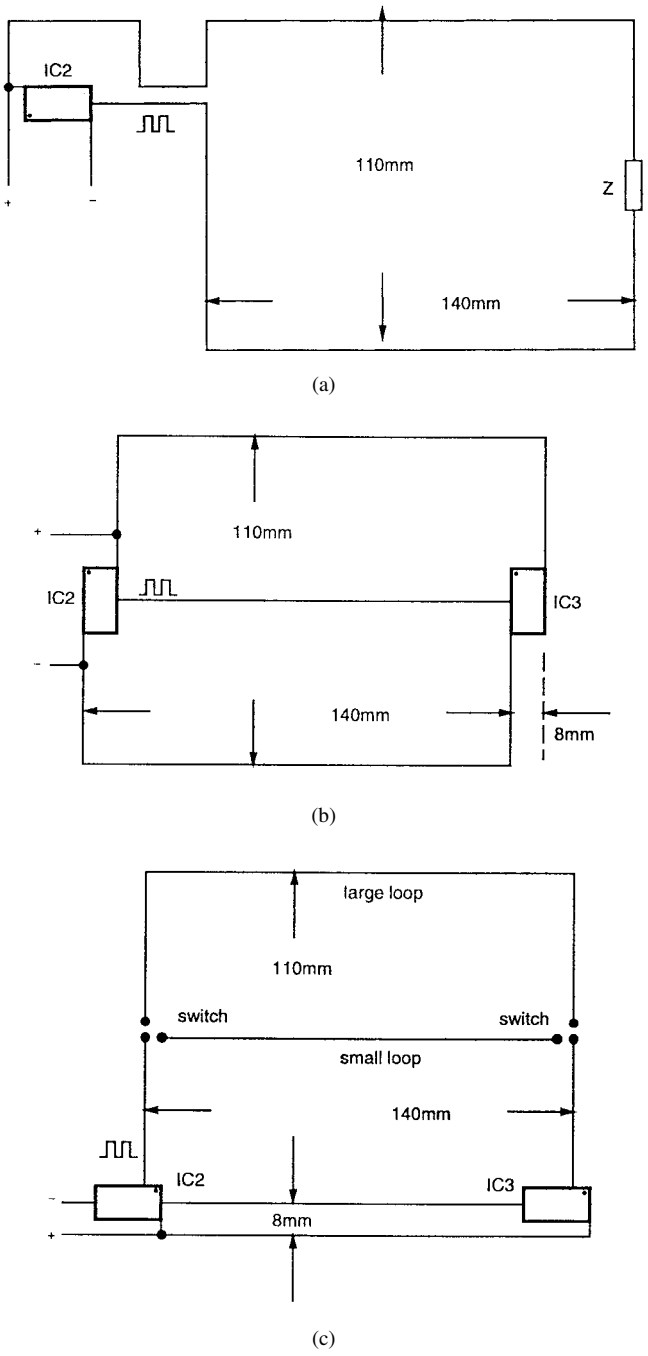


Fig. 2. Layouts of circuits for emissions testing. (a) Single loop. (b) Power tracks widely separated. (c) Power tracks close together.

route the signal around a "small" or a "large" loop. The size of each PCB was 150 × 250 mm. A second version of each PCB was made with a ground plane, which was soldered to the "ground" pins of the IC's.

Emissions measurements were also performed on a more complex, multifunction circuit, which has been developed at the University of York for demonstrating principles of EMC and radio-frequency interference [7], [5]. In this circuit, several analog and digital functions are mixed on the same board. An audio signal is converted from analog to digital form and fed to a 74 166 parallel-in serial-out shift register. This produces a serial data stream which in turn is fed to a 74 164 serial-in parallel-out shift register and then converted back to an audio signal. The digital functions are controlled by a 625-kHz clock signal.

This is obtained from a 10-MHz oscillator based on a crystal and two 7404 logic gates, the frequency of which is divided twice by 74 161 counters. The tracks of the clock circuitry form several loops whose areas are of the order of 10^{-3} m^2. There are several other logic IC's on the PCB, which is 210 $\times$ 100 mm in size.

With a minor modification, the clock circuitry was able to operate with all seven logic families except 4000B CMOS. Most of the logic IC's, including the 7404 and 74 161 of the clock circuitry, were available in all the logic families. Where IC's were unavailable, 74LS was substituted when testing TTL families and 74HCT when testing CMOS families.

III. Measurements

A. Radiated Emissions

Radiated emissions from the circuits were measured in the far field on a standard open-field test site. A horizontally polarized "Bilog" antenna [8] was mounted at 3 m from the PCB with both antenna and PCB at a height of 1 m. Measurements were made with a spectrum analyzer and were corrected for antenna factor.

Initial measurements with 74F logic were used to determine which orientation of the PCB gave greatest peak emissions. For each layout this was found to be with the PCB horizontal and with the longer side of the loop perpendicular to the direction of propagation. Measurements on one of the PCB's [Fig. 2(b)] showed that this orientation also gave the maximum emissions for each of the other logic families. Subsequent measurements were made with the PCB's fixed in this orientation.

Far-field measurements of peak radiated emissions were made for all the PCB's [including both configurations for Fig. 2(c)] both with and without ground planes. Further measurements on Fig. 2(b) (no ground plane) were made with IC3 removed and replaced in turn by a 270-Ω resistor, a 1-kΩ resistor, and finally left open-circuit.

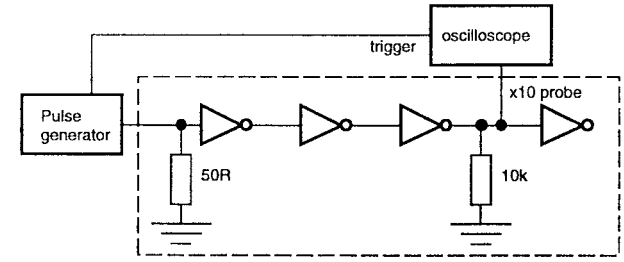
Emissions from the PCB's without ground planes were also measured in the near field at a point 200 mm from the center of the PCB and in the plane of the PCB. A 70-mm-long dipole sensor was used to measure the electric field and a 40-mm-diameter loop sensor to measure the magnetic field. The sensors were connected to a spectrum analyzer.

B. Switching Parameters

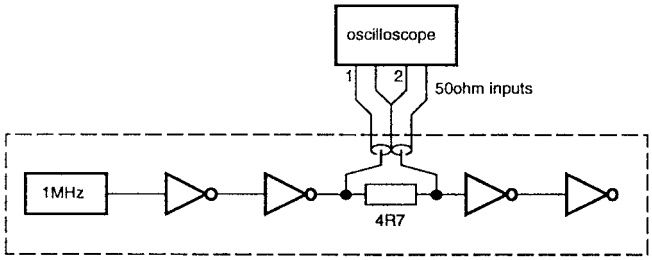
Fig. 3 shows test circuits that were used for the measurement of the switching parameters of the logic families. Each parameter was measured for the two IC's from each family previously used in the emission measurements.

The test circuit shown in Fig. 3(a) was used to measure rise and fall times, amplitude, and maximum switching frequency. A fast-pulse generator and a 500-MHz sampling oscilloscope were used to give the necessary bandwidth for the measurements. The amplitude and rise and fall times (10–90% values) were calculated automatically by the oscilloscope and were obtained at frequencies of 1 and 2 MHz. The maximum switching frequency was obtained by increasing the input frequency until the output waveform failed to cross both 0.8 and 2.0 V (the specified limits for the TTL threshold).

The test circuit shown in Fig. 3(b) was used to measure the transient switching currents between logic gates. A small resistor (4.7 Ω) was inserted between two gates and the voltage across it measured with 50-Ω coaxial cables connected to the sampling oscilloscope with 50-Ω inputs. Two cables were used to provide a balanced load at radio frequencies. The load between the gates appears as a resistance of 4.7 Ω in parallel with 100 Ω and the switching current is, therefore, given by half the measured voltage divided by this resistance. The waveform of the switching current was found to show a transient peak as



(a)



(b)

Fig. 3. Circuits for measurement of switching parameters. (a) Rise and fall times and maximum clock frequency. (b) Transient switching current.

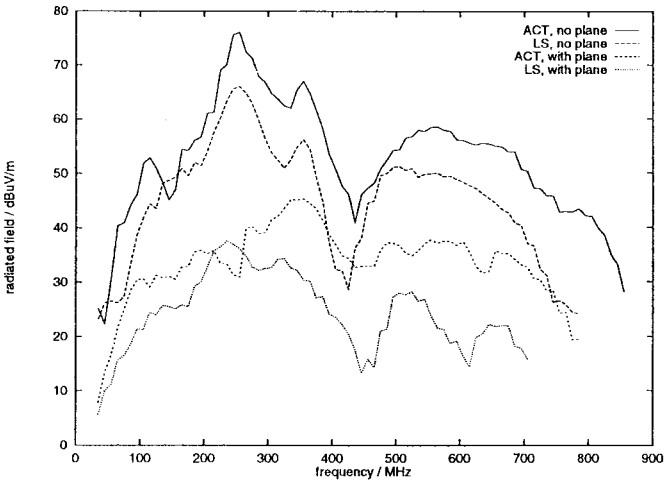


Fig. 4. Radiated spectrum from two logic families in Fig. 2(c) with and without ground plane.

the gates switched from low to high or vice versa. The peak transient current was at least ten times higher than the dc output current.

IV. Results

A. Radiated Emissions

The radiated field was found to depend on both logic family and circuit layout. Fig. 4 shows the full radiated spectrum for a "fast" and a "slow" logic family (74ACT and 74LS). The circuit layout was that shown in Fig. 2(c) with the smaller loop switched in. Results are shown for the PCB's with and without a ground plane. To make the general trend more apparent, the data have been smoothed by performing a two-point moving average on the values of radiated power at successive harmonics.

We can see from Fig. 4 that although introducing a ground plane reduces the emissions by over 30 dB, the difference in peak emissions

TABLE II
PEAK EMISSIONS IN DECIBELS RELATIVE TO 74ACT

Family	no. of comparisons		simple circuits		multi-function circuit
	far field	near field	$\overline{\Delta E_{dB}}$	$\sigma(\Delta E_{dB})$	$\overline{\Delta E_{dB}}$
74LS	12	8	-9.8	2.2	-13.2
74ALS	12	8	-7.2	2.9	-11.2
74F	12	8	-3.7	2.9	+0.9
4000B	8	8	-19.8	3.4	-
74HC	12	8	-6.2	2.9	-11.3
74HCT	12	8	-5.9	2.0	-8.3

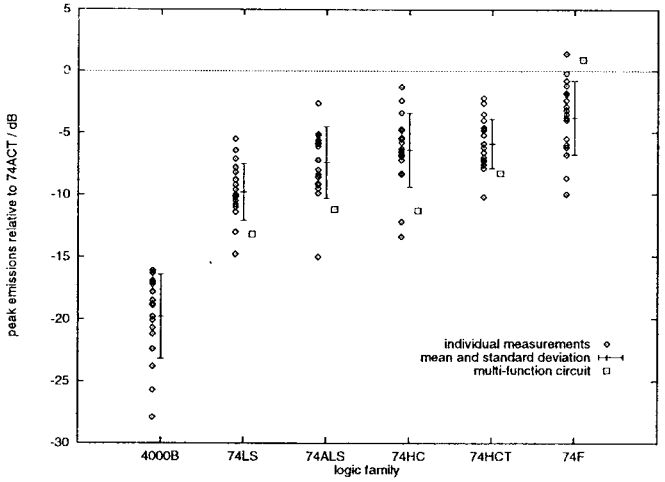


Fig. 5. Peak radiated emissions from logic families relative to 74ACT.

between ACT and LS is similar for the two layouts (approximately 10 dB for the circuit without the ground plane, approximately 8 dB for that with a ground plane). In general, the difference in peak emissions between any two families showed no obvious correlation with circuit layout or with the presence or otherwise of a ground plane.

To consider the effect of logic family independently of circuit layout, the difference in peak emissions in decibels ΔE_{dB} was calculated relative to one particular family. As 74ACT gave the highest peak emission in all but one set of measurements; this was used as the reference.

Table II shows the mean and standard deviation of ΔE_{dB} for each family. For most of the families, twenty comparisons were made. However, in the four far-field measurements on the circuits with ground planes, comparisons could not be made with the slowest family (4000B) because all the harmonics were below the noise floor.

Fig. 5 shows the individual measurements and the mean values of ΔE_{dB} for each family. This figure illustrates how the radiation from a circuit can be reduced by not using the "fastest possible" logic family in a design. It can also be seen that although there is considerable spread in the values of ΔE_{dB}, most of the points lie within ± 3 dB of the mean.

The effects of the ground plane and load impedance on radiated emissions were also considered. Table III shows the mean and standard deviation of ΔE_{dB}^{GP}, defined as the change in peak emissions due to the presence of a ground plane. Six comparisons were made for each layout corresponding to each of the logic families except 4000B CMOS. As mentioned above, the emissions from circuits with a ground plane and the slowest logic were too low to be measurable.

TABLE III
CHANGE IN PEAK EMISSIONS DUE TO GROUND PLANE

Layout	$\overline{\Delta E_{dB}^{GP}}$ (dB)	$\sigma(\Delta E_{dB}^{GP})$ (dB)
A	-22.2	2.4
B	-25.2	4.9
C (small)	-34.1	2.3
C (large)	-33.2	2.2

TABLE IV
DIFFERENCE IN PEAK EMISSIONS IN DECIBELS DUE TO REPLACING IC3 WITH A LOAD

Layout	$\overline{\Delta E_{dB}^{L}}$ (dB)	$\sigma(\Delta E_{dB}^{L})$ (dB)
270 Ω	-1.5	1.8
1 kΩ	+3.5	1.6
open circuit	+5.2	1.6

TABLE V
MEASURED SWITCHING PARAMETERS

Family	f_{max} (MHz)	A (V)	τ_r (ns)	τ_f (ns)	τ_{mean} (ns)	I_{tr} (mA)
74LS	60	3.4	12.1	2.7	7.4	60
74ALS	66	3.5	13.8	1.8	7.8	68
74F	171	3.5	1.8	1.0	1.4	103
4000B	8.5	4.8	48	33	40	15
74HC	66	5.0	1.7	2.1	1.9	98
74HCT	80	5.0	1.9	1.6	1.7	104
74ACT	198	5.0	1.0	1.2	1.1	132

Table IV shows the mean and standard deviation of ΔE_{dB}^{L}, defined as the change in peak emissions when IC3 was replaced with a passive load. Seven comparisons were made for each load, corresponding to each of the logic families. Note that these results apply only to the layout in Fig. 2(b) without a ground plane.

The radiated spectrum from the multifunction circuit was found to be dominated by the harmonics of the 10-MHz clock signal. The last column of Table II shows values of ΔE_{dB} for this circuit, which are the mean of far-field values measured on the test site and near-field values measured with the loop sensor. The values of ΔE_{dB} lie within the spread of measurements made on the loop circuits, but just outside one standard deviation from the mean.

B. Switching Parameters

Table V shows the measured maximum switching frequency $f_{\max}$, amplitude A, rise and fall times τ_r, and τ_f, the mean of rise and fall times τ_{mean}, and the peak to peak transient switching current $I_{\rm tr}$. Note the difference in amplitude between the TTL and CMOS families.

Values of $\Delta E_{\rm dB}$ were calculated from (3) and (4) by comparing values of $|c_n|$

$$\Delta E_{\rm dB} = 20\log_{10}|c_n(\text{family})| - 20\log_{10}|c_n(74\text{ACT})|. \quad (5)$$

Values of A, τ_r, and τ_f were taken from Table V. A value of $n = 21$ was used, corresponding to 210 MHz as the peak emissions

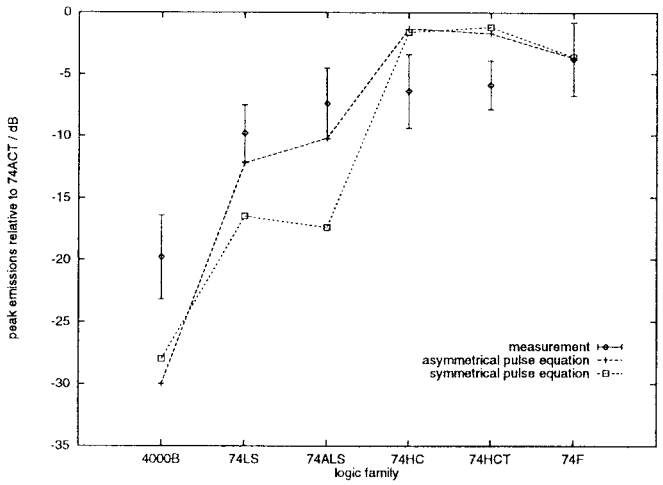


Fig. 6. Values of ΔE_{dB} calculated from (5).

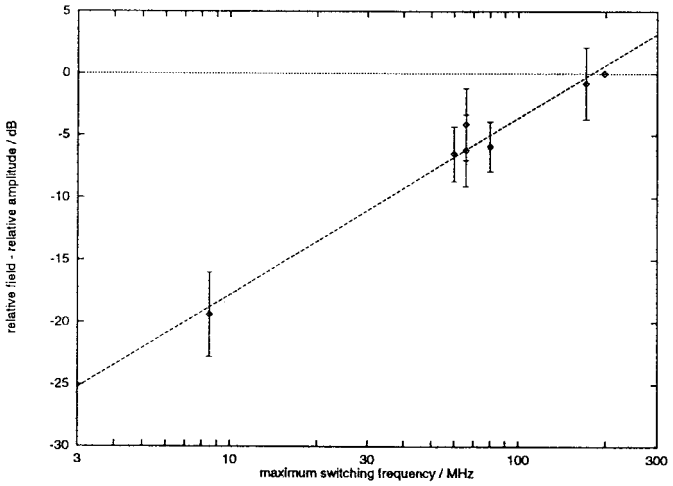


Fig. 7. Variation of $\Delta E_{\mathrm{dB}} - \Delta A_{\mathrm{dB}}$ with $f_{\max}$.

were usually in the range 190–240 MHz. However, for 4000B CMOS, a value of $n = 22$ was used in (3), as this was the only case in which the calculated value of c_{22} was greater than c_{21}. Values obtained from the two equations are compared to measurement in Fig. 6. It can be seen that for some of the logic families, calculated and measured values differ by more than 10 dB.

An alternative to using three and four is to develop empirical relationships between peak emissions and the switching parameters. To do this, we first note that if all other factors are equal the radiated field should be proportional to the amplitude of the signal. To remove this dependence we therefore consider the quantity $\Delta E_{\mathrm{dB}} - \Delta A_{\mathrm{dB}}$ where ΔA_{dB} is the difference in decibels between the values of A for a particular logic family and for 74ACT. Figs. 7–9 show $\Delta E_{\mathrm{dB}} - \Delta A_{\mathrm{dB}}$ plotted against $f_{\max}$, τ_{mean}, and I_{tr}, respectively, while Fig. 10 shows $\Delta E_{\mathrm{dB}} - \Delta A_{\mathrm{dB}}$ plotted against the literature values of propagation delay τ_{pd} shown in Table I. It can be seen that peak emissions tend to increase with $f_{\max}$ and I_{tr} and fall with τ_{mean} and τ_{pd}.

An equation of the form

$$\Delta E_{\mathrm{dB}} - \Delta A_{\mathrm{dB}} = m \log_{10} x + c \tag{6}$$

has been fitted by linear regression analysis to each of the switching

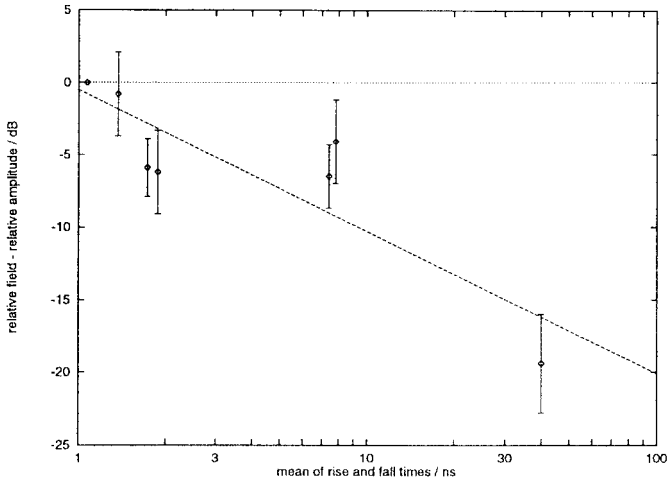


Fig. 8. Variation of $\Delta E_{\mathrm{dB}} - \Delta A_{\mathrm{dB}}$ with τ_{mean}.

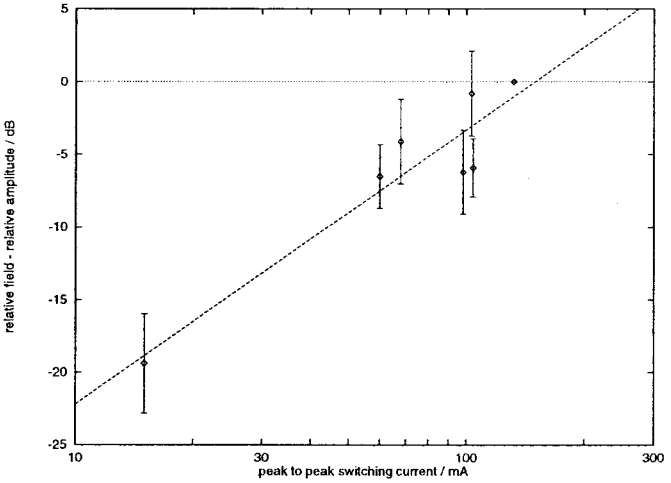


Fig. 9. Variation of $\Delta E_{\mathrm{dB}} - \Delta A_{\mathrm{dB}}$ with I_{tr}.

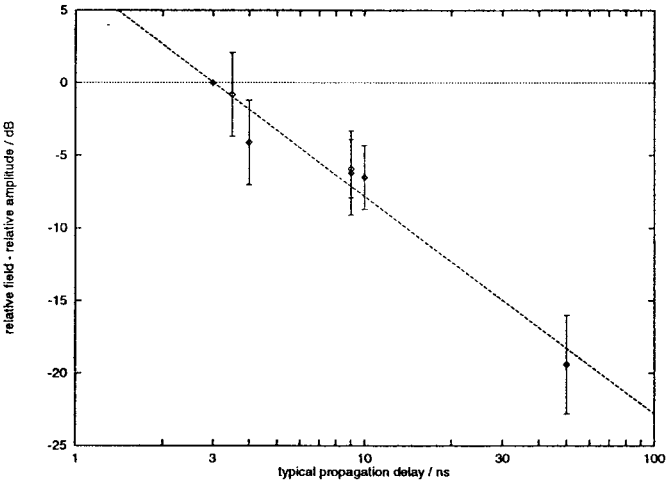


Fig. 10. Variation of $\Delta E_{\mathrm{dB}} - \Delta A_{\mathrm{dB}}$ with τ_{pd}.

parameters x considered above. Table VI shows the calculated values of m and c and the regression coefficient r for each of the parameters.

TABLE VI
CALCULATED VALUES OF CONSTANTS IN (6) AND REGRESSION COEFFICIENTS

Parameter	c (dB)	m	r
f_{max} (MHz)	-32.0	14.2	0.987
τ_{mean} (ns)	-0.5	-9.8	-0.861
I_{tr} (mA)	-41.1	18.9	0.939
τ_{pd} (ns)	7.2	-15.0	-0.979

The highest values of $|r|$, corresponding to the best fit to the data, are for maximum switching frequency and for propagation delay. Equation (6) implies that on a linear scale, the peak radiated emission is given by

$$E = kAf_{\max}^{0.71} \tag{7}$$

or by

$$E = k'A\tau_{pd}^{0.75} \tag{8}$$

where k and k' are constants dependent on the layout of the circuit. Similar equations may be derived for τ_{mean} and I_{tr} with exponents of -0.49 and 0.95, respectively.

V. DISCUSSION

The results provide quantitative evidence that digital circuits designed with faster logic do give higher radiated emissions. Furthermore, the difference in peak emissions between one logic family and another appears to be independent of layout or grounding scheme. Of the families tested, the highest peak emissions were from 74ACT and the lowest from 4000 CMOS. Of the TTL families, 74F was highest, 74LS lowest.

There was some spread in the values of relative peak emission ΔE_{dB}. This may be partly due to the relative strength of the odd and even harmonics in the spectrum of the signal. In (4), for the coefficients of the harmonics there is a factor $\sin \pi n\tau/T$. If the duty cycle of the signal is exactly 50%, then $\tau/T = 1/2$ and $\sin \pi n\tau/T = 0$ for all even n. However, if the duty cycle is only slightly different from 50%, then the nulls of this factor no longer coincide with the even harmonics. There are then regions of the spectrum where the nulls fall very close to alternate harmonics and other regions where they fall mid way between harmonics. This is observed in practice. Calculations show that over a small region of the spectrum, the peak values in the former case are approximately 3 dB higher than in the latter case. Similar behavior results when the rise and fall times are different, which was so for all the logic families tested (see Table V). This would account for a variation of 3 dB in the peak emissions due to one logic family and, hence, a 6-dB variation in the difference between two families. In fact, most of the measured values of ΔE_{dB} lie within ± 3 dB of the mean.

A second reason for the spread of values of ΔE_{dB} may be a change in the frequency of the peak harmonic, which was observed to vary by up to 50 MHz in one set of measurements. If this were partly due to a changing circuit resonance, then the peak emission would vary depending on whether the maximum of the resonance lay on or between the 10-MHz harmonics of the signal. Inspection of the spectra suggests that this could account for a further 1-dB variation in ΔE_{dB}. However, this value would be likely to increase if a higher clock frequency were used as the harmonics would be further apart in frequency.

The measurements on the multifunction circuit show that the values obtained from the simple loop circuits are relevant to a circuit that performs more realistic functions. The differences between the two types of circuit may be due to the effects discussed above, or it may be because the multifunction circuit contains several radiating loops. Since the logic families have different propagation delays, this could cause a difference in phase between the loops that further reduces the radiation from the slower families. Further work is needed to investigate this.

The results have shown that (3) and (4) give poor prediction of ΔE_{dB} for some of the families. A problem with using these equations is that the peak emissions occur at different frequencies for the different logic families, making it difficult to use the equations for comparisons. Other reasons for the discrepancy may be that the values of rise and fall time vary with circuit layout or that a trapezoid is not a good approximation to the waveform.

By contrast, the empirically derived formulas provide useful relationships between parameters that are used in circuit design. Designers may often wish to maximize the operating frequency of a circuit while minimizing the radiated emissions and (7) and (8) will aid them in making decisions. Apart from the dependence on the switching amplitude, the formulas are empirical. Further measurements would be needed to test whether they applied to other or future types of logic device. However, they have the advantage of being simple to use without requiring detailed knowledge of the circuit or its layout.

It is interesting to compare the effect of logic family with the effect of a ground plane. The mean difference in peak emissions between the fastest and slowest families was approximately 20 dB, while the range for families able to operate above 10 MHz was only approximately 10 dB. By contrast, the difference in peak emissions for versions of a PCB with and without a ground plane ranged from 22 to 34 dB, depending on the layout.

The measurements described in this paper were made on standalone PCB's. In most electronic equipment the interactions of the PCB's with cables and enclosures must also be considered, and further work is needed to investigate these.

In conclusion, we have investigated the radiated emissions from a variety of circuits and shown that the relative value of peak emissions between two logic families is independent of layout or grounding scheme. For the first time, both the spread and the mean values of relative peak emissions have been quantified. It has also been shown how these values relate to important switching parameters such as the propagation delay and the maximum switching frequency. It is hoped that this work will be a useful step toward quantifying EMC design problems.

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