

# Impact of stress in ICP-CVD SiN<sub>x</sub> passivation films on the leakage current in AlGaIn/GaN HEMTs

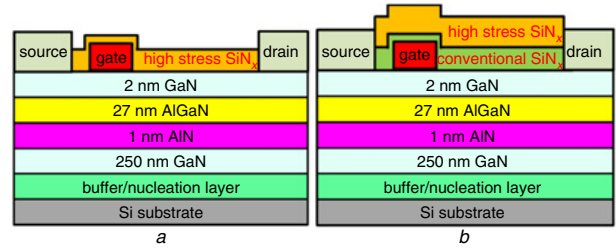
S.-J. Cho<sup>✉</sup>, X. Li, I. Guiney, K. Floros, D. Hemakumara, D.J. Wallis, C. Humphreys and I.G. Thayne

The impact of the stress in room temperature inductively coupled plasma chemical vapour deposited (ICP-CVD) SiN<sub>x</sub> surface passivation layers on off-state drain ( $I_{DS-off}$ ) and gate leakage currents ( $I_{GS}$ ) in AlGaIn/GaN high electron mobility transistors (HEMTs) is reported.  $I_{DS-off}$  and  $I_{GS}$  in 2  $\mu\text{m}$  gate length devices were reduced by up to four orders of magnitude to  $\sim 10$  pA/mm using a compressively stressed bilayer SiN<sub>x</sub> passivation scheme. In addition,  $I_{on}/I_{off}$  of  $\sim 10^{11}$  and sub-threshold slope of 68 mV/dec were obtained using this strain engineered surface passivation approach.

**Introduction:** AlGaIn/GaN HEMTs are a promising candidate for power and RF electronics due to the high breakdown voltage, high electron saturation velocity and good thermal stability of the GaN-based material system [1, 2]. Off-state drain to source ( $I_{DS-off}$ ) and gate leakage ( $I_{GS}$ ) currents must be minimised in these devices to improve the efficiency of their power switching. To reduce leakage currents, Al<sub>2</sub>O<sub>3</sub> passivation deposited by atomic layer deposition, wet chemical or plasma surface treatment before passivation and annealing after gate metal deposition have been reported [3–6]. SiN<sub>x</sub> has been widely used for surface passivation between the transistor gate and drain and shown to be effective in reducing current collapse and DC-to-RF dispersion arising from the large density of surface states and trapped surface charge [7]. Optimisation of the properties of the SiN<sub>x</sub> passivation film has been reported, including the impact of stress in the SiN<sub>x</sub> film on the properties of an AlGaIn/GaN HEMT by Gregušová *et al.* [8]. Fehlberg *et al.* [9] used Hall Bars to investigate the impact of stress in SiN<sub>x</sub> deposited films on the electrical transport properties of AlGaIn/GaN heterostructures. To date, all reports on the impact of stressed SiN<sub>x</sub> films have been restricted to passivation layers deposited by plasma enhanced chemical vapour deposition (PE-CVD) techniques with a maximum compressive stress of 150 MPa. Moreover, the use of SiN<sub>x</sub> by PE-CVD as a surface passivant can result in increased  $I_{DS-off}$  and  $I_{GS}$  [10]. To mitigate these effects, in this Letter, we compare the impact of both tensile and compressive stress in the range of  $-1622$  to  $+440$  MPa in room temperature deposited ICP-CVD SiN<sub>x</sub> surface passivation films on AlGaIn/GaN HEMTs. A significant reduction in  $I_{DS-off}$  and  $I_{GS}$  was observed for the optimally stressed films.

**Fabrication process:** The AlGaIn/GaN heterostructure epi-layers of this study were grown on a silicon substrate by metal organic chemical vapour deposition. From the substrate, the layer structure comprised a 0.25  $\mu\text{m}$  AlN nucleation layer; a  $10^{18}$  cm<sup>-3</sup> carbon doped buffer layer comprising a graded 1.8  $\mu\text{m}$  AlGaIn layer, followed by a 0.8  $\mu\text{m}$  GaN layer; a 0.25  $\mu\text{m}$  undoped GaN channel; a 1 nm mobility enhancing AlN interlayer; a 27 nm Al<sub>0.27</sub>Ga<sub>0.73</sub>N barrier and a 2 nm GaN cap layer. Transistors were fabricated by first performing an electron beam evaporation of 30/180/40/100 nm Ti/Al/Ni/Au source and drain ohmic contacts which were annealed at 770°C for 30 s in N<sub>2</sub>, followed by a 600 nm mesa isolation etch in a SiCl<sub>4</sub>-based plasma chemistry. Then, 2  $\mu\text{m}$  length, 20/200 nm thick Ni/Au Schottky gate contacts were defined by photolithography between the source and drain contacts. At this point, the ‘unpassivated’ transistor characteristics were measured on all samples.

The stress of an ICP-CVD SiN<sub>x</sub> passivation film can be adjusted by changing the ICP and RF platen powers [11]. Initially, without any surface pre-treatments, single layers of SiN<sub>x</sub> of various stresses were deposited on device samples described above as shown schematically in Fig. 1a. The stress in the films of Table 1 was determined when deposited on silicon substrates. With the exception of films (I) and (V) in Table 1, referred to elsewhere as ‘conventional SiN<sub>x</sub>’, all the other films (II to IV of Table 1) cracked or delaminated; an example is shown in Fig. 2a. It was discovered that this situation could be overcome by first depositing 70 nm SiN<sub>x</sub> films using process (I) in Table 1 followed by the higher stress films [(II) to (V) of Table 1]. ‘A typical bilayer’ films are shown in Figs. 1b and 2b.



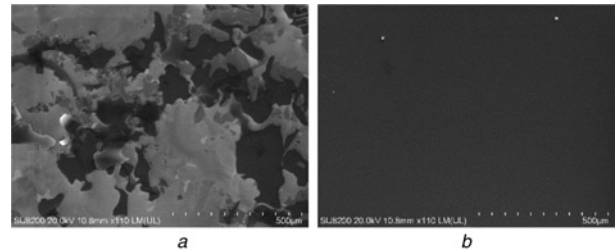
**Fig. 1** Cross-section of surface passivation

a ‘High’ stressed single layer surface passivation

b ‘High/conventional’ stressed bilayer surface passivation

**Table 1:** Stress conditions and type of SiN<sub>x</sub>

Ref.	ICP power, W	Platen power, W	Chamber pressure, mT	Stress, MPa	Refractive index
(I)	200	0	5	-280 (compressive)	2.01
(II)	200	4	5	-616 (compressive)	1.99
(III)	300	4	5	-1163 (compressive)	1.93
(IV)	300	8	5	-1622 (compressive)	1.89
(V)	300	0	7	+440 (tensile)	1.72

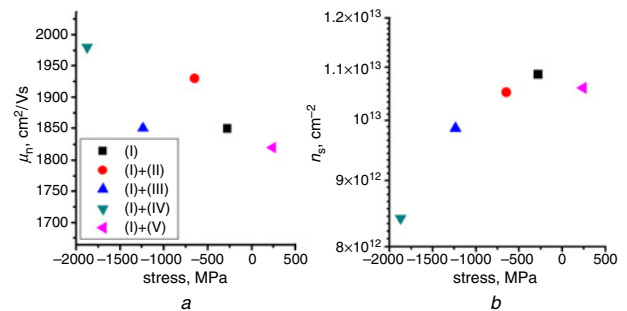


**Fig. 2** SEM image of surface passivation

a ‘High’ stressed single layer surface passivation

b ‘High/conventional’ stressed bilayer surface passivation

**Measurement results and discussion:** Fig. 3 shows room temperature electron mobility ( $\mu_n$ ) and carrier concentration ( $n_s$ ) as a function of various stress of SiN<sub>x</sub> bilayer as determined by Van der Pauw test structure measurement. Electron mobility is increased and carrier concentration is decreased as a consequence of highly compressive stress of SiN<sub>x</sub>. This suggests either highly compressive stress of SiN<sub>x</sub> passivation schemes have reduction of net positive charge effect at the GaN surface and/or the presence of fixed positive charge in the SiN<sub>x</sub> films [12].



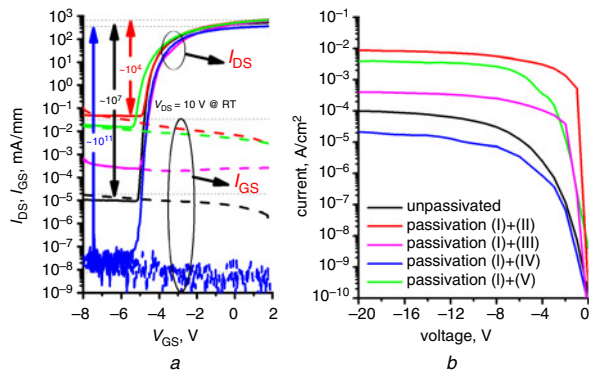
**Fig. 3** Room temperature Van der Pauw evaluation

a Stress–electron mobility by various passivation schemes

b Stress–carrier concentration by various passivation schemes

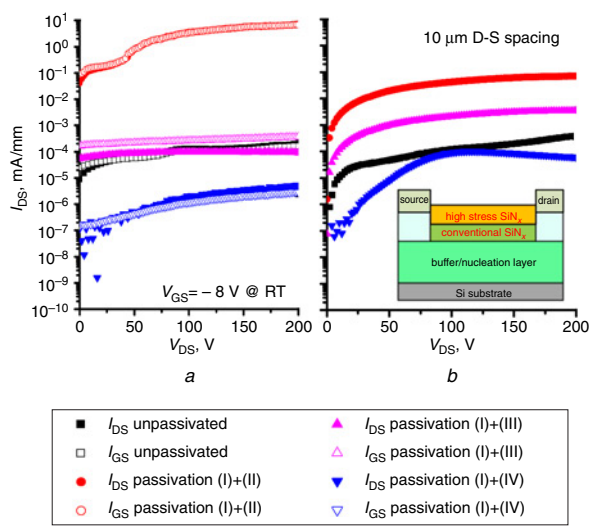
Fig. 4a shows semi-log scale  $I_{DS-off}$ – $V_{GS}$  and  $I_{GS}$ – $V_{GS}$  characteristics for the single and bilayer passivation schemes and are compared with unpassivated devices. The incorporation of passivations (I) + (II) and (I) + (V) result in three orders of magnitude increase in  $I_{DS-off}$  and  $I_{GS}$ , when compared to unpassivated devices which have leakage currents of order 10 nA/mm. In contrast, devices with passivation (I) + (IV) have around four orders of magnitude reduction in  $I_{DS-off}$  and  $I_{GS}$ , when compared to unpassivated devices. Devices with passivation (I) + (IV) demonstrated  $I_{on}/I_{off}$  ratio of  $\sim 10^{11}$  and subthreshold slope of 68 mV/dec. Fig. 4b shows reverse Schottky gate leakage comparison

of unpassivated and various stressed  $\text{SiN}_x$  surface passivation schemes. The rank of Schottky reverse bias leakage is same as  $I_{\text{GS}}$  leakage of Fig. 4a. Figs. 5a and b, respectively, show the  $I_{\text{DS}}-V_{\text{DS}}$  three terminal off-state leakage current and  $I_{\text{GS}}-V_{\text{DS}}$  lateral isolated leakage current ( $I_{\text{buffer}}$ ) characteristics for the various passivation schemes. These clearly show the bilayer passivation (I)+(IV) is optimal in reducing these contributors to device leakage current.



**Fig. 4** Semi-log scale off-state and gate leakage comparison of unpassivated and various stressed  $\text{SiN}_x$  surface passivation schemes

a  $I_{\text{DS}}-V_{\text{GS}}$  and  $I_{\text{GS}}-V_{\text{GS}}$  comparison ( $W_{\text{G}} = 100 \mu\text{m}$ ,  $L_{\text{GS}} = 2 \mu\text{m}$ ,  $L_{\text{G}} = 2 \mu\text{m}$ ,  $L_{\text{GD}} = 7 \mu\text{m}$ )  
 b Reverse Schottky gate leakage comparison



**Fig. 5** Semi-log scale off-state and lateral isolated leakage comparison of unpassivated and various stressed  $\text{SiN}_x$  surface passivation schemes

a  $I_{\text{DS}}-V_{\text{DS}}$  and  $I_{\text{GS}}-V_{\text{DS}}$  off-state leakage current characteristics ( $W_{\text{G}} = 100 \mu\text{m}$ ,  $L_{\text{GS}} = 2 \mu\text{m}$ ,  $L_{\text{G}} = 2 \mu\text{m}$ ,  $L_{\text{GD}} = 7 \mu\text{m}$ )  
 b Lateral isolated leakage current characteristics

**Conclusion:** In this Letter, the impact of stress in ICP-CVD  $\text{SiN}_x$  surface passivation layers deposited at room temperature on  $I_{\text{DS-off}}$  and  $I_{\text{GS}}$  in AlGaIn/GaN HEMTs is assessed. The use of a bilayer  $\text{SiN}_x$  passivation scheme comprising 70 nm 280 MPa compressively strained film followed by a 150 nm 1.6 GPa compressively strained layer resulted in  $I_{\text{DS-off}}$  and  $I_{\text{GS}}$  reduction by up to four orders of magnitude when compared to unpassivated devices and up to seven orders of magnitude in comparison with devices with a single 70 nm 280 MPa compressively strained passivation layer.  $I_{\text{DS-off}}$  and  $I_{\text{GS}}$  of  $\sim 10 \text{ pA/mm}$ ,  $I_{\text{on}}/I_{\text{off}}$  of  $\sim 10^{11}$  and subthreshold slope of 68 mV/dec are obtained using the optimal process.

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One or more of the Figures in this Letter are available in colour online.

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