A Charge Correction Cell for *FGMOS*-based Circuits

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Abstract

This paper describes a novel cell used in circuits with Floating Gate *MOS* transistors (*FGMOS*) to compensate variations in the device effective threshold voltages caused by the trapped charge at the floating gate. The performance of the circuit is illustrated with experimental results showing a residual error below *1%*. This coarse compensation makes possible to reduce charge effects to the same order of magnitude than the conventional mismatching in normal *MOS* transistors.

Key words: FGMOS analog circuits, Floating gate charge correction.

1. Introduction

Important drivers for microelectronics in the last years has been low power and low voltage portable systems market. The interest of *IC* designers has focused in the development of digital and analog techniques intended to minimize both power and voltage supply. Among the analog methods, the use of the Floating Gate *MOS* transistor has emerged as one of the most promising and challenging as well [1]. Working with *FGMOS* forces designers to tackle with several problems related to the existence of the floating node. One of its main shortcomings in the low voltage and low power context has to do with the charge that can stay trapped at the floating gate during the fabrication process. This paper proposes a four-transistor cell which compares the threshold voltage of a normal *MOS* device with the one of an identical sized *FGMOS* and provides an output depending on the value of the trapped charge. Connecting it to the *FGMOS* transistors in the circuit, the change of their threshold voltages caused by that term can be compensated. Section 2 will describe the most common used techniques for trapped charge erasing/processing in FGMOS circuits. In Section 3, our proposed circuit is introduced and a practical realization is reported whose experimental behaviour is explained in Section 4.

2. Charge Induced Correction Techniques

One of the drawbacks for the use of *FGMOS* transistor has is that the quantity of charge trapped at its gate during the fabrication process is unknown. This charge could be either an advantage or a disadvantage depending on the application the transistor is going to be used. The solutions designers have adopted for dealing with this problem could be classified in: solutions oriented to control that charge, as the functionality of the circuit is based on its exact value, and solutions trying to erase it, since its presence could spoil the block performance. The most relevant techniques are: 1) The use of the tunnel effect and the hot electron injection [2], [6]. 2) The application of UltraViolet Light (UV) for charge cleaning [3], [4]. 3) Fixing an initial electrical condition at the floating gate [5].

The first technique controls the charge either positive or negative. The use of both processes (tunnelling and hot electron injection) allows increment or decrement of charge. They could also be combined with the aim of erasing, but that would bring several added drawbacks as

for example the need of additional circuitry as well as the use of high voltages. Besides, they are not modelled in all the technologies. Hence, the first step would be to model them, and this is not a simple task. Only a few designers have done it for certain technologies [1].

The cleaning with ultraviolet light is based on the fact that when the surface of any semiconductor is lightened with light or any other electromagnetic radiation, part of it is reflected, part of it is absorbed, and the rest is transmitted. The number of absorbed photons is proportional to the total number of them, and therefore to the light intensity. It also depends on the kind of semiconductor, wave length of the photons and the applied electric field. When the floating gate is lightened with *UV* light, the electrons trapped at the gate can travel through the potential barrier in the interface Oxide/Silicon. The main drawback this technique has is that it depends on the kind of passivation making more or less easy to eliminate the charge. However, this is the simplest method as no extra circuitry is required.

The third technique is very useful in certain examples but it is not as general as the *UV* cleaning. It consists of short-circuiting the floating gate to a certain value ($V_{FG}(0)$) that would set the wished operating point for a certain combination of inputs. It would evolve to a high impedance state afterwards [5].

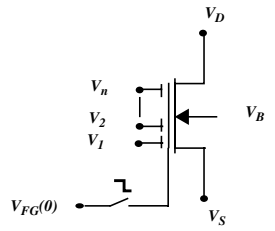

Fig. 1. Technique to set the initial conditions at the floating gate.

This technique has a lot of detractors among some *FGMOS* designers who think the gate is not floating any more. Having a switch accessing to it has the drawback that, even when this is in a high impedance state, there is a leakage current flowing through the switch that will discharge the floating gate after some time. It would be needed to refresh the gate with a certain frequency, in the order of *kHz*. This would not have to be a problem in digital cells that carry out a lot of operations in that time. In analog circuits it is not easy to use, though, as an adequate reset configuration has to be found which makes the circuit evolves fast enough afterwards.

3. The Circuit for Charge Error Sensing and Correction

A Floating Gate *MOS* transistor (*FGMOS*) is a *MOS* transistor whose polysilicon gate, completely wrapped in silicon dioxide, has no DC path to a fixed potential. It can modulate the channel between a source and drain and therefore it can be used in computation. The coupling capacitors to the floating gate becomes effective gates of the device, depending the gate strength upon the capacitor size [7]. This is mathematically described by eq.(1) which represents the voltage at the floating gate in an *N*-input *FGMOS* transistor, whose input capacitances and voltages are C_i and V_i, respectively, and C_{GD}, C_{GS} and C_{GB} are the capacitive couplings to the other terminals: drain, source and bulk. C_T is the value of the total capacitance seen from the floating gate.

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GB}}{C_T} V_B + \\ + \frac{C_{GD}}{C_T} V_D + \frac{C_{GS}}{C_T} V_S + \frac{Q_{FG}}{C_T} \tag{1}$$

being,

$$C_T = \sum_{i=1}^{N} C_i + C_{GB} + C_{GD} + C_{GS} \tag{2}$$

The last term in eq.(1) takes into account the contribution to the gate voltage of the charge that can stay trapped on it during the fabrication process. If this expression is mapped to the gate voltage in the current law of a normal *MOS* transistor the new equations for the *FGMOS* arise, in which the term Q_{FG}/C_T can be associated to the nominal threshold voltage, and a new effective one can be defined. The latter differs of the same parameter for

an identical *MOS* transistor whenever this term is different from zero.

The circuit presented in this paper for charge sensing and correction is drawn in Fig. 2. The basic idea relies on the comparison between the gate voltages of two transistors, a *MOS* and a *FGMOS*, with equal aspect ratios (*M1* and *M2,* respectively). If the drain current is the same in both, the gate voltage will also be the same. After a few basic manipulations, if the transistor pairs *M1-M2* and *M3-M4* are identical and the deviations in the threshold voltages (V_{th}) and current factor (β) originated by mismatching are negligible, the V_{FG2} voltage at the floating gate of *M2* can be expressed as:

$$V_{FG2} \approx V_{in} \tag{3}$$

Substituting the left hand side in eq.(3) by its expression as function of the transistor's terminal voltages, the value of the trapped charge at the floating gate could be obtained as:

$$\frac{\Delta Q}{C_{ox}} \approx V_{in} - \frac{C_{in}}{C_T} V_{in} - \frac{(C_{out} + C_{GD})}{C_T} V_{out2} = \left(1 - \frac{C_{in}}{C_T}\right) V_{in} - \left(\frac{C_{out}}{C_T} + \frac{C_{GD}}{C_T}\right)(V_{out2o} + \Delta V_{out2}) \tag{4}$$

being C_{GD} the gate to drain capacitance of transistor *M2* and V_{out2o} represents the value of V_{out2}'s in absence of trapped charge. Hence, if $C_{GD}, C_{GS}, C_{GB} \ll C_{out}$ and $C_{out} = C_{in}$, for $\Delta Q = 0$, $V_{out2o} \approx V_{in}$. The linear relationship in eq.(4) makes possible to sense ΔQ charge by means of a straight line curve. This process is shown in Fig. 3 for the two straight line parameters: slope (*m*) and origin coordinate (*b*).

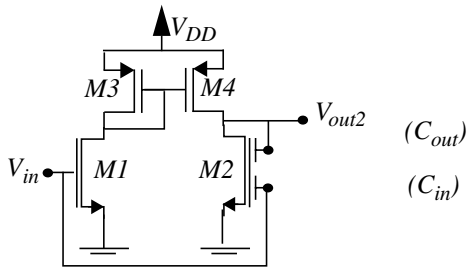

Fig. 2. Basic circuit for sensing the trapped charge.

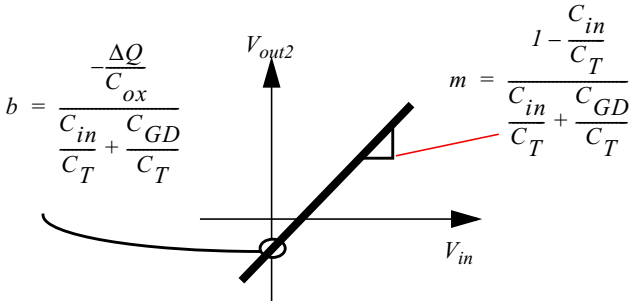

Fig. 3. Graphic representation for eq. (4) to extract ΔQ related parameter values.

For a constant voltage V_{in}, the deviation of V_{out2} from its expected nominal value is:

$$\Delta V_{out2} \approx -\frac{C_T}{C_{in}} \frac{\Delta Q}{C_{ox}} \tag{5}$$

This means that the induced charge error can be measured as a voltage increment in the output terminals. Let us consider now the circuit in Fig. 4. All the transistors have the same sizes, and the input capacitances have the same values in the two *FGMOS*. One of the inputs in the two *FGMOS* transistors (*M2* and *M5*) is connected to V_{out2}. The other three are connected to V_{in}, but they could in general have different voltages. If we Consider that the ΔQ induced error is the same in *M2* and *M5* and the voltage at the floating gate of the second *FGMOS* transistor, V_{FG5}, then:

$$V_{FG5} = \frac{3C_{in}}{C_T} V_{in} + \frac{C_{in}}{C_T} V_{out2o} + \frac{C_{in}}{C_T} \Delta V_{out2} + \frac{\Delta Q}{C_T} = V_{FG5o} + \Delta V_{FG5} = V_{G6} \tag{6}$$

which has a nominal value, V_{FG5o}, given by the first two terms of the right hand side in eq.(6), and an error term which is cancelled thanks to the connection to the output of the previous block (eq.(5)):

$$\Delta V_{FG5} \approx \frac{\Delta Q}{C_{ox}} \left(1 - \frac{C_{in}}{C_{in}}\right) = 0 \tag{7}$$

The output of this block will be the voltage V_{G6}. Its value will sense the voltage at V_{FG5}. Hence the error due to the trapped charge at a floating gate can be corrected by connecting the transistor to the output of a block like the

one in Fig. 4, in the way that has been previously presented. The transistors in this block have to be designed with the same aspect ratio as the one's whose deviations are wanted to be corrected, and the input capacitances must be much larger than the gate to drain parasitic.

4. Experimental Results

To prove this idea, a circuit prototype has been fabricated and tested. This prototype consists in two circuits: one with the configuration in Fig. 4, and another with the schematic in Fig 5. The micro photograph of the chip is shown in Fig. 6. It has been fabricated in a *0.8*μ*m*, double polysilicon *CMOS* technology. Aspect-ratios for *NMOS* transistor are (*W*/*L*)=(*4*μ*m/1*μ*m*), while input capacitors are equals to *100fF*. In the test process, for the first configuration, V_{in} is set to *1.5V*. The floating-gate voltage values are sensed throughout the gates of *M2* and M6, giving the V_{out2} and V_{G6} signals. The *M4* and M7 transistors are equals, so load effect is the same. The values obtained for the output voltages are $V_{out2} = V_{G6} = 1.03V$. These are nearly equal, so these means that ΔQ is very low for this run or technology. Circuit in Fig. 5serves us to prove eq. (5). A voltage signal, V_{error}, has been connected to one of the input gates of *M2* and *M5*. This allows to generate an equivalent error on both transistor that will reproduce the ΔQ effects. The responses for the two circuits are shown in Fig. 7. It can be noticed how V_{out2} is affected by this error while V_{FG6} is nearly constant, and equal to the value measured before. This proves the error correction mechanism. The V_{G6} voltage changes only *1%* around *1.03V* when V_{error} goes from *0.4V* to *1.5V*.

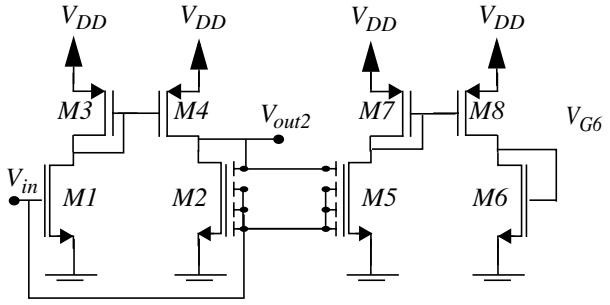

Fig. 4. Circuit for sensing and compensating the trapped charge effects.

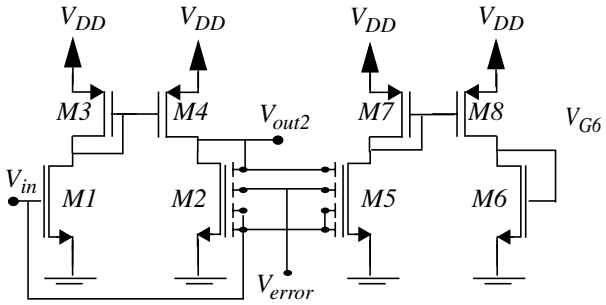

Fig. 5. ΔQ simulation error circuit by means of V_{error} signal in the proposed control test circuit.

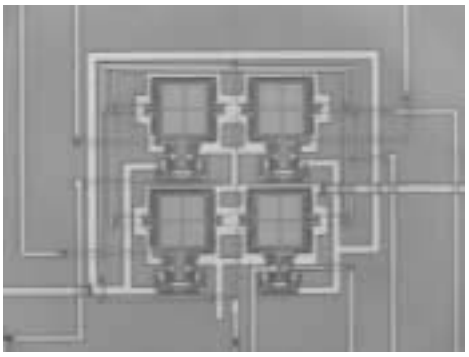

Fig. 6. Microphotograph of charge control circuit.

The proposed cell can be used to charge control in continuous time *FGMOS* based filters, as for example the reported in [8]. Figure 8 shows the *FGMOS* version of a transconductor. Charge trapped at each *M1* and *M2* transistors can be cancelled by adding an extra input and connecting it to the proposed cell in this paper. The results for this application example will be shown at the conference (or at the final version of the paper).

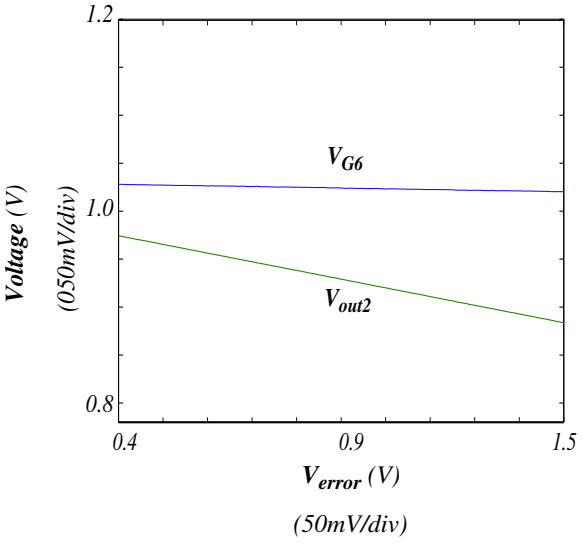

Fig. 7. Evolution of V_{out2} and V_{G6} when a voltage signal (V_{error}) is applied for simulating a ΔQ charge on *M2* and *M6* floating gates.

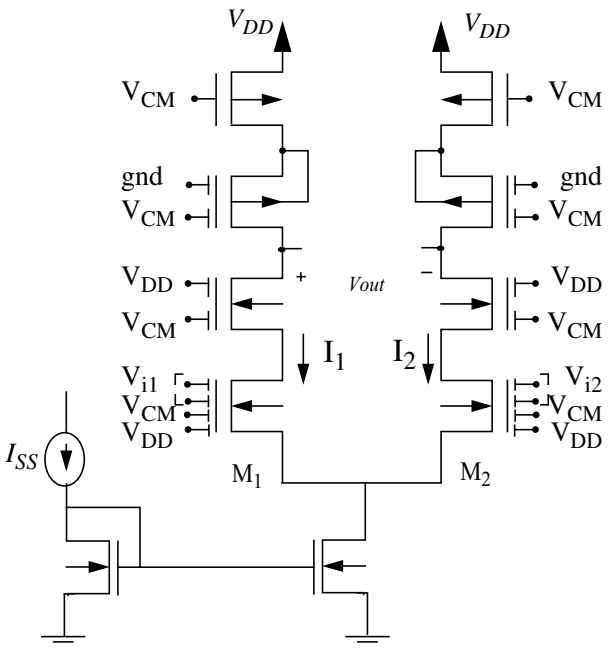

Fig. 8. *FGMOS*-based Transconductor.

5. Conclusions

A four-transistor cell, intended to coarsely correct effective threshold voltage offsets due to trapped charge during the fabrication process in the *FGMOS* transistors has been presented in this paper. Its functionality has been proven The residual error after applying the correction mechanism become smaller than *1%* the value of the initial induced error term in *FGMOS* devices with *W/L=4μm/1μm* and input capacitances in the order of *100fF*.

6. References

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