Complementary Tunnel Gate Topology to Reduce Crosstalk Effects

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***Abstract*— Tunnel transistors are one of the most attractive steep subthreshold slope devices which are being investigated to overcome power density and energy inefficiency exhibited by CMOS technology. There are design challenges associated to their distinguishing characteristic which are being addressed. In this paper the impact of the non-symmetric conduction of tunnel transistors (TFETs) on the speed of TFETs circuits under crosstalk is analyzed and a novel topology for complementary tunnel transistors gates, which mitigates the observed performance degradation without power penalties, is described and evaluated.**

***Keywords*— Tunnel transistors, Steep subthreshold slope, noise coupling, Low power, Energy efficieny, Low supply voltage.**

I. INTRODUCTION

Tunnel transistors (TFETs) are currently receiving a lot of attention as potential candidates to substitute or complement CMOS devices. They are one of the most attractive steep subthreshold slope devices [1], [2]. Steep subthreshold slope enables low voltage operation with acceptable speed leading to power and energy and thus they are being explored to overcome the power density and energy inefficiency problems exhibited by CMOS due to its 60 mV/decade minimum subthreshold slope (SS) [3]-[8] .

Subthreshold swing under 60mV/dec has been experimentally obtained in different material system. In particular, research on III-V TFETS has been advancing rapidly in recent years due to that they exhibits higher ON currents than TFETs from group IV materials (Si or Ge). The limited ON current is, in fact, one of the major uncertainties of these devices. However, there are projections for ON currents of 1900µA per micrometer of channel width with 0.4 V supply voltage [9] which would be competitive with respect to high performance MOSFET. Revisions of state of the art in TFETs development can be found in [10], [11].

At the circuit level, there are design challenges associated to the distinguishing characteristic of TFETs with respect to MOSFETs, including super-linear onset, ambipolarity, enhanced Miller capacitance effect due to dominance of gate to drain capacitance or asymmetric conduction, also referred as unidirectional current conduction.

It is well known that due to this later characteristic, the topology of pass-transistor logic circuits or static random access memory cells require to be modified from those used in CMOS [12], but there are also circuit operation effects in complementary logic gates associated with the asymmetric conduction.

In [13] circuit operation effects associated to the low conduction of the *n*-type (*p*-type) TFET transistors with negative (positive) drain to source voltage are analyzed. They show that relatively high voltages can be bootstrapped within digital TFETs circuits which may have significant speed and reliability impacts and propose redesign at the logic level to mitigate this problem. In [14] this unidirectional conduction is analyzed in relation to the crosstalk phenomenon, which is exacerbated by technology scaling and short transitions times. In this context, they show that because this characteristic of TFETs, coupling cause significant delay variation and degrade performance.

In this paper the operation of TFETs circuits under crosstalk conditions is analyzed in depth and a novel topology for complementary tunnel transistors gates which mitigates the performance degradation cause by noise coupling in TFET circuits is described and evaluated.

Simulations have been carried out using TFET transistor models from Notre Dame University, corresponding to double-gate p–i–n InAs TFETs [15]. The current model, based on the Kane-Sze formula for tunneling, is valid in all four operating quadrants [16]. Gate length for both *n* and *p* transistors is 20nm. For comparison purpose, simulations of CMOS circuits have been also carried out. Predictive PTM models [17] with channel lengths similar to the available

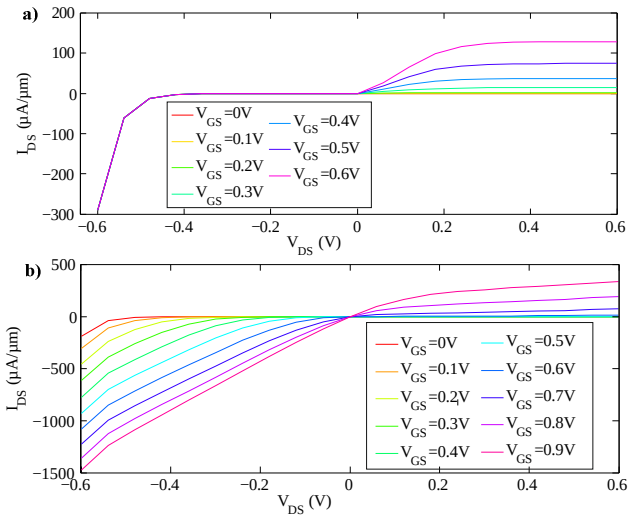

Fig. 1 *I-V* characteristics a) *n*-TFET b) *n*-MOSFET.

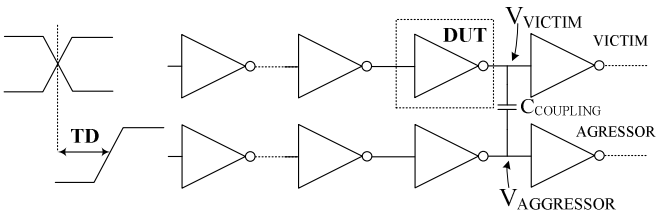

Fig. 2 Schematic of circuit used for crosstalk analysis after [14].

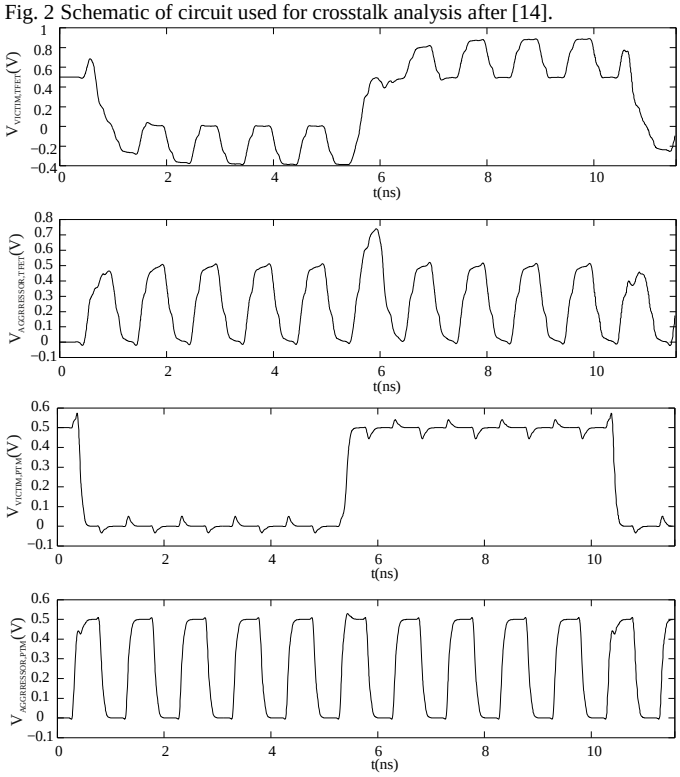

Fig. 3 Waveforms showing behavior under crosstalk for TFET and PTM circuits.

TFETs have been used. Fig. 1 depicts I_{DS}-V_{DS} for both *n* transistors. Differences for negative V_{DS} values are evident.

The paper is organized as follow. Section II analyzes the speed degradation produced by crosstalk associated to the asymmetric conduction of TFET transistors. Section III describes the proposed topologies for complementary gates which overcomes this limitation and evaluates its performance in terms of power overhead. Finally, Section IV summarizes some conclusions.

II. Efect of non-symetric conduction of TFETs under Crosstalk

Fig. 2 depicts the schematic of the circuit we have used for the crosstalk analysis [14]. Fig. 3 shows waveforms comparing TFET and CMOS behavior. Identical inputs have been applied to the TFET and PTM circuits. V_{VICTIM} for the TFET circuit ($V_{VICTIM,TFET}$) and for its PTM counterpart ($V_{VICTIM,PTM}$) are shown. It is clear that they are very different. In both cases, it is observed that the rising of $V_{AGGRESSOR}$ signal is capacitively coupled to the output of the DUT inverter (V_{VICTIM}) and the victim node goes beyond the positive supply voltage when it is at logic 1. For CMOS gates, the pull-up network (single *p*-MOSFET in this example) is able to sink current such that voltage noise at the output disappears. However, due to the low conduction of *p*-TFETs with positive V_{DS}, pull-up network of TFET gates (single PTFET in this example) cannot discharge $V_{VICTIM,TFET}$, which results in a sustained voltage over V_{DD}.

Similarly, it can be observed that the falling switching of $V_{AGGRESSOR}$ signal is capacitively coupled to the output of the DUT inverter (V_{VICTIM}) and the victim node goes beyond the negative supply voltage when it is at logic 0, resulting in a negative sustained voltage noise in the TFET circuit.

The magnitude of the sustained coupling noise is related to the ratio of the fixed to coupling capacitance and supply voltage. It increases with the later and decreases with larger fixed capacitance. There could be reliability concerns associated to the large voltages appearing in the circuit.

In addition, there are timing concerns. Delay increases due to larger voltage swing. Fig. 4 illustrates the delay increment. The responses at the output of the victim inverter for different conditions at the output of the aggressor inverter are compared. Signal OUT_{COUP} is the output of the inverter when the aggressor output is switching producing sustained noise pulses. *OUT* is the response of the inverter when the aggressor does not switch (IN_{VICTIM} is the input of the victim inverter). Both propagation delays have been measured for different

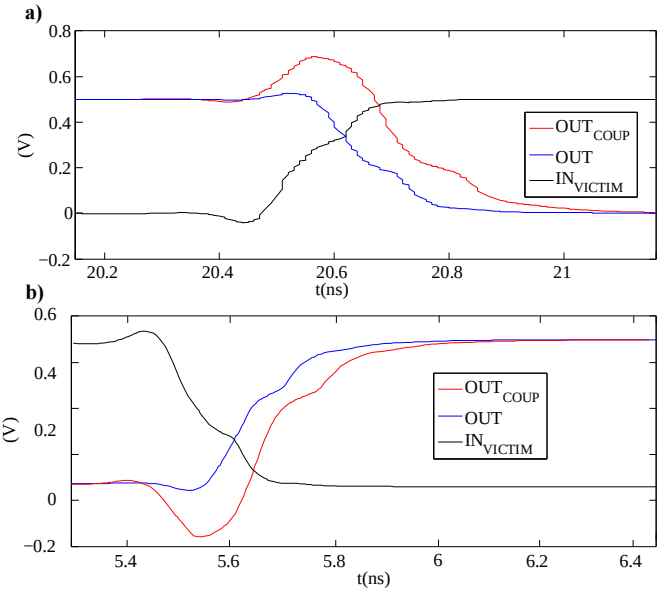

Fig. 4 Waveforms illustrating delay increment produced by crosstalk for both (a) falling and (b) rising edges of the victim.

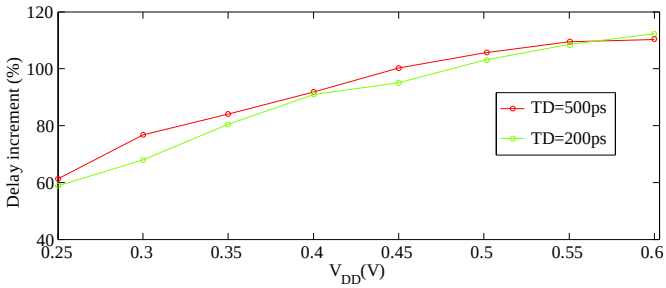

Fig. 5 Measured delay increment.

supply voltages (V_{DD}), coupling capacitance values and victim-aggressor input delay. Fig. 5 reports measured average delay increments (%) versus V_{DD} for $C_{COUPLING}$=0.2fF and two values of *TD* (200ps and 500ps).

Two types of solutions are discussed in [13] for the bootstrapping problem. First they suggest engineering of the TFET´s I-V characteristic along with low voltage operation. Second, logic redesign including buffer insertion and input ordering swapping is also considered. Unlike, we propose a modification of the gate topology to overcome the problem.

III. PROPOSED COMPLEMENTARY GATE

The rationale of our proposal is providing a conduction path alternative to the natural one to charge/discharge noise voltage pulses at the gate output. By natural one, we mean the *p* transistor with positive V_{DS} (in general the *p*-type pull-up network) for positive noise pulses and the n transistor with negative V_{DS} (in general the n-type pull-down network).

A *p*-type transistor with its source connected to the output node, its drain to V_{DD} and its gate connected to negative supply voltage (Fig. 6a) would be able to discharge a positive noise pulse. Such p-transistor might be also useful to cope with a negative noise pulse due to the diode current occurring for enough large positive V_{DS}. This transistor in this situation exhibits a drain to source voltage greater than V_{DD}. Thus depending on V_{DD} it could solve also the negative noise pulse. In the same way, an *n*–type transistor with its source connected to the output node, its drain to negative supply voltage and its gate to V_{DD} (Fig. 6b) would be able to charge a negative noise pulse. Equivalently, the added *n*-transistor could be able to discharge a positive noise pulse. Therefore, we explored topologies with a single added transistor (*N* or *P*) and with the two extra transistors (*NP*) [18].

However, not only the capability of a single extra transistor to cope with both types of noise pulses depends on selected V_{DD} value, but also the power performance of the modified gates. The usefulness of each of the above mentioned topologies and its power performance have been evaluated for different supply voltages. TABLE I. summarizes results. Data on delay reductions for high to low transitions obtained by each modified topology and their power overheads with respect to the standard complementary one are reported. Delay reductions increases with supply voltage for the three topologies. This is due to the fact that the amplitude of the noise pulses directly depends on V_{DD} and so delay degradation is more important for larger V_{DD} values and the modified topologies, which mitigates this phenomenon, achieves larger speed improvements. It is also interesting comparing the results obtained for the three topologies. For lower V_{DD} values, the *N* topology is worse than the *P* one in reducing delay. This is because the *P* topology is exploiting tunnel conduction (V_{DS} negative) while the *N* one is mitigating the positive noise pulse through an NTFET biased with negative V_{DS}. However for the larger V_{DD} values, delays improvements are more important in the *N* topology. This is because the extra n-transistor is now biased with a large enough negative V_{DS} activating diode current, being more efficient to discharge the noise pulse. Delay reductions for both modified topologies are comparable at V_{DD} =0.4V. A similar behavior has been obtained for delays reduction associated with low to high switching, but now the role of the *n* and the *p* transistors is exchanged. The *NP* topology obtains speed improvements similar to the best one between the other two modified topologies.

Note that the reported reductions cannot be directly compared to the delay increments depicted in Fig. 5 because percentage has been calculated with respect to distinct reference delays values. In Fig. 5, delay increment is evaluated with respect to the delay without crosstalk effect, while delay reduction is evaluated with respect to the delay with coupling due to crosstalk. The latter is larger than the former by the amount shown in Fig. 5. For example for V_{DD}=0.45V, delay increment is around 100% in Fig. 5 and delay reduction is 40% for *NP* topology. Thus, delay increment of *NP* topology with crosstalk effect with respect to the standard topology without crosstalk effect is only 20%. The effect of crosstalk on delay has been reduced from 100% to 20%.

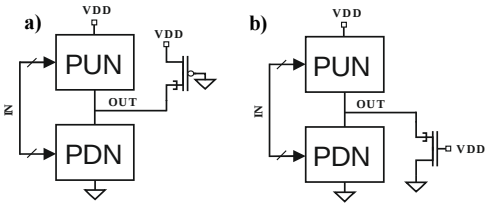

Fig. 6 Alternative options to cope with noise pulses a) flipped *p*-type transistor b) flipped *n*-type transistor

TABLE I. CHARACTERIZATION OF *N*, *P* AND *NP* TOPOLOGIES

V_{DD}	Delay reduction (%)			Power overhead (%)		
	N	*P*	*NP*	*N*	*P*	*NP*
0.25	0.38	16.83	12.70	-3.47	-3.95	-3.47
0.30	5.85	21.75	20.08	5.23	4.65	6.10
0.35	17.75	26.72	26.50	2.72	-2.96	0.06
0.40	31.69	32.00	34.06	4.36	4.45	18.10
0.45	42.10	35.72	40.39	31.91	32.05	71.05
0.50	45.91	36.98	44.97	94.54	94.75	184.51
0.55	48.01	36.69	47.51	212.32	212.56	379.56
0.60	49.29	35.13	48.60	407.46	407.67	663.61

Unacceptable power overheads have been obtained for V_{DD} over 0.4V. For those supply voltages, when the output of the gate is at logic 0, the extra *p*-transistor is biased with a large enough positive V_{DS} activating diode current and enabling a DC current path from V_{DD} to ground which translates in static power consumption. That is, the same conduction mechanism which makes possible that the extra *p*-transistor can be applied to manage negative noise pulses if V_{DD} is enough high, causes important power overheads if V_{DD} is too high. Similarly, when the output of the gate is at logic 1, the extra *n*-transistor is biased with a large enough negative V_{DS} able to activate diode current. The worst power penalties are for the topology with the two extra transistors because both output values exhibit DC current. Power data in this experiment has been obtained at 500MHz, except for V_{DD}=0.25 which has been obtained at 100MHz. At lower frequencies the contribution of the static

power to the total power is more important and even larger penalties are produced.

Fig. 7 shows simulation results for the three topologies at V_{DD} =0.5V supporting previous explanation. Each output signal (in blue) is depicted together with the current provided by its supply source (in green). DC currents are clearly observed as well as associated output voltage level degradation.

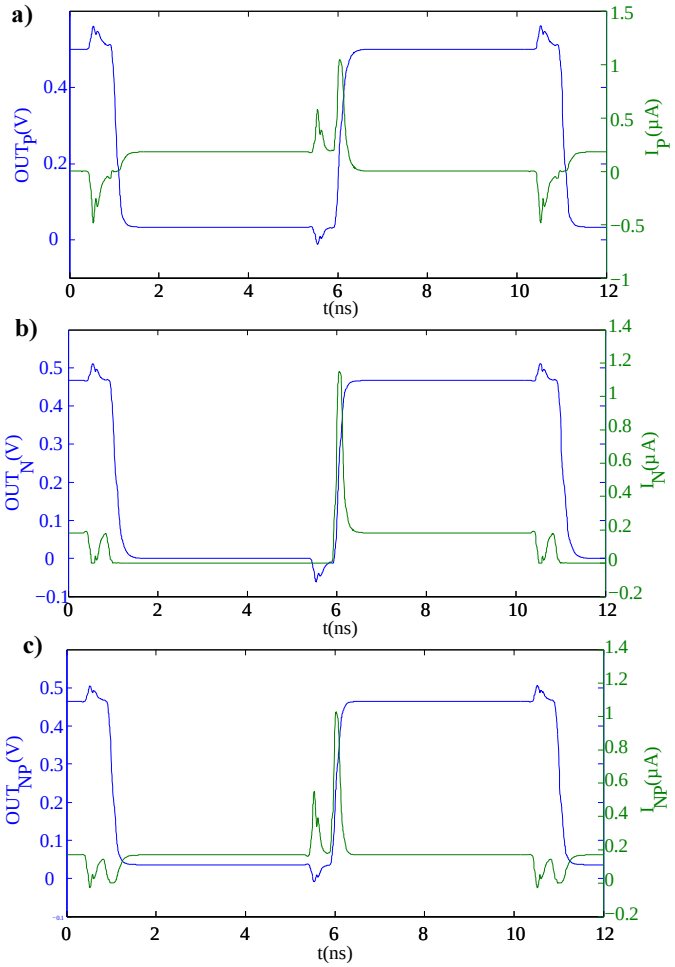

Fig. 7 Waveforms illustrating the behavior of (a) *N*, (b) *P* and (c) *NP* topologies.

TABLE II. CHARACTERIZATION OF *NP2* TOPOLOGY

V_{DD}	*NP2*	
	Delay reduction (%)	Power overhead (%)
0.25	8,58	-5,82
0.30	14.46	4.45
0.35	20.14	-4.55
0.40	26.85	-5.56
0.45	32.03	-4.95
0.50	35.18	-4.37
0.55	36.60	-3.69
0.60	37.30	-2.46

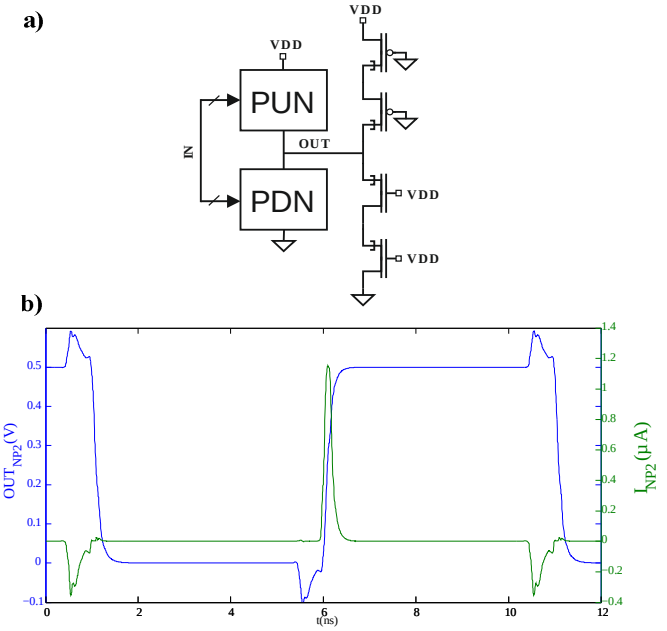

Fig. 8 (a) Proposed *NP2* topology. (b) Simulation results that illustrate the operation on the *NP2* topology.

In order to be able to operate circuits over 0.4V without significant power overheads, it is required to eliminate the activation of the diode current. Extra p-transistor (n-transistor) should not be biased at large positive (negative V_{DS}). This can be achieved if each extra transistor is implemented by the two series connected transistors. Clearly this translates in topology with extra n transistors being not able to mitigate positive noise pulses and in the same way, topology with extra p-transistors are not able to mitigate negative noise pulses. Fig. 8a depicts the generic topology proposed for complementary TFET gates (*NP2*). Fig. 8b shows simulations equivalent to those in Fig. 7 for the novel topology. It can be observed that there is not static current and full logic swing is obtained. Results in TABLE II. characterize the proposed topology in terms of delay reduction and power penalties with respect to standard complementary implementation. Compared with results in TABLE I. delay improvements are slightly reduced because conduction has been decreased. Power overheads have been eliminated.

IV. CONCLUSIONS

The non-symmetric conduction of tunnel transistors (TFETs) degrades the speed of TFETs circuits under crosstalk. Positive and negative voltage pulses beyond rail voltages appear in theses circuits increasing logic swing and thus rising gate delays. Extra flipped *p*-type and *n*-type transistors can be used to discharge and charge the noise pulses. However, increasing supply voltage activates diode current leading to unacceptable power overheads. The proposed modified complementary gate topology reduces delays with respect to standard one without such power limitation.

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