Design of a Power-Efficient Widely-Programmable Gm-LC Band-Pass Sigma-Delta Modulator for SDR

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***Abstract*—This paper presents the design and implementation of a fourth-order band-pass continuous-time $\Sigma\Delta$ modulator intended for the digitization of radio-frequency signals in software-defined-radio applications. The modulator architecture consists of two Gm-LC resonators with a tunable notch frequency and a 4-bit flash analog-to-digital converter in the forward path and a non-return-to-zero digital-to-analog converter with a finite-impulse-response filter in the feedback path. Both system-level and circuit-level reconfiguration techniques are included in order to allow the modulator to digitize signals placed at different carrier frequencies, from 450MHz to 950MHz. A proper synthesis methodology of the loop-filter coefficients at system level and the use of inverter-based switchable transconductors allow to optimize the performance in terms of robustness to circuit errors, stability and power consumption. The circuit, implemented in 65-nm CMOS, can digitise signals with up to 57-dB SNDR within a 40-MHz bandwidth, with an adaptive power dissipation of 16.7-to-22.8 mW and a programmable 1.2/2GHz clock rate[1].**

I. Introduction

Continuous-Time $\Sigma\Delta$ Modulators (CT-$\Sigma\Delta$Ms) are proving to be a competitive solution for the implementation of power-efficient Analog-to-Digital Converters (ADCs) operating in the GHz range, thus opening the door to use them in *digital-intensive* Radio-Frequency (RF) transceivers and Software Defined Radio (SDR) [1]–[7]. One of the trends to implement such SDR receivers consists of placing a Band-Pass (BP) CT-$\Sigma\Delta$M as close as possible to the antenna, yielding to the so-called *RF-to-digital converters* [1], [4], [6], [8]–[10]. These $\Sigma\Delta$M-based RF *digitizers* include diverse strategies to reduce their aggressive specifications in terms of the sampling frequency (f_s) and the Dynamic Range (DR), including, among others, embedded out-of-band filtering [1], frequency-translating and *undersampling* or *subsampling* [6]. The latter allows to digitize RF signals placed at $f_{\text{RF}} > f_s/2$, while keeping high values of the OverSampling Ratio (OSR), since the signal bandwidth is typically $B_w \ll (f_{\text{RF}}, f_s)$. Other authors have proposed the use of a tunable center frequency or *notch frequency* in order to simplify the design of the frequency synthesizer needed in the RF receiver [4], [6], [11].

In spite of their potential benefits, the performance of CT-$\Sigma\Delta$ RF-to-digital converters is still well short of what is needed for comercialization. The main challenge is associated with the design of the loop filter, so that a high-quality and accurate resonance can be achieved, while keeping the necessary tuning range, robustness and stability. Thus, LC tanks are great from a power and linearity perspective but typically support a reduced range, whereas active-RC resonators can be widely tunable but require amplifiers with high gain at the ADC center (RF carrier) frequency.

One of the key points to address these challenges is to optimize the design of BP CT-$\Sigma\Delta$Ms by properly selecting the modulator loop-filter coefficients in terms of tunnability, resonator input/output swing and simplicity of the circuit implementation. This paper contributes to this topic and describes the design and layout-level implementation of a fourth-order Gm-LC BP CT-$\Sigma\Delta$M in a 65-nm CMOS technology. A systematic methodology is used to optimize the loop-filter design in order to reduce the power consumption to be competitive with conventional baseband digitization, while keeping the benefits of RF digitization. Simulation data feature 9-bit effective resolution for 40-MHz signals placed at 450-to-950 MHz with scalable 16.6-to-22.7mW power dissipation.

II. Modulator Architecture

Fig. 1 shows the modulator architecture. It consists of a fourth-order BP CT-$\Sigma\Delta$M with multi-bit ($B = 4$ bit) quantizer and a loop filter made up of two LC-based resonators with a transfer function, $R(s) = \omega s/(s^2 + \omega^2)$, where normalized values of s and ω are considered with respect to f_s, so that $s = 2\pi f/f_s$ and $\omega \equiv 2\pi f_n/f_s$. For synthesis purposes, the forward-path coefficients are defined as $k_{1,2} = k/SfR_{1,2}$ and $k_3 = 1/(SfR_1 \cdot SfR_2)$, where k is a coefficient used to equalize the Signal Transfer Function (STF) and $SfR_{1,2}$ are the scaling caling coefficients which modify the resonator gain, $R_{\text{gain}} = \omega \cdot s$ [11] . The feedback path consists of a Non-Return-to-Zero (NRZ) Digital-to-Analog Converter (DAC) and a two-tap half-delayed Finite-Impulse-Response (FIR) filter, with scaling coefficients, c_i and c_{id}, that provide the necessary degrees of freedom in the synthesis of the Noise Transfer Function (NTF) when applying a CT-to-DT equivalence. Additional feedback paths with scaling gains, c_{0j}, are included to compensate for the Excess Loop Delay (ELD) error.

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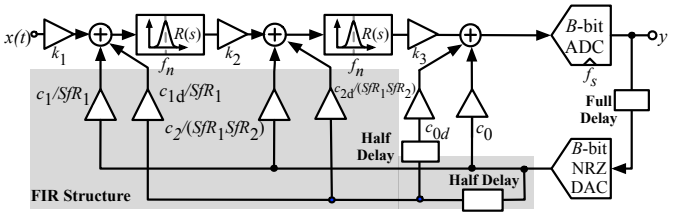


Fig. 1. Block diagram of the fourth-order BP CT-ΣΔM.

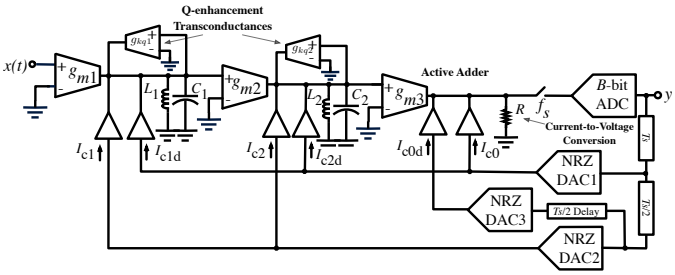


Fig. 2. Conceptual Gm-LC schematic of the proposed modulator.

A. Gm-LC Implementation

The BP CT-ΣΔM in Fig. 1 can be implemented using any arbitrary CT circuit technique, either active-RC or Gm-LC. In this work, a Gm-LC implementation – conceptually depicted in Fig. 2 – has been considered, where $g_{m1,2} = k_{1,2} \cdot C \cdot \omega \cdot f_s$, $g_{m3} = k_3/R$, $I_{c0,c0d} = (c_0, c_{0d}) \cdot V_{\text{FS}}$, $I_{c1,c1d} = (c_1, c_{1d}) \cdot g_{m1} \cdot V_{\text{FS}}$, $I_{c2,c2d} = (c_2, c_{2d}) \cdot g_{m2} \cdot V_{\text{FS}}/SfR_1$, and $V_{\text{FS}} = 1$V stands for the full-scale reference voltage. A fully differential version of this circuit – not shown in Fig. 2 for simplicity – is implemented in practice. All transconductors are realized as multiples of a unitary transconductance element, g_{mu}. The quality factor, Q, of Gm- LC resonators is enhanced by adding two extra transconductances, $g_{kq1,2}$. The 4-bit quantizer is made up of a flash ADC in the loop-filter forward path and a NRZ current-steering FIR-DAC in the feedback path.

B. High-Level Synthesis

The modulator in Fig. 2 has been synthesized by applying a CT-to-DT transformation to a BP DT-ΣΔM with a NTF which satisfies the required specifications in terms of DR and signal bandwidth, B_w. To this end, the Schreier's toolbox is used to synthesize the NTF for a given value of f_n and Out-of-Band Gain (OBG), and the modulator loop-filter is derived from the impulse-invariant transformation. Once the ideal NTF and STF have been synthesized, the best values of the loop-filter coefficients are selected in order to optimize the performance of the BP CT-ΣΔM in terms of robustness and stability, while maximizing DR and the Signal-to-(Noise+Distortion) Ratio (SNDR) with the minimum power consumption, P.

The values of DR and SNDR can be computed from simulation by using SIMSIDES [12] and P can be approximately estimated as the sum of the power consumed by resonators, P_{RES}, by the active adder, P_{ADD}, and by the embedded quantizer, i.e. the ADC and the DAC. The latter is estimated from electrical simulations from Cadence Spectre®, whereas P_{RES} and P_{ADD} are respectively derived as:

$$P_{\text{RES}} = V_{\text{DD}} \cdot \left[\sum_{i=1}^{2} (I_{ci} + I_{cid}) + \frac{g_{m1} + g_{m2}}{g_{mID}} \right]$$
$$P_{\text{ADD}} = V_{\text{DD}} \cdot \left[\frac{g_{m3}}{g_{mID}} + \frac{c_0 + c_{0d}}{R} \cdot V_{\text{FS}} \right] \quad (1)$$

where V_{DD} is the supply voltage and g_{mID} stands for the transconductance-versus-current efficiency. In this design, the same capacitances, $C_1 = C_2 = C$, inductances, $L_1 = L_2 = L$, and Q-enhancement gains, $g_{kq1} = g_{kq2} = g_{kq}$, are assumed for both resonators.

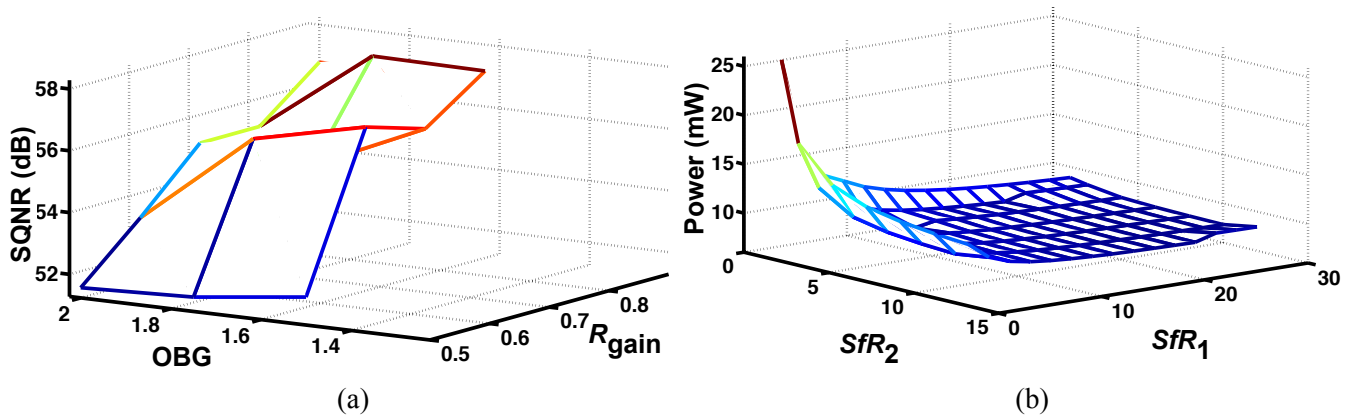
Given a set of specifications defined in terms of SNDR, B_w and P, the optimization procedure can be formulated as a design problem with five design variables, namely: OBG , R_{gain}, $SfR_{1,2}$ and g_{kq}. In order to optimize these design variables, the following step-by-step procedure has been followed:

- Step 1, in which parameters R_{gain} and OBG are optimized based on a parametric simulation analysis, where R_{gain} and OBG are swept, and the rest of parameters are fixed to ideal values
- Step 2, where parameters SfR_1 and SfR_2 are optimized. At this step, ideal values of $g_{kq1,2}$ are used, and R_{gain} and OBG are set to the values obtained at step 1
- Step 3, where the parameters $g_{kq1,2}$ are optimized and the rest of parameters are fixed to the values determined at the previous steps.

Fig. 3 illustrates the above step-by-step optimization procedure by depicting some parametric analysis carried out at steps 1 and 2. At each optimization step, a SIMSIDES model of the modulator shown in Fig. 2 is simulated and initial ranges considered for the design variables are heuristically set based on the designers experience. The design parameters are selected according to the trade-off obtained between SNDR, P, and stability. Table I summarizes the results of this optimization procedure by showing the values of selected design parameters for each standard and operation mode targeted by the modulator. One of the key strategies to minimize P consists of reducing the values of k_i coefficients, which is compensated by increasing the gain of the active adder in order to obtain the necessary loop-filter gain. The values of main circuit elements, i.e. transconductors, capacitors and inductors can be computed from the coefficient values shown in Table I by using the expressions described above, and are used to start the design of the modulator subcircuits.

III. Circuit-Level Reconfiguration Techniques

The main subcircuits of the BP CT-ΣΔM in Fig. 2 are the Gm-LC resonators, the active adder and the 4-bit quantizer. The latter is implemented by using a conventional 4-bit flash ADC made up of a resistor ladder and regenerative-latch based comparators and a feedback current-steering DAC that uses cascode current cells to improve the output resistance. Special care is put in the reconfiguration and design strategies applied to the resonators and the active adder, since they are key factors to optimize the performance in terms of reconfigurability, power consumption and robustness to circuit variations.



(a) (b)

Fig. 3. Optimization procedure. (a) SQDR vs. OBG, R_{gain}. (b) P vs. $SfR_{1,2}$.

Fig. 4(a) shows a conceptual schematic of the Gm-LC resonators. The circuit is made up of an LC tank and reconfigurable transconductors – depicted in Fig. 4(b). The forward-path transconductors correspond to $g_{m1,2}$ in Fig. 2 and are used to process the resonator input signals, while feedback transconductors implement $g_{kq1,2}$ coefficients in Fig. 2. In both cases, the values of required transconductances are obtained by connecting switchable unitary inverter-based transconductors, so that depending on the operation mode in which the modulator is working, these unitary elements are either switched on or off (and powered down) in order to obtain the required ADC performance with the minimum power consumption.

A similar strategy is followed for the capacitors used in the LC tank, where a number of unitary MiM capacitors are connected through CMOS switches, which are controlled by digital logic in order to program the required notch frequency. An MOS varactor is also used to fine-tune the required resonance frequency needed in each case.

The analog active adder is one of the most critical building blocks of the BP CT-ΣΔM since it has to sum and amplify signals within the GHz range. This circuit has been designed to have a nominal gain of 64 in order to reduce the rest of loop-filter coefficients, with the subsequent benefits in terms of input/output swing, power dissipation and simplicity in the design of the transconductors described above. The price to pay is that a more complex circuit is needed to implement the adder. In order to achieve the required gain, a fourth-stage amplifier has been considered. Each stage is made up of a transconductor based on a similar topology to that shown in Fig. 4(b) and a transImpedance amplifier. This adder circuit constitutes one of the design bottlenecks of the presented modulator, by consuming a significant part of its overall power consumption.

TABLE I
HIGH-LEVEL SYNTHESIS OF THE BP CT-ΣΔM

Loop-Filter Coefficients

	c_0	c_{0d}	c_1	c_{1d}	c_2	c_{2d}
CDMA-450	−0.62	1.22	−2.92	2.76	1.72	−1.28
LTE-700	−0.73	1.33	−3.32	2.10	1.48	−2.07
GSM-900	−0.46	0.80	0	−3.32	−3.12	−1.28

System-Level Design Parameters

	OBG	SfR_1	SfR_2	R_{gain}	g_{kq1}(mS)	g_{kq2}(mS)
CDMA-450	2.5	16	4	1	5.8	5.8
LTE-700	2.5	16	4	1	2.0	2.0
GSM-900	2.5	16	4	0.8	1.6	1.6

Signal and Circuit Parameters

	f_n (GHz)	f_s (GHz)	L(nH)	C(pF)	R(kΩ)	Q
CDMA-450	0.45	1.25	6.7	18.6	1000	8.8
LTE-700	0.75	2	6.9	6.5	50	12.4
GSM-900	0.95	2	7.1	4.0	50	14.1

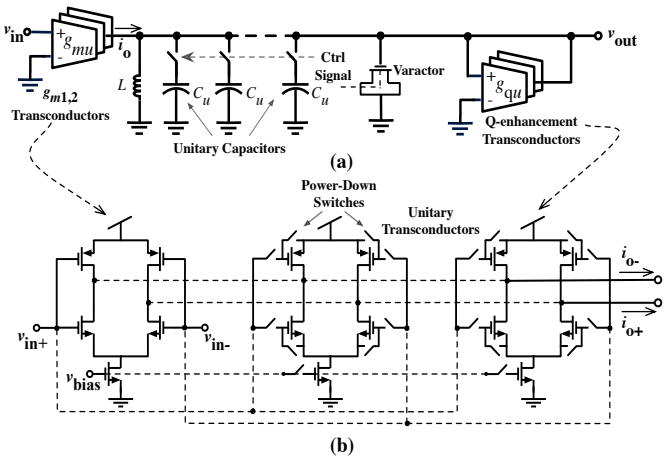


Fig. 4. Conceptual schematic of: (a) resonators and (b) transconductors.

IV. Layout and Simulation Results

The modulator has been implemented in a 65-nm CMOS technology. Fig. 5 shows the complete layout of the chip, highlighting their main parts. The modulator core occupies an active area of 1.55x1.55mm^2, and the layout floorplan considers separate analog, mixed and digital supplies, as well as guard-rings surrounding each section of the circuit. The area of the analog section is mostly devoted to the transconductors, inductors, capacitors, varactors, active adder, feedback DAC current sources and master-bias current generator. Comparator latches and switches are included in the mixed-signal section, while the digital part encloses the clock-phase generator and the required digital control/reconfiguration logic, that includes

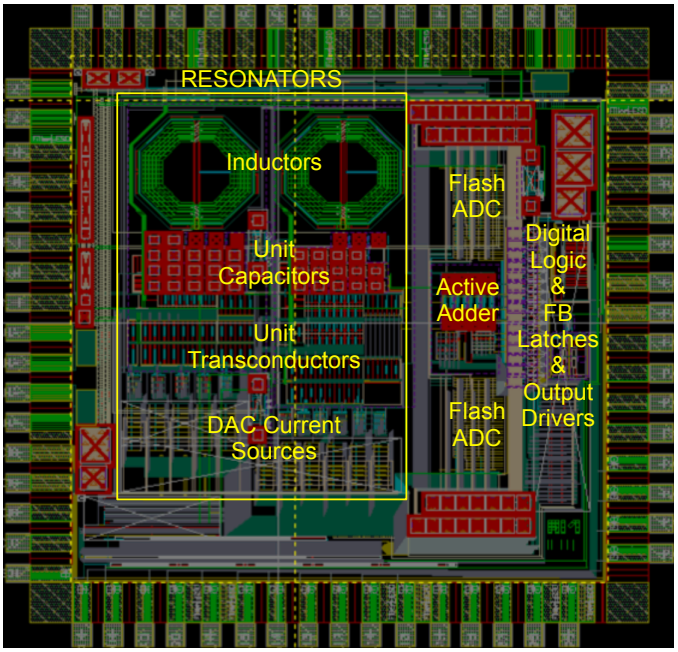


Fig. 5. Chip layout highlighting their main building blocks.

a ROM and a 4-bit parallel-to-serial register to transform the 4-bit 1.25/2GHz output bitstream into a 16-bit digital output clocked at 500MHz to simplify the test. Calibration techniques have been also included in the chip in order to separately test critical building blocks of the modulator, i.e. resonators, adder and quantizer. To this end, on-chip test buffers and switches can be configured to check the resonators outputs as well as their corresponding input test signals.

As an illustration, Fig. 6 shows the output spectrum of the modulator corresponding to the CDMA operation mode. Finally, Table II summarizes the results of the modulator and compares its simulated performance with the state of the art in BP-ΣΔMs with programmable notch. Note that the presented design features the lowest power consumption, while keeping a competitive performance in terms of B_w, DR and Figure-of-Merit[2] (FOM).

V. Conclusions

The design of a Gm-LC fourth-order BP CT-ΣΔM in 65-nm CMOS has been presented. A key contribution of this design is based on a systematic synthesis methodology which optimizes the loop-filter coefficients at system level, and the transconductor implementation at circuit level, in order to efficiently digitize RF signals with 40-MHz bandwidth placed at carrier frequencies within the 450-to-950MHz band, while clocked at 1.25/2GHz. These results show the potential effectiveness of the presented techniques for practical implementation of SDRs and next-generation mobile systems.

[2]FOM metrics in Table II are defined as: FOMw $\equiv \frac{P(\text{W})}{2\cdot B_w(\text{Hz})\cdot 2^{\text{ENOB(bit)}}}$ and FOMs $\equiv$ DR(dB) $+ 10\cdot\log_{10}[B_w(\text{Hz})/P(\text{W})]$, where ENOB stands for Effective Number Of Bits.

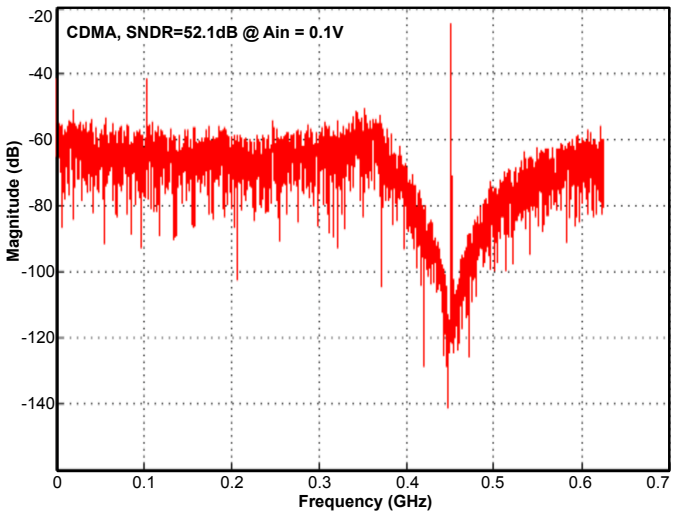


Fig. 6. Output spectrum of the modulator for CDMA standard.

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TABLE II
Simulated Performance Summary

	f_n,f_s(GHz)	B_w(MHz)	DR(dB)	P(mW)	FOMw(pJ/c)	FOMs(dB)
CDMA	0.45, 1.25	40	50	22.7	1.11	142
LTE	0.75, 2.0		57	22.8	0.48	149
GSM	0.95, 2.0		56	16.6	0.41	150
State-of-the-Art BP-ΣΔMs with Programmable Notch						
[4]	(0-1),(2-4)	150	69	550	0.8	153
[6]	(0.8-2),(2.6-3.4)	1	46	30	92.0	121
[7]	(0.7-2.7),(1.25)	15	43	90	26.9	103
[10]	(0.4-4),(2)	10	65	40.3	2015	149