Low-Voltage CMOS Log-Companding Techniques for Audio Applications

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Abstract. This paper presents a collection of novel current-mode circuit techniques for the integration of very low-voltage (down to 1V) low-power (few hundreds of μA) complete SoCs in CMOS technologies. The new design proposal is based on both, the Log Companding theory and the MOSFET operating in subthreshold. Several basic building blocks for audio amplification, AGC and arbitrary filtering are given. The feasibility of the proposed CMOS circuits is illustrated through experimental data for different design case studies in 1.2μm and 0.35μm VLSI technologies.

Keywords: Low-Voltage, CMOS, Subthreshold, Log, Companding, Audio, Design, Hearing-Aids

1. Introduction

The increasing market demand on portable System-on-Chip (SoC) applications has stimulated the search for new low-voltage and low-power analog techniques for mixed VLSI circuits. The critical design constrains in such products come from the battery technology itself, which imposes very low-voltage supply operation (down to 1.1V) combined with low-power figures (below 1mA) in order to extend battery life as long as possible.

In order to overcome the very low-voltage restriction in CMOS technologies, supply multipliers based on charge pumps [1] are commonly used, although some effort are being done in switched-capacitors filters for very low-voltage compatibility [2]. In most cases, doublers or triplers are included to boost the real internal operation of the analog parts of the SoC. However, supply multipliers tend to increase both die area and the number of discrete components around the SoC. Also, power efficiency may be strongly reduced in the final product.

On the other hand, Instantaneous Companding theory [3] and particularly Log processing [4] seems a good choice to implement general

analog processing under demanding specifications of supply scaling due to its inner voltage compression, so allowing true very low-voltage operation. Most of the reported works in such a current-mode technique have been only focused on BJT circuits [5, 6, 7, 8, 9, 10, 11, 12]. Furthermore, the few existing CMOS proposals suffer from poor low-voltage capabilities [13, 14, 15, 16] need of local bulks [17, 18] (i.e. separated wells required and not compatible with general anti latch-up rules of standard VLSI technologies) or lack of generalization [19, 20].

This paper performs a summary of novel CMOS circuit techniques based on the MOSFET operating in subthreshold (i.e. weak inversion region) for the low-voltage and compact integration of general Log processing, some of them already reported in [21, 22, 23]. The resulting circuit topologies are suitable for low-frequency (up to 100KHz) and optimized for very low-voltage (down to 1V) and low-power applications, such as Hearing Aids.

Next section makes a short review of Log Companding basis on amplification and filtering, and presents their generalization for MOS transistors. Then, a full set of CMOS basic building blocks are proposed in Section 3 for very low-voltage operation. Section 4 introduces some practical circuit realizations with experimental data. Finally, overall conclusions are argued in Section 5.

2. Log-Companding Principle of Operation and CMOS Generalization

The main scenario of the Companding processing is illustrated in Figure 1. In a current-mode scheme, y-variables are the externally-linear current signals (i.e. I) and all x's belong to the internally-compressed voltage domain (i.e. V) according to the following normalization:

(Place for Figure 1)

$$y \doteq \frac{I}{I_S} \qquad \overset{F}{\longleftrightarrow} \qquad x \doteq \frac{V}{U_t} \tag{1}$$

where I_S and U_t stand for the basic current-parameter of the specific semiconductor device and the thermal potential, respectively. In this context, the general Log Companding function is defined as:

$$y = F(x) = e^x \tag{2}$$

Typically, Companding chains involve *comp*ressing and ex*panding* stages which pre- and post-distortion signals according to F, respec-

tively. However, if a suitable non-linear processing is designed in the x-domain of Figure 1, the overall system can be kept externally linear, while resulting in an important reduction of the internal dynamic range (DR_x) respect to the incoming and outgoing signals (DR_y). The main advantage of this strategy comes from such a limitation in the internal voltage swings, which allows true low-voltage operation for the implemented circuits. In fact, when applied to VLSI circuits where parasitic devices are mainly capacitive, this inner voltage compression makes the Companding strategy not only suitable for very low-voltage supplies, but also for high-frequency and low-power applications, and even compatible with non-ideal devices (e.g. non-linear capacitors).

For the CMOS circuit implementation, the following MOSFET equations in weak inversion ($V_{SB,DB} \gg \frac{V_{GB}-V_{TO}}{n}$) will be taken from the EKV model [24]:

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} \left(e^{-\frac{V_{SB}}{U_t}} - e^{-\frac{V_{DB}}{U_t}} \right) \qquad I_S = 2n\beta U_t^2 \tag{3}$$

which can be simplified in forward saturation as:

$$I_D \simeq I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \qquad (V_{DB} - V_{SB}) \gg U_t \tag{4}$$

and where I_S, n, β, V_{TO} stand for the specific current, subthreshold slope, current factor and threshold voltage of the MOS transistor, respectively. From the above device characteristics, three CMOS Log Companding F functions at transistor level are proposed here according to the terminal used to compress the internal voltage signal: Gate (GD), Bulk (BD) or Source (SD) driven, as shown in Figure 2 and where V_{bias} stands for the suitable reference supplied by the biasing circuitry. Following device model in equation (4):

(Place for Figure 2)

$$I = F(V) = \begin{cases} I_S e^{-\frac{V_{TO}+nV_{bias}}{nU_t}} e^{\frac{V}{nU_t}} & \text{GD} \\ I_S e^{\frac{V_{bias}-V_{TO}}{nU_t}} e^{\left(1-\frac{1}{n}\right)\frac{V}{U_t}} & \text{BD} \\ I_S e^{\frac{V_{bias}-V_{TO}}{nU_t}} e^{-\frac{V}{U_t}} & \text{SD} \end{cases} \qquad I > 0 \tag{5}$$

Since our interest is focused in new circuit techniques compatible with the anti latch-up rules of standard VLSI processes, the rest of this study will be focused on the GD and SD alternatives only (i.e. Bulk terminals in all schematics will be not shown and assumed to be connected to the supply potentials). In this sense, the required processing in the Log domain for arbitrary amplification and filtering

and their general implementation through MOS devices operating in subthreshold is obtained in next subsections.

2.1. Amplification

The purpose of any amplifying stage is to obtain an output scaled copy (y_{out}) of the incoming signal (y_{in}):

$$y_{out} \doteq G y_{in} \tag{6}$$

where G stands for the Gain Factor. The equivalent processing in the compressed domain x, after the compressor and before the expander, can be obtained from applying the Companding function F in (2) to (6), so:

$$x_{out} = x_{gain} + x_{in} \tag{7}$$

where:

$$G \doteq e^{x_{gain}} \qquad G[\text{dB}] = 20 \log (e) x_{gain} \tag{8}$$

being x_{gain} the necessary gain control signal to keep the system externally linear. Direct control of x_{gain} allows electronic tuning for either fixed, programmable or time-variant amplification factors. Furthermore, the linear relation in decibels from (8) is of special interest when processing signals with large DR (e.g. audio applications).

In particular, the use of such logarithmic amplifiers simplifies the synthesis at system level of compression laws in AGC algorithms [25, 26]. In this sense, a general attenuation model is depicted in Figure 3, where the tilde operator (i.e. ˜) denotes signal envelope.

(Place for Figure 3)

The AGC system usually involves two Log amplifiers devoted to signal processing and control of the threshold knee point (y_{tk}), respectively. The feedback path begins starts by the effective output envelope ($\tilde{y}_{out}$), which sets the transient response of the whole loop. Typically, this block consists on a full-wave rectification (y_{rect}) plus two low-pass stages in parallel that set the attack (i.e. fast filter) and release (i.e. slow filter) times [27] for the particular signal processing application. The comparison between $\tilde{y}_{out}$ and the processed y_{tk} is then translated into the Log domain, where first-quadrant-only propagation automatically ensures linear operation for $\tilde{y}_{in} \leq y_{tk}$ (i.e. the threshold knee point). Once in closed-loop operation, the scaling factor m defines the non-linear compression curve:

$$\tilde{y}_{out} = \begin{cases} \tilde{y}_{in} & \tilde{y}_{in} \leq y_{tk} \\ y_{tk}^{m}\tilde{y}_{in}^{1-m} & \tilde{y}_{in} > y_{tk} \quad \text{and} \quad 0 < m < 1 \end{cases} \tag{9}$$

Hence, the resulting output DR reduction can be expressed using the Compression Ratio (CR):

$$CR \doteq \frac{\partial \tilde{y}_{in}[\text{dB}]}{\partial \tilde{y}_{out}[\text{dB}]} = \frac{1}{1-m} \qquad 0 < m < 1 \tag{10}$$

where upper and lower boundaries from (9) are fixed by the limiter (i.e. $CR = \infty : 1$, $m = 1$, $\tilde{y}_{out} \equiv y_{tk}$) and the linear amplifier (i.e. $CR = 1 : 1$, $m = 0$, $\tilde{y}_{out} \equiv \tilde{y}_{in}$), respectively. Note that AGC syllabic compression must not be confused with the circuit Companding approach itself, since the latter operates instantaneously, restores the original DR at the output, and it is directly synthesized at transistor level.

Based on the required processing in the compressed V-domain from equation (7), the general G-tuning strategy of Figure 4(left) is proposed. Two different CMOS techniques result from this idea: Gate (GC) and Source-Controlled (SC), which corresponds to the V_{gainGC} and V_{gainSC} sources in the same figure, respectively. Both matched devices M1 and M2 are supposed to operate in weak inversion saturation in order to implement the compression and the expansion functions.

(Place for Figure 4)

In fact, the two types of gain control can be mixed together and are compatible with all types of signal compression in (5). The unified expression of the resulting gain $G = I_{out}/I_{in}$ in the I-domain is given by:

$$G[\text{dB}] = 20\log(e)\left[\left(\frac{1}{n}\right)\frac{V_{gainGC}}{U_t} - \frac{V_{gainSC}}{U_t}\right] \tag{11}$$

Clearly, both control strategies require a Proportional-To-Absolute-Temperature (PTAT) voltage generator to cancel out their first-order thermal sensitivity [28]. However, some technological dependency still remains in the GC case through n, although this parameter shows little process spread. Furthermore, the SC approach exhibits better gain sensitivity than GC for the typical range of $1 < n < 2$. For example, a 40dB factor requires only a gain voltage of $4.6U_t$ in the SC case, while this control signal must be increased to $6.0U_t$ in GC topologies. Taking into account all these considerations, the Gate-Driven Source-Controlled (i.e. GD-SC) combination is chosen here as the most suitable

solution for amplification. Furthermore, the differential control voltage V_{gainSC} in Figure 4(left) is split into two sources referred to ground ($V_{gaini,o}$) as shown in Figure 4(right). This modification simplifies the synthesis of such low-impedance sources, as discussed later on, and also supplies two independent signals in the Log domain for amplification and attenuation control, respectively. From (11), the resulting Gain expression is:

$$G[\mathrm{dB}] = 20\log(e)\frac{V_{gaini} - V_{gaino}}{U_t} \tag{12}$$

showing a gain sensitivity to the control voltages of about 0.35dB/mV at room temperature. In practice, these gain control signals are usually limited to $0 < V_{gain} < 7U_t$, which corresponds to a total programmable amplification range as large as ±60dB.

2.2. Filtering

The basic integrator will be used here to illustrate the internal requirements of Log Companding filtering, whose equation is:

$$\frac{\mathrm{d}y_{out}}{\mathrm{d}t} \doteq \frac{y_{in}}{\tau} \tag{13}$$

being τ the integrator time constant. As proposed in [4], the equivalent processing in the compressed domain x of Figure 1 is obtained applying the Chain Rule to (13) and assuming that the internal state space variable (x_{out}) is stored in a grounded linear capacitor ($x_{cap} \equiv x_{out}$):

$$\frac{\mathrm{d}y_{out}}{\mathrm{d}t} = \frac{\mathrm{d}y_{out}}{\mathrm{d}x_{out}}\frac{\mathrm{d}x_{out}}{\mathrm{d}x_{cap}}\frac{\mathrm{d}x_{cap}}{\mathrm{d}t} = y_{out}\frac{\mathrm{d}x_{cap}}{\mathrm{d}t} \tag{14}$$

Then, if a tuning magnitude y_{tun} is defined as reported in [5], the above equation can be easily understood as a product of currents:

$$y_{out}\underbrace{C\frac{\mathrm{d}x_{cap}}{\mathrm{d}t}\frac{U_t}{I_S}}_{y_{cap}} = y_{tun}y_{in} \qquad y_{tun} \doteq \frac{CU_t}{\tau I_S} \tag{15}$$

where C stands for the capacitance value and y_{cap} is its current. Such multipliers are usually built in BJT implementations through the Translinear Principle (TP) [29]. A detailed revision of the TP for MOS devices can be found from these authors in [21]. However, the synthesis of an arbitrary N-order filter transfer function $H(s)$ requires in general multiple Translinear Loops (TLs) with shared components, which are

difficult to identify. Hence, the theoretical workround proposed in [6] is selected here to rewrite the product of (15) as:

$$y_{cap} = y_{tun} e^{x_{in} - x_{cap}} \tag{16}$$

The above expression defines the internal non-linear transconductance driving the integrator capacitor in order to achieve external linearity. Also, an equivalent State-Space (SS) matrix description is preferred here for generalization:

$$\begin{cases} \dfrac{\mathrm{d}I}{\mathrm{d}t} = AI + BI_{in} \\ I_{out} = CI + DI_{in} \end{cases} \tag{17}$$

where A, B, C, and D stand for the classic SS formulation of dynamic linear systems [30]. In practice, the second SS equation in (17) can be easily synthesized in the linear current domain through simple KCL algebra. Thus, the major design problem to be faced is reduced to implement N first-order Ordinary Differential Equations (ODEs) of the form:

$$\frac{\mathrm{d}I_i}{\mathrm{d}t} = \sum_{j=1}^{N} A_{ij} I_j + \sum_{j=1}^{M} B_{ij} I_{inj} \qquad \text{for } i = 1 \text{ to } N \tag{18}$$

From this point on, the specific internal non-linear processing depends on the particular CMOS Log Companding F functions proposed in (5). Applying such functions to the above equation, the equivalent non-linear ODEs in the compressed V domain can be expressed as :

$$C_i \frac{\mathrm{d}V_i}{\mathrm{d}t} = \begin{cases} \displaystyle\sum_{j=1}^{N} I_{tunAij} e^{\frac{V_j - V_i}{nU_t}} + \sum_{j=1}^{M} I_{tunBij} e^{\frac{V_{inj} - V_i}{nU_t}} & \text{GD} \\ \displaystyle -\sum_{j=1}^{N} I_{tunAij} e^{\frac{V_i - V_j}{U_t}} - \sum_{j=1}^{M} I_{tunBij} e^{\frac{V_i - V_{inj}}{U_t}} & \text{SD} \end{cases} \tag{19}$$

where tuning parameters for the A_{ij}-case are controlled through:

$$I_{tunAij} = \begin{cases} nU_t C_i A_{ij} & \text{GD} \\ U_t C_i A_{ij} & \text{SD} \end{cases} \tag{20}$$

showing a typical frequency sensitivity of about 0.16KHzpF/nA at room temperature. Similarly to the amplification topologies, PTAT current generators should be used in GD and SD options to eliminate first order thermal dependencies on frequency tuning [28].

By the simple inspection of (19), we propose a generalized CMOS solution for TLs based on building all MOS filters by means of matched

pairs in GD (i.e. common Source and Bulk) or SD (i.e. common Gate and Bulk) configurations as listed in Figure 5. Apart from the global thermal matching, technological matching for n and V_{TO} is assumed at pair and global levels for the SD and GD cases, respectively.

(Place for Figure 5)

3. Basic Building Blocks

Based on the generalization of the Log Companding theory for MOS devices presented in previous section, a full set of very low-voltage and low-power CMOS basic building blocks for both Log amplification and filtering are proposed as follows, including all the auxiliary circuitry required for biasing and tuning.

3.1. Amplification

Obviously, some extra circuitry must be added to the amplification cell of Figure 3 in order to allow proper operation of both key devices in terms of biasing, compensation and tuning. In this sense, a general low-voltage implementation is proposed in Figure 6, where I_{in} and I_{out} stand for the incoming and outgoing signals in the linear domain.

(Place for Figure 6)

First of all, a low-enough input impedance must be supplied at the compressor M1, as any current-mode block. For this purpose, a novel strategy is proposed in Figure 7, which makes use of local feedback at the M1 compressor through an Operational transResistance Amplifier (ORA). The role of the ORA block is not only to lower the input impedance, but also to operate M1 at the desired DC bias (I_{biasi}). Due to the resulting impedance values (typically below 1KΩ), optional V/I conversion in the input linear domain can be easily obtained by a simple series resistor and a decoupling capacitor. Furthermore, the proposed control technique minimizes the channel length modulation effect in M1, allowing minimum channel length selection for such a device. This possibility means an important Si area saving due to the wide aspect ratios usually required in compressors and expanders to keep such devices in weak inversion. The same technique applies to the expander transistor M2 provided that a similar control loop is included in the cascaded stage. A low-voltage CMOS implementation of the

above idea is proposed in Figure 7, where C_{in} and C_{comp} stand for the input parasitic and compensation capacitances, respectively. The resulting damping factor (ζ) of the compression stage can be computed via the following rational equation:

$$\zeta = \frac{1}{2}\sqrt{\frac{KC_{comp}}{C_{in}}} \tag{21}$$

(Place for Figure 7)

Hence, apart from its low-voltage compatibility, the proposed circuit implementation of Figure 7 exhibits a very simple frequency compensation procedure, unlike classical techniques as [31, 32, 33]. In fact, overshooting can be simply avoided by choosing a suitable $C_{comp} > 2C_{in}/K$.

Next design step is devoted to generate both the input bias level (I_{biasi}) and the proper value to be subtracted at the expander (I_{biaso}) in order to obtain a DC free output signal. Furthermore, the auxiliary circuitry dedicated to biasing must adjust dynamically such current references to any changes in the values of $V_{gaini,o}$ caused by gain programming or AGC feedback. In this sense, the key design parameter here is the maximum signal level allowed in compressors and expanders (I_{max}) according to power and DR issues. Biasing is performed in the circuit of Figure 6 through M7-M8 which act as a parallel GD-SC cell controlled by the same gain G and operated in open-loop as an attenuator (i.e. $I_{biasi} = I_{max}$). Its output is permanently monitored by M9-M10, so in case it exceeds the allowed range (i.e. $I_{biaso} > I_{max}$), the error amplifier M11-M12 automatically corrects the I_{biasi} value. The required copies of $I_{biasi,o}$ for both compressor and expander devices M1 and M2 are easily obtained through M13-M15 and M16, respectively. Hence, the proposed solution is compatible with either amplification ($G > 1$) or attenuation ($G < 1$) factors. The design variable N sets the resolution of the whole bias control: larger N values return better insensitivity to G, but in counterpart it may require some frequency compensation at the Gate of M7 for large $G \gg 1$.

Finally, built-in voltage-controlled voltage sources (VCVS) are needed even for fixed gain stages to translate the high-impedance PTAT reference or control signal (V_{ctrl}) to the desired low-impedance V_{gain} port of the amplifier in Figure 6. Again, due to the inner voltage compression of the GD-SC topology, $V_{gaini,o}$ signals are commonly limited to less than $7U_t$ (i.e. 175mV at room temperature), so no rail-to-rail operation is needed for such voltage sources. Taking benefit of this advantage, two different VCVS low-voltage CMOS implementations are proposed

in Figure 8. The first solution is optimized against technology mismatching by using the reduced group of devices M3-M6 to compute the error signal. On the other hand, the second approach generates lower output noise. In both cases, I_{source} should be chosen according to bandwidth and PSRR requirements of the particular application. Also for Figure 8(right), I_{source} must be chosen low-enough to not disturb the PTAT voltage reference V_{ctrl} due to transistor mismatching.

(Place for Figure 8)

3.2. Filtering

In general, several building blocks are required: compressor, expander and coefficients of the transconductance matrix (diagonal, positive and negative non-diagonal elements). These basic blocks can be implemented using either GD or SD techniques. We will also consider saturated and non-saturated cells, all of them compatible with the basic topological restrictions depicted in Figure 5.

By inspection of (19), two complete sets of low-voltage CMOS saturated cells are proposed in Figure 9. All boxed devices are supposed to operate in their weak inversion saturation region. The proposed compressors synthesize the following Companding functions:

$$I_{in} = F(V_{in}) = \begin{cases} I_{ref} e^{\frac{V_{in}-V_{ref}}{nU_t}} & \text{GD} \\ I_{ref} e^{\frac{V_{ref}-V_{in}}{U_t}} & \text{SD} \end{cases} \qquad I > 0 \qquad (22)$$

where I_{ref} and V_{ref} are the biasing design parameters in both the linear and the compressed domains, respectively. The separated definition of compressor and expander basic building blocks allows independence between signal range (I_{ref}) and frequency tuning (I_{tun}) specifications. Also, such splitting simplifies multi-path propagation of compressed input signals. Furthermore, all resulting filter topologies are compatible with syllabic circuit techniques [34]. Notice that transconductances for A and B coefficients are synthesized to only charge or discharge the SS variable stored in C_i. Such a simplification is derived from the Log nature of I/V compression which requires $I > 0$. We assume that a DC operating point exists for the given SS equations. Otherwise, a proper initial description should be obtained by classic matrix linear transformations. The role of the Operational transResistance Amplifier (ORA) is the same as in the amplifier cell of Figure 6. A Voltage Follower (VF) is mandatory for every capacitor in the SD case.

(Place for Figure 9)

An alternative set of CMOS basic building blocks based on no-saturated weak inversion operation are also proposed for Log filtering. These cells use the same Log Companding F function as the Saturated SD type given in (22), so both compressor and expander basic building blocks can be taken directly from Figure 9. However, in this case every coefficient of the SD differential equation in (19) is split as follows:

$$\begin{aligned} C_i \frac{\mathrm{d}V_i}{\mathrm{d}t} &= -\sum_{j=1}^{N} I_{tunAij} e^{\frac{V_i - V_j}{U_t}} + \dots \\ &\equiv \sum_{\substack{j=1 \\ j \neq i}}^{N} I_{tunAij} e^{\frac{V_i}{U_t}} \underbrace{\left(e^{\frac{-V_i}{U_t}} - e^{\frac{-V_j}{U_t}} \right)} - \sum_{j=1}^{N} I_{tunAij} + \dots \end{aligned} \tag{23}$$

Now, while the second series has an immediate correspondence to a DC current source attached to the grounded capacitor C_i, underbraced terms recall the MOSFET equation in weak inversion non-saturation from (3). The remaining part in (23) is equivalent to a signal dependent Gate tuning. Such a tuning can be exercised by using the low-voltage cells proposed in Figure 10, where a matched device operating in weak inversion saturation, fed at I_{tunAij} and sharing the same Source bias generates the required Gate control. As expected, the tuning parameter I_{tunAij} matches with the corresponding Saturated SD equation in (20). Again, a VF block is required to sense each grounded capacitor C_i, and also a Current Inverter (CI) may be needed in this case for negative coefficients.

(Place for Figure 10)

At a first glance, this strategy seems to suffer from limited DR due to the need of keeping M1 in non-saturation. But such a condition has not been supposed in the splitting of expression (23). In fact, the basic building blocks of Figure 10 work perfectly even once entered the saturation region, which can be understood just as an asymptotic case of the general conduction expression (3). In our particular case, saturation is equivalent to blocking the corresponding SD cell of Figure 9. In practice, this limit is difficult to reach due to the inner voltage compression of Log Companding. For example, taking the SD F function from (22), the resulting compressed swing for a 90% modulated input signal is reduced to:

$$\Delta V_{inj} = U_t \ln \frac{1.9 I_{ref}}{0.1 I_{ref}} \simeq 3U_t \tag{24}$$

A quick comparison between all types of CMOS basic building blocks reveals strongest area compaction for GD, and larger signal compression and better technology independence for both SD strategies. In addition, the non-saturated SD class simplifies optimization against technology mismatch as the VF blocks can be designed against such effects independently from the transistors operating in weak inversion. All the proposed basic building blocks exhibit very low-voltage capabilities, which can be exploited in each case through the tune of V_{ref}. Also, the DC current sources in non-saturated SD cells can be eliminated if a suitable SS matrix description is selected with the same operating points in all state variables.

Finally, two compact VF and CI+VF implementations are presented in Figure 11(a) and (b), respectively. Again, due to the internal voltage compression, both VF and CI auxiliary controls do not require rail-to-rail operation. Concerning the principle of operation for the compact solution CI+VF, basically it behaves like a Current-Conveyor [35], but supplying a voltage copy in W instead of the classic current copy. Starting at the Y terminal, the matched cascode-pair ensures that X follows Y voltage, while the rest of the local feedback loop causes that the current through Y matches with the corresponding one at X. Then, a simple follower generates the voltage copy at W. Since the X, Y and W nodes exhibit the same voltage level, all the grounded devices can work in non-saturation, allowing again very low-voltage operation.

(Place for Figure 11)

4. Design Applications

Following the proposed basic building blocks, this section presents some practical design examples for very low-voltage and low-power audio applications. All case studies include demonstrators to illustrate the use of these novel CMOS circuit techniques. Two different double-polySi double-metal VLSI processes of 1.2μm and 0.35μm and $V_{TON}+|V_{TOP}|$=1.3V have been used to integrate the design examples.

4.1. Dual AGC for Speech Intelligibility

This first design example consists of a complete AGC circuit for syllabic speech processing. The stage is built around the amplifier cell of Figure 6 following the high-level model of Figure 3.

For the envelope detection, a high-precision full-wave rectifier is proposed in Figure 12, where I_{out} and I_{rect} stand for the incoming output from the Log amplifier and the full-wave rectified signal, respectively. Since current offsets caused by technology mismatching are also related to current bias as well, the proposed circuit approach minimizes such component by choosing quiescent biasing levels as low as $I_{rectq} \in (1\text{nA}, 10\text{nA})$. However, a low-enough input impedance should be also guaranteed to allow DC decoupling, as seen in Figure 12. Both design constrains can be reached by the local feedback loop M1-M8, which ensures a low input impedance even for very low values of current biasing. Two operation cases should be distinguished: while positive phases of I_{out} are processed by M1-M5 devices, negative swings are rectified through M6-M8, so the full rectified waveform I_{rect} is finally collected via M9-M10. Some frequency compensation (C_{comp}) may be required depending on the $I_{rectbias}/I_{rectq}$ ratio.

(Place for Figure 12)

The remaining filtering for the effective envelope detection of Figure 3 is implemented through the non-saturated basic building blocks of previous section. For speech processing, two low-pass filters are usually combined with time constants around 10ms and 250ms to ensure fast protection against overshoots and speech intelligibility, respectively. In this case, both filters are tuned at $I_{tuno} = 10\text{nA}$, so integrating two equivalent linear resistors of about 2.5MΩ. Corner frequencies of 14Hz and 0.6Hz are selected using external capacitors of 4.7nF and 100nF, respectively. Finally, the compression ratio CR is implemented using the first-quadrant Log ruler of Figure 13, where boxed devices are supposed to operate in weak inversion saturation.

(Place for Figure 13)

In fact, the proposed circuit topology can be understood as the basic GD-SC amplifier of Figure 4(right) with its input and output fed at GI_{tk} and $\tilde{I}_{out}$, respectively. According to design equation (12) and for $V_{gaini} \equiv 0$, the resulting control signal $V_{ctrl} = V_{gaino}$ follows:

$$V_{ctrl} = \begin{cases} 0 & \tilde{I}_{in} \leq I_{tk} \\ U_t \ln\left(\frac{\tilde{I}_{in}}{I_{tk}}\right) & \tilde{I}_{in} > I_{tk} \end{cases} \quad (25)$$

Hence, the required first-quadrant only propagation of V_{ctrl} in Figure 3 is already implemented here by the boundary condition $V_{ctrl} > 0$. Continuous tuning of the AGC Threshold Knee point is reduced to program the I_{tk} current source.

The complete AGC has been integrated in a 1.2μm technology as depicted in Figure 14. The transient behaviour results in an Attack Time of $t_{att} = 15$ms and Release Times adapted to input burst duration up to $t_{rel} < 500$ms, as shown in Figure 15. Also, the flexibility of the presented CMOS circuit techniques allows independent programming of the AGC Threshold Knee point $I_{tk} > 3$nA, the Compression Ratio $CR \in (1, \infty)$, as well as the open loop Gain $G \in (0, +40\text{dB})$ through the V_{gaini} port. All this configurability is illustrated in Figure 16. With the new circuit techniques, the complete AGC stage can truly operate at 1.0V supply, while exhibiting a power consumption as low as 60μW. The resulting input DR is more than 72dB.

(Place for Figure 14)

(Place for Figure 15)

(Place for Figure 16)

4.2. Arbitrary Filtering for Audio Processing

The first circuit realization presented in this category is an one-input one-output second-order high-pass filter implemented through the Saturated SD basic building blocks of Figure 9. The complete filter has been integrated through the same 1.2μm CMOS process of previous example, as depicted in the microscope photograph of Figure 17. Corner frequency is tunable from 100Hz to 10KHz with continuous or digital control. The measured large signal frequency response at half full-scale input (i.e. $1\mu\text{A}_{peak}$) for $f_{-3\text{dB}} = 1$KHz is represented in Figure 18. The filter exhibits an in-band Total Harmonic Distortion (THD) around 0.5% at 50% full-scale output. In this example, a DR of 63dB is achieved for 10pF capacitance value per pole.

(Place for Figure 17)

(Place for Figure 18)

The second design example consists of a one-input two-output second-order band/low-pass filter, with the following SS description:

$$\begin{cases} A = \begin{bmatrix} -w_o/Q & -w_o/Q \\ Qw_o & 0 \end{bmatrix} & B = \begin{bmatrix} w_o/Q & w_o/Q \\ 0 & -Qw_o \end{bmatrix} \\ C = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} & D = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \end{cases} \tag{26}$$

where w_o and Q stand for the central frequency and the quality factor respectively. Band and low pass responses are available at the first (I_{out1}) and second (I_{out2}) outputs respectively. In this case, a dummy input has been introduced in (26) to ensure stability. Circuit reductions can be clearly seen for its Saturated GD implementation in Figure 19, where $C \doteq C_1 \equiv C_2$ and $I_{tuno} = nU_tCw_o$. The tuning capabilities of this realization are depicted in Figure 20 for different central frequencies and quality factors, showing a typical $THD < 0.4\%$ at central frequency for 50% full-scale, and $DR = 60$dB for 10pF pole capacitors.

(Place for Figure 19)

(Place for Figure 20)

Last example is the one-input one-output third-order low-pass non-saturated SD filter of Figure 21, where $I_{tuno} = U_tCw_o$. Such case illustrates the modularity of the presented basic building blocks by means of a cascaded structure. Nevertheless, complex poles can also be implemented using the complete set of non-saturated cells. In general, selection of filter order can be easily implemented through switch-off and by-pass as shown in the same schematic. The resulting implementation with 50pF/pole in a 0.35μm CMOS technology is depicted in Figure 22, while experimental transfer functions are reported in Figure 23. In this case, DR is typically around 70dB depending on capacitance values, while THD is below 0.5% up to 90% of full-scale.

(Place for Figure 21)

(Place for Figure 22)

(Place for Figure 23)

5. Conclusions

A collection of novel current-mode circuit techniques for the integration of very low-voltage (down to 1V) low-power (few hundreds of μA) complete SoCs in CMOS technologies has been presented. The new design proposals make use of both, the Log Companding theory and the MOSFET operating in weak inversion. The former enables compatibility with very low-voltage supplies, while the latter allows low-power consumption and integration in standard VLSI technologies. In order to extend the applicability of the presented strategy, complete sets of basic building blocks for amplification, AGC and arbitrary filtering are given for audio processing. The feasibility of the proposed CMOS circuits has been illustrated through experimental data for different design case studies. These circuit techniques have also been successfully applied to the synthesis of Pulse Duration Modulators [36] and the design of a complete SoC for an industrial Hearing-Aids application [23]. Further work is currently being done for the use of non-linear MOS capacitors in order to obtain all-MOS circuit implementations, as well as to apply the filtering techniques to the synthesis of $\Sigma\Delta$ Modulators for oversampling A/D audio converters [37].

Acknowledgements

Research partially supported by Spanish CICYT-TIC97-1159, CICYT-TIC99-1084 and European ESPRIT-FUSE-23068 projects.

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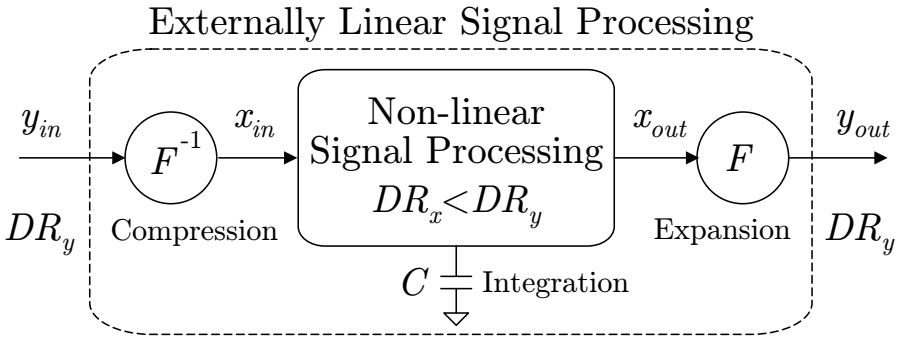

Figure 1. Generalized Companding processing.

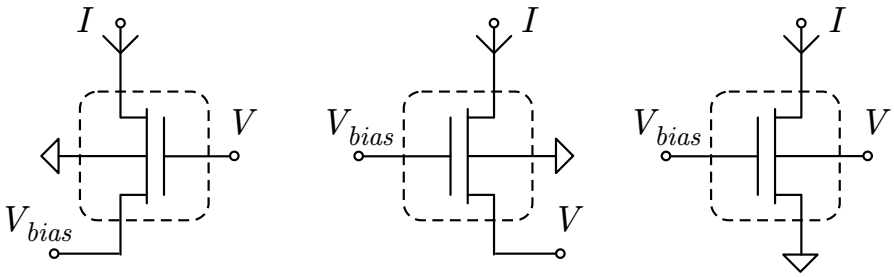

Figure 2. Transistor level GD (left), SD (center), and BD (right) implementation of the $F(x) = e^x$ Log Companding function (auxiliary circuitry not shown for simplification).

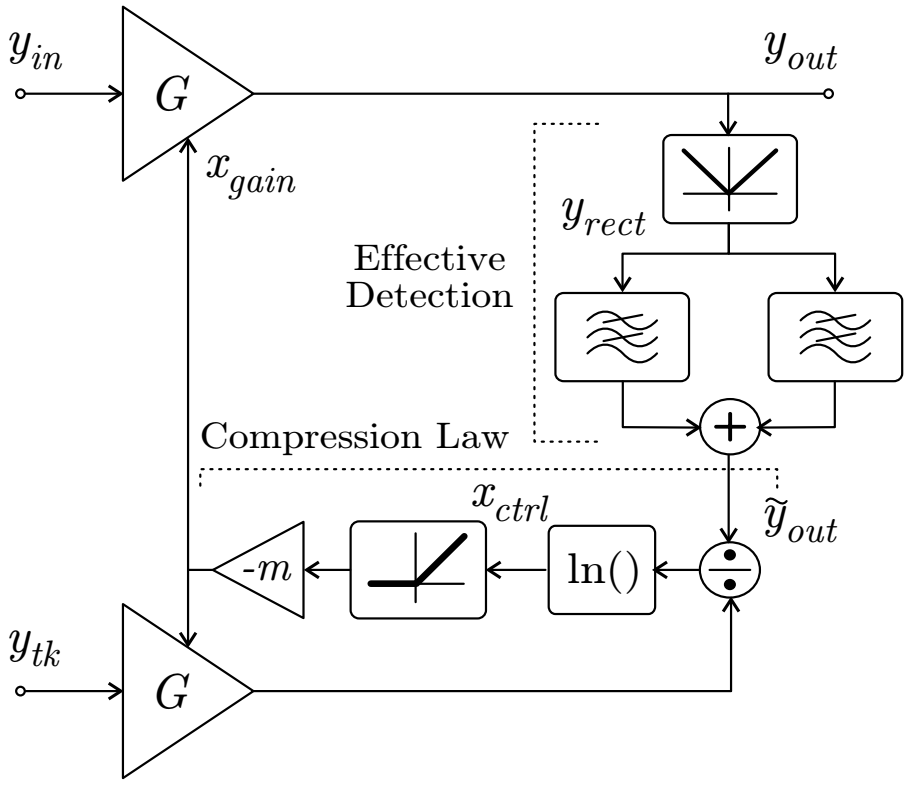

Figure 3. General AGC attenuation model using Log amplifiers, showing intermediate signals in the linear (i.e. y) and compressed (i.e. x) domains.

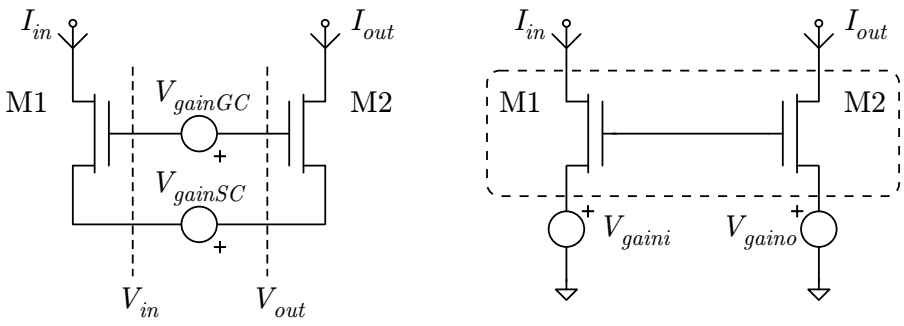

Figure 4. Summary of gain MOS topologies (left) and simplified schematic of the GD-SC amplifying cell (right).

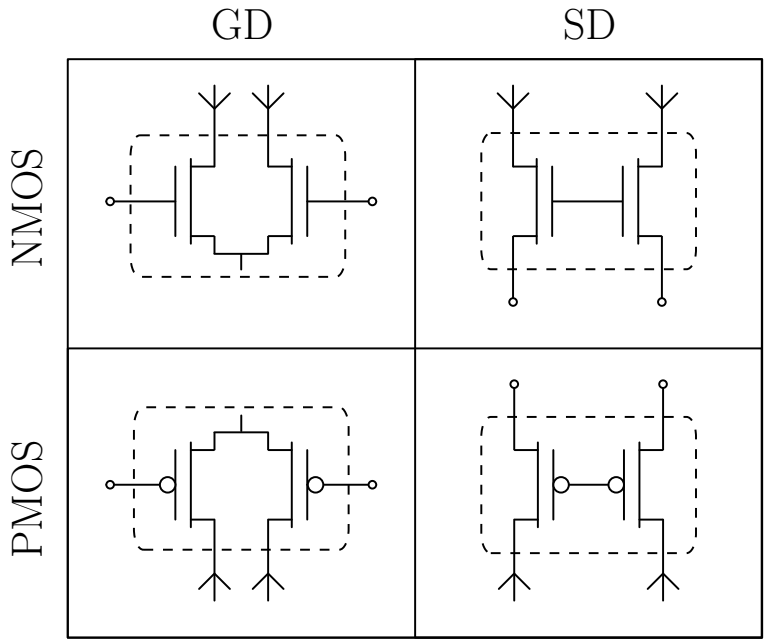

Figure 5. Proposed CMOS elements for Log filtering (auxiliary circuitry not shown for simplification).

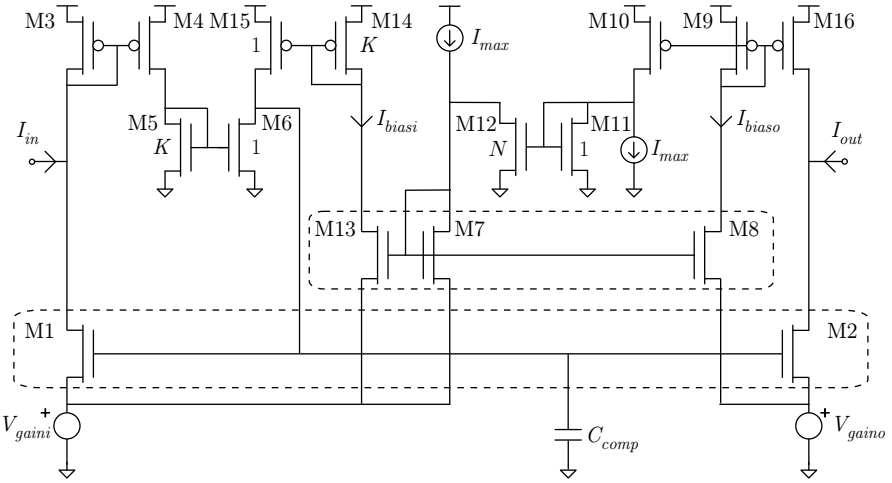

Figure 6. Low-voltage implementation of the controllable amplifier cell.

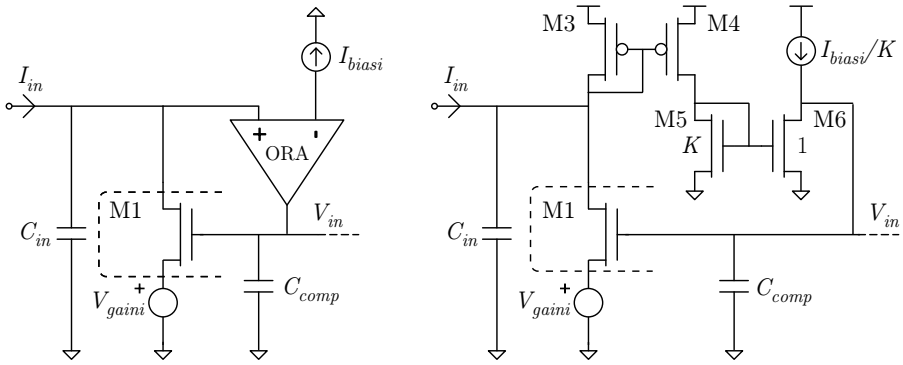

Figure 7. Proposed input impedance control (left) and low-voltage CMOS implementation (right).

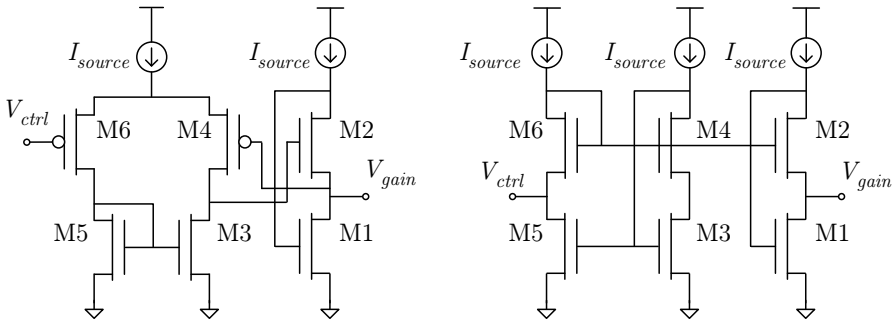

Figure 8. Low-voltage CMOS controlled sources proposed for low technology mismatching (left) and low output noise (right).

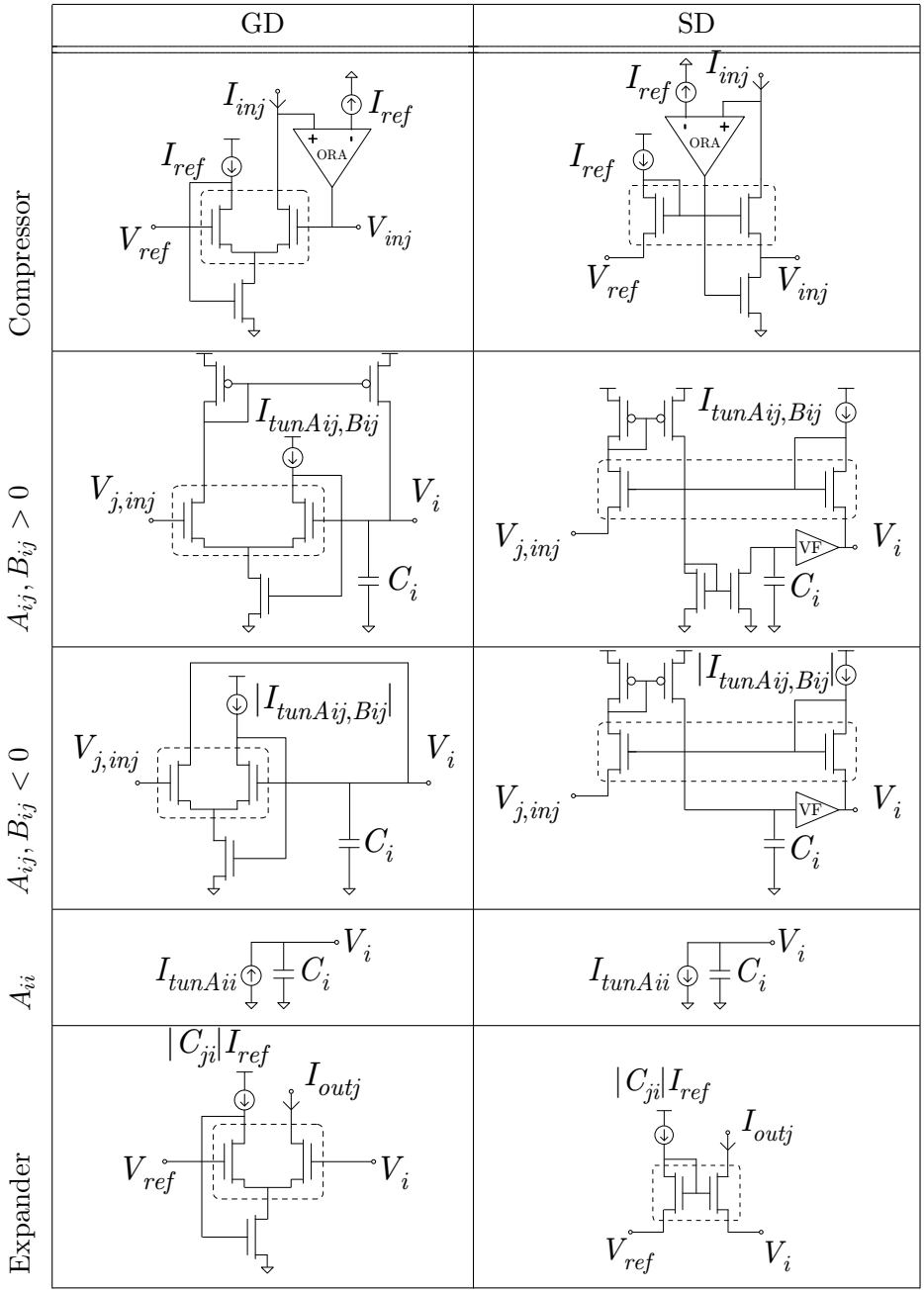

Figure 9. Proposed low-voltage Saturated CMOS cells for Log filtering.

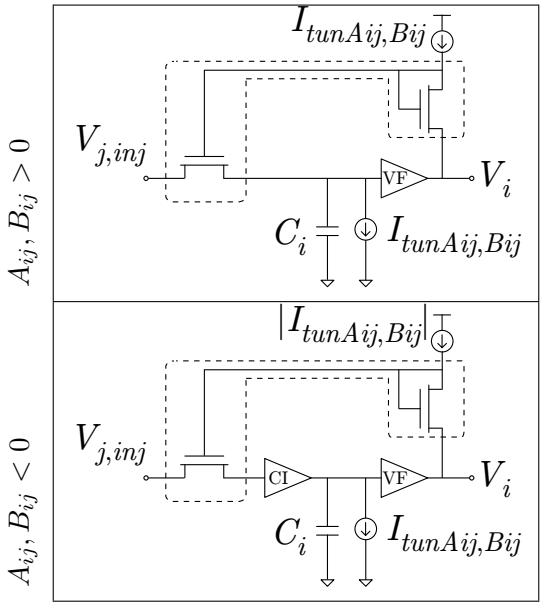

Figure 10. Proposed low-voltage non-saturated CMOS cells for Log filtering.

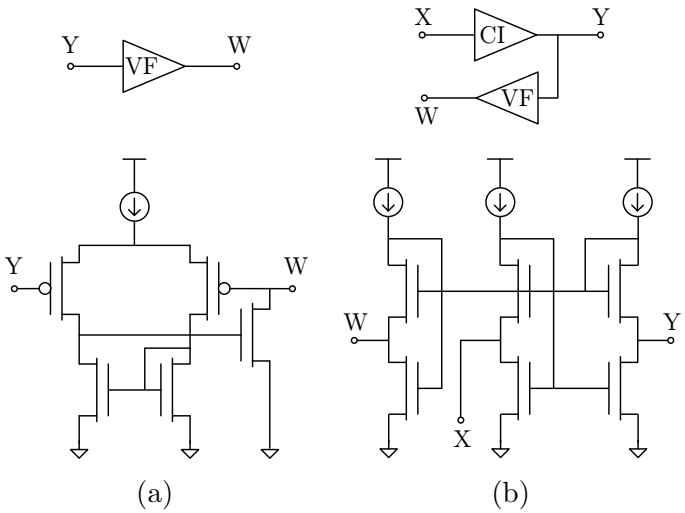

Figure 11. Proposed low-voltage VF (a) and VF+CI (b) blocks.

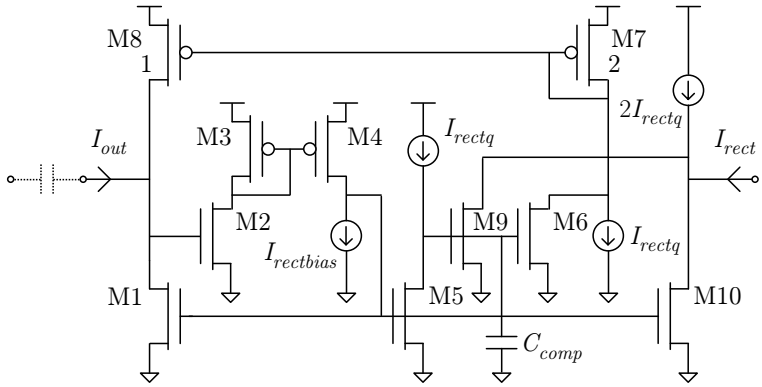

Figure 12. Low-voltage CMOS proposal for precision full-wave rectifying.

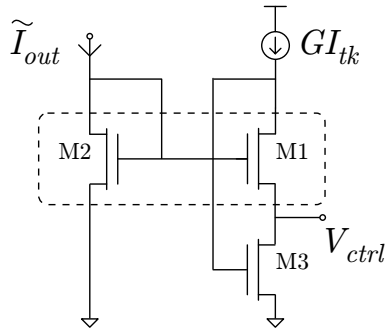

Figure 13. Low-voltage CMOS proposal for the Log ruler.

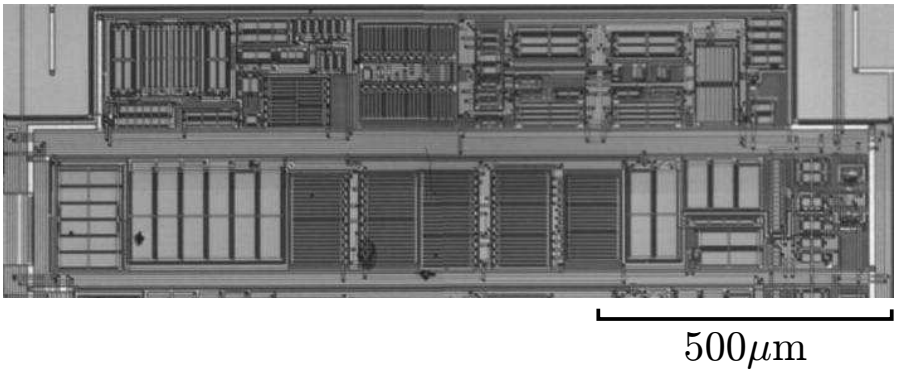

Figure 14. Microphotograph of the AGC example, consisting on a controllable amplifier (lower) and the AGC loop (upper).

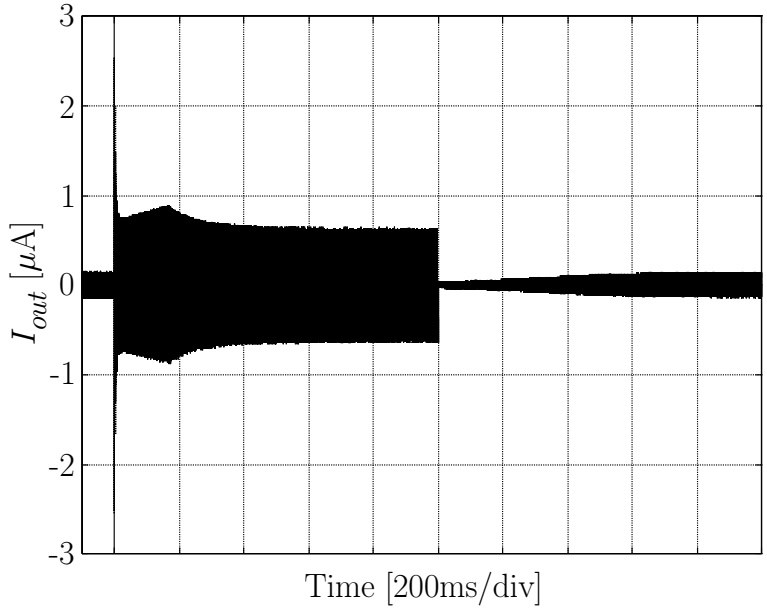

Figure 15. Experimental AGC transient output for a ±25dB input burst.

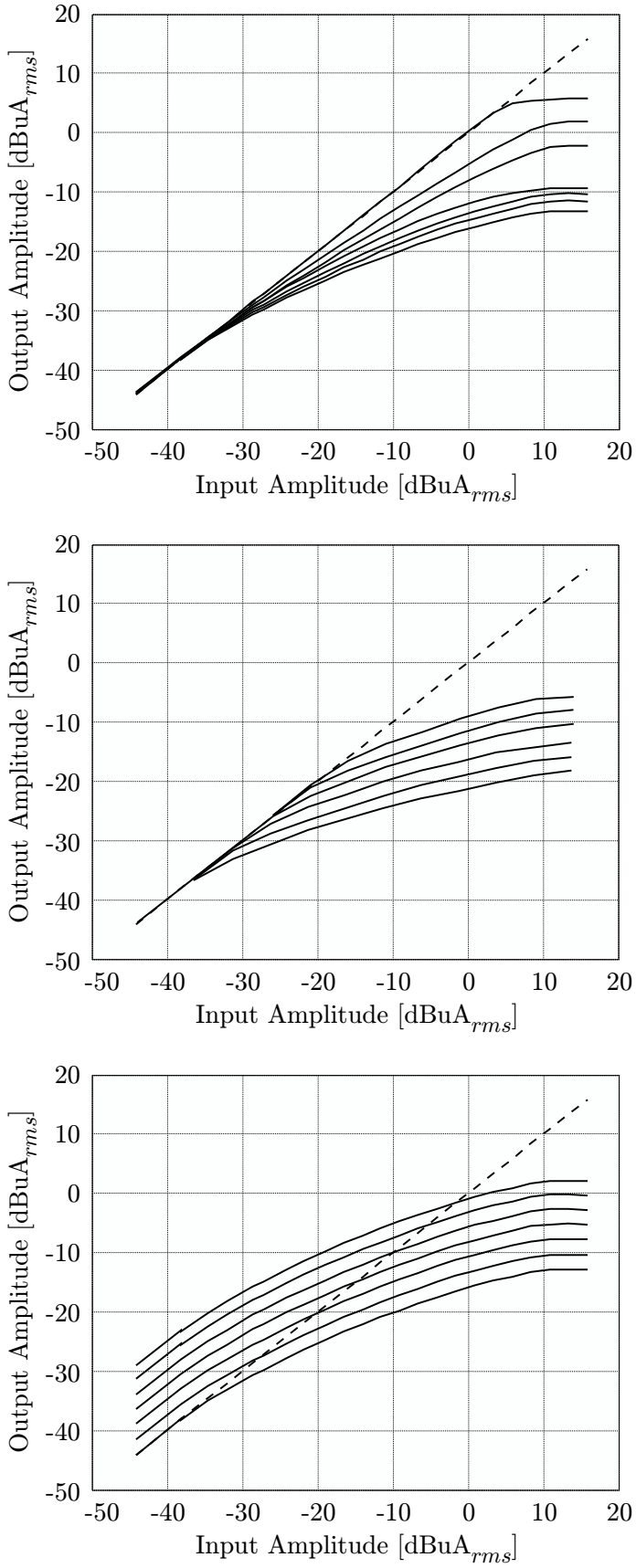

Figure 16. Experimental AGC steady-state input-output response at normalized gain versus compression-ratio (upper), threshold knee-point (middle) and open-loop gain (lower).

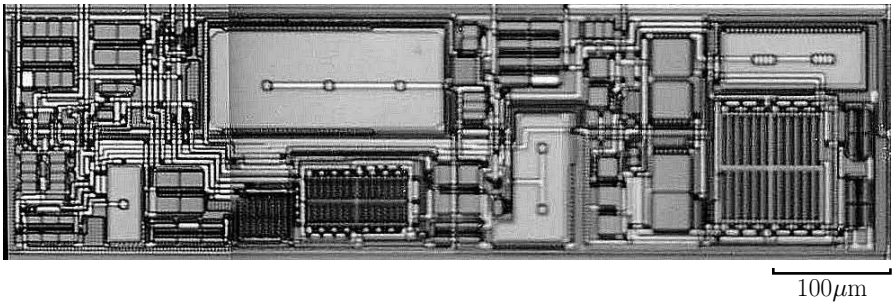

Figure 17. Microphotograph of the Saturated SD filter in a 1.2μm CMOS technology.

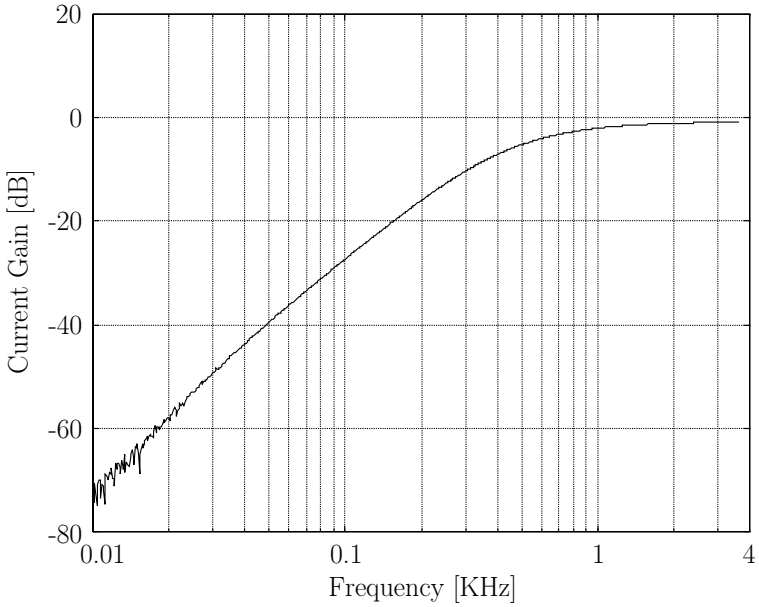

Figure 18. Experimental frequency response of the Saturated SD filter.

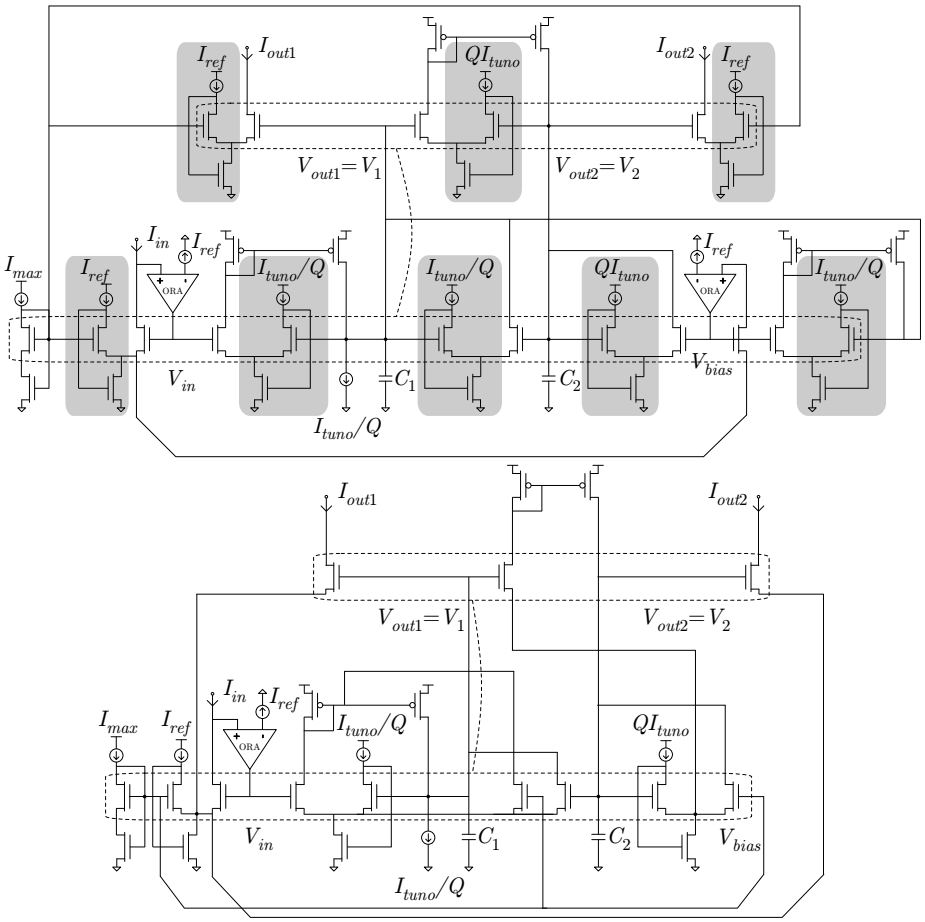

Figure 19. Second-order band/low-pass Saturated GD realization before (upper) and after (lower) circuit reductions.

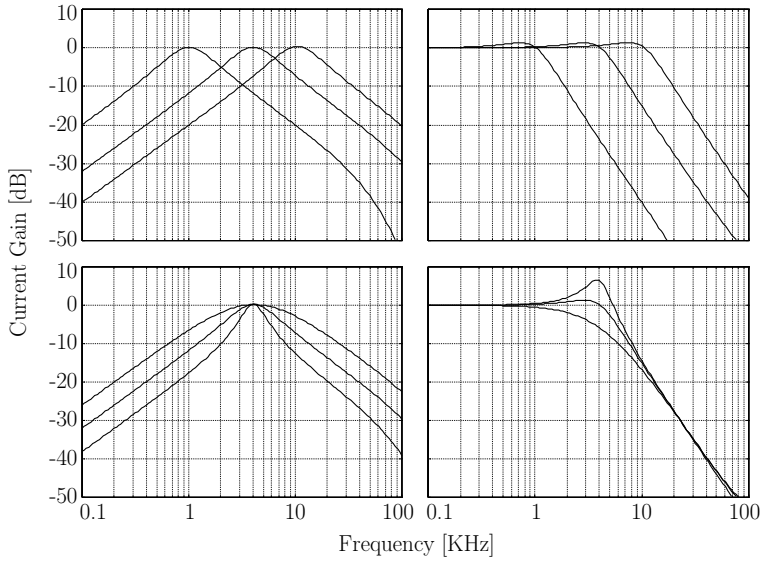

Figure 20. Simulated responses of the band (left) and low-pass (right) Saturated GD filter for $I_{tuno} = \{2.5\text{nA}, 10\text{nA}, 25\text{nA}\}$ (upper) and $Q = \{1/2, 1, 2\}$ (lower) cases.

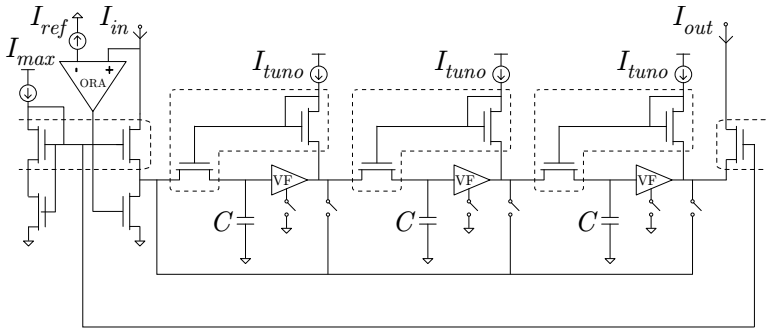

Figure 21. Simplified schematic of the non-saturated SD filter.

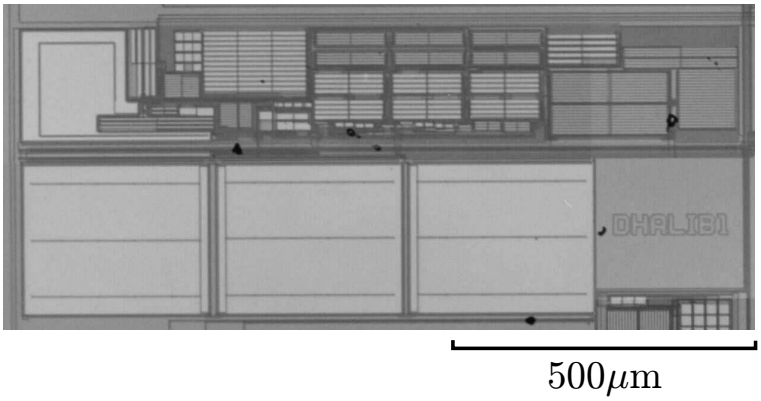

Figure 22. Microphotograph of the non-saturated SD filter in a 0.35μm CMOS technology.

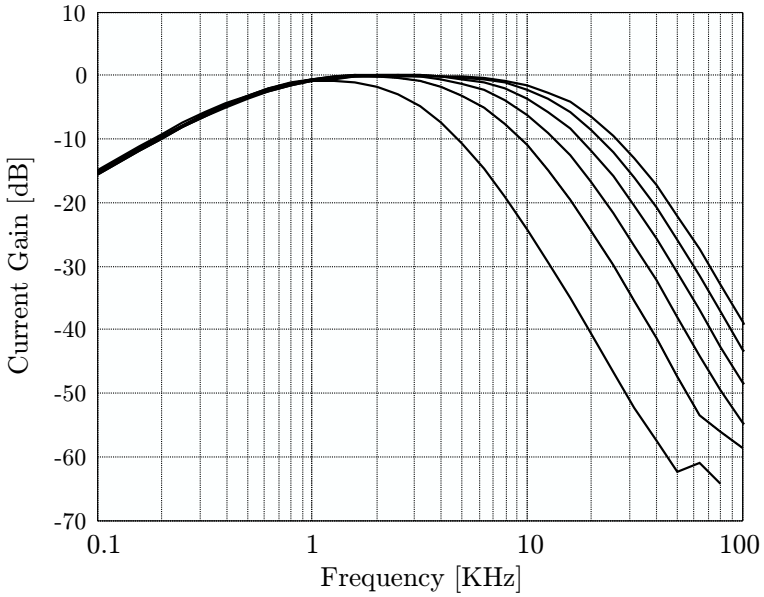

Figure 23. Experimental transfer functions at half-full-scale and 3rd-order selection for different tuning currents. A simple external RC series network has been added at the input of the test setup in order to allow linear V/I conversion, DC decoupling and low-frequency external noise rejection.

Keywords: Low-Voltage, CMOS, Subthreshold, Log, Companding, Audio, Design, Hearing-Aids

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