In-pixel Voltage-Controlled Ring-Oscillator for Phase Interpolation in ToF Image Sensors

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***Abstract*—The design and measurements of a CMOS pseudo-differential voltage-controlled ring-oscillator (VCRO) are presented. It is aimed to act as time interpolator for arrayable picosecond time-to-digital convertors (TDC). This design is incorporated into a 64×64 array of TDCs for time-of-flight (ToF) measurement. It has been fabricated in a 0.18µm standard CMOS technology. Small occupation area of 28×29µm² and low average power consumption of 1.17mW at 850MHz are promising figures for this application field. Embedded phase alignment and instantaneous start-up time are required to minimize the offset of time interval measurements. The measured gain of the VCRO is of 477MHz/V with a frequency tuning range of 53%. Moreover it features a linearity of 99.4% over a wide range of control frequencies, namely from 400MHz to 850MHz. The phase noise is of 102dBc/Hz at 2MHz offset frequency from 850MHz.**

Keywords—phase interpolator; pseudo-differential voltage-controlled ring-oscillator; time-to-digital converter

I. INTRODUCTION

Integrated **V**oltage-**C**ontrolled **R**ing-**O**scillators (VCRO) are among the most important building blocks in modern analog circuits. They constitute the base of complex mixed-signal circuits that require synchronized variable-frequency clock generators. Although they do not have the same performance in term of phase noise as LC-tanks, they still are the most preferred approach from the point of view of versatility, compactness, power dissipation, frequency tuning range, simultaneous multi-phase generation and CMOS compatibility.

One of the most popular circuits based on a VCRO is the phase locked loop (PLL), which is usually employed to synchronize signals or synthesize multiple stable frequencies.

Another field of application of VCROs is the development of CMOS compatible 3D imagers relying on direct **T**ime-**o**f-**F**light (ToF) measurements [1]. Picosecond **T**ime-to-**D**igital **C**onverters (TDC) are used to accurately measure time intervals. The simplest TDC topology could be just a counter. Unfortunately this is not reliable when the time bin goes below 200ps. In this case, the counter has to be driven by a clock reference of at least 5GHz, which becomes a challenge even for the finest technological nodes. The solution to avoid this limitation is to split the conversion in two stages: coarse and fine approximations. The first one is implemented by a counter working at much lower frequency. The second stage employs a thermometric-to-binary decoder fed by the phases of a VCRO. Thus for a particular time bin, the frequency of the reference clock that drives the coarse counter is divided by the number of phases, with respect to the scheme employing one counter alone for direct conversion. For instance 200ps time resolution can be achieved by a single clock of 5GHz or eight phases of 625MHz.

In order to generate an even number of phases for the decoder, both true and pseudo-differential ring oscillators are the most suitable approaches. The latter [2], [3] has some advantages over the former [4]. First, it minimizes the jitter from thermal noise by maximizing the waveform amplitude [5]. Second, it has zero static power consumption.

The output frequency can be controlled by current starved techniques [6], [7] or by acting on the time constant of the delay-cell output [8]. In this work, it is achieved by employing a variable resistor connected on the charging/ discharging path of the delay-cell output node capacitor. Comparing with the current starved technique, the variable resistor implemented with a transmission gate allows full swing between power rails, faster switching and 50% duty cycle over the whole range of output frequencies.

The design of such a circuit becomes more challenging when it is supposed to fit into a pixel-level TDC for direct ToF estimation. In this case the trade-off is on area and power consumption vs. phase interpolation granularity. The first parameter is related to the pixel pitch. The last parameter determines the time bin of the in-pixel TDC.

The contribution of the proposed design merges the advantages of a pseudo-differential scheme with the ones of variable resistor technique based on transmission gates. We achieved the best figures of the aforementioned parameters (see TABLE I.). The design has been fabricated in the UMC 0.180µm CMOS process. The area occupied by the VCRO is 28×29µm². The VCRO has eight interpolation phases at a top measured oscillation frequency of 850MHz. This means the TDC based on this interpolator can reach a time bin of 147ps. The full dynamic range is about 300ns, for an 11b TDC. If the TDC array works at 1000 conversions per second, the average power consumption per VCRO is about 350nW. These features make this work suitable to build arrays of TDCs [9].

This paper is organized as follows: the next section concentrates on the model of the VCRO and the computation of the oscillation frequency. The third section is dedicated to describe the experimental setup and measurements results regarding the gain, linearity, continuous run time average power consumption, simulated phase noise and measured jitter. The last section draws the conclusion of this work.

II. MODEL OF THE VCRO

The proposed scheme is depicted in Fig. 1. The VCRO is a four-stage pseudo-differential ring oscillator with linear wide-range voltage control of the output frequency. As mentioned in the previous section, TDCs are employed to measure time intervals very precisely.

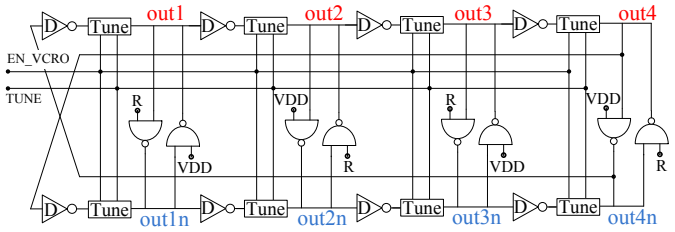


Fig. 1. Voltage-controlled ring-oscillator (VCRO) block diagram

This is done by starting the VCRO on the rising edge of the time interval. The coarse conversion bits are obtained by merely counting the integer number of oscillation periods. Later on the VCRO is frozen on the falling edge of the time interval and the fine conversion bits are recovered by decoding the VCRO phases. The start-up time of the VCRO is speeded up by the positive feedback between each pair of complementary outputs. It must be as short as possible to improve the overall accuracy of the TDC. Moreover, auto-alignment is performed by the reset signal, R, forcing the oscillator to start each time with the same phase.

The novelty of this scheme is the voltage-controlled oscillation capability based on the variable resistance of a transmission gate, represented by the block "Tune" (see Fig. 2a). The selection of the number of stages is a matter of tradeoff between the number of interpolation phases vs. area and power consumption.

The proposed schematic is a nonlinear oscillator. Therefore the accurate analysis by hand is a difficult task. However a first approximation of the oscillation frequency can be computed by combining small signal analysis with large signal considerations [10]. Let us consider $H_n(s)$, with $n = 1, \dots, 4$ being the transfer characteristic of the delay cells presented in Fig. 2. Hence the close loop transfer function is $H_{cl}(s)$:

$$H_{cl}(s) = \frac{H_{op}(s)}{1+H_{op(s)}} \tag{1}$$

Considering that $H_n(s) = H(s), \ \forall\, n = 1, \dots, 4$ the open loop gain, $H_{op}(s)$ is given by:

$$H_{op}(s) = [H(s)]^4 \tag{2}$$

According to Barkhausen criterion, at the oscillation frequency, ω_0, the overall phase shift is 2π and the loop gain is unity [5]. Therefore the following conditions have to be fulfilled:

$$\left|H_{op}(j\omega_0)\right| = 1 \tag{3}$$

$$\varphi(j\omega_0) = \arg\left[H_{op}(j\omega_0)\right] = 4\arg[H(j\omega_0)] = \pi \tag{4}$$

The transfer characteristic of the delay cell can be computed from the equivalent half circuit deployed in Fig. 3.

The transfer function of the delay cell can be expressed as:

$$H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{(g_{mn1}+g_{mp1})Z_{eq}R_o}{R_V+R_o+Z_{eq}} \tag{5}$$

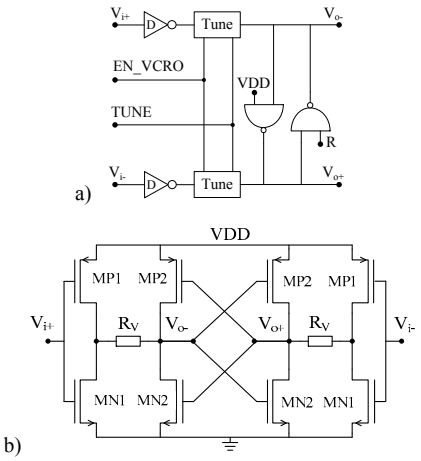


Fig. 2. a) Block diagram of the delay cell; b) Equivalent schematic of the delay cell

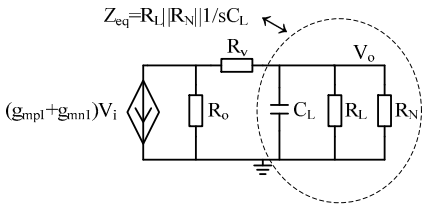


Fig. 3. Half equivalent circuit of the delay cell

where Z_{eq} is:

$$Z_{eq} = \frac{R_N R_L}{sC_L R_N R_L + R_N + R_L} \tag{6}$$

and g_{mn1}, g_{mp1} and R_o are the transconductances and the equivalent output resistance of transistors MN1, MP1. R_V is the variable resistance of the block labeled "Tune" (see Fig. 2a). This resistor is implemented with the help of a transmission gate and has the possibility to be cut off, leaving the terminals floating. In this way, the phases of the oscillator can be frozen at the end of the time interval that has to be measured. R_N is the input resistance of a cross coupled differential pair (see Fig. 2b), which is a negative resistance:

$$R_N = -\frac{1}{g_{mn2}+g_{mp2}} \tag{7}$$

Replacing (7) in (6):

$$Z_{eq} = \frac{R_L}{sC_L R_L - (g_{mn2}+g_{mp2})R_L + 1} \tag{8}$$

and then (8) in (5), $H(s)$ can be written as follows:

$$H(s) = -\frac{(g_{mn1}+g_{mp1})R_o R_L}{R_L + (R_V+R_o)[1-(g_{mn2}+g_{mp2})R_L + sC_L R_L]} \tag{9}$$

Considering (4) and (9) the phase shift condition at the oscillation frequency, f_o can be expressed as:

$$f_o = \frac{1}{2\pi \cdot C_L}\left[\frac{1}{R_L} + \frac{1}{R_V+R_o} - (g_{mn2}+g_{mp2})\right] \tag{10}$$

where the equivalent positive resistance and capacitance in the output node are:

$$R_L = r_{omn2} || r_{omp2} \quad (11)$$

$$C_L = C_G + C_D \quad (12)$$

$$C_G = C_{GS,mn1} + C_{GS,mp1} + C_{GS,mn2} + C_{GS,mp2} + C_{R_V} \quad (13)$$

$$C_{R_V} = C_{GS,n} + C_{GS,p} \quad (14)$$

$$C_D = C_{DG,mn1} + C_{DG,mp1} + C_{DG,mn2} + C_{DG,mp2} \quad (15)$$

C_{R_V} is the gate-source capacitance of the transmission gate transistors. C_G, C_D are the capacitances seen at the gates of the transistors MN1, MP1, MN2, MP2 and their drains, respectively.

According to (10) the design of the cross coupled differential pair is critical for the proper operation of the oscillator. It ensures enough phase shift to oscillate but also it can have an negative effect decreasing the oscillation frequency. Therefore, special care has to be taken to design the positive feedback by controlling the overall gain not to exceed unity. This will minimize the jitter introduced by regenerative switching.

Considering that MN1 and MP1 act as switches, the following assumptions are made:

$$R_o \ll R_V \quad (16)$$

$$\frac{1}{R_V + R_o} \gg \frac{1}{R_L} - (g_{mn2} + g_{mp2}) \quad (17)$$

Under the above circumstances the oscillation frequency is:

$$f_0 \cong \frac{1}{2\pi C_L R_V} \quad (18)$$

III. Measurement Results

The proposed VCRO has been employed in an array of 64×64 TDCs. The analog voltage for the control of the oscillation frequency of the array of VCROs is provided by an on-chip PLL whose core oscillator is a replica of the same VCRO. This global compensation mechanism is meant to mitigate the effect of **P**rocess, **V**oltage supply and **T**emperature (PVT) variations on the time accuracy of the TDCs [11]. The microphotograph of an individual pixel and the layout of the embedded VCRO are depicted in Fig. 4.

The measurements of the VCROs in the TDC array and the one in the PLL are presented further in this section. The measured sensitivity of the oscillation frequency to the control voltage, K_{VCRO} is consistent with the simulated curve (see Fig. 5a). K_{VCRO} computed in both cases is 477MHz/V. The oscillation frequency ranges from 300MHz to 800MHz when the control voltage ranges from 0.67V to 1.7V. The designed VCRO has a very good linearity of 99.4%. As the circuit is also employed as the core oscillator for the PLL, a high gain is required to avoid the PLL loop to unlock.

For PVT global compensation the control voltage of the in-pixel VCROs is provided by the PLL loop filter instead of an external reference. The dependence of the VCRO output frequency on the PLL's frequency division factor ÷N is shown in Fig. 5b. Notice that as long as the PLL is locked, the dependence is linear for a wide range of frequencies from 363MHz up to 765MHz.

The proposed VCRO has been tested also as a building block of the on-chip PLL (Fig. 6). As long as the PLL is locked, the synthesized output frequencies and loop filter output voltage are linearly dependent on the frequency division factor. The frequency range is from 400MHz to 850MHz, with a division factor step of 50MHz. The loop filter output, which is later buffered to the control input of the array of VCROs, ranges from 0.81V to 1.67V.

According to post-layout simulations, the phase noise is 102dBc/Hz at 2MHz from 850MHz. The RMS values of the in-pixel VCROs jitter is measured by running the VCRO continuously for the whole range of control voltages (Fig. 7).

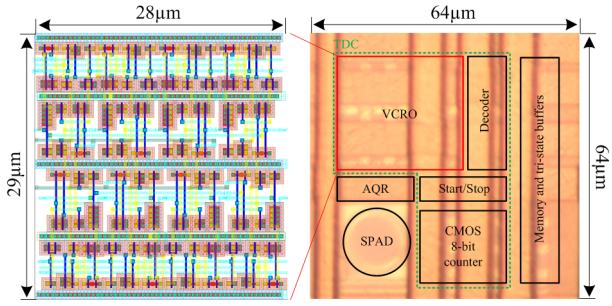
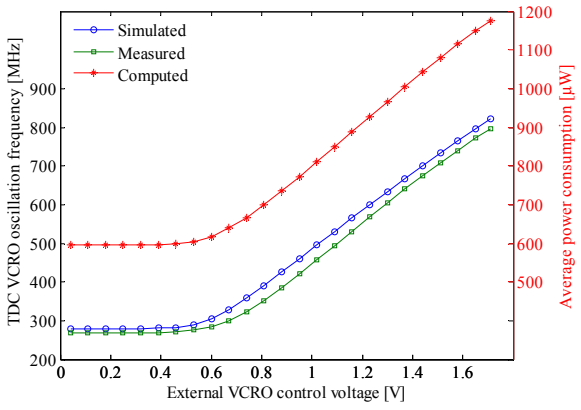
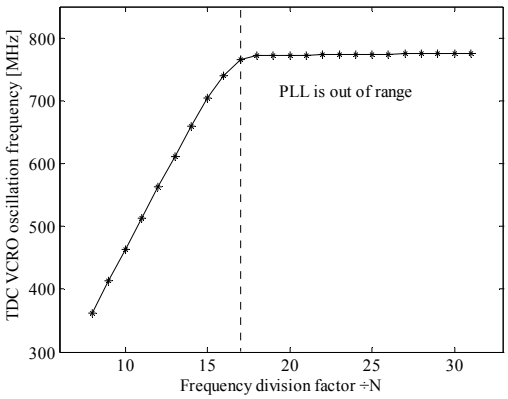


Fig. 4. Layout of the VCRO integrated into the in-pixel TDC



a)



b)

Fig. 5. a) Measured and simulated K_{VCRO} and average power consumption; b) VCRO output frequency vs. PLL division factor ÷N

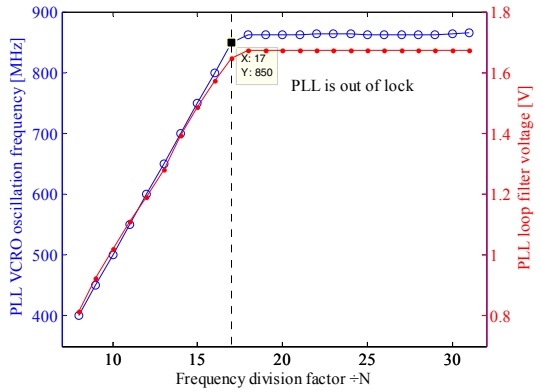


Fig. 6. Measured outputs of the PLL's master VCRO and loop filter vs. ÷N

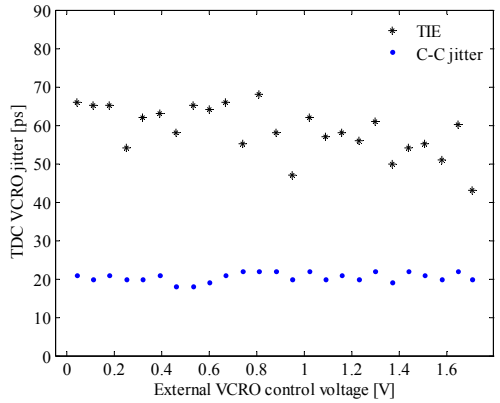


Fig. 7. Measured in-pixel VCRO jitter vs. external control voltage

TABLE I. COMPARISON WITH THE STATE-OF-THE-ART

Performances	**[2]**	**[8]**	**[12]**	**This work**
Technology	TSMC 0.18µm	TSMC 0.18µm	0.35µm	**UMC 0.18µm**
Voltage supply	1.8V	3.3V	3.3V	**1.8V**
Delay cell	Pseudo-differential	Single ended	Diffential	**Pseudo-differential**
Nr. of cells	2	3	4	**4**
Frequency range	440-1595MHz, 72%	16MHz-367MHz, 95.6%	1.07 and 2.06 GHz	**400-850MHz, 53%**
Nr. of phases	4	3	8	**8**
K_{VCO}	825MHz/V	153MHz/V	561MHz/V	**477MHz/V**
Linearity	87.3%	68.6%	-	**99.4%**
Phase noise [dBc/Hz]	-93 @1MHz	-88 @100KHz	-99 @2MHz	**-102 @2MHz**
Area/A_{VCRO}	3.11	1.53	-	**1**
Avg. power	26mW	35.5mW	14.6mW	**1.17mW**

IV. CONCLUSIONS

The design and measurements of a pseudo-differential voltage-controlled ring-oscillator (VCRO) aimed for in-pixel TDC is reported. The proposed VCRO has been tested both as a PLL building block and as a time interpolator for the in-pixel TDC. Comparison with the state-of-the-art is provided in TABLE I. The VCRO pitch of 28×29µm^2 is the best for this technological node. Average power consumption for continuous run time at the highest oscillation frequency is of 1.17mW. It has the best linearity of 99.4% over a wide measured frequencies range from 400MHz up to 850MHz, with K_{VCRO} of 477MHz/V.

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REFERENCES

[1] M. Gersbach, Y. Maruyama, R. Trimananda et al., "A time-resolved, low-noise single-photon image sensor fabricated in deep-submicron CMOS technology", *IEEE Journal of Solid-State Circuits*, Vol. 47, No. 6, pp. 1394-1407, June 2012

[2] Y. Chuang, S. Jang, J. Lee, S. Lee, "A low voltage 900MHz voltage controlled ring oscillator with wide tuning range", *IEEE Asia-Pacific Conference on Circuits and Systems*, Vol. 1, pp. 301-304, 2004

[3] M. Sheu, T. Lin, W. Hsu, "Wide frequency range voltage controlled ring oscillators based on transmission gates", *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, Vol. 3, pp. 2731-2734, 2005

[4] F. Kallel, M. Fakhfakh, M. Loulou, S. Oumansour, M. Sbaa, "Modelling the frequency sensitivity Kvco of a ring oscillator", *15th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2008)*, pp. 794-797, 2008

[5] B. Razavi, *Design of analog integrated circuits*, McGraw-Hill , 2001

[6] N. Retdian, S. Takagi, N. Fujii, "Voltage controlled ring oscillator with wide tuning range and fast voltage swing", *IEEE Asia-Pacific Conference on ASIC*, pp. 201-204, 2002

[7] M. Deen, M. Kazemeini, S. Naseh, "Performance characteristics of an ultra-low power VCO", *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. I-697 – I-700, 2003

[8] N. Gupta, "Voltage-controlled ring oscillator for low phase noise application", *International Journal of Computer Applications*, Vol. 14-No. 5, pp 23-27, 2011

[9] I. Vornicu, R. Carmona-Galán, Á. Rodríguez-Vázquez, "A CMOS 0.18µm 64×64 single photon image sensor with in-pixel 11b time-to-digital converter", *IEEE International Semiconductor Conference (CAS)*, pp. 131-134, October 2014

[10] H. Chen, R. Geiger, "Transfer characterization of CMOS ring voltage controlled oscillators", *44th IEEE Midwest Circuits and Systems (MWSCAS)*, Vol. 1, pp. 66-70, 2001

[11] I. Vornicu, R. Carmona-Galán, Á. Rodríguez-Vázquez, "A SPAD plus TDC array for 145ps-accuracy ToF measurement". *IS&T/SPIE Electronic Imaging: Image Sensors and Imaging Systems, Proceedings of SPIE*, San Francisco, California (USA), Vol. 9403, pp. 94030I.1-6, Feb. 2015

[12] Y. Han, K. Kim, J. Kim, K. Yoon, "A dual band CMOS VCO with a balanced duty cycle buffer", *Current Applied Physics* Vol. 5, No. 3, pp. 277-280, 2005