

AMS/RF-CMOS circuit design for wireless transceivers

Mobile phones have evolved from “simple” devices allowing phone calls over a wireless link to “all-in-one” devices. Besides keeping us always best connected, handheld devices have become true multimedia centers where we can watch movies or our favorite team’s soccer game while making a phone call or chatting over the internet. Hence, in mobile terminals, multi-standard capability is to be supported without compromising performance levels or battery life.

As we move from third generation (3G) to fourth generation (4G) wireless and beyond, and as we strive to meet the demands for higher data rates and short-distance wireless applications, a debate has ensued on whether cellular and WLAN/WiMAX are seen as complementary or competing technologies. In either case, wireless services beyond third generation (B3G) are moving to all- intellectual property (IP), always-best-connected, convergent wireless solutions requiring access to different wireless infrastructures from the same wireless device, be it a cell phone, a laptop or a PDA for a multitude of services, including voice, data and multimedia applications. For future handheld wireless devices, this requires low-power, low-cost, multi-standard, multi-band chipsets, the radio part of which will be increasingly complex with stringent demands on power consumption and cost as the two main differentiators.

Handheld devices have to adapt their operation mode to fulfill the requirements imposed by different bandwidths, data rates, modulation schemes, battery status, etc. The complexity of the wireless environment is escalating due to the proliferation of wireless standards. Furthermore, there are a number of bottlenecks that make the design of wireless transceivers increasingly challenging. These bottlenecks appear mainly in the radio-frequency (RF) and analog and mixed-signal (AMS) sections of transceivers since they do not benefit from the downscaling in nanometer technologies as much as their digital counterparts do.

Nevertheless, advances in both integrated circuit design and process technology, together with the development of novel architectures, new design methodologies and more powerful electronic design automation (EDA) tools, allow designing of increasingly complex wireless transceivers with a sufficiently low power consumption to make sense in handheld applications.

Much of the evolution that wireless transceivers have experienced in the last few years is due to the appearance of CMOS circuits suitable for RF. RF CMOS changed the landscape of radio transceivers completely. Different technologies (GaAs, SiGe, CMOS, etc.) have traditionally been used to meet the requirements of different parts of a wireless system or a chip set (RF front end, digital baseband, etc.). This leads to a high chip count or bill of materials and, therefore, large area and cost. CMOS did not seem like a winner in the RF battlefield due to its inferior RF performance levels with respect to other technologies. However, its ability to make up for its limitations in the analog and RF domains using digital techniques has turned CMOS into the technology of choice in many highly integrated low-cost RF systems such as single chip (radio, baseband and MAC) Bluetooth and Wi-Fi. It led to a shift from systems assembled by using discrete blocks built in different technologies and mostly based on the super heterodyne architecture, to levels of integration that could only be dreamed of several years ago.

Providing a “true single chip” solution is in the interest of area and power save. However, full system-on-chip (SoC), where digital, mixed-signal and RF blocks are integrated, presents serious reliability and yield issues. The level of uncertainty between simulated and fabricated circuits and the limitations of available automated design tools for AMS/RF circuits limit both the probability of first-pass success and the yield in mass production of circuits. In a SoC solution, the low yield of the RF and mixed-signal blocks compromises the yield of the overall system. Moreover, in contrast with their digital counter parts, analog and RF blocks have an extremely large design cycle. With increasingly tight time-to-market requirements and mask sets whose price escalate as technology is down sized, the weeks or even months of delay and increased cost that an extra silicon spin involves might turn out to be unacceptable. IP block reuse is, therefore, vital not only due to the time saving it entails but also due to reliability issues. Including silicon-proven blocks in a new design increases the chances of first-pass success. Auto-calibration techniques, which require in general digital programmability of the blocks, are also key in increasing the yield of integrated solutions as they can compensate for process variations. Applying digital solutions to the analog world such as built-in self-test and smart self-calibration techniques is vital in circumventing the impairments of RF and AMS blocks.

All in all, the design of RF and AMS sections of CMOS transceivers, playing a pivotal role in these communication systems, is a fertile research field where many researchers of both industry and academia are coming up with new, bright ideas to help overcome the above challenges. Along with the related design issues, and making the “right-on-time” and the “first-pass” factors a reality, there is a clear and present need for adequate design methodologies and tools to successfully deal with the many trade-off and key design decisions to be handled all along the design process of RF and AMS transceiver building blocks.

This special issue of Integration, the VLSI Journal is on AMS/RF-CMOS circuit design for wireless transceivers and deals with many of the challenges described above. The papers received were reviewed by outstanding researchers in this field. We are very grateful to them for their hard work and valuable suggestions. The papers selected for this issue are summarized as follows.

First, the paper titled “Input match and load tank digital calibration of an inductively degenerated CMOS LNA” presents a technique for independently tuning the center frequency and quality of the input match for a CMOS low-noise amplifier implemented using the inductive source degenerating topology, a technique that allows for the input match to be centered to the desired frequency in the presence of process shifts and parasitic elements.

Then, in the paper “Anti gone: top-down creation of analog-to-digital converter architectures”, a framework for high-level synthesis of data converters is described. This framework focuses on the translation of a functional description into behavioral models with values for the parameters of its building blocks. The methodology is illustrated with different types of A/D converters.

Subsequently, the paper titled “APLL-based synthesizer for tunable digital clock generation in a continuous-time SD A/D Converter” reports the design and implementation of a tunable clock synthesizer for driving two continuous-time SD ADCs in a 0.35- μm CMOS technology with clock frequencies ranging from 12 to 256MHz with a minimum tuning step of 10kHz. The PLL phase noise is kept below -80 dBc/Hz @ 1MHz offset for the entire output range, while drawing 2.2–5.6mA from a 3.3V supply voltage.

Thereafter, in a paper titled “Reconfigurable multi-mode sigma–delta converter for 4G mobile terminals ”a sigma–delta modulator that is able to support the predictable standards for 4G mobile communication systems, is presented. A key point is that the proposed architecture introduces the ability to process two different signals concurrently.

After that, in the paper “A mixed-signal demodulator for a low-complexity IR-UWB receiver: methodology, simulation and design” an integrated 0.18mm CMOS 2-PPM demodulator based on a switched capacitor network for an energy detection impulse-radio UWB receiver is described. The circuit has been designed using a top-down methodology that allows discovering the impact to flow-level non-idealities on system-level performance. This demodulator consumes 190pJ/bit at 1.8V.

Then, in “Nyquist-criterion based design of a CT sigma–delta- ADC with a reduced number of comparators ”a prototype continuous-time sigma–delta modulator in a 0.35 mm technology with a six-bit internal quantizer, realized with only 15 comparators, is presented. The presented design has two particular features. First, an explicit and controlled delay of 0.25 times the sampling period is introduced in the loop. Second, the Nyquist stability criterion and the vector gain margin are adopted to design a robustly stable modulator loop filter. Measurement results show a peak SNR of 82 dB and a dynamic range of 85 dB for a band width of 1.5 MHz.

Thereafter, in the paper titled “A low-power two-GHz data conversion using delta modulation for portable application ”a new band pass delta modulator dedicated to low-power and portable applications is reported. The proposed modulator can convert a wide frequency range of 500 MHz–2.6 GHz into an IF as low as 20 MHz by using under-sampling (with total power consumption of 37.2 mW when the voltage supply is 1.2 V). Simulation and experimental results obtained using the CMOS 0.13 mm IBM technology are presented and discussed.

The next contribution, in the paper “A fully integrated 23.2 dBm P1dB CMOS power amplifier for the IEEE 802.11a with 29% PAE”, reports the design of a two-stage fully integrated PA targeting IEEE 802.11a. Reported measurement results of this PA, implemented in a differential cascade mode, show a power gain of 21.1 dB, a P1dB of 23.2 dBm, a PAE of 29% and a 6.2 dBm OFDM output power at 54 Mbit/s.

After that, the paper “A1-VRF-CMOS LNA design utilizing the technique of capacitive feedback matching network” proposes a new LNA structure using an input matching topology based on a capacitive feedback matching network. This LNA has been implemented in a 0.18 μm CMOS technology, achieving again of 13.2dB at 12.8GHz with a noise figure of 4.57dB.

In the paper titled “Third order nonlinearity vs. load impedance for CMOS low noise amplifiers”, a low-frequency linearity estimation method valid for weakly non-linear amplifiers is presented. This method is based on extracting the Taylor expansion coefficients from DC I–V simulations. Two identical LNAs with different load impedances fabricated in a 90nm CMOS process have been used as a basis for comparison. The reported linearity estimations correlate well with the measurement results even though the center frequencies of the amplifiers areas high as 15 and 20GHz.

Last but not the least, the paper titled “Predictive test strategy for CMOS RF mixers” introduces two predictive test strategies for the down converter stage in a GSM receiver. These BiST strategies use test observables that significantly ease the measurements in test mode while keeping accuracy better than 2% when predicting the conversion gain and 1dB compression point rms as compared to the measured values.

R. Castro-López

D. Rodríguez de Llera

M. Ismail

F.V. Fernández