A Front-End ASIC for a 3-D Magnetometer for Space Applications by Using Anisotropic Magnetoresistors

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This paper presents an ASIC aimed for an alternative design of a digital 3D magnetometer for space applications, with a significant reduction in mass and volume while maintaining a high sensitivity. The proposed system uses magnetic field sensors based on anisotropic magnetoresistances (AMR) and a rad-hard mixed-signal ASIC designed in a standard 0.35 µm CMOS technology. The ASIC performs sensor-signal conditioning and analogue-to-digital conversion, and handles calibration tasks, system configuration and communication with the outside. The proposed system provides high sensitivity to low magnetic fields, down to 3 nT, while offering a small and reliable solution under extreme environmental conditions in terms of radiation and temperature.

***Index Terms*—Magnetometer, anisotropic magnetoresistance, CMOS mixed-signal ASIC, RHBD, aerospace electronics.**

I. Introduction

Fluxgate sensors have been traditionally used in space applications as magnetic field sensors because they offer a good performance in terms of accuracy and robustness in a relatively small and lightweight device [1]. However, the current trend of aerospace technology, which goes to the design of small-sized satellites to reduce costs, implies that the use of this type of magnetic field sensors is generally unaffordable due to its volume and weight [2]. The use of application-specific integrated circuits (ASICs) instead of discrete electronics [3]-[4] provides significant reductions in weight, volume, and power consumption, while maintaining the performance [5].

This paper presents the design of a 3D magnetometer for space applications based on anisotropic magnetoresistances (AMR) and a radiation hardened by design (RHBD) mixed-signal ASIC designed in a standard 0.35 µm CMOS technology to perform sensor conditioning, data acquisition, and calibration and communication tasks.

The proposed system has been developed in the frame of Mars MetNet mission. The objective is the measurement of the magnetic field at the Martian surface with a resolution of 3 nT in a field range of ±6.5 µT [6]. The field range has been extended up to ±100 µT to increase the functionality for future applications and/or field measurements on Earth. The expected extreme environmental conditions cover extended temperature range (from -90 ºC to +125 ºC) and radiation effects, which include long-term effects due to total dose (up to 318 krad) and single-event effects (SEEs) due to the impact of high-energy particles (mainly protons, but also heavy ions).

Section 2 describes the proposed system, disclosing its main design aspects. Experimental results about the performance and robustness of the ASIC are reported in Section 3, while Section 4 presents the conclusions.

II. System Description of the Magnetometer

Fig. 1 shows a simplified block diagram of the proposed 3D digital magnetometer. The magnetic field sensors considered belong to the HMC-1001/2 family from Honeywell Inc. These sensors are based on anisotropic magnetoresistances in a Wheatstone bridge configuration [7]. Three of these sensors are placed in orthogonal directions for 3D measurements. The resolution of these sensors is 3 nT and the field range is ±200 µT, which are under the requirements (3 nT, ±100 µT).

The ASIC provides the front-end electronics for the AMR sensors. It has been designed with a high level of configurability in terms of resolution and conversion rate, in order to be usable for different applications. It contains six conversion channels for precise sensor measurements, a four-channel single-slope ADC (SS ADC) for thermal calibration,

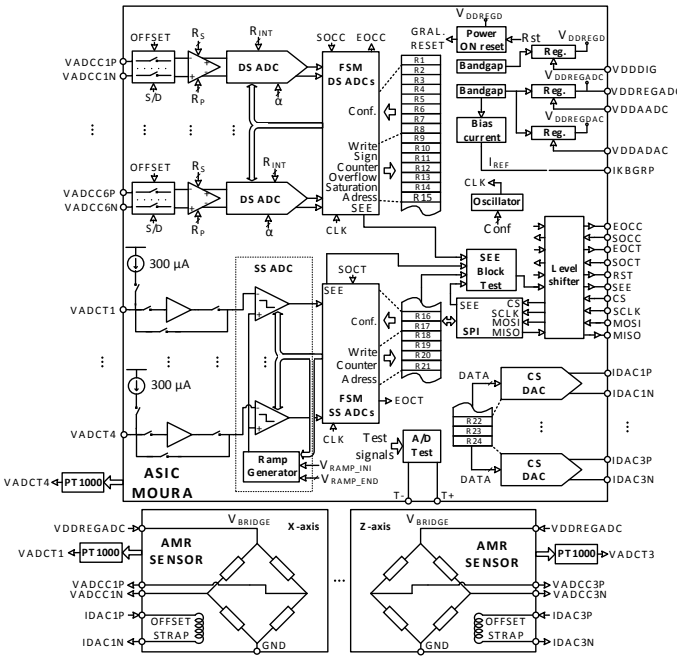

Fig. 1. Simplified block diagram of the proposed magnetometer.

and three current-steering DACs (CS DACs) for sensor conditioning. The digital output values and all the configuration options are stored in an internal memory map. The ASIC provides access to this memory map using a serial protocol interface (SPI). A configurable internal clock with a frequency up to 100 MHz controls the operation of the whole system.

A. AMR Sensor Measurements

Three of the six available channels are used to measure the AMR sensors, while the other three can be used for additional applications, like the measurement of gravitational orientation or others. The bias voltage of the bridge (3 V) is generated internally in the ASIC, in order to eliminate its influence in the relationship between magnetic field and digital code. As shown in Fig. 2, each conversion channel consists of a preamplifier and a dual-slope ADC (DS ADC).

The preamplifier performs sensor-signal conditioning functions. It limits the noise bandwidth of the sensor signal and provides programmable gain, high common-mode rejection and capacitive input impedance. It is implemented using a fully-differential instrumentation amplifier. The voltage gain G is configurable between 1 and 1000 by means of two programmable resistors R_S and R_P:

$$G = 1 + \frac{2 \cdot R_S}{R_P} \tag{1}$$

The DS ADC performs the analogue-to-digital conversion. It is implemented with an integrator and a comparator. This architecture provides high levels of accuracy, noise rejection and insensitivity to the precise value of their components. Its analogue and digital sections are simple, and do not require post-processing. This simplicity and robustness are important factors for space use, considering the extreme temperature ranges and the effects of radiation [8].

In order to meet the resolution requirements of 3 nT in a field range of ±100 μT, the maximum resolution of the DS ADC is 16 bits (15 bits plus sign) at 2.6 kS/s. The equivalent LSB at the preamplifier output (ADC input) is 60 μV, for a differential input range of ±2 V. Faster measurements can be achieved up to 20 kS/s at 12 bits.

The time constant of the integrator is programmable by setting R_{INT}, as required to exploit the full output signal swing under different resolution and speed configurations, while avoiding saturation. The value of the integration capacitor is 40 pF while the resistor can be set from 515 kΩ to 4.096 MΩ. The comparator, which must operate at the clock frequency, uses a regenerative latched approach with a preamplifier stage to mitigate the effective offset voltage and reduce the kickback effect. The relationship between the differential output voltage from the AMR sensor (V_{IN}) and the output code is given by:

$$N_{OUT} = sign(V_{IN}) \cdot \left| \frac{G \cdot V_{IN} \cdot N_{C1}}{\alpha \cdot V_{REF}} \right| \tag{2}$$

where N_{C1} is the duration of the first integration stage in clock cycles and $\alpha \cdot V_{REF}$ is the programmed internal reference voltage for the second integration stage. It is scaled from a general reference (V_{REF} = ±2 V) by a configurable factor α, yielding effective reference levels between ±250 mV and ±2 V with steps of 250 mV. The resolution is determined by setting the number of cycles of duration of the second integration stage (N_{C2} in Fig. 2). The relationship in (2) is independent of the clock frequency and the time constant of the integrator, providing high levels of insensitivity to their fluctuations. The resolution, expressed as 1 LSB of equivalent AMR sensor voltage, is:

$$LSB = \frac{|\alpha \cdot V_{REF}|}{G \cdot N_{C1}} \tag{3}$$

The programmability of N_{C1}, N_{C2}, f_{CLK}, R_{INT}, α and G makes the conversion channel very adaptable in terms of resolution, conversion rate, and input voltage range. Although not shown in Fig. 2, two voltage-level comparators monitor the operation of the integrator, alerting if the integrator saturates. The controlling finite-state machine (FSM) also alerts if there is an overflow in the count of the counter during the second integration stage. This not only alerts from malfunction, but also allows, in conjunction with the configurable gain of the preamplifier, a straightforward implementation of auto-ranging techniques. A specific operation mode is also included in order to perform offset measurements of the full conversion channel.

B. Temperature Measurements for Thermal Calibration

The sensitivity of the AMR sensors has a significant drift with temperature. Several approaches have been reported in order to improve the stability [9]-[10], but there is still a temperature dependence that becomes critical when measuring weak magnetic fields in environments with an extended operating temperature range. The effect of temperature in the sensitivity is linear [7], [11] and can be easily calibrated. Four MiniSens PT1000 are used as temperature sensors to monitor the temperature of the ASIC and the three AMR sensors.

A four-channel SS ADC is used to perform the analogue-to-digital conversion from the temperature sensors. The SS ADC consists of a ramp generator that is shared by four self-biased comparators in a parallel readout architecture, as shown in Fig. 3. An integrator driven by an NMOS transistor, acting as a voltage-controlled current source, implements the ramp generator. The generation of the ramp is controlled by a

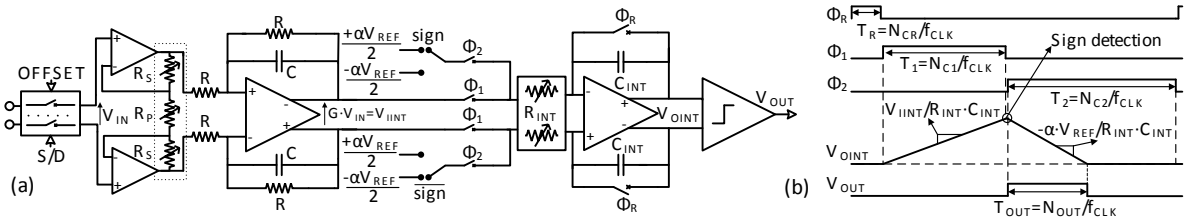

Fig. 2. Measurement system for the AMR sensors. (a) Simplified circuit schematic. (b) Timing diagram of the conversion cycle.

feedback loop comprised by a capacitor (C_F) and two pairs of switches [12]. The feedback loop locks the end value of the ramp, to the reference voltage (V_{REF_LAST}), by regulating the input voltage of the current source. Few cycles of adaption are needed until the ramp is fully adapted. The adaptive nature of the ramp generation makes it insensitive to any possible source of variations, except for the reference voltages defining the ramp excursions, which are obtained from an internal bandgap circuit. The resolution of the SS ADC is configurable between 10 bits at 77 kS/s and 15 bits at 3 kS/s. The input range is configurable with values between 0 and 2.8 V.

C. AMR Sensor Conditioning with Feedback Currents

The AMR sensors from Honeywell Inc. include an on-chip coil, called OFFSET strap, which can be used to generate a magnetic field in the sensitive direction [7]. The proposed magnetometer makes use of this strap as a negative feedback element in a closed loop configuration, by driving controlled currents to generate a magnetic field that cancels the external magnetic field to be measured, keeping the sensor in a close-to-zero field condition in order to improve the sensitivity, linearity and temperature characteristics.

These currents are generated using 3 monotonic binary-weighted CS DACs, as shown in Fig. 4. The resolution is 9 bits (8 bits plus sign) with a full-scale current of ±25 mA. The CS DACs are driven with the 9 most significant bits (8 bits plus the opposite sign) of the measurements performed by the DS ADCs. The linearity error of the CS DACs must only be below $2^7 \cdot$LSB, as the linearity of the 7 least significant bits is ensured by the measurements of the DS ADCs.

Additionally, the CS DACs can be used for offset disturbing magnetic field cancellation as well as other calibration functions. It is possible to check several parameters of the static transfer characteristic by applying a controlled ramp current through the OFFSET straps.

D. RHBD Techniques

AMR sensors have been proven to be inherently robust to radiation [11]. The design of this ASIC for space applications builds on previous work oriented to the characterization of radiation and low temperature effects on the selected standard CMOS process [13]. Specific RHBD techniques have been employed in this ASIC. This includes the use of ringed-source layouts for every NMOS transistor, for total ionizing dose (TID) effects improvements [14]. PMOS devices use a standard layout. Concerning single-event effects (SEEs), complete guard-rings have been used around every transistor.

All the storage elements are redundant and have a specific single-event upset (SEU) flag to alert of this eventuality through a global output pin. The FSMs are reset at the beginning of every conversion cycle, restoring it from any eventual error during the previous conversion. In addition, one-hot encoding has been used to implement the FSMs and the SPI interface.

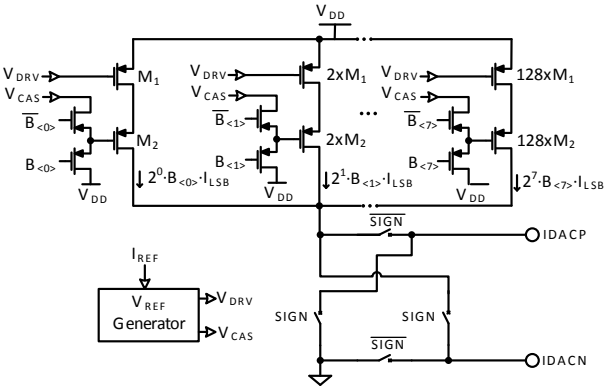

Fig. 4. Simplified circuit of the CS DAC for the AMR sensor conditioning.

III. Experimental Results

The ASIC has been fabricated in a 0.35 µm CMOS technology from Austria Microsystems (AMS). Fig. 5 shows its die photograph. The chip has a total area of 4.5 mm x 4.5 mm. The maximum power consumption of each individual DS ADC channel is 13.2 mW, and the four-channel SS ADC power consumption is 7.8 mW. Table I shows the experimental performance of the DS ADCs at room temperature, with G = 1, and with a clock frequency of 100 MHz and maximum input voltage range. The SS ADC has been tested in the same conditions, showing a monotonic transfer characteristic, a noise floor of 150 µV (rms) and a maximum non-linearity error of 0.02% of full-scale. The CS DACs are monotonic, with a non-linearity error below 0.3% of full-scale.

The performance against TID effects has been verified with irradiation tests using a Co-60 gamma-ray source in the facilities of the Centro Nacional de Aceleradores (CNA-CSIC,

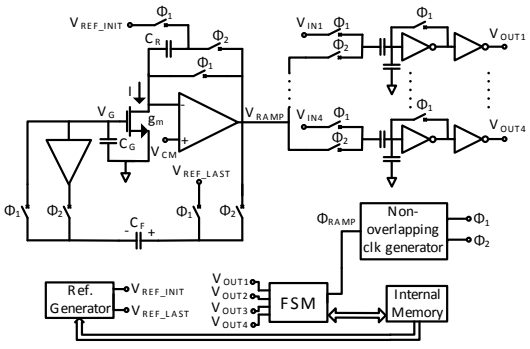

Fig. 3. Simplified circuit schematic for temperature measurements.

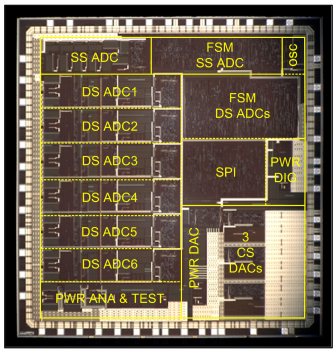

Fig. 5. Die photograph of the fabricated ASIC.

Spain), reaching a total dose of 318 krad. The results show very high levels of robustness. As an example, Fig. 6 shows the minor deviations of the integral non-linearity (INL) error of the DS ADCs at different TID levels, under the same conditions of Table I, at 16 bits.

SEE tests have been performed using the heavy–ion cyclotron facilities of Université Catholique de Louvain-la-Neuve. The resulting linear-energy transfer threshold (LET_{th}) for SEUs is 16.5 MeV·cm^2/mg. No latchup events were observed up to the maximum energy available from the facility: 80.8 MeV·cm^2/mg. For a geostationary orbit at the maximum of cosmic rays flux, the estimated SEU error rate is of $2.1 \cdot 10^{-5}$/day for each DS ADC conversion channel, and $3.4 \cdot 10^{-5}$/day for each channel of the SS ADC.

Temperature tests from -25ºC to +125ºC have shown no significant effect with respect to the results reported in Table I. The SS ADC, used to perform the thermal calibration, has shown high levels of temperature stability. Fig. 7 shows the percentage deviation of the slope of the transfer characteristic against temperature with respect to the nominal case at 25 ºC. The percentage deviation of the internal bandgap voltage is also shown. The total deviation is less than 0.8 % and correlates with the variation of the bandgap. According to previous characterization of individual electronic components in the CMOS process [13], the performance for temperatures down to -90ºC is expected to be correct as well.

TABLE I
EXPERIMENTAL PERFORMANCE SUMMARY OF THE DS ADCS

Resolution (bits)	12	13	14	15	16
Conv. time (µs)	51	72	112	194	378
INL	+0.065	+0.20	+0.55	+0.71	+0.86
	-0.054	-0.14	-0.31	-0.49	-1.1
DNL	+0.12	+0.14	+0.24	+0.35	+0.38
	-0.11	-0.17	-0.22	-0.25	-0.37
Root-mean-square noise	0.00	0.03	0.49	0.51	0.86

Results for INL, DNL and rms noise are in LSBs

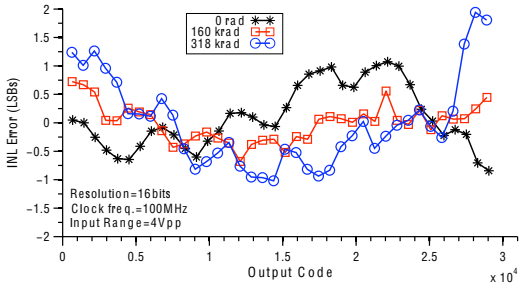

Fig. 6. DS ADCs INL error under TID effects.

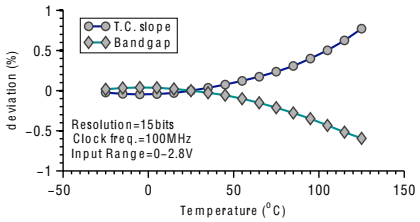

Fig. 7. Transfer characteristic slope deviation of the SS ADC with Tª.

IV. CONCLUSIONS

A digital magnetometer for space applications has been presented, achieving improvements in mass and volume while maintaining a high sensitivity. Experimental results show that its performance is highly insensitive to the effects of radiation. In addition, the designed ASIC incorporates precise thermal monitoring, calibration and sensor conditioning functions to be applied during operation in order to maximize the performance of the AMR sensors in an extended operating temperature range.

ACKNOWLEDGMENT

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