1.2V, 1.96mW @ 2.4GHz CMOS-90nm Switched-Transconductor Mixer

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***Abstract*—This paper presents the design of a fully differential double balanced switched transconductor mixer for ZigBee applications in the 2.4GHz band. It provides programmable conversion gain by using an active load stage. The design includes RF and LO input matching networks. It has been implemented in a 90nm 1P9M CMOS process. Post-layout simulations show conversion gains of 12dB/20dB, NF of 18.9dB/18.1dB and power consumption of 4.1mW/4.4mW at high and low gain mode respectively from a 1.2V power supply. It also offers very good linearity performance.**

I. INTRODUCTION

Mixers are one of the main blocks in RF systems performing the necessary frequency translation. The Gilbert-type mixer has been widely used because of its advantages in terms of gain, noise, port-to-port isolation, linearity, etc [1]. However, it has important limitations in other aspects that make them not suitable for LV-LP applications. Among other issues, the Gilbert Cell requires stacked transistors operating in the saturation region and large LO (Local Oscillator) swings. These aspects limit the required voltage supply, power consumption and output swing. Several techniques have been proposed to overcome such limitations [2]–[4]. For example, the folded structured method [2] reduces the number of stacked transistors allowing lower supply voltages. However, because this method requires more current to flow, power consumption is similar to the conventional Gilbert structure. In [3], low voltage operation using an LC tank is reported; large output swing is achieved at the cost of large are overhead.

The switched transconductor mixer topology [6] has been proposed as an alternative to the Gilbert one. They have similar performance in terms of conversion gain and linearity. However, the switched transconductor mixer achieves lower noise figure at high LO frequencies and allows lower voltage operation.

In this paper, a low voltage low power fully differential double balanced mixer with programmable gain is presented. It is intended for ZigBee applications in the 2.4GHz band [5]. Low-Voltage and Low Power operation are achieved by exploiting switches connected to the supply voltage and RF transistors in the weak inversion. On the other hand, the fully differential and double balanced topology guarantees good port isolation and linearity.

The paper is organized as follows. Section II reviews briefly the basis of the switched transconductor mixer. Section III describes the design of the proposed mixer intended for ZigBee applications in the 2.4GHz band. Section IV shows experimental results from the extracted layout. Finally, some conclusions are given in Section V.

II. SWITCHED TRANSCONDUCTOR MIXER

Figure 1 shows the simplified scheme of the mixer core. Two NMOS differential pairs biased at voltage V_B act as transconductors (represented with transconductances g_{m1} and g_{m2} in the figure). Two anti-phase driven CMOS inverters are used to turn on/off the corresponding transconductor accordingly to the anti-phase LO and XLO signals. Notice that the scheme is suitable for low voltage operation while large output swing can be achieved because stacked transistors are avoided.

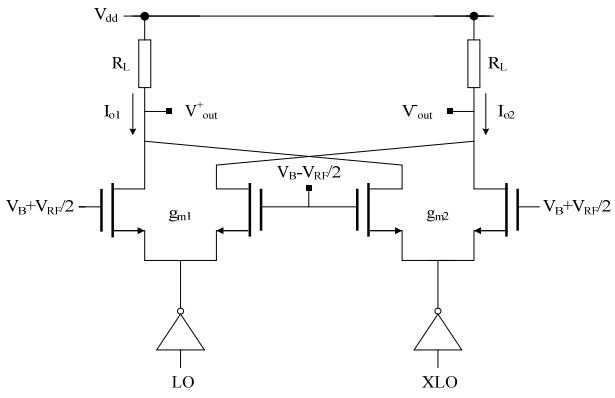

Figure 1. Double balanced switching-transconductor mixer

Assuming matched transconductors and instantaneous ideal switching, g_{m1}/g_{m2} is on/off or off/on. Thus, either I_{o1} or I_{o2} is equal to $I_B+g_mV_{RF}$ (where I_B is the current through the on transistors and g_m their equivalent transconductance at the bias point) and the other current is zero, just as in the Gilbert mixer. So, the differential conversion gain can then be expressed as,

$$GC \approx \frac{2}{\pi} \quad g_m \quad R_L \tag{1}$$

In terms of thermal noise, the contribution of the transconductance devices is roughly the same as in the Gilbert mixer topology at equal conversion transconductance. This makes sense, as either g_{m1} or g_{m2} is active, alternately producing (uncorrelated) thermal noise with a variance proportional to g_m. However, there is a significant difference if we consider the noise contribution of the switch devices (inverters). In the proposed topology, the noise current generated by the switches is in common mode, because the two MOS transistors from one transconductor pair are working at the same state. Then the noise is expected to be cancelled by the differential outputs. The approximate SSB NF (Single Side Band Noise Figure) is given aprox. by [6],

$$NF_{SSB} = \frac{\alpha}{c^2} + \frac{2(\gamma + r_g \quad g_m) \quad g_m\alpha + \frac{1}{R_L}}{c^2 g_m{}^2 R_s} \tag{2}$$

where the α and c are LO related parameters, γ, r_g and g_m denote the noise factor, gate resistance and transconductance respectively and R_s is the resistance of the signal source used for noise figure evaluation (usually 50Ω).

III. THE PROPOSED MIXER DESIGN

In this section, the design of a mixer based on the scheme in Figure 1 and intended for ZigBee applications in the 2.4GHz band using a 90nm CMOS technology and 1.2V of voltage supply is described. An intermediate frequency f_{IF} equal to 2.5MHz has been chosen as a good compromise between image rejection requirements and channel selection filter specifications (cut-off frequency and selectivity). In order to maximize the transferred signal from the balun to the circuit, the mixer should have 50 Ω input single ended impedance. An RLC network has been used. In this configuration, the resistance R_g generates the real part, inductor L_g and the capacitor C_{gs} form a tank resonating at 2.4GHz. Figure 7 shows the S_{11} curve of the mixer. The input return loss is below -20 dB@2.4GHz.

Figure 2 shows the schematic of the proposed mixer including input matching networks at LO and RF ports. The switching inverters are composed by transistors M1-M_4 and the RF transconductance stages by M_5-M_8. The output load corresponds to a common mode feedback structure composed by resistors R_L, transistors M_9-M_{10} and the current source I_b, that is used to set the common mode voltage. Power consumption is directly related to the size and bias voltage of the transconductance transistors (M_5-M_8). From this point of view, it is desired to keep them in weak inversion. This way, large output swing can also be achieved even for low voltage supply. On the other hand, the W/L ratio of such transistors should be large in order to obtain high conversion gain. These circumstances are desirable from the power point of view, but this is not the case for thermal noise [7].

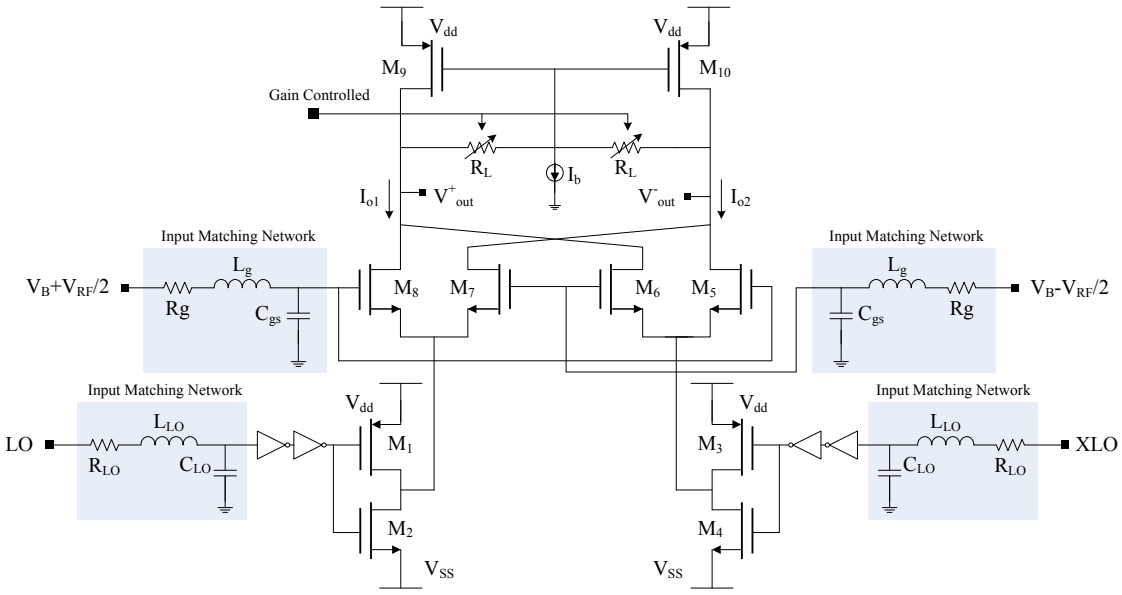

Figure 2. Double balanced switched implemented transconductor mixer

Thus, the W/L of M_5-M_8 transistors must be chosen based on a tradeoff between power consumption and noise. Moreover, the RF input matching network modifies the conversion gain described in (1). Namely, it can be shown that the conversion gain now becomes,

$$GC \approx \frac{2}{\pi} \frac{g_m R_L}{C_{gs} R_g \omega_o} \quad (3)$$

The LO signals are coupled to the LO input of the mixer by RLC narrowband networks resonating at 2.4 GHz. As can be seen in Figure 2, two scaled CMOS inverters in cascade are used to drive the LO signal. This way, at the output of the buffer inverters, the signal results in trapezium waveforms, with 1.2V amplitude, as shown in Figure 3. Nevertheless, the switches can be directly driven by antiphase sinewave signals, without an additional LO buffer, but in this case, the conversion gain is degraded. Figure 4 shows the comparison of the simulated conversion gain when input matching and LO buffers are used and when the sinewave signals are directly driven to the switches. It can be seen that the input matching and the buffer increases the conversion gain. Moreover, the LO buffer reestablishes the LO levels, keeping the conversion gain in 20 dB when the LO amplitude is decreased.

The choice of the ratio W_P/W_N of the switch transistors affects the ratio between the ON- and OFF-switching time and common-mode output currents. As PMOS transistors have mobility roughly two times lower approximately, W_P/W_N is chosen to be around two. If the switch width decreases, keeping W_P/W_N=2, the conversion gain results in a gradual degradation, as shown in Figure 5. The final decision was W_N/L_N=25u/0.24u and W_P/L_P=50u/0.24u

The ZigBee standard imposes that the system should work properly for input signal power from -20dBm to -85dBm. In order to relax the variable gain amplifier specifications and reduce the overall noise in the whole receiver, the mixer was designed with two gain modes; 12 dB for R_L =1kΩ and 20 dB for R_L=12kΩ.

The common-mode current is absorbed by the two PMOS load transistors, allowing for more conversion gain. The current source I_b shifts the common-mode output voltage to near 0.6V. This current source is adapted to the gain mode, in order to maintain the output common mode voltage around 0.6V when the gain is changed.

The selected element sizes and dimensions are listed in Table I.

Mixer design has been performed under the Cadence® Design Framework II environment using SpectreRF simulator. Figure 6 shows the S_{11} curve of the mixer. The input return loss is below -20 dB@2.4GHz. Noise Figure (NF) results are shown in Figure 7; values at 2.5MHz are 18.1dB at high gain and 18.9 dB at low gain mode. As expected from (9), NF is higher in the low gain mode because the load resistor is smaller. Input third order intercept point IIP_3 is set at RF frequency of 2.4025 GHz and 2.4035 GHz with 1MHz separated. Figure 8 shows the output power of fundamental and 3rd-order inter-modulation. . IIP3 is determined to be -3.1dBm and -3.5dBm while P_{1dB} is -11.6dBm and -10.5dBm at low and high gain respectively.

TABLE I. Device sizes and dimensions

$M_{1,3}$ (μm)	$M_{2,4}$ (μm)	M_{5-8} (μm)	$M_{9,10}$ (μm)	R_L (kΩ)	V_B (V)
50/0.24	25/0.24	160/0.24	52.8/0.24	1-12	0.5
R_g (Ω)	**L_g (nH)**	**C_{gs} (pF)**	**R_{LO} (Ω)**	**L_{LO} (nH)**	**C_{LO} (pF)**
51	2.13	1.60	17	2.13	1.85

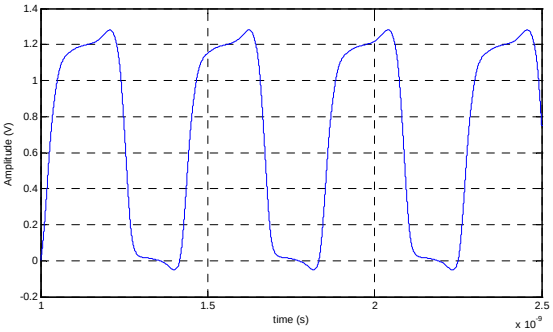

Figure 3. Waveform at the output of the LO buffer inverters

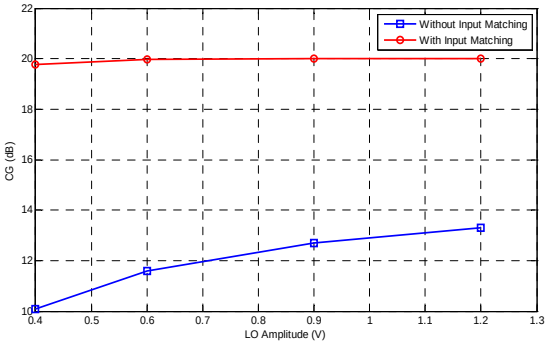

Figure 4. Simulated Conversion Gain versus LO amplitude with and without input matching and LO buffer (R_L=12KΩ)

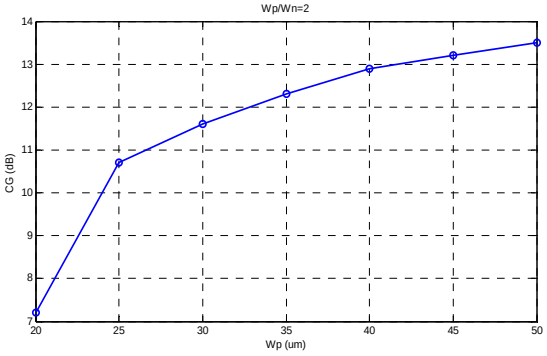

Figure 5. Simulated conversion gain as a function of swicth width (keeping Wp/Wn=2, R_L=1KΩ)

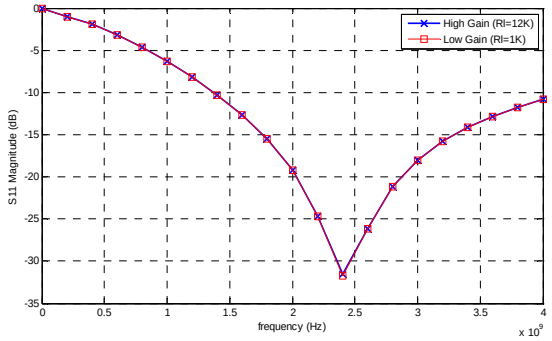

Figure 6. S_{11} simulation results for the two gain mode

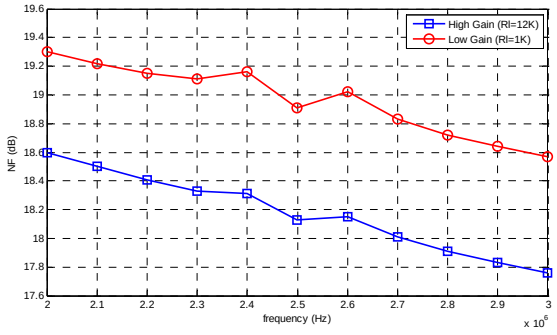

Figure 7. NF simulation results for the two gain mode

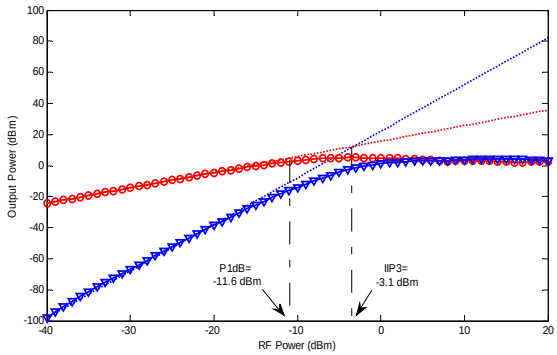

Figure 8. Simulated IF output power versus RF power.

IV. IC Implementation and Measurements

Figure 9 shows a photograph of the implemented mixer. The total core silicon area including on-chip matching networks is 1005x855µm2, while the power consumption is 4.1mW and 4.4mW in low and high mode gain respectively (it includes the bias circuitry, LO buffers and ESD circuit protection). The mixer core consumes 1.96mW in both cases because the transconductance stages and the input and output common mode voltage remain identical when the gain mode is changed. Nevertheless, the current I_b is increased at low gain mode, in order to maintain the output common mode voltage around 0.6V. For this reason, power consumption is higher in the low gain mode.

The chip has been measured via on-wafer probing of RF and LO ports through G-S-G-S-G probes using baluns for single to differential conversion at the input signals. A differential probe was used to measure the differential output voltage. Figure 10 shows the block diagram of the measure setup. HP8664A and HP81134A signal generators have been used to generate the required RF and LO signals at the 2.4 GHz band. The differential output signal is converted to single in order to be measured using the HP8562E Spectrum Analyzer. Despite the experimental inaccuracies, it can be concluded that the mixer has the expected 12dB and 20dB conversion gain at low and high gain modes respectively. Figure 11 shows the output signal spectrum for an input single tone at 2.4025GHz and a power of -26dBm. LO is centered at 2.4GHz and the mixer is programmed in high gain mode.

In order to evaluate the linearity of the mixer, measurements with two input tones separate 1MHz at 2.4025GHz and 2.4035GHz have been carried out. Figure 12 shows the output signal spectrum for high gain mode and LO at 2.4GHz. The two input tones after mixing operation are situated at 2.5MHz and 3.5MHz while the 3rd-order intermodulation tones are at 1.5MHz and 4.5MHz. As it is shown in Figure 12, the intermodulation tones present attenuation with respect the desired tones of 50dB approximately.

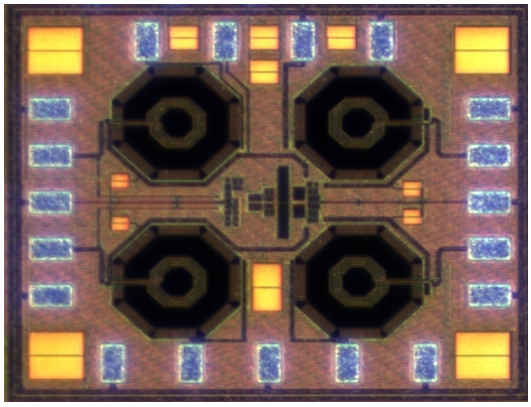

Figure 9. Layout of the designed mixer

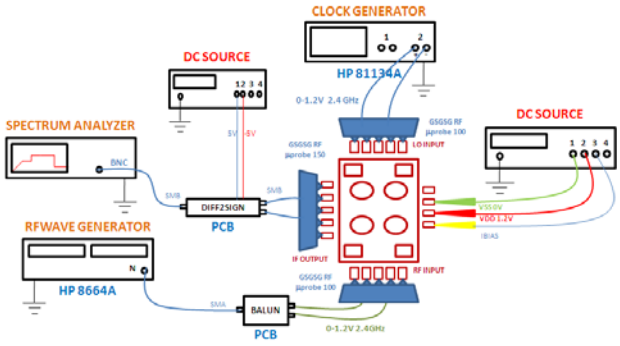

Figure 10. Measure Setup Block Diagram

TABLE II. Performance summary and comparison to other CMOS mixers

Ref	CMOS Process	RF Frequency [GHz]	IF Frequency [MHz]	CG [dB]	NF [dB]	IIP3 [dBm]	Power [mW]	Chip size [mm^2]
[8]	0.18 µm	2.4	0	15.6	6.9	1.5	7.6	N.A.
[9]	0.18 µm	2.4	1	13†	18†	-1†	7.2†	0.67
[10]	0.13 µm	2.4	60	15.7†	15.7†	-9†	0.5†	0.8
[11]	0.18 µm	2.4	1	16	12.9	1	8.1	0.32
This work	90 nm	2.4	2.5	12 / 20*†	18.9 / 18.1*	-3.1/ -3.5*	4.4 / 4.1*† (1.96 core)	0.85

*Low / High gain mode †Experimental Results

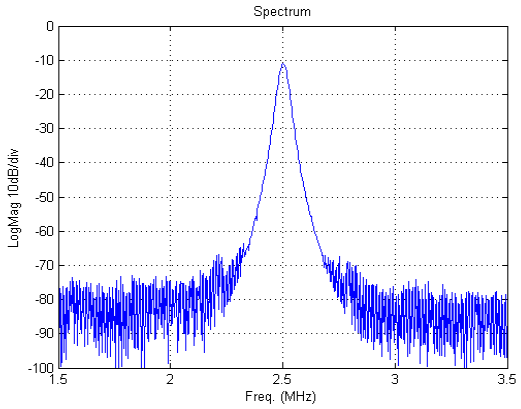

Figure 11. Output Signal Spectrum spectrum for an input single tone at 2.4025GHz and a power of -26dBm

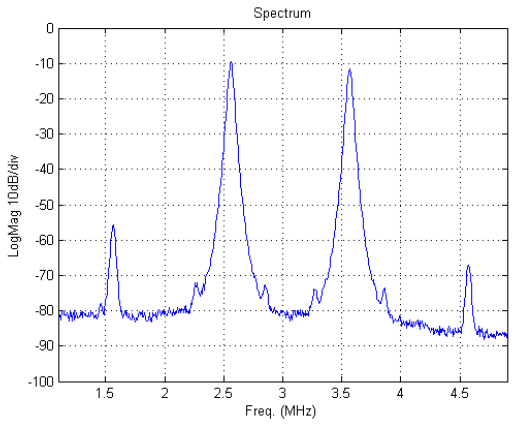

Figure 12. IM3 Test for f_1=2.4025GHz and f_2=2.4035GHz

V. CONCLUSIONS

A low voltage and low power switched transconductor mixer in a 90nm CMOS process has been presented. RF and LO input matching networks are included in order to be measured using on- wafer probing. Two possible gains of 12dB and 20dB can be set by programming the load resistor. LO signals are driven by CMOS buffer inverters to avoid conversion gain degradation. The RF stage operates in weak inversion for low power consumption; it is 4.1mW and 4.4mW at high and low gain mode respectively from a 1.2V power supply, but the core cell only takes 1.96mW. Simulation and experimental results show a very good performance in terms of linearity and noise when compared to other mixers in the literature.

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