# Overview of Carbon-Based Circuits and Systems

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***Abstract*—This paper presents an overview of the state of the art on carbon-based circuits and systems made up of carbon nanotubes and graphene transistors. A tutorial description of the most important devices and their potential benefits and limitations is given, trying to identify their suitability to implement analog and digital circuits and systems. Main electrical models reported so far for the design of carbon-based field-effect devices are surveyed, and the main sizing parameters required to implement such devices in practical integrated circuits are analyzed. The solutions proposed by cutting-edge integrated circuits and devices are discussed, identifying current trends, challenges and opportunities for the circuits and systems community[1].**

## I. Introduction

Carbon-based nanomaterials and nanodevices, such as graphene and Carbon NanoTubes (CNTs), are among the most promising candidates to either replace or complement silicon-based Field-Effect Transistors (FETs) in future beyond-CMOS Integrated Circuits (ICs). The outstanding physical and electrical properties of these nanomaterials, including their – a priori – excellent carrier mobility, current density, transition frequency, near-ballistic transport, thermal conductivity, adjustable bandgap as well as the possibility to use the same material to build diverse IC elements, have prompted the interest of many researchers in both academy and industry for CNT-FETs and Graphene-FETs (G-FETs) in order to continue the technology downscaling toward *deep nanoscale* level in an efficient way in terms of energy and cost [1], [2].

In spite of the mentioned benefits, after the initial enthusiasm for carbon-based nanoelectronics, a number of inherent physical limitations and device imperfections have been reported that make the use of CNT-FETs and G-FETs to implement competitive chips still far from reality. Among others, the most limiting factors are the poor current saturation, the large contact/access resistances, the influence of synthesis/fabrication process variability (in CNTs); the missing gap, the ambipolar conduction, the difficulty to switch off and the carrier mobility-vs-bandgap trade-off (in G-FETs). As a consequence, state-of-the-art carbon-based ICs mostly consist of small circuits made up of single devices or just a few transistors [3], [4].

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With the aim of addressing these limitations, recent advances in device fabrication techniques as well as appropriate design methodologies are being developed in order to push CNT and graphene technologies forward and to demonstrate the feasibility of carbon-based integrated circuits and systems [5]. These methods are running in parallel with the development of SPICE models to accurately simulate CNT-FET/G-FET circuits and to systematize their analysis and design by following a top-down/bottom-up approach [6]–[14].

In this scenario, the aim of this overview paper and this special session is to present a survey of recent advances in CNT-FET and G-FET circuits and systems. To this end, the fundamental concepts related to carbon-based transistors are reviewed, putting emphasis on their physical structure, electrical properties and main design/sizing parameters. The most relevant electrical models and design methods are discussed in order to show the current state of the art on CNT and graphene technologies, from a circuits-and-systems perspective, by covering the main aspects of the design procedure, physical implementation and applications. Main practical issues and trends are identified as well as the solutions proposed by cutting-edge designers, with emphasis on those applications in which carbon-based nanodevices may be competitive with respect to standard CMOS. All these ingredients are put together as an introduction to this special session, contributed by several selected experts in the field, which present their recent results and developments in the frontiers of the state of the art on carbon-based nanoelectronics.

## II. Survey of Carbon-Based Transistors

Carbon-based transistors aim to get advantage of the excellent electronic properties of two allotropic forms of carbon, namely: CNTs and graphene. To this end, different FET devices can be built by replacing the channel of a conventional CMOS transistor by either CNTs or graphene sheets. This is illustrated in Fig. 1, which shows the conceptual structure of some CNT-FETs and G-FETs reported in literature.

### A. CNT Transistors

Fig. 1(a) shows the schematic cross-sectional structure and symbol of a typical CNT transistor. In this device, the channel consists of a number, $n_{\text{tub}}$, of CNTs which connect the drain and source terminals, and its conductance is modulated by the voltage applied at the gate terminal – similarly to

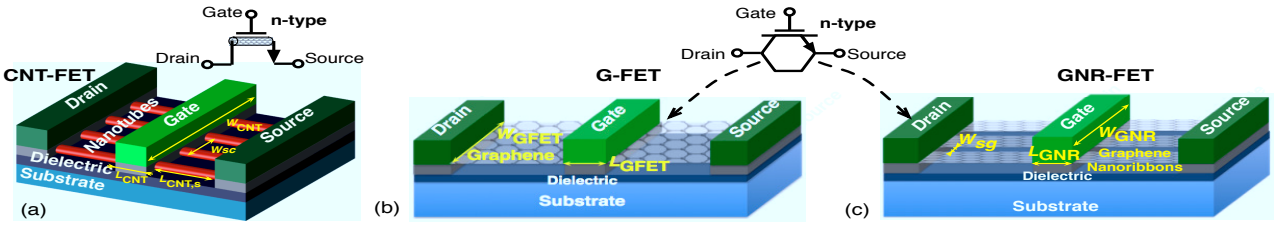


Fig. 1. Schematic symbol and cross-sectional conceptual view of the physical structure of: (a) CNT-FETs. (b) G-FETs. (c) GNR-FETs

CMOS transistors. Indeed, the main sizing parameters are the dimensions of the channel – defined by the length, $L_{\text{CNT}}$, and width, given by $W_{\text{CNT}} = n_{\text{tub}} \cdot W_{sc}$, with $W_{sc}$ being the separation between the centres of two adjacent CNTs. Note that $W_{\text{CNT}}$ is proportional to the diameter of the CNTs, given by $d_{\text{CNT}} = a/\pi \cdot \sqrt{m^2 + m \cdot n + n^2}$, with $(m, n)$ denoting the chirality vector and $a = 2.49$Å being the lattice constant [6]. Another important characteristic of CNTs is that their band-gap energy, $E_g$, is inversely proportional to $d_{\text{CNT}}$. This property makes CNTs a powerful material for electronics, although it strongly depends on the way in which CNTs are synthesized and grown. Typically, CNTs with $d_{\text{CNT}} = 1.5$nm, $m = 19, n = 0$ (zigzag CNT), $W_{sc} = 4$-5nm are fabricated with densities of 200-250 CNTs/$\mu$m [5], [10].

The CNT transistor in Fig. 1(a) can be modeled at electrical-level for circuit design and simulation purposes. One of the most successful and accurate SPICE models was developed by Deng *et al* at Stanford University [6], [7]. Based on this model, the following simplified expression of the drain-source current, $I_{\text{DS-CNT}}$, can be derived as [10]:

$$I_{\text{DS-CNT}} = \frac{n_{\text{tub}} \cdot g_{\text{CNT}} \cdot (V_{\text{DD}} - V_{\text{th,CNT}})}{1 + g_{\text{CNT}} \cdot L_{\text{CNT,s}}} \quad (1)$$

where $V_{\text{DD}}$ is the supply voltage, $g_{\text{CNT}}$ is the transconductance per CNT, $V_{\text{th,CNT}}$ is the threshold voltage and $L_{\text{CNT,s}}$ is the length of the doped source region of the CNT (see Fig. 1(a)). Although the above expression may be useful for some hand calculations, the complete SPICE model [6], [7], is used for a precise simulation. An alternative model can be derived using the Landauer formula [15]. However, this procedure requires using numerical methods to obtain closed-form solutions, what makes it difficult its use in circuit design [16], [17].

### *B. Graphene Transistors*

A G-FET can be built by using a graphene sheet to implement the transistor channel, as conceptually depicted in Fig. 1(b). The potential use of this device in ICs has prompted the interest of a number of researchers for finding out electrical models which can be used for circuit design and simulation [12], [14], [18], [19]. Among others, the model proposed by Frégonèse *et al* at the University of Bordeaux [12] provides an accurate description of the device operation, including its main non-ideal and second-order phenomena, and can be coded in SPICE or Verilog-A for circuit simulation. Based on this model, the drain-source current of a G-FET can be expressed as [14]:

$$I_{\text{DS-GFET}} = \mu W_{\text{GFET}} \cdot \frac{\int_0^{V_{\text{DS}_i}} (|Q_{\text{net}}| + e \cdot n_{\text{puddle}}) dV}{L_{\text{GFET}} + \mu \cdot \left| \int_0^{V_{\text{DS}_i}} \frac{1}{v_{\text{SAT}}} dV \right|} \quad (2)$$

where $\mu$ is the electron mobility, $Q_{\text{net}}$ is the net mobile charge density per unit area, $e$ is the electron charge, $V_{\text{DS}_i}$ is the internal drain-source voltage, $v_{\text{sat}}$ is the saturation velocity and $n_{\text{puddle}} = \Delta^2/\pi\hbar^2 v_f^2$, with $\Delta$ being the spatial inhomogeneity of the electrostatic potential, $\hbar$ is the reduced Planck constant, and $v_f$ is the Fermi velocity.

Note from (2) that the basic sizing parameters of a G-FET are the length, $L_{\text{GFET}}$, and the width, $W_{\text{GFET}}$, of the graphene sheet, i.e. the channel dimensions – similar to CMOS. However, if the graphene sheet is not narrow enough, $E_g = 0$. This property has two critical consequences for the operation of G-FETs. First, the transistor does not switch off completely. Instead, a minimum off drain-source current is found in the inflection point (also called Dirac point) resulting in low on/off current ratios which limit their application for digital circuits. Second, the device presents an ambipolar conduction, behaving as either an n-type or p-type FET, depending on the polarity of the voltage applied at the gate [3]. This is illustrated in Fig. 2(a), where $I_{\text{DS-GFET}}$ is plotted versus $V_{GS}$, by using HSPICE® for different sizings compared to 32-nm CMOS.

Both CNT-FETs and G-FETs have shown saturation regions which are an important requirement to build amplifiers. Indeed, under specific biasing conditions, G-FETs exhibit negative differential resistance which can be very useful for oscillators and latch-based circuits design. This is illustrated in Fig. 2(b), which compares the $I_{\text{DS}}$-vs-$V_{\text{DS}}$ curves of G-FETs and CNT-FETs for different technology nodes.

An alternative to solve the switching problem of G-FETs consists of replacing the large-area graphene sheet by a

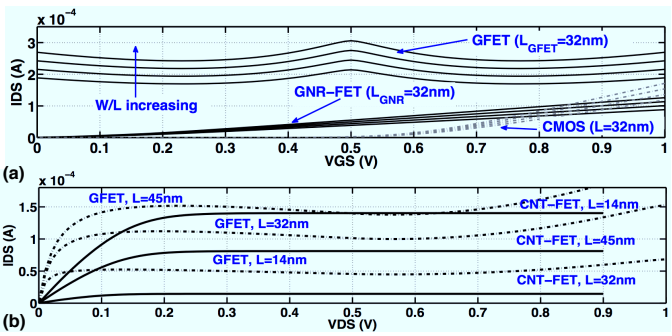


Fig. 2. Characteristics of carbon FETs: (a) $I_{\text{DS}}$-vs-$V_{\text{GS}}$. (b) $I_{\text{DS}}$-vs-$V_{\text{DS}}$.

number of graphene ribbons with narrow widths (typically $<$ 10nm). This way, as $E_g$ is inversely proportional to the ribbon width, the resulted transistors, named Graphene NanoRibbon FETs (GNR-FETs), *open* the bandgap of graphene, and hence, can be switched off and used for digital logic purposes [3].

Fig. 1(c) shows the conceptual structure of a typical GNR-FET, where main design parameters are highlighted – based on the SPICE model presented in [13] and available in [20]. According to this model, the channel length, $L_{\text{GNR}}$, is the length of one of the graphene nanoribbons, while the channel width can be expressed as $W_{\text{GNR}} = n_{\text{rib}} \cdot (W_{sg} + 2 \cdot W_c)$ [13], where $n_{\text{rib}}$ is the number of nanoribbons, $W_{sg}$ is the spacing between two adjacent nanoribbons and $W_c = \sqrt{3} d_{cc} \cdot (N+1)/2$, with $d_{cc} = 0.142$nm being the carbon-carbon bond distance and $N$ is the number of dime lines [13]. As shown in Fig. 2(a), the transfer characteristic of a GNR-FET is similar to that of CMOS, although GNR-FETs feature a more resistive behavior.

## III. State of the Art on CNT-Based ICs

CNT-FETs are – a priori – excellent candidates for building highly energy-efficient digital systems, in which are projected to achieve an order of magnitude improvements in energy-delay product compared with silicon-based CMOS at highly scaled technology nodes [2], [5]. However, since the first experimental demonstrations of CNT-FETs, the majority of reported ICs have been based on device-level measured results [21]. The implementation of more complex CNT-FET ICs has not been possible due to inherent CNT imperfections and variations, among others: mispositioned CNTs, presence of metallic CNTs, $n_{\text{tub}}$/CNT-FET density variations, etc [10].

These limitations may severely degrade the performance of CNT-FET based ICs, what has motivated the development of suitable design methodologies to overcome them. One of the most successful approaches is the so-called *imperfection-immune design paradigm* (IIDP) proposed by Zhang *et al.* [11], which is based on CNT-specific aligned-active layout techniques to control and minimize the mentioned CNT variations. This methodology can be combined with the so-called VLSI-compatible Metallic CNT Removal (VMR) technique to improve the ratio of semiconductor and metallic CNTs up to 99.99% [9]. Based on these strategies, the authors in [8] presented a technique for designing CNT-FET logic circuits with a number of misaligned and mispositioned CNTs. The implemented CNT-FET immune logic ICs demonstrated to be 13 times more efficient than their 32-nm CMOS counterparts, in terms of energy-delay product. Indeed, the use of IIDP and VMR techniques enabled the first experimental demonstration of several functional CNFET logic circuits, namely: VLSI-compatible CNFET full adders and other arithmetic elements and latches [9], [22] as well as monolithic 3D ICs using CNFETs [23]. Other CNFET circuit demonstrations include ring-oscillators [24] and adder circuits on a single CNT [25].

Apart from their use in digital applications, more recently, a group of researchers from Stanford University and Katholieke Universiteit Leuven (KUL) has successfully demonstrated a complete sensor interface IC made up of CNT-FETs [5]. All these demonstrators, fueled by the development of appropriate design methodologies and fabrication techniques, are making possible the implementation of more and more complex CNT-FET based ICs, which are expected to outperform technologies based on other alternative nanodevices – like FinFETs and silicon-nanowire transistors – at highly scaled nodes ($<$ 9nm) with reduced operating voltage ($<$ 0.5V) [5], [26].

## IV. State of the Art on Graphene-Based ICs

One of the big advantages of graphene with respect to silicon CMOS is its superior electron mobility. It has been shown that carrier mobilities of graphene in $SiO_2$ substrate supported devices can be $\mu = 2 \times 10^4 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ [27]. As a comparison, a standard 65-nm RF CMOS process – commonly used in today's consumer electronics – has a low-field mobility of barely $\mu = 350 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$. In practice, charged impurities in the dielectrics degrade the electronic properties of graphene, and particularly its mobility. This problem can be tackled by using other dielectrics such as h-BN, leading to $\mu = 6 \times 10^4 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ [28]. These high mobilities are directly reflected in high intrinsic transit frequencies, $f_T$. Indeed, cutting-edge G-FET devices feature $f_T = 210$ GHz for $L_{\text{GFET}} = 210$nm [29], $f_T = 280$ GHz for $L_{\text{GFET}} = 40$nm [30], and $f_T = 300$ GHz for $L_{\text{GFET}} = 144$nm [31].

Based on their outstanding mobilities, the state-of-the-art shows the potential of G-FETs for ultra-high-data rate mobile communications systems. In addition, G-FETs present very high linearity performance which is fundamental in RF front-ends [32]. Indeed, one promising approach is an all-graphene based mm-wave radio module, which can be connected to silicon-based digital baseband processors in next-generation (5G) mobile communication systems as conceptually illustrated in Fig. 3. These systems will require circuits operating in the mm-wave range, i.e. 10GHz-100GHz. Although latest nanometer CMOS technologies can potentially provide a cost-effective solution if products enter mass-production stage, the use of G-FETs may become more energy-efficient.

Indeed, although current graphene technology is not mature enough, ultra-high-frequency/RF G-FET ICs have been successfully demonstrated. Thus, a broadband mixer working up to 10 GHz has been reported in [33], an harmonic mixer operating at 30 GHz in [34] and a ring oscillator working at 1.28 GHz in [35]. Apart from being used in transistors, the outstanding electric and mechanic characteristics of graphene

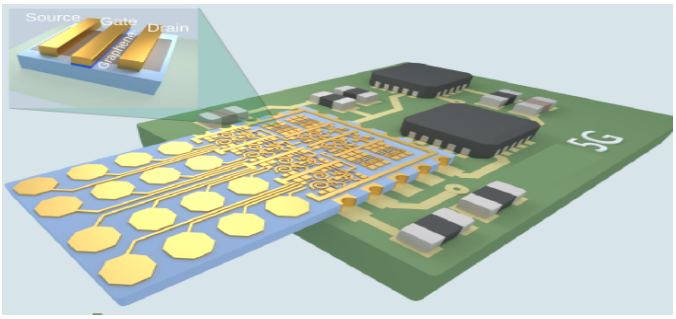


Fig. 3. Conceptual illustration of G-FET-based 5G telecom systems.

have also attracted attention in other related fields. Thus, suspended graphene membranes which can be mechanically actuated by an external electric field have been used in RF MEMs. These devices can be applied to build RF switches, variable capacitors and resonant cavities, among others [36]. All these results – comparable or even outperforming similarly sized CMOS transistors – are extremely encouraging considering that the first G-FETs appeared only a few years ago.

## V. Conclusions and Special-Session Overview

An overview of the state of the art on carbon-based circuits and systems has been presented, giving a tutorial survey of CNT-FETs and G-FETs, their main electrical characteristics, potential advantages and limitations. Cutting-edge ICs has been revised, which demonstrate that by using suitable design methodologies and implementation strategies, successful and even outstanding performance can be achieved in both analog and digital applications. The versatility of graphene and CNT materials to implement different types of circuit elements in an IC, together with their benefits with respect to silicon-based CMOS transistors, demonstrate the strong potential of G-FETs for future energy-efficient digital logic and ultra-high-speed analog/RF ICs in the *post*-CMOS era. However, there are still a number of practical issues to be addressed in order to achieve a performance comparable to standard CMOS VLSI chips.

This special session covers diverse aspects of the present status of carbon-based nanoelectronics. In the first paper, Akinwande *et al.* present recent progress on carbon-based flexible electronics. The second paper, presented by Frégonèse *et al*, deals with the pros and counts of using G-FETs for RF applications. The third paper, co-authored by Gielen *et al.* discusses the use of CNT technology to implement time-based sensors, based on the experience of the collaboration of the groups at Stanford and KUL. Finally, the session is concluded by the work of Zhang and Delgado-Frias, who present their recent results on using near-threshold CNT-FET SRAM cells.

## References


[1] Y. Wu *et al.*, "Graphene Electronics: Materials, Devices, and Circuits," *Proceedings of the IEEE*, vol. 101, pp. 1620–1637, July 2013.

[2] W. Hai *et al.*, "Carbon nanotube circuits: Opportunities and challenges," *Proc. of the 2013 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, vol. 12, pp. 619–624, March 2013.

[3] F. Schwierz, "Graphene Transistors: Status, Prospects, and Problems," *Proceedings of the IEEE*, vol. 101, pp. 1567–1584, July 2013.

[4] J. Liang *et al.*, "Design and Evaluation of Multiple Valued Logic Gates Using Pseudo N-Type Carbon Nanotube FETs," *IEEE Trans. on Nanotechnology*, vol. 13, pp. 695–708, July 2014.

[5] M. M. Shulaker *et al.*, "Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs," *IEEE J. of Solid-State Circuits*, vol. 49, pp. 190–201, January 2014.

[6] J. Deng *et al.*, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application – Part I: Model of the Intrinsic Channel Region," *IEEE Trans. on Elect. Devices.*, vol. 54, pp. 3186–3194, December 2007.

[7] J. Deng *et al.*, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application – Part II: Full Device Model and Circuit Performance Benchmarking," *IEEE Trans. on Elect. Devices*, vol. 54, pp. 3195–3205, December 2007.

[8] N. Patil *et al.*, "Design Methods for Misaligned and Mispositioned Carbon-Nanotube Immune Circuits," *IEEE Trans. on Computer-Aided Design of Integ. Circ. and Syst.*, vol. 27, pp. 1725–1736, Oct. 2008.

[9] N. Patil *et al.*, "VMR: VLSI-compatible metallic carbon nanotube removal for imperfection-immune cascaded multi-stage digital logic circuits using Carbon Nanotube FETs," *Proc. of the 2009 IEEE Elect. Devices Meeting (IEDM)*, pp. 1–4, December 2009.

[10] N. Patil *et al.*, "Circuit-Level Performance Benchmarking and Scalability Analysis of Carbon Nanotube Transistor Circuits," *IEEE Trans. on Nanotechnology*, vol. 8, pp. 37–45, January 2009.

[11] J. Zhang *et al.*, "Robust Digital VLSI Using Carbon Nanotubes," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, pp. 453–471, April 2012.

[12] S. Fregonese *et al.*, "Scalable Electrical Compact Modeling for Graphene FET Transistors," *IEEE Trans. on Nanotech.*, pp. 539–546, July 2013.

[13] Y. Y. Chen *et al.*, "A SPICE-compatible model of Graphene Nano-Ribbon Field-Effect Transistors enabling circuit-level delay and power analysis under process variation," *Proc. of the 2013 DATE Conf.*, pp. 1789–1794, March 2013.

[14] S. Rodriguez *et al.*, "A Comprehensive Graphene FET Model for Circuit Design," *IEEE Trans. Elect. Devices*, vol. 61, pp. 1199–1206, April 2014.

[15] A. Raychowdhury and K. Roy, "Carbon-Nanotube-Based Voltage-Mode Multiple-Valued Logic Design," *IEEE Trans. on Nanotechnology*, vol. 4, pp. 168–179, March 2005.

[16] I. O. Connor *et al.*, "CNTFET Modeling and Reconfigurable Logic-Circuit Design," *IEEE Trans. on Circuits and Systems – I: Regular Papers*, vol. 54, pp. 2365–2379, November 2007.

[17] G. Gelao *et al.*, "A Semiempirical SPICE Model for n-Type Conventional CNTFETs," *IEEE Trans. on Nanot.*, pp. 506–512, May 2005.

[18] K. L. Shepard, I. Meric, and P. Kim, "Characterization and modeling of graphene field-effect devices," *Proc. of the 2008 IEEE/ACM International Conf. on Computer-Aided Design*, pp. 406–411, November 2008.

[19] D. Jimenez and O. Moldovan, "Explicit drain-current model of graphene field-effect transistors targeting analog and radio-frequency applications," *IEEE Trans. on Elec. Dev.*, vol. 58, pp. 4049–4052, Nov. 2011.

[20] Y.-Y. Chen *et al.*, *SPICE Model of Graphene Nanoribbon FETs.* [Online]. Available: https://nanohub.org/resources/17074., 2008.

[21] R. A. Martel *et al.*, "Single- and multi-wall carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 73, no. 17, pp. 2447–2449, 1998.

[22] N. Patil *et al.*, "Scalable carbon nanotube computational and storage circuits immune to metallic and mis-positioned carbon nanotubes," *IEEE Trans. on Nanotechnology*, vol. 10, pp. 744–750, July 2011.

[23] L. Wei *et al.*, "Performance Benchmarks for Si, III-V, TFET, and Carbon Nanotube FET – Re-thinking the Technology Assessment Methodology for Complementary Logic Applications," *Proc. of the 2010 IEEE Elect. Devices Meeting (IEDM)*, pp. 391–394, December 2010.

[24] Z. Chen *et al.*, "An Integrated Logic Circuit Assembled on a Single Carbon Nanotube," *Science*, vol. 301, p. 1735, 2006.

[25] L. Ding *et al.*, "CMOS-based carbon nanotube pass-transistor logic integrated circuits," *Nature Comm.*, vol. 3, p. 677, 2012.

[26] A. D. Franklin *et al.*, "Sub-10 nm carbon nanotube transistor," *Nano Lett.*, vol. 12, no. 2, pp. 758–762, 2012.

[27] J. Chen *et al.*, "Intrinsic and extrinsic performance limits of graphene devices on SiO2," *Nature Nanotech.*, vol. 3, no. 4, pp. 206–209, 2008.

[28] C. R. Dean *et al.*, "Boron Nitride Substrates for High-Quality Graphene Electronics," *Nature Nanotechnology*, pp. 722–726, August 2010.

[29] Y.-M. Lin *et al.*, "Enhanced Performance in Epitaxial Graphene FETs With Optimized Channel Morphology," *IEEE Electron Device Letters*, vol. 32, no. 10, pp. 1343–1345, 2011.

[30] Y. Wu *et al.*, "Record high RF performance for epitaxial graphene transistors," *Proc. IEEE IEDM*, pp. 23.8.1–23.8.3, 2011.

[31] L. Liao *et al.*, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature*, vol. 467, pp. 305–308, September 2010.

[32] S. Rodriguez *et al.*, "Static Non-linearity in Graphene Field Effect Transistors," *IEEE Trans. Elect. Devices*, no. 8, pp. 3001–3003, 2014.

[33] Y.-M. Lin *et al.*, "Wafer-scale graphene integrated circuit.," *Science*, vol. 332, no. 6035, pp. 1294–7, 2011.

[34] O. Habibpour *et al.*, "A 30-GHz Integrated Subharmonic Mixer Based on a Multichannel Graphene FET," *IEEE Trans. Microw. Theory Tech*, vol. 61, no. 2, pp. 841–847, 2013.

[35] E. Guerriero *et al.*, "Gigahertz Integrated Graphene Ring Oscillators," *ACS nano*, vol. 7, no. 6, pp. 5588–5589, 2013.

[36] J. Perruisseau-Carrier, "Graphene for antenna applications: Opportunities and challenges from microwaves to THz," *Proc. IEEE Loughborough Antennas & Propagation Conference*, pp. 1–4, 2012.