

ECCTD 2007 Special Issue **'Bridging Technology Innovations to Foundations'**

This special issue includes extended versions of 14 contributions that were presented at the *2007 European Conference on Circuit Theory and Design*, held in Seville, Spain. They were selected out of the 259 contributions presented as lectures at the conference sessions. The selection was made by the Guest Editors based on three criteria. First, the novelty and relevance of the ideas and results embedded in the contributions. Second, the scores of the referees who evaluated the manuscripts sent to ECCTD; they all were in full-paper format and got a minimum of three reviews each. Third, the feedback provided by the session chairmen and the audience of the lecture presentations. After completing such a selection process, 25 authors were invited to send extended versions of their conference papers. The manuscripts submitted for publication entered a peer-review process involving a minimum of three referees complementary to those who reviewed the papers sent to the conference. The 14 papers included in the issue were finally recommended for publication after a two-iteration review cycle. Unfortunately, the page budget available for this special issue is necessarily limited and hence, many high-quality papers that were presented at the conference could not find their way to this special issue. We would like to thank all the authors and presenters of ECCTD 2007 for their excellent contributions to the conference.

The motto of the 2007 conference was '*Bridging Technology Innovations to Foundations*'. Understanding the foundation of circuit theory has been from the very beginning at the focus of the ECCTD series of conferences, as well as at the focus of the IJCTA. Such fundamental understanding is crucial to design the innovative micro- and nano-electronic circuit and systems that are ubiquitous in the modern world. Besides, the ever increasing, astonishing potentials of the technologies that are currently available to build these systems define new challenges for further foundational works. The papers compiled in this special issue are aligned to this motto and cover a wide range of topics: devices, analog blocks and subsystems, low-voltage analog and digital design, structured analog design, calibration and error correction, RF circuits, sensor circuits and communication systems.

The first two papers address challenges that are close to the device level. The first paper, by Paula López *et al.*, develops a physical I-V DC model for short-channel polygonal-shape enclosed-layout transistors, which covers the most relevant second-order phenomena that degrade the operation of this type of transistors. This model, supported by experimental results, is useful in applications involving the design of radiation-hardened circuits. The second paper, by Daniel Durini *et al.*, addresses the design of a pixel detector in CMOS silicon-on-insulator technology. Novel device and circuit considerations are presented to allow the design of imagers with enhanced quantum efficiency in the near infrared region of the spectra.

The next two papers present considerations and results that rely on innovative ways of using the MOS transistor. The design with low-voltage supplies is addressed in both papers. The third paper in the issue, by Pietro Monsurr`o *et al.*, employs the transistor substrate as a signal-driven terminal to reduce the minimum supply requirement in the design of analog building blocks. Specifically, it reduces by two MOS thresholds the supply required for a rail-to-rail amplifier with complementary input stages. Innovative single-stage amplifier topologies are reported capable to operate with down to 0.9V supply and to provide up to 56 dB DC gain. The fourth paper, by Omer Can Akgun *et al.*, addresses the optimization of the temporal response of digital circuits capable to operate with 220mV supply by biasing the MOST in the weak inversion region. Design and simulation results of a novel current sensing-based completion detection circuit are presented, which achieve speed improvements close to 20% versus conventional approaches.

The fifth and the sixth papers in the issue, respectively by Arantxa Otín *et al.* and José L. Ausín *et al.*, present innovative solutions related to the incorporation of programmability into some key analog building blocks; namely filters and oscillators. The paper by Arantxa Otín *et al.*, focuses on the concurrent tuning of both frequency and quality factor for digitally programmable continuous time Gm-C filters. A hybrid frequency tuning method that allows both analog and digital control is presented based on a digital phase comparator in the phase-locked loop. Tuning accuracy in the range of 4% is measured on a silicon prototype. The paper by José L. Ausín *et al.* proposes a novel way to make a switched-capacitor relaxation oscillator programmable without neither modifying component values nor clock frequencies. Instead the size of charge packets is modified by resorting to programmable reference voltages controlled by a noise-shaping feedback coder.

The next two papers in the special issue present contributions to methodologies for the structured design of analog circuits. On the one hand, the paper by Jouni Kaukovuori *et al.* addresses the systematic design of a common-gate LNA for wideband applications; including the analysis of the different components in matching network and an illustrative design. On the other hand, the paper by Helmut Graeb *et al.*, deals with the systematic exploration of trade-offs arising in the design of analog building blocks. Starting with a comprehensive description of the fundamentals of Pareto optimization tools, the paper presents solutions to the challenge of addressing variability during the design optimization process.

The ninth paper in the special issue, by Pieter Harpe *et al.*, addresses the very important topic of error correction in analog circuits. It presents a method for on-chip measurement and correction of gain errors, offset errors and time-skew errors in time-interleaved ADCs. These methods are complemented with the proposal of an architecture that incorporates feedback loops to set key analog parameters and hence attenuate the impact of channel matching errors.

The last group of papers in this issue is concerned with systems and applications. The tenth paper of the issue, by Robert Sobot *et al.*, focuses on the full 0.35_μm CMOS implementation of a mixed-signal receiver for high-speed multi standard (T1/E1/J1) digital communication networks. Comprehensive simulations and experiments validate the functionality of the system-on-chip prototype, the mixed-signal part of which occupies 1.2mm×1.8mm and drains 120mW of power at 3.3V, and which incorporates local RAM to store cable models for compensation purposes. The 11th paper of the issue, by Lasse Aaltonen *et al.*, contributes to the characterization and control-oriented dynamic model of a MEMs-based analog closed-loop capacitive accelerometer, addressing different instability mechanisms. A 10mm², 15mW BiCMOS circuit implementation of the controller, validated experimentally, yields 120 dB dynamic range within a 300 Hz band. The 12th paper of the issue, by Hakan Gürkan *et al.*, presents a novel lossy compression method for electroencephalogram signals. Authors demonstrate that the proposed approach, based on construction of the classified signature and envelope vector sets, provides better performance under different standard evaluation criteria than previously reported wavelet-transform methods with respect to four different mother wavelets. The 13th paper in the issue, by Timo Rautio *et al.*, addresses the challenge of characterizing nonlinearity in RF power amplifier (RF PA) targeting its pre-distortion in envelope-tracking transmitter architectures for non-constant envelope digital modulations. A 0.5W 1 GHz class-AB LDMOS-based RF PA is considered to demonstrate the use of digital pre-distortion to successfully reduce the nonlinearities introduced by the power supply dependence. The complete system results in a 15 dB improvement in adjacent channel power ratio, 30% reduction in error vector magnitude and a 50% reduction of AM/PM distortion characteristics, so that the overall efficiency is largely enhanced. The issue is closed by the paper '*Error Resilient Data Transport in Sensor Network Applications: A Generic Perspective*' by Rachit Agarwal *et al.* The paper presents an energy model to characterize error recovery schemes, together with a suitable performance metric to draw inferences on design criteria for such schemes. Based on these criteria, a multi-codec Reed-Solomon error correction scheme is proposed, which is demonstrated to outperform conventional approaches for packet reliability in wireless sensor networks.

We would like to transmit our deepest gratitude to the many volunteers involved in the different revision processes towards this special issue. Many thanks also to all the authors for carefully addressing the reviewer recommendations. Finally, we would like to acknowledge the support provided by Prof. Marco Gilli and the editorial board of IJCTA. We hope that this issue will reflect the strong health and polychrome scope of ECCTD and will provide you, the reader, with new insights into circuit theory and design.

Guest Editors:

Manuel Delgado-Restituto, Eduard Alarcón, Ángel Rodríguez-Vázquez,