Investigation of FACTS Devices to Improve Power Quality in Distribution Networks

Muhammad Asim Rehman Shaikh

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Control and Power Group
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Declaration

As required by the College, I hereby declare that this thesis is the result of my own work, and that any ideas or quotations from the work of other people, published or otherwise, are appropriately referenced.

Muhammad Asim Rehman Shaikh
Imperial College London
30 September 2010

Dedicated to my Mother
Anees-Un-Nisa

Abstract

Flexible AC transmission system (FACTS) technologies are power electronic solutions that improve power transmission through enhanced power transfer volume and stability, and resolve quality and reliability issues in distribution networks carrying sensitive equipment and non-linear loads. The use of FACTS in distribution systems is still in its infancy. Voltages and power ratings in distribution networks are at a level where realistic FACTS devices can be deployed. Efficient power converters and therefore loss minimisation are crucial prerequisites for deployment of FACTS devices.

This thesis investigates high power semiconductor device losses in detail. Analytical closed form equations are developed for conduction loss in power devices as a function of device ratings and operating conditions. These formulae have been shown to predict losses very accurately, in line with manufacturer data. The developed formulae enable circuit designers to quickly estimate circuit losses and determine the sensitivity of those losses to device voltage and current ratings, and thus select the optimal semiconductor device for a specific application.

It is shown that in the case of majority carrier devices (such as power MOSFETs), the conduction power loss (at rated current) increases linearly in relation to the varying rated current (at constant blocking voltage), but is a square root of the variable blocking voltage when rated current is fixed. For minority carrier devices (such as a *pin* diode or IGBT), a similar relationship is observed for varying current, however where the blocking voltage is altered, power losses are derived as a square root with an offset (from the origin).

Finally, this thesis conducts a power loss-oriented evaluation of cascade type multilevel converters suited to reactive power compensation in 11kV and 33kV systems. The cascade cell converter is constructed from a series arrangement of cell modules. Two prospective structures of cascade type converters were compared as a case study: the traditional type which uses equal-sized cells in its chain, and a second with a ternary relationship between its dc-link voltages. Modelling (at 81 and 27 levels) was carried out under steady state conditions, with simplified models based on the switching function and using standard circuit simulators. A detailed survey of non punch through (NPT) and punch through (PT) IGBTs was completed for the purpose of designing the two cascaded converters. Results show that conduction losses are dominant in both types of converters in NPT

and PT IGBTs for 11kV and 33kV systems. The equal-sized converter is only likely to be useful in one case (27-levels in the 33kV system). The ternary-sequence converter produces lower losses in all other cases, and this is especially noticeable for the 81-level converter operating in an 11kV network.

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"We all take different paths in life,
but no matter where we go,
we take a little of each other everywhere"
- Tim McGraw

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Asim Rehman
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GLOSSARY OF SYMBOLS

A	-	conduction area of a semiconductor
C_N	-	cell number in the chain of ternary sequence cascade topology
D_p	-	diffusion constant of holes
E_{max}	-	maximum electric field strength with specific doping density
E_{tot}	-	average total energy loss during on and off transition of the switch
f_{sw}	-	switching frequency of the cell
h	-	heat transfer coefficient per unit area
$i(t)$	-	switch current
I	-	operating current
I_R	-	rated current
I_m	-	peak value of the switch current
J_p	-	hole current density
J_n	-	electron current density
J	-	current density
k_{icls}	-	IGBT Conduction Loss Scaling Constant
k_{mcls}	-	MOSFET Conduction Loss Scaling Constant
$k_{P/A}$	-	maximum heat flow per unit area
L_a	-	ambipolar diffusion length
L_{JFET}	-	JFET region length of IGBT
L_n	-	depletion length extended in the n type region
m	-	number of voltage levels in the phase voltage waveform of a multi-level converter
n, p	-	electron, hole concentration
$n_D(x)$	-	optimum doping density profile in actual power MOSFET designs
n_i	-	intrinsic carrier concentration
N	-	number of H-bridge cells implementing one phase of a cascade converter
N_D	-	uniform doping concentration
N_{SW}	-	number of switching cycles per fundamental cycle
p_0	-	maximum concentration of minority carrier holes at $x = 0$, p^+/n^- junction in an IGBT
$7p$ values	-	$p_1 - p_7$, best-fit parameter values for IGBT overall model identification
P_{cond}	-	power loss due to conduction

P_d	-	rate of heat transfer (*i.e.,* the power dissipated)
P_{sw}	-	switching power loss of a cell
q	-	electronic charge
R_{bh}	-	thermal resistance from the base to the heat sink
R_{Jb}	-	thermal resistance from the Junction to the base
R_{JFET}	-	resistance of the JFET region (below the gate) in an IGBT
R_{ha}	-	thermal resistance from the heat sink to the ambient
R_{slope}	-	slope resistance of minority carrier devices
RA	-	area normalized on-resistance
R_A	-	resistance of accumulation region
R_{CD}	-	drain electrode resistance
R_{CH}	-	resistance of channel region
R_{CS}	-	source diffusion resistance
R_D	-	drift region resistance
$R_{DS(on)}$	-	drain-source on-state resistance
R_{N+}	-	substrate resistance
R_{TH}	-	thermal resistance
T_0	-	fundamental period
T	-	conduction time of switch in a H-bridge cell
U	-	cost function
$v_{junction}$	-	junction voltage drop in an IGBT
v_{on}	-	on-state voltage drop - *knee* point of the *I-V* curve
v_{JFET}	-	JFET region voltage drop in an IGBT
$V(x)$	-	voltage at a point x away from the junction
V_{block}	-	voltage that the device will be able to block
v_f		forward voltage drop
V_T	-	kT/q, thermal voltage
x_i	-	distance x to a point at which conductivity modulation takes place in the drift region of an IGBT
x	-	distance perpendicular to the junction
α_{pnp}	-	current gain of an IGBT
ΔT	-	temperature difference between regions of heat transfer
ε_o	-	permittivity of free space
ε_s	-	relative permittivity of silicon
λ	-	lagrange multiplier
μ_e,μ_p	-	electron, hole mobility
ρ_c	-	charge density per unit volume
ρ_r	-	resistivity of the drift region (n^- layer) to a uniformly distributed current
a and b	-	doping concentration at two extreme points in the n^- drift region

List of Abbreviations

AC	Alternating Current
BJT	Bipolar Junction Transistor
$COMFET$	Conductivity-modulate FET
$CSTBT$	Carrier Stored Trench Gate Bipolar
DC	Direct Current
DVR	Dynamic Voltage Restorer
$EPRI$	Electric Power Research Institute
$FACTS$	Flexible AC Transmission Systems
GTO	Gate Turn-Off Thyristor
$HVDC$	High Voltage DC Transmission
$IGBT$	Insulated Gate Bipolar Transistor
$IGCT$	Integrated Gate Commutated Thyristor
IPM	Intelligent Power Module
$MOSFET$	Metal Oxide Semiconductor Field Effect Transistor
MCT	MOS Controlled Thyristor
NPC	Neutral Point Clamped
NPT	Non Punch Through
PT	Punch Through
PWM	Pulse Width Modulation
$SITH$	Static Induction Thyristor
$SSSC$	Static Series Synchronous Compensator
$SSTS$	Solid State Transfer Switch
$SSCL$	Solid State Current Limiter
$SSCB$	Solid State Circuit Breaker
$STATCOM$	Static Compensator
SVC	Static VAr Compensator
$TCSC$	Thyristor Controlled Series Compensator
$UPFC$	Unified Power Flow Controller
VA	Volt-Ampere
VAr	Volt-Ampere reactive

Chapter 1

Introduction

1.1 Background

With the ongoing expansion and growth of the electric utility industry in both developed and developing nations, including deregulation and introduction of renewables, change is afoot in a once predictable business. Developed nations are facing the need to replace old systems with newer ones. Transmission systems are being pushed closer to their stability and thermal limits while the emphasis on the quality of power delivered is greater than ever [1]. The traditional focus of electrical power system infrastructure upgrades has traditionally been new transmission or distribution lines, substations and associated equipment made of copper and iron. However, as experience has shown over the past decade or so, the process of gaining permission to construct new lines has become extremely difficult, expensive, and time-consuming [2]. Moreover, the concern in pollution problems associated with fossil fuel thermal power plants and depletion of fossil resources has raised the need for flexible, more controllable electric grids, to meet new challenges of renewable energy integration. There are also concerns from a customer viewpoint regarding the quality and reliability of power in distribution networks. The large numbers of microprocessor units installed during the last two to three decade has raised demand for an improvement in the quality and reliability of the power supply [3]. Undoubtedly, new demands are stretching the resources of network operators and it is becoming increasingly difficult to provide a consistent and reliable quality of supply [4].

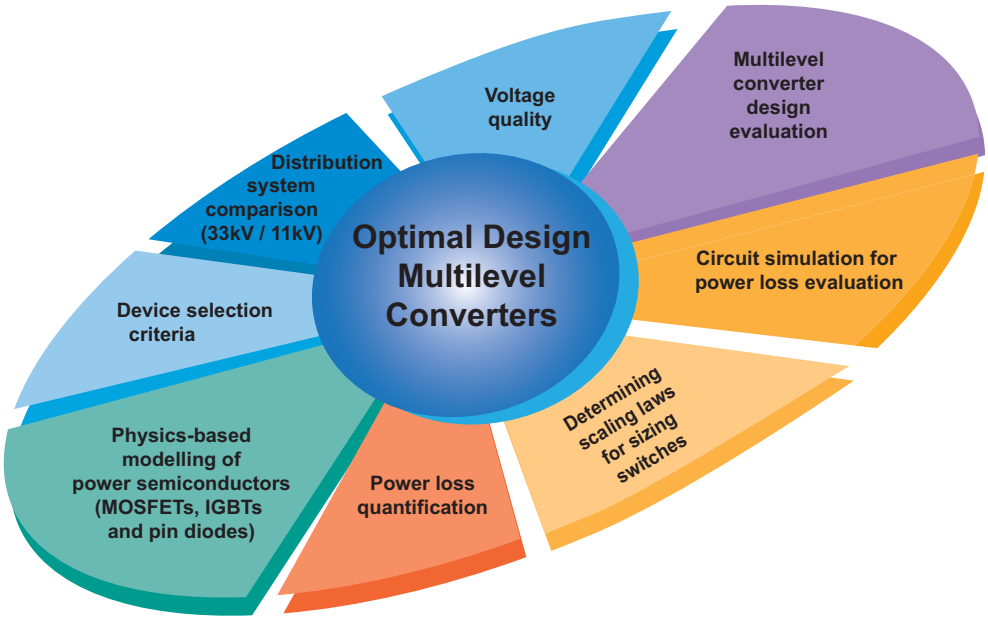


Figure 1.1: Overview of the research work.

1.2 Research motivation and objectives

With the increased demand for energy saving, the high efficiency of power electronics became of greater concern and it has attracted much attention [5]. High performing and cost effective multilevel power converters can greatly enhance the functioning and efficiency of electricity distribution systems. This thesis investigates the efficiency of cascaded multilevel power converters for FACTS (Flexible AC Transmission Systems) [6, 7] applications in distribution networks. The research focus is on the power losses of power semiconductors, which are the major components of such power converters. The overall research intent is to create analytical models to support enhanced understanding of losses in deployment of power semiconductors in electricity systems as a design aid. The purpose is to offer guidelines to the power semiconductor user community for the selection and application of devices. It is hoped that continued dissemination of this research will result in better understanding and cooperation between device manufacturers, power electronic circuit designers and system planners for optimum utilisation of power converters in enhancing the performance of power networks.

The objectives of this thesis are thus four-fold:

- A review of power semiconductors physics used in high density power converters (IGBT technologies, Power MOSFETs and *pin* diodes)

- Formulate scaling laws to quantify conduction losses in power semiconductors to facilitate easy evaluation of losses in circuits by designers
- Comparative evaluation of the available multilevel power converters with detailed emphasis on the cascaded type (topology choice), considering their power losses in distribution systems
- Validate the scaling laws with developed simulation model for cascaded power converters and device manufacturers data

A diagrammatic overview of the research that has fed into this work is presented in Figure 1.1.

It is essential to validate theory with test scenarios that are sufficiently comprehensive and realistic. In this thesis this has been achieved by including manufacturer data in simulations, and by simulating the conduction, switching and reverse recovery losses of actual devices. This enables the generation of solutions and associated practical challenges for reducing the power losses of power converters that can be applied in the real world.

To set this work in context, the rest of this chapter briefly introduces contemporary power quality issues, sources of network disturbance, and their impact on end users to justify a need for FACTS devices. FACTS device technologies are then described. The opportunities presented by enhanced deployment of power semiconductors in these applications are highlighted. This chapter closes by describing the structure of the rest of the thesis.

1.3 Power disruption and its impact on end-users

Power 'quality' means different things to different people. In this work, the term refers to the faithfulness of system supply to the specifications and the standard of received electrical power. The term 'reliability' relates to the continuity of the electric supply. Power supply networks can be disturbed in a variety of ways, as set out in Table 1.1.

Today there is widespread use of microelectronics, computers and high speed communications for control and protection of power systems. Minor disturbances have little impact on the operation of traditional machinery and processes, which are robust in both design and circuitry. In contrast, the electronics involved in sophisticated computer-controlled variable voltage, variable frequency drives are much more sensitive to fluctuations in the

Table 1.1: Typical Power Network Disturbances

SYMPTOM	POSSIBLE CAUSE
Supply outage Complete loss of supply	• Accidents • Planned maintenance • Line faults
Over voltage Long term increase in supply voltage	• Light system loading • Poor voltage regulation
Voltage surge Medium term (ms-seconds) Increase 10-30% in amplitude	• Circuit capacitance • Switching out large loads
Under voltage Long term lowering of the supply loading	• Heavy network loading • Lack of VAR support • Peak demand operation
Voltage sags Medium term dips in the voltage amplitude	• Large loads being switched in • Faults before circuit breakers operate • Large demands on the power supply • Inductive loading
Voltage transients Short duration (ms) impulse voltage spike	• Current surges caused by fast switching • Low fault current trip protection • Non linear switching loads e.g. rectifying units, variable speed drives, power conditioners and converter units • Transmitted noise through the supply system
Current harmonics Periodic waveforms which deform the supply signal	• Increased use of non-linear circuit elements • High frequency switches, computers and fluorescent lighting • Users unaware of signal pollution generated by equipment

quality of supply.

Today, power distribution systems are generally mechanically controlled. When operating signals are transmitted to the distant power circuits where power control action is taken, the switching devices are mechanical so there is little high-speed control. Also, control interventions cannot be activated so frequently as these mechanical devices tend to wear out rapidly compared to solid-static electronic switches. Network operators have learned to survive with this constraint by having to apply a mixture of ingenious techniques to make the system work effectively, but at the price of providing bigger operating margins and redundancies.

Disturbance, even if short in duration, can be extremely expensive. Because of this, studies on power quality have intensified. For example, the cost to US industry of voltage dips is estimated to be US$10 billion per year [8]. The cost of a single severe voltage

Table 1.2: Cost of power disturbances for industrial customers per event in US $

Scenario	Costs (US $)
4 hour outage without notice	74835
1 hour outage without notice	39459
1 hour outage with notice	22973
Voltage sag	7694
Momentary outage	11027

dip to one semiconductor manufacturer in country-regionplaceSingapore was estimated to be US $1 million per event [9]. The magnitude of average loss per event for in the US customers is given in Table 1.2 [10].

Technical barriers to reducing and remediating disturbance, and its economic costs, are forcing a rethink of conventional power systems development philosophies. In these circumstances, work to improve power electronics technology is enabling greater system flexibility, and a consequential improvement in the overall quality of supply follows.

1.4 Power electronic solutions in power networks

System planners consider a range of advanced options to enhance power quality and reliability. They make decisions based not only on technical and cost considerations, but also on return on investment. In many parts of the world, deregulation, re-regulation, restructuring and continued uncertainties of what is yet to come has led utilities to make different investment choices. However, in general, power networks must be economical, meet requirements for system reliability, and provide sufficient capacity to satisfy the needs of customers. In power networks, investment benefits are often reaped on a system wide basis and it is not always clear who should make the investment. With that perspective, the utilisation of power electronics technology folded into the FACTS concept permit utilities to enhance the grid flexibility, and usable capacity at a reasonable cost [11–13].

Various compensation devices are already employed by network operators to provide operational flexibility. The compensators allow properties of the system, such as voltage and frequency, to be kept within defined limits. Compensation equipment may be split into two broad classes; traditional devices [14,15] and FACTS devices [16–19]. Traditional devices are constructed from passive components, mechanical switches and synchronous machines. FACTS devices are constructed from passive components and power electronic

devices.

Power semiconductor devices are at the heart of modern research into power electronic solutions to quality and reliability issues. The evolution of power converters has followed the evolution of power semiconductor devices. The recent development of power semiconductors with improved characteristics in the last decade has provided a basis for FACTS technology uptake [20, 21] in both the transmission and distribution sectors technology and covers a variety of power electronic solutions created to enhance the performance of the traditional grid. The Electric Power Research Institute (EPRI) has helped to pioneer FACTS in transmission systems, and also in the distribution sector under the generic name of Custom Power [22–25].

The application of power electronics to power systems has a long tradition. It started with bulk long distance power transmission through high voltage direct current (HVDC) transmission in 1954 by ASEA (a founding company of ABB) [26, 27]. Some of the power electronic converters, now within the FACTS arena, predate the introduction of the FACTS initiative, such as shunt-connected VAR Compensators (SVCs) for voltage control, are available since 1970. First SVC was demonstrated in Nebraska and commercialised by GE in 1974 and by Westinghouse in Minnesota in 1975.

Figure 1.2 portrays the overall place of FACTS devices in a power network.

1.5 Goals and Challenges for FACTS technologies

FACTS devices allow greater control of power flow and secure loading of transmission lines to levels nearer to their thermal limits, supplementing or offering an alternative to new transmission line construction. Custom power, applicable to distribution systems, focuses on the reliability and quality of power flow. FACTS technologies are enabling, allowing continuous control of active and reactive power flows.

FACTS, despite being a topic of great interest in academia and industry for around a decade, has so far been unable to bring about significant difference to today's power systems with the exception of a few examples where network operators replaced existing equipment with FACTS devices. This low take up is probably because it evolved from the transmission side of the network rather than the distribution side due to the prior knowledge of the engineers working on the devices. Transmission level voltages provide a significant obstacle to implementation whereas distribution level voltages mean that

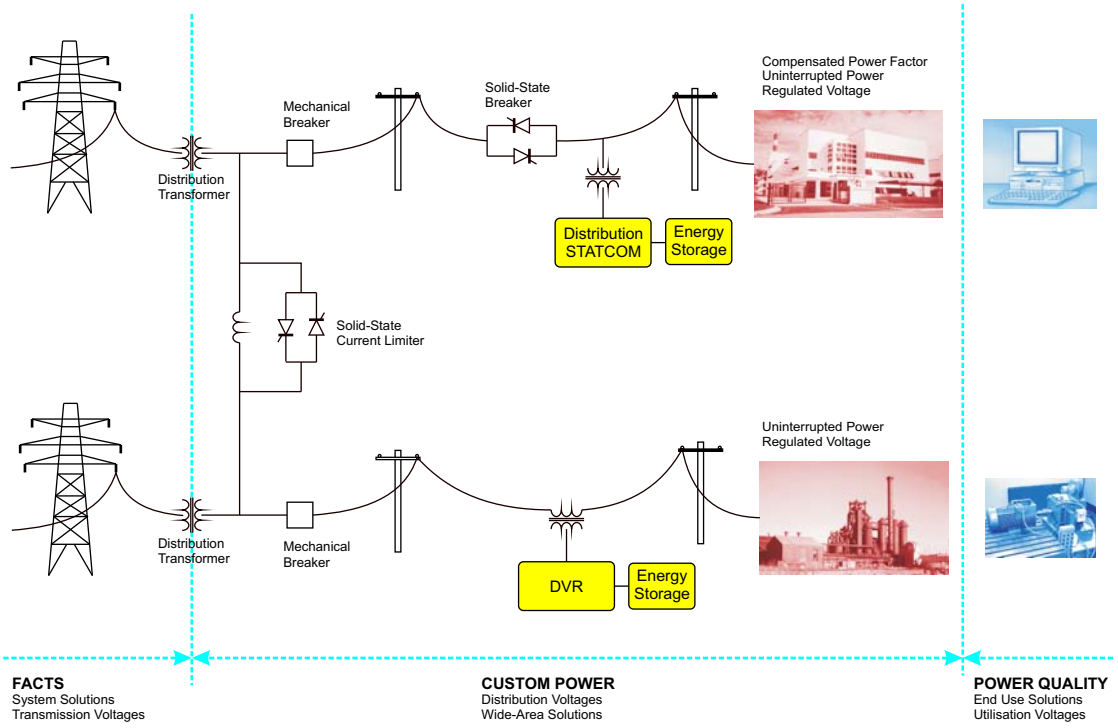


Figure 1.2: Network design using FACTS power electronic converters in transmission and distribution systems.

realistic solutions can be achieved. Secondly the equipment's efficiency and reliability was not very encouraging at high level voltages.

Generally, FACTS devices have the following advantages over traditional ones:

1. **Flexibility**: The influence of a FACTS compensator on a system depends upon the compensator design, its control system and its location. The control system for a FACTS compensator is often easily adaptable [28]. It is also possible to build re-locatable FACTS compensators [29] that can be moved for better utilisation should conditions change.

2. **Better control performance**: FACTS compensators allow for more accurate, rapid and frequent control over transmission system parameters because they use power electronic switches rather than mechanical ones. Power electronic switches are faster and more durable in terms of switching cycles than mechanical switches. Power electronics thereby allows new compensator designs to be developed with improved performance [30, 31].

The potential benefits of FACTS equipment are now widely recognized by the power

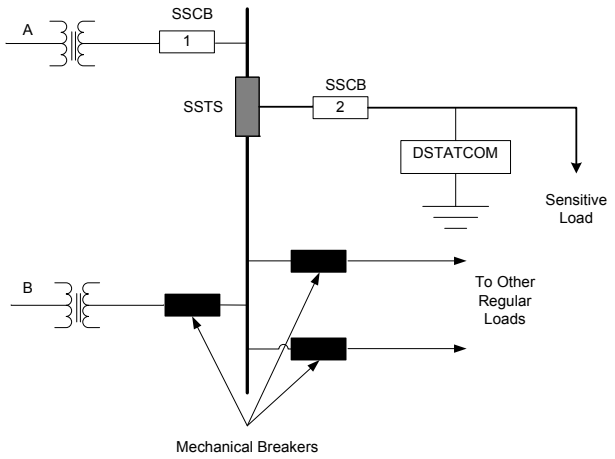


Figure 1.3: A hypothetical distribution system equipped with FACTS devices to protect sensitive loads.

engineering community [32–35]. Voltage source converter (VSC) technology such as the Static Synchronous Compensators (STATCOM) utilising GTOs (Gate Turn Off Thyristors), IGCTs (Insulated Gate Commutated Thyristor), and IGBTs has been used for installing Static Synchronous Compensators (STATCOM) [36–38], such as those in the State of Vermont [39] and California [40]. Unified Power Flow Controllers (UPFC) is another FACTS concept implemented [41–43] that simultaneously provides both shunt and series compensation to a transmission line.

FACTS technologies, applicable to distribution systems, focus on the reliability and quality of power flow. They are two types: *network reconfiguring* and *compensating*. Network reconfiguring equipment can be IGBT or thyristor based. They are usually used for fast current limiting and current breaking during faults. They can also prompt a fast load transfer to an alternate feeder to protect a load from voltage sag/swell or a fault in supplying a feeder. They are mainly solid state current limiter (SSCL), solid state circuit breaker (SSCB) and solid state transfer switches (SSTS). Compensating devices are used for active filtering, load balancing, power factor correction and voltage regulation. The active filters, which eliminate the harmonic currents, can be connected in both shunt and series. The family of compensating devices includes DSTATCOM (Distribution Static Compensator), DVR (Dynamic Voltage Restorer) and UPFC (Unified Power Flow Controller).

One example of how these FACTS devices can be inserted in distribution systems to protect sensitive loads is given in [22] and is shown in Figure 1.3.

This network contains a sensitive load in addition to other regular loads. The loads are

supplied by two independent incoming feeders, A and B. Normally the SSTS is connected such that a sensitive load is supplied by feeder A and other regular loads are supplied by feeder B. Therefore any fault upwards or downwards in feeder B does not affect the sensitive load. For a fault upwards in feeder A, the SSCB 1 opens and the sensitive load is transferred to feeder B in less than a cycle by the SSTS. In the same way, a sensitive load can also be transferred to feeder B in the case of a voltage sag/swell in feeder A. The voltage of the sensitive load can be regulated by a DSTATCOM. A DSTATCOM can eliminate any fluctuation in the load terminal voltage. In the case of a fault at the distribution bus, SSCB 2 opens to isolate the fault quickly and the DSTATCOM supplies power to the load. However this can only be a temporary arrangement as a DSTATCOM has only enough energy to ride through during a short fault. Once the mechanical breakers of feeder B clear the fault and SSCB 2 is closed, the sensitive load starts getting its supply from feeder A. The dc capacitor of the DSTATCOM is then recharged by absorbing power from feeders.

1.6 Attributes of the ideal power semiconductor devices

Power devices characteristics, including most notably conduction losses, switching losses and switching speed, are central to the performance of a power converter. If losses were zero and switching speed was unlimited, devices and everything supporting them inside a converter would minimize and the cost of converters would reduce by orders of magnitude. While this ideal can never be attained, there is much that can be done and is being done to move closer to it.

Future 'ideal' power devices would have the following attributes:

- Minimal power loss in the on-state
- Minimal power loss during switching
- Minimal power loss in the off-state
- Minimal power required to control their operation
- Easy to use
- Inexpensive
- Robust (ability to withstand current overloads and voltage transient)

However in reality, power semiconductor devices do have losses, especially in the on-state, and switching losses. On-state losses are the product of the on-state voltage and

the device on-state current. Switching losses are produced with the turn-on and turn-off of the device itself. Power network losses are usually evaluated as high cost factors. This translates into a desire to reduce semiconductor power devices on-state and switching losses. Designers of power converters, particularly in medium or high voltage applications, are therefore very sensitive to power losses [44]. Reductions in power losses can be achieved by altering the device characteristics themselves or by adjusting deployment on the basis of the device rating.

The requirement to develop a cost effective FACTS technologies, gives focus on the right selection of power semiconductors. This in turn will support the commercialisation of modern power converters under development. However, the voltage and current rating of FACTS equipment place it at the limit of semiconductor technology. The low voltage and high conduction and switching losses of semiconductor devices make targets difficult to achieve using standard converter designs [45]. There are cases which show that important progress towards the consolidation of promising concepts, such as the STATCOM (advanced form of SVC), are gaining ground [46]. However this is far from satisfying the expectations of utility companies, who are forced to reconsider their immediate interest in using them. All these facts mean advanced FACTS devices are still not in wide use. On the other hand, new ideas concerning the development of high power converters involving multilevel chain cell designs have been proposed [47–50]. Investigation into multilevel converter topologies is a fundamental area of the research on FACTS devices.

1.7 Role and importance of power semiconductor devices in FACTS converter development

The cost, performance, and market success of FACTS technology is very much tied to progress in power semiconductor devices and the selection and placement of a device by designers. Suppliers of FACTS technologies should assess and improve the use of their devices. Designers require tools to evaluate the state of device technology and select the right device to reduce the losses.

A FACTS converter is an assembly of valves (with other equipment). Each valve is an assembly of power devices which are used as switches with high V and I capability. These power switches can be either turned-off or turned-on. The device ratings and characteristics and their assembly design has a significant effect on the cost, performance, size, weight and losses of FACTS applications (and indeed all power device applications).

These devices effect the cost and size of all that surrounds them, including transformers and other magnetic equipment, cooling equipment, and operational and maintenance requirements.

Power semiconductor devices are the most multifaceted and delicate element in a power converter. Optimum use of semiconductor devices can not only reduce costs, it can be an asset in terms of reliability, redundancy, and thus investment. Power losses of a compensation device involve a penalty in the return investment of such a device. This cost must be weighed against the benefits of using it. Because of the high cost of compensation devices and the high cost of power losses (when compared to the total operation cost of a transmission system), power losses in high density power converters should be minimal.

The trade-off between converter efficiency and switching frequency has a long record in power electronic design. The higher the required converter efficiency the lower the switching frequency at which power semiconductor devices can be operated. In GTO's for example, increasing the switching frequency from line frequency (50/60Hz) to a few hundred hertz (250 Hz) normally doubles the power losses [51].

1.8 Trends and Improvements

Enhanced design of power semiconductor devices such as IGBTs expands FACTS options and offers a competitive edge for a supplier of FACTS technology to meet a certain specified performance at the lowest evaluated cost. This is covered in greater detail in Chapter 2.

The power converters installed, however, pose demanding challenges for switching devices like IGBTs. Today's conventional HVDC transmissions utilise thyristors with very high power handling capability and excellent reliability records. Converter losses are low and equipment costs are minimised in this comparatively mature technology. Moreover, the converter must sustain different types of overload conditions emanating from various contingencies in the electrical network. The IGBT will in principle experience the same tough requirements on electrical and mechanical performance and robustness as the thyristor does. Modern power systems and the areas of traction, industrial drives, transmission and distribution (T&D) has found a great deal of interest in using IGBTs as power semiconductor switches, ranging from 600V to 6.5kV where they are replacing the conventional GTOs [52–54].

The cost of losses in power semiconductors will become a major challenge for converter manufacturers, with the aim of driving system cost down. This pursuit is quite predictable based on semiconductor manufacturing experience with HVDC thyristors. The high importance of removing the heat rapidly due to the power losses represents a high cost. Device packaging and cooling medium (heat sink) contributes considerably towards the size and weight of the equipment. Bringing IGBTs to level as good as with thyristors will only become possible if the obstacle posed by the famous three-way trade-off between on-state losses, switching losses and Safe Operating Area is overcome. This in turn will necessitate an ever-closer partnership between component and system manufacturers in the quest for new solutions.

1.9 Thesis organisation

The contents of the rest of the thesis are as follows:-

Chapter 2 introduces the power semiconductor device potentials, and the strengths of MOS-bipolar combination devices. The focus is on IGBTs, but its constituent devices such as *pin* diodes and Power MOSFETs are also discussed. Discussion is developed on *pin* diodes and Power MOSFETS, including their channel length, on-resistances, and capacitances effects, on the basis of physical principles of operation. Non-punch through (NPT) and punch through (PT) types of IGBTs are introduced. Their doping profiles and operational differences are described - different modes of operation, such as forward conduction and blocking modes are dealt with. The advantages of a trench-gate IGBT structure, an emerging concept, are then explained. This chapter provides both a retrospective summary and a bird's-eye view of future developments in IGBT technologies.

Chapter 3 presents the vital part of this research. Analytical models are derived to allow circuit designers to choose the right device on the basis of loss estimation. The scaling of losses are investigated in three main power devices (IGBT, MOSFET and *pin* diode) and closed form solutions for device conduction loss are derived based on device ratings and operating conditions. The analysis is first performed assuming an abrupt uniform junction before being extended to derive an optimised doping profile for actual MOSFET designs. An overall IGBT model that is capable of predicting exact on-state characteristics is also furnished. General constants of proportionality developed from these scaling laws are given. These mathematical tools were carefully developed and also validated from manufacturer datasheets following a study of the main classes and

types of devices on the market, and rely on an in depth knowledge of the device physics summarised in Chapter 2.

Chapter 4 presents the concept of multilevel power converters in the context of compensating FACTS technology. This chapter elucidates the diversity of possible multilevel converter topologies. An extensive review suggests that cascaded multilevel topologies are superior to others for reactive power compensation. Cascaded type converters are then evaluated at length and two attractive structures are shortlisted for achieving multiple voltage levels.

Chapter 5 describes the study and modeling of the two kinds of cascaded converters in SIMULINK/PLECS software. A comparative approach is put forward to evaluate them on the basis of power losses in distribution voltages. Then a vast survey of various voltage classes of IGBTs is conducted on the leading market manufacturers. Using manufacturer datasheets, power losses in each type of cascaded converter are quantified using the simulator. A process of optimum device selection for minimum losses is illustrated. This investigation determines the suitability of each IGBT device technology for the two kinds of converter in distribution voltages. Finally, the concept of predicting power losses accurately in such type of converters is provided.

Finally, **Chapter 6** draws together conclusions from this work, and highlights opportunities for future work.

Chapter 2

High-power Semiconductor Devices: Development and Technical Characteristics

2.1 Introduction

Progress in power semiconductors has by-and-large been a step-by-step evolution, with steady improvements being made in operating characteristics, ratings and packaging concepts. The cumulative effect, across some three decades has, however, been quite dramatic. In designing a high power density converter, the smaller package and lower power losses of semiconductor power devices are preferable. The gradual strengthening of mainstream power semiconductors has been complemented by the recent emergence of IGBTs, which are also referred to as conductivity-modulated FETs (COMFETs), insulated gate transistors (IGTs), or bipolar-mode MOSFETs. In the 20 years since commercialisation, IGBTs have already gained a strong foot hold in the marketplace, and power electronic systems have benefited greatly [55].

This work has a focus on the IGBT, which represents an interesting combination of *pin* diode, bipolar transistor, and power DMOS FET properties. The purpose of this chapter is to present a "snapshot" of the technical status of the IGBTs (power MOSFETs and *pin* diodes) used in high density power converters today and to review the device physics in order to facilitate the analysis of the following chapter. Advances in device technology have been made possible by advances in manufacturing techniques and processing technologies. This chapter highlights the aspects of performance that dictate device rating, creating a foundation for the analysis of the scaling of power losses in the next chapter.

2.2 Historical Advances in Power Semiconductor Devices

In 1947 the first major advance in semiconductor development took place when Bardeen, Brattain and Shockley demonstrated the bipolar junction transistor [56], which was followed by Shockley's classic paper on junction diodes and transistors [57]. Later, MOSFETs were demonstrated and advances lead to the evolution of high power devices such as the power MOSFET, and eventually the IGBT by B. Jayant Baliga. Developments of these power switches are shown in Figure 2.1. Hitachi invented what ultimately became the VMOS (V groove metal oxide semiconductor) in 1969, Siliconix introduced its VMOS in 1975, and International Rectifier unveiled the HEXFET in 1978 [58]. The desire for less bulky power supplies brought on these extraordinary developments. In the 1970s, the HP Californian Laboratory came up with the concept MOSFET [59], which became known as D-MOS, "D" standing for double diffused. In fact two separate teams in the HP lab were taking separate routes with D-MOS and the V-MOSFET [60]. The D-MOS team demonstrated it was superior with its lower on-resistance and higher breakdown voltage. B. Jayant Baliga commercialised the IGBT in 1980 time frame [61] and the first paper on IGBTs appeared in 1979 [62].

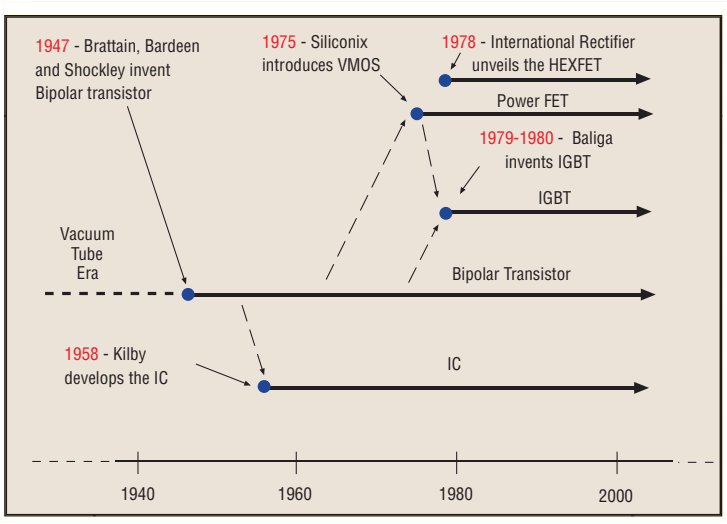


Figure 2.1: Chronology for some discrete power devices. Dotted arrows denote that invention was developed from earlier solid-state devices.

Through the early 1990s advances focused largely on the IGBT due to its superior performance to the MOSFET at high voltages. The latest IGBTs were introduced and promised to be a key component for the uptake of large power electronics systems.

2.3 The performance of Semiconductor Devices available today

A typical power network has a capability of several hundred and thousands of megawatts. The FACTS environment is one which pushes device technology to the limit.

Table 2.1 [63] shows a qualitative comparison of devices available in the market today. The IGBT stands out as having good overall performance (for medium/high voltage applications).

Table 2.1: Power semiconductor performance comparisons
*****Best; *Worst

Performance Parameter	Thyristor	GTO Thyristor	BJT	Power MOSFET	IGBT
Switching speed	**	****	***	*****	****
Switching loss	**	**	***	*****	*****
On-state loss	**	****	****	**	****
Ease of turn-on	*****	***	***	****	****
Ease of turn-off	*	**	**	*****	****
Current rating	*****	****	***	**	***
Voltage rating	*****	***	****	***	****

Figure 2.2 [64] shows ratings of commercially available power semiconductors. In here manufacturers like Eupec (now Infineon) ranked first in the supply of semiconductor market today [65] is used in our investigation along with Mitsubishi and International Rectifier.

The thyristor is a mature device with limited potential for further development. It is manufactured by using more conventional semiconductor technology process steps [66]. Of the controllable devices, the GTO is also proposed for commercial or prototype FACTS converters [67]. The GTO, too, is a conventional device. However, the IGBT is developing very fast and has now reached the power handling capability necessary for FACTS converters [68]. IGBTs are now used successfully at powers higher than 300 MW [69]. The complexity of the snubber (protection circuitry), gate drive requirements, anti-parallel free-wheeling diode are more extensive in GTOs than IGBTs. The speed of IGBT switching and their controllability makes them attractive (refer Table 2.1 and Table 2.2).

Being a transistor, the IGBT does not suffer from some of the problems associated with the regenerative behavior of thyristor structures. Its turn-off safe operating area (SOA)

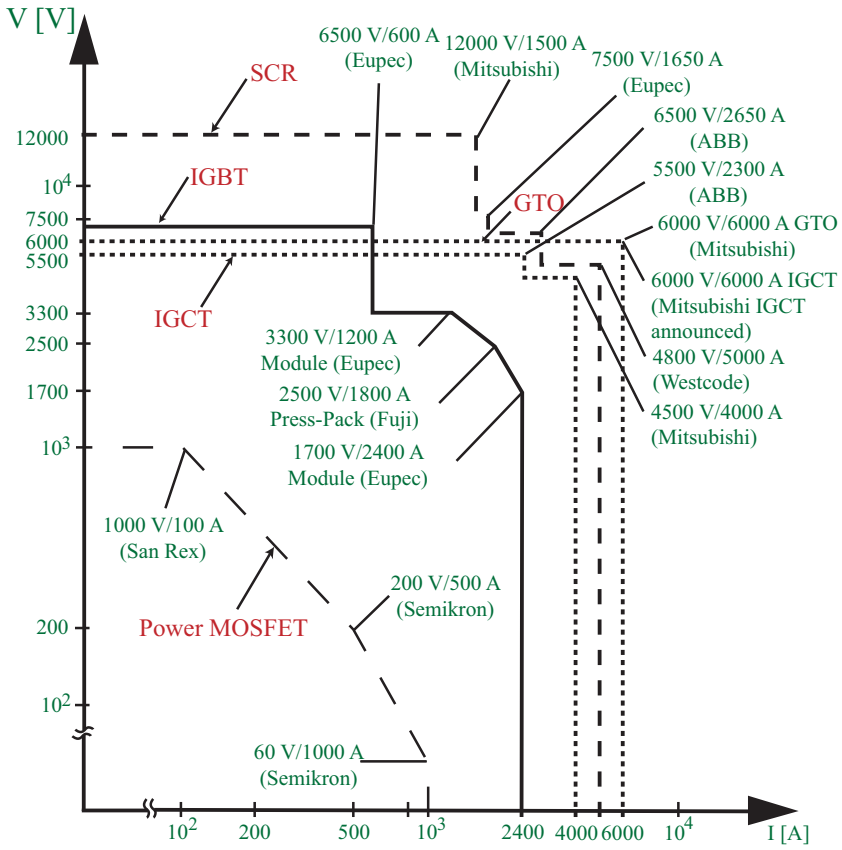


Figure 2.2: Ratings of commercially available power semiconductors [64].

is square [70], which means that theoretically little or no snubber (protection circuitry) is absolutely required. Moreover, the peak current in the on-state is limited by the overall transconductance, unlike thyristors which do not limit the current other than by series resistor. This property means that IGBTs are more able to limit and control the current even under fault conditions [71] (although operating them in such a way is very lossy).

Another important consideration is the ageing of devices. Although in theory, there are a number of mechanisms which could result in ageing of devices, practical operating experience (more than 20 years for diodes and thyristors, and 10 years for GTOs) and a few systematic studies give no indication that there is a deterioration of properly operated devices with time. IGBTs have proved very reliable purely because they are made in a similar way to MOS structures, in which there is vast experience [72].

Table 2.2 gives a summary of important device characteristics resulting from the device physics. It is however, difficult to make exact comparisons because devices with compatible power ratings are simply not available. In this table MCT is known as MOS-

Controlled Thyristor and SITh is Static Induction Thyristor.

Table 2.2: Comparison of device characteristics based on their physics [72]

Characteristics	**Thyristor**	**GTO**	**MCT**	**SITh**	**IGBT**
Forward current	Very high	High	Low	Medium	Medium/High
Forward blocking voltage	(Very) high	(Very) high	Principally high; trade off with max, controllable current	High; function of V_{gate}	Medium/High; expected to increase with further development
Reverse blocking voltage	Very high	Very low optimised switching	Very low for optimised switching	High	Very low
dv/dt in the off-state	Highly sensitive; limitation necessary	Low sensitivity because of carrier extraction through the gate	Less sensitive than GTO because of very efficient emitter shorts	Less sensitive than GTO	Very low sensitivity compared to other devices
Turn-on	Spreading velocity of conducting region – di/dt limited	Cellular therefore relatively fast	Cellular therefore relatively fast	Cellular; very fast	Cellular; very fast
didt capability	Limited	Less sensitive	Less sensitive	High	High
Non repetitive surge current capability	High	Less high	Less high	high	High
Forward voltage drop	Very low	Low	Higher; need of ballast resistors but low theoretical limit	Extremely low	Higher; only one emitter
holding current	Low	Higher	Higher	Very low	No latching
Turn-off losses of device	n/a	High	High	Low	Low
Sensitivity of temperature	Sensitive; current increases with temperature	Sensitive; current increases with temperature	Sensitive; current increases with temperature	Sensitive; current increases with temperature	-ve feedback; current decreases with temperature (NPT-IGBT)
Gate power requirements	Very low	High	Very low	(Very) high	Very low
Process complexity	Standard (base line)	Higher	Extremely high	Extremely high	Higher

2.4 Future Directions in Improved Power Device Performances

The most important future developments in power electronics equipment design are expected in power density elevation. New silicon based semiconductor materials such as silicon carbide [73] are going to be important in developing post-IGBT power device solutions. Silicon has been the dominating semiconductor material until now, but with the emergence of silicon carbide the potential for power density enhancements is significant. It has twice the thermal conductivity of silicon, accompanied with almost no reverse recovery losses, total system losses are greatly reduced, and allows for higher temperature operation [74–76].

Figure 2.3 shows how power density of devices has improved over the past two decades. Power density has been increasing almost linearly, with a near tenfold improvement. This trend will almost certainly continue with the introduction of new materials for power devices, and the use of new components based on IGBT technologies, such as the different families and generations of IPMs (Intelligent Power Module) [77].

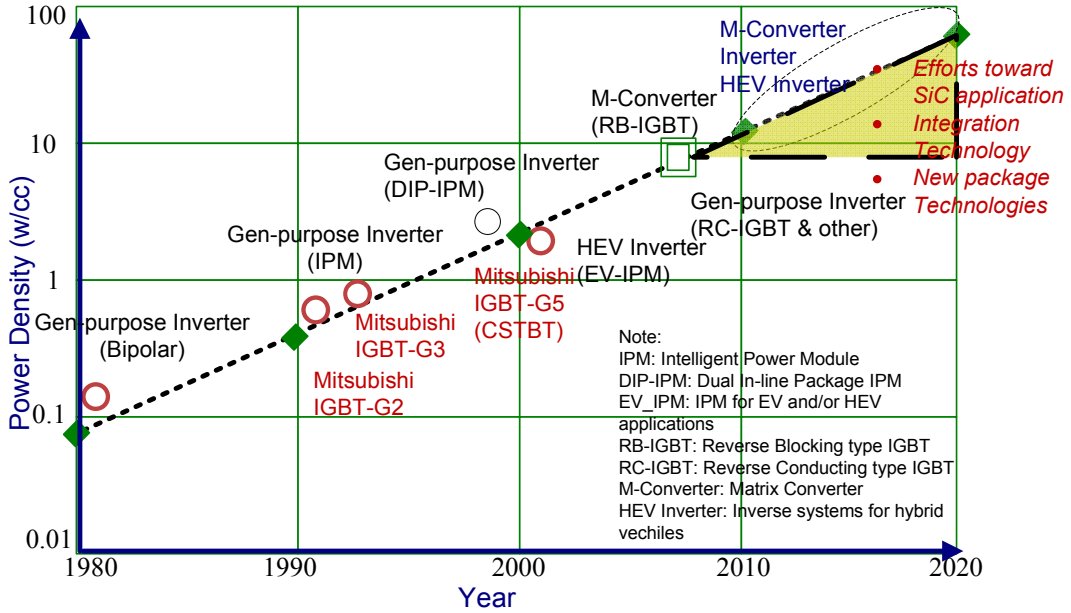


Figure 2.3: Past and projected growth of power density in power electronic system designs [77].

Figure 2.4 [78] maps trends in available IGBT/diode voltage ratings over the last two decades. There is a natural delay between research and product because, shortcomings

in device reliability are observed only after they are used in actual circuits. The traditional development approach for devices focuses mainly on device losses remains the major factor for selecting the optimum point on the technology curve for a given operating frequency and maximum allowable output current. However, as device designs operate close to their limits for a given blocking capability, parameters relating to device and circuit interaction during switching are becoming increasingly vital to achieve good performance with high reliability.

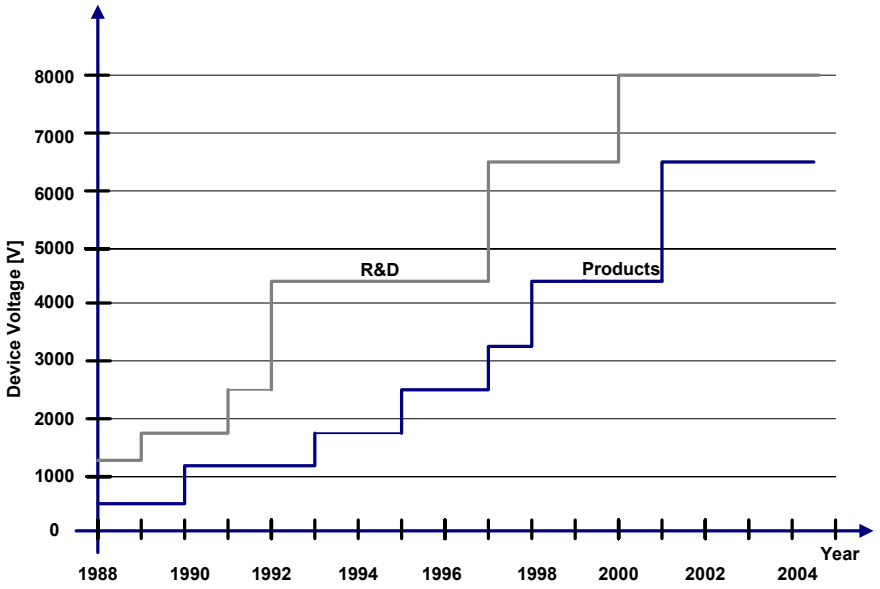


Figure 2.4: IGBT/Diode Voltage evolution [78].

In the coming sections, *pin* diodes and Power MOSFETs are discussed from the device physics view point to provide a context to compare for competing technologies. Along with the outline of IGBT device structures and their electrical characterisations, this forms a basis for developing mathematical tools for scaling the conduction, switching and reverse recovery power losses to device rating follow set out in chapter 3.

2.5 *pin* diodes

Figure 2.5 shows the most basic power *pn* junction [79] in which doping concentration on one side ($p+$) of the junction is very large when compared with the other side (n-). Here we see the stored charge in the depletion region $Q(x)$, maximum electric field $E(x)$ which decreases linearly from its maximum value E_{max} at the junction and the potential distribution $V(x)$.

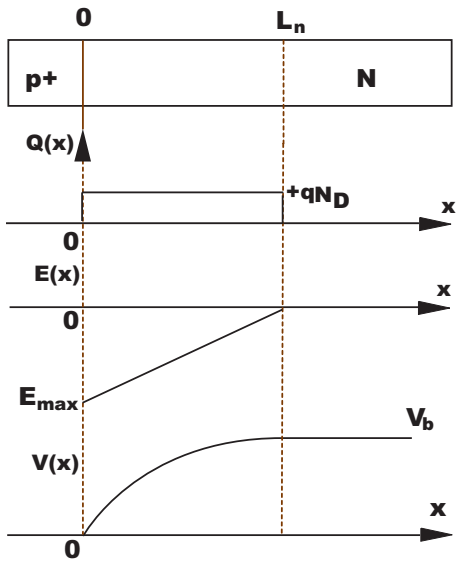


Figure 2.5: Basic *pn* diode - illustration of stored Charge $Q(x)$, Electric field $E(x)$ and potential distribution $V(x)$.

The depletion region width in Figure 2.5 increases with increasing applied bias, and the width is larger for junctions with lower doping concentration on the lightly doped side. Reducing the doping concentration allows the diode to support higher voltages. This is due to the smaller electric field for junctions with lower doping concentrations on the lightly doped side. Thus, the breakdown voltage can be increased by reducing the doping. This is the situation of high voltage power devices which require drift regions with relatively low doping concentrations and larger thicknesses (also refer Figure 3.3 and related explanation).

pin structure diodes are preferable for high voltage applications compared to the normal *pn* junction diodes due to their ability to support higher blocking voltages at low values of on-state loss. They use punch through structure which has a low doping concentration in the *i*-region [80]. The punch through structure is compared with the normal *pn* junction diodes in Figure 2.6. It can be seen here that, the electric field varies more gradually with distance within the lightly doped region due to its lower doping concentration. The result is a rectangular electric field profile which will also be observed in the case of Punch through IGBT in section 2.7.2.

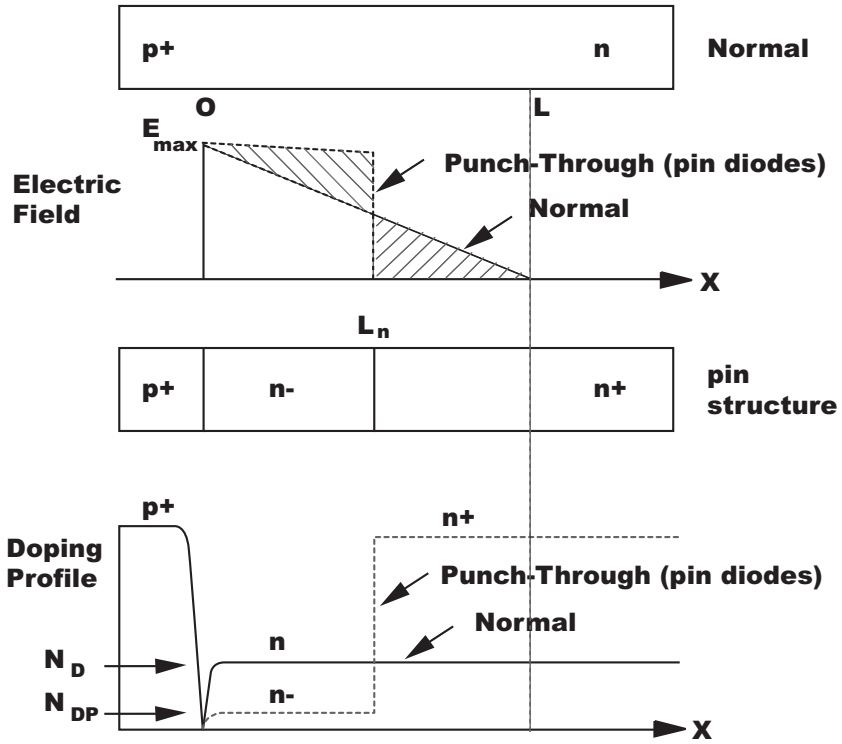


Figure 2.6: Comparison of punch through with normal *pn* junction diode structure.

In a more practical structure for HV diodes such as *pin*, there is injection from both sides of the lightly doped centre: holes from a *p*-emitter and electrons from the *n*-emitter into a lightly doped *n*- (intrinsic region). During on-state current flow, as the current density increases, the injected carrier density also increases and ultimately exceeds the relatively low background doping, N_B of the *n*-base region. Charge neutrality in the *n*-base region requires that the concentrations of holes and electrons become equal. Due to this, the resistance of the *i*-region becomes very small during current flow allowing these diodes to carry a high current density during forward conduction [81]. For this reason, the development of *pin* diode with very high breakdown voltages ranging up to 6500 volts has been possible. This condition is *called high level injection* or referred as *conductivity modulation*. An extremely important effect that allows transport of a high current density through the *pin* rectifier with low on-state voltage drop and maintaining high breakdown voltage rating. The sketch of carrier distribution in a *pin* diode under high level injection conditions is shown in the Figure 2.7, where "bath tub" curve for carrier density is also seen. It should be noted that *pin* diode peak reverse recovery current is typically equal to the forward current [82].

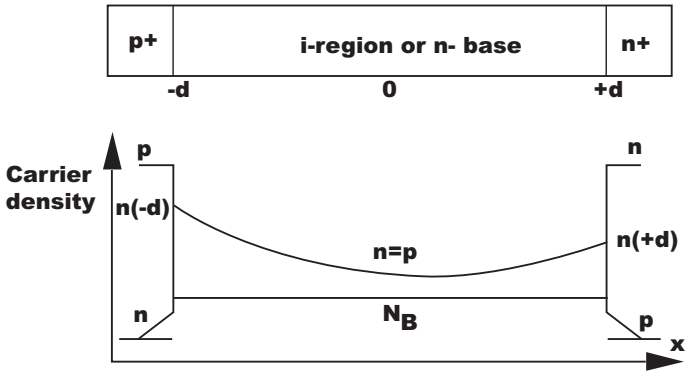


Figure 2.7: Carrier and potential distribution profiles in a *pin* diode under high level injection.

2.6 Power MOSFETs – a technology review

The core difference between power MOSFETs and signal-level field effect transistors [83], is the direction of the current flow through the silicon. It is vertical in power MOSFETs, rather than lateral. Although a power MOSFET works the same way as its low power version, there are number of structural differences. IC MOSFETs have a "planar" structure [84], all device terminals are on one side of the silicon pellet such that current flows parallel to the pellet surface. Power MOSFETs have a vertical structure, with current flow across the pellet, between its power terminals which make contact on opposite sides. This results in enhanced utlisation of the silicon. The first attempts to develop high voltage MOSFETS were performed by redesigning lateral MOSFETS to increase their voltage blocking capability [85].

The impetus to redesign BJTs was their need for large base drive current and limited switching speed capability. This redesign was motivated by the interest in high speed switches for driving piezoelectric devices in medical electronics [86]. The technology developed for these devices was double-diffused MOS (DMOSFET) as illustrated in Figure 2.8(b). At the time, the V-groove MOS (VMOSFET) structure shown in Figure 2.8(a) was also in production. Later studies and modeling revealed that the very high electric fields at the bottom of the V-groove caused significant reduction in the breakdown voltage compared to the DMOS geometry for the same drift layer doping and thickness. The VMOS structure was found to have a higher on-resistance than the DMOS structure for the same breakdown voltage [87]. The DMOS structure is therefore more successful in the market today.

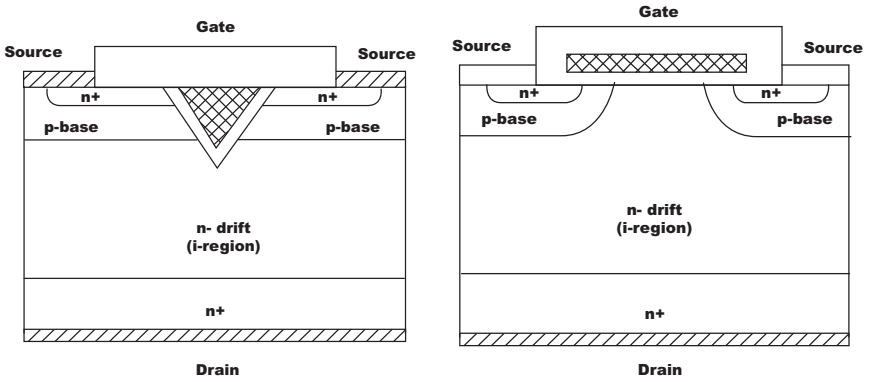


Figure 2.8: (a) The VMOSFET Structure (b) The DMOSFET Structure.

In high frequency applications the power MOSFET was particularly valuable due to its inherently high switching speed (1 to 10ns compared with 1s for bipolar transistors). This high speed capability was the result of current transport occurring via majority carriers alone. This eliminates the large carrier removal times observed in bipolar transistors due to minority carrier transport [88]. However, these merits of the power MOSFET were offset by a higher on-resistance per unit area compared to bipolar devices, especially at higher voltages.

Figure 2.8 shows that the n layer on the bottom constitutes the drain. This layer is actually made up of two layers: an outer $n+$ region (low resistivity) and an inner n- region (high resistivity). The high resistivity region provides voltage blocking capability, while the low resistivity region makes a low resistance contact with the drain surface metal. The gate terminal makes indirect contact with the silicon pellet through an insulating silicon dioxide layer between the silicon surface under the gate (see Figure 2.9). If positive voltage (compared to source) v_{GS} is applied to the gate, the electric field created pulls electrons from the n^+ zone into the p-base immediately near the gate. In this way a "channel" is created linking the source n^+ region and the drain n^- region, and serves as a path for current flow. The value of v_{GS} limits the maximum current that can flow through the channel, without significant voltage drop. In an attempt to increase the current, the drain-to-source voltage V_{DS} increases. There is a steep rise in current initially, but the current eventually reaches a saturation value I_{DS} limited by the channel pinching off, i.e., by v_{GS}. At this point, there is no further noticeable rise of current (saturation state) for that value of v_{GS}. At saturation level, increasing V_{DS} simply causes extra voltage drop across the device (and increased power dissipation). It is therefore desirable that

the current should be limited below the saturation level [89].

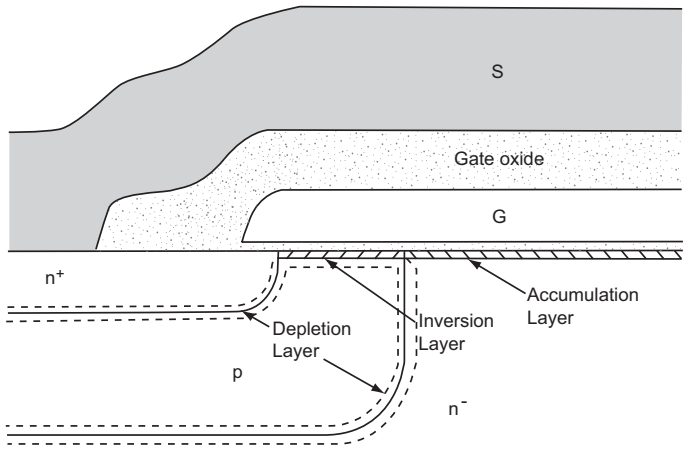


Figure 2.9: A closer look at the depletion layers of the Power MOSFET.

Above threshold voltage v_{TH}, initially for low values of I_{DS}, the device behaves like a resistance, and the current increases linearly with voltage. This is because, once the channel has been created, there is no pn junction in the current path and it can be looked upon as flowing through a series of resistances consisting of the bulk resistance to vertical current flow in the drain n^+ and n^- regions. The MOSFET operates in either the triode region (when the channel is continuous with no pinch-off, resulting in drain current proportional to the channel resistance) or the saturation region (the channel pinches off, resulting in constant I_D) [90].

2.6.1 Power MOSFET on-resistances

It is crucial to know the resistances seen by the flow of current through the power MOSFET. The total on-state resistance $R_{DS(on)}$ of a power MOSFET is made up of several components [91] as shown in Figure 2.10:

$$R_{DS(on)} = R_{CS} + R_{CH} + R_A + R_J + R_D + R_N + +R_{CD} \tag{2.1}$$

Where: R_{CS} = Source diffusion resistance; R_{CH} = Channel resistance; R_A = Accumulation resistance R_J = "JFET" component-resistance of the region between the two body regions;

R_D = Drift region resistance; R_{N+} = Substrate resistance; R_{CD} = Drain electrode resistance

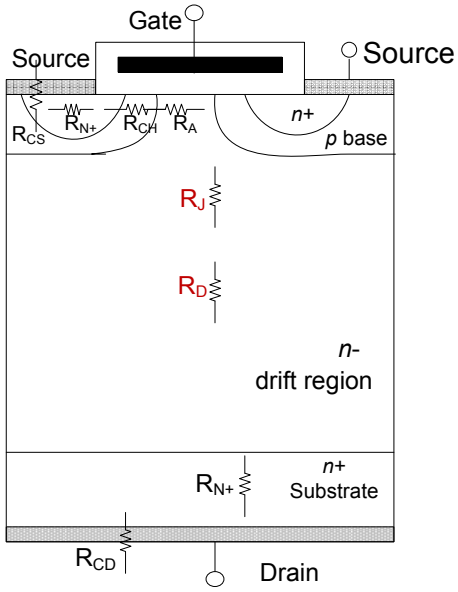


Figure 2.10: Power MOSFET specific on-resistances (R_J and R_D in red are dominating).

Figure 2.11 shows the relative significance of each of the components to $R_{DS(on)}$ over the voltage spectrum. At high voltages the $R_{DS(on)}$ is dominated by the epi-layer, and made up of the drift region resistance plus the JFET resistance. This component is higher in high voltage devices, as the lower background carrier concentration in the intrinsic region results in higher resistivity. The doping of the drift region needs to be reduced in relation to the increased breakdown voltage capability of the device, as discussed previously. The resistance contributed by the channel is pronounced in LV devices and its value depends upon the ratio L_{CH}/Z, the gate oxide thickness (via C_{ox}) and the gate drive voltage, v_{GG}. The channel resistance can be minimised by making its length L_{CH} small, and width Z large. For a high cell density device with good control over the p-base and $n+$ emitter diffusion profiles, it is desirable to keep the channel short without causing reach-through breakdown. The resistance of the drift region between the p-base diffusions is referred to as JFET resistance because the depletion layers resemble that in a junction field effect transistor [92] with the p-base regions acting as the gate regions. The depletion layer extension can then be a significant fraction of the gate length (L_G) leading to a large JFET resistance contribution. Increasing the gate length resolves this problem, but causes poor channel density. To obtain the desired breakdown voltage, it is therefore necessary to increase the doping concentration in the JFET region, while maintaining a lower doping concentration in the drift region.

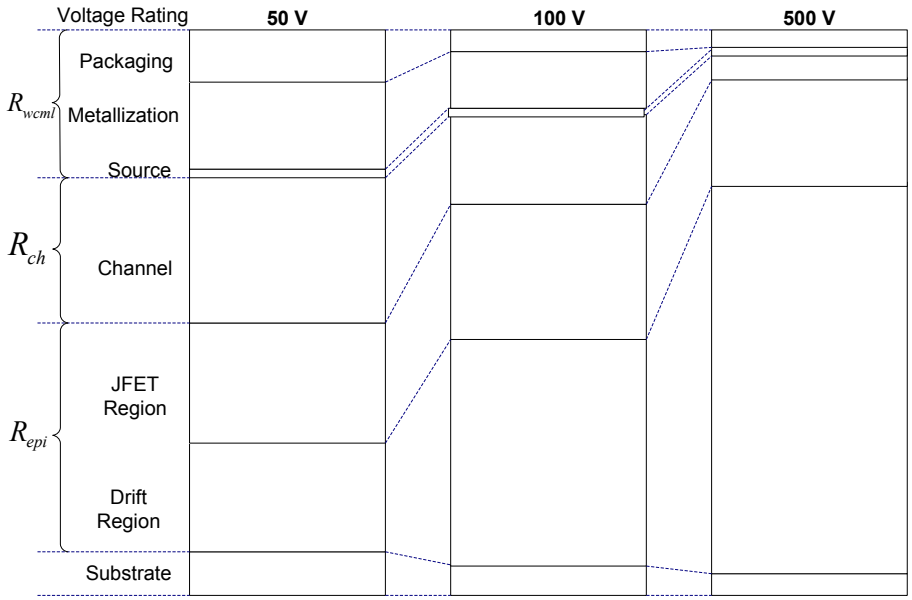


Figure 2.11: Importance of on-resistances with increasing voltage ratings of Power MOSFETs [93].

The dominant components of the on-resistance are the channel resistance, the accumulation layer resistance, the JFET region resistance, and the drift region resistance. For LV power MOSFETs, when the gate length is small, the JFET and drift region resistance becomes large due to the small width through which the current must flow into the channel. At the same time, the accumulation layer resistance becomes small because of the shorter path. The channel and accumulation layer resistances increase as the gate length increases. Concurrently, the resistances of the JFET and drift regions decreases because of an increase in the cross-sectional area of the current flow. It is worth noting that the channel resistance at the optimum gate length is significantly larger than all the other components. This indicates that improvements in performance of the low breakdown voltage can be obtained (a) by increasing the channel density, (b) by reducing the channel length, and (c) by reducing the gate oxide thickness. For HV power MOSFETs, the drift region resistance at the optimum gate length is dominant and other resistance components are much smaller [94]. This demonstrates how important geometry is to the design of power devices.

2.7 Power IGBTs - the best of the MOSFET and BJT

IGBT developments that have reached the marketplace over the past years reflect many relatively small step-by-step evolutionary improvements. The concern throughout the power semiconductor device development has been improving methods to enhance the trade-off between on-state voltage drop and breakdown voltage (BV) characteristics without compromising the switching speed of the device. Literally hundreds of different IGBT types exist, each targeted for a specific mix of parameters needed for the separate application. Manufacturers are forever "tweaking" the process so as to optimise the trade-offs between critical parameters such as on-state voltage drop, gain, safe operating area (SOA) and switching speed. Much of the comparison between power MOSFETs and bipolar's has centered around the fact that the conduction voltage drops of a MOSFET is higher than a bipolar. This is because of a MOSFET's small stored charge (and thus high on-state resistance) which becomes progressively greater as voltage rating increases. This means that the conduction losses of a power MOSFETs when operating near rated current will generally be greater than those of a bipolar, resulting in the dissipation of power in the on-state. The switching losses of a MOSFET are, on the other hand, almost negligible, while the switching losses of a bipolar are often much greater than the conduction losses and becomes progressively larger as frequency increases. The result is that the bipolar is more efficient at low frequency, the MOSFET at high frequency. In addition, control of the MOSFET through the gate is easier than the bipolar base.

The IGBT makes use of both the Power MOSFET and BJT. Its concept integrates the best attributes of both devices for optimal characteristics obtaining the benefits of MOS gate control and bipolar current conduction within the same semiconductor device. This arrangement combines the relatively low conduction placevoltage of the bipolar transistor with the fast switching time of the MOSFET [95].

2.7.1 Current flows in Standard IGBT

The functional integration into monolithic form of the power MOSFET and BJT devices into an IGBT is illustrated in Figure. 2.12.

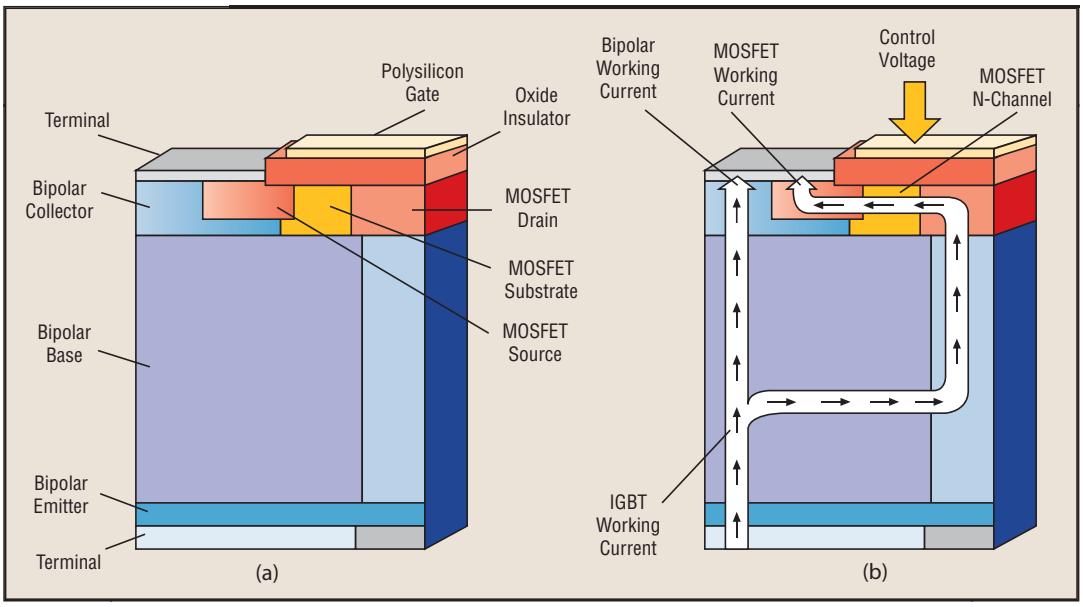


Figure 2.12: The IGBT structure and its equivalent circuit [96].

Conceptually, the MOSFET is used to switch the load current, while the bipolar device is used to conductivity modulate the drift region resistance of the high Voltage MOSFET. This hybrid device can be gated in the same way as a power MOSFET with low on-state resistance because most of the output current is handled by the BJT. Since BJT is low current gain, an equal sized MOSFET is desirable as a driver. When comparing with power MOSFETs the absence of the integral body diode in IGBTs can be viewed as an advantage or perhaps disadvantage, depending upon the application (current requirements and switching speed). An external fast-recovery diode (or a *pin* diode) in the same package is provided for specific applications. IGBTs have significantly reduced silicon area when one looks at the same rated power MOSFETs. Hence by swapping power MOSFETs with IGBTs, efficiency is enhanced and operating cost is lowered.

At turn-on, the MOSFET and the bipolar are driven together. The MOSFET inherently picks up the current during the transitional turn-on interval, because of its faster switching speed. The current then transfers naturally to the bipolar, as this comes into full conduction. At turn-off, base drive is removed from the bipolar, but drive voltage is initially retained on the gate of the MOSFET. Once the current in the bipolar has transferred to the MOSFET, it is switched off [96]. The result of this combined switching arrangement is low conduction losses and low switching losses. The total losses can be considerably lower than for either device by itself.

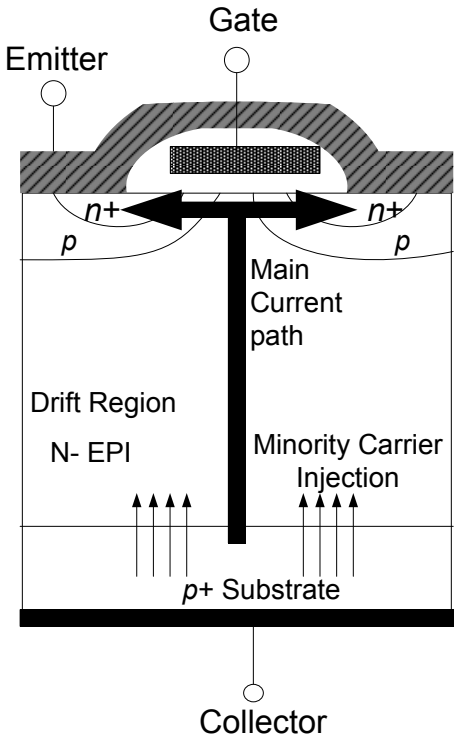


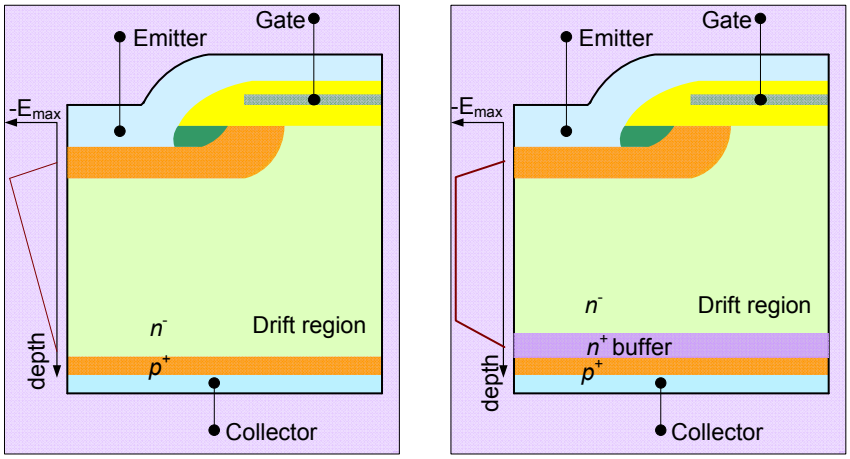
Figure 2.13: Flow of main current through a Standard IGBT Structure.

Figure 2.13 shows when a positive potential is applied to the gate and exceeds the threshold voltage v_{TH} required to invert the MOS region under the gate, an n-channel is formed, which provides a path for electrons to flow into the n-drift region. The pn-junction formed by the n-drift region and p-substrate is forward-biased. The holes starts flowing into the n- region. The additional holes are attracted by the electrons in the drift region to sustain space-charge neutrality and reduce the drift region resistance. As the current density increases, the injected carrier density exceeds the low doping of the base region and becomes much larger than the background doping (typically 100 to 1000 times higher [96]). It is this conductivity modulation of the drift region that means the IGBT has a much greater current density than a power MOSFET, with reduced forward-voltage drop [97].

2.7.2 Two main IGBT structures: Non Punch Through (NPT) and Punch Through

Future development of IGBTs will depend on specific application demands and this requires a detailed understanding of tradeoffs between the different design and operational parameters. IGBT structures have evolved over the years through the continuous demand for lower overall losses and better switching performance. IGBTs have traditionally been

classified under two headings: non-punch through (NPT) and the punch through (PT) type [98, 99]. Non-punch through IGBTs are also referred to as *symmetrical* (equal forward and reverse blocking capability) and punch-through *asymmetrical* IGBTs (less reverse blocking than forward). Figure 2.14a and Figure 2.14b shows the two IGBT structures and their E-field profiles during voltage blocking.



(a) Non-Punch Through (NPT) IGBT (b) PunchThrough (PT)IGBT

Figure 2.14: Two main IGBT technologies.

The cost of fabricating the NPT-IGBT is lower than the PT-IGBT. For example, the NPT-IGBT can be fabricated on a floating zone wafer but the PT-IGBT is fabricated on a wafer by epitaxial growth [100]. There exists a trade-off in conduction and switching losses between these two types because of their different device physics. Table 2.3 lists the salient features of the two types of IGBTs.

Table 2.3: NPT- IGBT versus PT- IGBT

Feature	**NPT-IGBT**	**PT-IGBT**
Process technology and cost-effectiveness	Manufactured using diffusion steps. Less expensive.	Fabricated in a n^- epitaxial wafer. More expensive.
n^- buffer layer and n^- base thickness	Thick n^- base. Does not contain any n^- buffer layer. Space charge spreads across the wide n^- base to withstand the voltage. NPT structure provides bidirectional blocking capabilility. High carrier lifetime yields a low forward drop.	Thin n^- base. Contains an n^- buffer layer. Penetration of depletion region into this layer avoids the use of a broad n^- base. This IGBT has lower reverse blocking capability.
Carrier lifetime in n^- base and conductivity modulation	High Carrier lifetime yields a low forward drop.	Lower lifetime able to provide adequate conductivity modulation as the n^- base is thin. Forward drop is higher & determined by the carrier lifetime in n^- base and injection efficiency of $p+$ substrate.
Collector doping and turn-off time	Collector is lightly doped (p only). Electron back injection from n^- base into p collector gives satisfactory turn-off time.	Heavy doped collector ($p+$). Injection efficiency reduction of the $p+$ substrate by the buffer layer makes its fall time and the current tail shorter.
Turn-off loss	More loss. Slow recombination of stored charge.	Less loss. Faster recombination of stored charge.
Thermal stability	More thermally stable.	Less thermally stable. Thermal run-away occurs at a lower junction temperature.
Short-Circuit failure	More rugged.	Less rugged.

Figures 2.15(a) and (b) aid the comparison of the doping profile and electric field distribution of symmetrical NPT-IGBTs and the asymmetrical PT-IGBTs device. In the asymmetrical IGBT structure, the uniformly doped n^- drift region of the symmetrical IGBT is replaced by a two layer n^- drift region. This alters the electric field distribution as illustrated on the right-hand side of the figures. If the critical electric field for breakdown is assumed to be independent of the n^- drift region doping level, and the n^- drift region doping in n^- base layer is very low, the electric field distribution changes from the triangular case in the symmetrical IGBT to a rectangular case in the asymmetrical structure. Since NPT has a triangular field, so needs a thicker base to block a certain voltage than the PT, which has a flat field profile. Thus, for the same conduction loss, the PT can have carriers of a lower lifetime than the NPT, so PT is faster for a given I/V rating.

Differences between the two devices are observed in the turn-off transient and the on-state voltage drop. The fall in the NPT IGBT current during turn-off has two time stages. The first is the usual expected turn-off time of a MOSFET device. During the second stage the collector current tails off due to the stored charge in the n^- drift region. This is because of the fact that even though the MOS structure quickly switches off, stored carriers are still present in the device and must be removed. Stored charge removal is therefore by recombination within the n^- drift region and gradual flow out of the device. Since it is desirable that the excess carrier lifetime is large, to reduce the on-state voltage drop, tail current duration is long. This results in additional switching losses within the device [101].

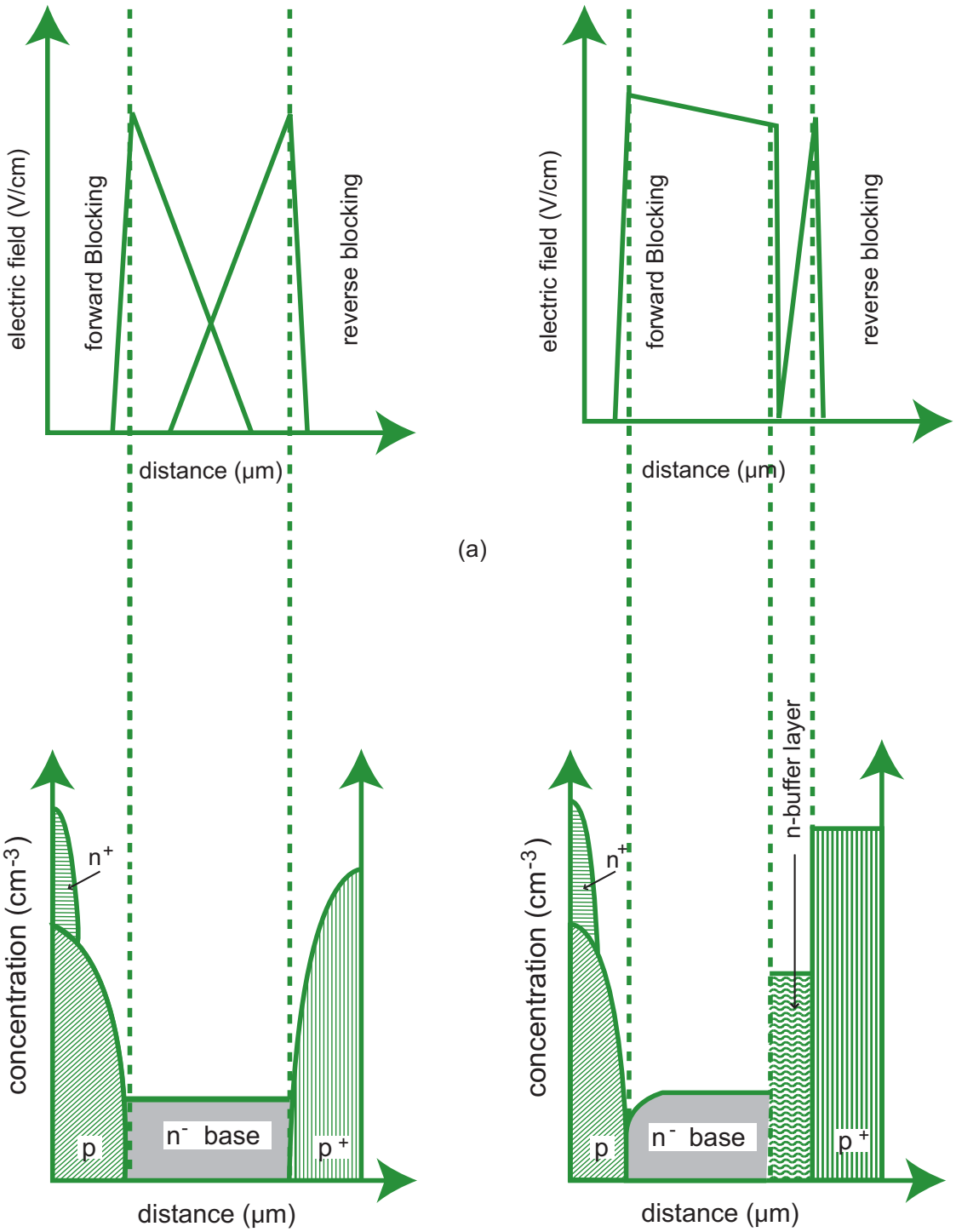


Figure 2.15: NPT IGBT, symmetrical structure (left) and PT IGBT asymmetrical structure (right): a) electric field distribution and b) Doping profile [82].

The added advantage of having the extra $n+$ layer in the PT IGBT is that it enhances the removal of stored charge from the drift region, which acts as a sink for the excess holes and shortens the tail time at turn-off instant. But at the same time, on-state losses can be higher in PT devices because hole injection efficiency from the collector is reduced due to the presence of the $n+$ region. This causes poorer conductivity modulation of the drift region [102].

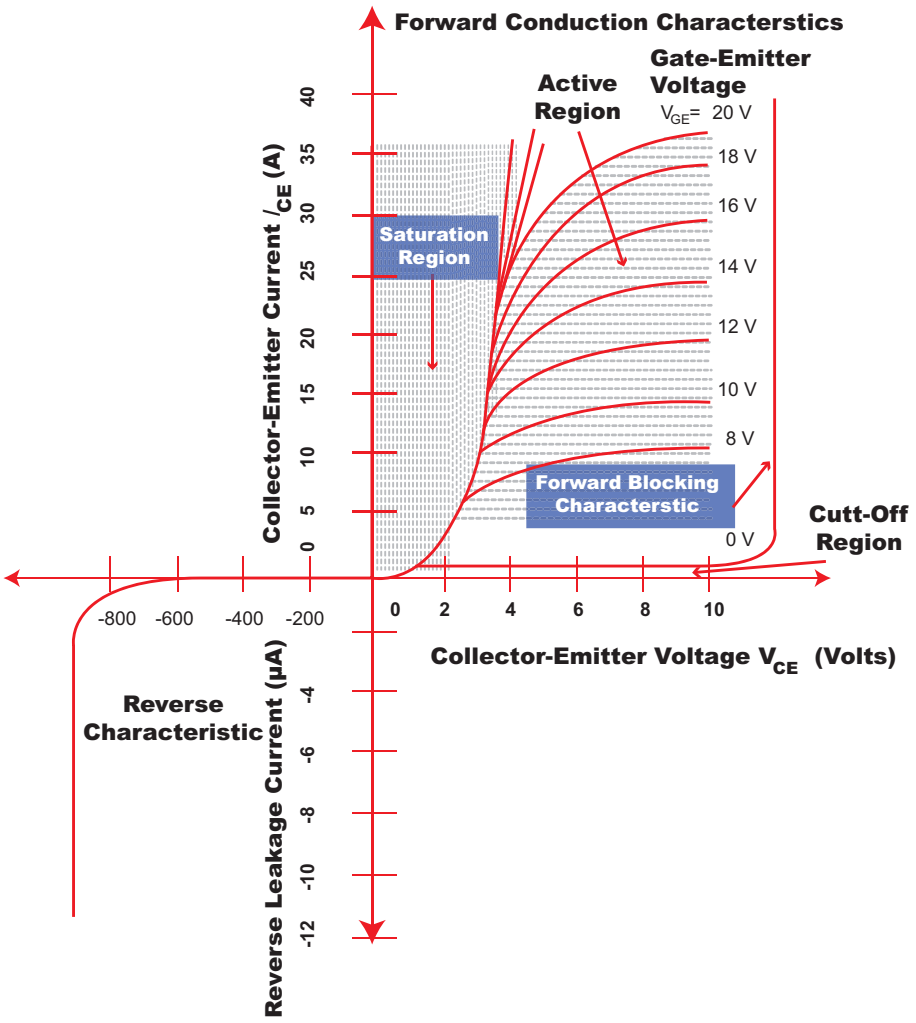


Figure 2.16: Output current-voltage characteristics of a NPT-IGBT [103].

The output characteristics of a NPT-IGBT, as depicted in Figure 2.16, consist of two operating regions. The forward I-V characteristics are plotted in the first quadrant, while the reverse I-V characteristics are plotted in the third quadrant. The IGBT forward characteristics looks similar to the MOSFET. A prominent difference is a one order of magnitude higher current obtained in IGBT compared to a power MOSFET of com-

parable voltage and current rating. Another important distinguishing feature is the approximate 0.7V offset from the origin. The entire IGBT characteristic family is interpreted from the origin by an offset of 0.7V [103]. It may be recalled that replacing the $n+$ substrate of the MOSFET with the $p+$ substrate in the IGBT, adds an extra pn junction in the device. The voltage drop across the IGBT is the sum of the voltage drop across the pn junction, drift region and that across the driving MOSFET. Unlike in a power MOSFET, the voltage drop across the IGBT never falls below the diode threshold. This additional diode drop is shown in the first quadrant characteristics.

2.8 Recent IGBT Design innovations

A promising new IGBT structure available in the market is the Trench-gate structure depicted in Figure 2.17 [104]. This was developed from experience gained from the power MOSFET UMOS gate structure. The Trench gate improves the resistance for the MOS current path by replacing the DMOS structure with a UMOS structure in the IGBT.

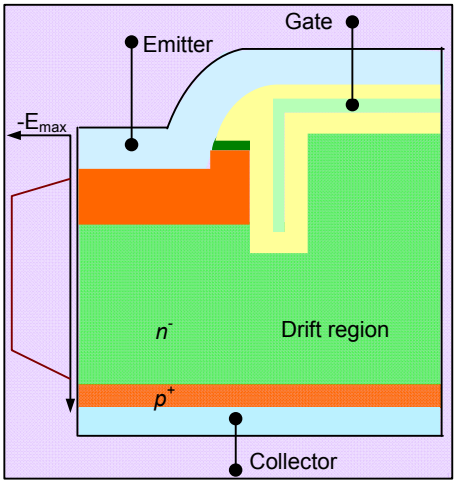


Figure 2.17: Trench Gate NPT IGBT.

The reason for reduced on-resistance in the UMOS structure is the elimination of the JFET resistance contribution and also an increase in the channel density through better use of the silicon wafer. For IGBTs, the voltage drop from the MOSFET portion is a small percentage of the total on-state voltage when the lifetime in the n- drift region is large. As in the case of the power MOSFET, the trench gate must extend below the junction between the P-base region and the n- drift region to form a gate bias induced channel between the $n+$ emitter and the n- drift region. The electron current path faces

no JFET resistance in the UMOS structure. This reduces the overall resistance for the current flow. The MOS channel of a Trench IGBT is rotated by 90° compared with a planar IGBT, as demonstrated in Figure 2.17 [104].

As the safe-operating-area of the UMOS structure has been shown to be superior to that of the DMOS structure, it can be anticipated that trench gate IGBT's will replace DMOS IGBT structures in the future.

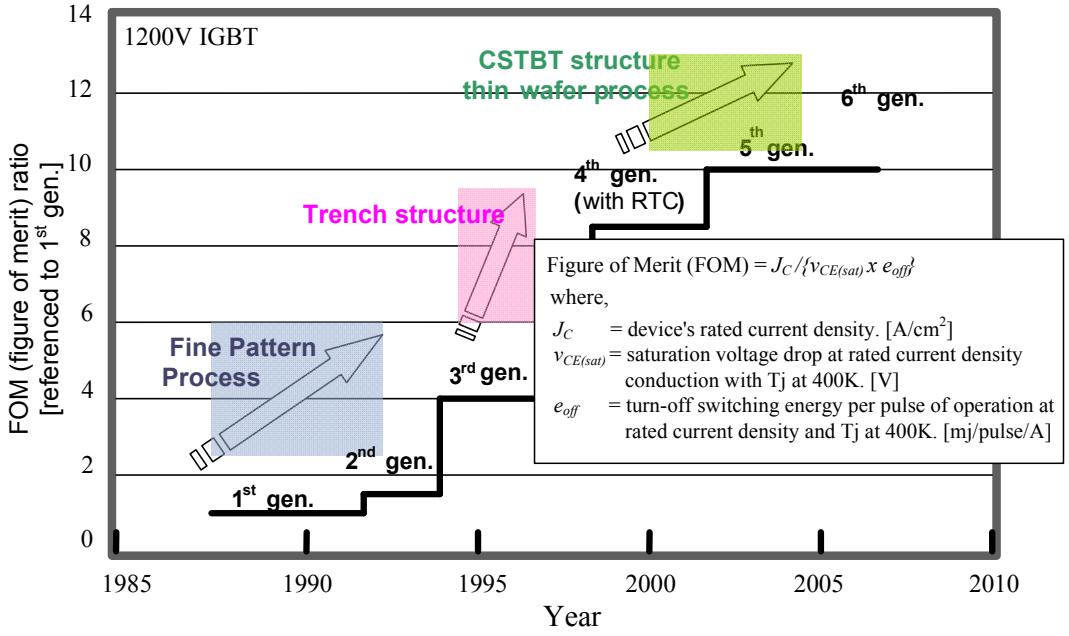


Figure 2.18: The chronograph of IGBTs FOM improvement [105].

To visualise the performance benefits of IGBTs relative to other power devices, a figure-of-merit (FOM) term relating current density, saturation voltage drop and turn-off switching energy has been proposed [106]. This FOM and a chronograph of performance improvements is given in Figure 2.18. The key technologies related to structural aspects of various generations of IGBT devices are also summarised in the diagram. The 1st generation level of IGBT evolution is the planar IGBT, the second is the standard NPT, the third is the PT, and the fourth Trench-gate structures. The Carrier Stored Trench Gate Bipolar Transistor (CSTBT) device cell concept [105] has also helped improve the defined FOM greatly since its debut at the 5^{th} generation level. All this is sketched in Figure 2.19. Along with the improvement of FOM, the various new generations of IGBT structures have also advanced greatly in power loss reduction. This trend has been plotted in comparison with the performance made by an equivalent BJT module in the early 1980s. As depicted, losses are reduced in the new CSTBT and Trench gate IGBT structures.

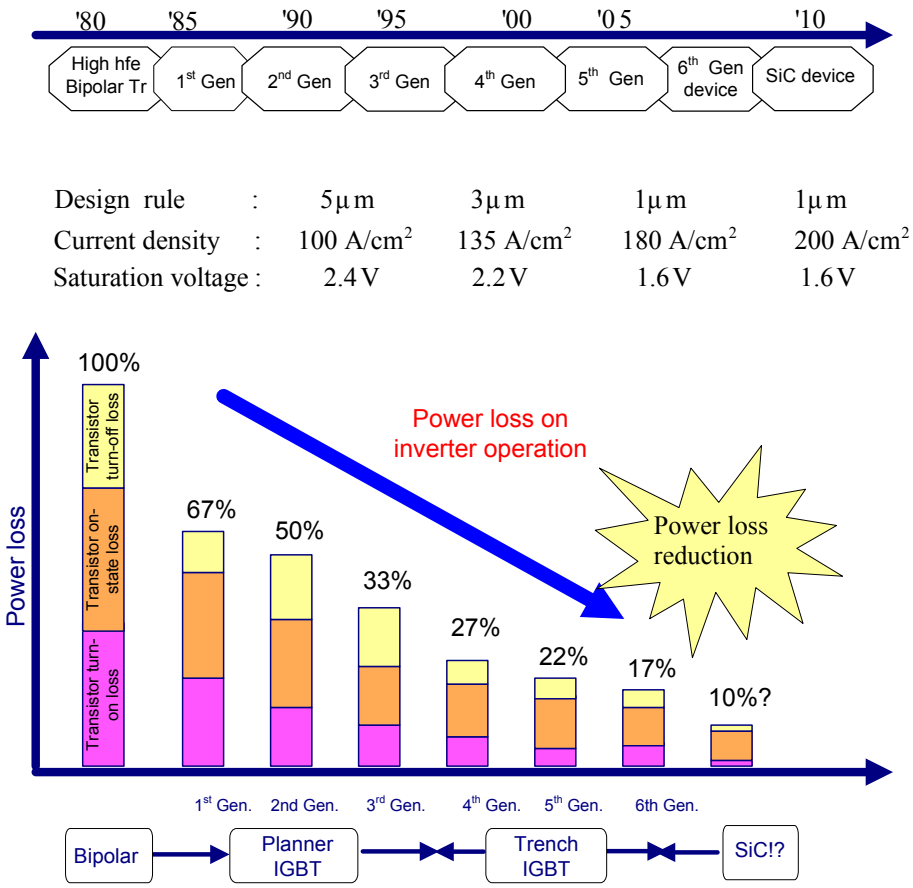


Figure 2.19: Trend of operating losses of various power devices [105]

Today manufacturers focuses on silicon based power semiconductor devices, which are expected to remain workhorse semiconductor power devices. However, work is been done in several places on alternative materials. Silicon based power switching devices are reaching fundamental limits imposed by the low breakdown field of the material. Silicon carbide (SiC) is the most promising alternative material for use in manufacturing as depicted in Figure 2.19, with its higher field characteristic, is a promising choice for high power, high temperature and high frequency applications in the future [107]. However it may well take another five to ten years, before devices for high voltage and high power ratings become available for commercial use. In the meantime, work is continuing on perfecting silicon technology for high power applications.

2.9 Conclusions

This chapter summarises the present technological status of emerging semiconductors, and their historical development. Major research activity has focused on developing new device structures based on MOS-BJT technology integration to increase the power rating. The major families of IGBTs, power MOSFETs, and *pin* diodes were reviewed in terms of their physical structure and its impact on device performance.

IGBTs are fully controllable switches that have carved a niche for themselves in medium to high power applications where BJTs and MOSFETs have limits. However, although IGBTs posses both forward and reverse blocking capabilities, device designers often sacrifice the reverse blocking capability in favour of forward voltage drop with switching speed. The PT IGBT are superior in switching performance [108], but are less optimal from on-state voltage drop and ruggedness viewpoint. Any single IGBT structure is not universally optimal. Making a choice of IGBT is not a straightforward task, and this is explored later in the thesis. Chapter 3 will focus on building analytical models for scaling power losses with the device rating using the physical principles of device operation provided in this chapter. Such understandings are foundational for comparing competing power converters employed in distribution systems using contending IGBT devices structures.

Chapter 3

Scaling of Losses with Device Rating in Power Semiconductor Devices

3.1 Introduction

This chapter establishes important basic analytical relationships for device losses based on fundamental device physics for MOSFETs, *pin* diodes and IGBTs so that power conduction losses can easily be calculated for each device type, given the device's ratings and operating conditions. This allows a circuit designer to determine the predicted losses of a power converter design, and to see how these losses are expected to scale with converter and device rating. Although modern power device technologies are highly complex and many are available in the market, it is still possible to get a good estimation of losses through the use of relatively simple physics-based models, and this is the approach that has been taken here.

3.2 View Point Statement

In consumer and industrial environments, power electronic designers continually strive for improvements in efficiency, size, and weight within stringent cost and manufacturing constraints. Further, device manufacturers prefer to use as little silicon as possible to realise the required voltage and current ratings in order to minimise the cost of their devices. From the power electronic circuit designer's perspective, how much loss to expect in a device with a particular rating when it is operated at or below these ratings

needs to be known in order to determine circuit efficiency and cooling requirements. This means that both manufacturer and circuit designer are interested in the basic scaling laws of the losses of power devices with rating and operating condition.

Power losses can be read from manufacturer data sheets for specific devices, but this does not give an indication of the scaling of losses with ratings or operating conditions. In this chapter, basic equations for losses in 3 devices (MOSFET, *pin* diode and IGBT) have been derived as a function of rated current I_R and blocking voltage V_{block}, operating current I and operating voltage V, based on basic semiconductor physics. The resulting equations have been curve fitted to known, commercially available device data in order to obtain suitable parameters for certain constants in the equations. In this way, the scaling of losses for these 3 device types can easily be seen and absolute loss figures obtained under given operating conditions. Once the scaling laws and constants for individual devices have been determined, these equations can be used in turn to calculate the overall losses in different power converter topologies.

Semiconductor devices will operate normally as long as their temperature does not exceed an upper limit (specified as the temperature of the junctions in the device). When this upper limit is exceeded, the semiconductor stops operating normally and becomes damaged. Therefore, it is necessary to successfully dissipate the generated heat so as to keep the temperature within a specified level.

3.3 Thermal Criteria

The consequence of heat loss in a power semiconductor device is temperature rise. Heat is generated in the silicon wafer due to ohmic losses and carrier recombination. The power losses raises the temperature of the wafer, and the temperature gradient created between the device and the ambient causes heat to flow out of the package. To facilitate the easier flow of heat energy to the atmosphere, it is common practice to mount the package on a heat sink. Heat sinks are made of metal and provide a large surface area from which the heat can pass by convection and radiation to the ambient.

The limiting factors for power semiconductor device operation are ultimately twofold:

- The rate at which the silicon can be cooled with a certain current flowing
- The amount of silicon required to block a given voltage

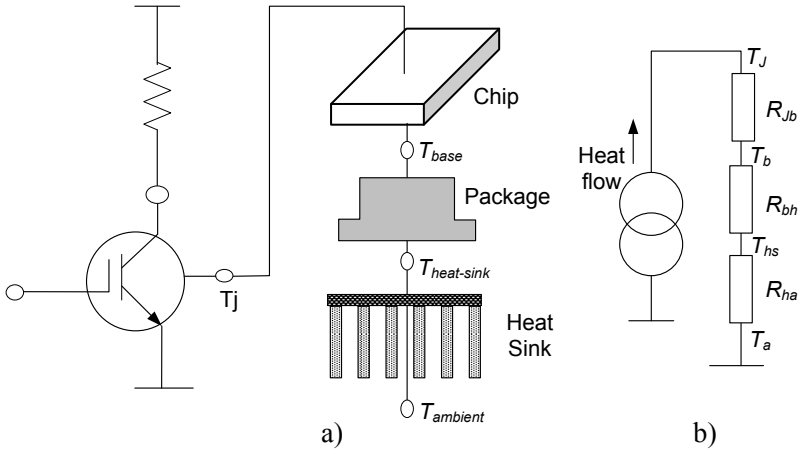


Figure 3.1: Heat flow from the device: a) physical and b) electrical equivalent lumped element model.

The heat energy caused by power losses in a device (Figure 3.1) flows through a series combination of thermal resistances: 1) from the junction (J) to the base (B); 2) from the base (B) to the outer surface of the heat sink (S); 3) from heat sink (S) to the ambient atmosphere (A), which we shall assume to be an external region sufficiently distant from the heat sink, at constant temperature. The thermal resistances R_{Jb} often dominates due to the compact packaging of the device and they cannot be modified by the end user, whereas the resistance between the heat sink and ambient can be modified by the user through choice of heat sink. These resistances are inversely proportional to the contact areas [109].

The basic equation for heat transfer under steady state conditions is:

$$P_d = \frac{\Delta T}{R_{TH}} = \Delta T.h.A \quad [\text{W}] \tag{3.1}$$

Where:

P_d is the rate of heat transfer (*i.e.,* the power dissipated),
ΔT is the temperature difference between regions of heat transfer,
R_{TH} is the thermal resistance,
h is the heat transfer coefficient per unit area and
A is the contact area of the device involved.

In this work to simplify the analysis, it is assumed that the thermal resistance per unit area between the chip and package/base is constant (and thus heat transfer coefficient is constant). As discussed above, this thermal resistance depends on the packaging of the

device and estimation of this thermal resistance is somewhat difficult because of compact interconnection between junction and base/case surfaces. Therefore, for a particular maximum die temperature (which is assumed constant for a silicon based device), and a particular ambient temperature, the maximum power loss from the device is proportional to the silicon area of the device.

$$P_{loss-\max} = k_{P/A} \times Area \tag{3.2}$$

Where $k_{P/A}$ is the maximum heat flow per unit area for a given device type in a particular manufacturing technology/material.

3.4 Scaling Laws for Conduction Losses in Power MOSFET

As illustrated previously in section 2.6.1, the bulk of the power loss in a high voltage power MOSFET is caused by the drift region resistance (which is relatively high due to the low doping required to provide high voltage blocking capability). The drift region is assumed to be a block of silicon, as shown in Figure 3.2. This region is particularly critical to the design of a power MOSFET. Its principal function is to block the full off-state voltage when the device is turned-off. However, this region also has to carry the full forward current in the on-state.

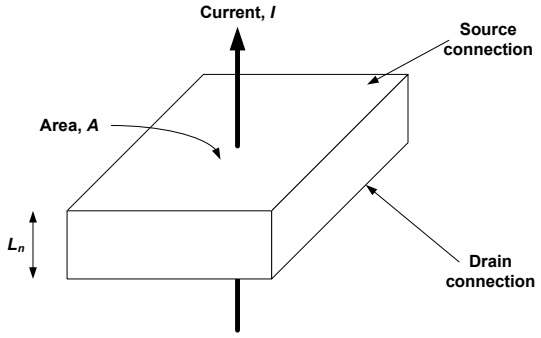


Figure 3.2: Block of silicon as the drift region of the MOSFET.

The conduction power loss, P_{cond}, in this block of silicon is given by:

$$P_{cond} = I^2 R_{DS(on)} = I^2 \frac{\rho_r L_n}{A} \tag{3.3}$$

Where I is the operating current, $R_{DS(on)}$ is the drain-source on-state resistance and the length, L_n, of the drift region determines the voltage, V_{block} that the device will be able to block. Here ρ_r is the resistivity of the drift region (n^- layer) to a uniformly distributed current of majority electrons, and A is the area of the semiconductor.

In the following analysis, simplified expressions are considered for the design of a planar p^+ base/n^- drift region junction (the junction of interest to us). Since proper design requires a measure of the highest voltage that a device can sustain, these equations are further modified for avalanche breakdown conditions. A relationship between V_{block} and on-resistance, assuming a uniform doping profile, is developed to serve as an initial qualitative guide. In practice, devices are optimized through non-uniform doping in the regions of blocking and conduction that minimizes the overall resistance [110]. The analysis is therefore extended to find a relationship between $R_{DS(on)}$ and V_{block} under an optimised doping profile, which is shown to fit well with commercial devices. Consequently, an associated functional relationship between on-state resistance and V_{block} is given. This study will support power conduction loss analysis, a matter to turn to second.

3.4.1 On-Resistance and Blocking Voltage for Uniform Doping Density in n^- drift Layer

The maximum electric field strength, E_{max} in the depletion region is determined by integrating the charge density across the depletion layer. Assuming all the voltage is blocked by the n^- drift region due to the high doping ratio in a p^+ n^- junction, applying Poisson's equation [80] in the n^- region, the electric field strength *E(x)* in the junction, is given by:

$$E(x) = \frac{1}{\varepsilon_o \varepsilon_s} \int_{L_n}^{x} \rho_c(\xi) d\xi \tag{3.4}$$

Where:

ε_o permittivity of free space $[F/m]$
ε_s relative permittivity of silicon [-]
L_n depletion length extended in the n type region $[m]$
ρ_c charge density per unit volume $[m^{-3}]$
x is the distance perpendicular to the junction $[m]$
ξ is a dummy variable

The integration limits in eqn. (3.4) imply the boundary condition $E(L_n) = 0$. ρ_c in the n^- region is equal to $+qN_D$ (-qN_A in the p^+ region), where q is the charge on the electron and N_A, N_D is acceptor, donor concentration or doping density in the p and n region. For a given doping density, the peak value of E, -E_{max}, occurs at the origin of the junction $x = 0$ ($\therefore E(0) = -E_{max}$). Integration of eqn. (3.4) gives the solution:

$$E(x) = \frac{qN_D}{\varepsilon_o \varepsilon_s} (x - L_n) \tag{3.5}$$

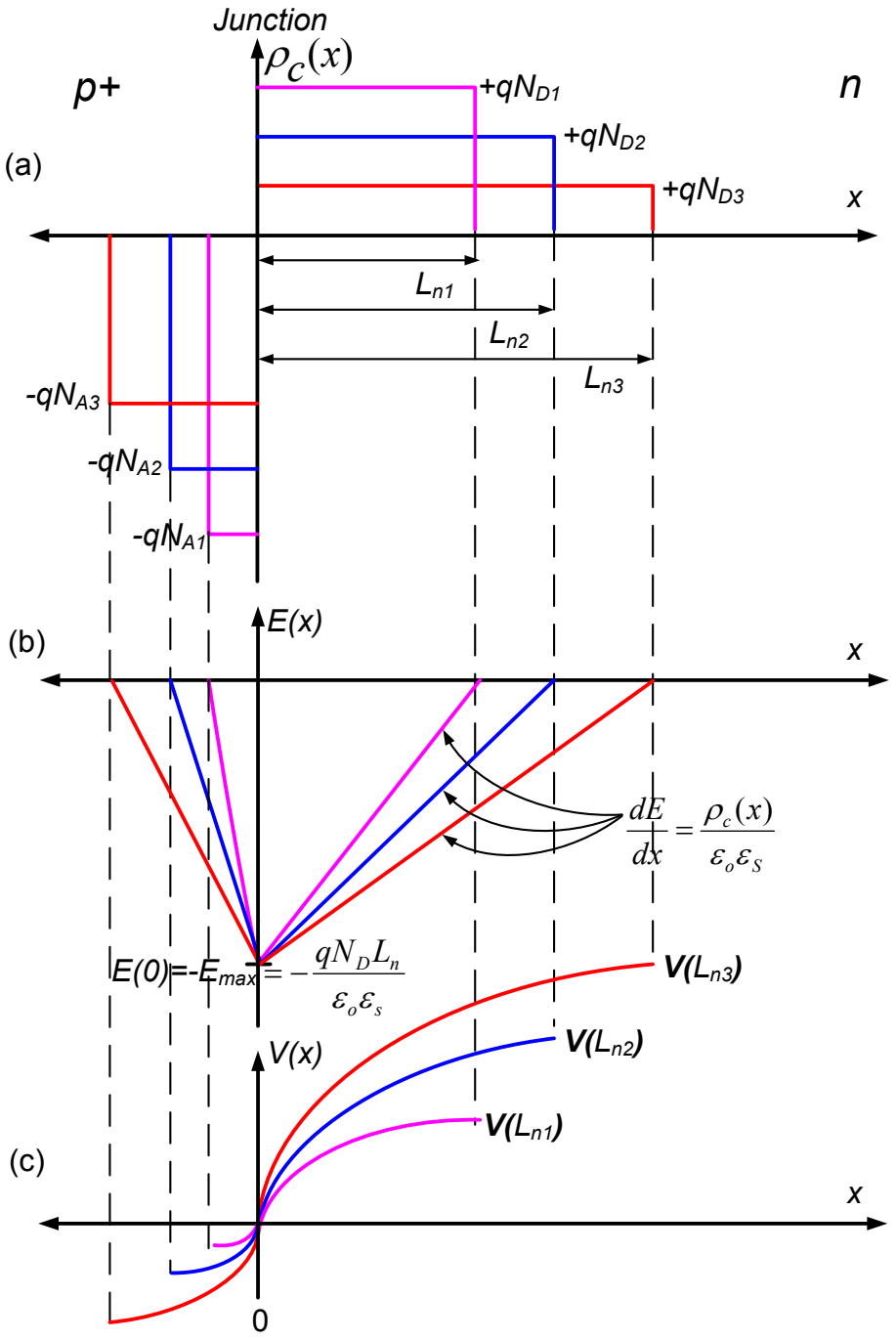


Figure 3.3: The p^+n^- junction for three example cases of uniform doping profile where $N_{D1} > N_{D2} > N_{D3}$: a) net charge concentration in the depletion layer, showing greater extent into the more lightly doped n^-region; b) electric field distribution, same E_{max} limits the breakdown voltage; c) potential variation, shows that low doping (allows longer depletion layer) blocks higher voltages.

Therefore,

$$E_{\max} = \frac{qN_D}{\varepsilon_o \varepsilon_s} L_n \tag{3.6}$$

Integrating eqn. (3.5) gives the voltage *V(x)* at a point x away from the junction (with boundary condition $V(0) = 0$) of:

$$V(x) = -\int E(x)\, dx = -\frac{qN_D}{\varepsilon_o \varepsilon_s} \left(\frac{x^2}{2} - xL_n \right) \tag{3.7}$$

of which the maximum value occurs at $x = L_n$, thus $V(L_n)$ is the blocking voltage given as:

$$V_{block} = \frac{qN_D}{2\varepsilon_o \varepsilon_s} L_n^2 \tag{3.8}$$

and by substituting eqn. (3.6) in eqn. (3.8), we get:

$$V_{block} = \frac{1}{2} E_{\max} L_n \tag{3.9}$$

which is as expected for a triangular field profile. Re-arranging eqn. (3.8) to see the dependence of the depletion region length on V_{block} and N_D yields:

$$L_n = \sqrt{\frac{2\varepsilon_o \varepsilon_s V_{block}}{qN_D}} \tag{3.10}$$

This expression shows that the depletion region length increases with increasing blocking voltage and is larger for the junctions with lower doping concentration. Consequently, reducing the doping concentration allows the junction to support high voltages. From eqn. (3.6) and eqn. (3.9), the maximum electric field can be related to the blocking voltage as:

$$E_{\max} = \sqrt{\frac{2qV_{block}N_D}{\varepsilon_o \varepsilon_S}} \tag{3.11}$$

or,

$$N_D = \frac{E_{\max}^2 \varepsilon_o \varepsilon_S}{2qV_{block}} \tag{3.12}$$

The maximum electric field in the depletion region of a device with specific doping density increases with applied reverse voltage and overall is smaller for junctions with lower doping concentrations. Thus, the blocking voltage can be increased by reducing the doping, if the material critical field strength is assumed to be same in any case.

Differentiating eqn. (3.4) gives:

$$\frac{dE}{dx} = \frac{\rho_c(x)}{\varepsilon_o \varepsilon_s} \tag{3.13}$$

with which we can identify the slope of the $E(x)$ curve. All the ideas presented thus far are clarified in Figure 3.3, where the $\rho_c(x)$, $E(x)$ and $V(x)$ curves are illustrated.

The doping density of the drift region, N_D, and the resistivity, ρ_r, are inversely proportional to one another as:

$$\rho_r = \frac{1}{\mu_e \rho_c} = \frac{1}{\mu_e q N_D} \tag{3.14}$$

where μ_e is the electron mobility. By substituting eqn. (3.12) into eqn. (3.14), it can be shown that:

$$\rho_r = \frac{2V_{block}}{E_{\max}^2 \mu_e \varepsilon_o \varepsilon_s} \tag{3.15}$$

and understood in simple terms that resistivity is proportional to the blocking voltage for a given E_{max}. Using eqns. (3.9) and (3.15) we can therefore show that the resistance of the drift region of area A is given by:

$$RA = \rho_r L_n = \frac{4V_{block}^2}{E_{\max}^3 \mu_e \varepsilon_o \varepsilon_s} \tag{3.16}$$

Thus, we have the result that $RA \propto V_{block}^2$ for a given E_{max}. (RA is the area normalized on-resistance, often referred to as specific on-resistance [111])

The ability of a semiconductor power device to support blocking voltage is actually determined by the onset of avalanche breakdown condition [112], which occurs when the electric field within the device becomes large. At high electric field, due to increased reverse applied voltage, the mobile carriers gain sufficient kinetic energy and generate a cascade of electron-hole pairs in the depletion region, by a multiplicative phenomenon known as impact ionization [113]. This condition is a fundamental limitation to the maximum voltage that the device can block. Therefore, our derived general relationship (3.16), needs further modification which takes into account the device's ultimate breakdown limit. This modification is described next.

A well-established closed form empirical relationship found by evaluating the ionization integral [114] gives the critical depletion region length at the point of breakdown (valid for Si):

$$L_n = 4.75 \times 10^{13} N_D^{-7/8} \tag{3.17}$$

where L_n and N_D are measured in m and m^{-3} respectively. Substituting eqn. (3.17) into eqn. (3.10) gives the relationship between the breakdown voltage and the doping density as:

$$V_{block} = 1.69 \times 10^{18} N_D^{-3/4} \tag{3.18}$$

The maximum electric field, which is critical for the device's breakdown condition, can therefore be obtained by inserting eqn. (3.18) back into eqn. (3.11) to yield:

$$E_{\max} = 71309 N_D^{1/8} \tag{3.19}$$

we now associate the relationship of RA from the product of eqn. (3.14) and eqn. (3.17) as:

$$RA = \rho_r L_n = \frac{4.75 \times 10^{13}}{\mu_e q} \frac{1}{N_D^{15/8}} \tag{3.20}$$

Substituting N_D from eqn. (3.18) in eqn. (3.20) finally gives the relationship of RA and V_{block} as [115]:

$$RA = \rho_r L_n = 5.6 \times 10^{-13} V_{block}^{2.5}\ \Omega\mathrm{m}^2 \tag{3.21}$$

where $\mu_e = 0.135 m^2/Vs$ and $q = 1.6 \times 10^{-19} C$.

So far in this section, the derived RA expressions (eqn. (3.16) and eqn. (3.21)) represent the operation and characteristics of a device with an idealised planar junction (without lateral non-uniformities) and consequently an apparent one-dimensional current flow. This rather simplified analysis nevertheless predicts well the local growth of the depletion layers when uniform doping densities are assumed. The actual devices investigated show lateral non-uniformity of the current distribution due to their non-uniform doping profile (see section 3.4.5). The theory presented so far is therefore too simplified.

Figure 3.4 [93] is a starting point for further explaining why these simplified theoretical relationships (eqn. (3.16) and eqn. (3.21)) do not match the manufacturer's published data of actual devices.

In Figure 3.4, RA versus rated forward-blocking voltage of a MOSFET is compared for commercially available power MOSFETs in curve (a) with the theoretical curves (c) and (d) for derived relationships eqn. (3.16) and eqn. (3.21) respectively (E_{max} is assumed to be critical electric field strength of Si based devices). As can be seen from curve (a) there are significant departures predicted by the simple theory, and in practice, RA increases linearly (slope=1 on log-log scale) with the blocking voltage of the device (up to about

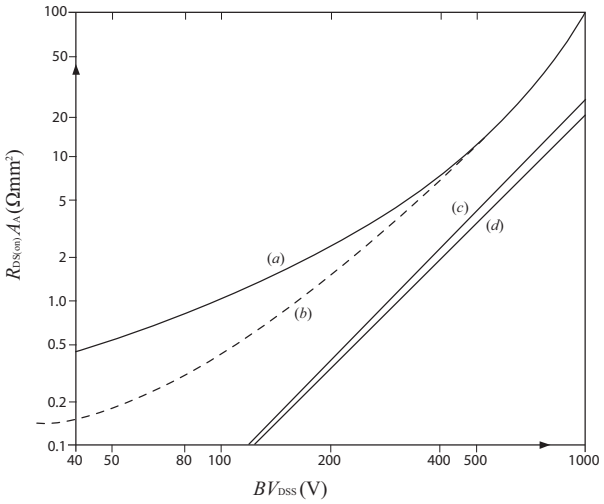


Figure 3.4: MOSFET on-resistance vs breakdown voltage. Values for commercially available devices are compared with the theoretical curves depicting: (a) standard commercial devices (b) typical modern low-voltage devices; (c) eqn. (3.16); (d) eqn. (3.21) [93].

400V) as opposed to having a slope of 2 or 2.5 (case c and d in Figure 3.4). This leads to an important relationship that can be validated in practice:

$$RA = \rho_r L_n \propto V_{block} \tag{3.22}$$

As will become clear, eqn. (3.22) (in comparison to eqns. (3.16) and eqn. (3.21)) takes into account the fact that the doping density, N_D, varies locally in actual devices (and with it so does the local value of resistivity ρ_r). The analysis of devices with non-uniform density is described next.

The expression (3.19) shows that the critical electrical field for breakdown condition is a weak function of the doping concentration. Therefore in the work that follows, E_{max} is assumed to be independent of device doping and geometry [114]. This is only an approximation but making this assumption allows greatly simplified formulae to be derived.

3.4.2 On-Resistance and Blocking Voltage for Optimum Doping Density in n^-drift Layer

It is possible to exploit a device design with non-uniform doping profile such that the overall RA is minimal without losing blocking voltage performance. The principal purpose of the following analysis (from eqn. (3.23) to eqn. (3.58)) is to find a non-uniform optimal profile of N_D, an unknown function $n_D(x)$ so far, which is subsequently used to

explain why RA is proportional to V_{block} in commercially available devices (see curve a of Figure 3.4). The features of the derived $n_D(x)$ to the uniform N_D are then compared. This analysis aims to increase understanding of the fabrication criteria used by manufacturers and to clarify some key underlying physical properties namely the interdependence of N_D and L_n.

Using of Poisson's equation which relates the doping density as a function of distance (x) and electric field strength, $\rho_c = qn_D(x)$, eqn. (3.13) can be written as:

$$\frac{dE}{dx} = \frac{q}{\varepsilon_o \varepsilon_s} n_D\left(x\right) \tag{3.23}$$

where also from eqn. (3.7),

$$E = -\frac{dV}{dx} \tag{3.24}$$

Differentiating eqn. (3.24) again, and equating with eqn. (3.23), we obtain:

$$\frac{dE}{dx} = -\frac{d^2V}{dx^2} = \frac{q}{\varepsilon_o \varepsilon_s} n_D\left(x\right) \tag{3.25}$$

The resistance of a device of area, A is expressed as:

$$RA\left(x\right) = \int_0^x \rho_r(\xi) d\xi \tag{3.26}$$

which implies:

$$\frac{d(RA)}{dx} = \rho_r(x) \tag{3.27}$$

By definition: ρ_r is inversely related to $n_D(x)$ (refer eqn. (3.14)). Re-arranging eqn. (3.25) for $n_D(x)$ and substitute into eqn. (3.27), to obtain:

$$\frac{d(RA)}{dx} = \frac{1}{\mu_e q n_D\left(x\right)} = -\frac{1}{\mu_e \varepsilon_o \varepsilon_s \frac{d^2V}{dx^2}} \tag{3.28}$$

In order to reduce losses, we seek to find an $n_D(x)$ which minimises RA subject to the constraint that V_{block} remains constant. We can therefore consider the minimisation of $RA(L_n) - RA(0)$ subject to $V(L_n) - V(0)(= V_{block})$ remaining constant, say at voltage V_B. Therefore, we wish to minimise the following cost function:

$$U = RA\left(L_n\right) - RA\left(0\right) + \lambda\left(V\left(L_n\right) - V\left(0\right) - V_B\right) \tag{3.29}$$

in which λ is a "Lagrange multiplier". Mathematically, this is equivalent to minimising the following integral:

$$U = \int_0^{L_n} \left(\frac{d\left(RA\right)}{dx} + \lambda \left(\frac{dV}{dx} - \frac{V_B}{L_n} \right) \right) dx \tag{3.30}$$

A similar optimisation procedure has been carried out in [116]. For cost functions having the integral form of eqn. (3.30), λ is normally a function of x because the constraint is prescribed for every value of the independent variable x. In the present case, however, λ has a constant value independent of x because it relates to a constraint in the cost function of eqn. (3.29) which has algebraic form. The integral form of the cost function is simply a reformulation of this algebraic form. Equation (3.30) can be minimized by considering the standard Euler-Lagrange equation [117], however, we have used a simpler approach which allows for a basic hypothesis to be tested: given the independence of λ with x, relationship (3.30) is minimised if there is an $n_D(x)$ for which $RA(x)$ is linearly dependent on $V(x)$, or equivalently

$$\frac{d\,(RA)}{dx} = \gamma \frac{dV}{dx} \tag{3.31}$$

Obviously the optimal solution has to satisfy the constraint equation or equally it has to lie on the "constraint curve" dV/dx. The best that can be achieved is for the $n_D(x)$ which minimises dV/dx to also minimise $d(RA)/dx$ so that the cost in eqn. (3.30) is minimised; remember that only the first term, $d(RA)/dx$, in eqn. (3.30) contributes to the real value of the cost function since the second term, which is multiplied by λ, is by definition zero. These observations lead us to the hypothesis of eqn. (3.31). Substituting eqn. (3.28) into eqn. (3.31) gives:

$$\frac{dV}{dx}\frac{d^2V}{dx^2} = -\frac{1}{\gamma \mu_e \varepsilon_o \varepsilon_s} \tag{3.32}$$

Suppose $\frac{dV}{dx} = g(x)$, then eqn. (3.32) is rewritten as:

$$g\frac{dg}{dx} = \gamma_1 \tag{3.33}$$

Where $\gamma_1 = -\frac{1}{\gamma \mu_e \varepsilon_o \varepsilon_s}$. Integrating eqn. (3.33) becomes:

$$\int g dg = \int \gamma_1 dx \tag{3.34}$$

Which then gives:

$$g(x) = \sqrt{2\gamma_1 x + C} = \frac{dV}{dx} \tag{3.35}$$

This is a proper solution to the optimisation problem and hence our hypothesis in eqn. (3.31) is sufficient. Note that we have additionally solved the optimisation problem using the Euler-Lagrange equation and we have been able to validate our answers, though the additional derivation is not shown here. Differentiating eqn. (3.35) again, and equating with eqn. (3.25), results in

$$\frac{d^2V}{dx^2} = \frac{\gamma_1}{\sqrt{2\gamma_1 x + C}} = -\frac{q}{\varepsilon_o \varepsilon_s} n_D\,(x) \tag{3.36}$$

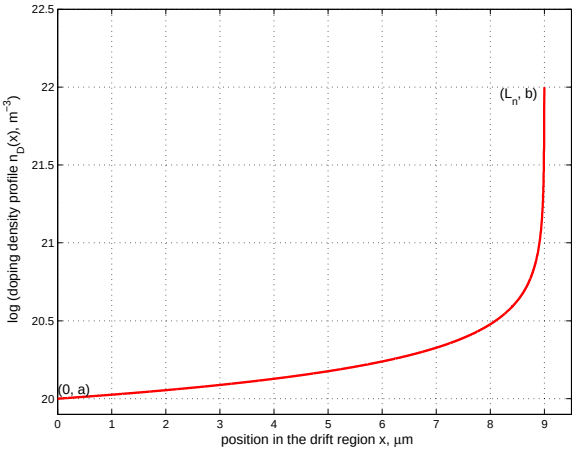


Figure 3.5: Shape of the derived optimum doping density profile $n_D(x)$, according to eqn. (3.38), log-linear scale is used. In this example case: $L_n = 9\mu m$, $a = 1 \times 10^{20} m^{-3}$, $b = 1 \times 10^{22} m^{-3}$and $E_{max} = 1.75 \times 10^7 V/m$ corresponding to a device capable of blocking $100V$.

from which $n_D(x)$ is found to be of the form:

$$n_D(x) = \frac{1}{\sqrt{\gamma_2 x + \gamma_3}} \tag{3.37}$$

in which γ_2 and γ_3 are the constant parameters of $n_D(x)$. The identified doping density profile $n_D(x)$is defined by the set of coordinates $(0, a)$ and (L_n, b), then we evaluate:

$$n_D(0) = a = \frac{1}{\sqrt{\gamma_3}} => \gamma_3 = \frac{1}{a^2}$$

$$n_D(L_n) = b = \frac{1}{\sqrt{\gamma_2 L_n + \gamma_3}} => \gamma_2 L_n + \gamma_3 = \frac{1}{b^2} => \gamma_2 = \frac{\frac{1}{b^2} - \frac{1}{a^2}}{L_n}$$

substitute both γ_2 and γ_3 back into the derived $n_D(x)$ in eqn. (3.37) , finally the form is:

$$\therefore n_D(x) = \frac{1}{\sqrt{\left(\frac{\frac{1}{b^2} - \frac{1}{a^2}}{L_n}\right) x + \frac{1}{a^2}}} \tag{3.38}$$

The shape of $n_D(x)$ for typical values of doping densities is shown in Figure 3.5. In these design calculations, b is equal to $10^{22} m^{-3}$. The choice of this value as well as the influence of parameter b on the optimality of the design will become apparent later. It is clear from the curve that most of the depletion region is at doping density nearly equal to a and this value can be treated as analogous to N_D in the uniform profile case.

It is worth pointing out that the profile defined by eqn. (3.38) can be completely defined by knowledge of the doping density at any two spatial points (along a line). In our analysis we have chosen the two most extreme points in the n^- drift region, at $x = 0$ and $x = L_n$, which are assumed to have doping densities of a and b respectively. Note that the location of $x = 0$ is at the p diffusion/n^- junction and $x = L_n$ is where depletion region ends. Therefore even though parameters a and b are merely the doping densities of the drift region at the boundaries, i.e. $n_D(0)$ and $n_D(L_n)$, they are also enough to define completely the shape of the doping profile everywhere. As we will see at the end of this Section, in order to fully utilise the properties of the optimum profile in a certain region, that region should have a doping density which starts at a defined value a and rises sharply towards infinity at the end boundary. In our case, for practical reasons, we implement a near optimal design by choosing a value for b which is finite but significantly higher than a.

If we now substitute the derived $n_D(x)$ in the well-known electric field expression of eqn. (3.4) and solve with the boundary conditions: $E = 0$ when $x = L_n$, gives:

$$E(x) = \frac{\frac{2q}{\varepsilon_0 \varepsilon_S}\left(\sqrt{\left(\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}\right)x + \frac{1}{a^2}} - \frac{1}{b}\right)}{\left(\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}\right)} \tag{3.39}$$

and integrating to find $V(x)$:

$$V(x) = -\int E(x)\,dx = -\frac{\frac{2q}{\varepsilon_o \varepsilon_S}\left[\frac{\frac{2}{3}\left(\left[\left(\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}\right)x+\frac{1}{a^2}\right]^{3/2} - \frac{1}{a^3}\right)}{\left(\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}\right)} - \frac{x}{b}\right]}{\left(\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}\right)} \tag{3.40}$$

in which the boundary condition $V(0) = 0$ is implied. The overall blocking voltage across the device is:

$$V_{block} = V(L_n) - V(0) \tag{3.41}$$

$$= -\frac{\frac{2q}{\varepsilon_o \varepsilon_S}}{\left(\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}\right)}\left[\frac{\frac{2}{3}\left(\frac{1}{b^3}-\frac{1}{a^3}\right)}{\left(\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}\right)} - \frac{L_n}{b}\right] \tag{3.42}$$

Rewriting eqn. (3.26) and substituting the derived $n_D(x)$ of eqn. (3.38), yields:

$$RA\left(x\right) = \int_0^x \rho_r\left(\xi\right) d\xi = \int_0^x \frac{1}{\mu_e q n_D\left(\xi\right)} d\xi \tag{3.43}$$

$$= \frac{\frac{2}{3}\left(\left[\left(\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}\right)x + \frac{1}{a^2}\right]^{3/2} - \frac{1}{a^3}\right)\frac{1}{\mu_e q}}{\left(\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}\right)}$$

Thus the total RA of the depletion region is $RA(L_n) - RA(0)$ which on simplification, reduces to:

$$RA = \frac{\frac{2}{3}\left(\frac{1}{b^3} - \frac{1}{a^3}\right)\frac{1}{\mu_e q}}{\frac{\frac{1}{b^2}-\frac{1}{a^2}}{L_n}} \tag{3.44}$$

The original requirement was that $RA(x)$ varies linearly with $V(x)$ (see eqn. (3.31)). By observing eqns. (3.40) and (3.43), this requirement is satisfied when $b \to \infty$. This is not practically possible, but a choice of b which is much larger than a is a satisfactory approximation.

3.4.3 Comparison of Uniform and Optimum Doping Density Profile

It is interesting to derive the new relationships between a, E_{max}, V_{block} and RA for the optimised profile. Expressions for these variables can be obtained by taking the $\lim b \to \infty$ as follows. From eqn. (3.38):

$$n_D\left(x\right) = \frac{a}{\sqrt{1 - \frac{x}{L_n}}} \tag{3.45}$$

From eqn. (3.39):

$$E\left(x\right) = -\frac{2q}{\varepsilon_o \varepsilon_s} L_n a \sqrt{1 - \frac{x}{L_n}} \tag{3.46}$$

At $x = 0$:

$$E_{\max} = \frac{2q}{\varepsilon_o \varepsilon_s} L_n a \tag{3.47}$$

And from eqn. (3.40):

$$V\left(x\right) = \frac{2}{3}\frac{2q}{\varepsilon_o \varepsilon_s} L_n^2 a \left[1 - \left(1 - \frac{x}{L_n}\right)^{3/2}\right] \tag{3.48}$$

The blocking voltage is $V(L_n)$,

$$V_{block} = \frac{2}{3}\frac{2q}{\varepsilon_o \varepsilon_s} L_n^2 a \tag{3.49}$$

By substituting eqn. (3.47) in eqn. (3.49), we get the V_{block} expression for optimal device design as:

$$V_{block} = \frac{2}{3} E_{\max} L_n \tag{3.50}$$

A direct comparison of eqn. (3.50) and eqn. (3.9) shows an increase of 33% in the blocking capability of a device with optimum doping profile as compared to one with uniform doping density. This improvement is observed for the same L_n. Using L_n from eqn. (3.50) and substituting back into eqn. (3.47) generates:

$$a = \frac{\varepsilon_o \varepsilon_s E_{\max}^2}{3 q V_{block}} \tag{3.51}$$

which provides a rule for choosing the doping density a parameter for designing a device of a specific blocking capability (for fixed E_{max}). In otherwords parameter a is the minimum doping concentration of the optimised doping profile $n_D(x)$ which determines the voltage rating required.

The corresponding expression for RA can be found from eqn. (3.43):

$$RA\,(x) = \frac{2}{3} \frac{L_n}{\mu_e q a} \left[1 - \left(1 - \frac{x}{L_n} \right)^{3/2} \right] \tag{3.52}$$

The total RA is $RA(L_n) - RA(0)$ which can be evaluated from eqn. (3.52). Further substituting eqns. (3.50) and (3.51) in its solution, gives optimal RA as:

$$(RA)_{Opt} = \frac{4}{3} \frac{L_n^2}{\mu_e \varepsilon_o \varepsilon_s E_{\max}} \tag{3.53}$$

For comparison purposes, RA for uniform doping case can be integrated from eqn. (3.26), then replacing ρ_r from eqn. (3.14) and substituting N_D from eqn. (3.6), yields uniform RA as:

$$(RA)_{Uni} = \frac{L_n}{\mu_e q N_D} \Rightarrow \frac{L_n^2}{\mu_e \varepsilon_o \varepsilon_s E_{\max}} \tag{3.54}$$

At first glance, the RA expressions (3.53) and (3.54) show an increase of optimized RA by 33% for the same L_n. This does not mean that the optimised profile is poor, because the L_n for the same V_{block} also needs to be taken into account. Thus if we rewrite eqns. (3.53) and (3.54) as functions of V_{block} we subsequently get:

$$(RA)_{Uni} = \frac{4 V_{block}^2}{\mu_e \varepsilon_o \varepsilon_s {E_{\max}}^3} \tag{3.55}$$

and

$$(RA)_{Opt} = \frac{3 V_{block}^2}{\mu_e \varepsilon_o \varepsilon_s {E_{\max}}^3} \tag{3.56}$$

It is then seen that the derived optimal doping profile gives a reduced RA by 25% for same voltage blocking. Note that this RA relation concerns the region of the device that is predominantly used for blocking. A different relation applies to the conduction region and we will derive this in the next section.

An illustration of the uniform doping and its effect on electric field distribution and acquired blocking voltage was depicted in Figure 3.3. A comparison of a uniform profile with the optimum doping profile $n_D(x)$ for various device designs is provided in Figure 3.6-3.9. Devices ranging from 50V to 350V are considered. In the results presented, E_{max} is assumed to be at $1.75 \times 10^7 V/m$. This value is typical for Si based devices [82]. Also note that the values used for the material properties constants correspond to a temperature of 125^oC for all subsequent results in this Chapter.

From Figure 3.6, it is evident that as the V_{block} increases the depletion region length L_n is increased in both uniform and non-uniform profiles (see eqns. (3.9) and (3.50), and reduced doping concentration enables a device to block larger voltage (eqn. (3.12) and (3.51)).

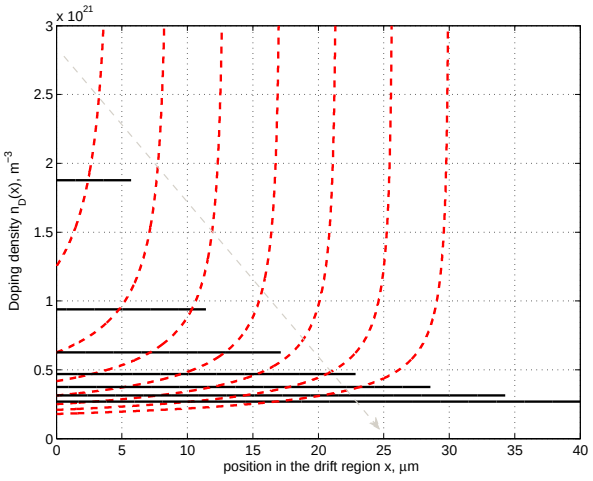


Figure 3.6: Uniform (solid lines) and optimum (dashed lines) doping density $n_D(x)$ profiles, for a range of blocking voltages. 7 designs at 50V, 100V, 150V, 200V, 250V, 300V, 350V are shown, increasing in the direction of the arrow. Equations (3.12) and (3.9) are used to plot uniform doping density whereas eqn. (3.38) is used with ($b = 10^{22}$ and a is given by eqn. (3.51) to plot the optimum profiles.

In Figure 3.7 the electric field distributions for the devices presented in Figure 3.6, are shown.

The ability of a device to block maximum voltage can be understood by examining

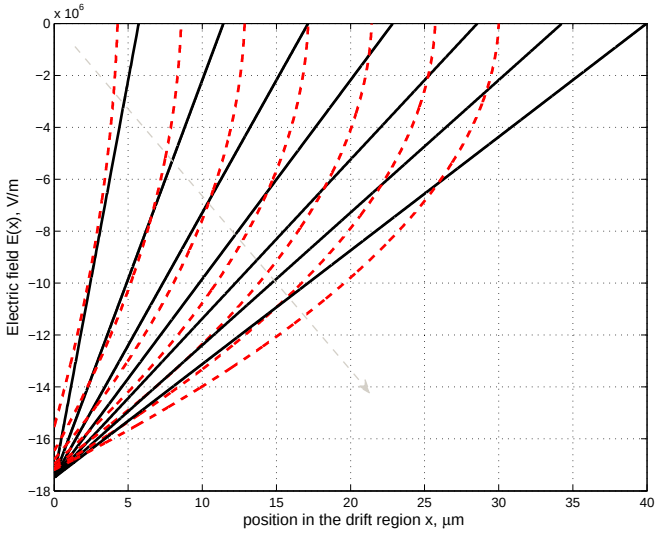


Figure 3.7: Electric field distribution for the uniform (solid lines, eqn. (3.5)) and optimum doping (dashed lines, eqn. (3.39)) for Figure 3.6 devices. $E_{max} = 1.75 \times 10^7 V/m$. Note that this plot relates to the devices presented Figure 3.6.

Figure 3.7. This is observed both in terms of the formation of electric fields and associated length of drift regions by underlying doping concentrations. As the applied voltage is increased the depletion region grows in agreement with constant field slope, whose point of intersection with the E axis is the peak value of E (from both the p and n sides, here p is ignored, due to its negligible influence on blocking capability). This peak value increases until it reaches E_{max} at which point the horizontal point of intersection of the electric field curve is at its largest value. This signifies the maximum depletion region length L_n for a certain V_{block}.

The gradient of the field is proportional to the doping density and therefore devices with lower doping densities have a lower electric field gradient, which intersects the horizontal axis at larger distances, implying that L_n in those devices is larger. Larger L_n is associated with higher blocking capability. Another noteworthy aspect of Figure 3.7 is that E_{max} for the devices with optimised doping profile is reached at a smaller L_n for the same V_{block}, compared to a device of uniform doping profile.

It may therefore be expected that for a desired V_{block}, the optimised doping profile will have reduced resistance, and this will be observed shortly.

Figure 3.8 illustrates the variation of the voltage along the depletion region for the devices presented in Figure 3.6. As V_{block} increases, the depletion region length L_n increases but at a smaller extent compared to the uniform profiles, as seen previously. In other words,

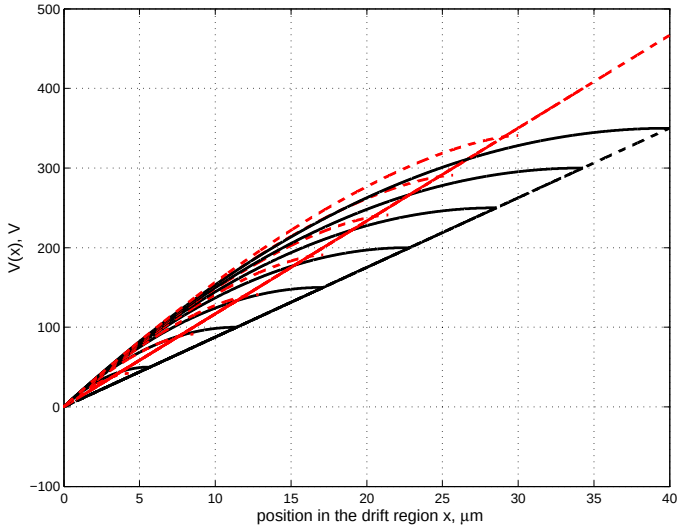


Figure 3.8: Plot of voltage variation for both uniform (solid lines) and optimum doping (dashed lines) profiles from eqns. (3.7) and (3.40) respectively. The locus of final values (L_n, V_{block}) of both solid and dashed curves are plotted from eqn. (3.9) and (3.50) respectively. It can be noted that the device with optimum profile blocks same voltage, but at a reduced L_n. This difference becomes larger on higher voltage ratings. Note that this plot relates to the devices presented in Figure 3.6.

for the same L_n it is possible to block more voltage with the optimised profile. This difference becomes more pronounced at higher voltage ratings. As predicted by eqns. (3.9) and (3.50) the locus of L_n and V_{block} for each family of doping profiles lies on a straight line, with the gradient of the line being larger in the optimised profile case.

Figure 3.9 shows the dependence of RA with device length at different blocking voltages. For uniform doping densities RA varies linearly with distance (eqn. (3.26)) while for optimised doping densities it varies according to expression (3.43). The locus of L_n, $RA(L_n)$ values (using eqn. (3.53) and eqn. (3.54)) is drawn for each family and it can be seen that they are both of quadratic form. In summary, for the same L_n the optimised device has larger RA but will also block more voltage, and optimised profiles produce smaller $RA(L_n)$ values at the same blocking capability.

3.4.4 On-resistance and Blocking Voltage in Actual Devices

As discussed previously with reference to Figure 3.4, commercially available power MOSFETs are dominated by two-dimensional current flow with non-uniform doping density, in which the carriers travel along the surface/accumulation layer and then flow into the JFET/drift region. Basically, the regions between the p-diffusions and the gate areas act

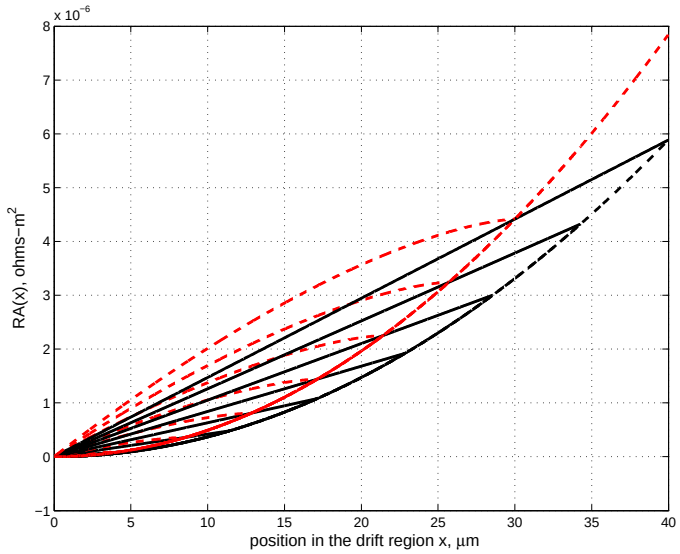


Figure 3.9: Variation of RA with length for both uniform (solid lines) and optimum (dashed lines) doping cases. Eqn. (3.26) is used to simulate uniform cases, and its locus formed by L_n values for each device is plotted using eqn. (3.54). For the optimised cases eqn. (3.43) is used and its locus is drawn with the help of eqn. (3.53).

as a throat. They constrict the drain current as the depletion layers tend to expand on either side beneath the gate, as illustrated in Figure 3.10. This effect is offset by increasing the doping concentration in the drain throat area. This improves the conductivity and decreases the width of the depletion layer thereby increasing the cross sectional area available for conduction, as shown in Figure 3.11.

This is the reason why in the optimum design, the doping concentration has a peak value in the accumulation/JFET region of the order of $10^{22}m^{-3}$. Then it becomes gradually lighter into the main n^- drift region ($5 \times 10^{20}m^{-3}$) [93] to achieve maximum blocking capability. These features are portrayed in Figure 3.12. Note that the channel (p regions) are located close to the corner of the blue region where the drift region doping density has its lowest value. They are not shown in this picture because they are much smaller in scale than the dimensions involved in this figure.

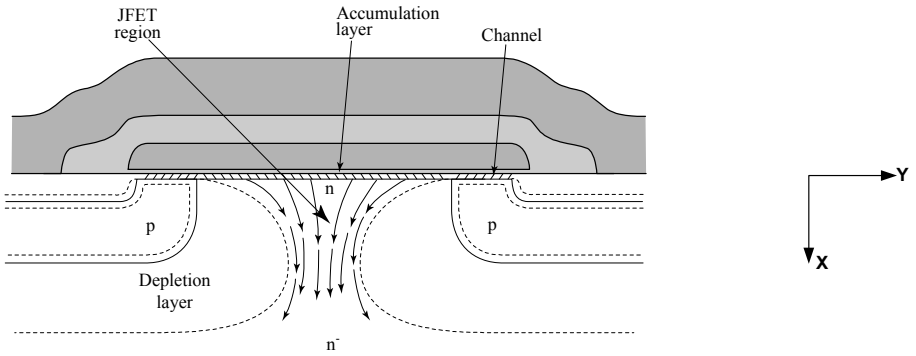


Figure 3.10: Depletion layers pinch off the neck region in a uniformly doped drift region of a power MOSFET.

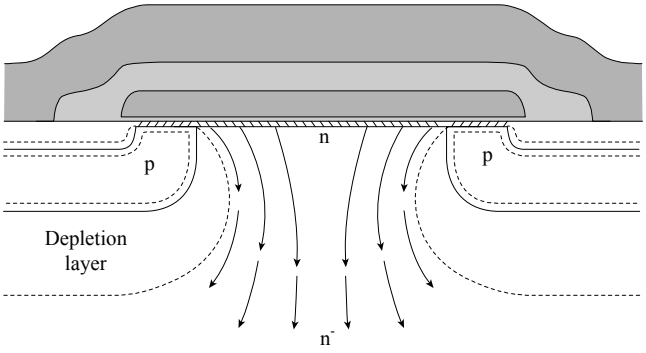


Figure 3.11: Depletion-layer thickness is reduced when the doping level under the gate is increased, improving the conduction in a power MOSFET.

The receding effect of laterally uniform doping concentration from the areas under the gate region (the throat of the device) into the drift region, and the associated boundary values, are common across devices of different rated blocking voltages [118]. The carriers will mostly conduct from the purple region in Figure 3.12 until they reach further into the main part of the drift region where due to lateral non-uniformities of the doping profile they will spread out in a trapezoidal fashion. The RA of the purple region will be the dominant component of the device on-resistance, and therefore when a doping profile of eqn. (3.38) is considered in this region with boundary doping densities a and b constant across devices (mentioned earlier), it is possible to see by rearranging eqn. (3.44) that:

$$RA = \left[\frac{\frac{2}{3}\left(\frac{1}{b^3} - \frac{1}{a^3}\right)\frac{1}{\mu_e q}}{\frac{1}{b^2} - \frac{1}{a^2}} \right] L_n$$

becomes:

$$RA \propto L_n \tag{3.57}$$

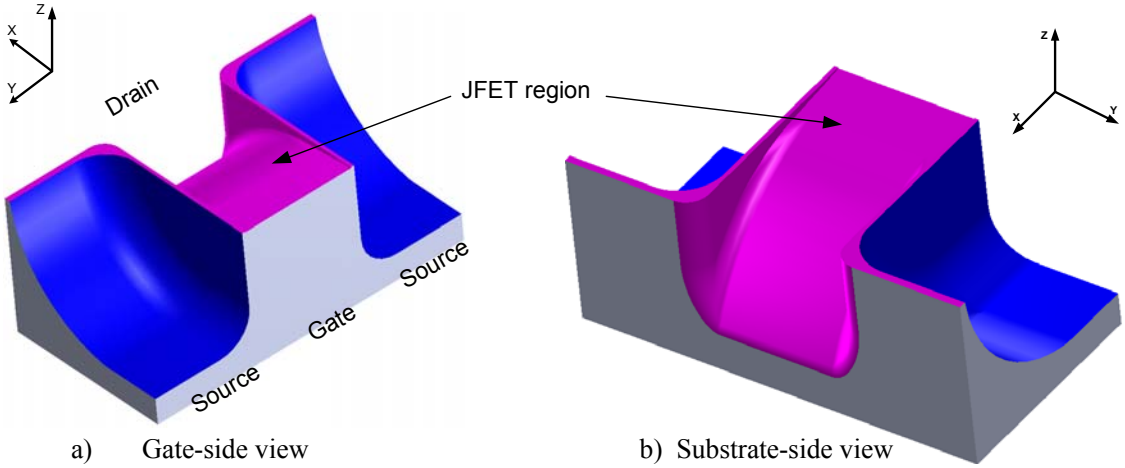


Figure 3.12: Variation of optimized doping profile (z-axis) of n^-drift layer (x-, y-axes, as in Figure 3.10) for well-designed MOSFETs, comprising two distinct regions: (1) blue region, surrounding the p^+n junctions, with donor concentration optimized for voltage blocking according to eqn. (3.38). The maximum doping density in this region is $10^{22}m^{-3}$ and the lowest depends on the voltage rating required; (2) purple region, extending from the surface region into the epilayer, optimized for conduction, also contributing to voltage blocking in reverse bias mode. The typical values of maximum doping density in this region is $10^{22}m^{-3}$ and the lowest is $5 \times 10^{20}m^{-3}$.

The length of the drift region is assumed here to be the same as the length L_n of the depletion region required to provide the voltage blocking capability; see blue region in Figure 3.12. Note that it is possible to obtain the same relation of eqn. (3.57) with alternative but similar doping profiles to eqn. (3.38) in the purple region. We already know from eqn. (3.50) that $V_{block} \propto L_n$ for fixed critical electric field strength and with eqn. (3.57) can prove previously quoted relationship (3.22):

$$RA \propto V_{block} \tag{3.58}$$

At this stage, it is helpful to clarify the difference in RA relationship obtained in eqn. (3.58) as compared to eqn. (3.56) which predicts that $RA \propto V_{block}^2$. The relationship derived in eqn. (3.56) describes the situation in the blue region of Figure 3.12, which is where the blocking of the device mainly takes place. This equation is derived on the basis that to block a specific voltage, a has to be adjusted accordingly while b ($10^{22}m^{-3}$) is much larger than a. In contrast eqn. (3.58) is associated with the purple area of the device which is primarily used for conduction and has limited participation in the blocking action, and irrespective of change in device size and associated blocking capability, parameters a and b remain the same.

This work now turns to develop analytical models to calculate power conduction losses

in actual power MOSFET designs. Re-writing eqn. (3.3) as:

$$\frac{P_{cond}}{A} = I^2 \frac{RA}{A^2} \tag{3.59}$$

At rated current, I_R, the power loss per unit area will be the maximum allowed, $k_{P/A}$, (refer eqn. (3.2)) and so we have:

$$k_{P/A} = I_R^2 \frac{RA}{A^2} \tag{3.60}$$

and so,

$$A = I_R \sqrt{\frac{RA}{k_{P/A}}} \tag{3.61}$$

Using the relationship of eqn. (3.58), eqn. (3.61) becomes:

$$A = I_R \sqrt{\frac{\gamma V_{block}}{k_{P/A}}} \tag{3.62}$$

Where γ is the constant of proportionality of eqn. (3.58). Thus, it can be seen that the device area is proportional to the product of the rated current and the square root of the blocking voltage. The first important basic scaling laws for majority carrier semiconductor device design are:

$$A \propto I_R \quad \text{(for a given blocking voltage)} \tag{3.63}$$

$$A \propto \sqrt{V_{block}} \quad \text{(for a given rated current)} \tag{3.64}$$

The actual operating conduction power loss scales as a function of device ratings and the device operating current can be written using eqn. (3.59) and eqn. (3.62) as:

$$P_{cond} = I^2 \frac{\gamma V_{block}}{I_R \sqrt{\frac{\gamma V_{block}}{k_{P/A}}}} \tag{3.65}$$

and thus:

$$P_{cond} = \frac{I^2}{I_R} \sqrt{\gamma k_{P/A} V_{block}} \tag{3.66}$$

The simple formula of eqn. (3.66) was tested against device manufacturer data sheets [119] by plotting best-fit curves through the data to indicate the on-state conduction loss. The data constituted on-state resistance $R_{DS(on)}$ for a given rated drain current I_R and V_{block}. Each data point corresponds to a different device carrying its rated current *i.e.,* $I = I_R$.

Therefore eqn. (3.66), becomes:

$$P_{cond} = P_{cond-\max} = I_R\sqrt{\gamma k_{P/A} V_{block}} \tag{3.67}$$

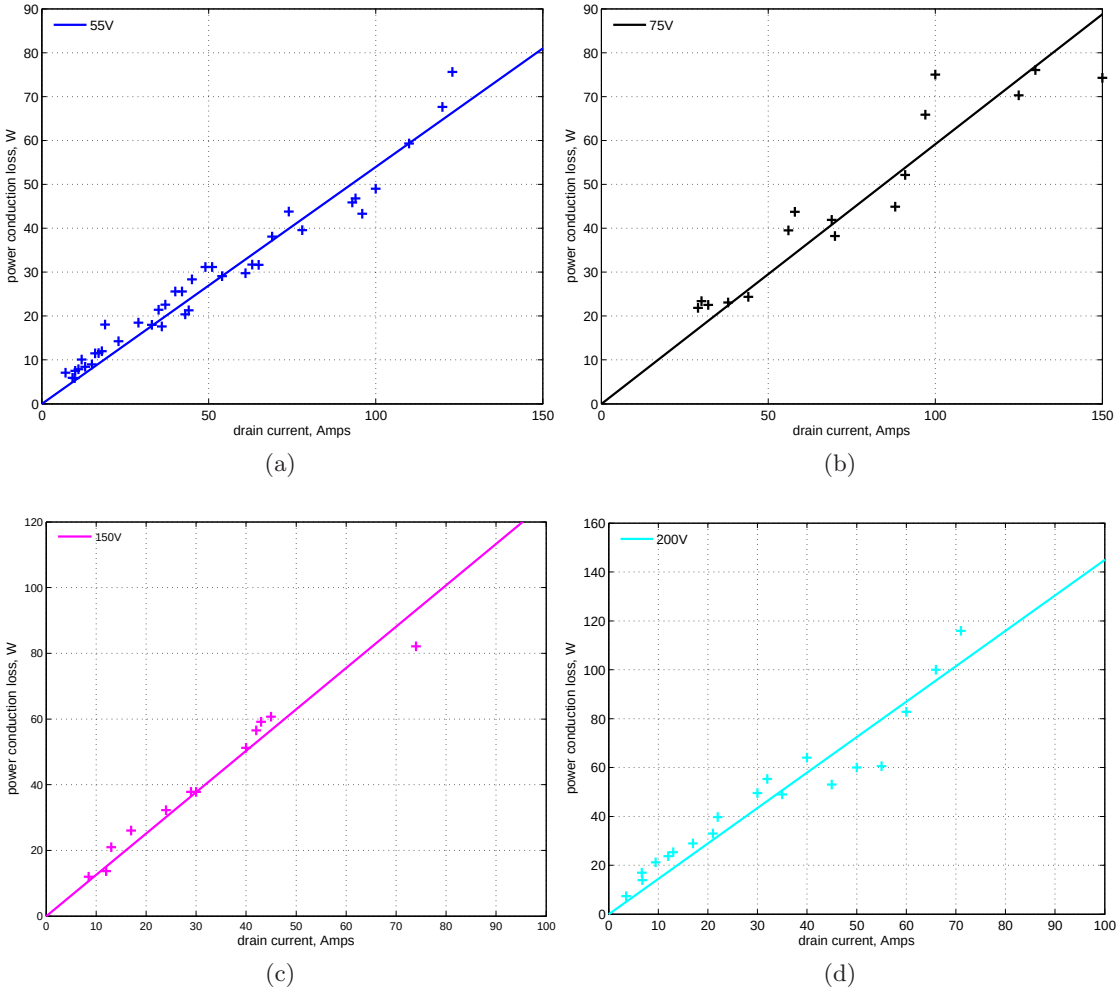


Figure 3.13: Power MOSFET conduction loss for rated drain current, I_R – sample result of (a)55V family (b)75V family (c)150V family d)200V family.

This amounts, first, to a linear relationship between conduction power loss and variable rated current, with a fixed blocking voltage. Second, it shows a square-root relationship between conduction power loss and blocking voltage, with a fixed rated current. Curves were fitted against the manufacturer data using the method of least squares in MATLAB, to prove the derived relationship of eqn. (3.67).

Figure 3.13 (*a*, *b*, *c* and *d*) illustrates the sample results for families of 55V, 75V, 150V and 200V MOSFETs, where the rated power conduction loss is compared against varying

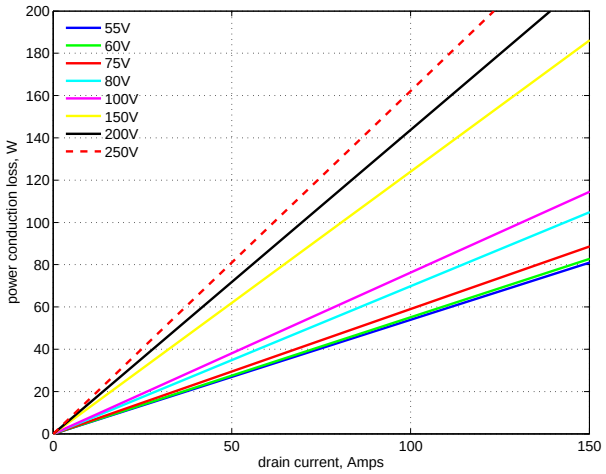


Figure 3.14: Power MOSFET conduction loss for rated drain current, I_R (range of International Rectifier devices).

rated drain currents using manufacturer data sheets. As can be seen, the best-fit straight line is a good representation of the trend, justifying earlier analytical assertions.

Figure 3.14 depicts the same linear relationship for a range of MOSFET families at different rated blocking voltages. Specific points are omitted for clarity in this graph. The individual best-fit straight line of each family of device is the same as in Figure 3.13.

This proves the first scaling law to estimate conduction power losses as established in eqn. (3.67). In order to verify the relationship between power loss for varying blocking voltage rating (at constant current), best-fit square root curves were fitted against manufacturer data, examples of which are shown in Figure 3.15(a, b, c and d). These results clearly indicate a square root relationship for a family of 30A, 35A, 40A and 45A devices. The same process was repeated for a variety of MOSFETs, operated at their rated current, as a function of blocking voltage. The results are plotted together in Figure 3.16, where again, specific data points are omitted for clarity in the graph. The individual best-fit for each MOSFET family is similar to Figure 3.15.

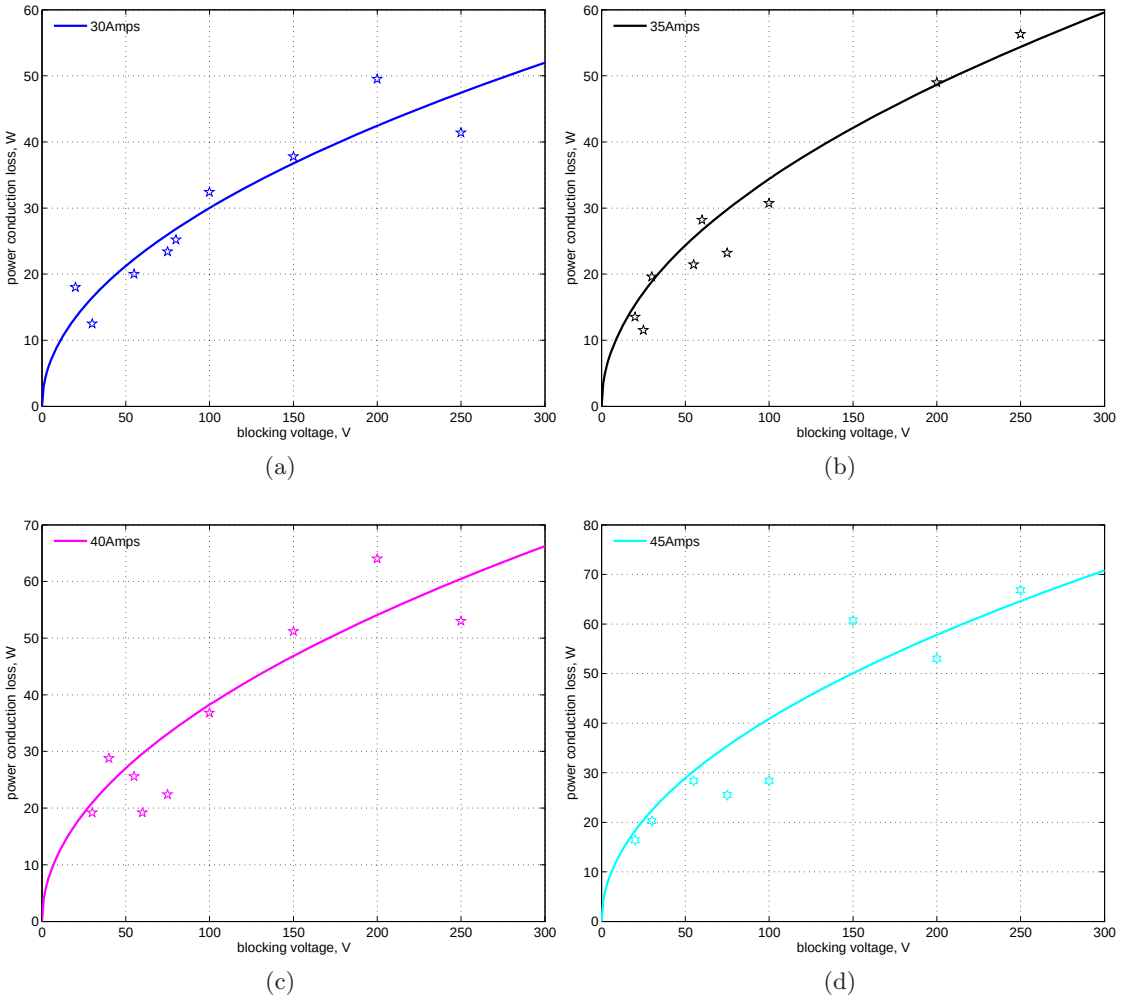


Figure 3.15: Power MOSFET conduction loss for rated blocking voltage, V_{block} (a) 30A family (b) 35A family (c) 40A family (d) 45A family.

This validates the second law for scaling conduction power loss with fixed current and variable blocking voltage (refer eqn. (3.67)). In summary, the expected trend deduced from the simple analytical model for conduction loss of a power MOSFET structure for rated current and blocking voltage conditions against experimented points from the manufacturer has been observed. This gives a good indication as to how conduction losses scale in majority carrier devices.

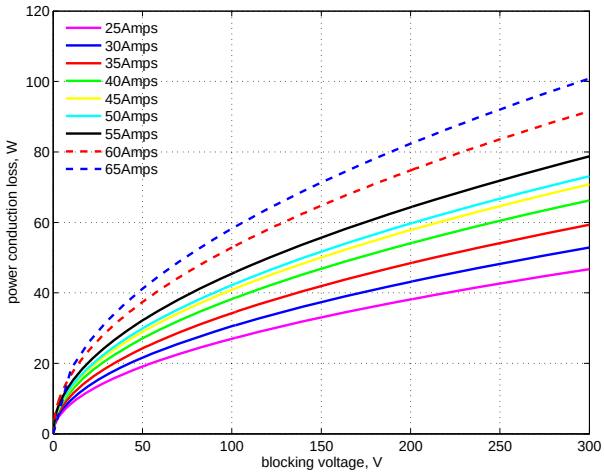


Figure 3.16: Power MOSFET conduction loss trend for variable blocking voltage (range of International Rectifier devices).

3.4.5 MOSFET Conduction Loss Scaling Constant k_{mcls} (Universal Coefficient)

In the previous section, the scaling relationships of power losses for variable current and voltage cases for a range of power MOSFETs were validated and linear and square root relationships were found. For each individual case it is possible to calculate a constant of proportionality for the power loss of the devices of the form:-

$$P_{cond-\max} = k_I \left(V_{block}\right) I_R \tag{3.68}$$

for a particular V_{block}, where $k_I = \sqrt{\gamma k_{P/A} V_{block}}$.

$$P_{cond-\max} = k_V \left(I_R\right) \sqrt{V_{block}} \tag{3.69}$$

for a particular I_R, where $k_V = I_R \sqrt{\gamma k_{P/A}}$.

Figure 3.17 illustrates the constants for both cases (variable I and variable V). The next step is to find one unique constant, that agrees with the estimated constants of all the families of MOSFET devices. This constant of proportionality, known in this thesis as the MOSFET conduction loss scaling constant k_{mcls}, must satisfy all the calculations, based on the manufacturer data points and the best curve fits obtained so far. With this constant any power loss value on the chart can be predicted for any rated voltage and rated current of the device. We can rewrite the power loss equation more generally as:

$$P_{cond} = k_{mcls} \frac{I^2}{I_R} \sqrt{V_{block}} \tag{3.70}$$

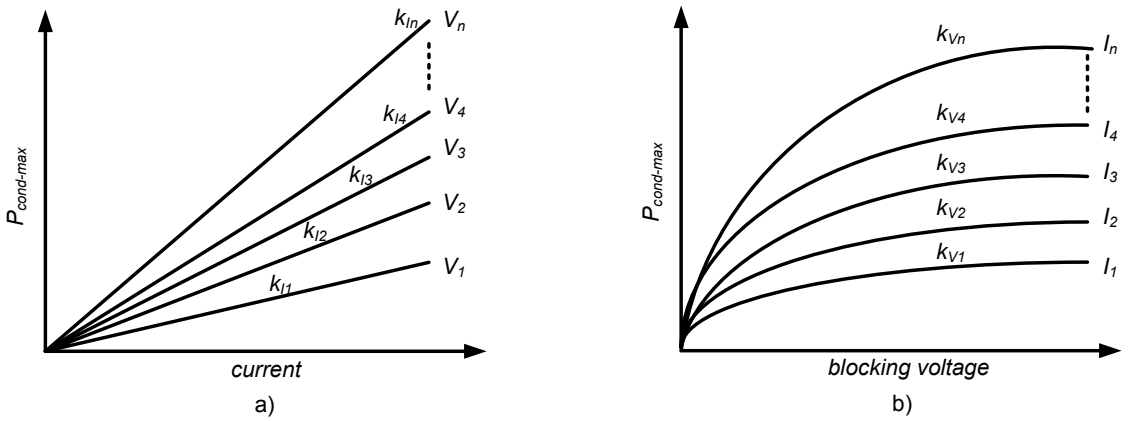


Figure 3.17: Illustration of constants of each MOSFET family for varying (a) current and (b) blocking voltage case.

or,

$$P_{cond-\max} = k_{mcls} I_R \sqrt{V_{block}} \tag{3.71}$$

where $k_{mcls} = \sqrt{\gamma k_{P/A}}$.

This constant of proportionality, k_{mcls} (or the universal conduction scaling loss coefficient), valid for all MOSFET devices, can now be calculated. The units of this constant are $V^{0.5}$. All the k_I values from eqn. (3.68), can be generated and plotted as a function of blocking voltage. As, $k_I = k_{mcls}\sqrt{V_{block}}$, it is expected that a plot of k_I against V_{block} is a square root. These values are plotted in the Figure 3.18. k_{mcls} can be calculated as a best fit through the graph of Figure 3.18. In this case, k_{mcls}, is found to be:

$$k_{mcls} = 0.091 V^{0.5} \tag{3.72}$$

Likewise, from the eqn. (3.69), all the k_V values can be found. As, $k_V = k_{mcls} I_R$, we

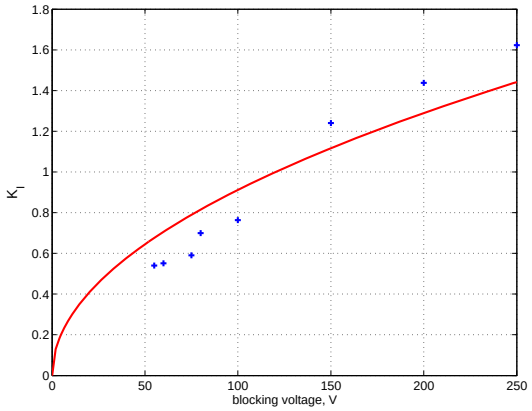


Figure 3.18: Estimated constants k_I's for variable blocking voltage case.

expect a straight line between k_V and I_R. This is plotted in the Figure 3.19 as:

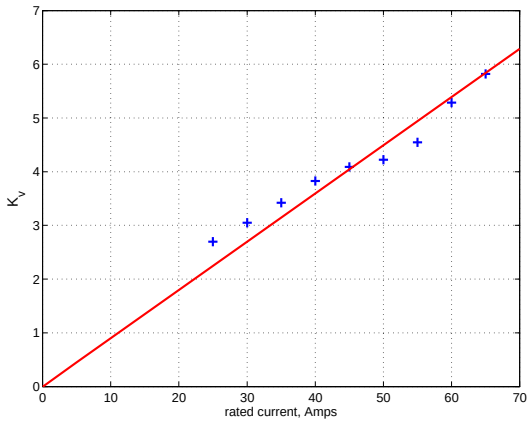


Figure 3.19: Estimated constants k_V's for variable current case.

The best fit of this data shows k_{mcls}, to be:

$$k_{mcls} = 0.089V^{0.5} \tag{3.73}$$

Notably, the k_{mcls} values emerging out of eqns. (3.72) and (3.73) were very close to one another, for both rated current and voltage cases. An approximation of $k_{mcls} = 0.09V^{0.5}$ is adopted in this work.

Figure 3.20 shows the key result obtained from the calculated single constant of proportionality, k_{mcls}, and indicates conduction loss as a function of device rating. This plot is aligned with the theory and trends established earlier for majority carrier devices (the best match of Figure 3.13-3.16). This result is a reconstruction of all the plots without using any manufacturer data sheets or any of the previous best curve fits.

Using this scaling law and constant will facilitate computation of power losses for any rating of a given device family including extrapolation of device characteristics beyond a manufacturer's given data. One simple analytical model, eqn. (3.71) and derived k_{mcls} will allow a circuit designer to observe the circuit efficiency and practical (threshold) rating range of a device quickly, with almost no knowledge of device physics.

For silicon, there is a value of doping for which ρ_r/E_{max} is minimised. Assuming we are on this point, it is clear that k_{mcls} is a single constant for the MOSFET in silicon and therefore our calculations provide an absolute limit for majority carrier silicon devices.

Finally, conduction loss in a Si power MOSFET can be written accurately and simply as:- $P_{cond} = k_{mcls}\frac{I^2}{I_R}\sqrt{V_{block}}$; where $k_{mcls} = 0.09V^{0.5}$

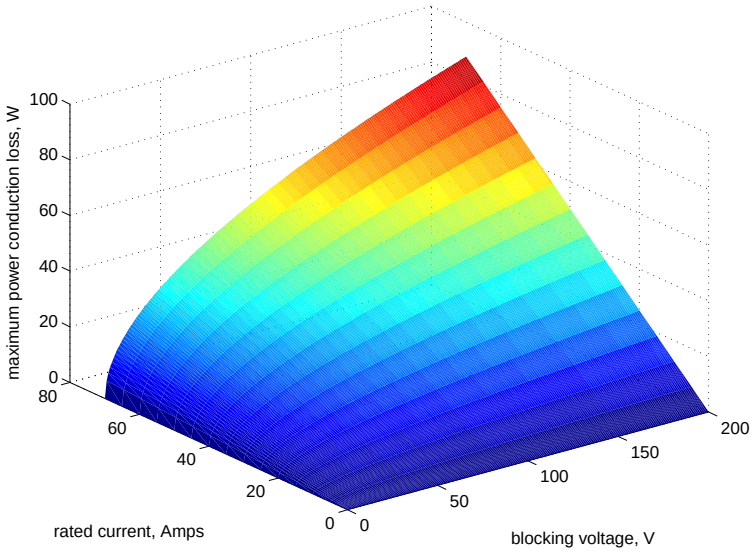


Figure 3.20: Power conduction losses for a range of power MOSFETs using eqn. (3.71) and constant k_{mcls}.

The following section will establish the scaling laws for conduction power loss in minority carrier devices (such as a *pin* diode and IGBT) and their respective scaling loss constants.

3.5 Scaling Laws for Conduction Losses in IGBT and *pin* Diode

The MOSFET is simple to analyse because it is a majority carrier device and consequently it looks like a constant valued resistance between source and drain when in its linear region (which is the region of most interest to the power electronics community). However, the *pin* diode and the IGBT are minority carrier devices and thus have junction voltage drops present in them. A correction factor to account for such *pn* junction drop is thus required on top of the MOSFET scaling equations to determine power loss scaling in minority carrier devices such as the power diode (a *pin* diode) and the IGBT. The power lost in IGBTs and diodes is quantified by investigating the forward conduction characteristics for these devices. The on-state characteristics of IGBTs, which resemble those for *pin* [96], are therefore described together in this section with the derived analytical models.

A simple DC model which allows conduction power loss in both the IGBT and the *pin* diode to be calculated is shown in Figure 3.21.

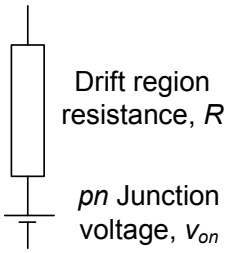


Figure 3.21: Large signal model of GBT/*pin* diode.

This model is justified because there are two main components of voltage drop in these devices – the *pn* junction type drop, which is of the order of few volts and accounts for power loss due to recombination, and also a resistive drop due to the series resistance present in the device which accounts for normal resistive power loss. A general *I-V* characteristic for these devices is shown in Figure 3.22 where the static characteristic of the device is approximated using a piece-wise linear approximation suitable for static modeling in power electronic circuits. It includes an offset on-state voltage v_{on}, and a series resistor of value R_{slope} to account for the slope in the actual forward characteristics.

The IGBT device is preferred over the MOSFET at high blocking voltages because the resistive element is lower in the IGBT due to conductivity modulation of the drift region. However, at low voltages, the IGBT has a higher on-state voltage compared to the MOSFET because the embedded *pnp* bipolar transistor in the IGBT never operates in saturation, so a junction voltage drop always exists across the device when it is turned on.

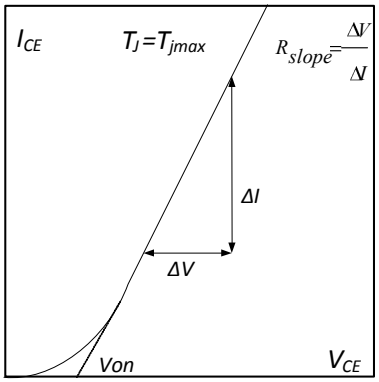


Figure 3.22: Typical on-state characteristic of an IGBT.

3.5.1 Experimentally verified on-state analytical model for voltage drop calculation

Power conduction loss in the IGBT has direct relevance to the overall forward voltage drop in the forward conducting state. Close scrutiny of the three discrete regions of the IGBT structure: the MOSFET, *pin* diode (as p^+n^-), and *pnp* transistor components reveals the contributions to voltage drop from each portion. The purpose of this section is to make use of physics-based analysis to improve existing IGBT mathematical models by adding complicated features that are important to the accuracy of predicted on-state voltage drop and forward current. Therefore, in the present section an attempt is made to build a complete model for the IGBT voltage drop, based on the physical operation of the device from first principles [120], validating against manufacturer experimented data-sheets. As different equations apply to each device region, this analysis matches boundary conditions at the interfaces between the regions, and joins each solution together to construct a general model for the IGBT final I-V curve. The analytical model accounts for ambipolar transport equations [121] during steady-state condition. I-V characteristic models have also previously been explored in [122, 123].

Simulation results are plotted for a broad range of IGBTs (NPT and PT) to demonstrate model versatility. The IGBT model is in strong agreement with commercially available IGBTs. It reproduces exact on-state forward characteristics. The model can be used to predict manufacturer IGBT designs successfully, exposing the voltage drop contributions of each of the above-mentioned three discrete regions. The results and theory presented here are believed to provide insight into optimal IGBT design, and show that theory is obeyed in practice.

Unknown governing device design parameters can therefore be identified (or calculated) using this model. These include the operating current density J, conduction area A, the ambipolar diffusion length L_a, the length of the JFET region (neck of the device) L_{JFET} and the thickness of the n^- drift region L_n (dependent on the doping concentration) for a range of blocking voltage and rated current. Thus, the functional relationship of L_a, L_{JFET}, J, R_{slope} and A with respect to the rated V (or V_{block}) and I can be found. This analysis enables us to see the size of these quantities with rated V and I for an optimal IGBT design and also calculate the impact of varying the device parameters.

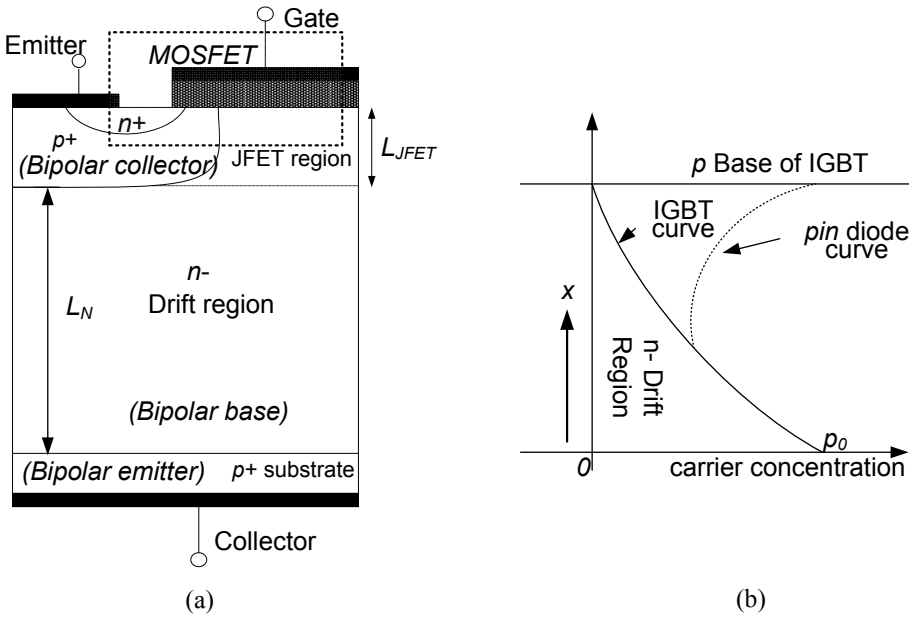


Figure 3.23: IGBT structure (transistor and MOSFET components also marked) b) Comparison of carrier concentrations in IGBT and *pin* diode under conductivity modulation conditions, illustrating p_0, maximum concentration of minority carrier holes at $x = 0$ and its distribution as a function of x. *pin* distinguishes the IGBT because carriers first fall but begin to rise again as one approaches the n^-end region.

3.5.2 Physical Description of the Model

As previously noted in Chapter 2, the IGBT behaves as a bipolar transistor (*pnp*) supplied with base current (electrons) by a MOSFET. The collector of the *pnp* is shorted to the MOSFET drain at the edge of the n^-drift/$p-$base junction where the excess carrier concentration is almost zero, as shown in Figure 3.23(b). The carrier distribution profile of an IGBT is compared with the *pin* diode catenary carrier distribution in Figure 3.23(b). The main difference is at the n^- drift region/p base junction. This is due to the conductivity modulation effect in the JFET region. The IGBT has much less modulation, due to the reverse biased junction during forward conduction mode in the JFET region. This region contributes noticeably towards the potential drop in IGBTs, as will be seen shortly. A *pin* diode does not face the same issue because there is no JFET effect (carrier injection occurs from both the $p+$ and $n+$ end regions in the n^-layer forming a 'bath tub' shown in Figure 3.23 (b). The bipolar transistor component of the IGBT can be treated in a similar way to a *pin* diode, but with transistor boundary conditions, i.e., $p(L_n) = 0$ and $p(0) = p_0$. p_0 is used as a parameter for the model development and is eventually eliminated in terms of the current density, J.

In this analysis the analytical model of IGBT voltage drop is given by the sum of three regions:
(1) the junction drop $v_{junction}$ across p^+/n^- junction, or classified as the emitter/base junction of the p^+n^-p transitor;
(2) the n^- drift drop v_{drift}, usually referred to as the conductivity modulated low doped region. It is further subdivided into two parts: (i) when $p, n >> N_D$ background doping and (ii) when $p << N_D$, falling to zero close to the reverse biased n-drift/p base junction;
(3) the JFET region drop, v_{JFET}. The channel and accumulation layer voltage drops are assumed negligible in our model, as suggested by numerical results in [124].

(1) On-state Voltage Drop, $v_{junction}$, across the Forward Biased p^+/n^- Junction modulates the conductivity of the drift layer, and serves to reduce the on-state resistance by injecting excess minority carriers (holes). $v_{junction}$ is obtained by using the oft-quoted built-in potential relationship from the law of junction:

$$v_{junction} = V_T \ln\left(\frac{p_0 N_D}{n_i^2}\right) \tag{3.74}$$

Here $V_T = kT/q$. Defining p_0, the concentration of holes at the junction $x = 0$ in the n^-region [82]:

$$p_0 = \frac{JL_a}{2qD_p}\tanh\left(\frac{L_n}{L_a}\right) \tag{3.75}$$

where D_p is diffusion constant of holes. Substituting eqn. (3.75) in eqn. (3.74) gives the $v_{junction}$, responsible for producing the "*knee*" or "*kink*" in the forward conduction I-V curve as:

$$v_{junction} = V_T \ln\left[\frac{JL_a N_D}{2qD_p n_i^2}\tanh\left(\frac{L_n}{L_a}\right)\right] \tag{3.76}$$

where quantities J and L_a have an influence on the value of $v_{junction}$.

(2) On-state Voltage Drop, v_{drift}, from modulated n^- Drift Layer, when conductivity modulation takes place in most of the layer, is derived by integrating the electric field distribution $E(x)$ across this layer. To obtain $E(x)$, the high level injection condition $n(x) = p(x)$ is applied. We know that the net flow of current is the sum of the two separate effects, drift and diffusion current [125]. Hence, the total current due to the hole current density is:

$$J_p = q\mu_p\left[pE - V_T\frac{dp}{dx}\right] \tag{3.77}$$

and similarly the total current due to the electron current density is:

$$J_n = q\mu_n\left[nE + V_T\frac{dn}{dx}\right] \tag{3.78}$$

The total current density in the modulated drift region is expressed as $J(x) = Jn(x) + Jp(x)$= constant. The first terms in eqns. (3.77) and (3.78) are due to drift and the second terms are due to diffusion. After rearranging and simplifying both these eqns. we obtain the $E(x)$ of the form:

$$E(x) = \frac{V_T}{L_a}\left[\frac{2\mu_p}{(\mu_n+\mu_p)}\frac{\cosh\left({}^{L_n}/_{L_a}\right)}{\sinh\left\{{}^{(L_n-x)}/_{L_a}\right\}} + \frac{\mu_n-\mu_p}{\mu_n+\mu_p}\frac{1}{\tanh\left\{{}^{(L_n-x)}/_{L_a}\right\}}\right] \tag{3.79}$$

in which the expression for minority carrier distribution in the drift region is given by [126]:

$$p(x) = \frac{JL_a}{2qD_p}\left(\frac{\sinh\left[\frac{L_n-x}{L_a}\right]}{\cosh\left[\frac{L_n}{L_a}\right]}\right) \tag{3.80}$$

has been used. Equation (3.80) is obtained by solving the continuity equation under steady-state conditions, with appropriate choice of boundary condition, and describes the steady-state distribution and shape of the excess carriers in the drift (middle) high-level injection region. p is greater than N_D in much of the region, but decreases below background doping density N_D in a 'small' region of drift layer near the bipolar collector junction, as depicted in Figure 3.24. The hole concentration is maximum at the p^+/n^- junction $x = 0$) and diffuses or falls away from the edge of this junction with distance x, reaching zero by the reverse bias at the end of the drift region. In order to calculate the voltage drop in the drift (middle) region, we consider the hole and electron concentrations $p(x)$ and $n(x)$ under conductivity modulation. The analysis is performed using the boundary conditions defined in Figure 3.24. The electron concentration is at N_D away from the junction until $x = x_i$, below which the minority hole concentration exceeds N_D, as illustrated in Figure 3.24. Charge neutrality dictates that $n = p$ for $x < x_i$ and conductivity modulation takes place in $0 < x < x_i$.

Eqn. (3.80) can be rewritten to calculate x_i:

$$x_i = L_n - L_a\text{arcsinh}\left(\frac{2qD_pN_D}{JL_a}\cosh\left[\frac{L_n}{L_a}\right]\right) \tag{3.81}$$

In the case that maximum hole concentration p_0 is less than N_D (equilibrium value), x_i becomes negative according to eqn. (3.81). This implies that *region-I* has zero length and therefore for this we use the simplified result that: $V_{drift1} = 0$ for $x_i < 0$. In any other case the voltage drop in the *region-I* of Figure 3.24 is found by integrating the eqn.

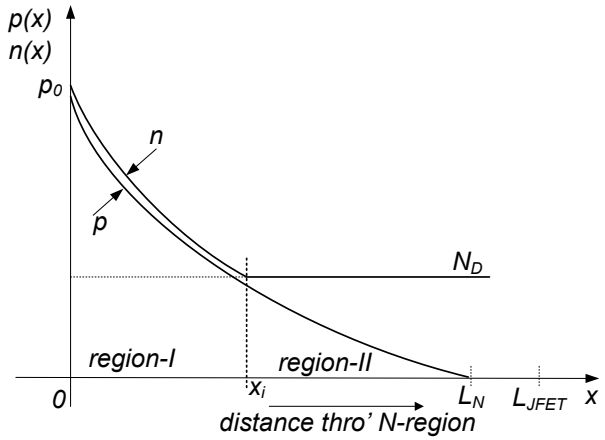


Figure 3.24: Coordinate system used in developing IGBT drift region voltage drop model, shows the distribution of holes and electrons in the N-region $w.r.t$ distance x, to a point at which conductivity modulation takes place in $0 < x < x_i$ indicated as region-I. Beyond distance x_i is region-II, where $p < N_D$ and goes to zero, while $n = N_D$.

(3.79) from 0 to x_i, yielding:

$$\begin{aligned} v_{drift1} &= -\int_0^{x_i} E(x)\,dx \\ &= -2V_T \frac{\mu_p}{\mu_n+\mu_p} \cosh\left(\frac{L_n}{L_a}\right) \ln\left(\frac{\tanh\left[\operatorname{arcsinh}\left(\frac{2qD_pN_D}{JL_a}\cosh\left[\frac{L_n}{L_a}\right]\right)\right]}{\tanh\left(\frac{L_n}{L_a}\right)}\right) \\ &\quad -V_T\left(\frac{\mu_n-\mu_p}{\mu_n+\mu_p}\right)\ln\left(\frac{2qD_pN_D}{JL_a\tanh\left(\frac{L_n}{L_a}\right)}\right) \end{aligned} \tag{3.82}$$

The calculation of voltage drop in the drift region is completed by working out the remaining potential drop from $x = x_i$ to $x = L_n$ in the *region-II* of Figure 3.24, referred as v_{drift2}. In this region the current is dominated by the majority carriers, n, electrons, which are maintained at constant value N_D. Therefore,

$$v_{drift2} = R_{drift}I = \rho_{drift}\frac{L}{A}I \tag{3.83}$$

Here $L = L_n - x_i$ and substituting ρ_{drift} from eqn. (3.13), we obtain:

$$v_{drift2} = \frac{(L_n - x_i)\,I}{\mu_n q N_D A} \quad \text{for} \quad x_i > 0 \tag{3.84}$$

or;

$$v_{drift2} = \frac{L_n I}{\mu_n q N_D A} \quad \text{for} \quad x_i < 0 \tag{3.85}$$

In addition to $v_{junction}$; interestingly v_{drift1} and v_{drift2} also provide an extra contribution to the *knee* of the device's *I-V* curve, as demonstrated in Figure 3.25.

Previous attempts to provide an expression for the total voltage drop in the drift region [82] integrate eqn. (3.79) across the whole drift region, rather than from zero to x_i. Furthermore the resulting equation in that case is missing some terms. If these missing terms are included, an infinite voltage drop across the drift region is predicted - due to the doping concentration of the holes going to zero at the end of the drift region - implying infinite resistance. This is clearly in error. The limit $x = x_i$ is crucial in integrating eqn. (3.79).

(3) On-state Voltage Drop v_{JFET} from the JFET Region, is the product of the resistance of the unmodulated JFET region R_{JFET} (below the gate) and the current I as:

$$v_{JFET} = R_{JFET} I \left(1 - \alpha_{pnp}\right) \tag{3.86}$$

in which, the current gain, defined as: $\alpha_{pnp} = \frac{1}{cosh(L_n/L_a)}$ [127], is used to account for the fact that a small proportion of the current (holes) will not pass from the JFET region, but instead will flow in the area underneath the p-base. The term derived here relates to the familiar linear part (slope) of the *I-V* characteristic just after the *knee*. The slope of this part is $1/R_{slope}$ where:

$$R_{slope} = R_{JFET} \left(1 - \alpha_{pnp}\right) \tag{3.87}$$

leading to:

$$v_{JFET} = R_{slope} I \tag{3.88}$$

Furthermore, eqn. (3.87) can be used to calculate the area of the device, also required in evaluating $V_{junction}$, V_{drift1}, and V_{drift2}. Making use of ρ_{JFET} from eqn. (3.14), the expression (3.87) becomes:

$$R_{slope} = \frac{L_{JFET}(1 - \alpha_{pnp})}{q\mu_n N_D A} \tag{3.89}$$

assuming a uniform doping density N_D in the JFET region. Therefore, we have:

$$A = \frac{L_{JFET}(1 - \alpha_{pnp})}{q\mu_n N_D R_{slope}} \tag{3.90}$$

Here it is assumed that the area of the JFET region is the same as the area of the device. This is a reasonable approximation, especially for large devices. The mathematical expressions (3.74)-(3.90) derived in this section will now be tested, by using them to derive *I-V* curves for a range of IGBTs manufactured by industry [128].

3.5.3 Characterisation of the Model

The preceding analysis and equations presented are used to provide a relationship between the operating current through and the voltage drop across the device in any general case, the *I-V* characteristic. The overall aim is to derive a general and unified analytical model that is capable of predicting IGBT *I-V* relationships of any family and rating with relative accuracy. Once that is achieved, it is straightforward to predict conduction losses under general operating conditions for any rating and scale losses with device area A, V_{block} and I_R.

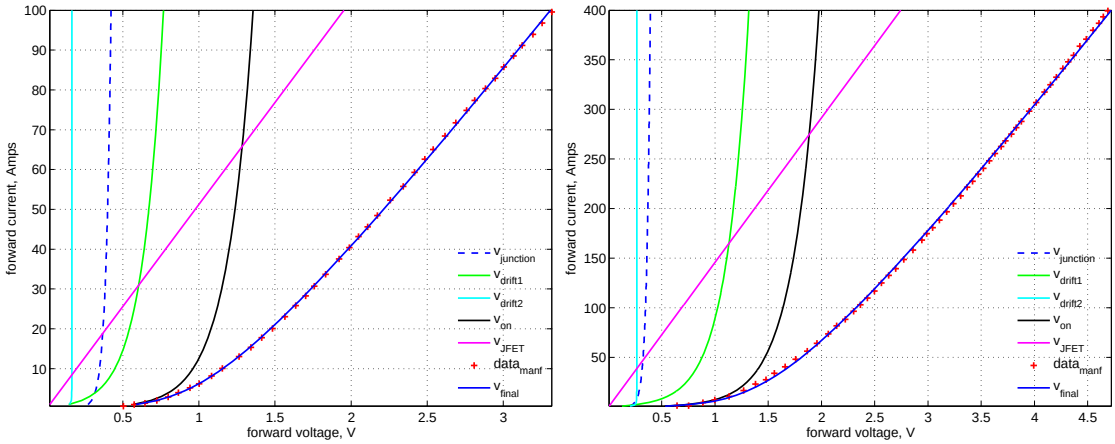
The task here is to find a complete set of parameters which describes device output characteristics accurately. This model is parameterised and built in terms of three unknown quantities: L_a, L_{JFET} and R_{slope} whose set can be identified individually for each of the IGBT devices from *I-V* curves provided by the manufacturer. As a by-product, device area A can also be calculated from expression (3.90). The parameter identification is carried out by setting up a cost function of squares of the errors between measured *I-V* data provided by the manufacturer and model prediction. This is then minimised via nonlinear constrained optimisation routines in Matlab programme (fmincon), to yield the optimal parameter values for L_a, L_{JFET} and R_{slope}. Individual devices are identified in terms of their I_R and V_{block} ability, and it is beneficial to quantify the variation of the characterising parameters of the model in terms of these rated values.

Procedure of Parameters L_a, L_{JFET} and R_{slope} Extraction for Individual Cases

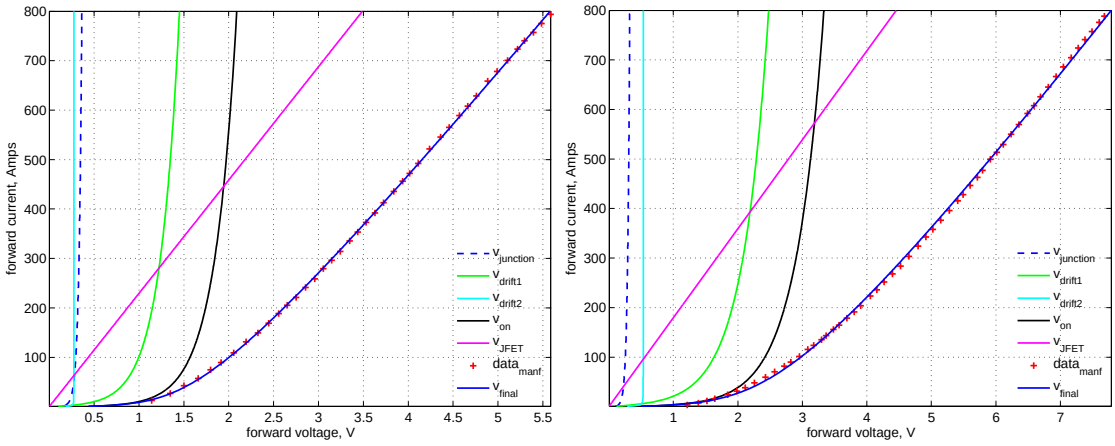
The manufacturer *I-V* characteristic curves provided were obtained in digital form, either by scanning or from the original source pdf file, and were imported as bitmaps into MATLAB. Manual tracking via the *ginput* (The Mathworks Inc., 2000) [129] command was then necessary to obtain x-y coordinates. Care was taken to obtain the data points with the highest possible accuracy. The Sequential Quadratic Programming constrained optimisation routine *fmincon* (The Mathworks Inc.) was employed to iteratively improve the elements of a starting vector of parameters appearing in the derived eqns. (3.76), (3.84), (3.85), (3.88), (3.90), to obtain a best fit (in a least sum of squares of differences sense) of the formulae to the measurements.

In order to ensure convergence to the optimal solution, it was often needed to provide reasonably accurate starting values for the parameters. The measured *I-V* characteristic ($T_j = 125^oC$ at gate voltage of $15V$) provided by the IGBT manufacturer and the predicted *I-V* characteristic from the model are illustrated in Figure 3.25 for a few sam-

ple results. For, 600V/50A IGBT, the identified $L_a = 24.7\mu m$, $L_{JFET} = 2.84\mu m$ and $R_{slope} = 20m\Omega$ precisely computes the manufacturer *I-V* curve, shown in Figure 3.25a. The procedure was repeated in this manner to predict the output characteristics of a range of IGBTs (25 cases). Figures 3.25(*b-d*) shows the sample results of 1700V/200A, 3300V/400A, 6500V/400A devices. Identified parameter values and L_n and *Area* calculations for Figure 3.25 devices, together with the rest of the ratings are summarised in Table 3.1. Note that NPT-IGBTs are investigated in this section.



(a) 600V/50A (Part No.BSM50GB60DLC) (b) 1700V/200A (Part No.BSM200GA170DLC)



(c) 3300V/400A (Part No.FZ400R33KL2CB5) (d) 6500V/400A (Part No.FZ400R65KF1)

Figure 3.25: Demonstration of IGBT model validation against manufacturer devices (four sample results). Illustrating individual voltage drop contributions from *junction* (eqn. (3.76)) *drift* (eqns. (3.82)-(3.84)) and *JFET* regions (eqn. (3.89)) using the derived analytical expressions. Note that on the final *I-V* curve, plus symbols + relate to the manufacturer data points, matching accurately to the derived model (solid blue line v_{final}), *i.e.,* sum of $v_{on}(= v_{junction} + v_{drift1} + v_{drift2})$ and v_{JFET}.

It can be seen from Figure 3.25, that the model developed predicts an accurate *I-V* relationship, matching to the device manufacturer's, with representation of the *knee* and *linear* parts and the voltage drop contributions of the device's distinct regions explicitly shown. As expected, the junction drop $v_{junction}$ is an exponential shape and contributes to the *knee* of the curve. Interestingly the remaining contributions to the knee come from the drift region drop v_{drift}. The two parts of the voltage drop v_{drift1} and v_{drift2} in this region are illustrated separately and one can see that they mostly affect the *knee* of the characteristic.

The model also explains why there is a linear part in the characteristic curve at higher operating current. This is produced by the voltage drop in the JFET region v_{JFET} which is plainly an ohmic drop. It is well known that IGBT devices produce larger on state voltage drops compared to a *pin* structure and the components of the model utilised here explain, from first principles, why this is the case. It is due, in particular, to carrier distribution differences in the middle (or n^-) regions under conductivity modulation conditions.

3.5.4 Tables of key IGBT Parameters

Whilst it is useful to see the various voltage drop contributions in the IGBT, features of the identified parameters are also important, with changes and an emerging pattern across a range of ratings. Table 3.1 - Table 3.2 summarise the individually identified and calculated IGBT parameters from the built analytical model which predicts accurate *I-V* curves for commercially available devices. Table 3.1 reveals the L_a, L_{JFET}, L_n and *Area* values of these devices, parameters not given by the manufacturer (to keep the design recipe under wraps). Derived analytical expressions: (3.76), (3.82), (3.84), (3.88) are evaluated to produce Table 3.2. Meaningful comparison of parameters for a range of voltage classes of various ratings, provides additional insight into general design rules. Several observations can be made immediately from Table 3.1 and Table 3.2:

- A quantity of particular interest for the IGBT voltage drop calculation is the ambipolar diffusion length L_a, which is found to be approximately one third of the drift region length L_n. This reveals the extent to which the drift region has to be in conductivity modulation for the model to give accurate predictions. This finding is physically meaningful and of great significance in understanding IGBT manufacturing.
- L_a follows a regular pattern of staying constant for a particular V_{block} (any I_R)

- L_{JFET} is only a few μm in any case which is minimal compared to the size of the other two lengths: L_n and L_a. L_{JFET} does not vary with the I_R of the device.
- Current density $J_{rated}(= I_{rated}/A)$ is solely a function of V_{block} - independent of the I_R.
- Forward voltage drop v_f depends on the V_{block} , not on the I_R.
- *Area* varies in a more complicated manner with V_{block} and I_R, than the other quantities mentioned above.

Table 3.1: IGBT parameters for industry devices (Infineon). The information from this table is used to calculate voltage drop contributions from distinct IGBT regions, and given in Table 3.2.

$V_{block}(V)$	$I_{rated}(A)$	$L_a(\mu m)$	L_{JFET} (μm)	R_{slope} $(m\Omega)$	$L_n(\mu m)$	$Area(cm^2)$
600	50	24.701	2.8409	19.526	68.57143	0.651477
	75	24.446	3.0032	12.922	68.57143	1.044842
	100	23.446	3.943	9.5446	68.57143	1.885764
	150	24.565	2.9433	6.4819	68.57143	2.037601
	200	24.93	3.0	4.9439	68.57143	2.707254
	300	24.04	3.2005	3.2098	68.57143	4.510904
1200	200	42.369	5.0509	4.4922	137.1429	10.59382
	300	42.711	4.8503	3.0176	137.1429	15.11057
	400	43.121	4.5211	2.2737	137.1429	18.64269
	600	42.856	4.9157	1.5166	137.1429	30.44207
	800	54.712	6.0979	1.1918	137.1429	43.83712
	1050	37.503	5.4111	1.2424	137.1429	42.23222
	1200	36.655	6.1909	1.0494	137.1429	57.45694
1700	200	59.808	2.8955	6.8596	194.2857	5.639764
	300	57.417	4.0918	4.4654	194.2857	12.37297
	400	58.121	3.7274	3.9782	194.2857	12.61304
	600	89.366	1.2685	2.0622	194.2857	6.909036
	800	59.572	4.1201	1.6915	194.2857	32.57895
	1200	57.433	5.5075	1.1109	194.2857	66.93755
3300	400	114.94	4.4588	4.3616	377.1429	26.58544
	800	118.81	2.9487	2.1736	377.1429	34.95765
	1200	119.45	2.4761	1.4483	377.1429	43.98698
6500	200	183.33	12.63	10.538	742.8571	64.11590
	400	188.28	8.051	5.5684	742.8571	76.97496
	600	184.2	10.241	3.6434	742.8571	150.1496

Table 3.2: IGBT on-state voltage drop values determined at I_R – a comprehensive breakdown of drops occurring in distinct regions of an IGBT. $v_f (= v_{junction} + v_{drift1} + v_{drift2} + v_{JFET} \approx v_{on} + I_R R_{slope})$ can be used to calculate the rated power conduction loss $P_{cond-max}$ of a device. Note that the v_{on}'s $(= v_{junction} + v_{drift1} + v_{drift2})$ calculated at half of the rated current (far right column of this table) from our built model matches to the values, when one draws the tangent 'by-hand' on the I-V curve of the data-sheet, to locate the knee point on the x-axis - a common practice in piece-wise linear approximation.

V_{block} (V)	I_{rated} (A)	$v_{junction}$ (V)	v_{drift1} (V)	v_{drift2} (V)	$v_{drift-total}$ (V)	v_{JFET} (V)	v_f (V)	$v_{on}(V)$ @I_{rated}	$v_{on}(V)$ @$I_{rated}/2$
600	50	0.40	0.67	0.17	0.84	0.98	2.21	1.23	1.12
	75	0.40	0.67	0.17	0.84	0.97	2.21	1.24	1.12
	100	0.39	0.68	0.19	0.87	0.95	2.21	1.25	1.12
	150	0.40	0.67	0.17	0.84	0.97	2.21	1.23	1.12
	200	0.40	0.66	0.16	0.82	0.99	2.21	1.21	1.09
	300	0.39	0.68	0.18	0.86	0.96	2.22	1.25	1.13
1200	200	0.35	0.88	0.26	1.15	0.90	2.39	1.49	1.32
	300	0.35	0.88	0.26	1.14	0.91	2.39	1.48	1.32
	400	0.35	0.88	0.25	1.13	0.91	2.39	1.48	1.32
	600	0.35	0.87	0.25	1.13	0.91	2.39	1.47	1.31
	800	0.36	0.57	0.13	0.69	0.95	2.00	1.05	0.95
	1050	0.35	1.22	0.40	1.62	1.30	3.28	1.97	1.73
	1200	0.35	1.23	0.43	1.66	1.26	3.27	2.01	1.75
1700	200	0.37	1.17	0.27	1.44	1.37	3.18	1.80	1.63
	300	0.36	1.19	0.30	1.50	1.34	3.19	1.85	1.66
	400	0.37	1.22	0.29	1.52	1.59	3.47	1.88	1.69
	600	0.41	0.66	0.09	0.75	1.24	2.40	1.16	1.08
	800	0.36	1.10	0.27	1.37	1.35	3.08	1.72	1.55
	1200	0.35	1.12	0.30	1.42	1.33	3.10	1.77	1.58
3300	400	0.34	1.30	0.27	1.57	1.74	3.66	1.91	1.74
	800	0.36	1.29	0.25	1.54	1.74	3.63	1.89	1.73
	1200	0.36	1.31	0.24	1.55	1.74	3.65	1.91	1.75
6500	200	0.28	2.18	0.60	2.78	2.10	5.16	3.06	2.71
	400	0.30	2.20	0.53	2.73	2.23	5.26	3.02	2.72
	600	0.29	2.22	0.58	2.80	2.19	5.28	3.09	2.76

It is worthy of note that for all devices considered the calculated value of α_{pnp} is approximately 0.1 or less. This parameter can be used to evaluate the current gain of the wide-base *pnp* transistor inside the IGBT, given by $\frac{\alpha_{pnp}}{(1-\alpha_{pnp})}$. It amounts to approximately 0.1 or less for all devices suggesting that the bipolar transistor of IGBTs considered here operates under low-gain conditions, contrary to the high-gain conditions of traditional bipolar transistors. This fact has been highlighted in [123] as the reason why the electron and hole transport equations can not be decoupled in IGBTs and more complicated analysis is required to study IGBTs. Our present results are in agreement with this argument.

3.5.5 Functional Relationship of Key Model Parameters with Device Ratings

Canvassing the variation of the identified parameters responsible for producing actual *I-V* characteristics for each device, establishes their general dependence with V_{block} and I_R. This enables us to build an overall model capable of predicting the characteristics of devices of any possible rating. The numerical results obtained for all devices can offer a convenient way to indicate their trend with varying blocking voltage.

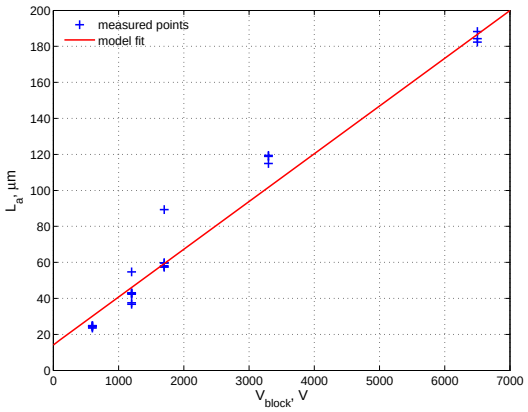


Figure 3.26: IGBT ambipolar diffusion length L_a paramter shown in +, against V_{block} with model fit from eqn. (3.91). The method by which p_1 and p_2 is identified is described in subsection 3.5.6.

The plots of L_a and L_{JFET} against V_{block} are shown in Figure 3.26-3.27 respectively, and it is recognised here that both L_a and L_{JFET} vary linearly with V_{block} with the L_{JFET} variation less pronounced. These crucial observations can simply be described

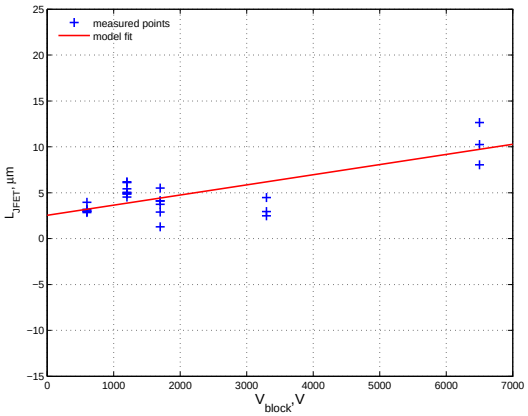


Figure 3.27: IGBT JFET region length L_{JFET} parameters shown in +, against V_{block} with model fit from eqn. (3.92). The method by which p_3 and p_4 is identified is described in subsection 3.5.6.

analytically in eqns. (3.91)-(3.92):

$$L_a = p_1 V_{block} + p_2 \tag{3.91}$$

$$L_{JFET} = p_3 V_{block} + p_4 \tag{3.92}$$

where p_1, p_2, p_3, p_4, are constants to be found.

Notice that, as the numerical results suggest (see Table 3.1), it can be assumed that L_a and L_{JFET} do not depend on I_R but only on V_{block}.

The Figure 3.28 plots show the calculated area A against the rated current I_R, and results for all the cases are given for a range of IGBT voltage classes, manufactured commercially. Clearly, it can be seen that A varies linearly with I_R for a given V_{block}. Hence:

$$A \propto I_R \quad \text{(for a given blocking voltage)} \tag{3.93}$$

which interestingly is the same scaling rule as in the case of power MOSFETs (refer eqn. (3.63)). The dependence of A on V_{block} is not as straightforward to establish. In order to do so, we now turn to describe the dependence of power conduction loss on IGBT area.

The next aim is to develop an analytical model for power conduction loss against area in minority carrier devices. Intuitively, one might it expect them to be proportional to each other, as was the case with majority carrier devices. But because the geometry of the device is different (an extra junction) the result is linear with an additional constant offset.

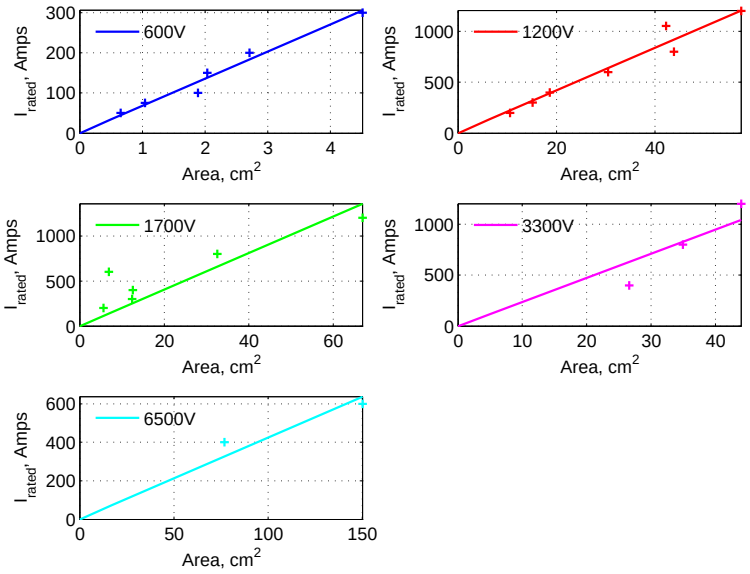


Figure 3.28: The IGBT rated current versus area for range of blocking voltages. Measured points are shown with +. A straight line fit from eqn. (3.102) is also illustrated with p_5 and p_6 identified according to the method described in subsection 3.5.6.

Considering the fact that

- the current density J_R, a ratio of A and I_R is solely dependent on V_{block} (which verifies our assumption in eqn. (3.93)); and
- forward voltage drop v_f changes only with V_{block};

it is interesting to see how both normalized area (on I_R) and v_f relate to one another.

Figure 3.29 plots v_f against A/I_R for the devices studied. It illustrates that both these quantities have a linear relationship, with an offset β. The plot strongly suggests that:

$$v_f = \alpha \left(\frac{A}{I_R} \right) + \beta \tag{3.94}$$

where α is the slope of the straight line and β is the constant offset of v_f from the origin, shown as solid red line in the Figure 3.29, with found α of 1.075×10^5, and β of 2.39.

When eqn. (3.94) is multiplied by I_R, it can be seen that power conduction loss is proportional to the area with a constant offset (dependent on rated current) which can be represented as:

$$P_{cond} = \alpha A + \beta I_R \tag{3.95}$$

The determined values of α and β from the Figure 3.29 plot and model eqn. (3.95), consequently can be used to plot against the calculated values (data points) of P_{cond} and

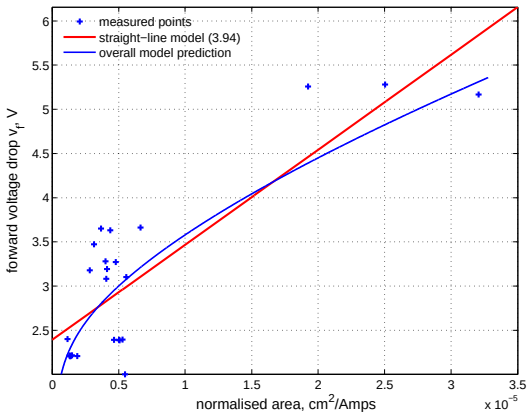


Figure 3.29: Illustrates how the forward voltage drop v_f varies with normalized area of the device. Measured points are shown with + and curve fitted with a straight-line model (3.94) (red line) and overall model fit (blue line) with identified parameters according to the method described in subsection 3.5.6.

A for each device from Table 3.1 and Table 3.2, to complete the analysis, as depicted in Figure 3.30.

The standard power conduction loss equation for a standard IGBT is:

$$P_{cond} = v_{on} I_R + I_R^2 R_{slope} \tag{3.96}$$

where v_{on}, is the on-state voltage drop (*knee* point, refer Figure 3.22) of the device.

Drawing on detailed analysis in the previous section, v_{on} is the voltage drop resulting from the addition of $v_{junction}$ and v_{drift}. Therefore, the first term, shows the conduction losses happening in the 'junction' and the 'drift' regions. The second term is responsible for the losses in the JFET region - the 'slope' of the I-V curve. Equating eqn. (3.95) with (3.96) and solving for area:

$$A = \frac{I_R}{2\alpha}\left[(v_{on} - \beta) \pm \sqrt{(v_{on} - \beta)^2 + 4\alpha\rho_{JFET}L_{JFET}}\right] \tag{3.97}$$

Substituting the expression for ρ_{JFET} given in eqn. (3.16), yields:

$$A = \frac{I_R}{2\alpha}\left[(v_{on} - \beta) \pm \sqrt{(v_{on} - \beta)^2 + \frac{8\alpha V_{block}L_{JFET}}{E_{\max}^2 \mu_e \varepsilon_o \varepsilon_s}}\right] \tag{3.98}$$

Since $\alpha, V_{block}, L_{JFET}$ and E_{max} are all positive quantities so

$$\sqrt{(v_{on} - \beta)^2 + \frac{8\alpha V_{block}L_{JFET}}{E_{\max}^2 \mu_e \varepsilon_0 \varepsilon_s}} > (v_{on} - \beta),$$

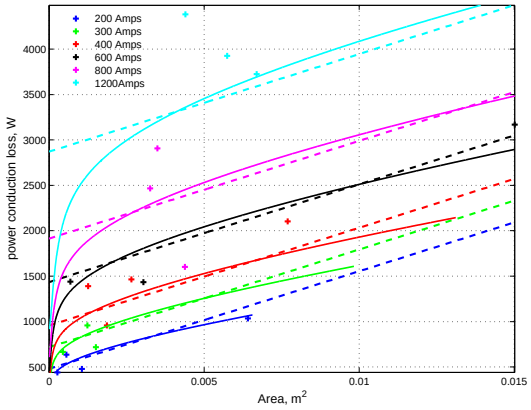


Figure 3.30: Power conduction loss in IGBTs plotted against the area of the device for a range of rated current. Measured points are shown with + and model eqn. (3.95) is represented by the broken line. The solid lines are obtained from the overall model. Matching colours correspond to the same current rating.

and the negative square root gives a negative area, which is meaningless, so the physical answer is the positive square root of eqn. (3.98), yielding:

$$A = \frac{I_R}{2\alpha}\left[(v_{on}-\beta) + \sqrt{(v_{on}-\beta)^2 + \frac{8\alpha V_{block} L_{JFET}}{E_{\max}^2 \mu_e \varepsilon_0 \varepsilon_s}}\right] \tag{3.99}$$

To derive the final area expression, it is essential to build and verify the $v_{on} - V_{block}$ model, and ultimately substitute back into eqn. (3.99). The behavior of the data shown in the Figure 3.31 plot suggests that the variation of v_{on} with V_{block} can be described as:

$$v_{on} = a_1 V_{block} + b_1 \tag{3.100}$$

where a_1 and b_1 are constants and represent the slope and the offset values respectively. Eqn. (3.100) can be rewritten as:

$$v_{on} - \beta = \underbrace{a_1}_{p_5} V_{block} + \underbrace{b_1 - \beta}_{p_6} \tag{3.101}$$

which is another straight-line parameterised in terms of p_5 and p_6 which are given through overall model identification in section 3.5.6. By choosing β as 2.39 as found previously: b_1 can be calculated as $p_6 + \beta$, and also $a_1 = p_5$ and hence eqn. (3.100) can be plotted onto the collected data-points as shown in Figure 3.31. The fit of the data-points at the assumed straight line relation (3.100) is sound, closely following the overall model prediction given by the solid red line.

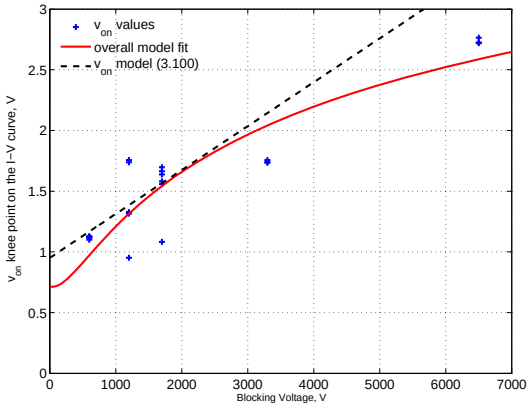


Figure 3.31: NPT-IGBTs v_{on} vs V_{block}. Measured points with +. The broken line is plotted using eqn. (3.100), whereas the overall model prediction is depicted by the solid line.

Now substituting eqn. (3.92), (3.101) and replacing α with the parameter p_7 in eqn. (3.99), the area expression finally becomes:

$$A = \frac{I_R}{2p_7}\left[p_5 V_{block} + p_6 + \sqrt{\left(p_5 V_{block} + p_6\right)^2 + \frac{8p_7 V_{block}\left(p_3 V_{block} + p_4\right)}{E_{\max}^2 \mu_e \varepsilon_0 \varepsilon_s}}\right] \tag{3.102}$$

Just as we expected, area turns out to be proportional to the rated current of the device (when V_{block} is fixed), as illustrated in Figure 3.28. Indeed, it is reassuring that the scaling law presented (eqn. (3.102)) from our analysis, agrees with the acquired area calculations. Further plotting the alternate scenario: area against V_{block} (when I_R is fixed) in the Figure 3.32 with the built model (3.102) with p values given Table 3.3, satisfies all the cases well.

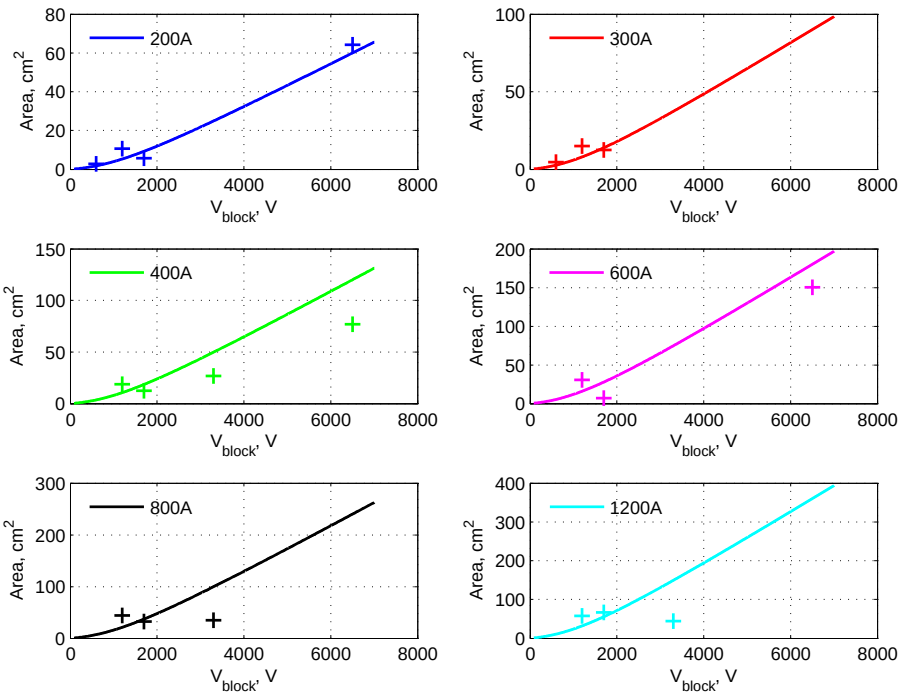


Figure 3.32: IGBTs calculated area against varying blocking voltage. Measured points are shown with + and model (eqn. (3.102)) prediction is shown with solid lines.

In practice, however, room for some 'tweaking' can conspire to complicate the state of affairs. This does not, however, invalidate the simple assumptions used above. These scaling laws will be validated using another approach shortly, reinforcing that the assumptions, theory and results are all aligned.

3.5.6 Optimal Parameters (p values)

The data gathered from 25 cases of IGBTs investigated earlier and the analytical models derived, can be used to identify the seven unknown parameters $p = [p_1, p_2, p_3, p_4, p_5, p_6, p_7]$ through an exhaustive full parameter search which is computationally intensive and on which the overall model identification is dependent. The initialised values were varied in the optimisation to obtain minimum possible error between the measured and predicted data, whilst ensuring that the optimal parameters did not violate any relevant constraints.

Unknown parameters are determined by solving the following least squares optimisation

problem using the *fmincon* Matlab function:

$$\underset{p}{Min} \sum_{(i,j)} \left(v_{(i,j)} - v_{junction(i,j)} - v_{drfit1(i,j)} - v_{drift2(i,j)} - v_{JFET(i,j)} \right)^2$$

where index i spans the 25 IGBT devices, and j spans all the data points within each device's characteristic. $v_{junction}$, v_{drift1}, v_{drift2} and v_{JFET} are the model predictions for the corresponding voltage drops. Added together, they amount to the predicted forward voltage. In order to calculate them it is required to use the actual current, blocking voltage and rated current values. v is the measured forward voltage. The p values obtained from the optimisation are given in Table 3.3.

Table 3.3: Best-fit parameter values used for overall model identification.

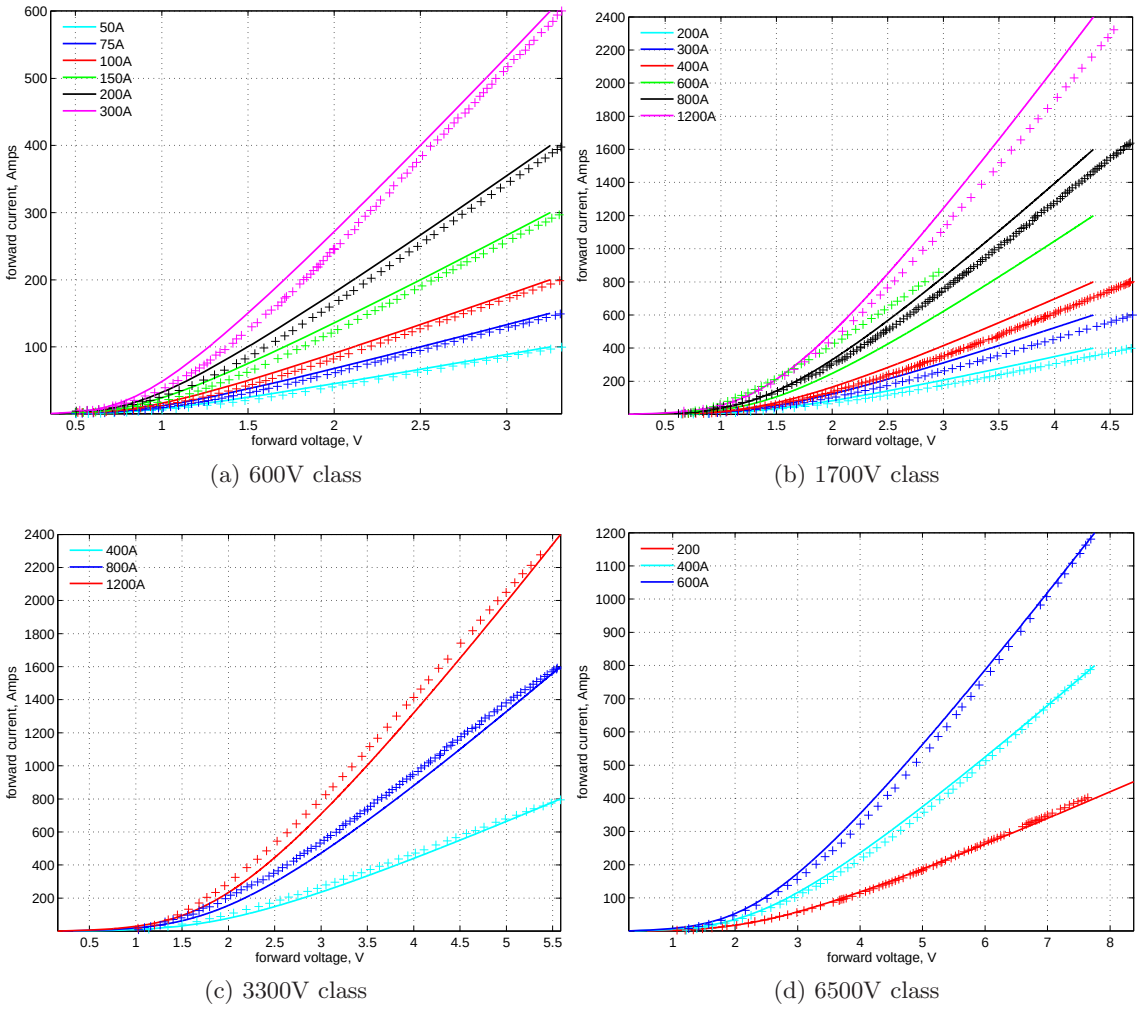
p_1	p_2	p_3	p_4	p_5	p_6	p_7
2.6542×10^{-8}	1.4135×10^{-5}	17.746×10^{-10}	1.2271×10^{-6}	0.0003616	-1.4415	1.09×10^{5}

Employing the mathematical models (3.91), (3.92) and (3.102) (derived above) and feeding the parameters identified (given in Table 3.3) back into these models, we can built an overall universal IGBT model, reproducing accurate *I-V* curves, and compute conduction losses for all ratings. Interpolation and extrapolation to any rating, which is a highly desirable feature, is also possible.

3.5.7 Performance of Overall IGBT *I-V* Model

The overall IGBT model is constituted on the model based L_a, L_{JFET} and R_{slope} (or *Area*) calculated through the parameter optimisation process and the best-fit parameter values of Table 3.3. Using the set of derived equations presented in subsection 3.5.2 and the new identified parameters L_a, L_{JFET} and R_{slope} we can predict the total on-state voltage drop and model other properties of a device without using any accumulated data of Table 3.1-3.2 other than specifying the device in terms of its V_{block} and I_R.

The quality of the best-fit using the optimised parameters is depicted in Figure 3.26 to 3.36. The correspondence of model fit to measured data from the given identified parameters is evident in these results. The results demonstrate that the numbers given in Table 3.3 globally satisfy the scaling laws built in this work.



(a) 600V class

(b) 1700V class

(c) 3300V class

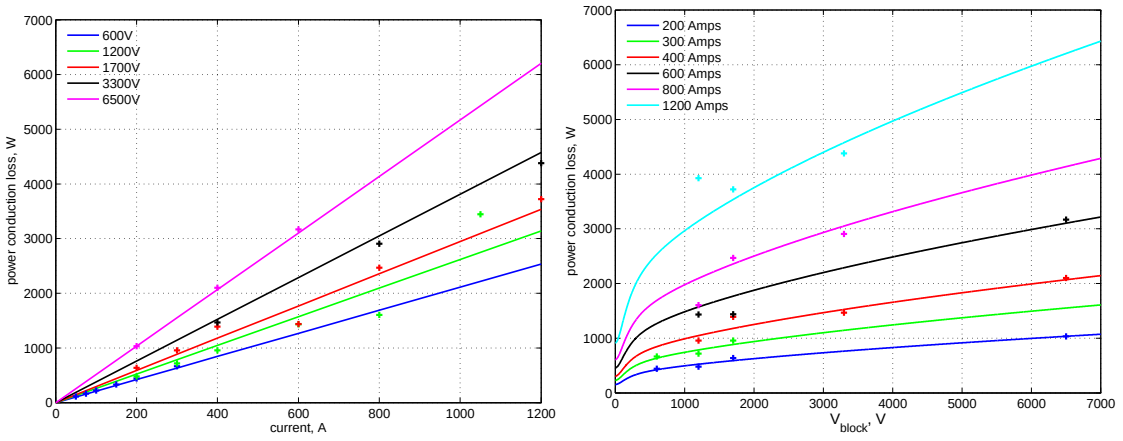
(d) 6500V class

Figure 3.33: IGBT overall model performance vs manufacturer device datasheets. Illustrating the final I-V curve of all the devices built on the basis of model based L_a, L_{JFET}, R_{slope} substituted into the derived eqns. of $v_{junction}$, v_{drift1}, v_{drift2}, and v_{JFET} to estimate the conduction characteristics. The cross symbols + depict manufacturer data points; the solid line is the derived overall model.

Analytical results obtained for I-V curves for each device from the overall optimisation are contrasted with the manufacturer datasheets in Figure 3.33, to assess the accuracy that the overall IGBT model is intended to represent. The results suggest that the agreement between the model prediction and the manufacturer measurements throughtout the range is remarkable (comparable to the individual identifications carried out in Subsection 3.5.3; with sample results depicted in Figure 3.25) except in couple of cases. These curves are reproduced only on the basis of the 7 p values. In this way reassurance is provided that the generic overall model can be employed with confidence to predict IGBT

characteristics for any rating, accurately reveals underlying key design parameters, and enables power conduction loss calculations.

The rated conduction power losses in IGBTs were calculated from manufacturer datasheets using the individual identifications in Subsection 3.5.3, and presented in Table 3.2, to see the trend and prove that the predictive capacity of the derived analytical model uses Table 3.3 parameters is reasonable. In Figure 3.34, power conduction loss is plotted against varying rated current (fixed V_{block}), and against blocking voltage (fixed I_R). In each case $P_{cond-max} = v_f \times I_R$ is used.



(a) (b)

Figure 3.34: Power conduction loss in IGBTs against varying: (a) rated current (fixed V_{block}) (b) blocking voltage (fixed I_R). Manufacturer measured values are shown with + and are found by the product of v_f and I_R from Table 3.2. The solid line curves are plotted using overall model.

As can be seen from Figure 3.34(a) the curve for variable current and constant blocking voltage appears to be a straight line and fits the data well. The linear dependence to I_R is reinforced by the argument made in Subsection 3.5.4 that v_f only depends on V_{block}, and thus $P_{cond-max} = v_f \times I_R$ or $P \propto I_R$.

It can be seen from Figure 3.34b that where blocking voltage varies (and rated current is fixed), power loss varies similarly to a square root with an offset from the origin, with the model prediction fitting the measurments well. The offset is due to the additional on-state junction drop in IGBTs. Note that so far NPT IGBTs are investigated.

It is informative to consider the trend of R_{slope} with device ratings, with respect to I_R and V_{block}, as done previously for the v_{on} component of the power loss expression (3.96).

The second component R_{slope} of eqn. (3.96) is quantified by deriving for R_{slope} in terms of the identified parameters of the overall model. Substituting eqn. (3.9) and eqn. (3.91), into α_{pnp} and using eqn. (3.92), (3.12), (3.102) into (3.89), we obtain:

$$R_{Slope} = \frac{\left[-(p_5 V_{block}+p_6)+\sqrt{(p_5 V_{block}+p_6)^2+\frac{8p_7 V_{block}(p_3 V_{block}+p_4)}{E_{\max}^2 \mu_e \varepsilon_0 \varepsilon_s}}\right]}{2I_R\left(1-\frac{1}{\cosh\left(\frac{\frac{2V_{block}}{E_{\max}}}{p_1 V_{block}+p_2}\right)}\right)} \tag{3.103}$$

Expression (3.103) shows that the slope resistance R_{slope} of a device is inversely proportional to the rated current (for fixed blocking voltage). Eqn. (3.104) expresses this relationship, and the plot of device slope resistance against varying I_R in Figure 3.35, proves it.

$$R_{slope} \propto \frac{1}{I_R} \text{(for a given blocking voltage)} \tag{3.104}$$

The overall model-fit of R_{slope} data points using the eqn. (3.103), and utilising identified parameters p, is good.

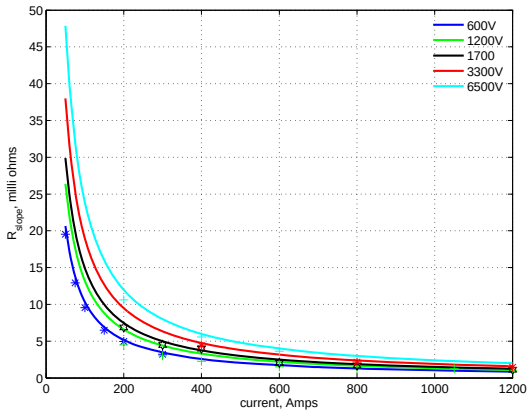


Figure 3.35: IGBT slope resistance R_{slope} vs I_R. The curve fits are plotted using eqn. (3.103).

3.6 Generalized IGBT and *pin* diode Conduction Loss Scaling

At the instigation of deriving power conduction scaling laws in minority carrier devices the forward conduction characteristics of IGBTs were modelled in previous Subsections 3.5.1

to 3.5.6. The design parameters, individual voltage drop contributions in various device regions, the functional relationships of key model parameters which govern the optimal device performance, together with the measurements given by the manufacturer and ultimately power loss variance scenarios with blocking voltage and rated current, have been unveiled step-by-step.

These high-fidelity models are critical to the accurate prediction of I-V curves for a range of IGBTs (existing and yet to be developed), and for understanding the complexities of device physics. However, we can take a further step, and derive one simple and accurate enough model with a single parameter, to readily determine power conduction losses in minority carrier devices, without becoming swamped by excessive detail and extensive simulation. This simple model contains one unique coefficient, and can cater sufficiently to the requirements of circuit designers in industrial and consumer electronics.

We have already established a reasonable approximation for power loss given in eqn. (3.95). Upon substitution of eqn. (3.99) into eqn. (3.95), we get:

$$P_{cond-\max} = \frac{I_R}{2}\left[(v_{on}+\beta) + \sqrt{(v_{on}-\beta)^2 + \frac{8\alpha V_{block} L_{JFET}}{E_{\max}^2 \mu_e \varepsilon_0 \varepsilon_s}}\right] \tag{3.105}$$

or

$$P_{cond-\max} = \frac{I_R}{2}\left[(v_{on}+\beta) + \sqrt{(v_{on}-\beta)^2 + V_{block} k_{icls}}\right] \tag{3.106}$$

where: $k_{icls} = 8\alpha L_{JFET}/E_{\max}^2 \mu_e \varepsilon_0 \varepsilon_s$. Further simplifying assumptions are made:

- v_{on} is linearly dependent with V_{block} according to eqn. (3.100) and as seen in Figure 3.31 (in the case of the NPT-IGBTs). a_1 and b_1 are found via best line fit of the $v_{on} - V_{block}$ data pairs.
- β is equal to the value of the offset b_1 in eqn. (3.100).
- L_{JFET} does not depend on V_{block} (it is a constant) which can be reasonably assumed in the case of NPT IGBT from examining Figure 3.27.

These assumptions imply that k_{icls-N} is a constant and eqn. (3.106) becomes:

$$P_{cond-\max} = \frac{I_R}{2}\left[a_1 V_{block} + 2b_1 + \sqrt{a_1 V_{block}^2 + V_{block} k_{icls}}\right] \tag{3.107}$$

3.6.1 IGBT (NPT and PT) and *pin* Diode Conduction loss Scaling Constants

A similar procedure to the one followed for MOSFET devices in Subsection 3.4.5 can be used to identify the 'unique' scaling constant that characterises power conduction losses for minority carrier devices such as IGBTs and *pin*. Parameter k_{icls} can be identified and used in eqn. (3.107) to predict power conduction losses in a quick manner. The approach taken previously involved separate curve fitting of the power losses for devices grouped in two different ways: 1) same blocking voltage but varying rated current, and 2) same rated current but varying blocking voltage. The scaling constant was then identified independently for each case, with a good overall match to any degree of approximation. This process was dependent on the existence of a good set of experimental data from the manufacturer.

A slightly different procedure is chosen here for the calculation of k_{icls} simply because there is less available device measured data. Instead of identifying the scaling parameter in stages, which nevertheless provides further insight into the physics of power losses, the identification of the single parameter is attempted at once. The complete set of data, comprising power loss estimates from Table 3.2 for all cases of rated current and rated voltage, was utilised via a least squares approximation of the power loss equation (3.107) to identify the only unknown, the scaling constant k_{icls}. The power loss equation is nonlinear and involves two independent variables, V_{block} and I_R. Therefore the advanced optimisation algorithm, sequential quadratic programming, provided by the MATLAB function *fmincon* was again used to perform the least squares approximation.

In the case of NPT-IGBT, k_{icls-N}, calculated for NPT-IGBTs was found to be: 0.0071V and substituted back into the expression (3.107) and plotted against the data, to verify, as shown in Figure 3.36. For further comparison, it was decided to plot the overall high-fidelity model from Figure 3.34(b) on top of it, to broadly indicate how close these two models are.

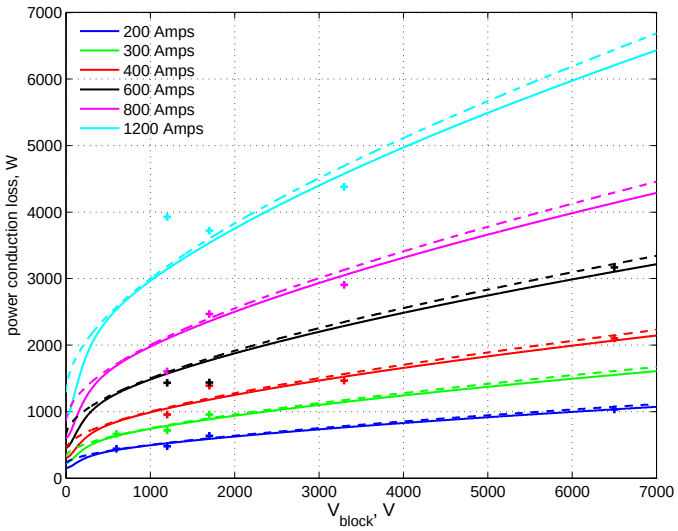


Figure 3.36: Power conduction losses in NPT-IGBT. Comparison of results obtained in the previous subsection and plot of Figure 3.34(b) high fidelity model represented in solid lines, with the simplified model eqn. (3.107) represented in broken lines.

As can be seen from Figure 3.36 the derived simple model eqn. (3.107) plotted in broken lines, is surprisingly close to the results obtained through the complex model from detailed analysis, shown in solid lines. It is therefore possible to predict power conduction losses in minority carrier devices through a simplified model using only one constant coefficient, without having to resort to the sophistication needed to build a high fidelity IGBT overall model, capturing micro-level device physics details. Notwithstanding the claim it is expected that highest overall benefit will accrue from a combined use of the complex and simplified models.

PT-IGBTs and *pin* diodes can be treated in the same way, relating to their respective $v_{on}-V_{block}$ plots. The values of v_{on} were directly extracted from manufacturer data-sheets [130] and eqn. (3.100) was plotted through the data-points, as shown in Figure 3.37.

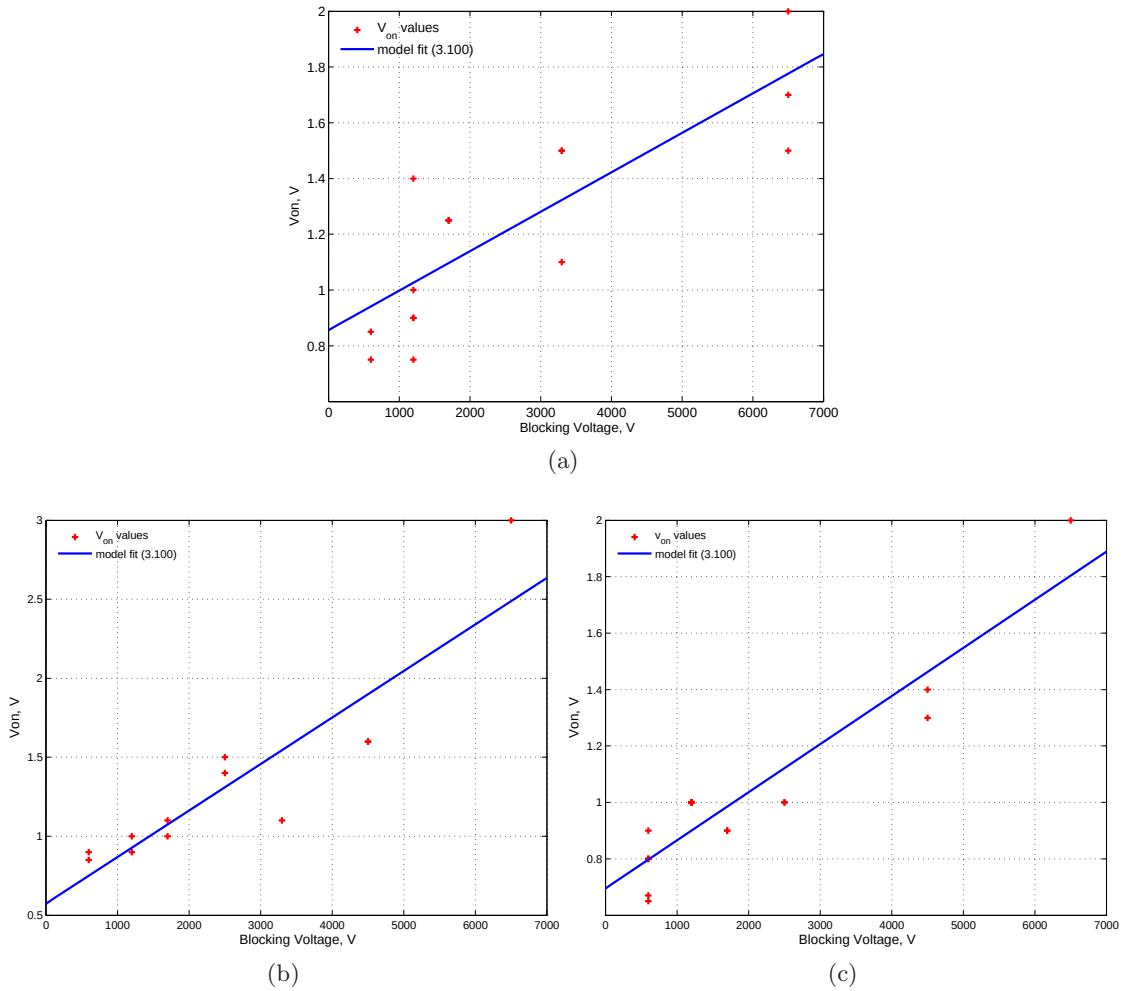


Figure 3.37: v_{on} vs V_{block} (a) *pin* diodes with NPT-IGBT package (Infineon) (b) PT IGBT (Mitsubishi) (c) *pin* diodes associated with PT-IGBT package (Mitsubishi).

The slope (a_1) and off-set (b_1) values of the straight-linear fit of Figure 3.37 plots was substituted into the power loss expression (eqn. (3.107)) to allow identify the general (universal) constants for PT-IGBTs and *pin* diodes. These scaling numbers were again fed into the simplified model (eqn. (3.107)) and plots made against the data, to validate the relationship, as shown in Figure 3.38. The assigned symbols and derived constant values are:

- NPT IGBT, k_{icls-N}: 0.0071V and associated *pin* Diode's, k_{dcls-N}: 0.0030V
- PT IGBTs, k_{icls-P}: 0.0064V and associated *pin* Diode's, k_{dcls-P}: 0.0029V

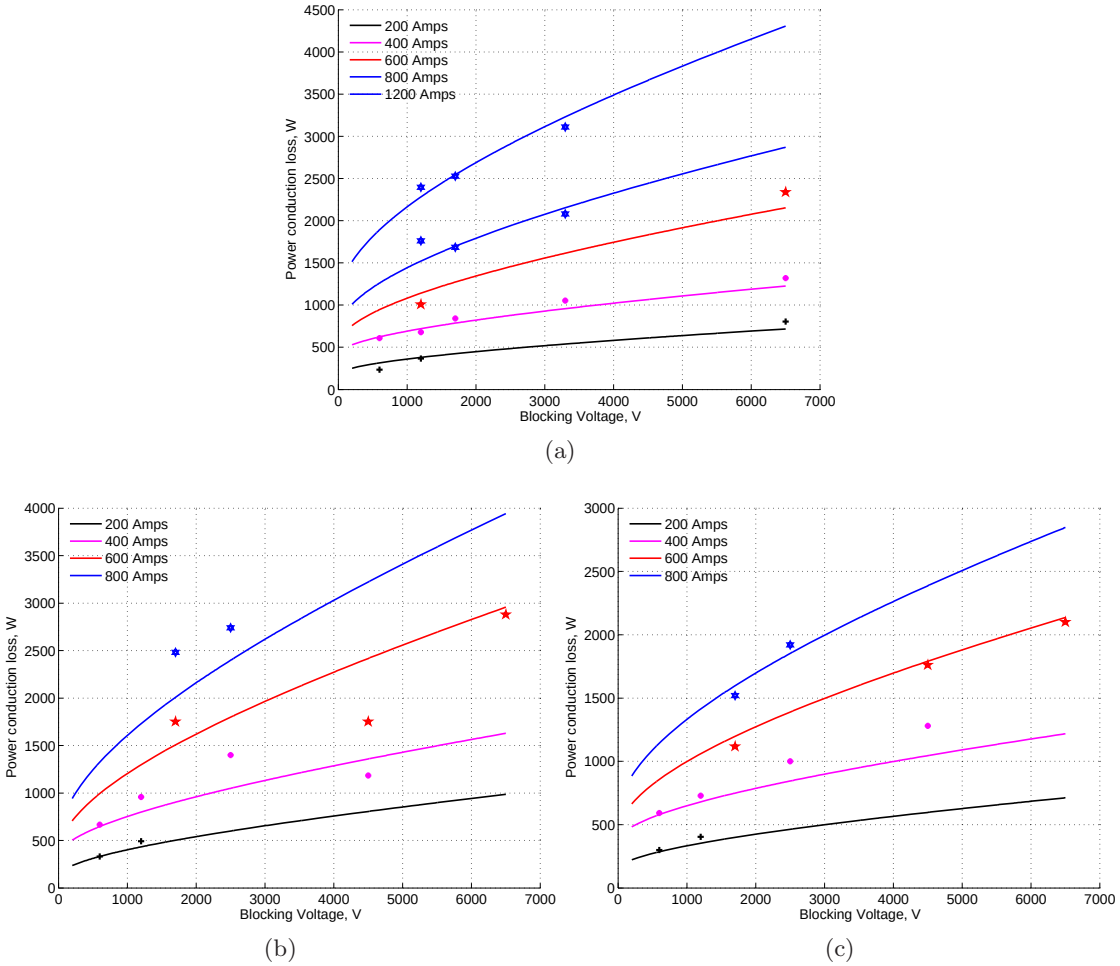


Figure 3.38: Power conduction loss at rated blocking voltage and fixed current (a) *pin* diodes with NPT-IGBT package (Infineon) (b) PT IGBT (c) *pin* diodes with PT-IGBT package (Mitsubishi)The cross symbols correspond to manufacturer data, and the solid lines to the simplified model eqn. (3.107) prediction.

Notably, the derived scaling number of PT IGBTs is lower than that of NPT-IGBTs. This confirms PT IGBTs improved conduction performance. This was elaborated on theoretically in section 2.9, where it was mentioned that a compromise solution is sought in PT structures: to strike a balance between forward drop, switch speed and collector output resistance. On-state voltage drop and turn-off time, based on the device design, showed that the PT IGBT yields lower power losses. This matches well with the analysis carried out in this section.

Figure 3.39 substantiates what was established in Section 3.5.5 for minority carrier devices: that power conduction loss will vary linearly with varying rated current (when V_{block} is fixed).

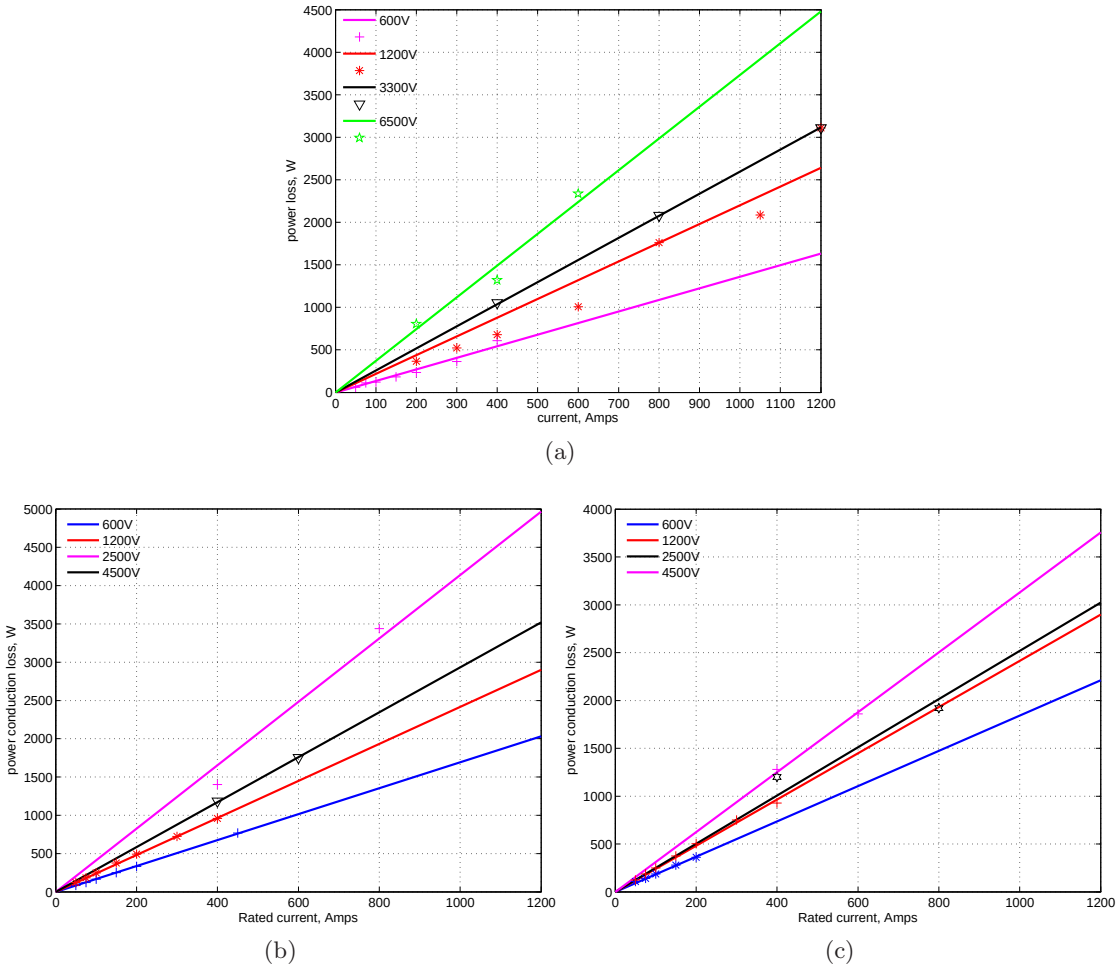


Figure 3.39: Power conduction loss at rated current and fixed blocking voltage (a) *pin* diodes with NPT-IGBT package (Infineon) (b) PT IGBT (c) *pin* diodes with PT-IGBT package (Mitsubishi).

3.7 Discussion and Practical Application

Device modeling and simulation can take on several different meanings, depending upon one's perspective [131]. For a device designer, simulation typically means using a detailed model of the physical operation of a particular structure to check device design variations without fabricating the structure. This would include variations in doping densities and profiles, vertical and lateral dimensions, and so forth. For a system or circuit designer, simulation typically means using a somewhat simplified (reduced or compact) model of the device that is physically accurate enough to describe device circuit behavior, but computationally simple enough (efficient) to be used in a full circuit or system simulation.

It is particularly valuable to build analytical models for high power semiconductor devices using parameters related to the scaling of the power losses. This work was directed towards the development of general representative laws, accurate to scale and predict device losses in a more simplified and qualitative way, giving basic as well as deeper insight as to what happens when designers substitute one device family with another. In this chapter, the derived scaling laws attributable for power losses in power MOSFETs, IGBTs and *pin* diodes indicate conduction loss as a function of device rating. These simple formulae are consistent with manufacturer data sheets, substantiating the analysis presented.

Conduction scaling loss coefficients for each device: power MOSFET, IGBT (NPT and PT), and *pin* diode have been derived by this work. These scaling laws and constants:

- facilitate computation of power losses for any rating of a given device family including extrapolation beyond manufacturers' data;
- minimise the need for detailed knowledge and interpretation of a manufacturers' data for appropriate device selection in circuit design;
- indicate the rating range over which each device is a good choice, e.g. the MOSFET is preferred at low voltage/current, whereas the IGBT is preferred at high voltage/current;
- enable a circuit designer to compute losses quickly, without the need to consider device physics in detail, or search for device data sheets - a potential increase in circuit efficiency by over-rating the device.

Figure 3.40 demonstrates the potential of the scaling laws built. It compares the power conduction loss of power MOSFETs and IGBTs, simply on the basis of the scaling laws and constants built in this chapter (without using any manufacturers data sheets). This is the practical significance of this work.

Figure 3.40 not only validates the trends established earlier on the basis of device physics, but also informs us that while MOSFET is a preferred device for voltages up to 500 volts, at higher blocking voltages the IGBT suffers less conduction loss. This is because power MOSFET on-resistance increases rapidly at higher voltages, resulting in a need to derate the current handling capability more severely than for the IGBT. This conforms with Chapter 2's detailed comparison of expected performance characteristics. It is clearly the reason why device manufacturers produce IGBTs at higher ratings (600 volts and above) and MOSFETs at lower ratings (500 volts and below).

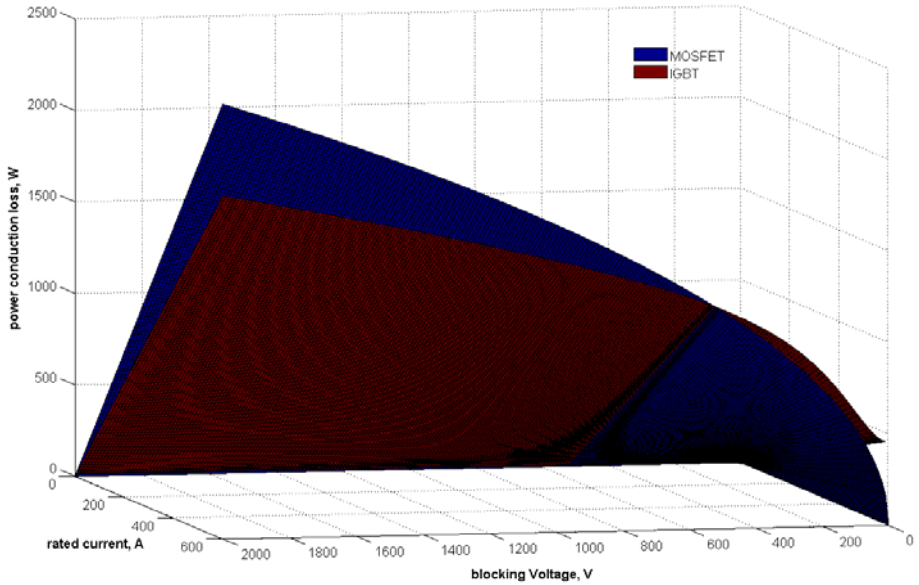


Figure 3.40: Power conduction loss: overall comparison between MOSFETs and IGBTs utilising the scaling laws and constants derived in this chapter.

3.8 Conclusions

Analytical models for scaling power losses can be built for a range of device ratings by applying the physical principles of device operation. These models are applicable to devices that fall within the ratings currently available from manufacturers and should also be applicable to larger devices. In this chapter, a set of equations was derived for calculating device power conduction losses for power MOSFETs, IGBT (NPT and PT) families and *pin* diodes. These analytical models compute power losses in good agreement with manufacturer's data, thus establishing their validity.

The idea was to use a physics based semiconductor device modeling approach and subsequently examine the commonly used power loss calculation method in the light of the new physical insights. These equations have been developed after careful study of the main classes and types of devices on the market, and allow the circuit designer to quickly estimate circuit losses and determine the sensitivity of those losses to device voltage and current ratings when choosing semiconductors for specific applications.

This chapter analyses MOSFET, IGBT and *pin* device designs with a view to understanding their relative merits, and in order to find optimal design criteria of state-of-the-art devices manufactured by industry experts. Simplified expressions for the planar p^+/n^-

junction design to sustain breakdown voltage conditions, forms the initial qualitative guide in the first part of the chapter covering power MOSFETs (majority carrier devices) design and scaling laws. In this regard, we derive an optimal doping $n_D(x)$ profile (refer eqn. (3.38), Section 3.4.2) shown to best exploit the device design such that overall on-resistance is minimal without losing blocking performance. The derived doping profile $n_D(x)$ for actual power MOSFETs is shown to fit well with commercial devices (International Rectifier). It has 33% increased blocking capability for the same drift region length, and reduced on-resistance by 25% for the same blocking capability, as compared to a MOSFET designed with a uniform doping density profile.

An important assumption of the analysis was that the power loss per unit area of the device is constant, because if the thermal resistance is inversely proportional to die area we can safely assume a constant power loss per unit area of die. It was found that the area of majority carrier semiconductor devices (such as a MOSFET) is proportional to the product of the rated current and square root of the blocking voltage. In other words, the conduction power loss (at rated current) increases linearly in relation to the variable rated current when blocking voltage is fixed. Similarly, the conduction power loss (at rated current) increases as a square root of the variable blocking voltage when rated current is fixed. These scaling laws were successfully verified against manufacturer data measurements for a vast range of power MOSFETs.

The second part of the chapter analysed conduction loss in IGBTs and *pin* diodes. We derive a generic and unified physics-based overall IGBT model that is capable of predicting exact on-static characteristics of any feasible rating. The governing IGBT design parameters such as ambipolar diffusion length L_a, JFET region length L_{JFET}, *Area* of the device, slope resistance R_{slope} (related to the JFET region resistance) and the thickness of the drift n^- region length L_n for a range of commercially available IGBTs were identified from the derived analytical model presented in section 3.5.3 (see summary Table 3.1). Moreover, their functional relationships with blocking voltage and rated current were also furnished in Section 3.5.5, to aid in deriving an overall IGBT model. The analysis also exposes the forward voltage drop contribution from distinct regions of an IGBT (see Table 3.2) during the forward conduction mode (junction, drift and JFET), and clearly indicates the regions responsible in forming the 'knee' and 'slope' parts of the *I-V* curve (refer Table 3.2). The overall model provides a sufficient basis for understanding key IGBT parameters, and is devised to fit as closely as possible to all aspects of the IGBT as well as to predict conduction power losses (Figure 3.26 to Figure 3.35).

In the case of power conduction scaling laws for minority carrier devices (such as a *pin* diode or IGBT), a similar linear relationship is observed for variation of current (where the blocking voltage is fixed) as is seen in power MOSFETs. But where the blocking voltage varies (and the rated current is fixed), power losses are described by a square root relationship with an offset (from the origin) relationship. This is due to the additional junction voltage drop. Also the slope resistance of the device is inversely proportional to the varying rated current.

Using the power loss graph of Figure 3.40, a device designer can easily select the appropriate rating for the intended industrial application. The simplified conduction scaling laws presented in equations (3.71) and (3.107), and the five new constants derived for majority and minority carrier devices, allow a circuit designer to compute losses quickly, without needing to apply detailed device physics or search for device data sheets. This study compares analytically derived findings with data points from a body of manufacturer device data, including MOSFETs, NPT and PT IGBT devices (and associated *pin* diodes). Plotting that data against the predictive models built, has validated their robustness.

Having catalogued power loss analytical models for each type and range of device ratings in this chapter, the ensuing chapter will focus on high density power converters. The generalized formulae derived here are of great relevance in the design process of high density power converters themselves, and their multilevel deployment on power networks.

Chapter 4

The Multi-level converter

4.1 Introduction

In this chapter different topologies of multi-level converter will be surveyed and compared. First a single-module converter will be introduced and its limitations discussed. Multi-module converters, which overcome some limitations of single-module converters, will then be presented. These converters are assessed in terms of functionality and design. The operating principle of each particular converter topology, and its advantages and disadvantages for the implementation of modern FACTS devices are briefly discussed. The focus is mainly on established and commercialised multi-level converter types, their structures and their advantages and disadvantages, also present comparisons of these topologies reported in the literature so far.

4.2 Why multi-level?

The voltage blocking levels required in the power electronic equipment connected to distribution grids are often larger than the voltage ratings of individual power semiconductor devices. One option to solve the voltage rating problem presented to the semiconductors is to reduce the line-voltage using a coupling transformer [132,133]. The transformer has to be rated to the nominal power, and thus its volume is a large problem of the converter size. Thus it is desirable to work with as high voltage as possible on the electronics side of the converter in order to remove the coupling transformer. Classically, two-level inverters have been used [134]. A further option is to continue using a two-level converter but with series-connection of the semiconductors (known as valves). However, it is difficult

to ensure that the entire voltage is equally distributed in all the semiconductors. It can be especially difficult to ensure that the dynamic voltage balance across all the semiconductors devices and auxiliary circuits is balanced during the commutations [135, 136].

Industry has begun to demand higher power equipment, which has now reached the megawatt level [137]. Despite the notable progress made in recent years in power device technology, at high voltage and power levels, ideal or quasi-ideal semiconductor switches are not available. At present, "ideality" of the switches can be attained only for medium and low powers, if traditional converters topologies are used. The standard 6-switch, 3-phase voltage source inverter shown in Figure 4.1 produces an output voltage with levels of either $\pm V_{dc}/2$ on each phase. It is known as a two-level (2-L) inverter with the primary function to convert a fixed dc voltage to a three-phase ac voltage with variable magnitude and frequency.

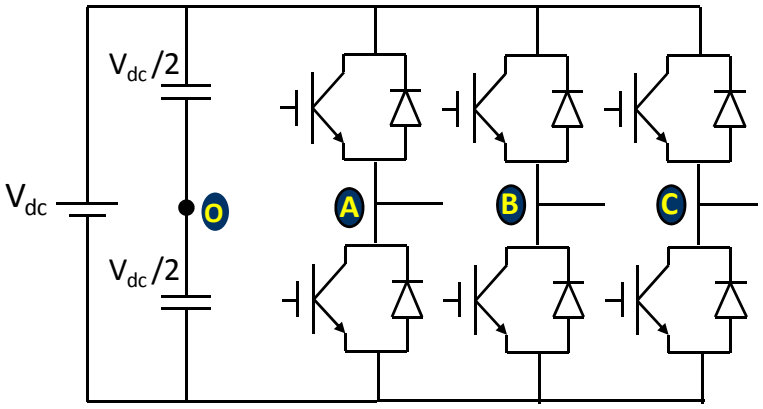
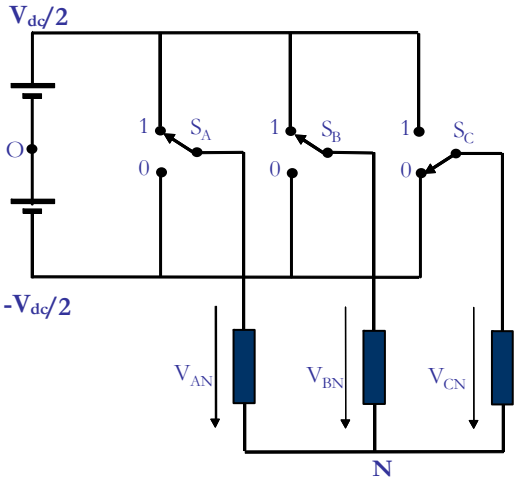


Figure 4.1: Simplified two-level inverter for high-power applications.

To obtain a high quality output voltage waveform with a small amount of ripple, a high switching frequency combined with various pulse-width modulation (PWM) strategies [138] are required. In high-power and high-voltage applications, these 2-L inverters have limitations operating at high frequency, due to switching losses of devices at these ratings [139]. Moreover, it is desirable that semiconductor switching devices are used in a manner that avoids the problems of static and dynamic current and voltage sharing associated with series-parallel combinations. Another major limitation for two-level modules is that if one single semiconductor valve fails, that converter can no longer function. A two-level inverter model is shown in Figure 4.2 with its switching states. It can be observed that only one commutation per cycle takes place. State 'S_2' is also highlighted in the resulting output waveform shown in Figure 4.3.



	Switches		
States	S_A	S_B	S_C
S0	0	0	0
S1	1	0	0
S2	1	1	0
S3	0	1	0
S4	0	1	1
S5	0	0	1
S6	1	0	1
S7	1	1	1

Figure 4.2: Two-level inverter model and switching states.

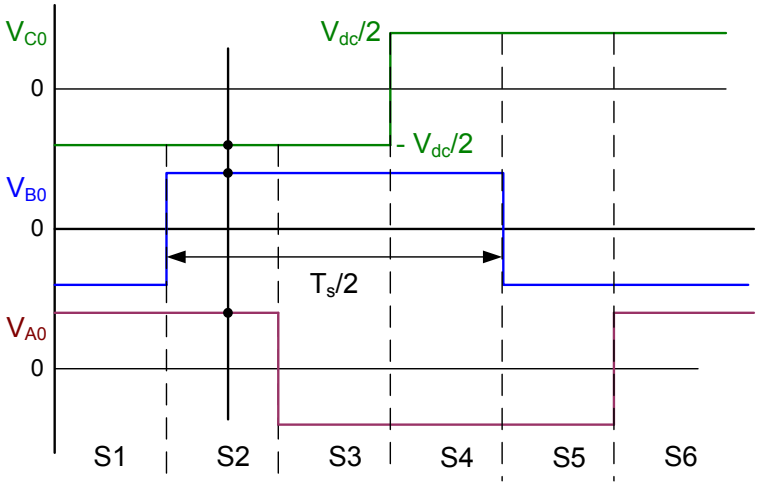


Figure 4.3: Three phase square wave voltage in each leg of the converter as per the switching states of Figure 4.2 (S_2 can be seen).

To summarise, the use of a single module converter such as a 6-pulse converter [140] (Figure 4.1) can be challenging for the following reasons:

1. To achieve the required voltage and current ratings for the converter, with present (and near term expected) semiconductor technology, semiconductor devices must be connected in series/parallel. These multi-device switches (in which all devices operate together) are known as valves. It can be difficult to operate valves so that they properly share voltage and current between individual devices during static and dynamic conditions. Not sharing voltage/current properly can damage devices subjected to excessive voltage or current [135] and cause converter failure.

2. To keep converter losses small, the switching frequency must be kept low. A single leg of a two-level converter generates one of two voltages at all times and therefore switching at low frequency causes the converter to generate square-wave phase voltages as shown in Figure 4.3. A square-wave voltage is high in harmonic content and will exhibit notable distorted current flow in a power network. This converter can of course be switched at a higher frequency using PWM and this will reduce the harmonic content of its phase voltages, but the losses of the converter will rise due to the higher switching frequency [141].

3. If a single valve fails in this converter topology then it will no longer function. Therefore, in order to provide redundancy in any application using such a converter, (such as a FACTS compensator) an identical two-level converter is needed. The extra converter can then be switched in-circuit during a failure and the old converter switched out. The need for a second fully-rated converter to provide redundancy for the failure of a single valve is expensive in terms of both cost and space.

In recent times the *multi-level converter* has drawn tremendous interest in the power industry to overcome some of these problems, particularly in high-power, medium low voltage applications [142]. Multi-level converters consists of an array of power switching devices and capacitors; they can synthesise output voltages with stepped waveforms. Commutation of the switches permits the addition and subtraction of the voltages on the different capacitors. The main motivation for multi-level topologies is:

- an increase in power rating;
- a reduction in voltage stress on individual power switching devices; and
- the generation of high quality output voltages.

As the number of output voltage levels increase, the harmonic content of the output voltage waveform decreases significantly [143]. The same can be achieved with 2-L converters using very high switching frequencies at the cost of increased switching losses. However, it is hard to find high switching frequency devices at higher ratings

Technological evolution will likely enable multi-level converters to be used for any power range in time. If voltage source inverters (VSI) could utilise ideal switches (able to commute infinite currents at infinite voltages and infinite frequencies), they would generate almost perfect waveforms. The level of power that can be managed by a VSI can be considerably raised by using converters with multi-level structures, where the various levels

correspond to the different dc sources available to the system. In addition, if a multi-level converter is suitably controlled, often it can meet the most rigorous requirements for fast dynamic responses [144].

4.3 Assessment of multi-level converter topologies

The term, multi-level, was first introduced in [145]. The basic concept behind a multi-level design is to use multiple semiconductor switches to switch between multiple voltage levels, thereby providing a stepped output voltage from the converter, depicted in Figure 4.4. The so-called "multi-level" approach utilises at least three levels.

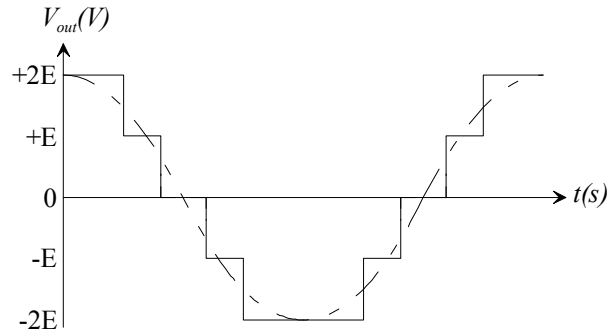


Figure 4.4: Example Multi-level Converter Waveform.

Three multi-level converter designs are discussed in this chapter. They are:

1. Neutral point clamped NPC (diode-clamped) [146],
2. Flying Capacitor FC (capacitor-clamped) [147, 148] and
3. Cascaded-cell [149, 150]

Other multi-level converter designs [151, 152] can be viewed as adaptations or combinations of the three basic converter designs presented. The three designs share two major characteristics:

1. The rating of all types of multi-level converter is increased by adding extra pairs of voltage levels to the converter. Each pair of levels requires the addition of four switches per phase. The switches are always controlled in complimentary pairs. Problems associated with static and dynamic I/V sharing on the valves are therefore avoided.

2. As the rating of a multi-level converter increases so too does the number of possible output voltage levels. Careful choice of the correct output levels will minimize harmonic content in the generated voltage waveform (see section 4.3.3). This is done without increasing the converter switching frequency.

The converters also have their own unique characteristics, bringing advantages and disadvantages. These unique characteristics are discussed in coming subsections.

Only single-phase implementations are discussed in detail in this chapter. However, where necessary, mention is made of three-phase operation.

4.3.1 Neutral-point clamped (diode-clamp) multi-level converter

In the early 1980s, a new converter topology was proposed by Nabae [146]: the diode-clamped multi-level converter. It employs clamped diodes and cascaded capacitors to produce ac phase voltage waveforms with multiple levels. It is often as known as a neutral-point clamped (NPC) converter because its mid-voltage level was defined as the neutral point. This converter can be configured as a three-, four-, or five-level topology, but only the three-level (3-L) NPC converter has found significant application in medium voltage drives [153–155]. The published work on NPC multi-level converters has mostly concentrated on 3-L NPC converters, although four [156] and five level [157] NPC converters have been investigated.

It should be noted that the initial multi-level converter topologies proposed by authors were, however, not practical, since high voltage blocking devices were required. The first practical structure was introduced in [146] and the application of the NPC converter and its extension to multi-level converter was found in [158]. Since all semiconductors are operated at a commutation voltage of half the dc-link voltage for 3-L topology hence offered a simple solution to extend voltage and power ranges of existing 2L-VSI technologies, which were severely limited by the blocking voltages of power semiconductors with both turn-on and turn-off capabilities. Hence, the converter was of particular interest for MV applications.

A three-level diode-clamp multi-level converter and its associated output waveform is shown in Figure 4.5.

A. Topology Description

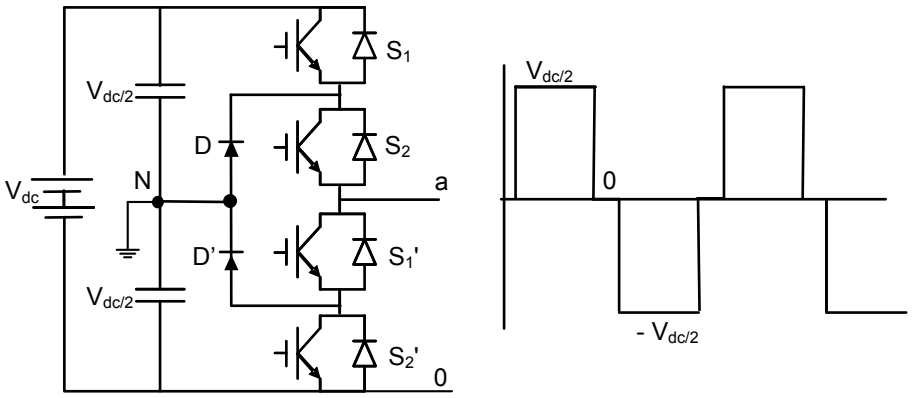


Figure 4.5: Three-level diode-clamp multi-level converter with output waveform.

The 3-L NPC converter shown in Figure 4.5 consists of a series chain of charged capacitors where each capacitor holds a voltage $V_{dc}/2$. Connections are made between the capacitors so that different voltage levels are tapped from the chain. These points are connected to the converter output by an arrangement of semiconductor switches and diodes. In the Figure 4.5 circuit, the dc-bus voltage is separate into three levels by two series-connected dc sources, The central point 'N' can be defined as the neutral point. It should be noticed that the output voltage has three states: $V_{dc}/2$, 0, and $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S_1' and S_2' need to be turned on; and for the 0 level, S_2 and S_1' need to be turned on.

The attributes that makes this circuit different to a standard 2-level inverter is the inclusion of clamping diodes D and D'. This adds the additional switching level (the neutral point) and means that each switch only needs to block 1/2 the level of dc-bus voltage.

Over the last decade plus, many extensions of the Figure 4.5 structure have been proposed in order to increase the number of levels [159], and take even more advantage of the potential benefits of NPC converters. Benefits that include, their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, with reduced voltage stress on the devices. Figure 4.6 shows one phase of a five-level NPC converter and its corresponding output voltage. The IGBT gate drive circuits of the converter topologies is an important part of the circuit design. This is achieved by means of coupling transformers (electrical isolation), optocoupler, or fiber optic cables. The general considerations that influence the design of drive circuit is given in [160].

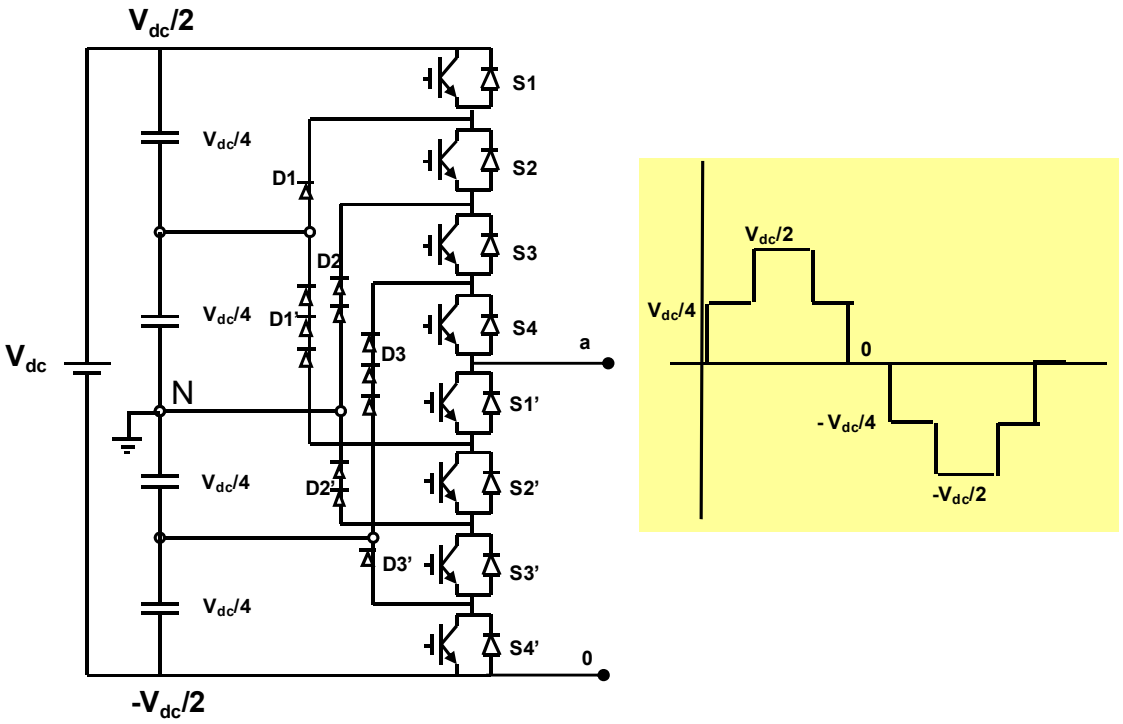


Figure 4.6: Five-level diode clamp multi-level converter with output waveform with respect to its neutral point.

With increased numbers of levels, the structure becomes more difficult to implement with greater complexity in the clamping diode network. For converters with over three levels, the diodes may need to be in a series string to achieve the required voltage rating [143], although this is often drawn as such in this circuit diagrams. Figure 4.6 further highlights the need for these diodes valves (please also refer Table 4.2). Another important factor that hampers practical application is the voltage imbalances in the different dc sources (the capacitors) when transferring power from the DC side to the AC side of the converter. As such, this topology is seldom extended beyond five levels.

In the Figure 4.6 five-level diode-clamped converter, the dc bus consists of four dc voltage sources. For dc-bus voltage V_{dc}, the voltage across each dc source is $V_{dc}/4$, and each device voltage stress will be limited to $V_{dc}/4$ across the clamping diodes. To show how the staircase voltage is formed, the neutral point N is treated as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across points 'a' and 'N'. Table 4.1 shows ways of outputting the levels for a five-level diode-clamped converter.

Table 4.1: Switch states for five-level NPC converter and output levels

Output Voltage V_{ao}	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_{dc}/2$	on	on	on	on	off	off	off	off
$V_{dc}/4$	off	on	on	on	on	off	off	off
0	off	off	on	on	on	on	off	off
$-V_{dc}/4$	off	off	off	on	on	on	on	off
$-V_{dc}/2$	off	off	off	off	on	on	on	on

B. Features

The NPC converter faces problems that cause design complexity, such as unequal duty-cycles between switches which means different switches require different current ratings. It can be seen for example from Table 4.1 that switch S_1, conducts only during $V_{ao} = V_{dc}/2$, while switch S_3, conducts over the entire cycle except $V_{ao} = 0$. This can further lead to capacitor voltages becoming imbalanced [161]. On the other hand, if the inverter design is to use the average duty for all devices, the outer switches may be oversized, and the inner switches may be undersized. If the design is to suit the worst case, then there will be $(m-1) \times (m-2)/2$ devices oversized.

Because every active switching device is expected to block a voltage level of $V_{dc}/(m-1)$, the clamping diodes need to have different voltage ratings for reverse voltage blocking. Supposing that each blocking diode voltage rating is similar to the active device voltage rating, the number of diodes required for each phase will be $(m-1) \times (m-2)$. This number express a quadratic rise in 'm' number of levels. When 'm' is reasonably high, the number of diodes required will make the system impractical to implement. The rating of the NPC increases as more levels (and more switches) are added. Unfortunately, for each additional pair of voltage levels, the number of clamp diodes required rises in a square-law fashion. When the number of converter levels becomes large, the number of components required becomes impractical high, or the physical layout of the clamp diodes becomes complex and costly. Converter reliability also reduces.

Table 4.2: NPC Converter component count

Number of Levels	**Number of Capacitors**	**Number of Blocking Diodes**	**Number of Switches**
3	2	2	4
5	4	12	8
7	6	20	12
9	8	56	16
m	$m-1$	m^2-3m+2	$2(m-1)$

Another limitation of the NPC converter is that in the case of a single switch failure, the whole converter becomes non-operational. To ensure continuous operation, a backup NPC converter with a power rating equal to that of the main converter is required.

Despite these difficulties, the diode clamped converter, particularly in its three level form, has received much attention and use. As a three level converter, it is relatively simple, and can remove the need for a transformer where one would otherwise exist. However, it has considerable disadvantages, particularly when extended beyond the simple three level topology. These issues, in practice, limit the diode-clamped topology to a maximum of five levels. They are, in summary:

- While the transformer can be excluded, extra components (diodes) are needed to maintain the load current. There is a steep increase in the number of extra components required as the number of levels increase.
- These extra components do not necessarily provide equal voltage sharing across switches.
- Outer switches receive a lower average load than others, and switch utilisation is unequal. This variation is particularly noticeable with higher numbers of levels.
- The power flows to and from the different capacitors are not balanced in a capacitor string, so further controls are utilised to balance the capacitor voltages.

4.3.2 Flying capacitor multi-level converter

In recent times, another multi-level topology was proposed by Meynard and Foch which was given the name flying capacitor (FC) converter [162,163]. This was because its design consists of independent capacitors clamping the device voltage to one capacitor voltage level.

In a standard 2-L voltage source converter, each phase leg is made up of a switch pair in parallel with a bus capacitor (generally common to all phase legs). These switch pairs are gated in a complimentary fashion. In this way, the phase leg output is at all times connected to either the positive or negative node of the bus capacitor. In a flying capacitor converter, this switch pair - capacitor "cell" is isolated, and inserted within a similar cell. Therefore the term *imbricated* cells converter can also be used [164]. This inner pair of switches and their related capacitor now "flies" to a new voltage reference as the outer pair of devices switch to a new configuration. The combination of conducting switches and capacitors ensures that the voltage across any blocking switch is always well

defined.

A. Topology Description

The circuit in Figure 4.7(a) illustrates the fundamental building blocks of a single-phase full-bridge flying-capacitor converter and provides a three-level output across a and N, i.e., $V_{dc}/2$, 0, or $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S_1' and S_2' need to be turned on; and for the 0 level either pair (S_1, S_1') or (S_2, S_2') need to be turned on. Clamping capacitor C_1 is charged when S_1 and S_1' are turned on, and discharged when S_2 and S_2' are turned on, if current is positive otherwise is vice versa.

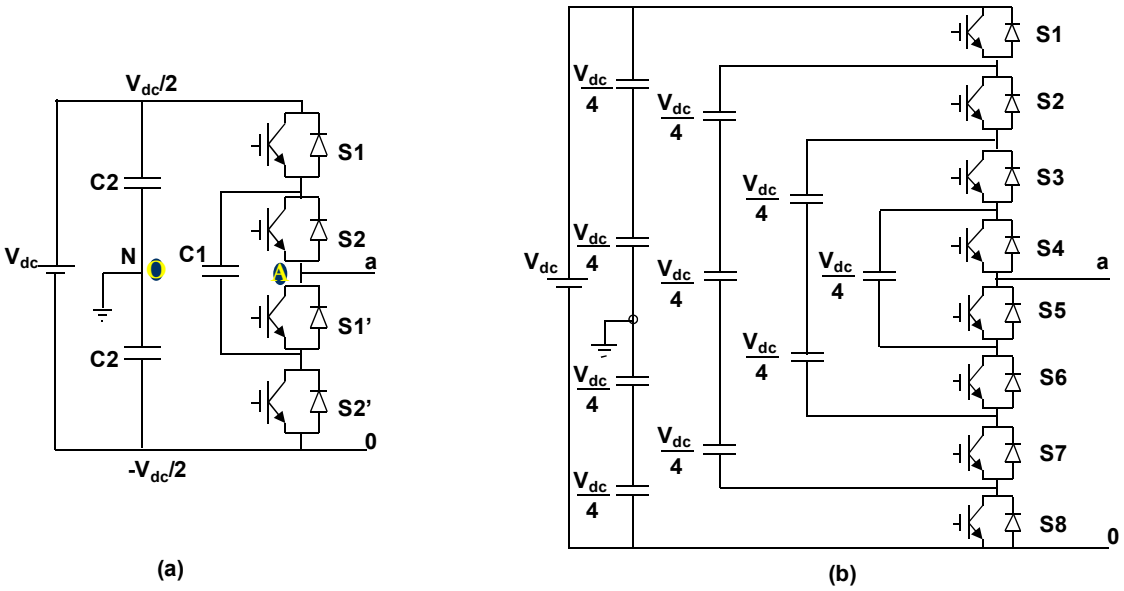


Figure 4.7: Flying Capacitor (FC) multi-level converter (a) Three-Level (b) Five-Level.

This design consists of a repeating unit of capacitor(s) and two switches as seen from the Figure 4.7(a) and (b). The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Figure 4.7(b) as the example, the voltage of the five-level phase-leg 'a' output with respect to the neutral point N, can be synthesised by the switch combinations illustrated in Table 4.3. A multi-level waveform is obtained by switching the FC converter units into circuit in either a positive or negative side.

Table 4.3: Switching states of five-level Flying Capacitor multi-level converter.

Switch states				Voltage level
S_1	S_2	S_3	S_4	$V_{dc}/2$
S_1	S_2	S_3	S_5	$V_{dc}/4$
S_2	S_3	S_4	S_8	
S_1	S_3	S_4	S_7	
S_1	S_2	S_4	S_6	
S_1	S_2	S_5	S_6	0
S_3	S_4	S_7	S_8	
S_1	S_3	S_5	S_7	
S_1	S_4	S_6	S_7	
S_2	S_4	S_6	S_8	
S_2	S_3	S_5	S_8	
S_1	S_5	S_6	S_7	$-V_{dc}/4$
S_4	S_6	S_7	S_8	
S_3	S_5	S_7	S_8	
S_2	S_5	S_6	S_8	
S_5	S_6	S_7	S_8	$-V_{dc}/2$

B. Features

Besides the difficulty of balancing voltage, the major problem in this converter is the requirement for a large number of storage capacitors – many more than other topologies. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level converter will require a total of $(m-1) \times (m-2)/2$ auxiliary capacitors per phase leg in addition to $(m-1)$ main dc bus capacitors. With the assumption that all capacitors have the same voltage rating regardless of dc-link voltage, an m-level diode-clamp inverter only requires $(m-1)$ capacitors. In order to balance the capacitor charge and discharge, one might utilise two or more switch combinations for middle voltage levels (i.e., $3V_{dc}/4$, $V_{dc}/2$, and $V_{dc}/4$) in one or several fundamental cycles. Thus, by proper selection of switch combinations. the flying-capacitor multi-level converter may be used in real power conversions. However in doing this, the selection of a switch combination becomes very complicated, and the switching frequency needs to be higher than the fundamental frequency (which means higher switching losses).

By proper selection of capacitor combinations, it is possible to balance the capacitor

charge [143, 165]. Similar to diode clamping, this requires a large number of bulk capacitors to clamp the voltage. The FC converter has a square law increase in capacitor count as the number of levels rise, as shown in Table 4.4, which makes packaging more difficult and expensive. If a switch fails in the FC converter, the converter will not remain fully operational, hence an extra fully-rated FC converter is required to provide redundancy in the system.

Table 4.4: Flying Capacitor Converter component count

Number of Levels	Number of Capacitors	Number of Blocking Diodes	Number of Switches
3	3	not required	4
5	10	not required	8
7	21	not required	12
9	36	not required	16
m	$1/2(m^2 - m)$	not required	$2(m - 1)$

4.3.3 Cascaded multi-level converter

A modular converter structure comprising cascaded-cells with separate dc sources first appeared in 1988 [166]. This converter type matured during the 1990s and gained more attention after 1997 [144, 167–169]. This converter avoids the need for clamping diodes or voltage balancing capacitors as in previously described multi-level converters. This has made it simple and easy to implement and a research focus for several years [170]. The stacked cell arrangement of this converter seems to be an obvious choice for achieving high voltage ratings. However, this converter topology did not become practical until a reliable realization could be attained by controlling the overall converter arrangement in a multi-level fashion. A five-level converter based on two single-phase bridges (or cells) was used to implement a power converter for applications in plasma control in the early 1990's [171]. A generalized version of this design, which increases the number of levels by increasing the number of series units, was reported in [150]. This converter requires separate dc sources for real power conversions, and thus applications concentrates on harmonic/reactive compensation (dc capacitors are needed only), especially attractive for STATCOMs [172–174].

A description of the cascaded multi-level converter and its features follows. This chapter concludes by comparing this converter with other topologies, and presents the argument that it is superior for use in FACTS applications.

A. Topology Description

Working of an H-bridge cell

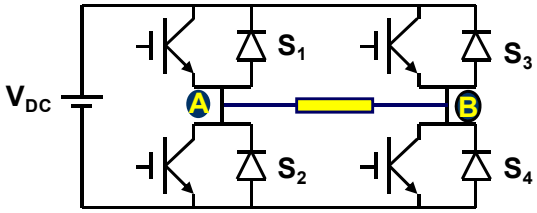


Figure 4.8: H-bridge module.

Figure 4.8 shows one H-bridge cell of a multi-level converter. The cell consists of four power switches which can be IGBT (as depicted), GTO or other power devices, and a DC source and 4 diodes anti-parallel with the switches. This arrangement is well known for use as a 4 quadrant DC motor drive.

The output voltage of H-bridge cell can be presented as:

$$V_{out} = (S_1 - S_3).V_{dc} \tag{4.1}$$

$$S_1 = \begin{cases} 1 & when\ S_1\ on \\ 0 & when\ S_1\ off \end{cases}$$

or

$$S_F = S_1 - S_3 = \begin{cases} +1 \\ 0 \\ -1 \end{cases}$$

$$V_{out} = S_F.V_{dc} \tag{4.2}$$

Where S_F is known as the switching function of the H-bridge.

The switching states for the four power devices have the constraints: $S1 = \overline{S2}$ and $S3 = \overline{S4}$ to prevent the formation of a short circuit. The output voltage of this cell can be $+V_{dc}$, $-V_{dc}$ or 0. This is made possible by connecting the dc sources sequentially to the ac side via the four semiconductor devices. Two options for generating a $0V$ output exist. When the two output terminals are both connected to either the positive or to negative dc-link, the output voltage is equal to $0V$. The H-bridge is in freewheeling state and freewheeling current (assuming reactive load) will pass through one inverse diode instead of the other switch.

A cascaded converter is formed by connecting more than one single-phase H-bridge cell

in series as shown in Figure 4.9a. Each cell generates a square wave voltage waveform with different duty cycles, which together form the output voltage waveform as shown.

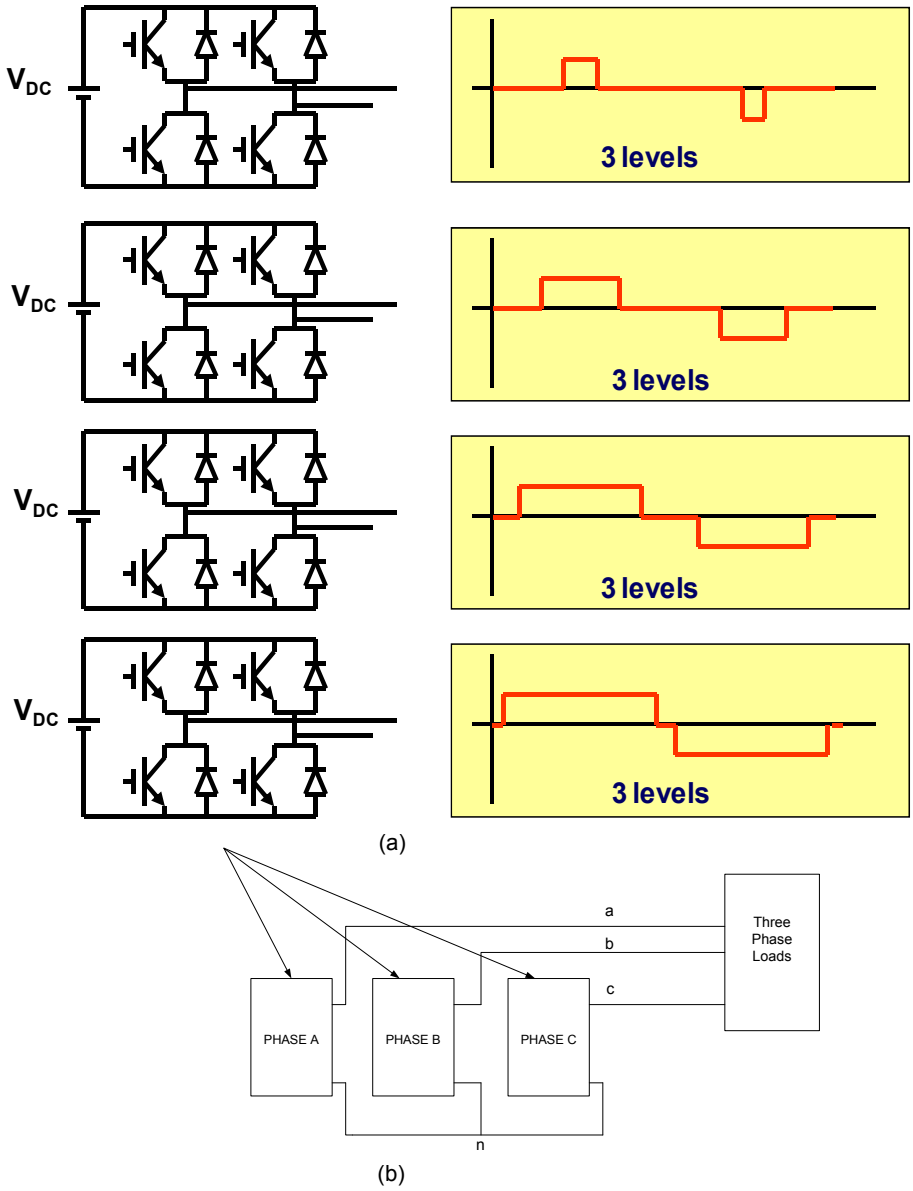


Figure 4.9: Connecting 3 single-phase cascaded converters to form a three-phase cascaded converter.

Figure 4.9 shows a block diagram of a single phase-leg of a cascade H-bridge inverter that uses an equal-rated voltage pattern of cell voltages switching at the fundamental frequency. In this way it is possible to make three phase cascaded converters from three single phase cascaded converters connected to a three phase load without the need for a transformer. Each cell includes a single-phase three-level H-bridge inverter, a capacitive

dc-link (also includes a rectifier, and an independent or isolated voltage source provided by transformer secondaries or batteries). A three-phase configuration can be obtained by connecting three of these converters in wye or delta (Figure 4.9b).

The phase output voltage is synthesised by the sum of four cell's outputs, i.e., $v_{an} = v_1 + v_2 + v_3 + v_4$. This is the traditional type of cascaded converter and the output voltage has $2N + 1$ levels, where N is the number of cells connected. Figure 4.10 also depicts a converter with four equal-sized cascade cells which can synthesize an output waveform from $+4V_{dc}$, via 0 to $-4V_{dc}$ in 9 levels. Any number of levels can be achieved by connecting an appropriate number of cells in series.

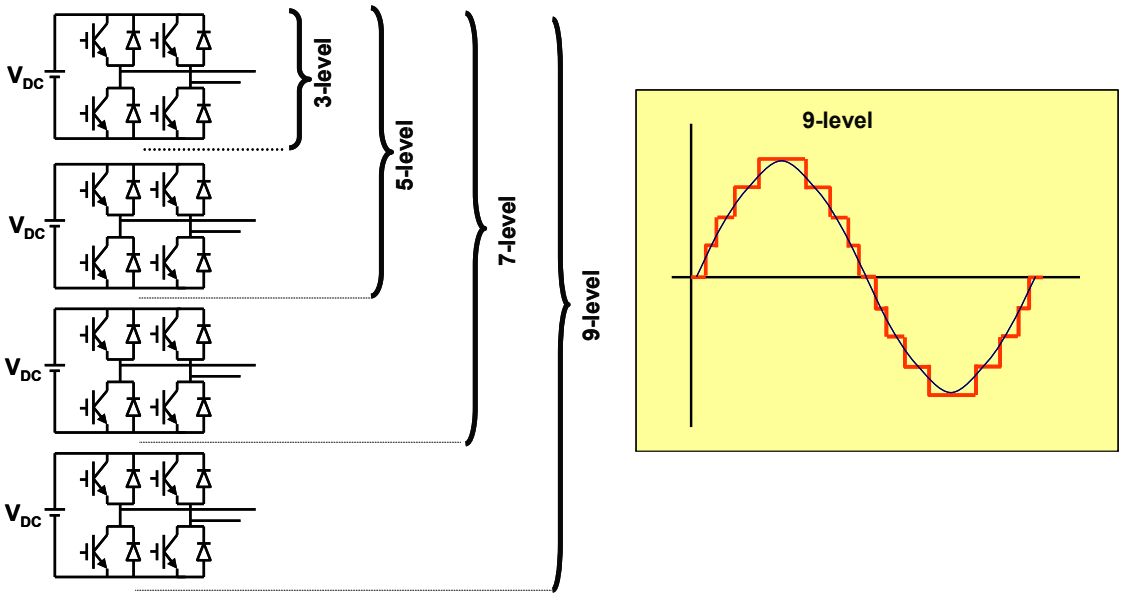


Figure 4.10: Identical H-bridge cells summing the output waveform to achieve 9-levels.

B. Features

The cascaded converter has no overall dc connection and each dc source must be separated from others as seen from Figures 4.9 and 4.10. In this situation, two cascaded-converters cannot be easily connected in a back-to-back fashion and if an attempt is made the electrical isolation between cells is broken and short-circuits occur. This immediately excludes use in certain FACTS designs, such as the UPFC compensator, which is a formation of two back-to-back converters operated via a common dc-link [41]. Cascaded-converters however can be connected back-to-back via an isolating transformer [175, 176], but this requires additional auxiliary converters which produce AC voltages for transformer coupling. This significantly adds to the cost and complexity of the converter. Despite

earlier invention of cascaded type converter, it demonstrated no distinctive practical use because of the real power requirement for individual cells in the chain. However, on re-examination this topology is being considered for applications, such as active power filtering and VAR compensation/STATCOM. Today, this converter topology is successfully implemented up to a range of 31MVA due to its series expansion capability [177]. In this application only a floating DC bus capacitor is required on each floating dc bus.

Other sources of power which could easily be made modular and floating are batteries for battery energy storage systems (BESS) [178], or alternative energy sources such as solar panels. For real power conversions (ac to dc and dc to ac), the cascaded-converter needs separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic [179], and biomass, etc. This topology was patented by Robicon Group in 1996 [180] and is one of the company's standard drive products.

It is of course possible to power the isolated bridges from multiple isolated transformer secondaries, each with their own rectifier [180] but with its customary disadvantages of extra circuitry . However, this multi-level converter structure has some very significant advantages if used as a VAR source/sink. Its advantages are:

- It has perhaps the simplest architecture and the lowest component count. No transformer is needed, so capital costs are low.
- Again, the converter is very modular and easy to understand. This applies not only to its structure, but also to its control.
- Should a module fail (or be removed), it must fail short circuit, or be bypassed. The converter can continue to operate unlike NPC or FC converter, at full current capacity, but at reduced voltage rating. This will in practice mean that if fault tolerance is required, the converter will need a more conservative voltage rating – though a potential cost penalty.

and the limitation:

- Needs separate dc sources for individual cells, and thus its applications are somewhat limited and concentrate on harmonic/reactive power compensation *i.e.*, STATCOM applications. Its use for real power conversion is somewhat limited, if structure is to be kept simple.

Table 4.5: Cascaded Converter component count

Number of Levels	Number of Capacitors	Number of Blocking Diodes	Number of Switches
3	1	4	4
5	2	8	8
7	3	12	12
9	4	16	16
m	$1/2(m-1)$	$2(m-1)$	$2(m-1)$

4.3.4 Asymmetrical cascaded converters

In the description of the previous section, the input dc voltages of the cascaded converter cells were equal to each other. This converter design is called the *equal rated* topology. However, it is possible to have a converter with different voltage levels on different cells [181, 182]. In this case the circuit can be called an asymmetric cascaded multi-level converter. It should be pointed out that cascaded multi-level converters [180] have been proposed with different scales of input dc voltages to achieve the maximum number of output levels from the configured H-bridge cells in a converter topology (refer Figure 4.11). This section will explain the construction and features of the hybrid type of cascaded converters so that a conclusion can be achieved on the best type of cascaded converters to be implemented in distribution networks.

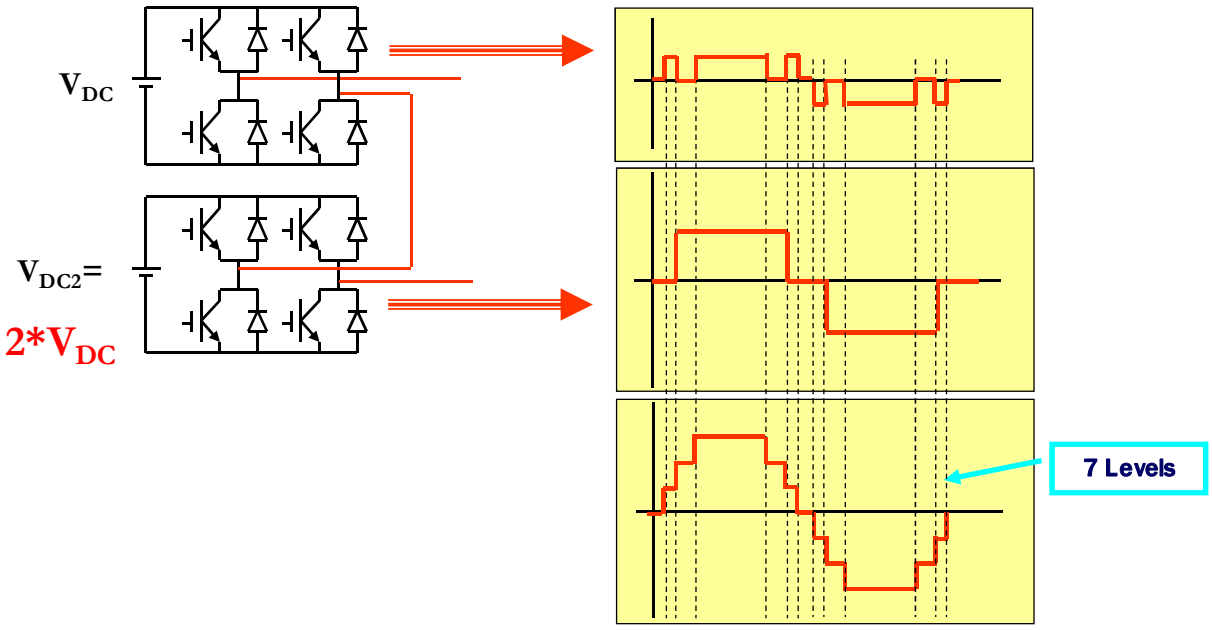


Figure 4.11: Asymmetric cascaded converter to form a 7 levels output waveform.

4.3.5 Hybrid and Quasilinear type cascaded converters

Figure 4.12(a) shows a block diagram of a single-phase leg for the hybrid H-bridge multi-level cascaded converter proposed in [152, 181]. This is known as a hybrid cascaded converter. For N number of H-bridge cells in the chain, the associated number of level is equal to $2^{N+1}-1$ levels, where N is total number of cells. For example, if three H-bridge cells with input dc voltages of the order of $1V_{DC}$, $2V_{DC}$, $4V_{DC}$ are connected then the output waveform would be 15 levels: $\pm 7V_{DC}$, $\pm 6V_{DC}$, $\pm 5V_{DC}$, $\pm 4V_{DC}$, $\pm 3V_{DC}$, $\pm 2V_{DC}$, $\pm 1V_{DC}$, and 0. In this type of topology the higher dc link cell has lesser number of commutations.

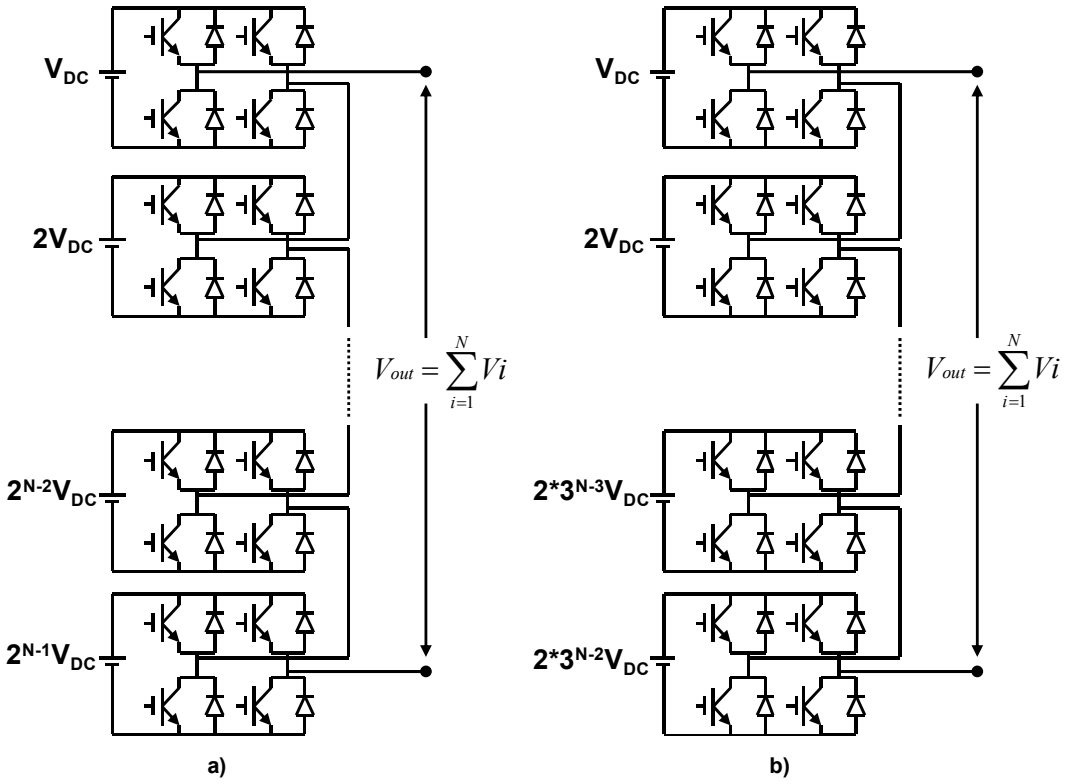


Figure 4.12: Asymmetric cascaded converters a) hybrid b) Quasilinear.

Figure 4.12(b) shows the so called quasilinear cascaded converter, originally introduced in [183]. The number of output waveform levels equals $(2 \times 3^{N-1}) + 1$. The input dc voltage relationship between the H-bridge cells is of the order of $1V_{DC}$, $2V_{DC}$, $6V_{DC}$. So for instance, the three cells in the chain will produce 19 levels in the output waveform: $\pm 9V_{DC}$, $\pm 8V_{DC}$, $\pm 7V_{DC}$, $\pm 6V_{DC}$, $\pm 5V_{DC}$, $\pm 4V_{DC}$, $\pm 3V_{DC}$, $\pm 2V_{DC}$, $\pm 1V_{DC}$, and 0.

It can be observed that for the same number of cells, quasilinear cascaded converter has

a considerably higher number of levels than hybrid topology.

4.3.6 Ternary-sequence cascaded converter

A new family of multi-level converters emerged as a solution for working with higher voltage levels [184]. Figure 4.13 shows this recently proposed converter, which is known as the *ternary-sequence* converter in this thesis, and consist of H-bridge cells connected in series as in section 4.3.3 but with the pattern of cell voltages of $1V_{dc}$, $3V_{dc}$, $9V_{dc}$,...., $3^{N-1}V_{dc}$. With this arrangement, the number of levels of the output waveform is 3^N. As illustrated in Figure 4.13, if four cells having relative values of *1*, *3*, *9*, and *27* are used, *81* levels can be achieved, *i.e.*, from $+40V_{dc}$, via *0* to $-40V_{dc}$ in steps of V_{dc}. The basic topology of this converter is shown in Table 4.6. This Table shows the input voltages and the switching frequency calculated for a 4-cell converter leg. The maximum output voltage of the highest cell is chosen as the base value for Table 4.6. The total voltage

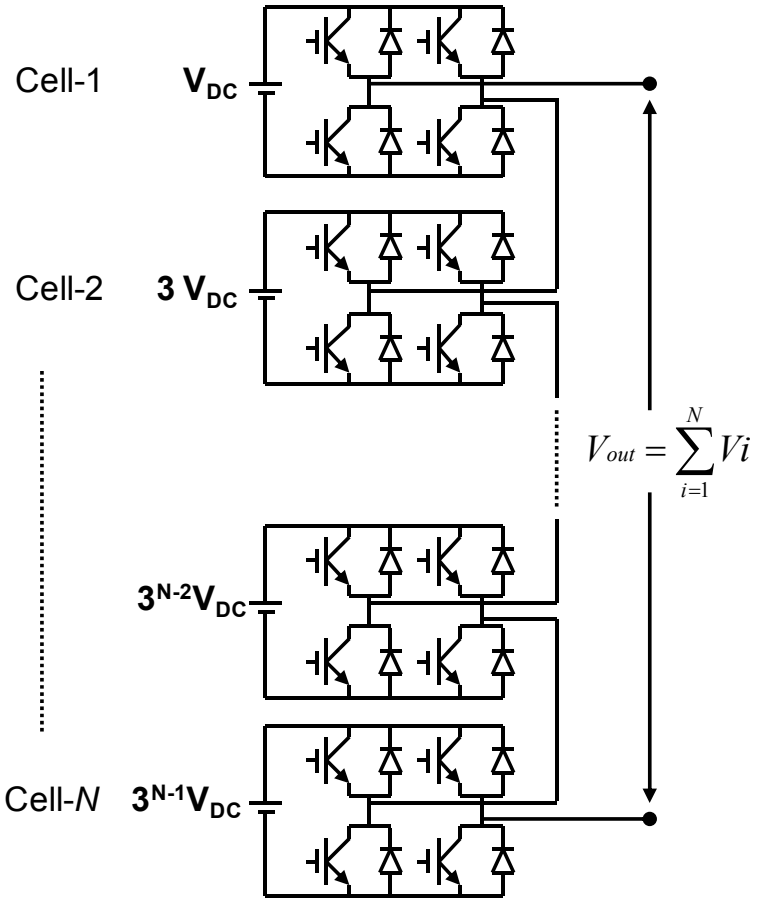


Figure 4.13: Ternary-sequence cascaded multi-level converter.

achieved from this topology is $(3^N - 1)/2] \times V_{dc}$ at a fundamental frequency f_o. This topology provides the maximum number of levels for the minimum number of H-bridges in any cascaded cell arrangement. Therefore this arrangement is highly suited for use in MV level distribution systems.

Table 4.6: Ternary-sequence cascaded multi-level topology

Cell	**Input voltage (p.u)** $1/3^N$	**Switching frequency (Hz)** $(2 \times 3^N - 1)f_o$
Cell I	1/27	$53f_o$
Cell II	1/9	$17f_o$
Cell III	1/3	$5f_o$
Cell IV	1.0	f_o

4.3.7 Review of the cascaded multi-level converters

Figure 4.14 and Table 4.7 show the comparison of the scaling of output voltage and number of levels of various types of cascaded arrangements of multi-level converters for N cells. It can be noted that in the ternary-sequence topology, the level number increases significantly compared to the others. This topology has the greatest number of levels for a given number of H-bridge cells at the expense of higher DC input voltages to its individual cells in the chain which results in the increased rating of the semiconductor device.

From the Table 4.7, it can be deduced that the *equal-rated* type offers modularity and simplicity because all cells are identical. On the other hand *ternary-sequence* gives a remarkable number of levels in the output waveform compared to any other style of cascaded converter for a given number of cells. We will compare these two attractive structures of cascaded converter on the basis of power losses in the next Chapter. The graph of Figure 4.14 shows the trend of the number of output levels achieved with H-bridge cells for various cascaded type converters.

Table 4.7: Assessment of cascaded converters

Cascaded Converter	**Input cell voltage**	**Max. Output Voltage**	**Output Levels**
Equal-rated	V_{DC}	$N \times V_{DC}$	$2 \times N + 1$
Hybrid	$(2^{N-1}) \times V_{DC}$	$(2^N - 1) \times V_{DC}$	$2^{N+1} - 1$
Quasilinear	$(2 \times 3^{N-2}) \times V_{DC}$	$(3^N - 1) \times V_{DC}$	$(2 \times 3^{N-1}) + 1$
Ternary-sequence	$3^{N-1} \times V_{DC}$	$(3^N - 1)/2 \times V_{DC}$	3^N

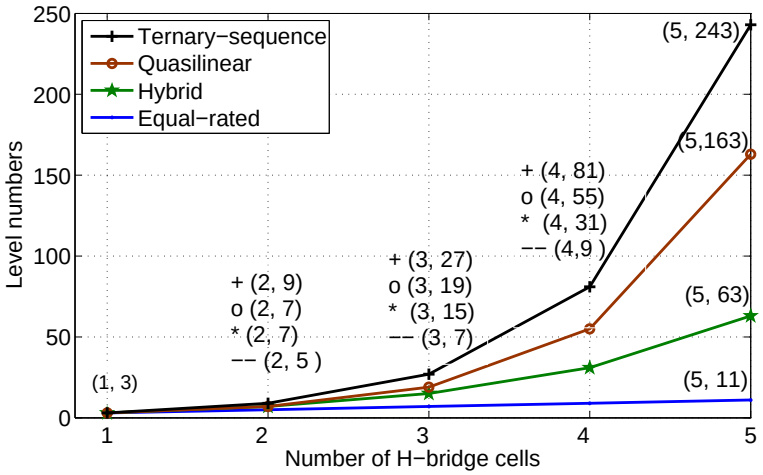


Figure 4.14: Comparison results of various cascaded multi-level converters.

4.4 Comparison of the multi-level converter topologies

The different topologies presented as multi-level converters in this chapter show a number of characteristics in common, giving them some clear advantages over two-level converters, such as:

- reduction in the commutation frequency applied to the power components;
- reduction in the voltages applied to the main power switches, enabling operation at higher load voltages;
- way forward for the future power compensators.

The main disadvantage associated with the multi-level configurations is their circuit complexity, requiring a high number of power switches that must be commutated in a precisely determined sequence by a dedicated (and complex) modulator circuit; they also require a great number of auxiliary dc levels, provided either by independent supplies or, more commonly, by cumbersome array of capacitive voltage dividers. In this case, ensuring that the dc voltages are kept in equilibrium is another factor that increases the complexity of the modulator circuit. In the past, these disadvantages were almost overwhelming, due to the cost differences they produced between multi-level and standard configurations. But the continuing development of high power high switch frequency devices such as insulated-gate bipolar transistors (IGBTs) working at 3.3, 4.5, and 6.5 kV, and insulated-gate commutated thyristors (IGCT) working at 4.5 or 6 kV (as discussed in Chapter 2) has improved overall converter performance, renewing the interest in multi-

level topologies, that may be able to compete in the market with the standard two-level pulse width modulation (PWM) converters at lower power ranges.

Cascaded-cell converter is made from a series connection of individual identical cells. Each cell consists of two pairs of complimentary controlled switches and one charged capacitor or a fixed dc source. This topology has better features such as component count. The cells in a cascaded-cell converter are all identical and therefore, this kind of converter is truly modular compared to any other type [143]. As the rating of the converter increases all component counts rises linearly as shown in Table 4.8. In the case of a single switch failure, it is only needed to have one additional cell to guarantee continued operation because only that cell is affected and not the whole converter. For a converter built from N cell modules, the rating of the redundant circuit is $1/N^{th}$ of the rating of the main converter. All the other multi-level converters requires a fully rated additional converter to provide redundancy. Ternary-sequence which is an extension of original cascaded type converter has a potential to compete with standard equal-rated topology (more levels with reduced number of cells, hence cost effective).

The comparison between these two designs (equal-rated and ternary-sequence) on distribution voltages will bring out some interesting evaluation and a choice to use them with optimum number of cells for highest output levels to achieve high quality of power supplied (investigated in the next Chapter).

Table 4.8: Comparison of Multi-level Converter Component Counts

Converter Type	**Number of Levels**	**Number of Capacitors**	**Number of Blocking Diodes**	**Number of Switches Switches**	**Total Component Count**
NPC	m	$m-1$	m^2-3m+2	$2(m-1)$	m^2-1
FC	m	$1/2(m^2-m)$	not required	$2(m-1)$	$1/2\times m^2$ $-3/2\times m-2$
Cascaded-cell	m	$1/2(m-1)$	not required	$2(m-1)$	$5/2\times m^2-5/2$

4.5 Applications of Cascaded Multi-level converters

It is evident that one of the key features of a multi-level converter, in spite of any topological design, is higher power rating than available from a single 2-level converter. A converter need not be limited in size by the prevailing semiconductor technology, since a multi-level converter allows the voltage and/or the current to be shared between a number of switches. This advantage has traditionally justified the extra complexity of multi-level converters only at very high power levels, for large motor drives and utility applications.

However, as the understanding and acceptance of multi-level converters has increased, these converters are being used at all power levels to extend the useful power range of semiconductor switches. For example, using multi-level topologies, IGBTs are challenging traditional GTO converters in motor drives and traction applications and MOSFETs are displacing IGBTs in some larger Switch Mode Power Supplies.

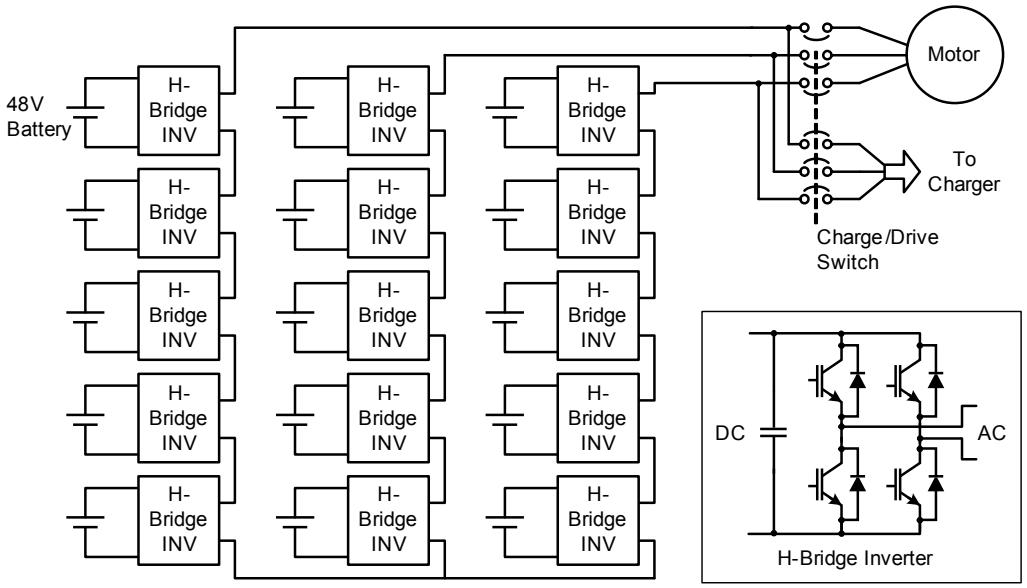


Figure 4.15: Cascade multi-level converter for electric vehicle application [182, 185].

Figure 4.15 [182,185] depicts one application of cascaded type of multi-level converter for electric vehicle application where in the motoring mode, power flows from the batteries through the cascaded converter to the motor. In charging mode, the cascaded converter acts as rectifier, and power flows from the source to the batteries. The cascaded converter can also be used as rectifier to recover kinetic energy of the vehicle if regenerative braking is used. Other useful applications of cascaded converters are reported in [186–188].

4.6 Conclusions

Multi-level converters were introduced almost thirty years ago and within this period they have grown from an attractive concept to a realistic industrial option to tackle power quality and reliability issues under the umbrella of FATCS technologies. Multi-level converters have been utilized for power conversion in medium and high power applications because it is impractical to connect a single power semiconductor switch directly to medium voltage grids (11kV/33kV) because of the limitation in device ratings. This chapter demonstrated the diversity of possible multi-level converter topologies. Each has its own set of advantages and disadvantages and for any one particular application, one topology may be more appropriate than the others.

The linear component count and the modularity of cascaded-cell converters brings significant advantages over both the NPC and FC multi-level converters types. With a balanced voltage stress in devices and utility compatible features, the cascaded design have shed a light in the power electronics arena and are emerging as a new breed of power converters for high-voltage high-power applications. However, it should not be forgotten that lack of a single DC-link in the cascaded topology can be a serious drawback if a UPFC compensator is to be built [161].

The cascaded-cell converter has two attractive structures for achieving multiple voltage levels. First is the traditional topology which applies equal-rated input dc voltages for each cell in the chain. The second is the recently proposed configuration with a ternary relationship for its dc voltage of each cell in the chain. The analysis based on modeling and simulation of these designs will provide a deeper understanding of the cascaded converter's capabilities. The device selection based on efficiency and performance of the converter will create possibilities for their right implementation on distribution systems, which is the aim of the ensuing chapter.

Chapter 5

Technology comparison for cascaded multi-level converters in distribution networks [1]

5.1 Introduction

This chapter compares two structures of cascaded multi-level converter for 11kV and 33kV distribution networks on the basis of power losses in the converters using both NPT and PT IGBT devices. The first structure is the traditional cascaded converter topology which has equal-sized cells in its chain. The other is the chain with a ternary relationship between its dc-link voltages, as presented in the previous chapter. Models with 81 and 27 levels are developed for both kinds of converter following the selection of suitable IGBT device technology. These converters (equal-rated and ternary sequence) are studied with regard to their suitability for use in power distribution networks.

The modeling has two objectives: first, the formation of staircase waveform using chain-cells; second, to facilitate the power loss evaluation of high voltage IGBTs and inverse diodes used in the construction of cascaded multi-level converters. This allows the power losses of the two topologies to be compared. Both types of converter are attractive but an assessment of overall power loss is important in determining the right topology for distribution networks. Further work compares the two converters on the basis of state-of-the-art- HV IGBTs. The IGBT device technologies used to evaluate the cascaded multi-level converters will be subject to change because new devices will appear on the

[1] Two papers were presented at the IET, 3^{rd} International conference PEMD'06 and IEEE, IECON'07 respectively, based on some of the work reported in this Chapter [189, 190]

market. However, the main purpose of this chapter is to evaluate the converter types rather than the specific devices. Various methods of calculating power losses in two level and multi-level inverters have been explored in [44, 141, 191, 192].

5.2 Comparison Approach for Cascaded-cell Converters

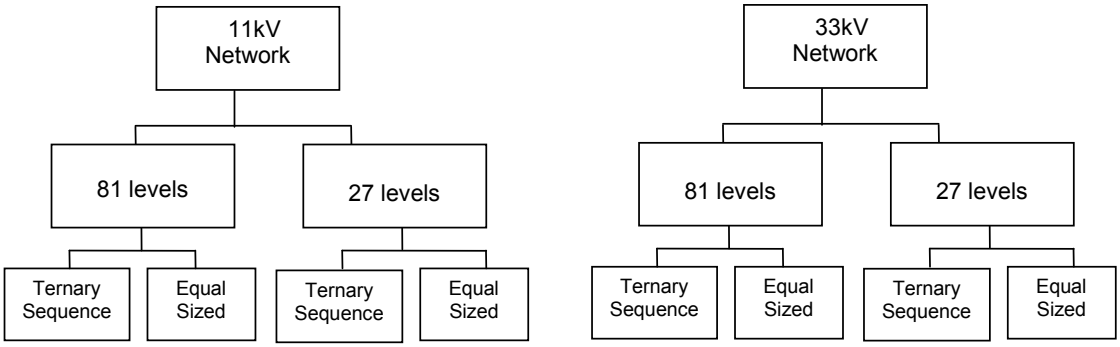


Figure 5.1: Comparison idea for two potential cascaded converters.

The power losses of each converter type deployed in both 11kV and 33kV distribution networks (a spectrum depicted in Figure 5.1) will be analysed in this chapter. 81 and 27 levels are generated by using 4 and 3 cells for ternary-sequence, whereas 40 and 13 cells respectively are required to produce the same number of levels with an equal-rated converter.

The choice of 81 and 27 levels as a comparison is practical because the next achievable level after 81 in a ternary-sequence converter is 243, which makes very little improvement to the quality of achieved wave shape. As Figure 5.3 shows, an almost perfect output (close to reference) is already achieved with 81 levels. Therefore, using another cell in the chain switching 3.5 times faster than the fastest cell in a 81-level converter would contribute more in losses than it would in improved output. Further, its counterpart equal-sized converter will require 121 cells in the chain for 243 levels, which will certainly increase its total size and cost in comparison to 40 cells for 81 levels. The next choice below 27 levels is 9 levels in the ternary-sequence topology. The output of a 9 level converter is considerably deteriorated and will require special control techniques to improve the wave shape. Any level between 81 and 27 levels can only be achieved with a equal-sized converter and not with a ternary-sequence converter (as illustrated in previous chapter of Subsection 4.3.6). Therefore, this assessment is set to 81 levels (4 vs. 40 cells) and 27 levels (3 vs. 13 cells). We have investigated sixteen designs of these two

type of cascaded converters and a total number of 320 individual cases to calculate power loss and thus efficiency for various MVA capacities in both 11kV and 33kV systems.

5.3 Modeling of Cascaded-cell Converters

This section examines in detail the operation of two types of cascaded-cell converter mentioned in Subsection 4.3.3. A model was developed in the PLECS/SIMULINK simulator similar to Figure 4.10. It can be modified for any number of cells and for equal-rated or ternary-sequence voltages. The device models of IGBTs and inverse diodes approximate the on state voltage drop by the summation of a slope resistance and a fixed voltage source.

The dc-link voltage of each cell in the chain, the MVA capacity of load, power factor and switching frequency of each converter were rated. For evaluation purposes, the converters are assumed to be operating in steady state at a constant case temperature of 80^{o}C and a maximum junction temperature of 125^{o}C. Although the major application for a multi-level converter is VAR compensation, it can also be used for other applications such as VSC-HVDC. Hence a P.F (power factor) of 0.9 was chosen for the load as a general assumption. For a fixed MVA load, the losses in the converter devices depends mainly on I_{rms}. We can connect a multi-level converter to the network for the sake of analysis, or representatively connect it as a stand-alone load to mimic network characteristics. To avoid complexity of modeling network characteristics, this work used a stand-alone load to derive power losses in the converter.

5.3.1 Modulation Method

In this model, a reference signal of a fundamental sinusoidal waveform is fed into a quantizer function block whose output is then used to find the states (either +1, -1 or 0) of the corresponding cell stored in a look up table. The modulation strategy shown in Figure 5.2 was chosen because of its simplicity for analysing the internal switching pattern of each cell in both cascaded-cell converters.

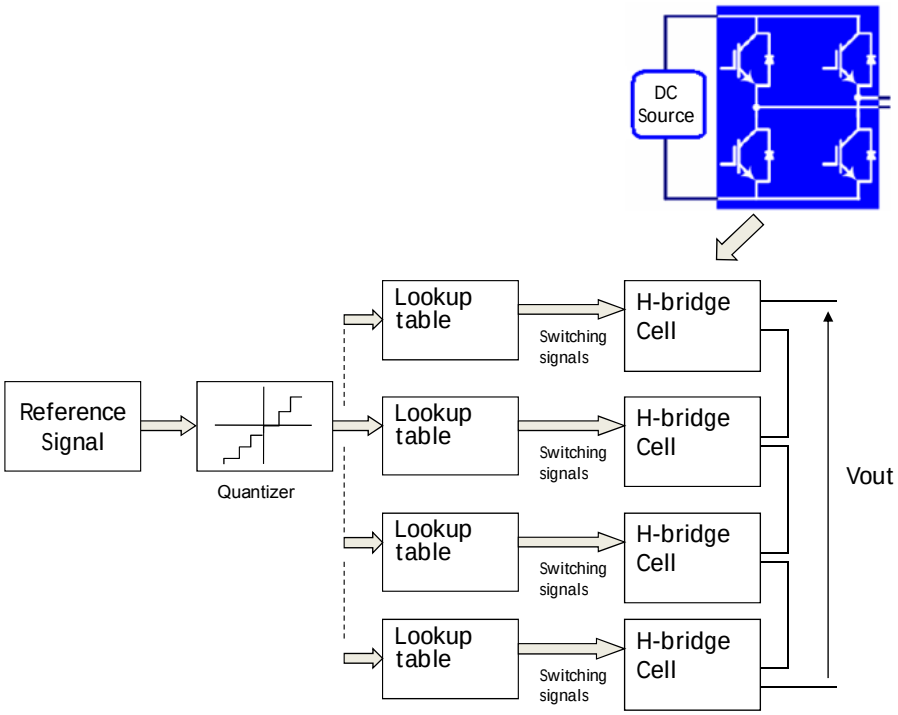


Figure 5.2: Modulation strategy for cascaded multi-level converters.

In a multi-level converter, the output voltage waveform is typically synthesised using the two voltage levels closest to the desired output voltage (reference voltage). This reduces the voltage deviation (error), and hence distortion of the voltage waveform with respect to the reference voltage, thus improving the quality of the voltage waveform (hence currents) without the need for an increase in the switching frequency. In this thesis, the reference voltage is synthesized (or approximated) using only the closest voltage level.

A strategy which utilises approximation is given in [193]. This method behaves like an A/D (Analogue to Digital) converter because it selects the voltage level closest to the reference voltage. This defines a band of half the distance between two consecutive levels, just like an A/D converter discretises an analogue signal into a digital discrete signal. This discretisation process is performed by a quantiser in our model.

The behavior of the quantiser which assumes equally spaced voltage levels, can be described mathematically as:

$$|v_{ref} - v_o| \leq \frac{Vdc}{2}$$

This assumes equally spaced voltage levels.

The PWM is also thought as a way of improving the approximation of the output to the reference voltage, in terms of the A/D conversion this means improving the resolution of the A/D converter. The principal reason for doing so is to be able to vary the output to reduce the harmonics. It goes without saying that the more pulses in the PWM, the higher the switching losses, so gains from the use of PWM have to be sufficient to justify an increase in switching losses.

The main limitation of the kind of modulation technique used in this work is relatively poor tracking of the fundamental voltage waveform. This strategy used here is able to provide only discrete fundamental voltages. However, errors reduces with an increasing number of levels. It can be seen from the simulation results shown in Figure 5.3 that for 81 levels, the output voltage is almost perfect.

5.3.2 4 and 40-cell modeling at 81 levels

The 4-cell configuration shown in Figure 4.13 has the relationship 1,3,9 and 27 V_{dc} - named "ternary–sequence" in this thesis. A look-up table is used to store the switching function for each cell. Cell-I has lowest rating devices but commutates at highest frequency of 2650Hz. The other three cells commutate at 850Hz, 250Hz and 50Hz. Note that the cell with the maximum rating has the fundamental commutation frequency (refer to Table 4.6). In the case of an equal-rated converter, all devices switch at the fundamental frequency.

The output waveform generated by both 4 and 40 cells is 81 levels (for ternary and equal-rated respectively) has identical wave shape as shown in Figure 5.3. This result prompts a question as to which type of cascaded converter (4-cell ternary or 40-cell equal rated) is suitable to implement in distribution networks. The ratings of devices used in equal-rated and ternary-sequence cascaded-cells and their selection criteria will be discussed in Section 5.5. Here, we focus on synthesizing the required multi-level output waveform from the model. Tables listing the converter states of 4 and 40 cell according to each output voltage level in the multi-level system are shown in Appendix A. The only difference in the model for both the cases is that 4 cells will be replaced by 40 cells having a look-up table assigned to each one of them.

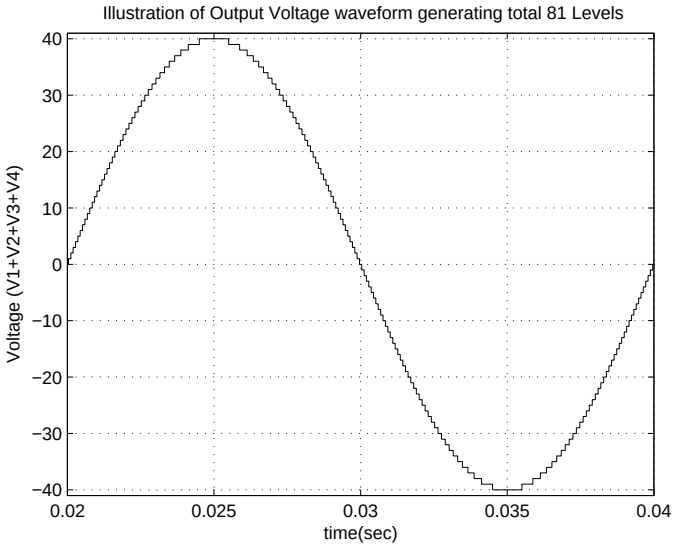


Figure 5.3: 81-level output waveform from cascaded multi-level converter.

5.3.3 Simulation Results

The switching waveforms of the cells in the 81-level ternary sequence converter are shown below:

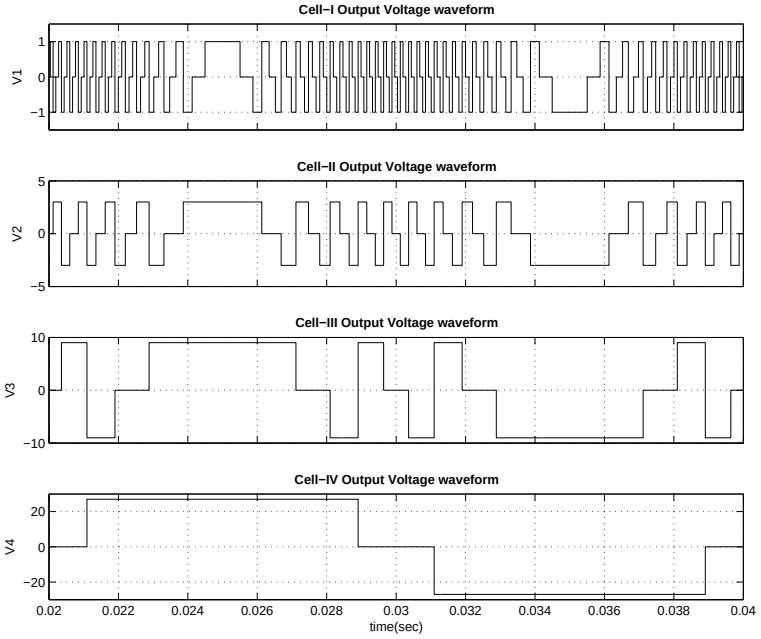


Figure 5.4: Output waveform of 4-cell in ternary-sequence converter.

We can observe from Figure 5.4 that cell-IV is the slowest (fundamental frequency) and cell-I is the fastest (2650Hz) switching device as calculated from Table 4.6 in Subsection 4.3.6. The output voltage of all these cells is added to attain the required 81 level output waveform as shown in Figure 5.3. Note that to avoid the start up transient in the simulation, the interval from 0ms to 20ms is removed.

5.3.4 3 and 13-cell modeling at 27 levels

The modeling and study of these cascaded converters is extended by changing the number of cells in the PLECS/SIMULINK model from 4 to 3 for ternary and 40 to 13 for equal-rated converter. The output voltage waveform attained is 27. The switching states for 3 and 13 cells of the ternary sequence converter are given in Appendix A.

5.3.5 Simulation Results

27 levels are produced successfully from 3 and 13 cells respectively as shown in Figure 5.5. The quality of the output voltage achieved using 3 and 13 cells is of course less in comparison to 4 and 40-cell converters.

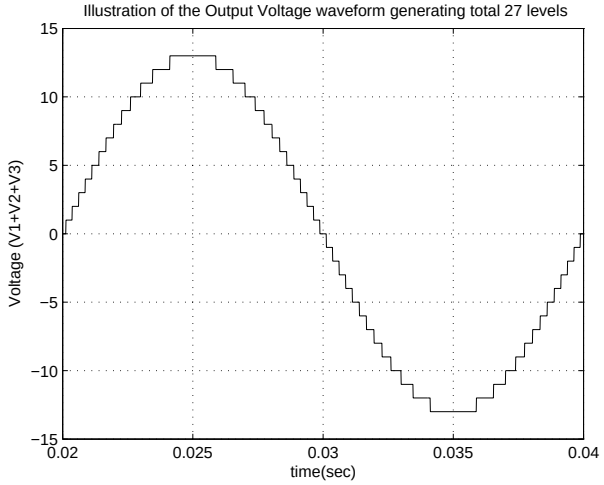


Figure 5.5: 27-level output waveform of cascaded multi-level converters.

In summary, models for 81-level and 27-level cascaded-cell converters of equal-sized and ternary sequence were developed in the PLECS/SIMULINK simulator. The simulation was executed and the desired output voltage waveform was synthesised from the multiple voltage levels with less distortion.

5.4 Semiconductor loss calculation method in cascaded-cell converters

Following the construction of the multileveled converter models, the losses in each type of converter should be calculated. Sources of loss in power semiconductor devices are:

- The loss during forward conduction. It is a function of the forward volt-drop and conduction current: or the square of the conduction current multiplied by the on-state resistance of the device. This is the major source of loss when operating at low frequency.
- The loss associated with the leakage current during the blocking state which is normally negligible.
- The loss occurring in the gate circuit as a result of the energy input from the gate signal. In practice, with pulse firing of thyristors or the high impedance gates of IGBTs, these losses are negligible.

The switching loss, that is, the power dissipated in the device during turn-on and turn-off. It can be significant when switching occurs at high frequency. The average power loss due to switching is given by the sum of the turn-on and turn-off energies multiplied by the frequency of the switching.

The sum of the conduction and switching losses in all devices is therefore a good estimation of the total power loss in a circuit.

5.4.1 Conduction losses

Conduction losses are dependent on the duty ratio of the IGBT and the reverse conducting diode in the converter. The average conduction losses P_{cond} due to the IGBT and inverse diodes in ternary and equal-rated converters can be expressed as [194]:

$$P_{cond} = \frac{1}{T_0}\left[\int_0^T V_f(t)i(t)dt\right] \tag{5.1}$$

Where:

$V_f(t) = v_{on} + Ri(t)$

P_{cond} = power loss due to conduction of a switch

$i(t)$ = switch current
V_f = forward voltage drop of the device
v_{on} = fixed component of forward voltage drop (*knee*) of a device's I-V curve
T_0 = fundamental period
T = conduction time of switch
R = slope resistance of device

The model data for the IGBT and inverse diode modules is based on their respective data-sheet values supplied by the manufacturer(s) [128,130]. The conduction losses depend on the number of devices in the output current path. Two switches are always conducting in each cell in the chain of both types of converter at any time in one fundamental period (refer Subsection 4.3.3-A). The calculation was made for each cell over a period and then losses in all the cells connected in the chain were summed over one fundamental period T_0. An example of the conduction loss calculation and the instant of turn-off is shown in Figure 5.6.

5.4.2 Switching losses

Switching losses can be estimated from the manufacturers graphs of switching energy loss as a function of current. Equation (5.2) is used for the equal-sized converter because the f_{SW} and E_{tot} of all the cells is the same.

$$P_{sw} = 4 * N(E_{tot} * f_{SW}) \tag{5.2}$$

Where:
P_{sw} = Switching power loss of a cell
E_{tot} = Average total energy loss during on and off transition of the switch
f_{sw} = Switching frequency of the cell
N = Number of cells in the chain

The ternary-sequence converter requires individual switching loss calculations for each cell because each cell has a different f_{SW} and E_{tot}. The switching loss at the instant of turn on and turn off of each switch for every cell was calculated during the simulation for a range of MVA capacity multi-level converters. Equation (5.3) is used to estimate the total switch loss of a cell in a ternary-sequence converter, where N_{SW} is the number of switching cycles per fundamental cycle.

$$P_{sw} = \frac{1}{T_o}\left(4.\sum_{k=1}^{N_{SW}} E_{on}(k) + 4.\sum_{j=1}^{N_{SW}} E_{off}(j)\right) \tag{5.3}$$

Where: $N_{SW} = round(f_{sw}/f_o)$ and $T_o = (1/f_o)$

It should be noted that diodes mainly experience turn off losses. With inductive load, the diode is carrying lagging current, which commutates to a transistor being turned on, thus forcing the diode to turn off and take over blocking voltage. The simplest way to determine switching losses is using the graphs of energy loss per switch provided by the manufacturer.

Conduction and switching losses are summed over one fundamental period of the output frequency. All the devices connected in the converters are considered. Diode reverse recovery energy is added to each turn-off energy dissipation per switching pulse. The total loss for IGBT and inverse diode in circuit can be written as:

$$P_{tot} = P_{cond} + P_{sw} \tag{5.4}$$

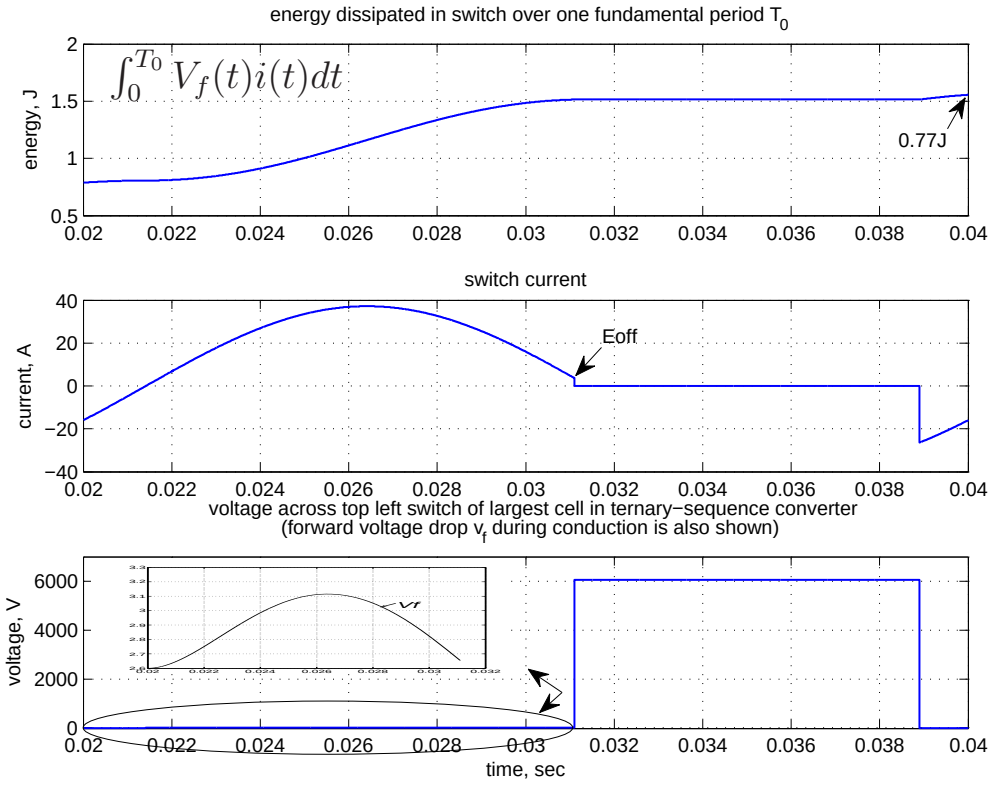


Figure 5.6: Voltage and current variation with energy dissipation of top left switch of largest cell in ternary-sequence converter.

5.5 Evaluation Criteria

As pointed out earlier in Chapter 2 that the trend in power semiconductor devices is towards HV-IGBTs, which have a MOSFET-like control properties and a bipolar-like conduction property designed in two main competing technologies, *i.e.,* NPT-IGBTs and PT- IGBTs. We will present the power loss comparison between these two varieties of IGBTs used in cascaded converter designs.

The choice of device technology is still an open question although the specific technology choice is narrowing with modern devices being a blend of traditional PT and NPT devices. When selecting a particular device for a specific application, there exists a tradeoff between fast switching characteristics and low forward voltages. Due to the market urge for smaller units and the concern about power losses, the question of inverter power losses versus costs has become a major issue. For this reason, a careful study has been performed on 600V, 1200V, 1600V/1700V, 3300V and 6500V classes of NPT IGBT. The following graphs of Figure 5.7, which are plotted by using the manufacturer data sheets, will help to understand the switching loss comparison at various current ratings of NPT IGBT.

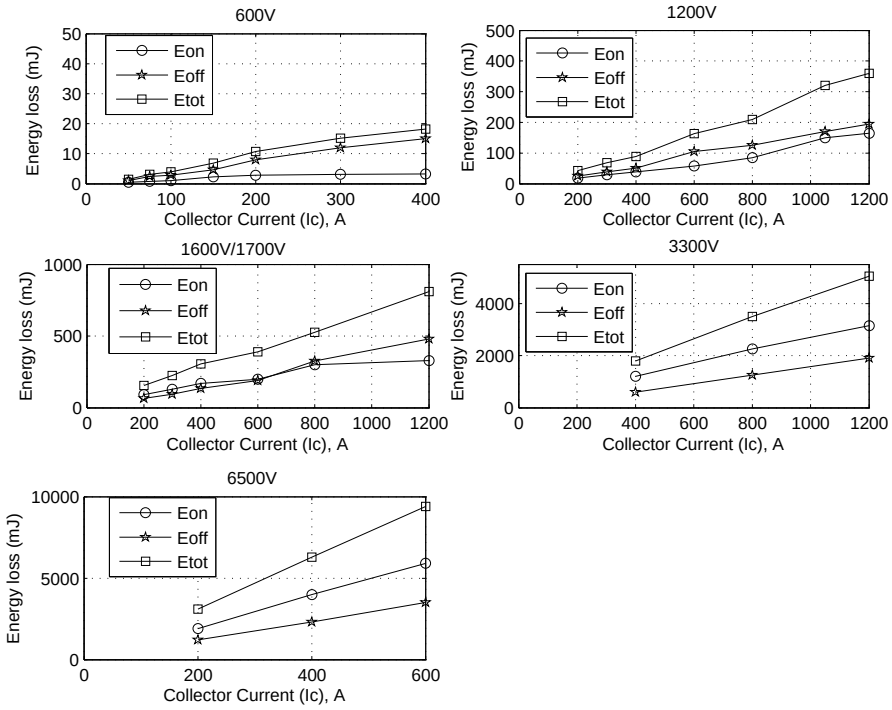


Figure 5.7: Energy loss per switch operation for various classes of IGBT at fundamental frequency (when switching at rated voltage).

In the ternary-sequence converter, the cell with the highest switching frequency has the lowest voltage rating in the chain and so it is not immediately obvious which cell suffers the highest switching loss. For example, one 6500V device can yield more switch loss at fundamental frequency than a 600V device switching at more than 2.5 kHz at same ampere rating. The graphs shown in Figure 5.7 are plotted using the manufacturer data sheets [131] and they form the basis of the switching loss comparison at various current and voltage ratings. The switching loss energies of the 600V IGBT are smaller by a factor of 4 to 5 as compared to the 1200V IGBT for the same device technology and current. This means that, connecting two 600V devices in series causes less than 50% of switching losses of one 1200V IGBT but results in twice the conduction losses (refer Figures 5.7 and 5.10). Further, replacing one 3300V device with two 1700V devices will reduce the switching loss energy by a factor of 3 but increase the conduction losses by around 33%. Interestingly, 3300V and 6500V devices have significantly higher turn-on losses than turn-off losses (internal geometry of the device changes at higher ratings). There is a high energy loss difference between the voltage classes of 1700V, 3300V and 6500V.

5.6 Investigation of 81 level Converters at 11kV

Ternary-sequence and equal-sized converters were simulated and compared first on an 11kV system. DC-link voltages, output voltages and switching frequency were calculated to construct 11kV phase voltages following careful selection of devices. The two converters have different constraints. For example, adding more cells in the ternary-sequence converter will increase the switching frequency of smallest cell in the chain, and of course, an IGBT has an upper switching frequency beyond which it cannot switch. Also, an equal-rated converter has 10 times more switches than the ternary-sequence converter in its layout, which increases the overall size and cost. In other words, this work is a comparison of 32 and 320 devices (ternary and equal rated respectively) on the 11kV system. Therefore, its essential to observe individual cells on the basis of their switching and conduction characteristics. Some of the simulation results of the model of the 0.5 MVA ternary-sequence multi-level converter are shown in Figure 5.8.

The dc bus currents flow through the four cells according to the switching states of the cells. These are decided by the output of the lookup tables in the PLECS/SIMULINK model. It can be seen that cell-I, which is the fastest in chain, commutates very fast compared to cell-IV which commutates at fundamental frequency and has the longest

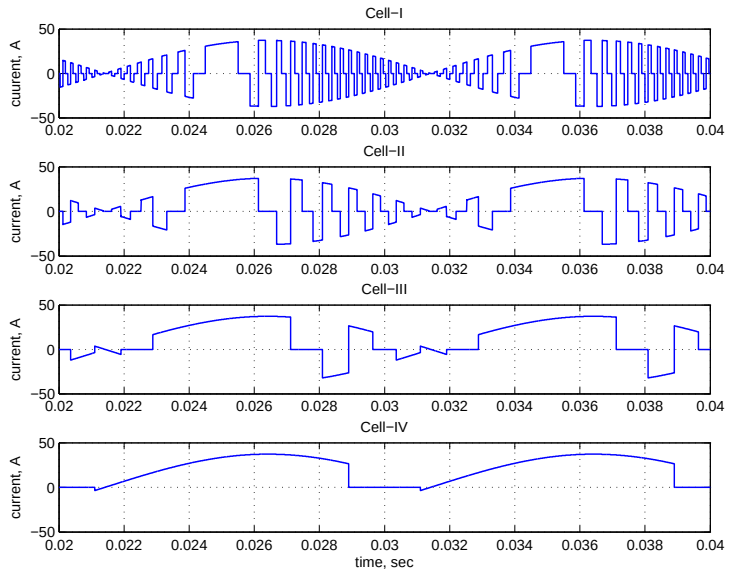


Figure 5.8: DC bus currents of a 4 cell converter in a 11kV Network.

continuous conduction time. In the first half of the fundamental cycle, the current flows from the positive dc-link terminal to the negative dc-link terminal. The period during which the current is zero in the dc-bus means cell is in off state and no current flows to or from the dc-bus. Here positive parts of the cell current flow through the IGBT and negative parts flow through the reverse conducting diodes which are anti-parallel to the IGBTs. In this state the cell is said to be free-wheeling.

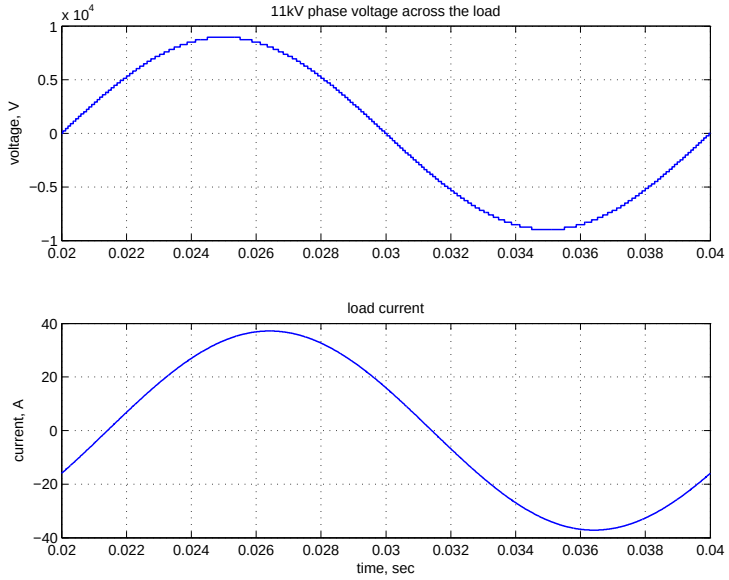


Figure 5.9: 11kV phase voltage (81 levels) and load current for ternary-sequence converter.

5.6.1 Forward-voltage drop Comparison for both Converters

In the ternary-sequence converter, 4 different devices (600V, 1200V, 3300V and 6500V) are used in the different voltage cells but the equal-size converter uses the same device (600V) for all of its cells in the chain. A variety of devices of different current ratings were selected for the range of MVA converter capacities required. Figure 5.10 shows that the value of v_f increases with MVA capacity except for the 4.0MVA case the device used at 4 MVA has a low v_{on} (*knee* of the *I-V* curve). Figure 5.11 shows a similar trend for the equal-size converter (with an exception at 6 MVA).

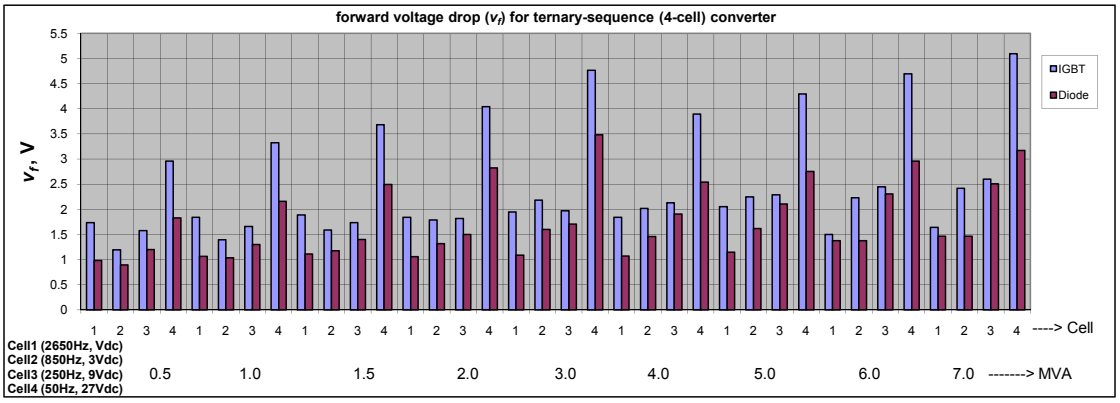


Figure 5.10: Forward-voltage drop of each cell of a ternary-sequence converter at several ratings.

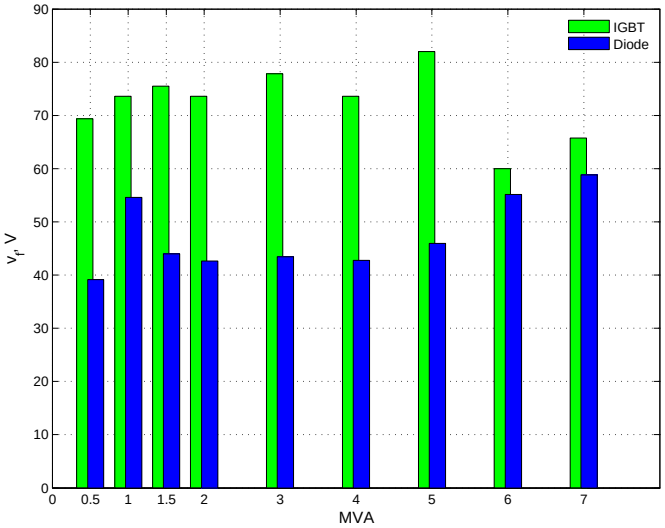


Figure 5.11: Forward-voltage drop for equal-sized converter.

5.6.2 Calculation Results for Total Loss

Various MVA capacities of multi-level converters were then designed keeping in view the availability of suitable devices. Simulations were performed for both converters and conduction and switching losses were calculated for each cell. The following loss calculation results shown in the Figures 5.12 - 5.14, show the switching and conduction losses of each cell. This analysis will help determine which devices in the chain dominate the losses.

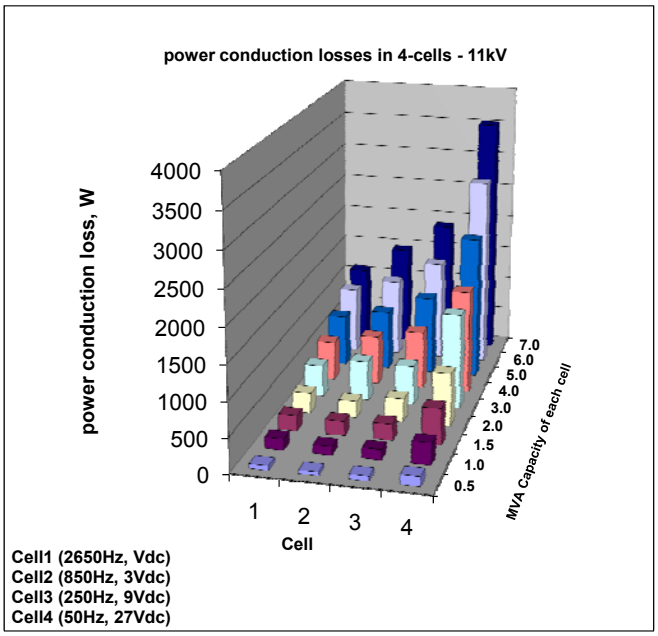


Figure 5.12: Individual conduction losses in 4-cells for 11kV system.

It is interesting to compare the performance of 4 cell converters with increasing MVA capacity (and therefore current). It can be seen that the device used in cell 3 stands out as different in its switching performance: it has the highest switching losses in all cases. The choice of device in cell 3 is far from ideal, however no other device was available with ratings close to those required and the next available device represents a large over design.

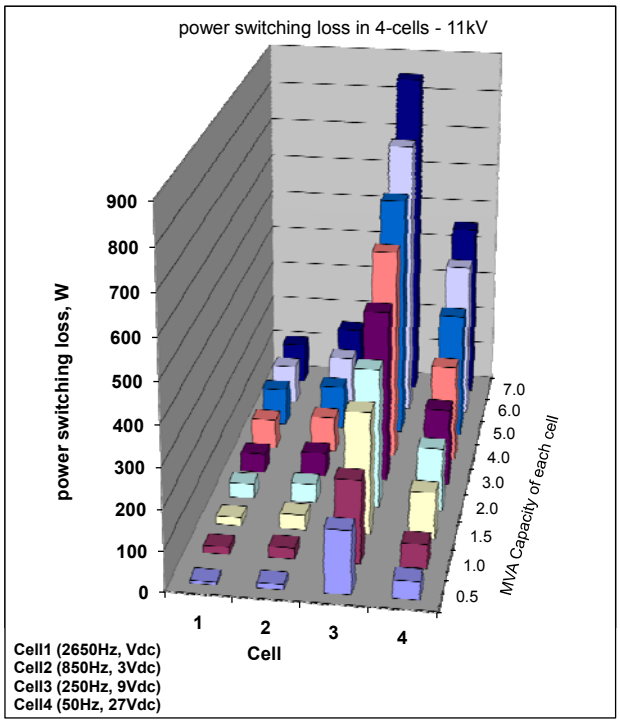


Figure 5.13: Individual switching losses in 4-cells for 11kV system.

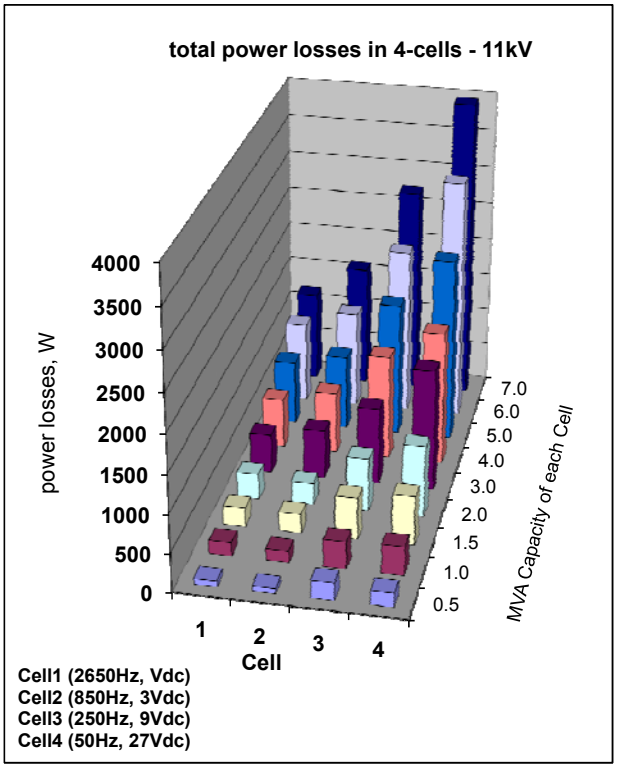


Figure 5.14: Total power losses in 4-cells for 11kV system.

It was cited earlier in Section 5.5 (during the IGBT survey and analysis) that the 600V device, whose switching frequency is more than 2.5 kHz, can produce less switching losses than the 6500V or 3300V device switching at slightly above or at the fundamental frequency. Cell-1 (600V/2650Hz) and cell-2 (1200V/850Hz) are switching 10 times and 3.5 times faster than cell-3(3300V/250Hz) but their rating is 5 times and 3 times less then cell 3 which consequently reduced the switch loss of cell 1 and cell 2. This phenomenon can be observed in all the results shown Figure 5.14. Cell 4, using a 6500V device has the highest conduction losses because of its high v_f. Overall, cell 4 produces maximum losses in the chain followed by cell 3. However, it should be noted that its rating is 27 times more than the smallest cell, whereas its overall losses are 3.5 times the smallest in the chain. This shows that although it contributes high absolute losses, it is still the most efficient cell. Cell 1 and 2 share almost same percentage of losses everywhere.

Figure 5.15 and Figure 5.16 depicts the comparison of overall power losses in the two converters. The ternary-sequence multi-level converter overall has 5 times less losses than an equal-sized converter. The conduction losses are dominant everywhere in both converters. As equal-sized converter uses 600V device which is considerably very low in rating and its switching frequency is 50Hz and therefore, it has negligible switching losses.

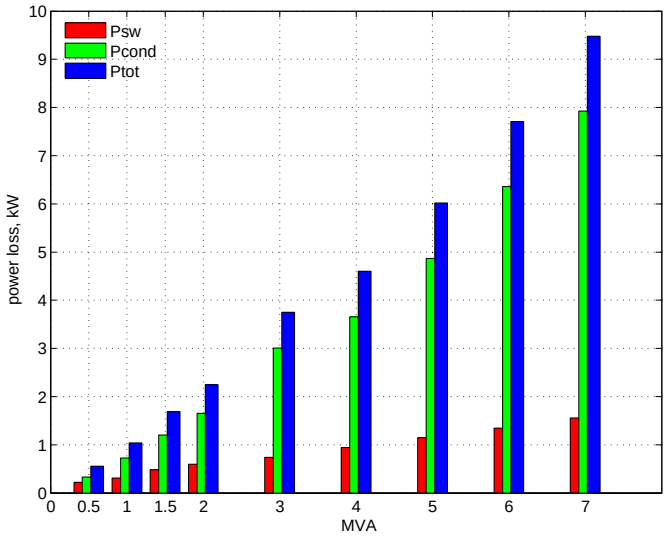


Figure 5.15: Overall power losses in all 4 cells of the ternary-sequence multi-level converter - 11kV system.

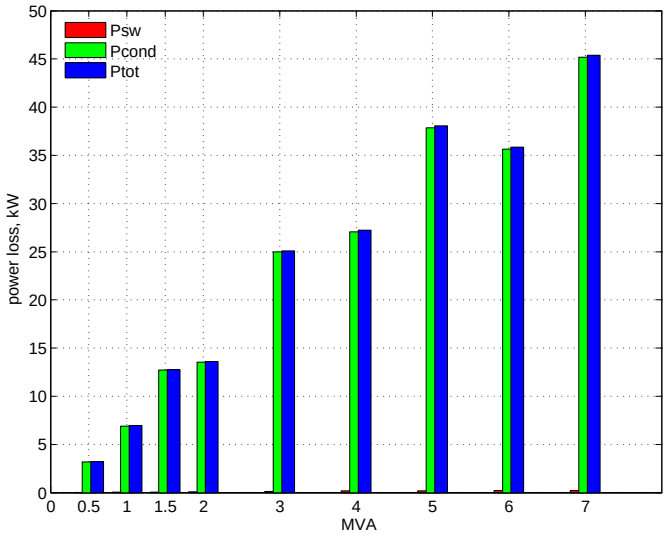


Figure 5.16: Overall power losses in 40 cells in equal-sized multi-level converter - 11kV system.

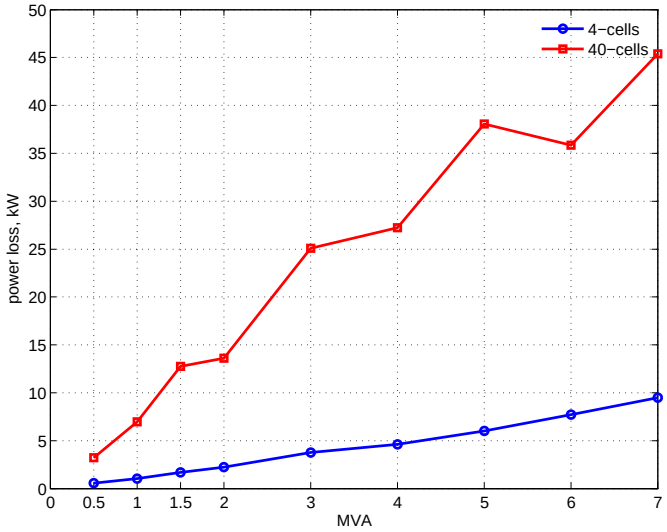


Figure 5.17: Power loss comparison between 40 and 4 cells in both equal-rated and ternary-sequence converters - 11kV System.

5.7 Investigation of 81 level Converters at 33kV

Figure 5.18 shows the basic structure of the ternary-sequence multi-level converter for a 33kV system. As the output voltage is 3 times higher than the 11kV system, the voltage level of each cell level is also increased. The selection criteria for devices in the

model was based on choosing better performances (and thus more expensive devices) as it is expected that the cost of power losses over a life cycle of a device would be much higher than the capital cost during the construction. As an example, two 600V devices are connected in series instead of using a single cheaper 1200V IGBT module for smallest cell in chain which has switching frequency of 2650Hz because they cause only 40 to 50 percent of the switching losses of one 1200V IGBT at same current rating while increasing the conduction losses by less then twice. This result in lower overall loss in this cell. Three 6500V IGBTs are used for the largest voltage cell because a single 18000V device is not available. In the middle, 3300V and 6500V IGBTs are used.

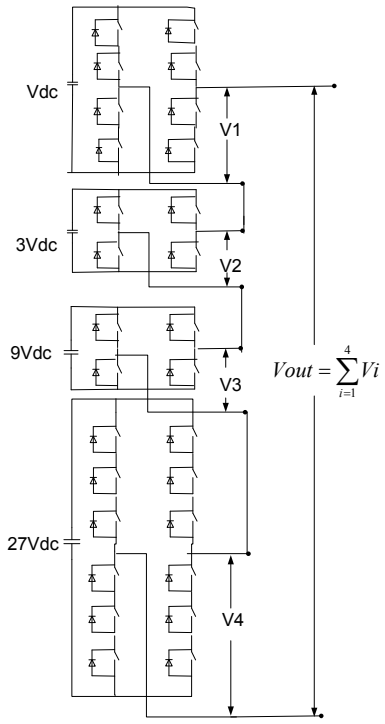


Figure 5.18: Design of ternary-sequence multi-level converter for 33kV system showing use of series valves to achieve required voltage blocking.

5.7.1 Forward-voltage Drop for both Converters

The number of IGBT modules used are more than in the 11kV design *i.e.,* now one device is replaced by 2 or 3 series devices, therefore the forward voltage drop is high in comparison to the previous case as shown in Figure 5.19 and Figure 5.20. In particular, cell 4 has 4 times more forward voltage drop in contrast to other three cells in the chain because it has 3 x 6500V IGBT modules in series instead of a single IGBT. The 40-

cell equal rated converter uses 1200V/200A devices throughout its chain in all the MVA sizes. Further, the equal-size converter has much higher forward voltage drop because of 10 times more devices are employed in its chain than ternary-sequence converter. It should be noted that the 4-cell converter does not use the 1200V device at all.

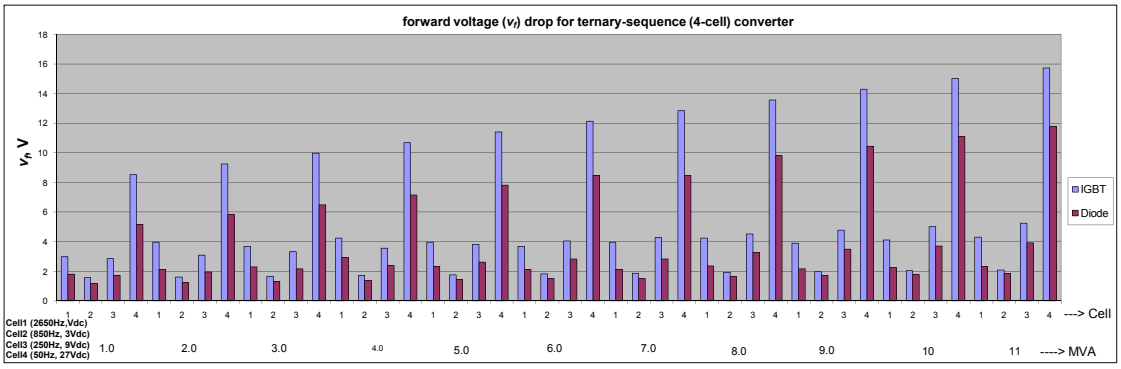


Figure 5.19: Forward-voltage drop for ternary-sequence converter.

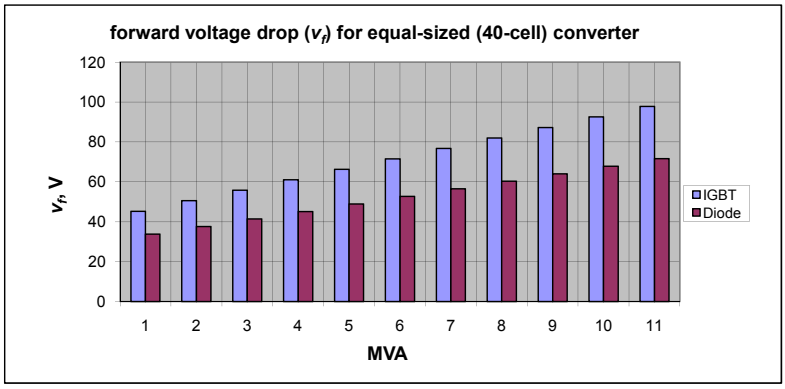


Figure 5.20: Forward-voltage drop for equal-sized converter.

5.7.2 Calculation Results for Total Loss

It is expected that cell 4 (which has the highest forward voltage drop) as shown in Figure 5.19 will yield more conduction losses compared to the other cells in the chain. Interestingly, this time the 3300V device, which produced maximum switching losses as cell 3 (f_{SW} = 250Hz) in previous case is now moved to cell 2 (f_{SW} = 850Hz) switching 3.5 times faster than in 11kV system and proves to be a poor device again. However, this device has less conduction losses compared to the neighboring cells in the chain for all MVA capacities of the ternary-sequence converter. We can see that cell 1 which is using $2 \times 600V$ devices instead of one large 1200V device has been a good choice because

it has trivial switching losses even at more than 2.5kHz. The conduction losses in each cell are shown in Figure 5.21.

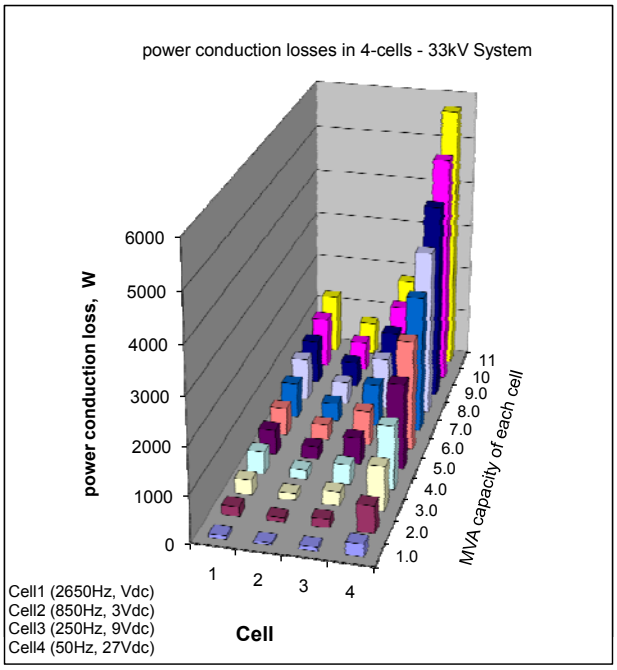


Figure 5.21: Individual conduction losses in 4-cells for 33kV system.

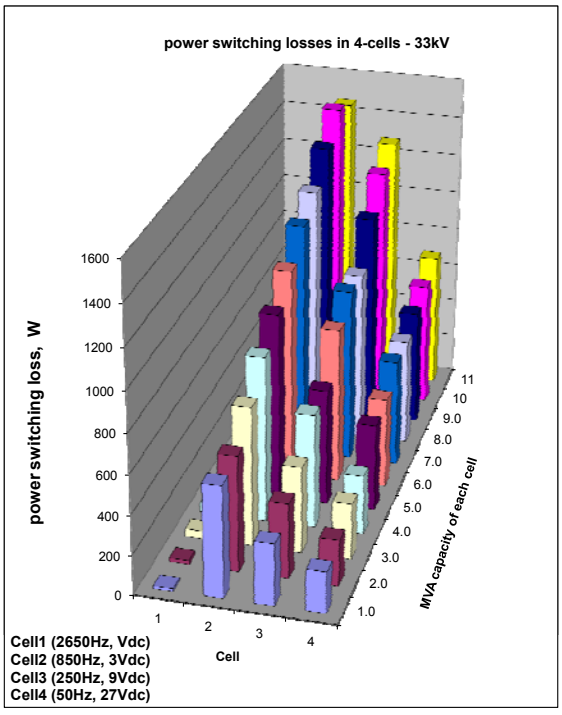


Figure 5.22: Individual switching losses in 4-cells for 33kV system.

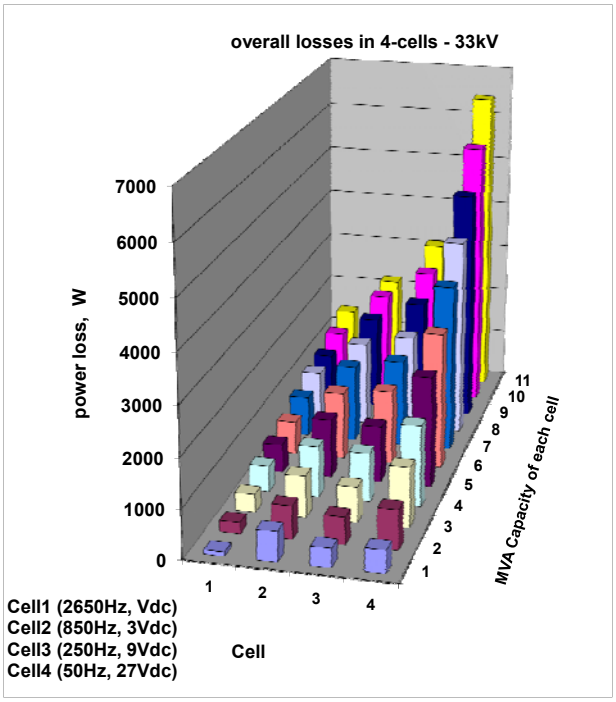


Figure 5.23: Individual overall power losses in 4-cells for 33kV system.

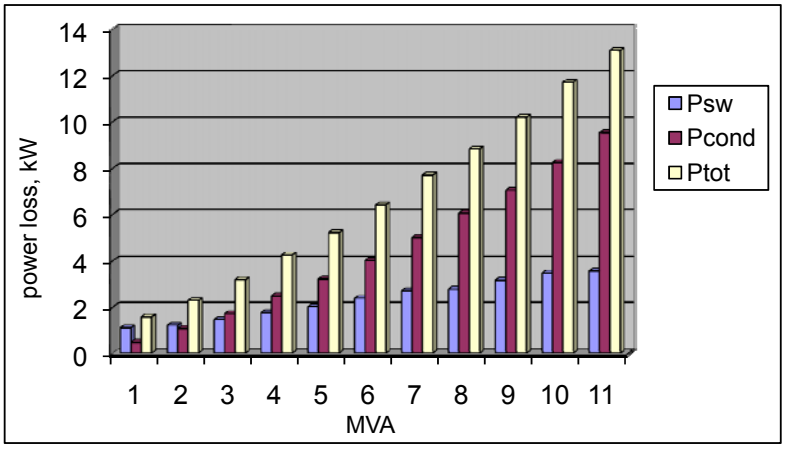


Figure 5.24: Overall power losses in ternary-sequence (4-cell) multi-level converter - 33kV system.

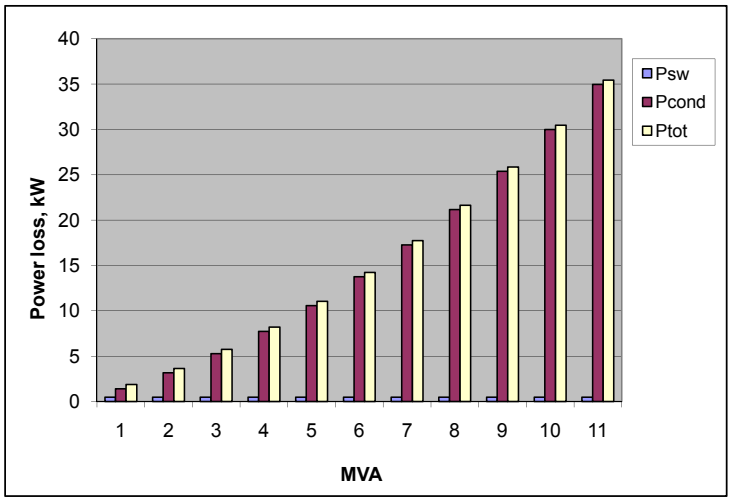


Figure 5.25: Overall power losses in equal-rated (40-cell) multi-level converter - 33kV system.

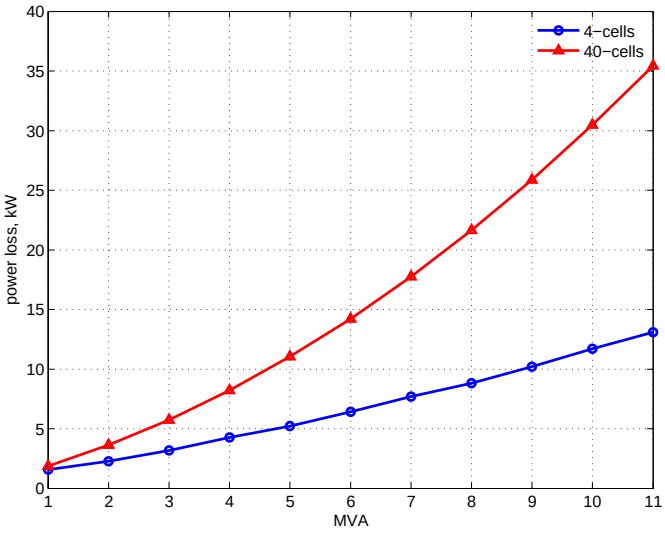


Figure 5.26: Comparison between overall power losses in equal-rated 4 and 40-cell multi-level converter - 33kV system.

5.7.3 Discussion of the 81 Level Converter

Cascaded multi-level converters of 81 levels were assessed on 11kV and 33kV distribution systems. The ternary and equal-sized converters required 4 and 40 cells respectively. It was observed that an appropriate selection of device ratings and series and parallel combinations can reduce the power losses. The ternary-sequence converter used different device ratings in each cell. The equal-sized converter used the same device in each cell.

In this example, the ternary-sequence has one cell which is underutilized and produces more losses than expected. An example of this cell could be present at any stage in the chain. In this example, the modeling of ternary-sequence converter, cell no. 3 and cell. no. 2 were the culprits for 11kV and 33kV distribution system respectively. This anomaly could probably be resolved by changing the device design for which we are dependent on the power semiconductor manufacturers. In the coming sections different IGBT technology will be tested in order to try to improve performance of this cell. Overall, the ternary sequence converter has lower losses than the equal-rated topology due to the lower conduction loss in ternary sequence devices to fewer cells.

5.8 Investigation of 27 Level Converters at 11kV

The 27 level case uses 3 and 13 cells for ternary and equal-sized converters. The required magnitude of output voltage is still 11kV phase voltage but now the number of cells is reduced therefore the voltage level of each cell in the chain must be raised and thus the rating of the individual devices increased as well.

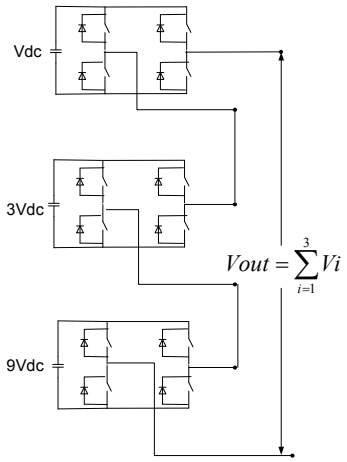


Figure 5.27: Design of ternary-sequence multi-level converter using 3 cell.

Figure 5.27 shows the configuration of the ternary-sequence converter. This converter uses 1200V, 3300V and 6500V devices for the cells, from top to bottom, with switching frequencies of 850Hz, 250Hz and 50Hz respectively. The equal-sized converter uses 1200V devices throughout in its chain in addition to the mentioned device ratings of ternary-sequence converter.

5.8.1 Forward-voltage Drop for both Topologies

To calculate the conduction losses in these devices, the on-state voltages and slope resistances were taken from their data sheets. These values were plotted over the range of MVA capacities of multi-level converter. Figure 5.28 shows the forward voltage drop of ternary-sequence converter. Cell 3 which used a 6500V device, is dominant in forward voltage drop (except at 4MVA because that device has a particularly low v_{on}). Figure 5.29 shows a similar trend for the equal-rated converter as the ternary-sequence converter.

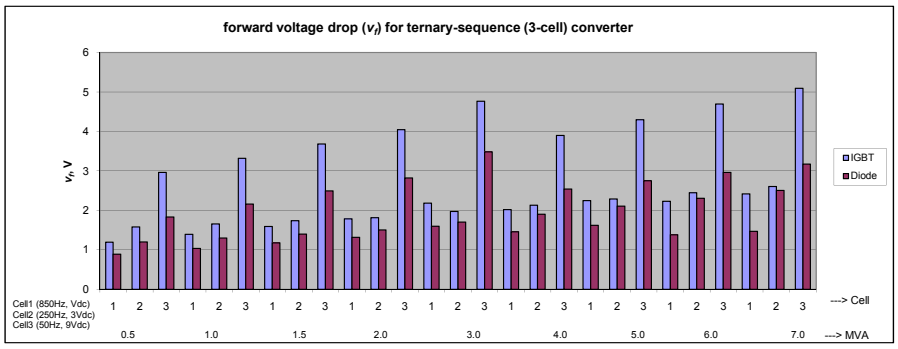


Figure 5.28: Forward-voltage drop for ternary-sequence converter.

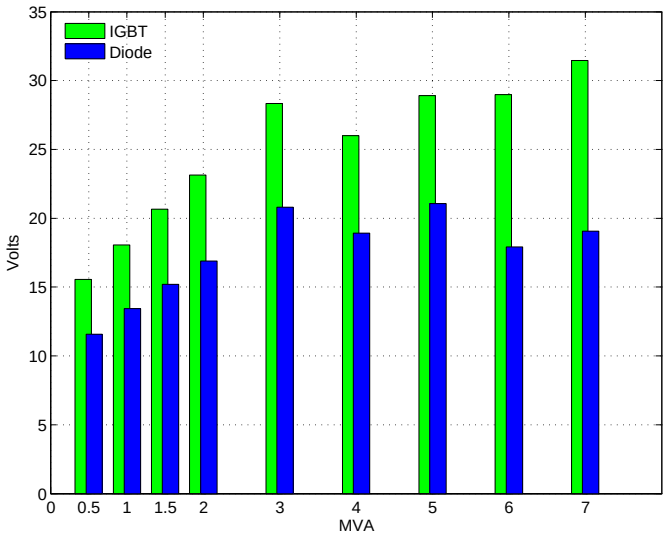


Figure 5.29: Forward-voltage drop for equal-sized converter.

5.8.2 Calculation Results for Total Loss

It would be reasonable for cell 3 in the ternary-sequence converter to cause the largest conduction loss due to its high forward voltage drop characteristics as shown earlier in Figure 5.28. Cell 2 is 3300V device which proved to be bad device in switching losses for 4-cell converter for 11kV and 33kV network. Now again, it produces the highest switching losses and shares the maximum losses for 7.0MVA capacity as depicted in Figure 5.30 as a sample result. Cell 3, which uses a 6500V device, shares the largest part of losses because its conduction losses increases at much higher rate than cell 2 switching losses. It can be seen that cell 2 has the highest switching losses and cell 3 has the highest conduction losses.

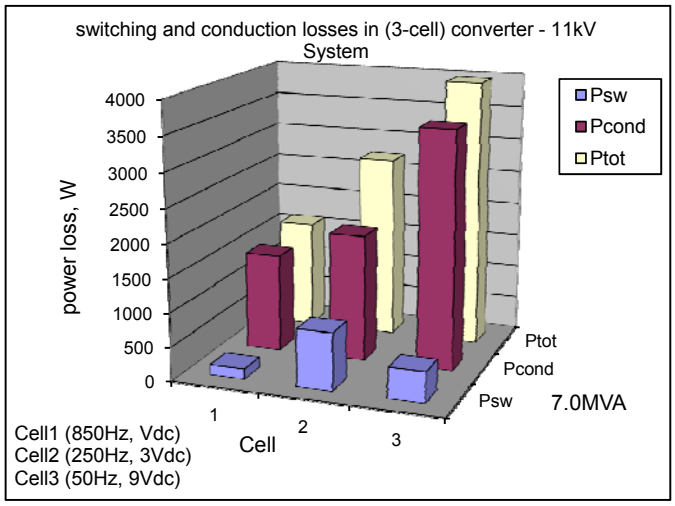


Figure 5.30: Power Losses in 3-cell at 7.0MVA (sample result).

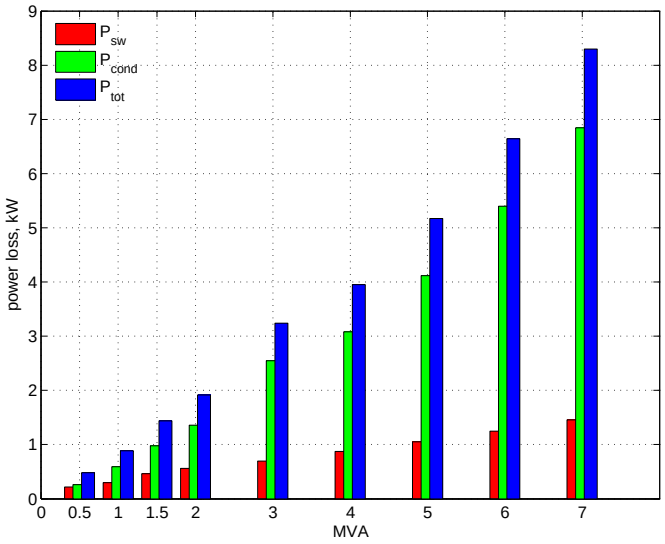


Figure 5.31: Overall Power Losses in ternary-sequence (3-cell) converter.

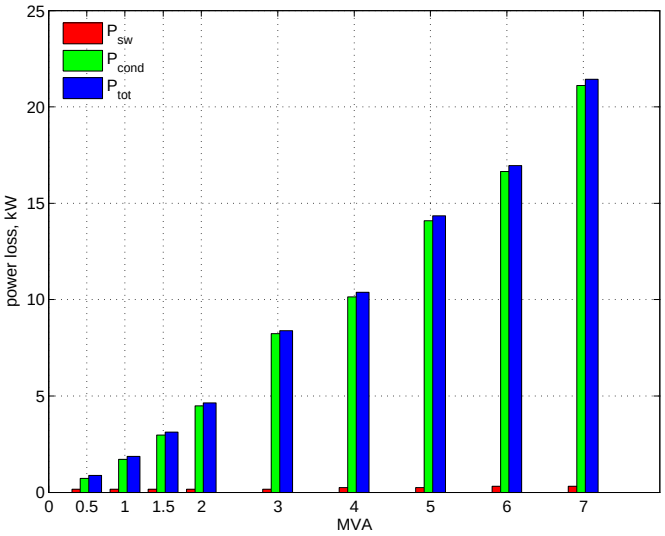


Figure 5.32: Overall Power Losses in equal-sized (13-cells) converter.

After analysing both 27 level converters (3 vs. 13 cells), the ternary sequence design has approximately two and half times lower losses than equal-rated converter. This makes ternary-sequence superior to equal-rated converter. The overall power loss calculation is shown in the Figure 5.31 and Figure 5.32 for both converters. Losses rise quadratically in both converters with MVA rating. The equal-sized converter has negligible switching losses due to its fundamental switching frequency for each cell in the chain. The simple formula of power loss eqn. (5.1) is tested against the results obtained in our simulations

to indicate the general trend of power conduction losses. This work will be shown in the Section 5.12.

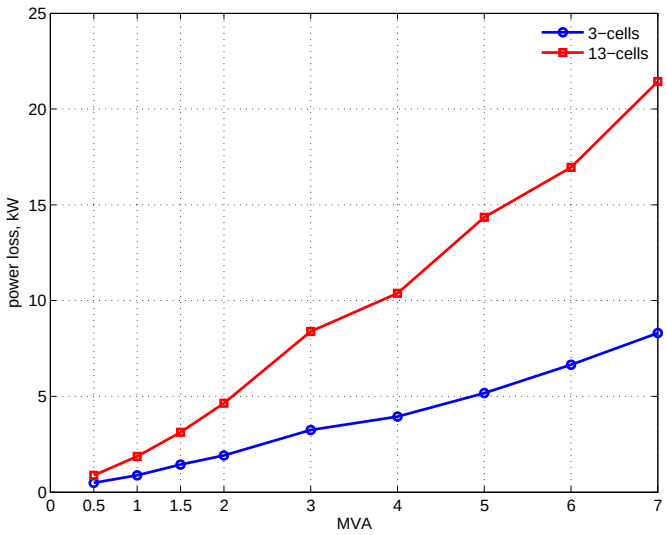


Figure 5.33: Power Loss comparison between 13 and 3 cells in both equal-rated and ternary-sequence converters - 11kV System.

5.9 Investigation of 27 Level Converters at 33kV

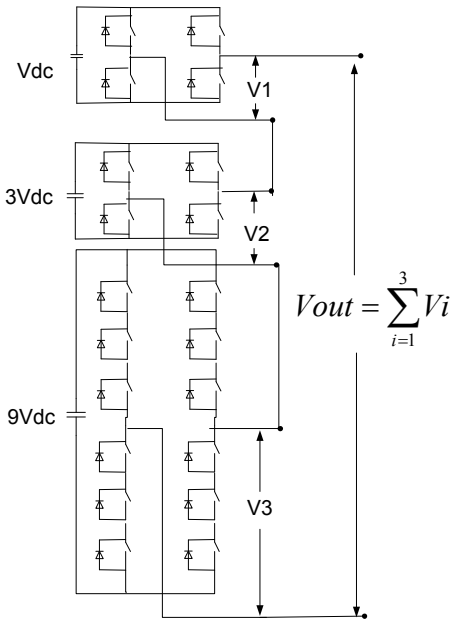


Figure 5.34: Design of ternary-sequence converter for 33kV System.

Figure 5.34 shows the design of a ternary-sequence converter for the 33kV distribution network. This converter uses three cells switching at 850Hz, 250Hz and 50Hz from top to bottom respectively. Here, the smallest cell uses 3300V devices as the fastest switching device in the chain whereas the other two cells are 6500V and 3 x 6500V respectively. The equal-sized converter uses 3300V devices throughout the chain for its 13 cells. For the case of the ternary-sequence converter, it is expected that cell-1 which is comprised of 3300V devices will produce the highest switching losses compared to the other two cells. In the previous converter design cases, we have seen 3300V device producing considerably higher switching losses even at lower switching frequencies in comparison to other cells in the chain. But especially this time due to its top position in the chain will allow it to produce the highest switching losses amongst all the precedent ternary-sequence cases. On the other hand, it posses the best conduction characteristics in contrast to other devices. Hence, it will have maximum switching and minimum conduction losses in all designed MVA capacities at 33kV system. Cell 3 is using 3 x 6500 IGBTs which must have highest v_f so it will lead in the conduction losses.

5.9.1 Forward-voltage Drop for Both Converters

We know that cell 1 is likely to have the lowest conduction loss and cell 3 has maximum v_f drop in the chain due to the requirements on blocking voltage. This agrees with Figure 5.35. Further, the equal-sized converter, which uses 3300V devices has proved to be the best device so far amongst all the equal-sized converter cases during these simulations. Analysis was also carried out to use two 1200V devices instead of one 3300V device to fulfill the same requirement but it had 3 times more v_f drop. Finally, the 3300V device has tilted the decision of equal-sized converter in its favor of ternary-sequence converter in the 33kV distribution system with 27 levels. This result has shown that the equal-sized converter can be superior over the ternary-sequence in some cases. This clearly indicates that if the device fits to the system requirement very well, then over all power losses can be minimised.

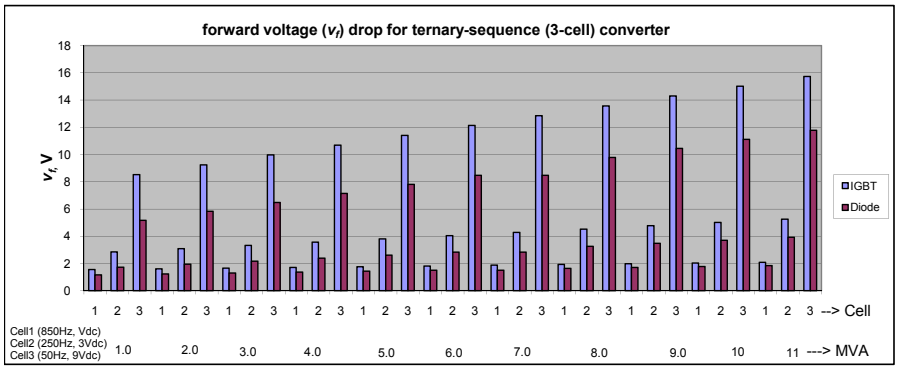


Figure 5.35: Forward-voltage drop for ternary-sequence converter.

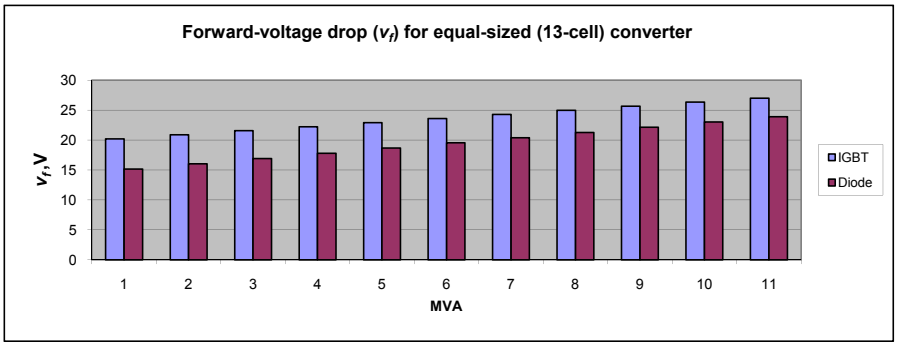


Figure 5.36: Forward-voltage drop for equal-rated converter.

5.9.2 Calculation Results for Total Loss

The results from the calculation of losses indicates that cell 1 has highest number of switching losses but minimum conduction losses in comparison to others at various MVA capacities. Cell 3 which has the highest forward voltage-drop v_f will produce maximum conduction losses. Cell 3 has overall maximum losses in the chain.

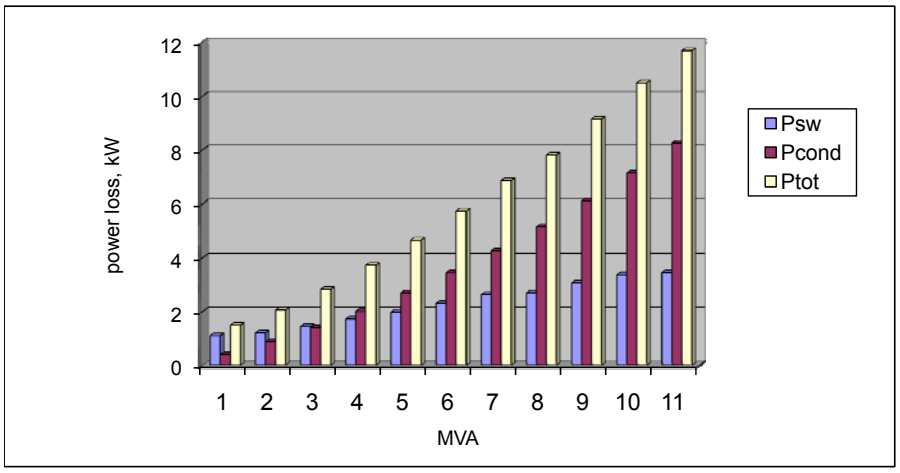


Figure 5.37: Overall Power Losses in ternary-sequence (3 cells) converter.

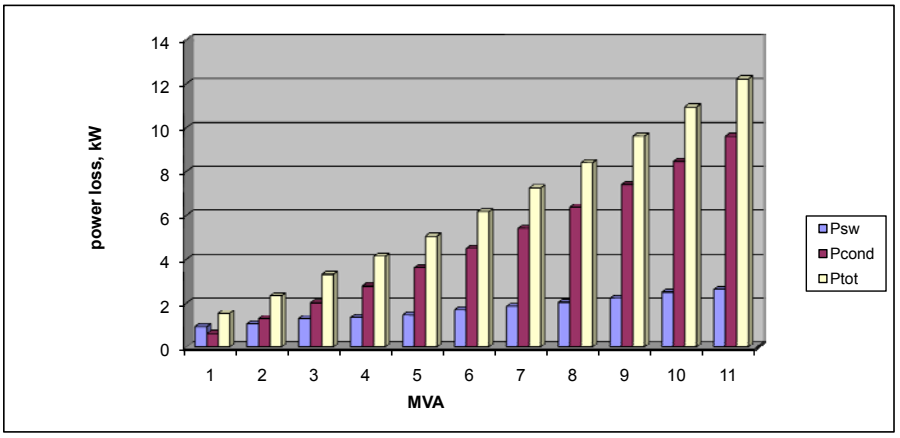


Figure 5.38: Overall Power Losses in equal-sized (13-cells) converter.

From the comparison of the two results from Figure 5.39 that both the converters have almost similar overall losses in the designed MVA capacities which was not happening in all the previous cases. It can be observed that losses are significantly reduced in equal-rated converter. It's because 3300V device which is used in the design has very high switching loss per turn on/off but has proved to be an excellent device for equal-rated converter in terms of conduction losses. This comparison has made the equal-sized converter superior to ternary-sequence converter.

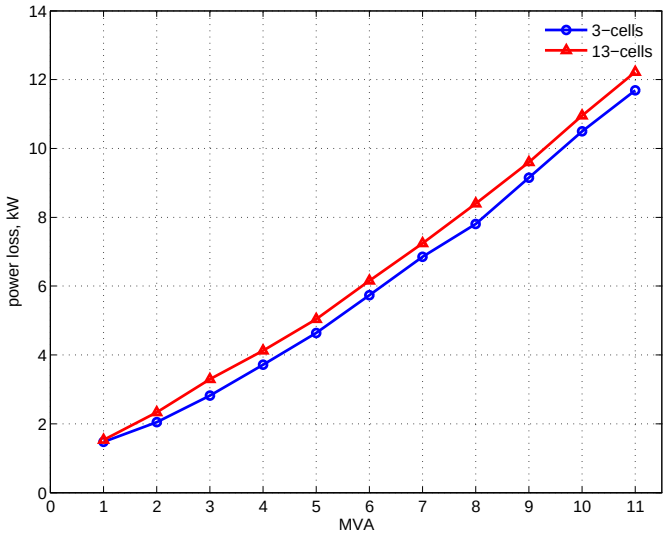


Figure 5.39: Comparison of overall Power Losses between equal-sized 3 and 13 cells converter - 33kV system.

5.10 Review of Converter Losses (ternary and equal-rated)

A review of losses for both the converter topologies using NPT IGBTs is presented in this section. On the 11kV system:

- The 4 and 3 cell ternary topology is significantly more efficient,
- The 13 cell converter takes second position whereas 40 cell converter is the least efficient. This difference is observed due to the major contribution of conduction losses in 40-cell equal-rated topology. The trends for 11kV system can be observed from the Figures 5.40 - 5.42.

In 33kV system, one interesting revelation is detected:

- The 13-cell topology has almost same efficiency as 4 and 3 cell converters,
- whereas 40-cell converter stands-out in terms of highest percentage of losses amongst all types of topologies. The graphical presentation of 33kV system analysis can be seen in the Figures 5.43 - 5.45.

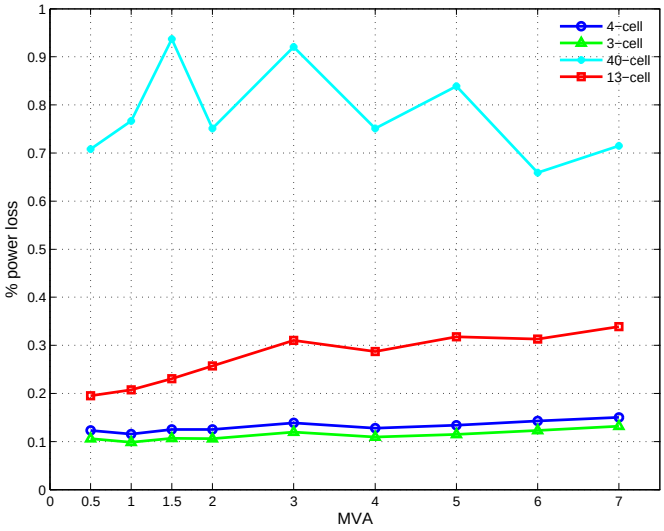


Figure 5.40: Review of percentage overall losses in both types of converters in 11kV system.

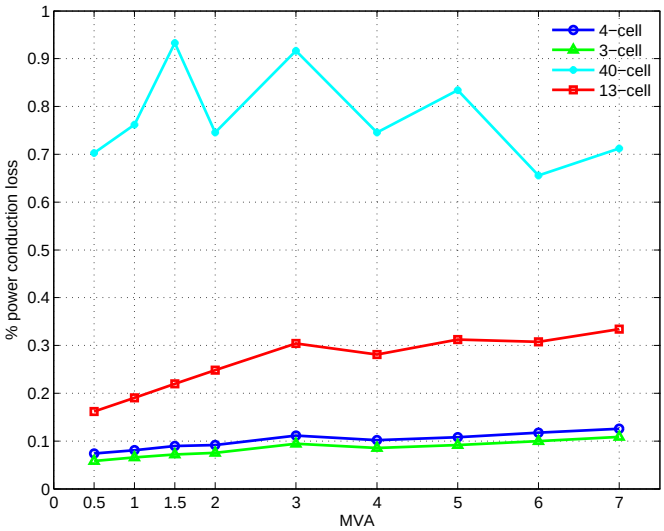


Figure 5.41: Review of percentage conduction losses in both types of converters in 11kV system.

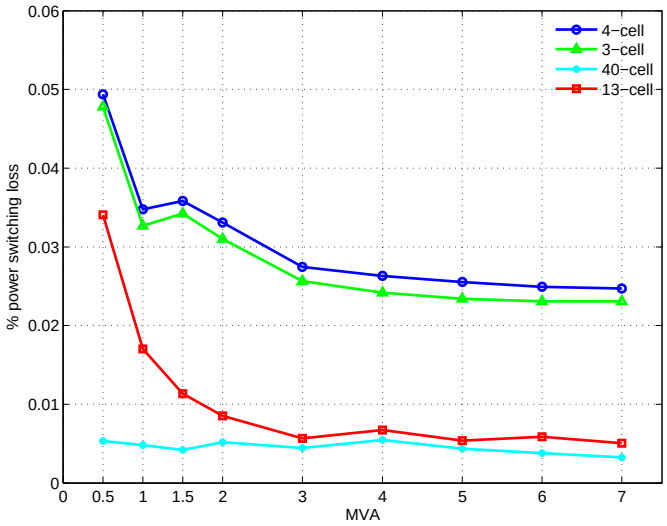


Figure 5.42: Review of percentage switching losses in both types of converters in 11kV system.

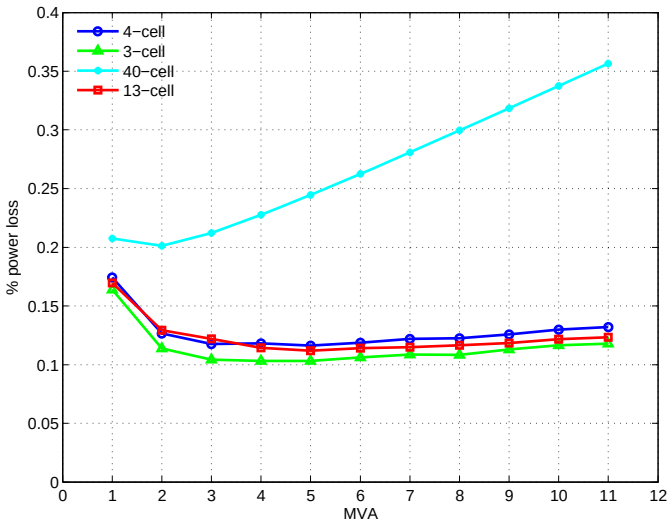


Figure 5.43: Review of percentage overall losses in both types of converters in 33kV system.

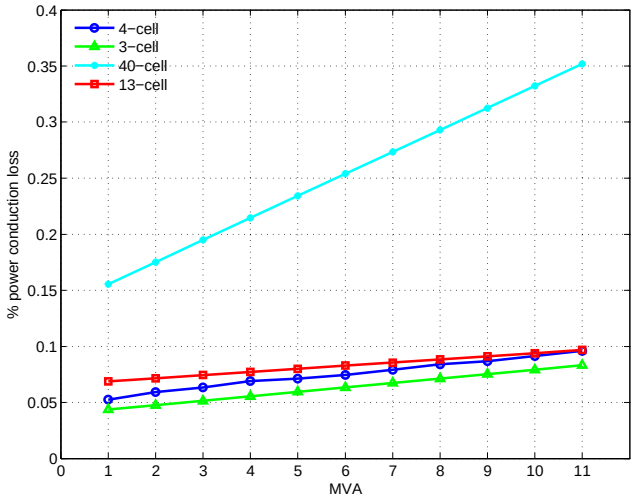


Figure 5.44: Review of percentage conduction losses in both types of converters in 33kV system.

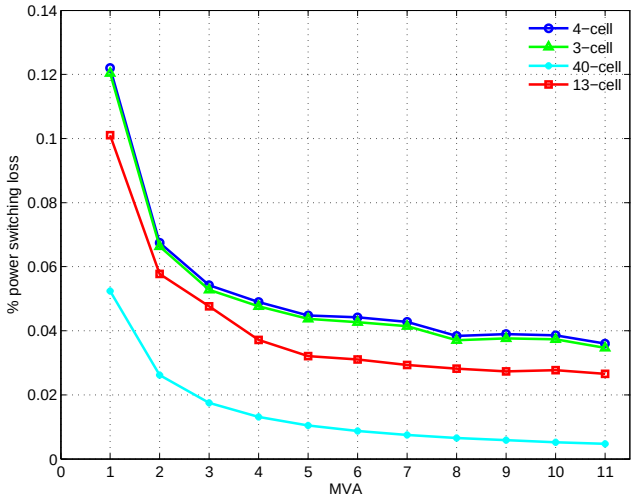


Figure 5.45: Review of percentage switching losses in both types of converters in 33kV system.

5.11 Loss comparison of NPT and PT IGBT

So far, the loss evaluation of both kinds of cascaded converters was presented using NPT IGBTs. This analysis was further extended to PT IGBTs to see if the device technology, specifically the different balance of conduction and switching loss, will affect the choice of converter. In the PLECS/SIMULINK model, the data of NPT IGBT was replaced by PT IGBT.

Table 5.1: Overall loss comparison summary of NPT and PT IGBT on 11kV and 33kV system

	Cell	11kV system	33kV System
81-Levels	(T) 4	NPT IGBT has 4-8% more losses	NPT IGBT has 5-25% more losses
	(E) 40	NPT IGBT has 15-30% more losses	PT IGBT has 25-50% more losses
27-Levels	(T) 3	NPT IGBT has 5-10% more losses	NPT IGBT has10-25% more losses
	(E) 13	PT IGBT has 15-30% more losses	NPT IGBT has 5-10 % more losses

The same assessment approach was adopted and all the system parameters were same except the device model now contains PT IGBTs slope resistances and on-state voltages of device manufacturer. Procedure for the loss calculation of cascaded converters described earlier was repeated in order to compare PT IGBTs to NPT IGBTs. The importance of inverse conducting diode should not be forgotten as it has an impact in the overall loss calculation results. The detail survey on various voltage classes of PT IGBT devices was undertaken and few unexpected facts were revealed about reverse conducting diodes. These diodes are sometimes overlooked while analysing converters. Inverse diodes which come along with the PT IGBT generally have more reverse recovery energy loss and less forward conduction losses in comparison to NPT IGBT. This fact has not really made a great deal of overall difference in the calculations because gaining on one hand and loosing on the other was taking place. The main difference observed was at 3300V device position in the ternary type of converters. In PT IGBT case, the 3300V devices has contributed 2 to 3 times less switching loss. A summary of the comparison between the NPT and PT IGBT technology is shown in Table 5.1.

5.12 Validation of Empirical Power Conduction Losses in Cascaded Converters

So far this work has investigated two attractive topologies of cascaded multi-level converter designs for achieving multiple voltage levels, with the aim of quantifying the power losses and hence the efficiency. The analysis considers different loss mechanisms and gives out quantitative descriptions of the power losses in each cell of the converter and useful design criteria in distribution networks. The analysis was done on different IGBT structures available in the market. It was desirable to predict power losses beyond the

available measured cases and develop a method which facilitates the rapid evaluation of converter designs.

This section extends the previous analysis, and takes steps in performing empirical validation of ternary-sequence converter loss findings against the power loss eqn. (5.1). Curve fitting techniques were applied using the fundamental power loss model. The plotted outputs yielded a close curve-fit to the power loss estimates generated through time-domain simulations, as presented in the previous section. The fitted curves developed for a range of converter designs have been used to find (to date) unknown constants of the power loss expression for each cell in the ternary-sequence converter chain. Inputting these constants into the power loss expression we can then easily predict losses for any cell in the chain, and extrapolate the power loss for an additional cell of future converter designs. This avoids the time-consuming simulation runs and laborious compilation of data. The developed model is fairly accurate to within about ten percent.

Rewriting eqn. (5.1):

$$\Delta P_{loss} = \frac{1}{T_0}\int_{t_1}^{t_2}\left[\left(I_m^2 \sin\omega t\right) R_{Slope} + v_{on} I_m \sin\omega t\right] dt \tag{5.5}$$

where I_m is the peak value of the switch current, and the ΔP_{loss} is the conduction loss in a switch within a specific time interval $[t_1 \;\; t_2]$ in one fundamental conduction cycle of T_0 interval. Note that conduction intervals can occur more than once in each cycle depending upon the switching function $f(t)$ of each cell. Example of current conduction in cells is shown in Figure 5.8, where conduction intervals are observed in one cycle.

After solving eqn. (5.5) we get:

$$\Delta P_{loss} = \frac{1}{T_0}\left[\frac{I_m^2 R_{Slope}}{2}\left\{\frac{2\omega\left(t_2 - t_1\right) + \sin(2\omega t_1) - \sin(2\omega t_2)}{2\omega}\right\} + \frac{v_{on}}{\omega} I_m \left(\cos(\omega t_1) - \cos(\omega t_2)\right)\right] \tag{5.6}$$

we already know: $\omega = 2\pi f$ and $T_0 = 1/f$ (=0.02sec), then eqn. (5.6) takes the form:

$$\Delta P_{loss} = I_m^2 R_{Slope} K_1\left(t_2, t_1\right) + v_{on} I_m K_2\left(t_2, t_1\right) \tag{5.7}$$

where K_1 and K_2 are constants:

$$K_1\left(t_2, t_1\right) = \left(\frac{200\pi\left(t_2 - t_1\right) + \sin\left(200\pi t_1\right) - \sin\left(200\pi t_2\right)}{8\pi}\right),$$

$$K_2\left(t_2, t_1\right) = \frac{1}{2\pi}\left(\cos(100\pi t_1) - \cos(100\pi t_2)\right)$$

Total power conduction loss for all time intervals in a cycle can be evaluated as:

$$P_{loss} = I_m^2 R_{Slope} \sum_{[t_1 \;\; t_2] \in f(t)} K_1\left(t_2, t_1\right) + v_{on} I_m \sum_{[t_1 \;\; t_2] \in f(t)} K_2\left(t_2, t_1\right) \tag{5.8}$$

Each device is characterised by R_{slope} and v_{on} and is fixed for each cell of the ternary sequence converter, so eqn. (5.8) reduces to:

$$P_{loss} = I_m^2 a\left(C_N\right) + I_m b\left(C_N\right) \tag{5.9}$$

which calculates power conduction loss in each cell of the converter. C_N is the cell number in the chain, where $C_N = 1, 2, 3, 4$ (for a 4-cell topology).

Equation (5.9) tells us that the expected trend of power loss in each cell is quadratic in I_m. The unknown coefficients $a(C_N)$ and $b(C_N)$ of eqn. (5.9) are determined by applying a polynomial curve fitting, in a least squares sense, of the measured conduction losses P_{loss} shown with a red + in Figures 5.46a and 5.48a (sample results) for 11kV and 33kV systems respectively. We have determined $a(C_N)$ and $b(C_N)$ values corresponding to each cell in the chain. These values are plotted in Figure 5.46b and 5.48b, shown as +, against each cell number.

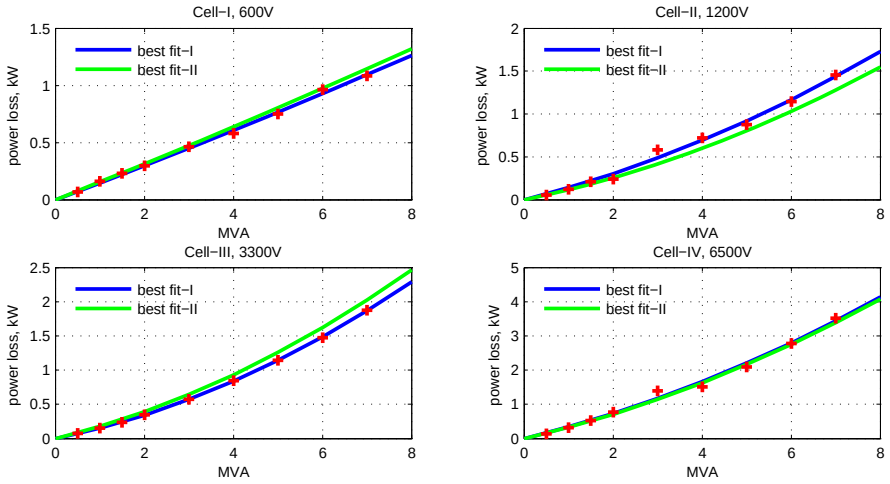
The following models were then used to obtain $a(C_N)$ and $b(C_N)$ against the cell number C_N to observe their generic trend:

$$a\left(C_N\right) = a_1 C_N^2 + a_2 C_N + a_3 \tag{5.10}$$

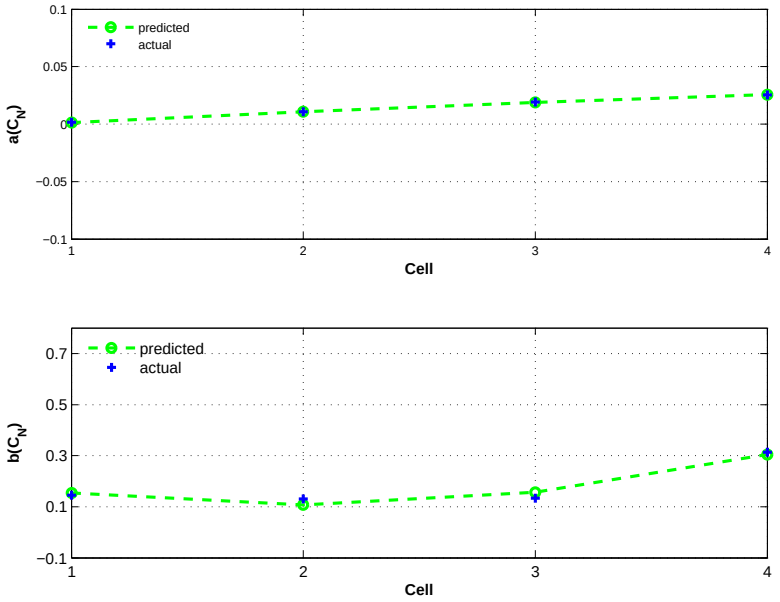
$$b\left(C_N\right) = b_1 C_N^2 + b_2 C_N + b_3 \tag{5.11}$$

In the above model the unknown coefficients: a_1, a_2, a_3 and b_1, b_2, b_3 are determined by using the computed values of $a(C_N)$ and $b(C_N)$ from eqn. (5.9), with their values shown in Table 5.2.

Hence we recalculate the new values of $a(C_N)$ and $b(C_N)$ using the model eqn. (5.10) and eqn. (5.11); bearing in mind that now we have the estimated coefficients: a_1, a_2, a_3 and b_1, b_2, b_3. The new predicted $a(C_N)$ and $b(C_N)$ are plotted in o, and the fit is given by a green broken line in the Figure 5.46b and 5.48b, labelled as 'predicted'. An accurate fit of the results is obtained.



(a)



(b)

Figure 5.46: Curve fitting for the power conduction loss for a 4-cell topology - 11kV (a) Best fits of power loss against MVA from Cell I to Cell IV (b) Estimated and predicted coefficients a and b for each cell.

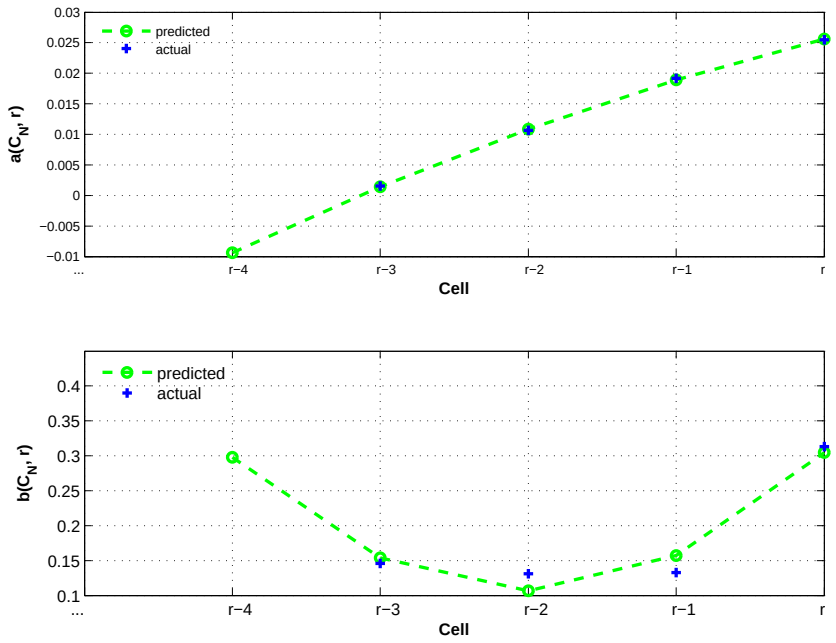
To demonstrate the accuracy of the power loss prediction of each cell in the chain for various MVA capacities, we have performed primary curve fitting (labelled as best fit-I in the Figures 5.46a and 5.48a) which uses the eqn. (5.9) and + values of Figures 5.46b and 5.48b respectively. This is followed by secondary curve fitting (labelled as best fit-II in the Figures 5.46a and 5.48a) which takes into account the predicted new $a(C_N)$ and $b(C_N)$ value of each cell. Both of these power loss curve fits of each cell in the converter are

plotted alongside to demonstrate the precision achieved. This technique for identifying the power loss trend in each cell can be extrapolated to predict power loss trends for any number of additional cells. This is possible if equations (5.10) and (5.11) are generalised according to the total number of cells 'r' as follows:

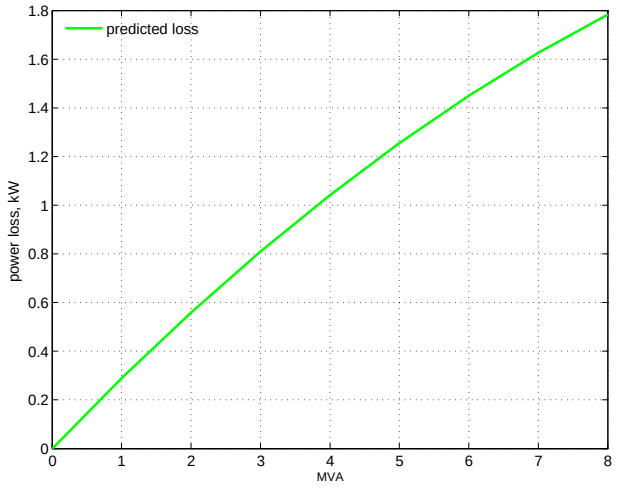
$$a\left(C_N, r\right) = a_1\left(C_N - r + 4\right)^2 + a_2\left(C_N - r + 4\right) + a_3 \tag{5.12}$$

$$b\left(C_N, r\right) = b_1\left(C_N - r + 4\right)^2 + b_2\left(C_N - r + 4\right) + b_3 \tag{5.13}$$

In these equations C_N is still the cell number. However it now takes values from 1 to r and the 4 which appears on the right hand side of the equations is the original number of cells which was used to derive values of a_i's and b_i's. It is obvious that when $r = 4$ we recover eqns. (5.10) and (5.11), while a larger number or r essentially shifts the whole power loss curve to the right by $r - 4$, as compared to the case for which the a_i's and b_i's were identified at $(r = 4)$. With a 3-cell converter as the starting point, for which a_i's and b_i's get identified the right hand side of the equation would include a 3 instead of a 4, and so on. In reality, once additional cells are introduced these are used to improve the resolution of the output waveform by increasing the number of levels while its amplitude remains essentially the same. As such, any extra cell in a ternary sequence contributes 1/3 of the voltage of the lowest voltage cell that existed in the chain prior to the introduction of the new cell. As an example, the parameters of a fifth cell of a hypothetical 5-cell topology designed for 11kV and 33kV systems are shown in Figures 5.47a and 5.49a, and its predicted power loss in Figures 5.47b and 5.49b.

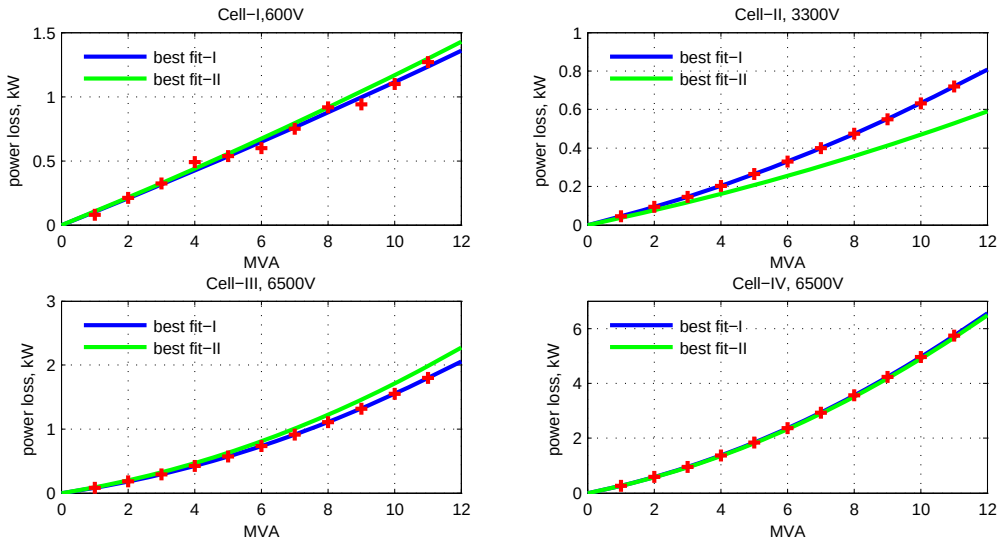


(a)

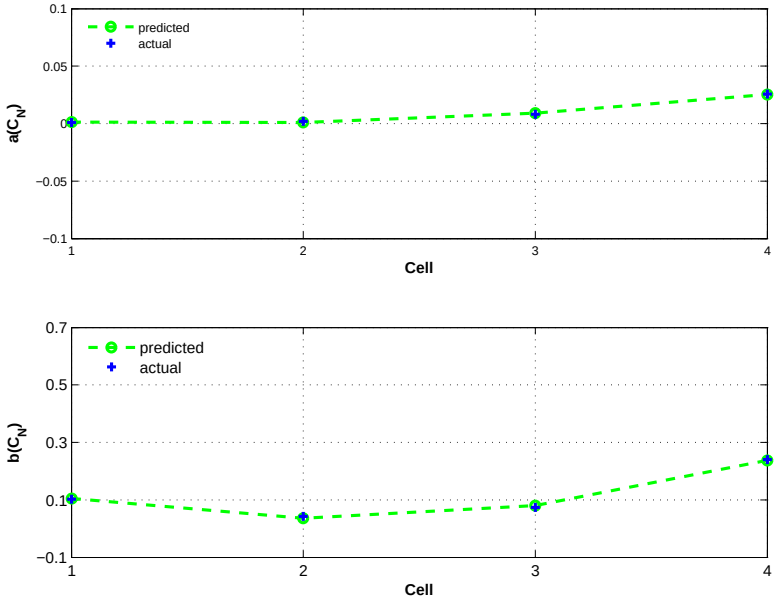


(b)

Figure 5.47: Power conduction loss for a 4-cell topology - 11kV as in Figure 5.46: (a) generalized and extrapolated to 5-cells (b) power loss prediction in fifth cell.

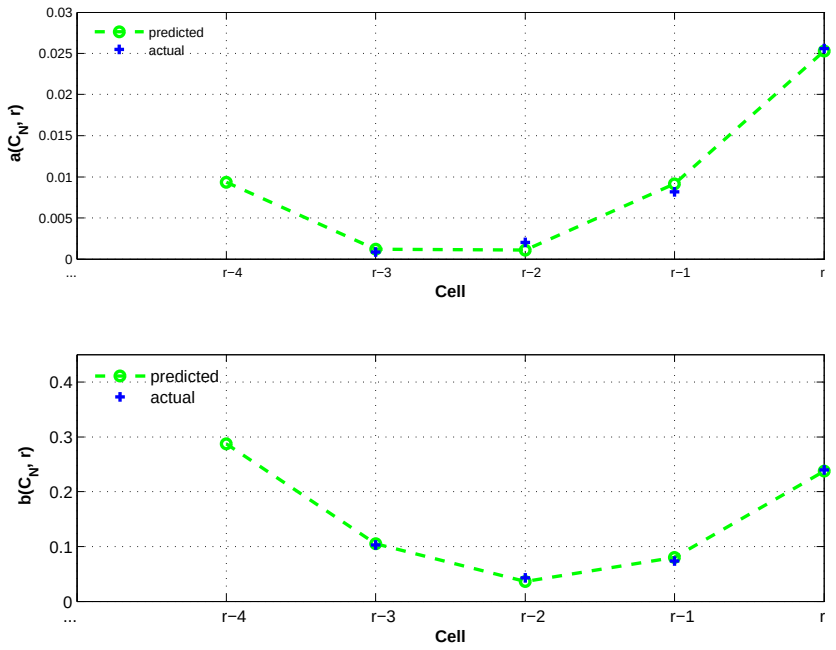


(a)

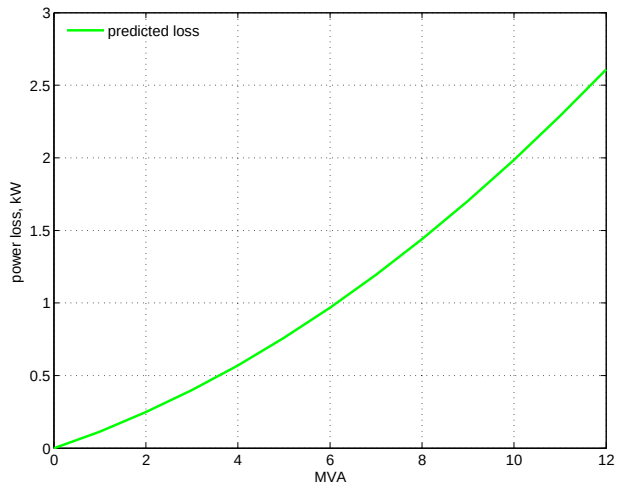


(b)

Figure 5.48: Curve fitting for the power conduction loss for a 4-cell topology - 33kV (a) Best fits of power loss against MVA from Cell I to Cell IV (b) Estimated and predicted coefficients a and b for each cell.



(a)



(b)

Figure 5.49: Power conduction loss for a 4-cell topology - 33kV as in Figure 5.48: (a) generalized and extrapolated to 5-cells (b) power loss prediction in fifth cell.

The same loss prediction method was repeated for all the ternary-sequence converter designs studied in this work and corresponding unique cell 'constants' (a_i's and b_i's) were found to enable prediction of the next a and b values of any additional cell in the chain (refer Table 5.2).

Table 5.2: Calculated values of a_i's and b_i's from eqn. (5.10) and eqn. (5.11) on 11kV and 33kV system for 3-cell and 4-cell ternary topologies built with NPT and PT IGBT device families.

	11kV System						33kV System					
No. of Cells	a_1	a_2	a_3	b_1	b_2	b_3	a_1	a_2	a_3	b_1	b_2	b_3
4-cell NPT-IGBT	-0.0007	0.0115	-0.0094	0.0487	-0.1930	0.2979	0.0041	-0.0122	0.0094	0.0566	-0.2388	0.2872
3-cell NPT-IGBT	-0.0034	0.0235	-0.0141	0.0982	-0.3109	0.3621	0.0056	-0.0107	0.0072	0.0680	-0.1736	0.1484
4-cell PT-IGBT	-0.0010	0.0104	-0.0049	0.0142	-0.0337	0.1660	0.0005	-0.0011	0.0021	0.0622	-0.2529	0.2921
3-cell PT-IGBT	-0.0175	0.0774	-0.0581	0.1063	-0.3920	0.4966	0.0027	-0.0094	0.0099	0.0730	-0.1738	0.1424

5.13 Conclusions

Multi-level cascaded inverter structures can be applied to distribution systems due to their ability to overcome the shortcomings in the ratings of semiconductor devices. Their structure allows them to reach high voltages without the use of transformers. In this chapter, cascaded multi-level converters with both 81 and 27 levels have been evaluated for 11kV and 33kV distribution systems. To examine the performance of cascaded converters, a model for equal-sized and ternary-sequence cascaded converters is developed to calculate the switching and conduction losses in IGBT devices of various ratings when designing various MVA capacity converters. Sixteen designs and a total of 320 individual cases were analysed to calculate power losses and efficiency for various MVA capacities in both 11kV and 33kV systems. It is demonstrated that the ternary sequence converter is superior to the equal-rated converter at 81-levels in 11kV and 33kV systems. But with 27 levels, the equal-rated (as well as ternary sequence) converter is a suitable option for a 33kV system. This analysis holds true for both NPT and PT types of IGBTs.

Overall, PT IGBTs have lower losses than NPT IGBTs in both designs of cascaded converter, with the exception of a few cases (refer summary Table 5.1). The difference in the losses was not as large as might be expected, because the diode in the PT module was different to that in the NPT module. The change in diode losses counter-acted the change in IGBT losses to some extent. It is concluded that the PT (which has lower switching loss) is a better technology for ternary-sequence converters used in distribution networks, because ternary-sequence converters use high switching frequency cells. On the other hand, NPT IGBTs can perform well for equal-rated converter designs due to their better conductivity modulation in this conduction loss dominated topology. Finally, this work suggests that the equal-rated design offers integration of redundancy at lower cost and in a less complicated fashion than the ternary-sequence converter because it requires

only one more equal-rated cell to cover failure of any other cell in the chain.

The last section of the chapter performs empirical validation of the loss findings of the ternary-sequence converter designs. The analytical models developed in eqns. (5.10) and (5.11) were plotted to the data, which fitted well. Cell constants for all the designs canvassed in this study were derived during the process. The model and cell constants were successfully used to predict power loss for an additional cell of a hypothetical converter in a 11kV or 33kV system. These fitted curves and the derived constants can be deployed as an aid to accurately predict power losses where no data is available or it is costly to compile and analyse.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

Power quality problems in distribution systems are not new, but customer awareness of these problems has increased. Conventional solutions such as phase shifter units, AC filters, and capacitor banks have been pursued for some time. However, these conventional solutions use passive design elements and cannot always be tuned as the characteristics of the power system change. An increasingly compelling alternative is to use power electronics to enhance the capabilities of transmission and distribution facilities and optimise their use. During the last decade, the potential presented by VSI-FACTS devices has been demonstrated, but their implementation still poses a major challenge for power electronics engineers and is therefore an active research area.

Multi-level forms of converters have emerged as a realistic industrial option to tackle power quality and reliability issues under the umbrella of FACTS technologies. In distribution systems, this type of power converter offers flexible solutions to many power quality problems. Multi-level converters have been applied in medium and high-voltage systems without the use of transformers because of their ability to overcome individual shortcomings in the rating of solid-state switching devices. The diverse range of multi-level converter topologies, each with their own advantages and disadvantages, can be tailored to a particular application.

Power loss assessment is of great relevance in the converter design process and is directly connected to converter size, capital cost and suitability of application in MV/LV systems. Accurate power loss estimates are vital for proper thermal management to ensure reliable converter operation.

Presently, there is a limited base of knowledge on how to quickly and accurately quantify losses, with methods either requiring time domain simulation (e.g., PLECS or SPICE) or approximate calculations based on limited information on device data-sheets. Time-domain simulation is time consuming, and in both cases results are hard to generalise across devices. The absence of quick, accurate loss quantification techniques is partly due to the complex semiconductor physics involved in calculations, and the range of competing device designs available in the market. It is also due to the separation of disciplines. On the one hand, the power systems community is not very familiar with the operation of semiconductor devices, and on the other hand, the power electronics community is accustomed to treating the device as a 'switch' during converter installation on the network. Therefore, expertise from both fields is required to develop power loss calculation models for multilevel converter typologies, that are both accurate and easy to use at the circuit design level.

The physics of device operation is fundamental for comparing competing power converters with different IGBT device structures. Although IGBTs possess both forward and reverse blocking capabilities, device designers often sacrifice the reverse blocking capability in favour of low forward voltage drop with switching speed. Applying physical principles of device operation, analytical models can be built for scaling power losses for a range of device ratings. These models are applicable to devices that fall within ratings currently available from manufacturers and should be applicable to larger devices.

General analytical relationships for device losses, based on fundamental device physics for MOSFETs, pin diodes and IGBTs, were developed in this work and successfully applied to estimate expected conduction losses for each device type, given any device rating and operating conditions. These analytical models compute power losses in good agreement with manufacturer data, thus establishing their validity. The impact of this physics-based semiconductor device modeling is that it enables circuit designers to quickly estimate power losses and their sensitivity to device ratings when choosing semiconductors for specific applications. Power losses during conduction, switching and reverse recovery processes offers a good estimation of overall converter efficiency.

With a view to inform optimal design criteria for state-of-the-art power MOSFET devices manufactured by industry experts, this work derived an optimal doping $n_D(x)$ profile (refer eqn. (3.38), Subsection 3.4.2) shown to best exploit the device design such that overall on-resistance is minimal without losing blocking performance. The derived doping profile $n_D(x)$ for actual power MOSFETs is shown to fit well with commercial devices

(International Rectifier). It has 33% increased blocking capability for the same drift region length, and reduced on-resistance by 33% for the same blocking capability, as compared to a MOSFET designed with a uniform doping density profile.

This thesis also develops a physics-based overall IGBT model that is capable of predicting exact on-static characteristics of any feasible rating. The governing IGBT design parameters such as ambipolar diffusion length L_a, JFET region length L_{JFET}, *Area* of the device, slope resistance R_{slope} (related to the JFET region resistance) and the thickness of the drift n- region length L_n were individually identified for a range of commercially available IGBTs from the analytical model presented in Subsection 3.5.3 (see summary Table 3.1). Moreover, their functional relationships with blocking voltage and rated current were also furnished in Subsection 3.5.5, to aid in deriving an overall IGBT model. The analysis also exposes the forward voltage drop contribution from distinct regions of an IGBT (junction, drift and JFET) during the forward conduction mode (see Table 3.2), and clearly indicates the regions responsible in forming the 'knee' and 'slope' parts of the I-V curve. The overall model provides a sufficient basis for understanding key IGBT parameters, and is devised to fit as closely as possible to all aspects of the IGBT, as well as to predict conduction power losses.

It is assumed in Chapter 3 that the rate of heat flow out of a device is proportional to area for a given die temperature and ambient temperature. It is shown that the area of majority carrier semiconductor devices (such as a MOSFET) is proportional to the product of the rated current and square root of the blocking voltage. In other words:

- The conduction power loss (at rated current) increases linearly in relation to the variable rated current when blocking voltage is fixed.
- The conduction power loss (at constant current) increases as a square root of the variable blocking voltage when rated current is fixed.

The constants of proportionality for the developed scaling laws can be derived from curve fits to manufacturer data sheets.

In minority carrier semiconductor devices (such as a *pin* diode or IGBT), a similar relationship is observed for variation of current (where the blocking voltage is fixed). But where the blocking voltage varies (and the rated current is fixed), the power losses vary as a square root with an offset (from the origin). This is due to the additional junction voltage drop. Also the slope resistance of the device is inversely proportional to the varying rated current.

The key features of these scaling constants include the following:

- They facilitate computation of power losses for any rating of a given device family including extrapolation of device characteristics beyond a manufacturer's given data.
- Their use minimises the need for detailed knowledge and interpretation of a manufacturer's data for appropriate device selection in circuit design.
- They indicate the rating range over which each device is a good choice, e.g. the MOSFET is preferred at low voltage/current, whereas the IGBT is preferred at high voltage/current.
- They allow a circuit designer to compute losses quickly, and without considering details of the device physics or searching for device datasheets - a potential increase in circuit efficiency by over-rating the device.

Analysis of the cascaded cell converters has revealed that equal-rated and ternary-sequence dc voltage to each cell in the chain are two attractive structures for achieving multiple voltage levels. The equal-rated design offers integration of redundancy at lower cost and in a less complicated fashion than the ternary-sequence converter because it requires only one more equal-rated cell to cover failure of any other cell in the chain. It is demonstrated that the ternary-sequence converter is superior to the equal rated converter at 81 levels in both 11kV and 33kV systems. However at 27 levels, the equal-rated converter is also a suitable option for a 33kV system. This analysis holds true for both NPT and PT types of IGBTs. Overall, PT IGBTs have less losses for both designs of cascaded converter, with the exception of a few cases. Finally, this work suggest that the equal-rated design offers integration of redundancy at lower cost and in a less complicated fashion than the ternary-sequence converter because it requires only one more equal-rated cell to cover failure of any other cell in the chain.

Empirical validation of this cascaded converter loss model was successfully performed through curve fitting techniques. The estimated curve-fits for a range of converter designs were used to generate unique 'constants' for each cell in the chain. Power losses can also be predicted for any additional cell in the chain. This is directly relevant to future designs.

6.2 Author's Contributions

The novelty and original contribution of the work presented in this thesis is the development of general analytical tools to scale power losses in high power semiconductor devices at various ratings, and evaluate the performance of cascaded converters in distribution systems. The author's specific contributions in this work can be summarised as follows:

1. Development of an overall IGBT model that predicts exact on-state characteristics and key design parameters. This thesis constructs an overall physics-based IGBT on-state model which exposes the voltage drop contributions of a device's discrete regions. The contribution was to move beyond analysis of physical operation and predict exact forward conduction characteristics of IGBT device designs built by manufacturers. Unknown governing optimal device design parameters were identified, and their functional relationships with device rated voltage and current revealed. Thus additional insight into general design rules adopted by the industry are provided. The built model predicts the manufacturer I-V measurements accurately throughout the range. Interpolation and extrapolation to any rating, which is a highly desirable feature, is also possible.

2. Formulation of scaling laws to quantify conduction losses. Formulae based on device physics have been derived, offering closed form solutions for device conduction loss calculation based on device ratings and operating conditions. These physics-based simplified analytical models allow a circuit designer to quickly estimate circuit losses and their sensitivity to device ratings when choosing semiconductors for specific applications. This will directly impact the size, weight, cost, performance, and market success of FACTS technology, and will in turn support the commercialisation of modern power converters under development.

3. Derivation of power loss scaling constants for minority and majority carrier devices. The author has derived power loss scaling constants from analytical relationships developed for both majority and minority carrier devices, and successfully validated them against data sheets from leading manufacturers. These numbers enable easy computation of device power loss, offering a simple conceptual window into their performance under various conditions of use. This enables the construction of power loss charts in the future (for a given device family) without the need for detailed knowledge and understanding of the vast majority of competing devices available in the market. This will also greatly ease the selection process of devices deployed on power networks.

4. Comparison of cascaded converter topologies for high power applications. Cascaded multi-level power converter topologies were identified and then examined in detail in order to assess their limitations and potential for resilience. With a medium-voltage reactive power application in mind, potential cascaded converter designs are compared objectively with all other types of multilevel converters in terms of their overall component count, modularity, ease of control and industrial application. This work explains why cascaded multi-level converters are particularly useful designs for medium voltage applications. This has a number of practical consequences.

5. Development of cascaded cell converter model. A cascaded cell converter simulation model has been developed using the PLECS/SIMULINK program to evaluate the candidate converter topologies on the basis of power losses in distribution systems. The time domain simulation model has the flexibility to be modified for any number of cells in the chain, thus providing a simulation platform to evaluate various scenarios. It can synthesise any required output voltage level, MVA load capacity, P.F, and device selection, without overcomplicated computational requirements (mimicking complex network characteristics, or using sophisticated control modulation strategies). For a circuit designer, an easy to use, compact and accurate enough model for performing loss evaluation of cascaded cell devices is now available for converter design in power network applications.

6. Predictability of power losses in cascaded converters. A loss evaluation of both equal-rated and ternary-sequence cascaded converters has been performed, and curve fitting techniques applied to empirically validate the cascaded converter loss model. The author has developed the concept of predicting losses accurately with the help of cell 'constants'. The curves fitted for a range of converter designs have been used to generate constants calculated for each cell in the chain during the validation process. These constants can predict losses for any additional cell added to the chain in future converter designs intended for use in distribution systems. This avoids the need for time consuming simulation, and speeds up the design process.

6.3 Further Work Suggestions

There are a number of research directions that stem from the work described in this thesis. These future areas of research are recommended below:

This thesis has stressed the importance of having the analytic models that enable circuit designers to calculate power losses for high power semiconductor devices as a function of device rated voltage and current and operating voltage and current. Conduction loss models of three device types (MOSFET, IGBT and *pin* diode)ave been developed. As the power converter topologies investigated in this thesis are mainly conduction loss dominated, these formulae provide information on the bulk of the losses. To improve the accuracy of these models and be able to apply the formulae to converter topologies with a higher fraction of switching losses, analytical expressions for switching losses must also be developed. This was explored during this work but not all issues have been resolved (not produced here). The input capacitance, gate resistance, di/dt and dv/dt capability of the device are all factors. Insight into the detail of how and why some parameters scale as a function of device rating, will emerge from discussions with device manufacturers.

The thesis also built models that quantify and extrapolate power losses in cascade type converters of various topologies. A further area of future research might involve investigation of losses with variations in the operating conditions, semiconductor components or structure of these and other converters. Power losses could be evaluated and compared for a broader spectrum of power factor cases, other converter topologies, or even topologies that involve combinations of devices from different families, such as PT, NPT and GTO.

The models developed might be further improved by including a correction factor to allow calculation of losses as a function of operating temperature. This may be especially important as the industry moves towards devices which are capable of operating over a wide temperature range, such as Silicon Carbide.

The work reported uses simple stair case modulation strategy to generate the converter output waveform, notwithstanding its limitations. Loss evaluation applying different modulation schemes, such as SVM space vector modulation or Sinusoidal PWM modulation, could also be investigated to observe loss assessment variations.

Whilst the formulae developed have been verified against simulations/modelling and manufacturer data, it would be beneficial, especially for formulae developed for power

losses in converters, to experimentally verify losses, probably using a scaled-down converter model. Bridging the gap of experimentation also has the potential to reinforce the value of built mathematical tools with a wider audience, including network operators and circuit designers.

6.4 Publications Arising from this Work

Journals

- M. A. Rehman-Shaikh, P. D. Mitcheson and T. C. Green, *Scaling of Losses with Device Rating in Power Semiconductor Devices*, International Journal of Electronics, to be submitted.
- M. A. Rehman-Shaikh, P. D. Mitcheson and T. C. Green, *Determining Scaling Laws for Sizing Switches in Multi-level Converters*, IEEE Transactions on Power Electronics, to be submitted.

Conferences

- M. A. Rehman-Shaikh, P. D. Mitcheson and T. C. Green, *Power Loss Minimization in Cascaded Multi-Level Converters for Distribution Networks*, 33rd Annual Conference of the IEEE in Industrial Electronics Society, 2007. IECON 2007. pp. 1774-1779.
- M. A. Rehman-Shaikh, P. D. Mitcheson and T. C. Green, *Efficiency Maximisation of Multilevel Converters in Active Distribution Networks*, IEEE General Meeting in Power Engineering Society, 2007.
- M. A. Rehman-Shaikh and T. C. Green, *Technology Comparison for Cascaded Multilevel Converters in Distribution Networks*, The 3rd IET International Conference in Power Electronics, Machines and Drives, 2006, pp. 571-575.
- M. A. Rehman-Shaikh, et al, *Interface Technologies for Distributed Power Generation*, Best Poster Prize, launch of Energy Futures Lab, Imperial College London, Nov 2005.

Appendix A

Switching Charts

27Vdc	9Vdc	3Vdc	1Vdc	Level
1	1	1	1	40
1	1	1	0	39
1	1	1	-1	38
1	1	0	1	37
1	1	0	0	36
1	1	0	-1	35
1	1	-1	1	34
1	1	-1	0	33
1	1	-1	-1	32
1	0	1	1	31
1	0	1	0	30
1	0	1	-1	29
1	0	0	1	28
1	0	0	0	27
1	0	0	-1	26
1	0	-1	1	25
1	0	-1	0	24
1	0	-1	-1	23
1	-1	1	1	22
1	-1	1	0	21
1	-1	1	-1	20
1	-1	0	1	19
1	-1	0	0	18
1	-1	0	-1	17
1	-1	-1	1	16
1	-1	-1	0	15
1	-1	-1	-1	14
0	1	1	1	13
0	1	1	0	12
0	1	1	-1	11
0	1	0	1	10
0	1	0	0	9
0	1	0	-1	8
0	1	-1	1	7
0	1	-1	0	6
0	1	-1	-1	5
0	0	1	1	4
0	0	1	0	3
0	0	1	-1	2
0	0	0	1	1
0	0	0	0	0
0	0	0	-1	-1
0	0	-1	1	-2
0	0	-1	0	-3
0	0	-1	-1	-4
0	-1	1	1	-5
0	-1	1	0	-6
0	-1	1	-1	-7
0	-1	0	1	-8
0	-1	0	0	-9
0	-1	0	-1	-10
0	-1	-1	1	-11
0	-1	-1	0	-12
0	-1	-1	-1	-13
-1	1	1	1	-14
-1	1	1	0	-15
-1	1	1	-1	-16
-1	1	0	1	-17
-1	1	0	0	-18
-1	1	0	-1	-19
-1	1	-1	1	-20
-1	1	-1	0	-21
-1	1	-1	-1	-22
-1	0	1	1	-23
-1	0	1	0	-24
-1	0	1	-1	-25
-1	0	0	1	-26
-1	0	0	0	-27
-1	0	0	-1	-28
-1	0	-1	1	-29
-1	0	-1	0	-30
-1	0	-1	-1	-31
-1	-1	1	1	-32
-1	-1	1	0	-33
-1	-1	1	-1	-34
-1	-1	0	1	-35
-1	-1	0	0	-36
-1	-1	0	-1	-37
-1	-1	-1	1	-38
-1	-1	-1	0	-39
-1	-1	-1	-1	-40

Table A.1: 81 voltage levels and their cell states for ternary-sequence converter

	Cell No																																												
Level	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
-40	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
-39	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0
-38	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0
-37	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0
-36	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0
-35	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0
-34	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0
-34	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0
-33	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0
-32	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0
-31	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0
-30	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0
-29	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0
-29	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0
-28	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0
-27	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0
-26	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-25	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-24	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-23	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-22	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-21	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-20	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-19	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-18	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-17	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-16	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-15	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-14	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-13	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-12	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-11	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-10	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-9	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-8	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-7	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-6	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-5	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-4	-1	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-3	-1	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-2	-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
27	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
28	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
29	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
30	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
31	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
32	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
33	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
34	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
35	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
36	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
37	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
38	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
39	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
40	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table A.2: 81 level cell switching states for equal-sized converter (40-cell)

Level	Cell		
	9Vdc	3Vdc	Vdc
-13	-1	-1	-1
-12	-1	-1	0
-11	-1	-1	1
-10	-1	0	-1
-9	-1	0	0
-8	-1	0	1
-7	-1	1	-1
-6	-1	1	0
-5	-1	1	1
-4	0	-1	-1
-3	0	-1	0
-2	0	-1	1
-1	0	0	-1
0	0	0	0
1	0	0	1
2	0	1	-1
3	0	1	0
4	0	1	1
5	1	-1	-1
6	1	-1	0
7	1	-1	1
8	1	0	-1
9	1	0	0
10	1	0	1
11	1	1	-1
12	1	1	0
13	1	1	1

Table A.3: 27 Voltage Levels and their cell states for ternary-sequence converter

Level	Cell No												
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**
-13	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
-12	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0
-11	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0
-10	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0
-9	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0
-8	-1	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0
-7	-1	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0
-6	-1	-1	-1	-1	-1	-1	0	0	0	0	0	0	0
-5	-1	-1	-1	-1	-1	0	0	0	0	0	0	0	0
-4	-1	-1	-1	-1	0	0	0	0	0	0	0	0	0
-3	-1	-1	-1	0	0	0	0	0	0	0	0	0	0
-2	-1	-1	0	0	0	0	0	0	0	0	0	0	0
-1	-1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0	0	0	0	0	0
4	1	1	1	1	0	0	0	0	0	0	0	0	0
5	1	1	1	1	1	0	0	0	0	0	0	0	0
6	1	1	1	1	1	1	0	0	0	0	0	0	0
7	1	1	1	1	1	1	1	0	0	0	0	0	0
8	1	1	1	1	1	1	1	1	0	0	0	0	0
9	1	1	1	1	1	1	1	1	1	0	0	0	0
10	1	1	1	1	1	1	1	1	1	1	0	0	0
11	1	1	1	1	1	1	1	1	1	1	1	0	0
12	1	1	1	1	1	1	1	1	1	1	1	1	0
13	1	1	1	1	1	1	1	1	1	1	1	1	1

Table A.4: 27 voltage levels and their cell states for equal-sized converter

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