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Design and Implementation of a Sliding-Mode Controller for Digital Low-Dropout/Linear Regulators

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***Abstract*— This paper presents an approach to utilize of sliding-mode (SM) controller in digital low-dropout/linear regulators. Various design aspects, including the extraction of the regulator state-space model and sliding coefficients by considering the hitting, existence, and stability conditions are described. Moreover, the freeze control block is introduced as a solution to compensate the high frequency chattering phenomenon of SM, resulting in reduction of switching losses. In order to verify the statements, a quasi digital low-dropout/linear regulator (QDLDO) is implemented in a discrete form on a PCB. The circuit consists of the proposed current-mode current feedback amplifier (CFA)-based SM controller and switched-mode PMOS array driven by a bidirectional serial shift register, which is controlled by the SM controller. The results reveal that the controller detects the load changes rapidly, and eliminates the output limit-cycle oscillation, providing a robust and stable output voltage.**

***Index Terms*— current-mode, digital LDO, linear regulator, Low-dropout, nonlinear control, sliding-mode.**

I. Introduction

POWER supply management is a critical issue for portable electronic devices to increase the battery life and provide stable supply voltages during fast varying load currents. Power supply circuits can generally be categorized as linear and switching regulators. Linear regulators are widely used in analog, mixed-mode, and RF applications. They provide several advantages with respect to the switching regulators in terms of lower output ripple, more integrability with minimal external passive components, higher accuracy, faster transient response, and lower noise [1, 2]. Low-dropout (LDO) regulators are more efficient in comparison to their conventional linear counterparts due to the lower difference between their input and output voltages. As it is shown in Fig. 1, LDO regulators may either be analog-LDO (ALDO) or digital-LDO (DLDO). Although DLDO structure is similar to ALDO, it consists of a clock-based comparator instead of the error amplifier (EA) to monitor the output voltage, V_{out}, and compare it with the reference voltage, V_{ref}. Moreover, in this structure, the shift register/digital controller generates the required digital code to drive the PMOS array [3, 4].

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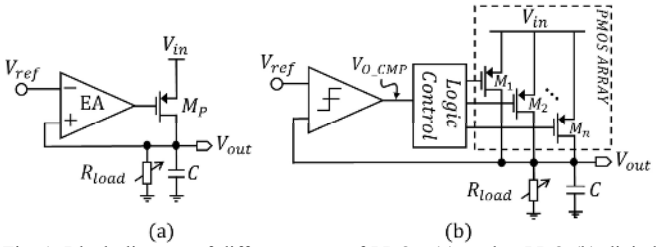

Fig. 1. Block diagram of different types of LDOs, (a) analog LDO (b) digital LDO.

The conventional control methods utilized in LDOs are based on classical techniques of linear feedback control [5]. These methods impose them to be linear around a reference voltage, while dynamic governing equations that model the LDO equivalent behavior are nonlinear during large dynamic varying load currents, which are challenging for the linear control methods [6]. This aspect justifies the lack of a method for modeling and controlling these kinds of systems. On the other hand, the modern control theories like sliding-mode (SM) control, fuzzy control, adaptive control, and etc., have been utilized to control the nonlinear systems. Among them, SM controller has been studied and represented to be a highly promising solution for nonlinear systems and is widely used in DC/DC converters [7, 8], because of its capability to improve the dynamic performance, being robustness against parameter variations, while requiring no complex processing [9]. As a result, it is feasible to apply the SM control technique on the LDOs. DLDO can be a good candidate for this purpose due to the fact that the signals in its control loop are propagated during the clock cycle. However, it suffers from some drawbacks like limit-cycle oscillation as well as current dependent output ripples [10].

This paper indicates how a sliding-mode controller can be applied to a LDO/linear regulator and presents a discrete form implementation of a SM control-based quasi digital LDO (QDLDO). The rest of the paper is as follows; section II presents the description of the proposed SM controller for the LDO. Discrete implementation of the proposed regulator based on the SM controller is presented in section III. The results are presented in section IV followed by the conclusion in section V.

II. The Proposed Sliding-Mode Controller for LDO

A. System Description

Fig. 2 shows the schematic of the proposed QDLDO based on the SM controller [11]. It consists of a PMOS array, bi-directional shift register, on-chip output capacitor, C, SM control block, and clock freeze block. R_L represents the output

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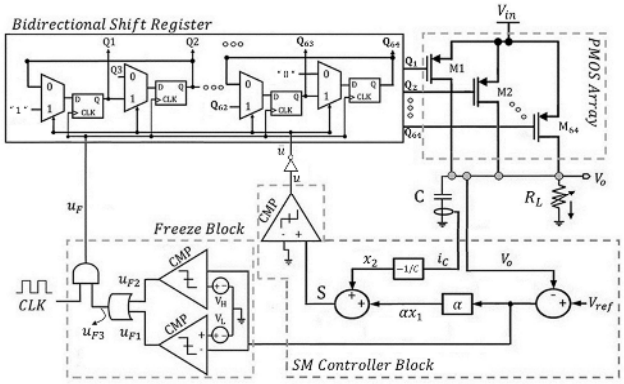

Fig. 2. Proposed QDLDO regulator based on the SM controller.

load. The sliding switching surface, S, is created based on the output voltage error, x_1, and its derivative, x_2, obtained from the output capacitor current, i_C, in the SM control loop. It is noted that the reference voltage is considered constant. The control signal u, created via the hysteresis thresholding, is fed to the bi-directional shift register (its complementary signal, $\bar{u}$, is used) to generate the required digital thermo-code for driving the PMOS array. The signals u_{F1}, u_{F2}, and u_{F3} of the freeze block develop u_F for enabling/disabling the external clock of the shift register. In this way, the shift register produces the digital thermo-code or holds its previous value. The state-space model of the SM control for the QDLDO is expressed as below:

$$\begin{aligned} x_1 &= V_{ref} - V_o \\ x_2 = \dot{x}_1 &= -\frac{dV_o}{dt} = -\frac{1}{C} i_C = \frac{1}{C}\left(\frac{V_o}{R_L} - NI_P\right) \\ \dot{x}_2 &= \frac{1}{R_L C}\frac{dV_o}{dt} - \frac{I_P}{C}\frac{dN}{dt} = -\frac{1}{R_L C} x_2 - \frac{I_P}{C} u \end{aligned} \tag{1}$$

where N and u are the number of PMOS transistors turned on/off and the rate of changes in the number of turned on/off PMOS transistors, respectively. Thus, the state-space model can be achieved as below:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = Ax + Bu = \begin{bmatrix} 0 & 1 \\ 0 & -\frac{1}{R_L C} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{I_P}{C} \end{bmatrix} u \tag{2}$$

The SM control signal, u, specifies the shifting state of the N-bit shift register, which acts as an integrator, and can be 0 or 1. u=1/0 allows the serial shift register to turn on/off the PMOS array through its complementary signal, $\bar{u}$ (Fig. 3).

B. Sliding-Mode Control Design Criteria

The sliding-mode control allows an n-th order problem to be replaced by an equivalent first order one. For doing that, a control law is designed to lead the state trajectories to a sliding surface in finite time which then the desired trajectories can meet asymptotically. The entire sliding-mode control is separated into two phases: reaching and sliding phases. These two phases are feasible through the three conditions: hitting, existence, and stability conditions [9].

Fig. 4 indicates the graphical behavior of the trajectories at any arbitrary locations. In the open-loop system without the sliding control loop, the phase trajectory will converge to the

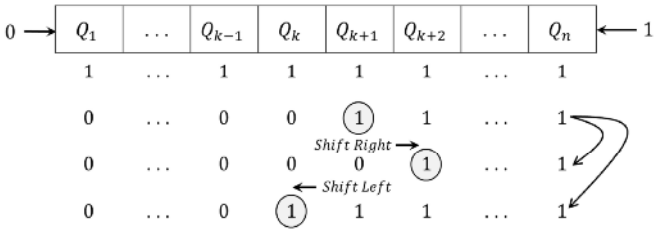

Fig. 3. Operation of the bi-directional shift register.

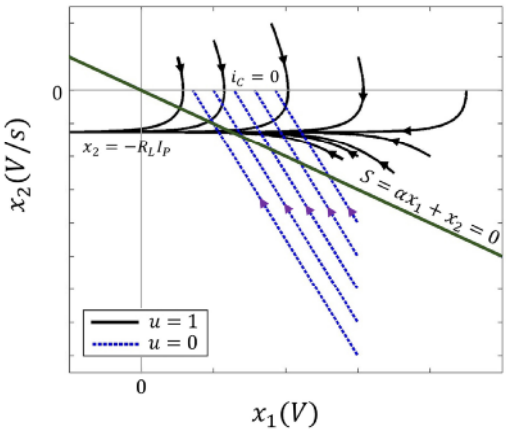

Fig. 4. Phase plane of the substructure corresponding to both u=1 and u=0 for different starting positions (x_1, x_2).

$$S = \alpha x_1 + x_2 = \alpha(V_{ref} - V_o) - \frac{1}{C} i_C \tag{3}$$

lines of x_2=-$R_L I_P$ and x_2=0 with u=1 and u=0, respectively, for any arbitrary starting position. On the other hand, by applying the sliding control loop to the system, the controller employs the sliding surface to determine the state of the control signal u. In this work, the sliding surface, S, is composed of the control parameters x_1 and x_2, as given by (3), in which α is the sliding coefficient. Indeed, these parameters determine the state of the control signal u through the sliding surface. By enforcing S=0, the sliding line with gradient α is obtained separating the phase plane into two regions, each of them are specified by the state of the control signal u. The specified control signals direct the phase trajectories at any arbitrary location toward the sliding line. In this regard, u=1 should be applied when the phase trajectories are at any position above the sliding line. On the other hand, if the phase trajectories are at any position below the sliding line, then u=0 must be employed so that the trajectory is directed toward the sliding line. According to this behavior, the hitting condition of the proposed system will become satisfying when the switching function is considered as below:

$$u = \frac{1}{2}(1 + sign(S)) \rightarrow \begin{cases} u = 1 & 'On' \quad S > 0 \\ u = 0 & 'Off' \quad S < 0 \end{cases} \tag{4}$$

The existence condition which guarantees the state trajectories reach the sliding surface in finite time and remains on it thereafter is derived via the Lyapunov's direct method as follows:

$$\dot{V} = \lim_{S \to 0} S\dot{S} < 0 \tag{5}$$

By combining (2), (3), and (4), the following result can be obtained as (6):

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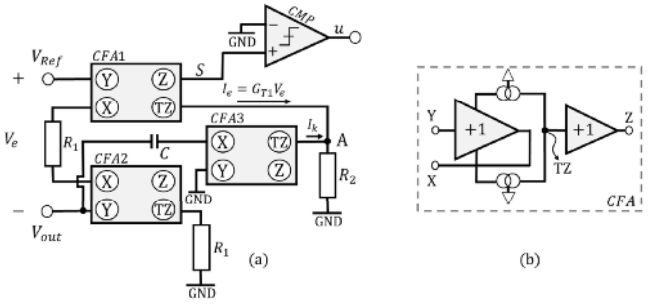

Fig. 5. (a) Proposed analog implementation of SM controller block based on CFA, (b) equivalent block for the CFA.

$$S\dot{S} = S(J^T Ax + \frac{1}{2}J^T B) + \frac{1}{2}J^T B|S| \tag{6}$$

where $J^T = [\alpha \ 1]$. Thus, the following existence condition will be achieved:

$$\begin{cases} -(\alpha - \frac{1}{R_L C})i_C < I_p & u = 1 \\ -(\alpha - \frac{1}{R_L C})i_C > 0 & u = 0 \end{cases} \tag{7}$$

Considering the capacitor charging/discharging behavior, i_C can be positive/negative, respectively. When u=0/1, the capacitor will be discharging/charging, and hence, i_C will be negative/positive. As a result, the condition given by (7) only depends on α for different output loads, which must be greater than $1/R_{L,min}C$ (the worst case) to convince the existence condition. It also guarantees the stability condition of the system according to Routh-Horwitz stability criterion and (3), which needs a positive value for α. On the other hand, by considering (3) equal to zero, the following result is achieved:

$$x_1(t) = Be^{-\alpha t} \rightarrow \tau = \frac{1}{\alpha} \tag{8}$$

where B and τ are a positive coefficient and time constant, respectively. Therefore, the dynamic response of the controller is also affected by α and the mentioned restriction on it ensures both the fast dynamic response with maximum time constant of $\tau_{max}=R_{L,min}C$ as well as existence condition.

The boundary layer via hysteresis thresholding is usually used to limit the high-frequency chattering phenomenon in the sliding-mode control. The freeze block is applied here to enable/disable the clock of the shift register by comparing the output voltage error with the high/low boundary condition of V_H/V_L. The clock will be disabled when $V_L < x_1 < V_H$. It means that the clock is enabled during the transient event while it is disabled in the steady-state when the output voltage reaches its desired value with an acceptable tolerance.

III. Discrete Implementation of the Regulator Based on the SM Controller

Sliding-mode control is an instantaneous control technique with multiple inputs and its implementation does not require an excessive and complex process. However, there are few existing analog and digital implementations of SM controllers. Digital implementations by means of microcontrollers are useful for low operating frequencies [12]. On the other hand, analog implementations of SM controllers are based on classical voltage-mode circuits, which results in severe bandwidth limitations [13]. In this work, current-mode circuit techniques based on current conveyors are considered to realize the SM controller. It is well known that utilizing currents as information-carrying signals reduce the impact of parasitic capacitances, corresponding to an increment in the maximum operating speed of the circuits. Indeed, current-mode circuits have a local open-loop high-bandwidth processing and the capability of directly implementing signal aggregations by virtue of Kirchoff's current law [8].

According to (3), α and -1/C are the coefficients of the state variables (V_{ref} - V_o) and i_C of the sliding surface. However, since the amount of the capacitor, C, used in this work is in the range of picofarad, its inverse term will be too high, making the coefficients out of range for practical implementation. Therefore, by applying an attenuation factor, the sliding surface can be modified as (9):

$$S = \beta\left[\alpha(V_{ref} - V_{out}) - \frac{1}{C}i_C\right] \tag{9}$$

where β is assumed as an attenuation factor. Thus, a practical form of implementation for the sliding surface is acquired. It should be noted that, in spite of this modification the existence condition will stay unchanged.

Fig. 5 (a) shows the analog implementation of the SM controller based on the current feedback amplifiers (CFAs). The CFA operation is based on both voltage copying (between high-impedance node Y and low impedance node X) and current copying (between node X and high-impedance node TZ, which is buffered at node Z), in an open-loop manner, as shown in Fig. 5 (b). The proposed implementation allows modular operation by a simple connection at node A, where the linear combination of the output voltage error and its derivative is produced, defining the switching surface represented in (9). As it is shown in Fig. 5 (a), CFA1 and CFA2 make a differential input transconductor with a high transconductance of G_{T1}=1/R_1 to convert the error voltage, V_e, to its equivalent current I_e. In addition, the derivative of the output voltage error is created by CFA3 and the capacitor, C in a current form of I_K. Finally, the linear summation of the produced current signals makes V_A via the resistor R_2, representing the switching surface, as below:

$$V_A = R_2(I_e + I_K) = R_2(G_{T1}V_e - C\frac{dV_O}{dt}) \tag{10}$$

So,

$$S = \frac{R_2}{R_1}(V_{ref} - V_{out}) - R_2 i_C \tag{11}$$

Equilibrating the equations (9) and (11), the attenuation factor and sliding coefficient can be obtained as β=R_2C and α=1/R_1C, respectively. Moreover, by assuming R_1<$R_{L,min}$, the restrictions on α will be satisfied. It is noted that the SM control signal, u, is achieved via a fast comparator with internal hysteresis to satisfy (4).

IV. Discrete Implementation and Experimental Results

In order to validate the statements, the proposed regulator based on the SM controller is implemented in a discrete form on a PCB. Fig. 6 shows the full schematic diagram of the pro-

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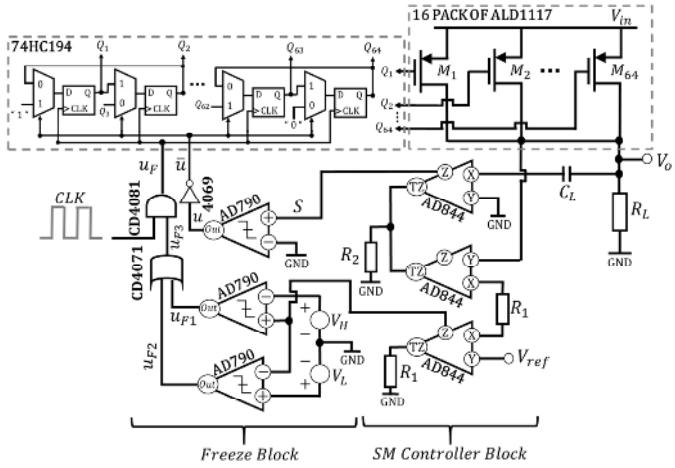

Fig. 6. The complete schematic diagram of the proposed regulator based on the sliding-mode controller.

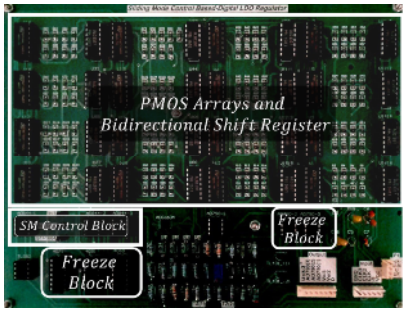

Fig. 7. The implemented PCB of the proposed regulator based on the SM controller.

posed SM controller-based regulator implemented by the CFA ICs of AD844. The PMOS array transistors must be matched to provide same currents. Due to some restrictions in providing the devices, 16 ICs of ALD1117, each of them consists of monolithic quad matched PMOS transistors with the threshold voltage of 0.7 V, are utilized as PMOS array. However, according to the data-sheet, ALD1117 needs a 2.5 V drain-source voltage to provide sufficient current. As a result, by considering a 5 V input voltage, the reference and output voltages of the regulator are set to 2.5 V, which does not fall into the low-dropout category. However, it should be noticed that the proposed SM controller can be used in low-dropout regulators in case of providing a suitable PMOS array with low drain-source voltage while sourcing sufficient current. The proposed regulator based on the SM controller is designed and implemented for the load current of 0.35-22.4 mA (each power transistor can source 0.35 mA current to the load with a dropout voltage of 2.5 V). Moreover, the output capacitor can be changed from 4 to 80 pF.

The implemented PCB of the proposed regulator based on the SM controller is illustrated in Fig. 7 which is composed of power transistors, 64-bit bi-directional shift register, SM controller block, and freeze block. The test setup for the measurement of the load transient response and output waveforms is indicated in Fig. 8. The external reference clock of 1 MHz is provided by AFG2125-3202, GW Instek function/arbitrary waveform generator and Tektronix TDS2024B oscilloscope is used to check the functionality of the proposed control loop. The transient load current is provided by a variable resistor R_H in parallel with a series

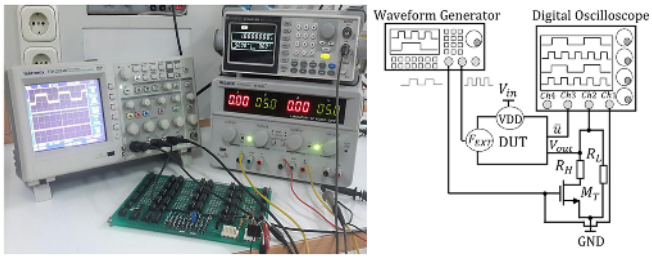

Fig. 8. (a) Lab measurement components, and (b) measurement setup.

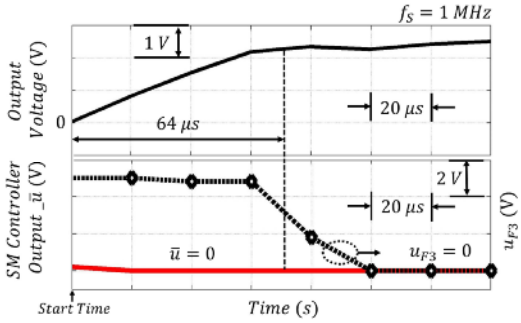

Fig. 9. Start-up response of the proposed regulator based on the SM controller.

combination of a commercial NMOS power transistor of IRF530, as a switch, and a variable resistor R_L. The resistors R_H and R_L are used to control the heavy/light load conditions during the transient response.

Fig. 9 shows the start-up results of the proposed regulator based on the SM controller with 1 MHz clock frequency for the maximum load current of 22.4 mA. As it can be seen, when the supply voltage is applied to the regulator (start time), the output voltage has reached its desired value during 64 µs, because of the clock frequency of 1 MHz (turning on the 64 PMOS transistors via the 64-bit bidirectional shift register). However, it is possible to reduce this settling time by increasing the clock frequency or using a better shift register like barrel shifter instead of a serial one. Indeed, the SM control loop can detect the load changes instantaneously when the supply is powered on. As a result, it is fast enough, and the delay is due to the shift register operation. Furthermore, since the freeze control block is employed, the clock of the shifter will be disabled when the output voltage reaches its desired value and the SM control signal, u ($\bar{u}$), holds its last value, meaning that the steady-state output voltage has no ripple.

Figs. 10 (a) and (b) show the load transient responses of the proposed SM controller-based regulator to different steps of the load current changes with rise and fall times of 400 ns. As it is obvious, when the load current changes between 11.2 mA (the current delivered by 32 power transistors) and 22.4 mA (the current provided by 64 power transistors) instantaneously, it takes 36 µs, to turn on or off the power transistors via the serial shifter driven by the SM control signal $\bar{u}$ (Fig. 10 (a)). As a result, after this duration, the output voltage is recovered to its previous (desired) value. In the case that the load current changes between 5.6 mA (provided by 16 power transistors) and 7 mA (delivered by 20 power transistors), the required time for settling the output voltage back to its desired value is 4 µs (Fig. 10 (b)). However, as it is obvious from Figs. 10 (a) and (b), the SM control signal $\bar{u}$ is fast enough to react against the load

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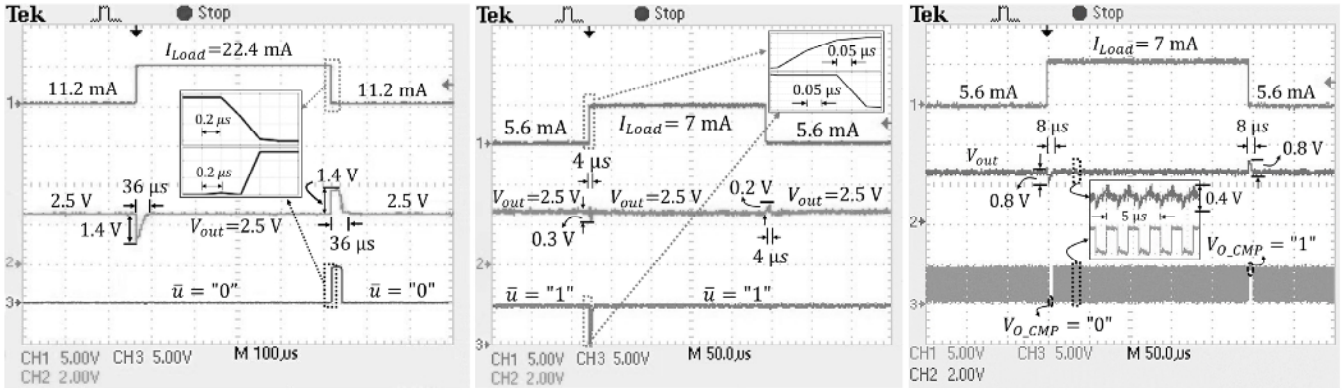

(a) (b) (c)

Fig. 10. Transient response of the proposed regulator based on the SM controller at 1 MHz clock frequency when the current changes from (a) 11.2 mA to 22.4 mA, (b) 5.6 mA to 7 mA, and (c) transient response of the regulator based on the conventional linear control (Fig.2 (b)).

changes, taking just 200 ns to detect the load events. As a result, the obtained settling time is due to the utilized serial shift register with its given clock frequency. Increasing the clock frequency or using a better shifter like barrel shifter will result in a better transient performance. It is noted that in all cases, the output voltage is stable without any oscillation. Moreover, it has no ripple in the steady-state due to the utilized freeze control block, which disables the clock of the shifter and makes the SM control signal $\bar{u}$ to hold its last value. This is the case that the initial values of $\bar{u}$ in Figs. 10 (a) and (b) are different. Indeed, the signal $\bar{u}$ is just used during the load event when the clock is enabled, while after activating the freeze signal, it is not usable.

In order to compare the performance of the proposed SM controller with the conventional linear one, a simple DLDO, (Fig. 2 (b)), based on the linear control is adopted here and its transient characteristic under the same load changes is evaluated. It consists of a fast linear comparator (AD790) with a latched output working at 1 MHz clock frequency to generate V_{O_CMP}, instead of the SM control. In addition, the utilized bi-directional shift register drived by the comparator as well as the power arrays are similar to their SM control-based LDO. Fig. 10 (c) shows the transient response of the linear control-based regulator as the load current changes between 5.6 and 7 mA. Accordingly, not only the output voltage deviation is more than that of the SM control-based LDO, the required time for settling the output voltage back to its desired value is twice of the SM control-based result (8 µs), which indicates the advantage of the SM control. Moreover, the steady-state limit-cycle oscillation is appeared at the comparator and DLDO outputs.

V. Conclusion

This paper presents a QDLDO/linear regulator based on the SM controller in which the output voltage error and its derivate are considered as the SM controller input and the generated control signals drive the power transistors via a shift register. The state-space model of the proposed regulator based on the SM controller and its sliding coefficients are extracted by considering the hitting, existence, and stability conditions. Furthermore, the chattering phenomenon is compensated by enabling the clock signal in the transient and disabling it in the steady-state condition through the freeze control signal. The results obtained from implementing the regulator based on the SM controller reveal that the controller detects the load changes rapidly, eliminates the output limit-cycle oscillation, and provides a robust and stable output voltage of 2.5 V for the input voltage of 5 V and load current of 0.35-22.4 mA.

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