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Analysis and design of a digital proportional-resonant controller for a single-phase bidirectional LC rectifier.

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Advisors: Robert Griñó and Domingo Biel

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Title of the thesis: **Analysis and design of a digital proportional-resonant controller for a single-phase bidirectional LC rectifier.**

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Abstract

A boost high-power-factor ac/dc converter is designed. The converter presents a bi-directional power flow capability. A bias capacitor connected in series with the ac source provides a dc voltage boost at the input. Accordingly, a voltage that is always positive is applied at the input of a conventional boost dc/dc converter. A bi-directional dc/dc boost converter is employed to couple the ac side with the dc output. The converter can be controlled with a sinusoidal average current at the ac side that is either in phase or 180^{o} out of phase with the ac source.

Therefore, this design can works with an unity power factor in rectification mode or inversion mode. The topology was employed for the design of an ac/dc battery charger with a unity power factor for rated power of 2 kVA. IGBT devices with anti-parallel diodes are used as switches. Replacing the diode bridge it can eliminates crossover distortions that are inevitable in a conventional Active Power Factor Correction (APFC) circuit with diode rectification bridge at its front end. Removing the diode bridge and usage of two bi-directional switches allows for bi-directional instantaneous power flow which makes possible operation in the inversion mode, in which power is transferred from the dc source to the ac source. At any instance of time only one semiconductor device conducts (as opposed to three or two in conventional rectifiers), which results in higher efficiency.

The proper design of the control loops guaranties the output voltage regulation and operation with a unity power factor and low harmonic distortion despite to the load variations or the grid harmonic contents.

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1. Introduction

a. Requirements and specifications.

The main requirements of the current project are: to model, design and test a boost converter with a unity power factor, inversion capability, bidirectionality in current, regulation of the output voltage and robustness with respect to disturbances/harmonics in the grid and changes in the load.

b. Statement of purpose

- Find the dynamic equations that describe the converter behaviour.
- Size the components of the boost converter according to the required performance and the desired dynamics.
- Obtain a model that describes the dynamics of the averaged system and select the values of the inductance current, the bias voltage and the references voltages for the control loops.
- Implement and simulate the system in Matlab [1] using the developed models and the controllers previously designed.
- Adjust the controller's parameters to achieve the performance initially established in the specifications.

c. Work plan

This section describes the particular goals of each stage of this work.

- Stage 1: Study of the boost converter.

  Objectives:

  - Determine the boost converter topology used in this work.
  - Find the equations of the dynamic system.
  - Study the zero dynamics.
  - Study the conditions that guarantee positive voltage.
  - Calculate the values of the bias capacitor and the output capacitor by using numerical methods with Maple software.

- Stage 2: Model the averaged system in the continuous time framework.

  Objectives:

  - Design a boost converter in averaged mode using Simulink software.
  - Test the design with constants voltages and changes in the load.
  - Implement the boost converter by using components of the Sim Power Systems Matlab toolbox.

- Stage 3: Controller design in continuous time framework.

  Objectives

  - Design of the current control loop parameters.

- Implement the controller with Simulink.
- Select the bias voltage and the output voltage.
- Design a proportional-resonator controller.
- Implement the controller with Simulink.
- Verify the proper controller's performance.

- Stage 4: Model and design the PWM.

  Objectives:

  - Study and find the best topology of PWM.
  - Select the minimum time interval that fulfils the required dead-time.
  - Implement the PWM with Simulink.
  - Verify the proper performance.

- Stage 5: Include the PWM to the boost converter.

  Objectives:

  - Include the PWM developed in the previous stage.
  - Test the system with constant voltages and adjust the dead time.

- Stage 6: Controller design in the discrete time framework.

  Objectives:

  - Design of current control loop in the discrete time framework.
  - Implement the discrete time controller with Simulink.
  - Select the bias voltage and the output voltage.
  - Design a discrete time proportional-resonator controller.
  - Implement the controller with Simulink.
  - Verify the proper controller's performance.

- Stage 7: Design of test bench.

  Objectives

  - Design the test to realistic cases by using test standards.

- Stage 8: Simulation Results.

  Objectives

  - Obtain simulation results in order to confirm the proper behaviour of the complete system.
  - Measure the voltages, the currents, the powers, the THD, the power factors and figure out some conclusions of the results.

- Stage 9: Report writing.

  Objectives

- Write the master's final project, reflecting the development carried out during the entire project lifecycle.

d. Gantt diagram.

Figure 1 shows the Gantt diagram of this work which considers the previously described stages.

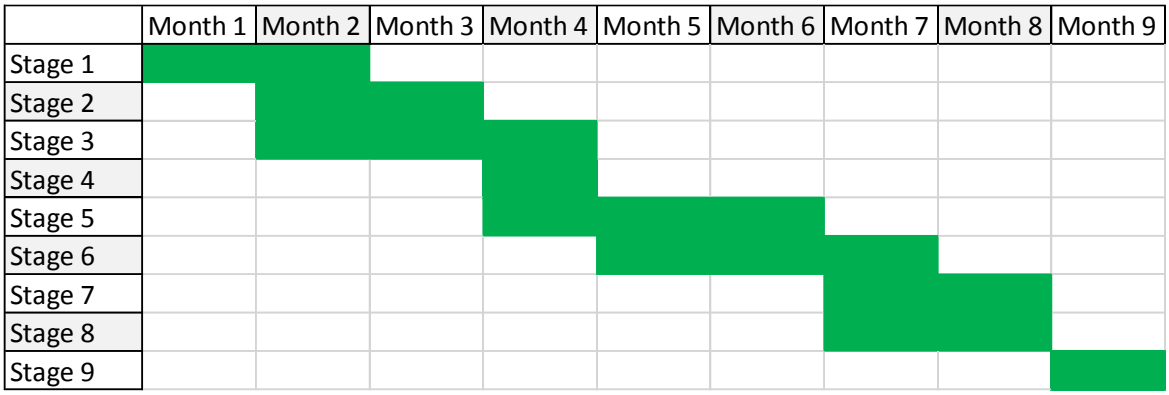


Figure 1. Gantt diagram

1.1. State of the art

1.1.1 Power converters

Nowadays power converters, with controlled or uncontrolled rectifiers, and motor drives operating at the mains voltage are the major pollutant of the ac power distribution grid.

The number of industrial, commercial and residential power consumers with non-linear input characteristics, due to the choppers and the frequency converters employed, has been increased in the last years thus leading to a grid pollution rising. An the problem constitutes a field of interest for many researchers and engineers that study how to manage the power converter (and its control) to get a better power factor correction with low harmonics operation.

There are some topologies suitable for PFC circuits (Cuck, Boost, Flyback…) [2], some which highly depend on the feedback control to achieve the low total harmonic distortion (THD) such as Boost and Flyback converters operated in continuous conduction mode (CCM). Other circuits seem to poses inherent high power factor properties like Boost and Flyback converters while operated in discontinuous conduction mode (DCM). Operation in critical conduction mode is also possible. In addition to finding suitable topologies, the control of active power factor correction implies a major challenge since this are systems with nonlinear-pulsating dynamics. Conventional small signal linearized models and control methods are difficult or impossible to apply because control parameters (such as duty ratio) are controlled to vary in a wide range, and requires a large signal control.

This work presents a novel topology [4] applicable for PFC circuits. A rectification diode bridge is not used to interface with the ac source, allowing the power flow in both directions. Thus, the very same circuit may be operated either as a high quality rectifier or as an inverter. A previous attempt to replace, the diode rectifier with a boost capacitor was based on Cuk topology implemented with bi-directional current switches. The topology proposed in that paper is based on the boost topology and implies the following advantages over the previous one: reduced order of the system (three state variables instead of four in the previous topology), better stability, decreases the number of components, better switch utilization, and reduced current stress on the switches. Improved efficiency and power factor are also expected as a result of omission of the diode rectification bridge.

1.1.2 Controllers

A summary of the mostly used control strategies in the industry is exposed in this section. Generally speaking in the industry one can find the following control structures:

- Proportional-integral-derivative (PID)
- Fuzzy control
- Sliding Mode control (SMC)
- Adaptive Feed-forward Cancellation(AFC)

Despite being almost 60 years old, Integral Derivative Proportional control (PID) is still extensively used in industrial applications. A PID controller continuously calculates an error signal e(t) as the difference between a desired setpoint (SP) and a measured process variable (PV) and applies a correction based on proportional, integral or derivative of that signal. The controller is able to reject constant disturbances but only reduces the effect of time variable ones. A PID, as its name suggests, acts at three different levels:

- Proportional: determines the reaction of the current error.
- Integral: corrects the integral of the error to reduce it to zero (error stationary).
- Derivative: determines the reaction of the time (derived) in which the error occurs.

Integration windup is a problem in PI feedback controllers that results in overshoot that would not occur if the system were being controlled only in its linear range. The linear range of a control system can be limited by saturation of the feedback controller output. The rise time of a system step response when the controller must initially be saturated is longer than that of the step response in the linear region. For that reason, the integrator will accumulate a larger output during the rise, causing overshoot. Integrator anti-windup can be used to avoid this overshoot.

Fuzzy controllers are very simple conceptually. They consist of an input stage, a processing stage, and an output stage. The input stage maps the sense signal or other inputs, such as switches, thumbwheels, and so on, to the appropriate membership functions and truth values. The processing stage invokes each appropriate rule and generates a result for each one, and combines the results of the rules. Finally, the output stage converts the combined result back into a specific control output value.

Sliding mode control, or SMC, is a nonlinear control method that modifies the dynamics of a nonlinear system by application of a discontinuous control signal that forces the system to "slide" along a cross-section of the system's normal behaviour. The state-feedback control law is not a continuous function of time. Instead, it can switch from one continuous structure to another based on the current position in the state space. Hence, sliding mode control is a variable structure control method.

The Adaptive Feed-forward Cancellation (AFC) is most robust than PI to reject whatever kind of harmonic no desired and with better results. This is a control technique that has been successfully applied to selectively reject periodic output disturbances in continuous-time mechanical systems [6]. This control technique allows the designer to reject or attenuate, in a selective manner, specific harmonics of periodic disturbance signals.

1.2. Thesis's objectives

The main objective of the thesis is the analysis, design, simulation, and control of a LC boost rectifier converter as an AC-DC inverter bidirectional in current. The system should be robust with respect to load changes, anomalies in the grid and should keep the desired voltage regulation and responding with a unit power factor and a THD<3% in any case.

- Study and evaluate the chosen topological.
- Model the LC boost rectifier and obtain the equations that describe its dynamic response.
- Design digital controllers in order to achieve the desired performance.
- Simulate the overall systems to validate the design.

2. Analysis and description of the boost converter

This chapter describes the methodologies applied to obtain the equations that describe the behaviour of the system. Additionally, the adjustment of the components values according to the desired performance is also detailed.

2.1. Topological description of the LC boost rectifier

This section is devoted to the analysis of the circuit (Figure 2) of the LC boost rectifier. The converter used in this work is split in 4 parts.

- The grid voltage that supplies to the converter the current demanded by the load. The grid is set to $v_r(t) = V_r sin(\omega t)$ and the current has to be $i(t) = Isin(\omega t)$, to ensure unity power factor at the input.
- A capacitor is connected in series with the grid. The functionality of this capacitor consist in adding a constant bias voltage that guarantees the boost condition. The voltage set in this capacitor is named V_C and it is considered constant in steady state.
- The typical boost (DC-DC Converter) is implemented just after the bias capacitor. It has 1 inductance to minimize the ripple, 2 switches with unidirectional voltage blocking capability (antiparallel diodes are placed in parallel with the IGBT transistors). Finally it has an output capacitor in order to keep a constant output voltage constant and to minimize the alternating current component. The size of the capacitor is obtained considering the maximum power that can deliver the converter and the allowed voltage ripple.
- The last part is the load which is considered pure resistive and consumes a current i_0 and has a voltage V_0.

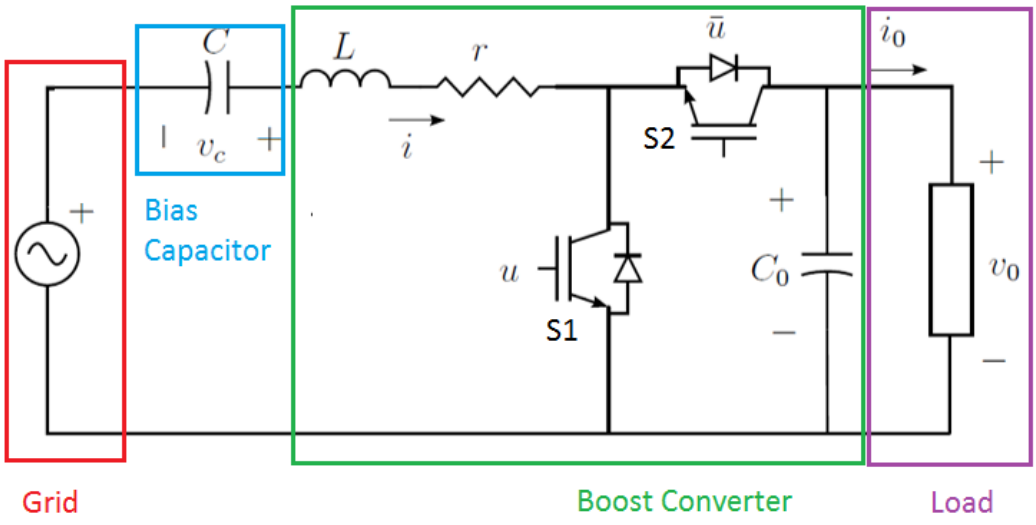
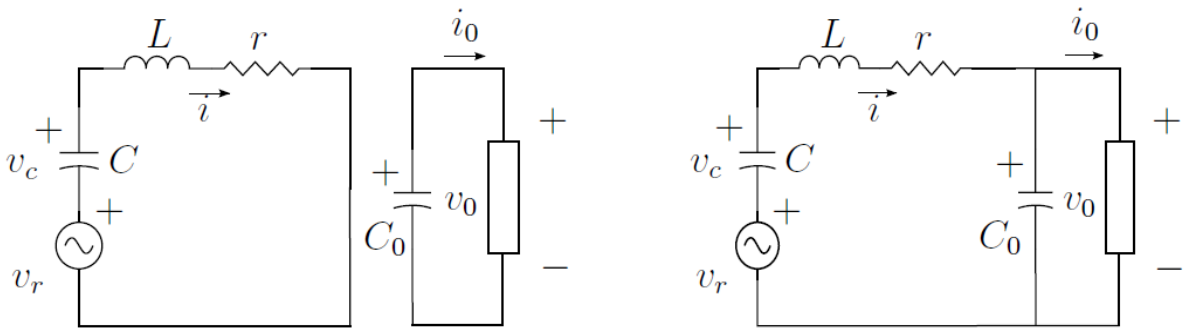


Figure 2. LC boost rectifier split in 4 parts: the grid, the bias capacitor, the boost converter and the load.

Since the voltage in the bias capacitor is always positive a low cost electrolytic capacitor can be employed. The inductance is used to reduce the switching ripple of the input current and its size is calculated for a maximum allowed ripple. It's important to mention that

chosen values take into account the ripple, the sizes and the bandwidth ranges because they are incompatible among them.

Two different topologies can be derived as functions of the switches states. This allowing to define the variable $u(t)$ to control the states of the switches.



$\boldsymbol{Mode\ 1: when\ u(t) = 1\ (S_1 = 1, S_2 = 0)}$ $\boldsymbol{Mode\ 2: when\ u(t) = 0\ (S_1 = 0, S_2 = 1)}$

Figure 3. Topologies of the LC boost according to the u variable.

Therefore, the variable $u\ (t)$ is defined as:

$$u\ (t) = 0 \ \text{ if S1 is open and S2 is closed}$$

$$u\ (t) = 1 \ \text{if S1 is closed and S2 is open}$$

The previous figure shows the operation modes. Each circuit depends on the switches position. Both switches work in different time intervals, and when one switch conducts and the other is opened and vice versa. Therefore, in a switching period one can obtain two different topologies (Figure 3). The resistor is included to emulate the power loses of the devices of the converter, assuming that they have same value in both circuits.

The modes behaviour can be described as follows:

- In mode 1 the control signal of switches is $u = 1$. There are two different states of behaviour. In the first one, with the positive semicycle of the grid voltage (V_r), the capacitor is charging and the inductance voltage is positive ($v_L > 0$), this implying an increase of the flowing current. In the negative semicycle, the capacitor is discharged and v_L remains positive. In both cases the output capacitor is discharge to supply the connected load.
- In mode 2 the control signal of switches is $u = 0$. Like happened in the first mode there are two states again. In the first positive semicycle both capacitors are charged due to the grid voltage, and, on the other hand, in the negative semicycle the bias capacitor manages the negative voltage of grid and therefore the output capacitor is charged. In both cases $v_L < 0$ and the current decreases.

To obtain a sinusoidal current in phase with output voltage is needed to control the current using the switches. It is also required an average voltage in the bias capacitor (v_C) that supports the grid and an enough capacity of C_0 to maintain the output voltage constant.

2.2. System dynamic equations

This section describes the dynamic equations obtained by analysing the converter in the different switching states. Once the equations are known, a linearization of the system is done assuming small values of the ripple produced by the switching with the finality to ease the control design.

The next set of equations are found through an analysis of the circuits (mode 1 and mode 2).The next table are summarized the results in both modes.

$v_r(t) + v_C(t) = r\, i(t) + L\frac{di(t)}{dt}$ $C\frac{dv_C(t)}{dt} = -i(t)$ $C_0\frac{dv_0(t)}{dt} = -i_0(t)$	$v_r(t) + v_C(t) = r\, i(t) + L\frac{di(t)}{dt} + v_o(t)$ $C\frac{dv_C(t)}{dt} = -i(t)$ $C_0\frac{dv_0(t)}{dt} = -i_0(t) + i(t)$
Dynamic equation in the mode 1	Dynamic equation in the mode 2

It is necessary to express the dynamic equations of the boost converter as a single system, instead of two separate ones as they appear in the table. Introducing the variable $u(t)$, the following set of equations can be easy obtained:

$$L\frac{di(t)}{dt} = v_r(t) + v_c(t) - r\, i(t) - v_0(t)u(t) \quad (1)$$

$$C\frac{dv_c(t)}{dt} = -i(t) \quad (3)$$

$$C_0\frac{dv_0(t)}{dt} = -i_0(t) + i(t)u(t) \quad (2)$$

The states of the signal $u(t)$ produces some ripple in the state variables at the switching frequency. This ripple in well-designed systems is quite small, making it possible to approximate with high accuracy the actual dynamics (with ripple) by smooth curves that will describe the averaged behaviour of the system. A method very common to erase the small perturbations and to get the "dominant part "of the actual behaviour consists in the use of moving averages in which each signal is replaced by its average during a period of commutation.

First of all, it is assumed that the system is studying in a working point, in which the state variables achieve their stationary values, these are defined as:

i^{ss} *Current in the inductance in stationary state.*

i_0^{ss} *Current in the output in stationary state.*

v_0^{ss} *Voltage in the output in steady state.*

v_c^{ss} *Bias voltage in steady state.*

u^{ss} *Duty cycle in steady state*

v_r^{ss} *Grid voltage in steady state.*

Applying the superposition principle to the system at the working point. Equations (1) and (2), result in:

$$0 = v_r^{ss} + v_c^{ss} - r\, i^{ss} - v_0^{ss}$$

$$0 = -i_0^{ss} + u^{ss} i^{ss}$$

which yields,

$$u^{ss} = \frac{i_0^{ss}}{i^{ss}}$$

At this point it is assumed that average duty cycle $\langle u(t) \rangle_{Ts}$ is equal to the static state value u^{ss} but with a perturbation around this value denoted by $\hat{u}(t)$:

$$\langle u(t) \rangle_{Ts} = u^{ss} + \hat{u}(t) \tag{3}$$

It is also assumed that the value of the disturbance $\hat{u}(t)$ is very small than the steady state value u^{ss} so that the average value of the duty cycle will always remain fairly close to u^{ss}.

The system will respond to this input disturbance with the average values of the variables as follows:

$$\langle v_0(t) \rangle_{Ts} = v_0^{ss} + \hat{v}_0(t) \tag{4}$$

$$\langle i_0(t) \rangle_{Ts} = i_0^{ss} + \hat{\imath}_0(t) \tag{5}$$

$$\langle i(t) \rangle_{Ts} = i^{ss} + \hat{\imath}(t) \tag{6}$$

$$\langle v_c(t) \rangle_{Ts} = v_c^{ss} + \hat{v}_c(t) \tag{7}$$

The perturbations mentioned previously in the equations (4), (5), (6) and (7) are considered to be very small with respect to the corresponding steady-state values.

Replacing the mean values defined by equations (4), (5), (6), (7) and (3) in the system equations defined by (1) and (2), the following set of equations is obtained:

$$L\frac{d}{dt}\left(i^{ss} + \hat{\imath}(t)\right) = v_r^{ss} + \left(v_c^{ss} + \hat{v}_c(t)\right) - r\,(i^{ss} + \hat{\imath}(t)) - (v_0^{ss} + \hat{v}_0(t))(u^{ss} + \hat{u}(t))$$

$$C_0\frac{d}{dt}(v_0^{ss} + \hat{v}_0(t)) = -(i_0^{ss} + \hat{\imath}_0(t)) + (i^{ss} + \hat{\imath}(t))(u^{ss} + \hat{u}(t))$$

Expanding the products of the brackets one obtain:

$$L\frac{d}{dt}\hat{\imath}(t) = v_r^{ss} + v_c^{ss} + \hat{v}_c(t) - r\,i^{ss} - r\,\hat{\imath}(t) - u^{ss}\cdot v_0^{ss} - u^{ss}\cdot\hat{v}_o(t) - \hat{u}(t)\hat{v}_0(t) - \hat{u}(t)v_0^{ss}$$

$$C_0\frac{d}{dt}\hat{v}_0(t) = u^{ss}i^{ss} + u^{ss}\,\hat{\imath}(t) + \hat{u}(t)i^{ss} + \hat{u}(t)\hat{\imath}(t) - i_0^{ss} - \hat{\imath}_0(t)$$

These equations should be simplified to obtain the linearized model. The first simplification can be easy figure out considering the equations at equilibrium (working point), that erase all the constant terms. The second simplification is done to eliminate the non-linear terms. As discussed above, the perturbations $\hat{u}(t), \hat{v}_0(t), \hat{\imath}_0(t), \hat{\imath}(t)$ and $\hat{v}_c$ (t) are considered to be very small and, therefore, any product between any of these terms will be even smaller and, then all the terms involving products between perturbations will be neglected. Applying this approximation the system of equations results in:

$$L\frac{d}{dt}\hat{\imath}(t) = v_r^{ss} + \hat{v}_c(t) - r\,\hat{\imath}(t) - u^{ss}\hat{v}_0(t) - \hat{u}(t)v_0^{ss} \tag{8}$$

$$C_0\frac{d}{dt}\hat{v}_0(t) = u^{ss}\hat{\imath}(t) + \hat{u}(t)i^{ss} - \hat{\imath}_0(t) \tag{9}$$

2.3. Study of the Zero Dynamics

Zero dynamics analysis is required to determine the controllability of this system. The nonlinearity of the system difficult to obtain an approximate model that accurately reflects the behaviour of the system. The method followed here consists in assuming the variables of the system at the steady state after a certain time, and verify if their values comply with the restrictions imposed by the model of the physical system, and, finally, figure out the conditions to be met for getting the desired performance.

If the performance is correct, the primary current is sinusoidal and is in phase with the voltage, that is, $v_r(t) = V_r sin(\omega t)$ and $i(t) = Isin(\omega t)$.

The equations that relate the behaviour of the variables v_c, v_0 and v is obtained by solving the system of differential equations with this condition of the current (assuming a pure resistive load). These equations have a corresponding part that describe the transient of the converter and another part that gives the steady-state behaviour of the operating mode. The goal is to get a asymptotically stable system. Therefore, we should verify that the transient tends to zero when time tends to infinite. It can be proved that this sentence is true since effectively the transient disappears and the steady-state is achieved. Then by neglecting the part corresponding to the transient of the equations, we get the expressions shown in the equations (10), (11), (12), which are the ones that describe the behaviour of the converter in the steady-state operation.

$$v_C(t) = V_C(0) - \frac{I}{\omega C} + \frac{I}{\omega C}cos(\omega t) \tag{10}$$

$$v_0(t) = \left(\begin{array}{c} -\frac{1}{2}IR(r\,I - V_r) + \frac{IR}{2C\omega}\left[\frac{4C_0R\omega(-I+CV_C\omega)\,cos(\omega t)}{4+C_0^2R^2\omega^2} - \right. \\ \frac{\omega\left(-C_0IR+C\left(-V_r+I\left(r+CLR\omega^2\right)\right)\right)cos(2\omega t)}{1+C_0^2R^2w\omega^2} + \frac{8(I-CV_C\omega)\,sin(\omega t)}{4+C_0^2R^2\omega^2} + \\ \left.\frac{\left(C_0CRV_r\omega^2+I\left(-1+C(L-C_0rR)\omega^2\right)\right)sin(2\omega t)}{1+C_0^2R^2\omega^2}\right] \end{array} \right)^{1/2} \tag{11}$$

$$u(t) = \frac{[I + \omega CV_c(0) + I\,cos(\omega t) - CIL\omega^2\,cos(\omega t) - CIr\omega\,sin(\omega t) + CV_r\omega sin(\omega t)]}{\omega C v_o(t)} \tag{12}$$

The equations (10), (11), (12) describe an oscillatory behaviour, because those equations are composed of sinus and cosines, with an average value different from zero in all cases. Furthermore, $v_0 > 0$ and, therefore, the denominator of u is never cancelled.

2.4. Calculation of the bias capacitor value in steady-state operation

The bias capacitor has to ensure that the input voltage should be positive. The input voltage is defined as: $v_{in} = v_r(t) + v_c(t)$. As already mentioned previously, v_c has to cope with the voltage of the half-period negative of v_r and in addition to supply the output capacitor C_0.This generates the following condition that has to be fulfilled for the converter to properly work.

$$v_r(t) + v_c(t) \geq 0 \tag{13}$$

From equation (13) the average value is extracted, equation (14), which has to be higher than the sum of its amplitude of oscillation plus the amplitude of the grid to ensure with a certain margin that the input voltage is always positive.

$$\bar{v}_c(t) = \frac{1}{C}\int_0^t i(t)dx + V_c(0) \tag{14}$$

In summary, the bias capacitor should meet the following condition:

$$\bar{v}_c(t) = V_c(0) - \frac{I}{\omega C} + \frac{I}{\omega C}cos(\omega t) > V_r \Rightarrow V_c(0) > 2\frac{I}{\omega C} + V_r$$

The design of the bias capacitor C that fulfils this condition ensures a positive voltage of bias.

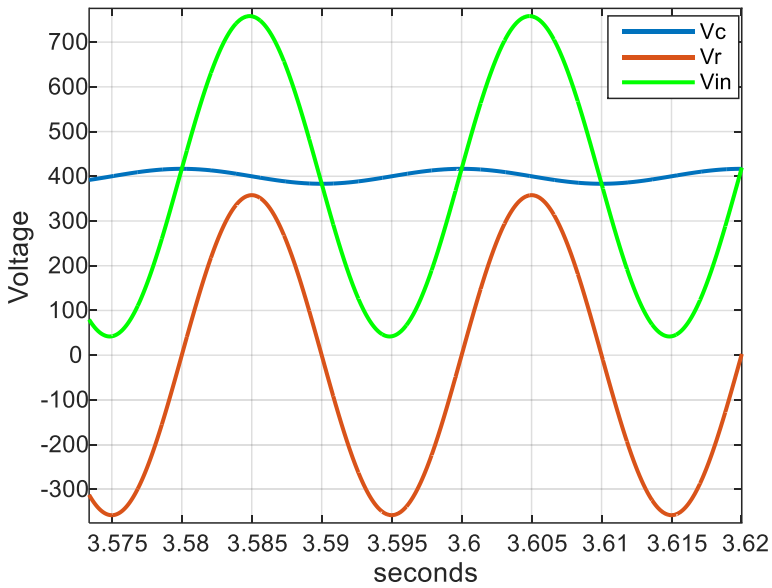


Figure 4. Grid voltage (brown), bias voltage (blue) and input voltage (green). Scales [Y: volts, X: seconds]

The following parameters have been used in the figure 4:

$$\mathrm{V_c}(0) = 400\mathrm{V}, C = 2340uF, P = 2000\,W$$

and the plotted signals are:

$$\mathrm{v_c(t)} = \mathrm{V_c(0)} + \frac{\mathrm{I}}{\omega\mathrm{C}}\cos(\omega\mathrm{t}) = 400 + 16.71\cos(100\pi\mathrm{t})$$

$$\mathrm{v_r(t)} = \sqrt{2}\cdot 230\sin(\omega\mathrm{t})$$

$$\mathrm{v_{in}(t)} = \mathrm{v_c(t)} + \mathrm{V_r(t)}$$

where the $\mathrm{V_{in}^{min}} = 40\,V$, which is the positive margin in case of bad performance, and it is set for safety reasons. As it can be seen in the figure, the chosen capacitor gives us a small ripple ($\pm 16\,V$) and in any case the sum of signals is below the minimum voltage.

2.5. Pulse-width modulator (PWM)

The model of the power converter used in the simulations is assembled by using SIMULINK standard components such as: voltage sources, resistor-inductor branches, diodes, capacitors, resistors and IGBT switches. The components are simulated by also

considering their parasitic losses in the linear components and saturation voltages in the switching devices. Figure 5 shows the implementation of the PWM modulator in SIMULINK.

A regular centered-pulse-width modulation (PWM) is implemented to drive the switches of the power converter. A switching frequency of F_S = 30 kHz is set to generate the PWM signals. The PWM modulator is built by comparing a triangular waveform with unity peak to peak amplitude and without dc offset. A 1 μs dead time has been included into the PWM modulators when generating complementary PWM signals, u and u', taking account for the non-instantaneous switching capabilities of the IGBT modules employed in the power stage.

The following block diagram shows the implemented model that includes the dead time and avoids the overlapped states within the switching periods.

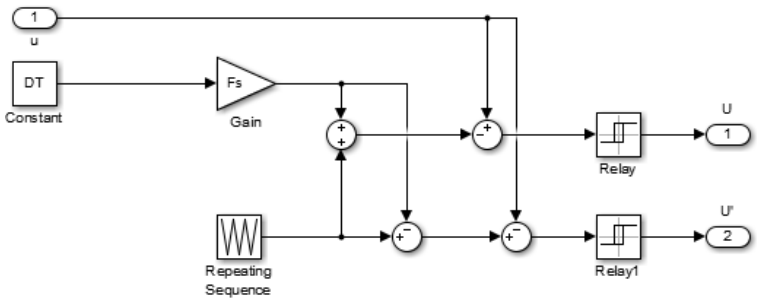


Figure 5. PWM Simulink block diagram with a centered signal like reference.

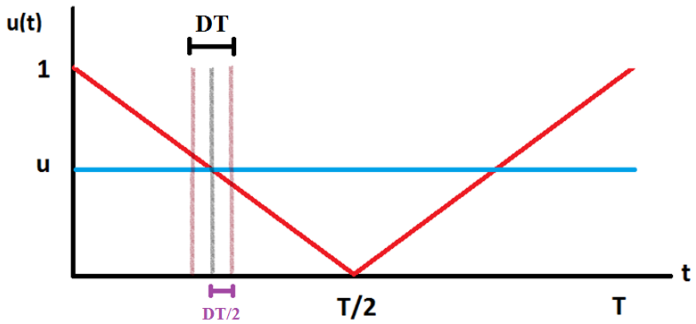


Figure 6. Modulation process using centered pulse.

The figure 6 presents the modulation process, that can be summarized by the following equations:

- Case of u: Where the Time's rank $\epsilon [0, \frac{T}{2}, T]$

$$\text{Value of t implementing dead time } \epsilon [1 + \frac{DT}{2}, \frac{DT}{T}, 1 + \frac{DT}{T}]$$

- Case of u': Where the Time's rank $[0, \frac{T}{2}, T]$

$$\text{Value of t implementing dead time } [1 - \frac{DT}{2}, \frac{DT}{T}, 1 - \frac{DT}{T}]$$

- Function of PWM: $u(t) = -\frac{2}{T}t_1 + 1$

  Given a margin in: $t_1 = \frac{DT}{2}$

  Trend of PWM when u = 1: $u_{max} = -\frac{2}{T}\frac{DT}{2} + 1 = 1 - \frac{DT}{2} = 1 - DT \cdot Fs$

Trend of PWM when u = 0: $u_{min} = 1 - (1 - DT \cdot Fs)$

This procedure gives a duty cycle margin that guarantees a dead time between shifting. These margins are implemented within relays (Figure 5).

2.6. Transfer functions

The linear model of the LC boost converter described by the equations (8) and (9) allow us to get the system transfer functions that will be used in the study and will allow to apply conventional control techniques.

Applying the following change of variable (call partial feedback):

$$w(t) = v_r(t) + v_c(t) - v_o(t)u(t)$$

And replacing in (1) and (2), one can be obtain the following set of equations:

$$L\frac{di(t)}{dt} = -r\, i(t) + w(t)$$

$$C\frac{dv_c(t)}{dt} = -i(t)$$

$$C_0\frac{dv_o(t)}{dt} = i\frac{v_r(t) + v_C(t) - w(t)}{V_o} - i_o(t)$$

Therefore, applying Laplace transform:

$$L\, s\, I(s) = -r\, I(s) + W(s) \tag{13}$$

$$C\, s\, Vc(s) = -I(s) \tag{14}$$

From (13), isolating the inductance current, one gets:

$$\frac{I(s)}{W(s)} = \frac{1}{Ls + r} \tag{15}$$

The equation (15) is replaced in (14), thus yielding:

$$\frac{V_c(s)}{W(s)} = \frac{-1}{Cs(Ls + r)} \tag{16}$$

Now the procedure consist in isolate $V_c(s), I(s)$ and $U(s)$ from (8) and (9):

$$L\, s\, I(s) = V_r + V_c(s) - rI(s) + V_0U(s)\ - V_0$$

$$C\, s\, V_c(s) = -I(s)$$

Replacing the partial feedback in (8) and (9) the transfer functions are finally obtained:

$$\frac{V_c(s)}{U(s)} = V_O\frac{\frac{-1}{sC(Ls + r)}}{1 - \frac{-1}{sC(Ls + r)}} = V_O\frac{-1}{LCs^2 + rCs + 1}$$

$$\frac{I(s)}{U(s)} = V_O\frac{\frac{-1}{(Ls + r)}}{1 + \frac{-1}{(Ls + r)}\frac{1}{sL}} = V_O\frac{-sC}{LCs^2 + rCs + 1}$$

3. Controller design

This section explains the control design in order to achieve the desired performance in the boost topology. Considering that the averaged model of the converter is non-linear, the linearization has been applied. On one hand the partial feedback technique is used and on the other hand the system is linearized around the working point. Therefore the linearized transfer functions described previously are used to design the controllers by employing traditional control techniques. The implemented controllers are detailed below:

I. Control of the input current

The first and fastest control loop ensures that the converter input current tracks the desired sine waveform. Proportional resonator Control is used in this stage. This control synchronizes the phase of the current with the grid voltage (by using PLL) getting a THD<3%.

II. Control of the capacitor bias voltage

The second control loop, which is slower than the previous one, controls the bias capacitor voltage in order to fulfil with the operating conditions. It injects additional current when the capacitor is in transitory state (charging) and keeps the voltage constant, according to the boost condition. This control is a PID.

III. Control of the output voltage

The third and slowest control loop regulates the current amplitude to ensure the power load demand.

3.1. Controller architecture

The figure 3 shows the controllers implemented in the system. The block called "V_0 controller" manages the load power modifying the current contribution. The block called "V_c controller" is designed to avoid that $v_{in} < (v_r(t) + v_c(t))$ and guarantees a stable voltage charging. The block called "I controller" synchronizes the inductance current phase and the phase of the grid and it is the fastest controller. A partial feedback is used to linearize and simplify the current loop. Finally the PWM controls the commutation of the switches according with the control variable states.

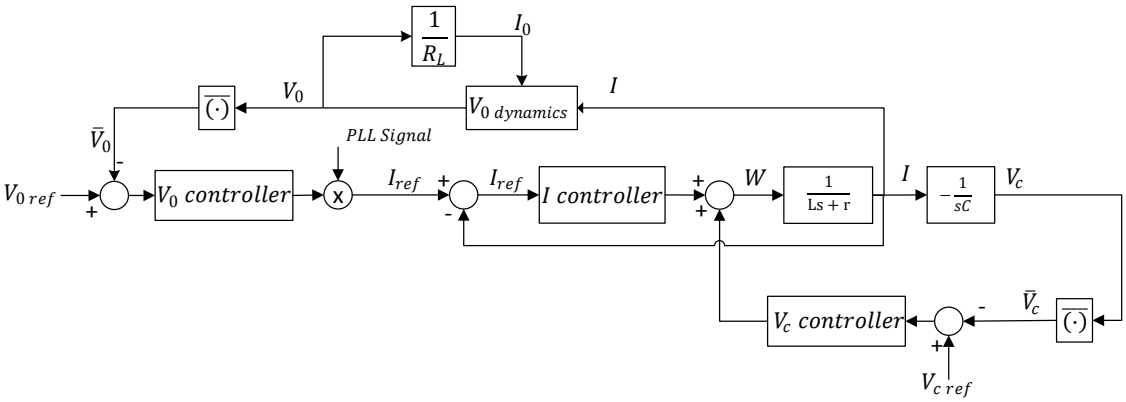


Figure 7. Block diagram of the control architecture.

3.1.1 Partial feedback

In order to simplify the current loop and to easy the design of its respective controller, a change of variables that transform the differential current equation in a linear one is applied. So, defining the variable: $w(t) = v_r(t) + v_c(t) - v_0(t)u(t)$. The equations of the system are reduced to

$$C\frac{dv_0(t)}{dt} = i\frac{v_r(t) + v_c(t) - w(t)}{v_0(t)} - i_0(t)$$

$$L\frac{di(t)}{dt} = r\,i(t) + w(t)$$

$$C\frac{dv_c(t)}{dt} = -i(t)$$

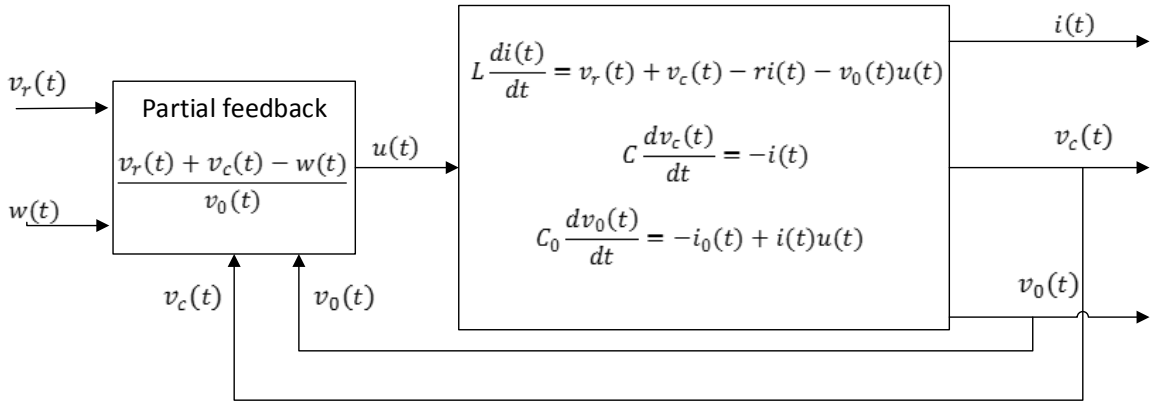


Figure 8. Partial feedback scheme.

With the partial feedback is easy to design of the current controller. Since the bilinear equation:

$$L\frac{di(t)}{dt} = r\,i(t) + v_r(t) + v_c(t) - v_0(t)u(t) \tag{17}$$

is transform to the linear one:

$$L\frac{di(t)}{dt} = r\,i(t) + w(t) \tag{18}$$

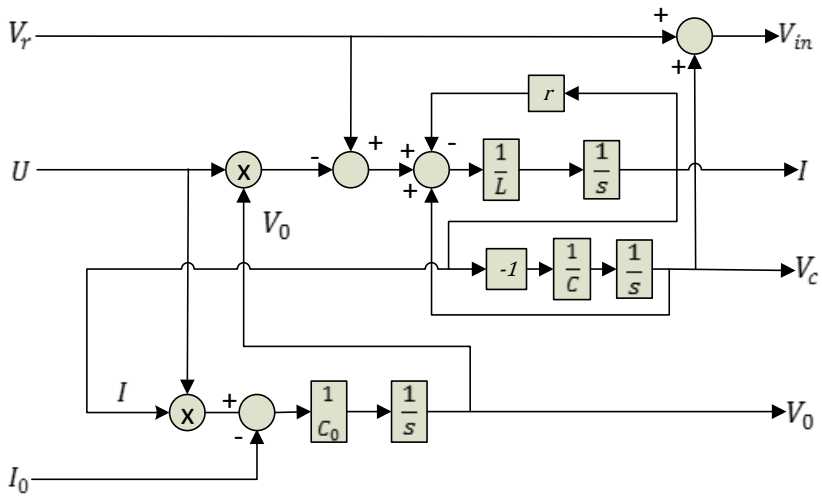


Figure 9. Model implemented in Simulink for the averaged equations of the boost converter.

3.2. Discrete-time controller design

The control has the following objectives:

- To keep the average value of the DC output voltage equal to the reference one.

- To keep the average value of the bias voltage of the capacitor to the reference one.

- To get a sinusoidal grid current in phase with the grid voltage. The amplitude of the current must be the required such that the balance of the real power of the system is fulfilled.

3.2.1 Design of the current control loop

The current control loop is implemented with a proportional-resonant [3] structure in order to reject periodic disturbances, such that the placement of an infinite gain on the open-loop transfer function is at the desired ω_k frequency of the disturbance. This task is done by the R_k resonator. A perfect disturbance rejection at such frequency can be expected. A proportional block with constant K_p is added in order to help the reference tracking. Figure 10 shows the block diagram for the proposed discrete-time resonator.

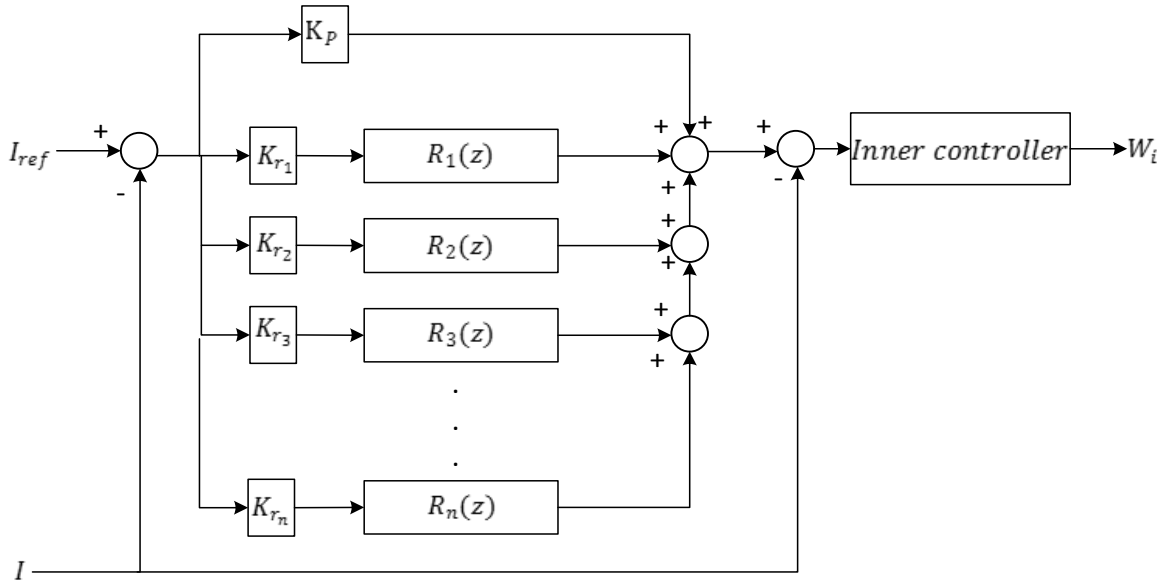


Figure 10. Block diagram of the proportional-resonant current controller with *n* resonators in parallel with an inner controller in series.

On the other hand, the internal control loop, see figure 10, has the following parts: 1- a stabilization controller $\boldsymbol{K_p}$, an inner controller (low pass filter) and the parallel chain formed by the sum of a proportional path $\boldsymbol{K_r}$ and the addition of the resonators $\sum_{i=1}^{n} \boldsymbol{R_i(z)}$. The inner control loop is designed to provide as high closed-loop bandwidth as possible. The overall behaviour of the resonators control loop is also determined by the behaviour of the closed inner control loop and, therefore, the premise is to get a well behaved inner-loop control. The sinusoidal reference tracking and periodic disturbance rejection capabilities are provided by the Resonators control loop.

In summary, the inner controller is composed by a stabilization controller, which is a low order controller, and presents the fastest dynamics with respect to the rest of the control loops. The objective of this controller is to stabilize the plant and attenuate the disturbances.

Finally, a resonator control loop is added before the inner loop one. This resonator control loop is configured as it is shown in the figure 11.

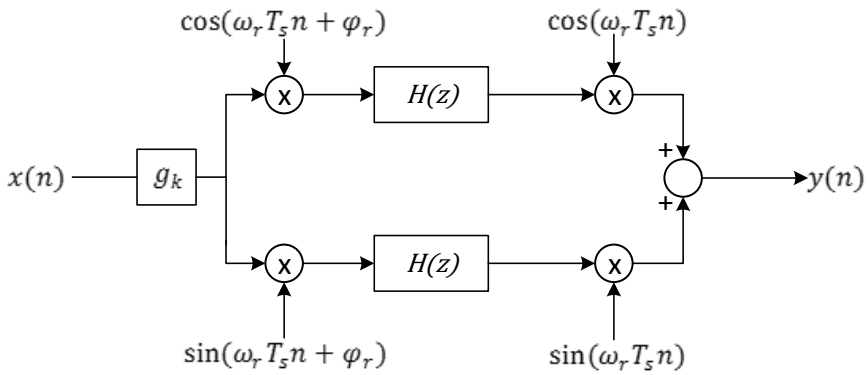


Figure 11. Discrete-time AFC Resonator block diagram.

The equations that describe the resonator control are:

$$R_k(z) = \frac{1}{2} g_k \left[H\left(ze^{-j\omega_k T}\right) e^{-j\varphi_k} + H\left(ze^{j\omega_k T}\right) e^{j\varphi_k} \right] \tag{19}$$

In this work, a Backward Euler integrator has been chosen for the $H(z)$ block:

$$H(z) = \frac{z}{z-1} \tag{20}$$

This has an effect when placing it in each resonator of the transfer function, that is to introduce infinity gain in each one of the ω_i frequencies.

By replacing equation (20) in the equation (19) and simplifying, the z-domain transfer function of the resonator becomes

$$R_k(z) = g_k \frac{cos(\varphi_k) z^2 - cos(\omega_k T_s + \varphi_k)\, z}{z^2 - 2\, cos(\omega_k T_s)\, z + 1} \tag{21}$$

Equation (21) shows the resulting structure for the discrete-time resonator implementation. The parameters involved in the discrete-time resonator are: g_k, ω_k, φ_k and T_s. Where g_k is a positive real gain, ω_k is the frequency, in rad/s, at which the desired resonating gain has to be placed, φ_k is the phase-shift parameter for the R_k resonator, in rad, and finally $T_s = 1/f_s$ is the sampling period, in seconds, for the discrete-time system.

In order to tune a resonator $R_k(z)$ at the resonating frequency ω_k is needed to configure:

- the gain K_r
- the phase ϕ_r.

Now, the phase and gain characteristics of the discrete-time resonator at the ω_k frequency are explored. The behaviour of the system around the resonating frequency ω_k can be studied departing from equation (19).

When the continuous-time frequency ω approaches ω_k, the z variable becomes $z = e^{j(\omega_k T_s + \varepsilon)}$, for a sufficiently small value of $|\varepsilon| \geq 0$. Having substituted this value in the equation (19) and simplifying, the resonator structure becomes

$$R_k(z) = \frac{1}{2} g_k \left[H\left(ze^{j\varepsilon}\right) e^{-j\varphi_k} + H\left(ze^{j2\omega_k T + \varepsilon}\right) e^{j\varphi_k} \right] \tag{22}$$

By replacing the equation (20) in the equation (22), the first term of the equation (22) can be rewritten as:

$$\frac{1}{2} g_k \left[H\left(ze^{j\varepsilon}\right) e^{-j\varphi_k} \right] = \frac{1}{4} g_k \left[\frac{e^{j\left(-\frac{\pi}{2} - \varphi_k\right)}}{sin\left(\frac{\varepsilon}{2}\right)} \right] \tag{23}$$

For the sake of simplicity, let us assume a unitary gain $g_k = 1$. As ε approaches zero from either right or left sides, the module of the equation (23) goes to infinite, as the denominator $\sin(\varepsilon/2)$ goes to zero. The effects of the second term of the equation (22) are marginal at this point, and the equation (24) dominates the behaviour of the resonator structure $R_k(z)$. When ε approaches zero from the left, which is equivalent to say that the input frequency approaches the resonating frequency from the left $(\omega \to \omega_k^-)$, the phase-shift of the system becomes

$$\angle\, R_k\left(e^{j\omega_k T_s}\right)|_{\omega \to \omega_k^-} = -\varphi_k + \frac{\pi}{2} \tag{24}$$

When ε approaches zero from the right, the phase component of the resonator structure becomes

$$\angle R_k\left(e^{j\omega_k T_s}\right)|_{\omega \to \omega_k^+} = -\varphi_k - \frac{\pi}{2} \tag{25}$$

Therefore, the phase-shift of the resonator at the resonating frequency ω_k, is the average of the phase shifts of the resonator when ω approaches ω_k from the right and from the left, hence:

$$\angle R_k\left(e^{j\omega_k T_s}\right) = -\varphi_k \tag{26}$$

The constant K_r is configured by applying an empiric way.

Testing of Resonators

The main difference of the resonators tuning is shown in two cases of study.

Case A: All φ_k parameters have been configured with their values adjusted.

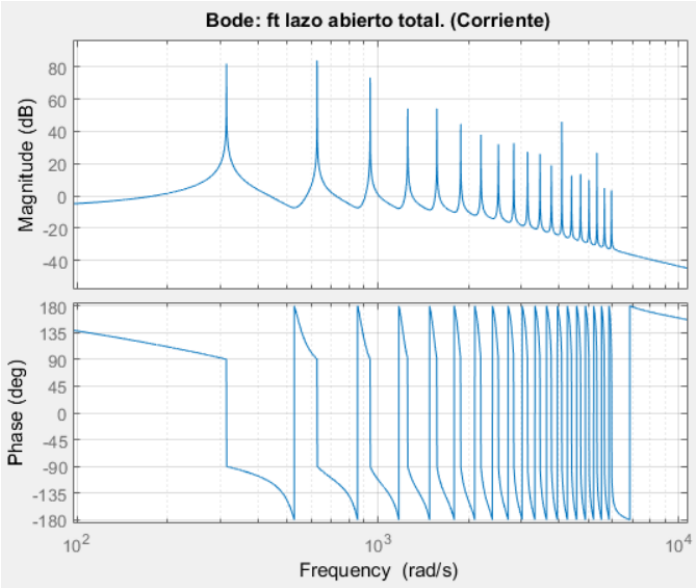


Figure 12. Bode plot of L(z) with adjusting the phase.

As can be seen from figure 12 there are 19 resonant peaks at 50 Hz (314 rad/s) and its respective harmonics. The phase-shifts are all centered at 0º, which guarantee the maximum phase margin on the system.

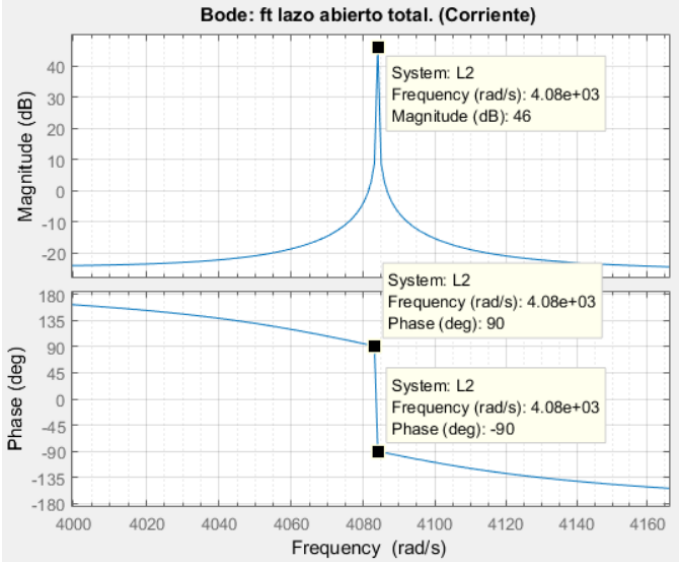


Figure 13. Bode of the 7th resonator with adjusting the phase.

Obviously all phase shifts are centered between 180º-180º (0º) and, then the average value is 0.

Case B: All φ_k parameters have been varied to 0.

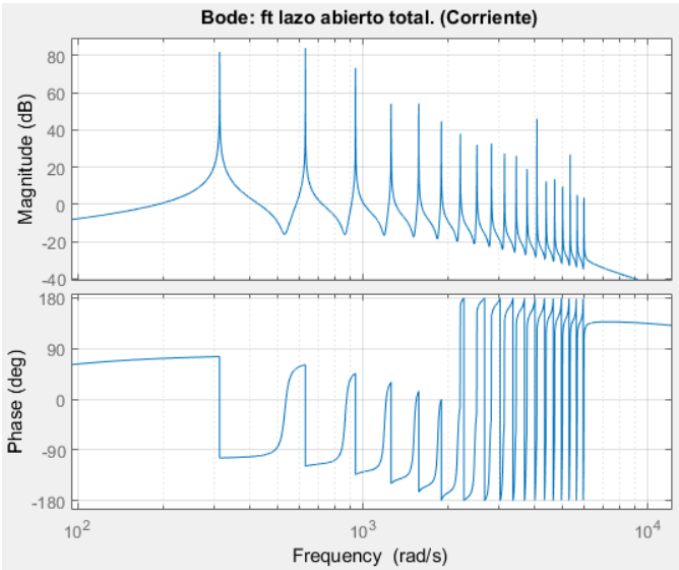


Figure 14. Bode plot of L(z) without adjusting the phases.

By this simulation is shown how the rejections at the desired harmonics are not produced. In the following zoom plot is possible to realize that the phase margin is not zero.

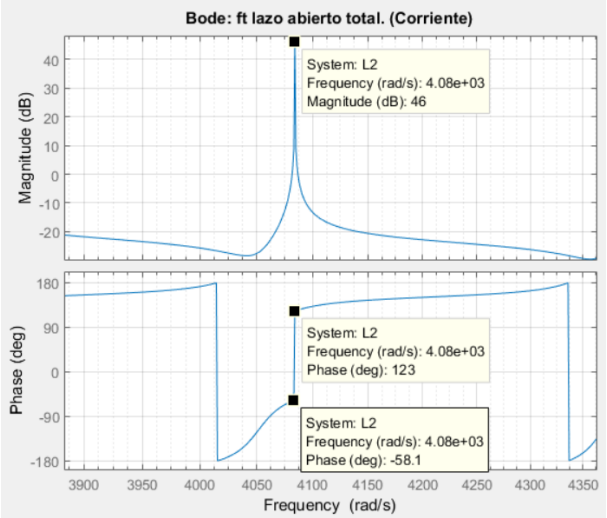


Figure 15. Bode of the 7th resonator without adjusting of shift phase.

$$\mathrm{MP} = \frac{123 + (-58.1)}{2} = 32{,}45º$$

The phase margin is 32.45º. This implies that the phase-shift is not centered to 0º and the resonator does not reject any harmonic with this frequency.

3.2.2 Design of the bias voltage control loop.

A PID controller is included to regulate the bias voltage of the capacitor. The figure 16 shows the placement of the PID in the closed-loop system.

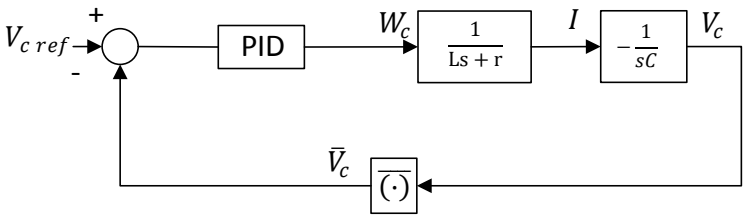


Figure 16. Bias voltage control loop.

The controller injects a momentary amplitude of the current when the voltage capacitor is in the transitory state until it arrives to its reference value.

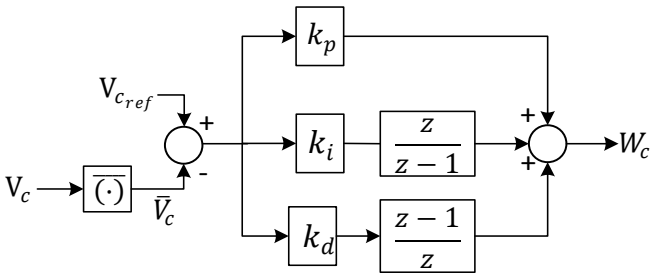


Figure 17. PID controller implementation.

The PID controller ensures that the mean value of the bias voltage is regulated to the desired value. For this purpose a mean value extractor is used. It should be notice that previously a pre-charge operation has to be applied before the bias voltage regulation.

The discrete-time PID controller, shown in the following formula, has been designed by finding convenient pole/zero locations using empiric methods.

$$\mathrm{PID(z)} = \mathrm{k_p} + \mathrm{k_i}\frac{\mathrm{z}}{\mathrm{z}-1} + \mathrm{k_d}\frac{\mathrm{z}-1}{\mathrm{z}}$$

3.2.3 Design of the output voltage control loop

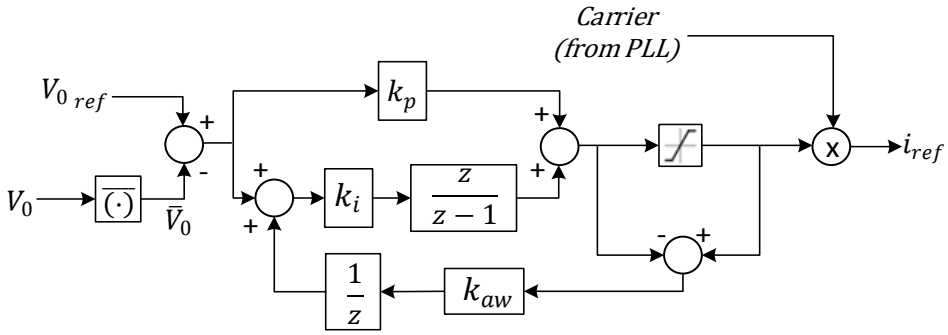


Figure 18. PID controller implemented with anti-windup in the output voltage loop.

The voltage control loop constitutes the external control loop that is responsible for regulating the voltage of the DC bus. This loop has the slowest dynamics and it is carried out by using a PI controller.

$$\mathrm{PI(z)} = \mathrm{k_p} + \mathrm{k_i}\frac{\mathrm{z}}{\mathrm{z}-1}$$

The main function of this loop is to perform a balance of real power of the global system. The input of this controller is the difference between the reference voltage and the average value (extracted with a mean value extractor) of the output voltage. The output of the controller is the required amplitude value of the grid current. This value is then multiplied by the carrier generated by the PLL, so that the result becomes the necessary, oscillating and synchronized reference of the current controller. As it was aforementioned, the voltage on the DC output can present oscillations if the grid voltage has harmonics. For this reason a comb filter has been included in the feedback of the voltage control loop to extract its average value.

Finally an anti-windup loop [7] has been added to the integral part in order to reduce the windup effect when the control is saturated. The saturation of the control variable could cause the instability of the closed-loop system in some circumstances. That is if the saturation of the duty cycle value is reached, the feedback loop is broken since the output of the saturating duty cycle is not influenced by its input. Let's now assume the output voltage reference is constant and the applied duty cycle value reaches its saturation level when having a constant charge at the output. Therefore, the error signal will be constant and the proportional part will have a constant output. The integral part instead, will have a constant value at its input. This could drift the output of the integrator to very large values. Let's now assume that the load is changed and that the output voltage level is equal to the output voltage reference, the proportional part output is zero. As the integral part value is very large, it could take a long time to recover, and this can cause the destabilization. In order to avoid this effect an anti-windup loop should be added.

Obviously, the stability of the system has to be guaranteed when the anti-windup is added. The open-loop transfer function of this new loop is given by:

$$L(z) = k_i \frac{z}{z-1}\frac{k_{aw}}{z} = \frac{k_{aw}k_i}{z-1}$$

the characteristic equation is: $d(z) = 1 + L(z) = z - 1 + k_{aw}k_i = 0$

defining the parameter $p_{aw} = 1 - k_{aw}k_i \Rightarrow k_{aw} = \frac{1-p_{aw}}{k_i}$.

Setting the closed-loop pole at $p_{aw} = 0.2 \rightarrow k_{aw} = \frac{0,8}{10T_s}$.

The anti-windup constant k_{aw} determines how fast is the integrator to recover the unsaturated state from a drift caused by a saturation state. In this case the pole p_{aw} has been configured using an empiric procedure. The anti-windup has to be at least two times faster than the external control.

3.2.4 Design of the mean value extractor

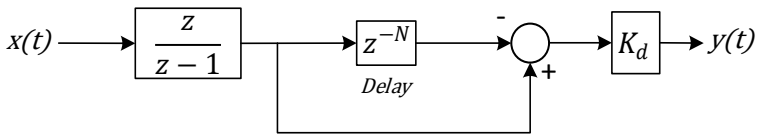


Figure 19. Mean value extractor implemented using a comb filter.

The mean value extractor consists in a comb filter capable of work with variable frequency signals. In the scheme parameter *N* is the ratio between the grid frequency and the switching frequency. The transfer function of the extractor is given by:

$$H(z) = \frac{1}{N}\sum_{k=0}^{N-1} z^{-k} = \frac{1}{N}\left(1 + z^{-1} + z^{-2} + \cdots z^{-(N-1)}\right) = \frac{1}{N}\cdot\frac{1-z^{-N}}{1-z^{-1}} = \frac{1}{N}\cdot\frac{z^N - 1}{z^N - z^{N-1}}$$

For a switching frequency $\mathrm{F_s}$ of $30kHz$ and a grid frequency $\mathrm{F_1}$ of $50Hz$:

$$N = \frac{F_s}{F_1} = \frac{30000}{50} = 600\ Samples$$

4 Simulation Results

4.1 Numeric values of the converter and control objectives

The designed bidirectional LC rectifier meets the following specifications:

- Inputs:

  – Grid voltage: 230 V ac rms.
  – Grid frequency: 50 Hz.
  – Bias voltage: 400V

- Outputs:

  – Output voltage: 800 Vdc.
  – Overload condition: 236 Ω
  – Full load condition: 256 Ω
  – Half load condition: 512 Ω
  – 10% load condition: 2560 Ω
  – Maximum output power: 2 kW.
  – Maximum input current THD: 3 %.
  – Minimum power factor of 0.99.

- Control objectives:

  –Output voltage: reference value is fixed to 800 V dc. Small oscillations in steady state, fast response and low overshoot in front of load variations.

  –Bias voltage: reference mean value is fixed to 400 V dc. Fast response and low overshoot for the mean value in front of load variations and grid voltage amplitude changes.

  –The current control used must allow good harmonic attenuation and good tracking of the fundamental (50 Hz) frequency component.

- The configuration variables of PWM are:

  $\text{Dead time, DT} = 1\ \mu\text{s},$

  $\text{Switching frequency, } F_s = 30\ \text{kHz},$

  They are obtained as:

$$u_{max} = 1 - 0{,}000001 \cdot 30000 = 0{,}97 \quad (17)$$

$$u_{min} = 1 - u_{max} = 1 - 0{,}97 = 0{,}03 \quad (18)$$

  For a correct performance of the PWM, it is must previously adjust each saturator showed in the figure 6 with the values obtained from (17) and (18) equations. It is important also to remember that the sampling frequency (30 kHz) coincides with the switching frequency used to operate the switches through PWM.

- The bias capacitor and the inductance are dimensioned according to the next procedure.

The transfer function from the control signal to the input current is

$$\frac{I(s)}{U(s)} = \frac{V_0 Cs}{CLs^2 + Crs + 1}$$

Selecting a switching frequency of $\mathrm{F_s} = 30\ \mathrm{kHz}$ the value of parameters L and C are chosen taking into account that they should be plausible and a gain of at most 20 dB is required at Fs.

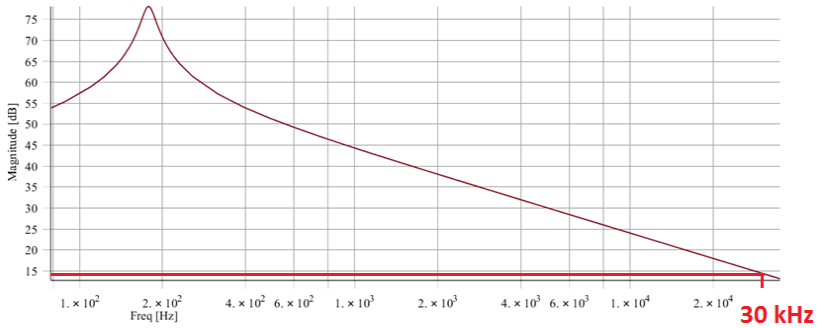


Figure 20 Bode diagram of LC boost

The selected values

$C = 2340\ \mu\mathrm{F}/450\ \mathrm{V}$

$L = 800\ \mu\mathrm{H}$

$Gain\ [\mathrm{dB}]_{F_s=30\ kHz} = 14{,}32\ \mathrm{dB}$

give a gain of 4,32 dB that is an amplification value of the fundamental component of the ripple equal to 5,24.

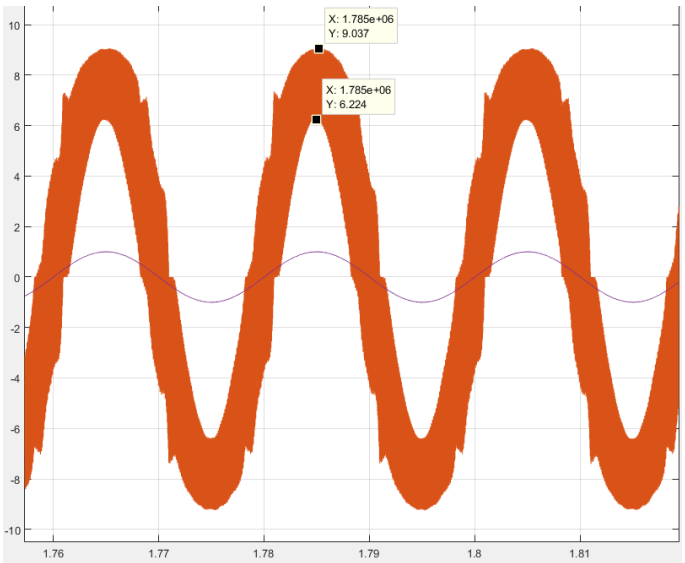


Figure 21 Current ripple of 2,88 A_{pp}

The measured value is checked with the plotted ripple value Figure 21. Using a sinusoidal control signal (u) of amplitude 0.5 the ripple has a value of 2,62 A peak to peak. Comparing this ripple value with the calculated one (2,88 A) it is observed a small difference.

The capacitance of the bias capacitor has been selected according to the maximum current that will pass through it considering that the sum of the grid voltage and the bias capacitor voltage must be always positive. To do that, the input current is assumed in phase with the grid voltage and, then, the abovementioned voltages will be in quadrature. Adding them correspondingly the maximum voltage should be lower of 450 V ($V_{c\,Max}$< 450 V) and greater than 0 V. However, to ensure the correct operation of the boost converter a minimum value of 40 V ($V_{in\,min} = 40\ V$) has been selected.

The capacitance must be large enough so that the voltage addition does not exceed 450 V (this limitation refers to the price of the capacitors) neither be less than the 40 V for the nominal input current of the converter plus an extra value to cover the transients.

Inductance, together with the bias capacitor, sets the bandwidth, of the plant current and the current ripple attenuation. Finally, an $800\ \mu H$ inductance and a $2340\ \mu F$ bias capacitor are selected for the converter.

It is important to remark that the initial charge of the bias capacitor, during the start of the converter, should be done avoiding to inverse polarize it. So, in a real setup a diode should be connected in parallel with the bias capacitor to prevent it.

The rest of relevant parameters of the system are:

–Output Capacitor: $300\ \mu F$
–Parasitic resistance of the converter: $50\ m\Omega$
–Full load: $256\ \Omega$
–Half load: $512\ \Omega$
–10% of Full load: $2560\ \Omega$

4.2 Parametric calculation of the controllers

This section adjusts all controllers with values to obtain an adequate closed-loop dynamical response.

4.2.1 PI Controller for the output voltage

The PI controller for the output voltage has been configured using the following parameters:

$$k_i = 1{,}7 \cdot 10^{-4}$$

$$k_p = 0{,}5$$

$$PI(z) = k_p + k_i \frac{z}{z-1} = \frac{0{,}5z + 0.04}{z-1}$$

This controller regulate the output voltage but, as this loop is slower, the tuning is easier to do with less iterations.

4.2.2 PID Controller for the bias voltage

The PID controller for the bias voltage has been configured using the following parameters:

$$k_d = -40{,}1$$

$$k_i = -2{,}7 \cdot 10^{-5}$$

$$k_p = -0{,}04$$

With these parameters the PID is

$$\mathrm{PID}(z) = k_p + k_i \frac{z}{z-1} + k_d \frac{z-1}{z} = \frac{-4{,}14z^2 + 80{,}24z - 40{,}1}{z^2 - z}$$

In this case, the discrete-time PID controller has been tuned empirically in the numerical simulations as its closed-loop dynamics is also quite slow.

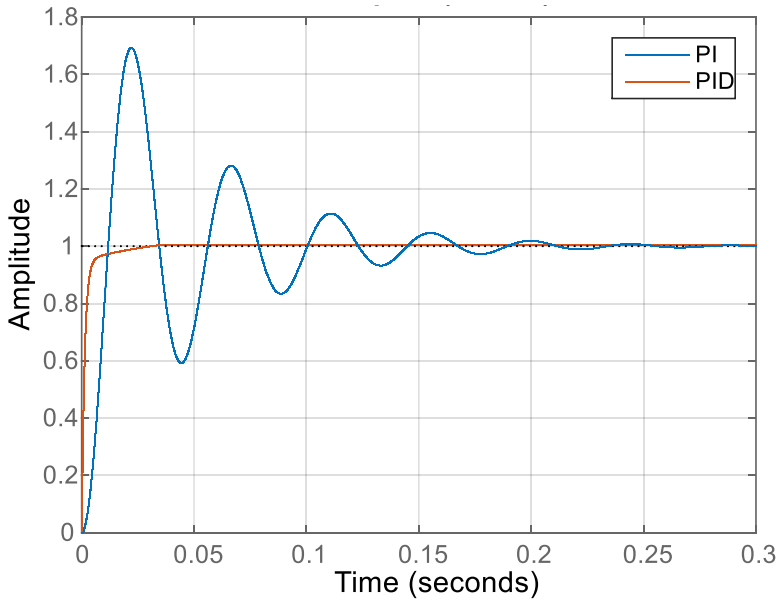


Figure 22 Comparative of the PID and PI action with an applied unitary step

In Figure 22 is shown how PID controller is faster arriving to the reference signal than a PI controller adjusted with the same gains. As a faster transient response with less overshoot is desired the derivative part is included in the final design.

4.2.3 PR Controller

The PR current controller has been configured using the parameters described in the following paragraphs.

Inner-loop controller design

As a first step, to be able to design the controller for the inner loop of the Resonator control scheme, the numerical values of the components used (that appear in Section 4.1), are substituted into next transfer function, obtaining

$$Gi(s) = \frac{1}{Ls + r} = \frac{1}{0.0008s + 0.00005}$$

The transfer function presented in the previous equation is a first-order transfer function. It would be convenient to make the controller design directly in the z-domain so $Gi(s)$ must be converted to a discrete-time model. The next equation shows the conversion result into the z-domain, by using a sampling frequency of Fs = 30 kHz and a ZOH,

,

$$Giz(z) = \frac{1}{z} \cdot Gi(z) = \frac{1}{z} \cdot \frac{0{,}04162}{z - 0{,}9979} = \frac{0{,}04162z}{z^2 - 0{,}9979z}$$

To stabilize the plant and attenuate the high frequency content of the control signal the following low pass filter, with a cut frequency of 500 Hz, is selected.

$$Ci(z) = \frac{0{,}05z + 0.05}{z - 0{,}9}$$

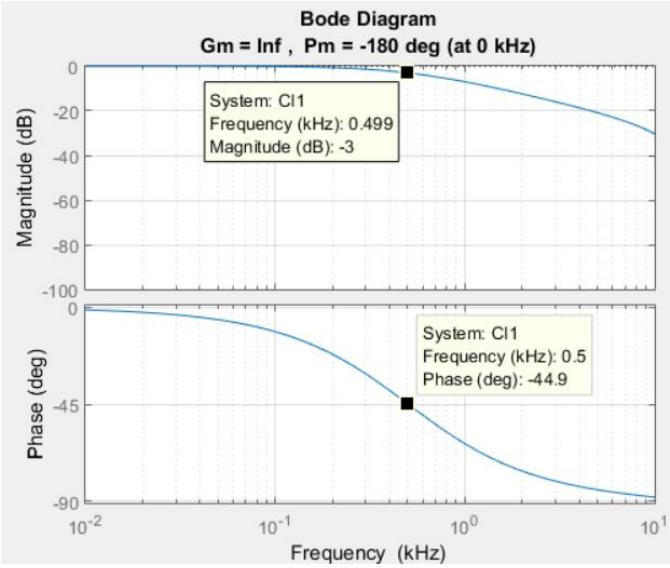


Figure 23 Bode plot of the LPF Ci(z)

Then, the open-loop transfer function of the inner loop is

$$L(z) = Giz(z) \cdot Ci(z) = \frac{0{,}002081z + 0{,}002081}{z^3 - 1{,}898z^2 + 0{,}8981z}$$

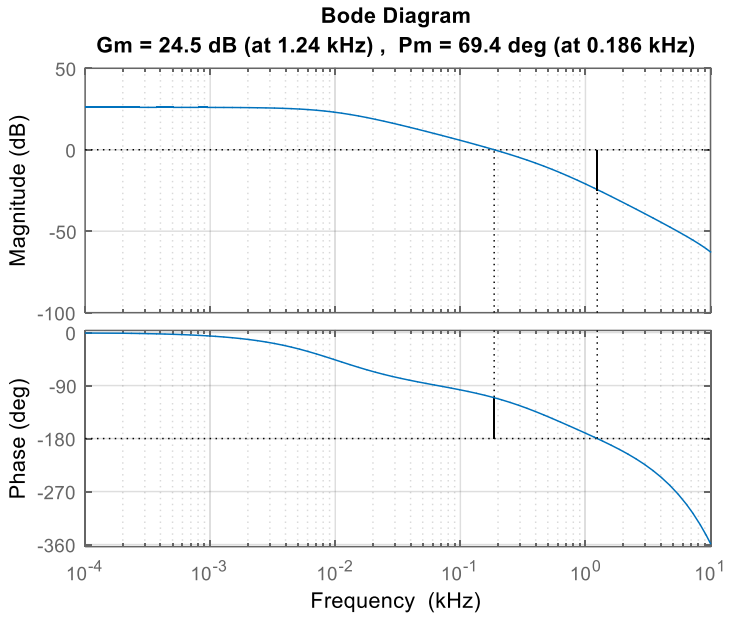


Figure 24 Bode plot of open-loop L(z)

The Bode plot for the open-loop transfer function is shown in Figure 24. As it can be observed, this design presents a gain margin of 24,5 dB at 1,24 kHz, and a phase margin of 69.4º at 186 Hz.

Having found an inner-loop controller, the inner control loop is closed giving, therefore, the closed-loop transfer function P(z):

$$P(z) = \frac{L(z)}{1 + L(z)} = \frac{0{,}002081z + 0{,}002081}{z^3 - 1{,}898z^2 + 0{,}9002z + 0{,}002081z}$$

$\mathrm{P(z)}$ acts as the new plant to be controlled by the PR control loop explained next paragraphs.

Resonators-loop controller design

The design of the resonators-loop controller consist mainly in adjusting 2 sets of parameters: $\mathrm{g_k}$ and φ_k.

The parameters $\mathrm{g_k}$ have been chosen by using the hyperbolic profile $g_k = 1{,}5 \cdot 10^{-2} \cdot \frac{1}{\mathrm{k}}$ This profile gives more gain to the low frequencies and less gain to the high frequencies. This shape allows the control system to provide the control signal highest energy levels to the region of the fundamental frequency and the lower harmonics where the highest levels of disturbance are usually located.

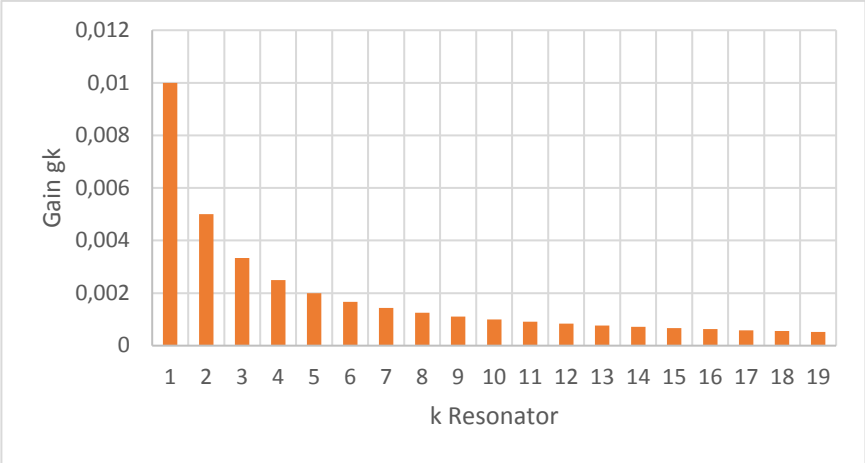


Figure 25 Contribution of g_k parameter within each resonator

The phase shift of the resonator $R_k(z)$ at the ω_k frequency will be $-\varphi_k$. A selection of $\varphi_k = P(z_k)$ wit $z_k = e^{j\omega_k T_s}$ will cause the resonator open-loop transfer function to center all the phase shifts, at the fundamental frequency and its harmonics, around 0º and, therefore, it will provide the system with a high level of robustness.

The parameters used on each resonator, according to the equation

$$R(z) = \sum_{k=1}^{n} R_k(z) = \sum_{k=1}^{n} g_k \frac{cos(\varphi_k)z^2 - cos(\omega_k T_s + \varphi_k)\, z}{z^2 - 2\, cos(\omega_k T_s)\, z + 1}$$

are presented in Table 1. The closed-loop system shows gain and phase margins with good values while keeping good attenuation at the desired harmonic frequencies.

k Resonator	fk [Hz]	ωk[rad/s]	gk	ϕk [rad]
1	50	2π50	0,01	-0,24628698
2	100	2π100	0,005	-0,50047343
3	150	2π150	0,00333333	-0,76657265
4	200	2π200	0,0025	-1,0410516
5	250	2π250	0,002	-1,31211519
6	300	2π300	0,00166667	-1,56473346
7	350	2π350	0,00142857	-1,78811499
8	400	2π400	0,00125	-1,97895257
9	450	2π450	0,00111111	-2,13954284
10	500	2π500	0,001	-2,27456209
11	550	2π550	0,00090909	-2,38893043
12	600	2π600	0,00083333	-2,48691913
13	650	2π650	0,00076923	-2,57195407
14	700	2π700	0,00071429	-2,64669438
15	750	2π750	0,00066667	-2,71318215
16	800	2π800	0,000625	-2,77298634
17	850	2π850	0,00058824	-2,8273198
18	900	2π900	0,00055556	-2,87712842
19	950	2π950	0,00052632	-2,92315735

Table 1 Resonators control loop (R(z)) - parameters used on the resonators

As it can be observed in the next figure, there are 19 resonant peaks at 50 Hz and its harmonics. The phase shifts are all centered at 0º, which guarantees the maximum phase margin in the system, see Figures 26 and 27

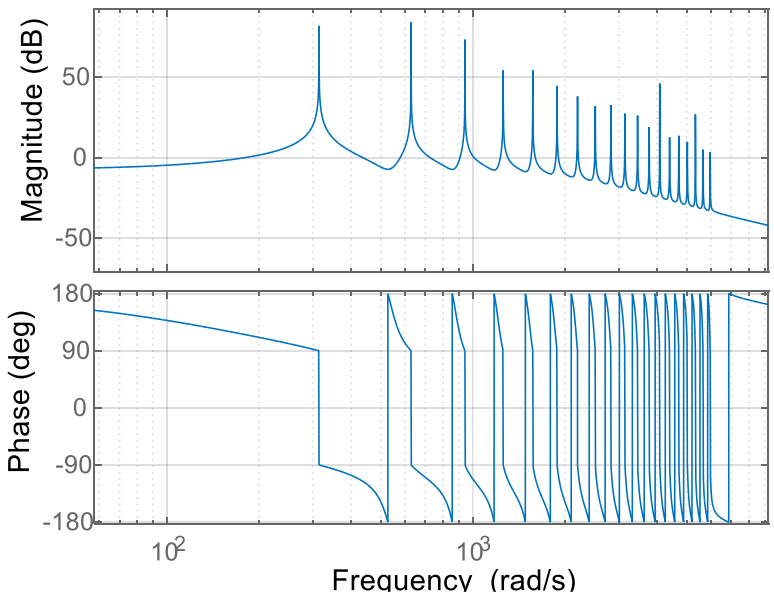


Figure 26 Bode plot of the R(z) open-loop transfer function current control

The Bode plot of the closed-loop transfer function of the system

$$T(z) = \frac{R(z)P(z)}{1 + R(z)P(z)}$$

is shown in Figure 28:

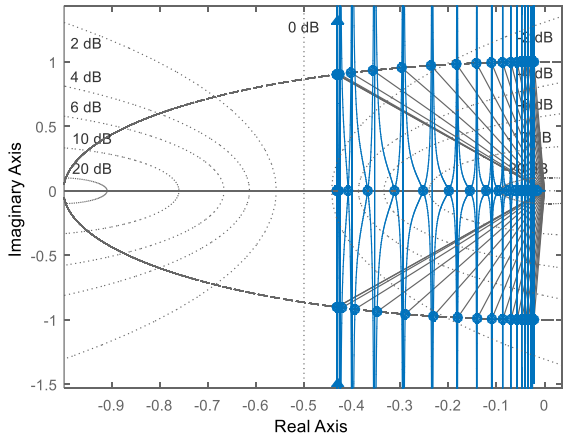


Figure 27 Nyquist plot of the open-loop transfer function of the system

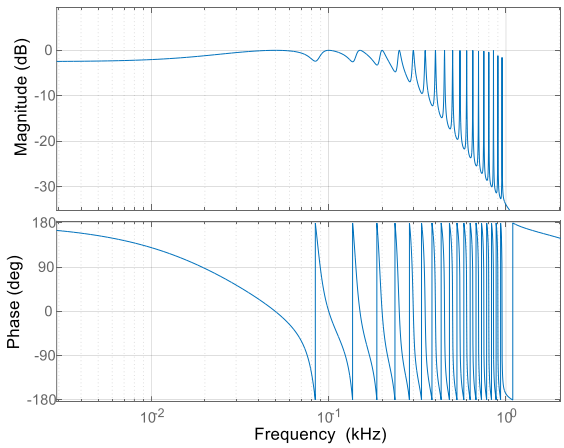


Figure 28 Bode plot of the closed-loop transfer function of the system.

The absolute value of the maximum pole in the closed-loop transfer function is 0,999971. It is important to remark that, in the Nyquist plot, the minimum distance to -1 of the polar plot is 0,5708.

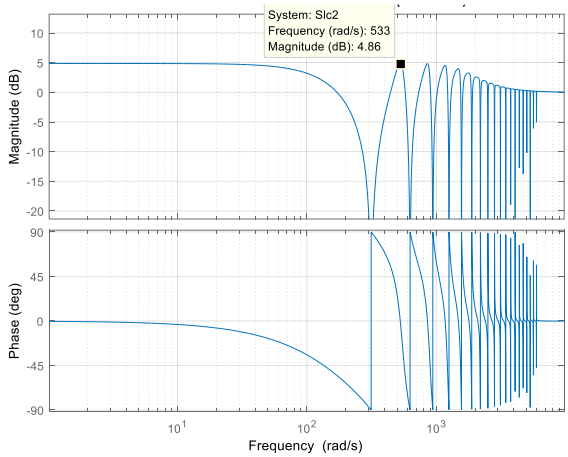


Figure 29 Bode plot of the sensitivity transfer function

The infinity norm of the sensitivity transfer function of the system (Figure 29) shows also how of far it is the polar plot from -1 (it is the inverse). In this case $||\boldsymbol{S_2(z)}||_\infty = \mathbf{4,87\ dB}$. The peaks with negative gains correspond to the fundamental frequency and its harmonics where the resonators are placed.

$$S_{AFC}(z) = \frac{1}{1 + R(z)P(z)}$$

4.3 Antialiasing Filter of the ADC

This filter is used within conditioning block for simulate the analog filters implemented before a real ADC. The cut-off frequency (f_h) is adjusted to 2500 Hz to attenuate the high frequency noise and to reduce the aliasing. The implemented filter is the continuous-time first-order transfer function

.

$$H(s) = \frac{1}{\tau s + 1}$$

$$\omega_o = \frac{1}{\tau} = 2\pi f_h$$

4.4 Pre-charging

This section describes the procedure to pre-charge the converter before the start of the operation of the control loop. To do this, the following procedure should be carried out: turn on the converter with a pre-charge resistor (5 Ω) and no load, as the switches are open the output capacitor is charged through the antiparallel diodes of the boost converter leg; the bias capacitor also charges but to prevent reverse polarize it a diode is connected in parallel with it; finally, when the voltages arrive to steady state the pre-charge resistor is short-circuited and the controller, and the PWM, start their operation closing the loop to the converter.

It is worth to note that the bias capacitor parallel will be always in non-conducting mode in the normal operation of the converter as the voltage of the bias capacitor is always positive

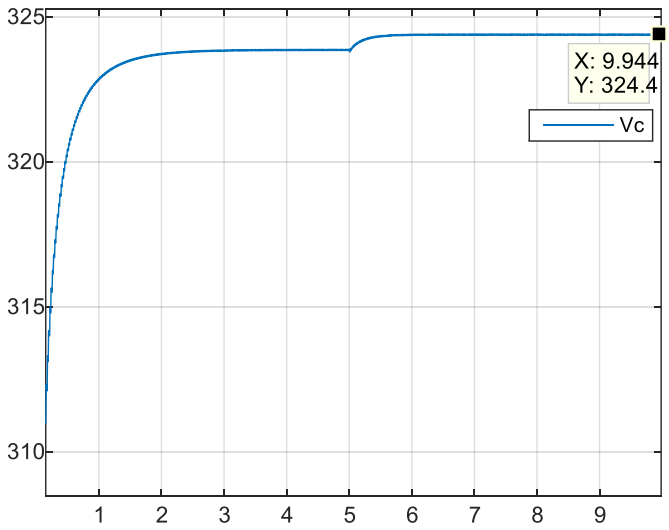


Figure 30 Finding the steady state of bias voltage. Scales[Y:volts ,X: seconds]

Figure 30 shows how the bias capacitor voltage arrives to 324,4 V according to the maximum voltage of the grid $V_p = V_g\sqrt{2} - V_d$=$230\sqrt{2} - 0.6 = 324{,}4V$.

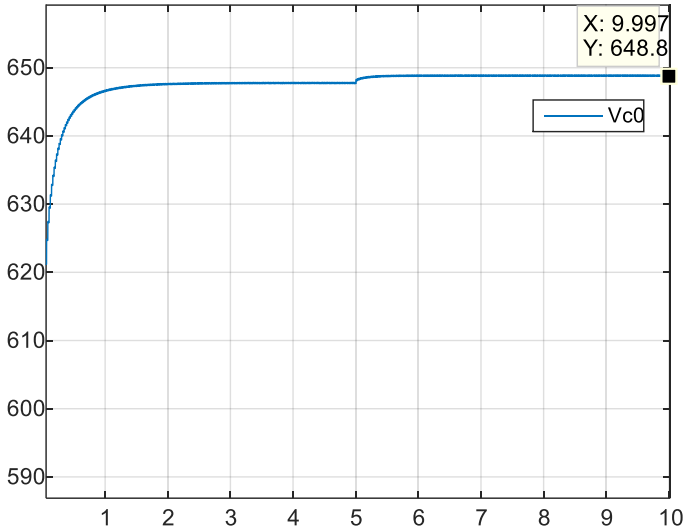


Figure 31 Finding the steady state of output voltage .Scales[Y:volts ,X:seconds]

Figure 31 shows how the output capacitor voltage arrives to 648,8 V. Both values will be used to adjust initial conditions in the numerical simulations.

4.5 Development of the auxiliary blocs for the simulation

4.5.1 Design of harmonics sources

$$\sum_{n=1}^{k} A_n \sin(n \cdot 2\pi F_r t + \varphi_n)$$

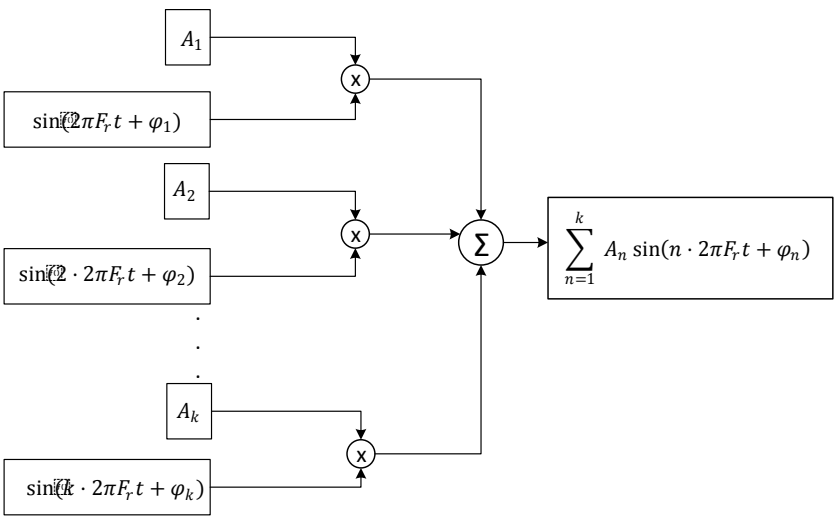


Figure 32 Harmonics generator algorithm with variable amplitudes, phases and frequencies.

In the simulator, to test the robustness of the resonators, a signal generator with harmonic content of different frequencies has been implemented.

This generator has been used to create the standard IEC77A class1 voltage that appears in the equation

$$v(t)_{\text{IEC77A}} = A_1 \sin(2\pi F_r t) + 0{,}08A_1 \sin(3 \cdot 2\pi F_r t) + 0{,}09A_1 \sin(5 \cdot 2\pi F_r t) + 0{,}05A_1 \sin(7 \cdot 2\pi F_r t) + 0.02A_1 \sin(11 \cdot 2\pi F_r t) + 0.02A_1 \sin(13 \cdot 2\pi F_r t)$$

The total harmonic distortion of IEC77A class1 voltage is 12,4%.

4.5.2 Design of THD measurements block

The quality of the current signal is measured by means of the Total Harmonic Distortion (THD). The equation that defines this quality indicator is

$$\text{THD}_{\text{RMS}} = \sqrt{\frac{I_{rms}^2 - I_0^2 - I_1^2}{I_{rms}^2}} = \sqrt{\frac{\sum_{k=2}^{\infty} I_k^2}{I_{rms}^2}} \tag{27}$$

A new measurement block to compute the THD with variable frequency has been coded. Obviously, the output of the block is only meaningful when the frequency has stopped is variation but it allows to test the THD in the experiments with stepped frequency variations.

The measured THD is respect to the RMS value of the signal thus giving an output in the range [0,1]. Another possibility with an infinite output range will be to compute the THD with respect to the fundamental content of the signal.

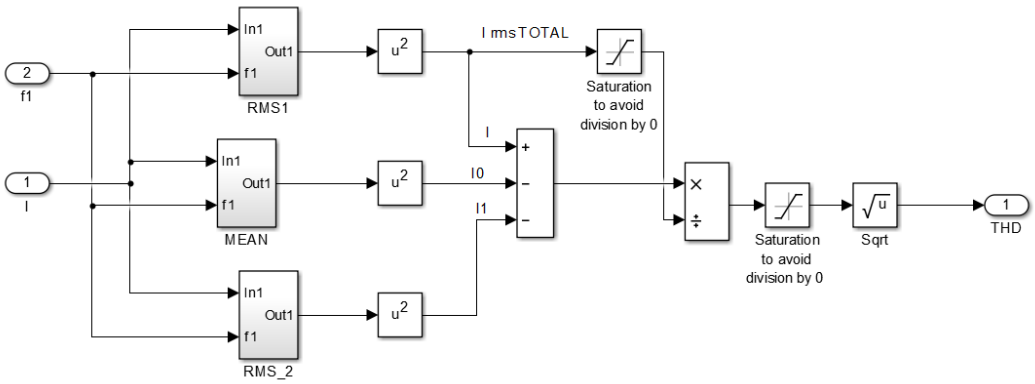


Figure 33 Block diagram for calculating the THD

In Figure 33 the harmonic component at the fundamental frequency is obtained from the RMS_2 block where 2 AM modulators move the fundamental component to zero frequency and, then, the mean value is calculated.

4.5.3 Design of power factor measurement block

This section explains the design of the power factor measurement blocks that are used in the simulations. Two types of regimes need to be distinguished in the calculation of the power factor:

Periodic regime (pure sinusoidal)

The following formulas are only valid assuming that the periodical regime is pure sinusoidal. We have that the apparent power is

$$S = V_{rms} \cdot I_{rms}$$

and the active power is the rms value of the voltage multiplied by the rms value of the current and multiplied by the cosine of phi (the angle between the voltage and current phasors):

$$P = V_{rms} \cdot I_{rms} \cdot \cos(\varphi)$$

So, the power factor is

$$PF = \frac{P}{S} = \cos(\varphi)$$

Besides, the reactive power is

$$Q = \sqrt{S^2 - P^2}\ .$$

General periodic regime (periodic non-sinusoidal)

In the case of a general periodic non-sinusoidal regime the previous equations can not be applied. The apparent power remain, as previously, as the product of the rms values of the voltage and the current at the port. This values are calculated as the average of the square of the signals over one period:

$$S_{rms}(t) = \sqrt{\frac{1}{T}\int_{t-T}^{t} v_r(\tau)^2 d\tau} \cdot \sqrt{\frac{1}{T}\int_{t-T}^{t} i(\tau)^2 d\tau}$$

The active power is the average, over one period, of the product of the voltage and the current at the port.

$$\bar{P}(t) = \frac{1}{T}\int_{t-T}^{t} v_r(\tau) i(\tau) d\tau$$

Then, the power factor to be used in the tests is computed as the division of the active power by the apparent power.

$$\mathrm{PF} = \frac{\bar{P}(t)}{S_{rms}(t)}$$

In this general case, it has no sense to talk about reactive power

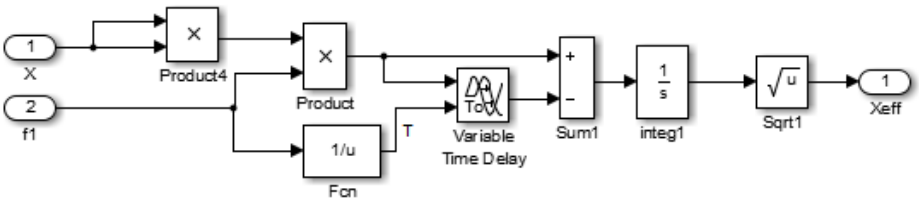


Figure 34 Block diagram implemented for the rms calculation

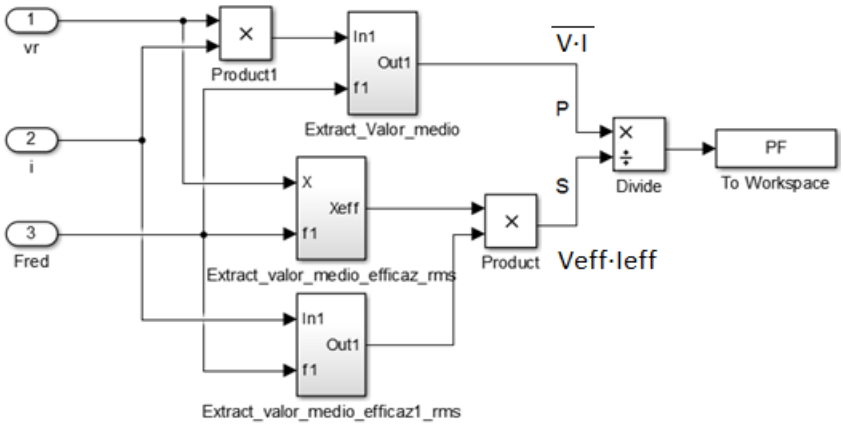


Figure 35 Block diagram for computing the power factor

4.6 Average model simulations

The designed discrete-time controller is tested in simulation firstly with an averaged model of the converter. This section shows some of the obtained results.

4.6.1 Full Load

Figure 36 shows how the current is in phase with the reference current and, then, with the grid voltage. Zooming the curves, a slight phase shift of one sampling period can be seen that is due to the computational delay of the control algorithm. Besides, an apparent low-level offset can be observed but, in fact, it is created by the small even harmonic content of the current. Figure 37 shows a moderate overshoot, not reaching 450 V, in the bias capacitor voltage.

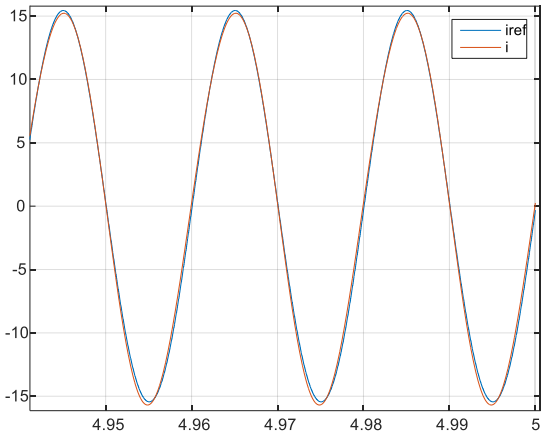


Figure 36 Reference current (blue) and measured current (red). Scales [Y: Amps ,X: seconds].

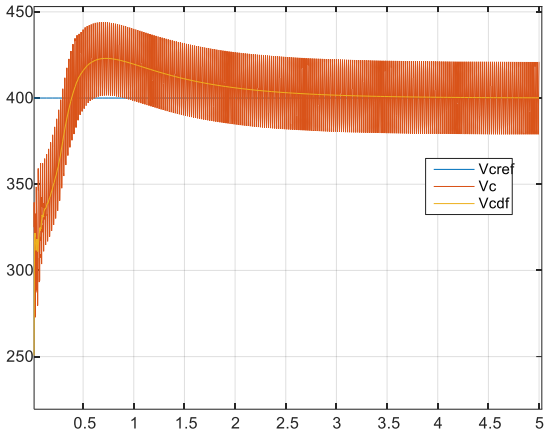


Figure 37 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

Figure 38 shows how the output voltage reference, measured and measured mean value. When the converter starts.

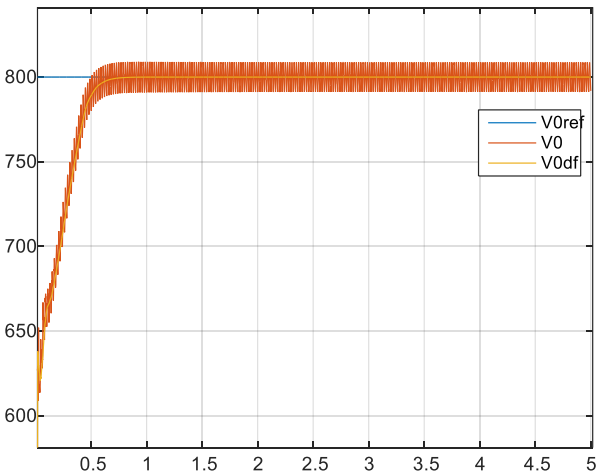


Figure 38 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y : volts, X: seconds].

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$
445	810	16

Table 2 Measurements of overvoltages and overcurrent

4.6.2 Load variations

In this test, the load is varied from full load to no load and, then, to full load again.

In the plots of Figures 39, 40 and 41 can be observed the behaviour of the input current, the bias voltage and the output voltage when the converter stars (with load) and in the transitions from full load to no load and vice versa. An overshoot of 825 V is observed in V_0 when the converter load pass from full to no load but this is the most unfavourable situation for the output voltage. During this transient, if a zoom is done in the input current, it can be observed that the converter returns power to the grid.

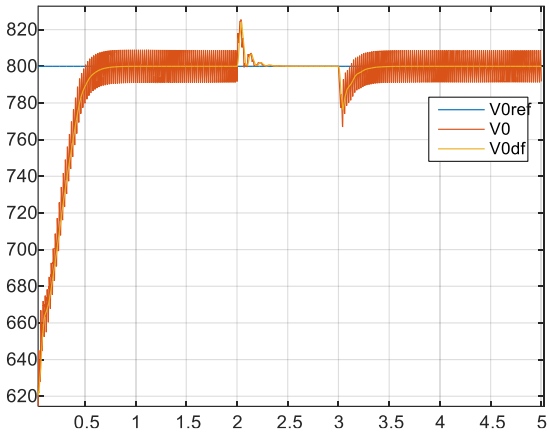


Figure 39 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

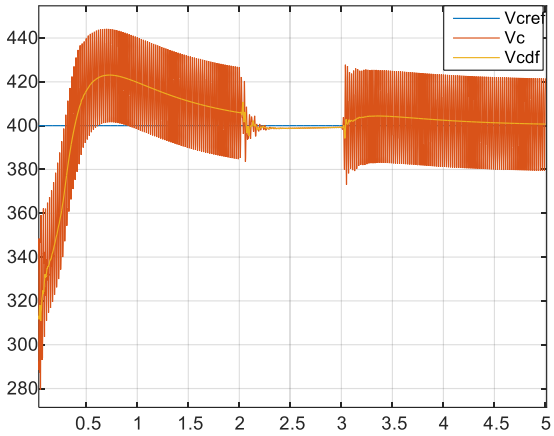


Figure 40 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

Figure 42 shows a zoom corresponding to the evolution of the current in the no load to full load transition. As it can be seen, the current reaches amplitude values close to the steady state in a few cycles.

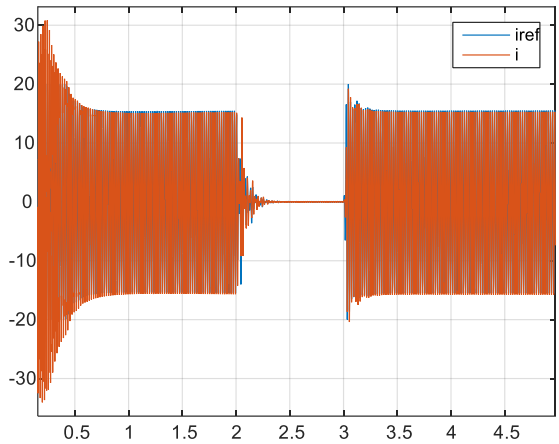


Figure 41 Current: reference (blue) and measured (red). Scales [Y: Amps, X: seconds].

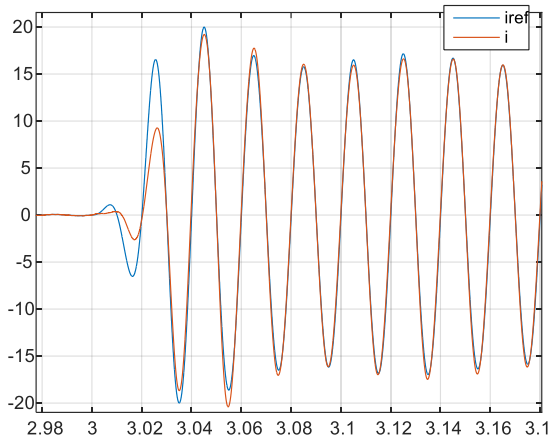


Figure 42 Zoom in Figure 41 during transition No load→Full Load.

4.7 Switched model simulations

Simulink allows the simulation of control systems, working on switching power converters by allowing the user to employ a combination of mathematical blocks simultaneously with electrical switching devices such as diodes, IGBTs, MOSFETs, BJTs, etc. This characteristic lets the designer to test control algorithms over the switched system, instead of using the averaged model, reflecting in a better way the expected behaviour of the closed-loop system under test.

4.7.1 Full load steady state

In this test the interesting thing is to observe the behaviour when the converter is working at full load, which will be the reference case to compare with it the following tests whose working conditions will be different.

The V_0 follows the reference in the start up (ramp reference) with an overshoot of 3%. The current is in phase with the carrier provided by the PLL that is a sinusoidal signal in phase with the fundamental component of the grid voltage.

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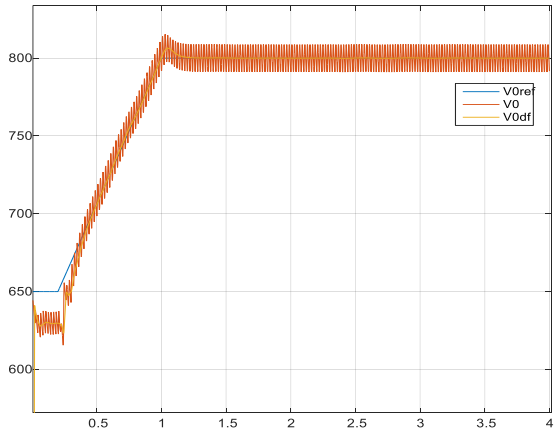

Figure 43 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

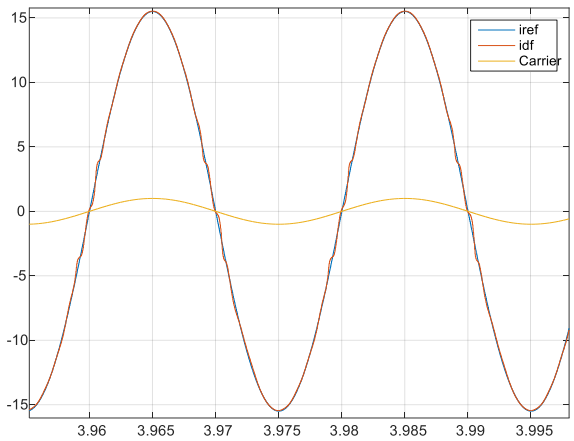

Figure 44 Input current: reference (blue), measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

The bias voltage dynamics suffer from a transient slightly longer than the output voltage dynamics. Figure 46 shows the apparent, active and reactive powers.

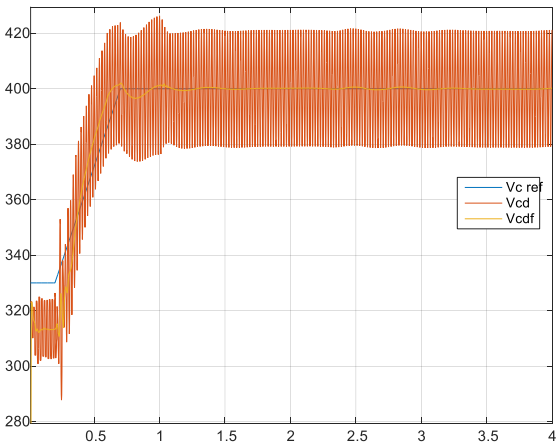

Figure 45 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

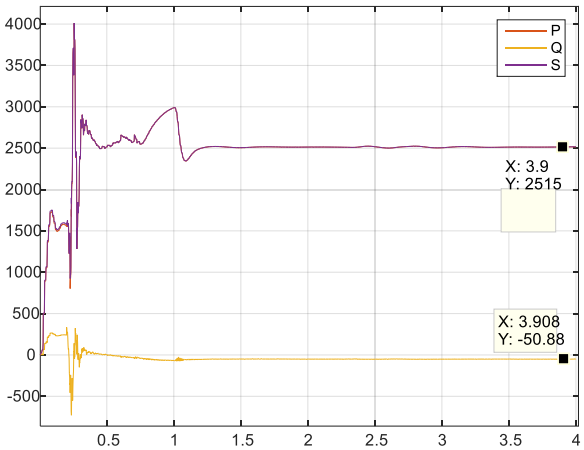

Figure 46 Active power (red), reactive power (yellow) and apparent power (violet). Scales [Y: Watts, Volt-Amps, X: seconds].

In this test a current THD of 2,21% and the PF of 99.38% has been obtained. These values are significant because they will be the reference values of correct performance to compare the other experiments.

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$	THD[%]	PF[%]
425	815	16	2,21	99,38

Table 3 Measurements of overshoots, PF and THD

4.7.2 Half-load steady state

The same test as in the previous section, but instead of working under full load, it is working at half load. A more relaxed dynamic is observed, with less overshoot, with a shorter transient and, especially, with a lower ripple in the case of V_0 and V_c compared with full load condition. This fact comes from the lower amplitude input current of the converter.

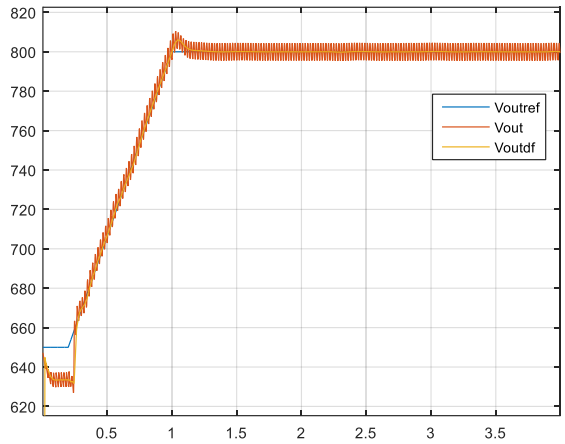

Figure 47 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

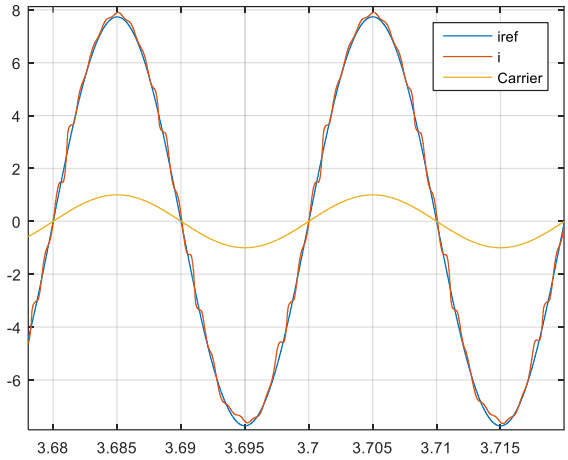

Figure 48 Input current: reference (blue), measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

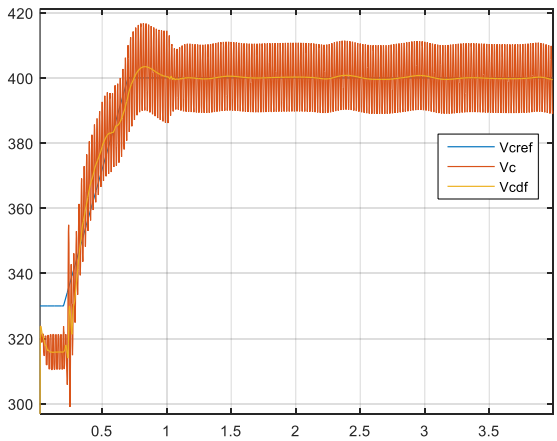

Figure 49 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

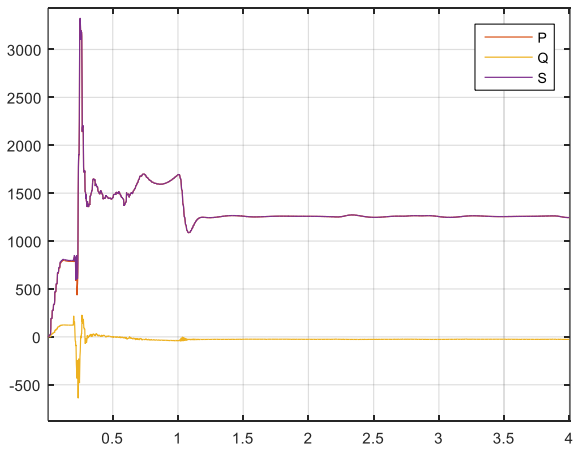

Figure 50 Active power (red), reactive power (yellow) and apparent power (violet). Scales [Y: Watts, Volt-Amps, X: seconds].

The power is obviously halved and the current THD is 2,53%. It is observed that converter working at half load generates a bit more distortion in the input current compared to the full load condition. The power factor is 98,68%. A slightly lower value than the corresponding one at full load.

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$	THD[%]	PF[%]
415	815	7,7	2,53	98,68

Table 4 Measurements of overshoots, PF and THD

4.7.3 DC load variations

$V_c^{ov}[V]$	$t_c^{ss}[s]$	$V_0^{ov}[V]$	$t_0^{ss}[s]$	$i_p[A]$	THD[%]	PF[%]
437	0,2	765	0,2-0,7	15,5	2,82	98,18

Table 5 Measurements of overshoots, steady state duration, PF and THD

This test consists of the following load variations from small load to overload condition to small load. Those changes are applied each 2 seconds.

When the first load change (10% to 110% load) is applied, the control loops act quickly and stabilize the variables in a short period of time. During the second load change (110% to 10% load) the variables stabilize more slowly and, in this case, the envelope of the current can reach a peak value of ±25A. The apparent power is about 2750 VA. A current THD of 2,82% is obtained. The obtained power factor is 98.18%.

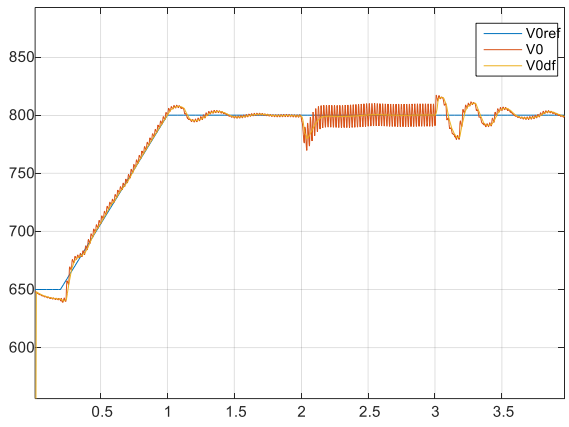

Figure 51 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

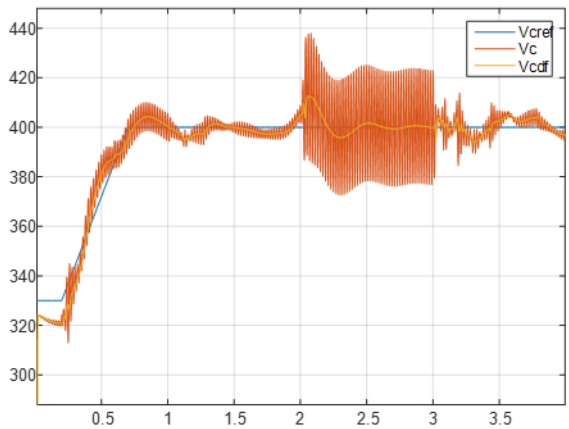

Figure 51 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

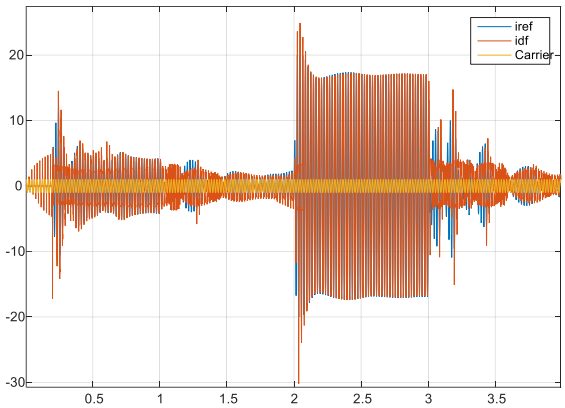

Figure 52 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

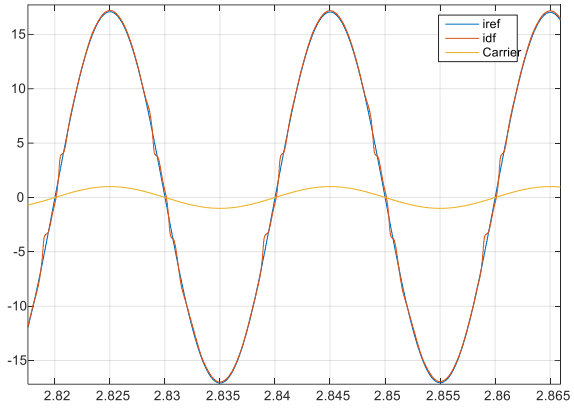

Figure 53 Zoom in Figure 53

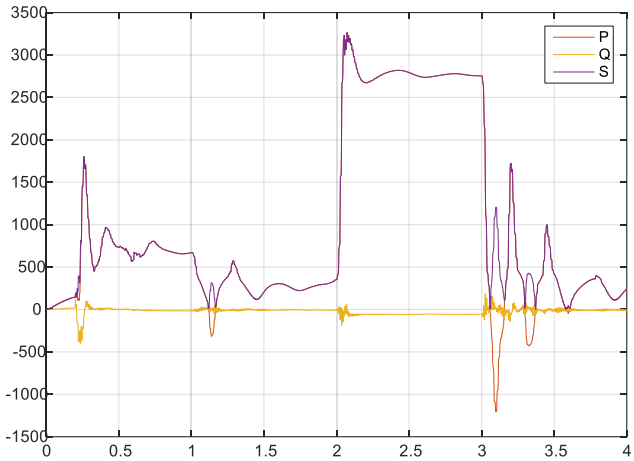

Figure 54 Active power (red), reactive power(yellow) and apparent power (violet). Scales [Y: Watts, Volt-Amps, X: seconds].

When changing from full load to small load condition (time = 3 s), it is observed that there is a peak of about -1250 W of active power. This shows that during this transient the current is flowing to the grid.

4.7.4 Grid voltage amplitude variations

In these tests the amplitude of the grid voltage changes with a more or less percentage and this change can have different durations in time.

4.7.4.1 Swells

This test consists in increasing a 20% the amplitude of the grid voltage with a duration of 4 grid periods in half-load condition.

Applying this disturbance, the control loop of the output voltage acts quickly reaching the steady state in less than 250 ms, the control loop of bias voltage is stabilized in 150 ms, and the current loop reaches the reference in 100 ms.

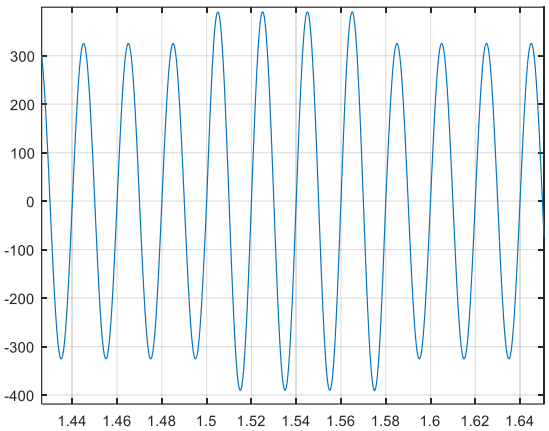

Figure 55 Grid voltage Scales[Y: volts, X: seconds]

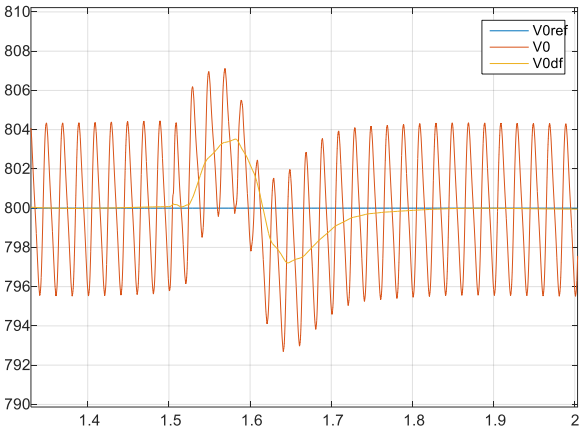

Figure 56 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

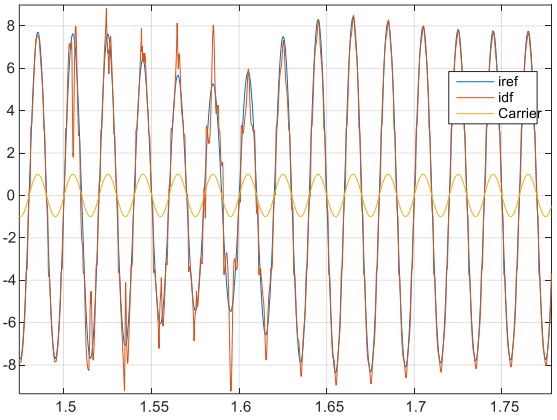

Figure 57 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

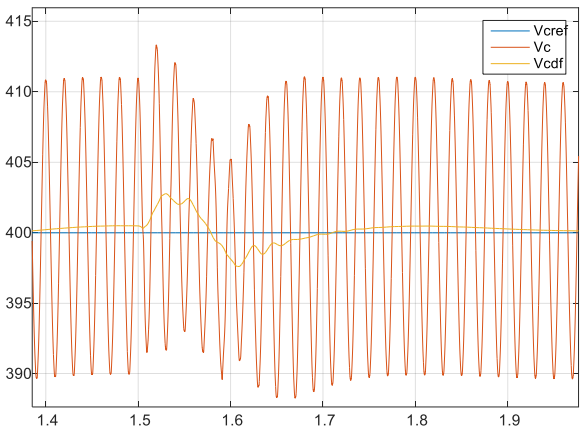

Figure 58 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

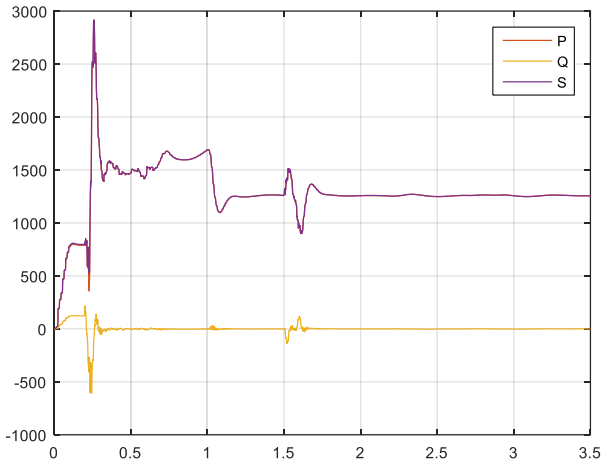

Figure 59 Active power (red), reactive power (yellow) and apparent power(violet). Scales [Y: Watts, Volt-Amps, X: seconds].

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$
[413-388]	[807-793]	8,5

Table 6 Measurements of overshoots.

4.7.4.2 Sags

In this test, with half load condition, a temporal 60% drop in the grid voltage during 4 mains periods is applied. The result is good because the output voltage controller acts relatively quickly and gives a moderate overshoot of 815 V, without decreasing more than 775 V and it stabilizes in the 300 ms. For the bias capacitor, it reaches about 426 V which does not exceed the maximum voltage allowed (450 V).

The current loop control acts quickly because in 150 ms the envelope recovers the reference level and is always in phase with the carrier signal..

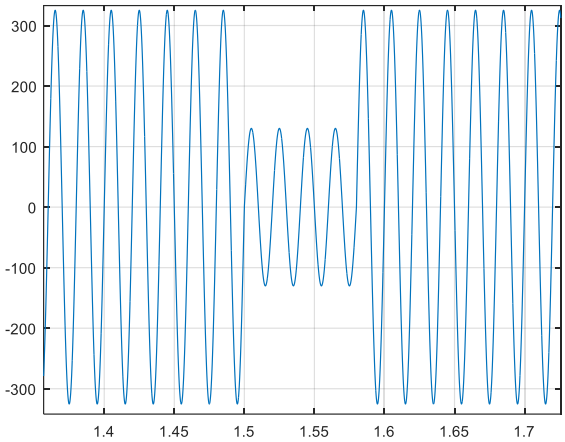

Figure 60 Grid voltage. Scales[Y: volts, X: seconds]

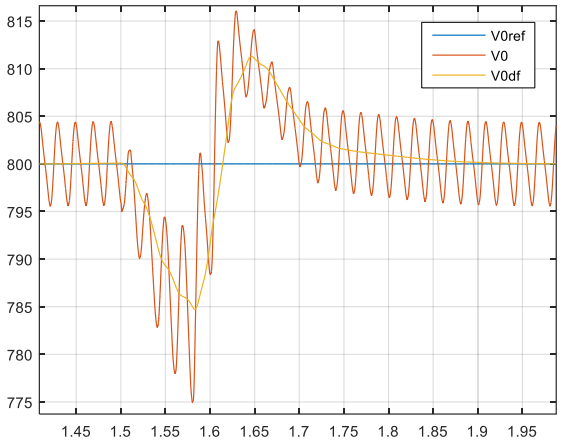

Figure 61 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

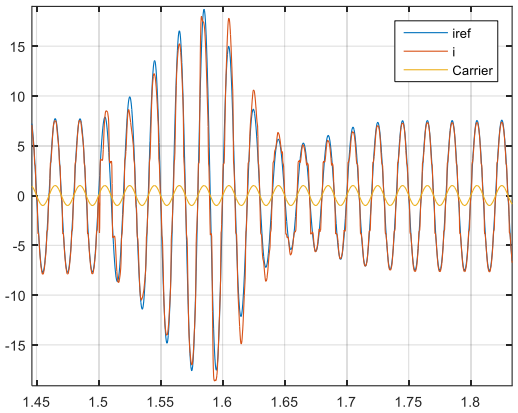

Figure 62 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

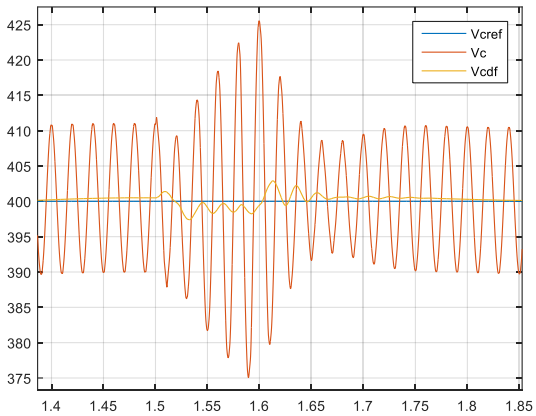

Figure 63 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

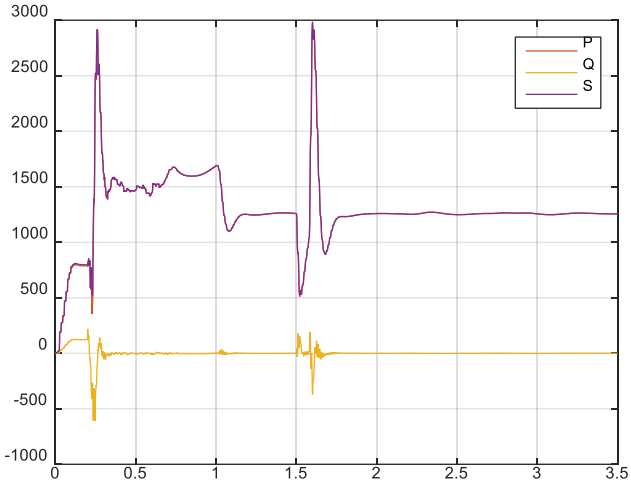

Figure 64 Active power (red), reactive power (yellow) and apparent power (violet). Scales [Y: Watts, Volt-Amps, X: seconds].

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$
425-375	816-775	19

Table 7 Measurements of overshoots.

4.7.4.3 Voltage interruption

This test is similar to the previous one but this time with a total voltage drop (the grid voltage value is zero) during 3 grid periods and half load at the output. The result obtained is that output voltage drops down to 760 V and, when the grid voltage returns, it has an overshoot of about 10 V. The current also increases, always in phase, to try to compensate this anomaly but this effort is futile as no power is drain from the grid. The bias voltage reaches a value of about 430 V. In summary: all the control loops act quickly returning the controlled variables to the corresponding reference levels when the disturbance disappears.

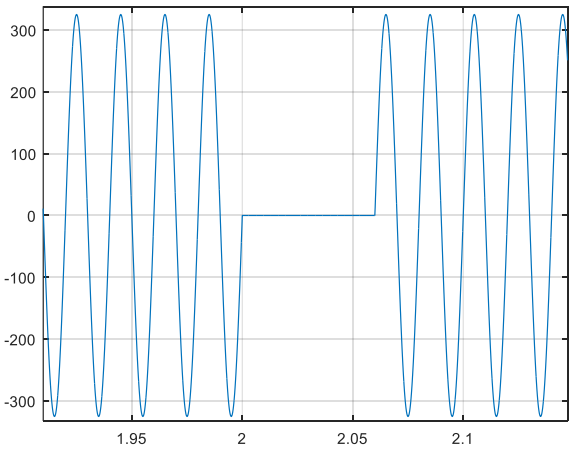

Figure 65 Grid voltage. Scales[Y: volts, X: seconds]

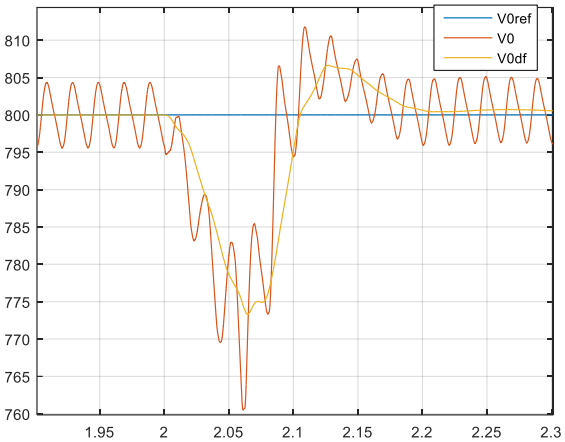

Figure 66 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

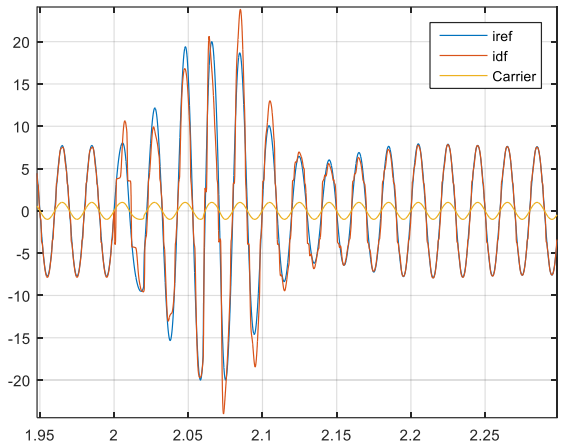

Figure 67 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

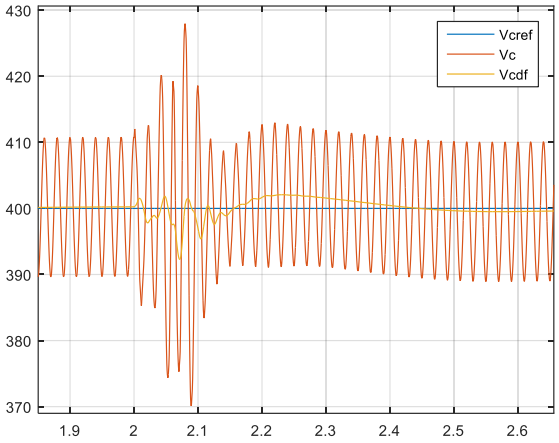

Figure 68 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

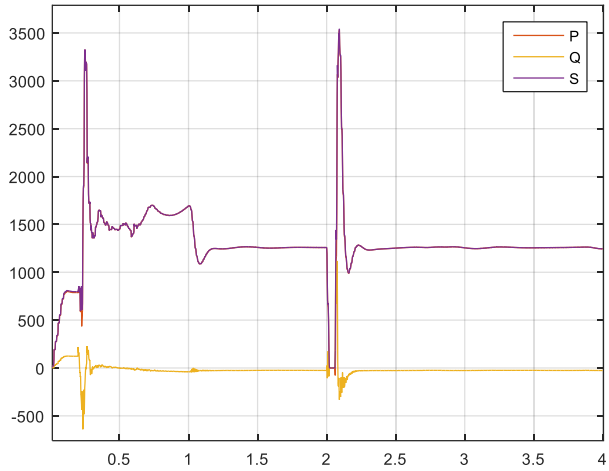

Figure 69 Active power (red), reactive power (yellow) and apparent power (violet). Scales [Y: Watts, Volt-Amps, X: seconds].

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$
427-370	761-812	25

Table 8 Measurements of overshoots

4.7.4.4 Continuous swell

This particular test has been carried out to check if the controller finally corrects the voltages and the input current if the disturbance was permanent. In the previous tests, it was not possible to check if the system finally returned to its reference value, in disturbed condition, because it recovered normal conditions.

Basically, the test consists of applying permanent overvoltage in the grid in time 2 seconds with half load. In a test carried out with a 20% overvoltage, the system ended up suffering a marginal stability with oscillatory tendencies in the voltages and current envelope. This happened because the system no longer meets the requirement of positive input voltage at the input of the boost converter. This situation forced us to reduce this percentage to 10%. The results obtained are not so good compared with the short swell. The envelope suffers a slight oscillation but it is practically negligible. As it can be observed, the output voltage envelope is quite stable. This behaviour is also observed in the input current that has a THD of 3,4%. Besides, the power factor is around 97,5%.

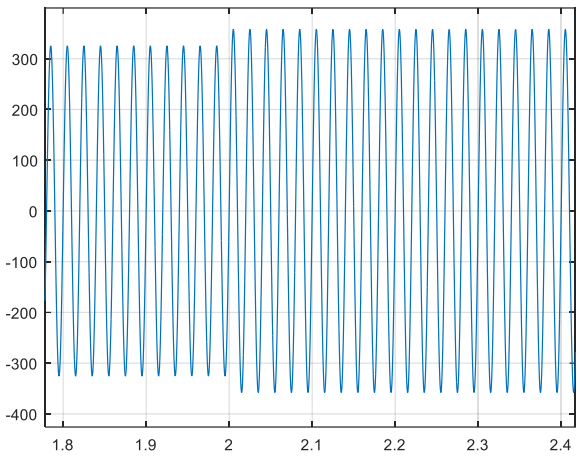

Figure 70 Grid voltage. Scales [Y: volts, X: seconds].

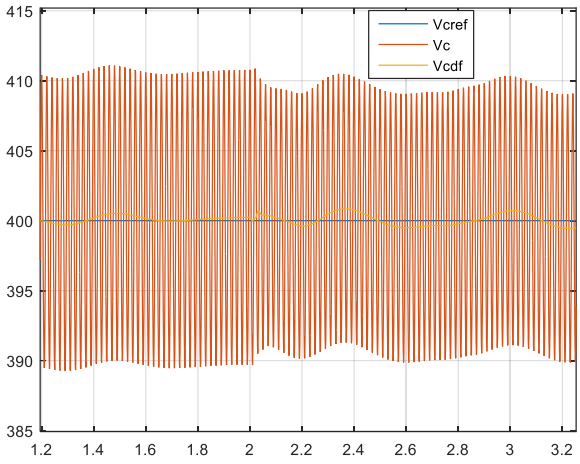

Figure 71 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

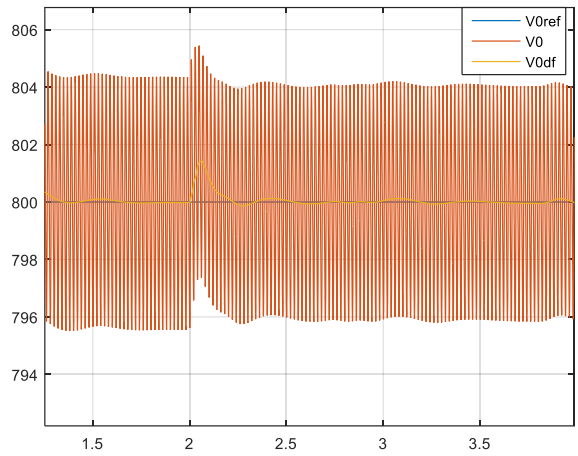

Figure 72 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

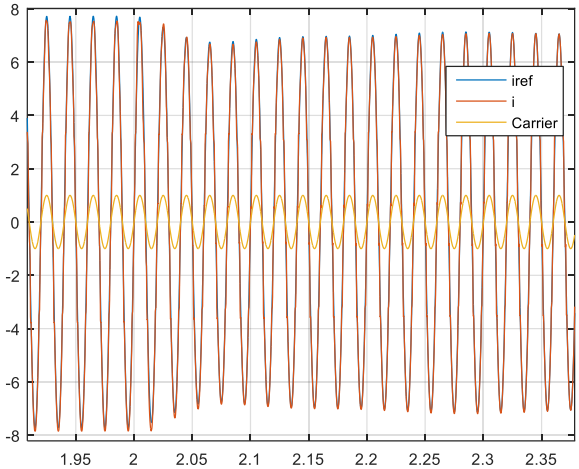

Figure 73 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

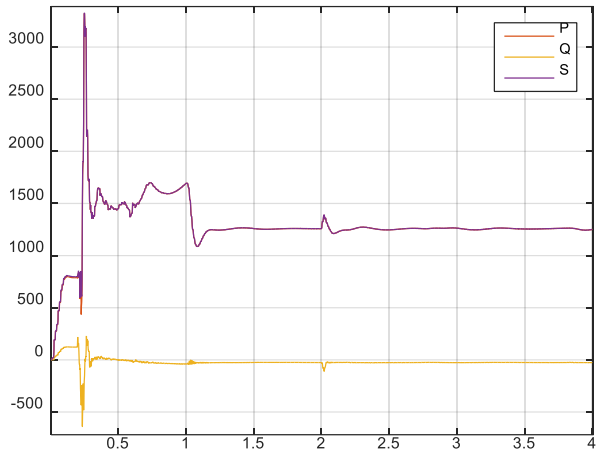

Figure 74 Active power (red), reactive power (yellow) and apparent power (violet). Scales [Y: Watts, Volt-Amps, X: seconds].

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$	THD[%]	PF[%]
411-393	805-797	7	3,4	97,46

Table 9 Measurements of overshoots, PF and THD.

4.7.4.5 Continuous sag

This test is carry out applying a permanent sag of 60% in the grid with half load condition. The output voltage recovers to reference value in 0.8 s without any overshoot, basically because the dynamics of this loop is quite slow. It is worth to remark that the ripple in the output voltage and the bias voltage increases due to greater amplitude of the input current during the sag.

The amplitude of the input current is grows from 7,5 A to 20 A (peak). During the transient, the apparent power fall from 1250VA to 500VA but it recovers the appropriate value in steady state. When the system is in this last situation, the power factor is 97,3% and the input current THD is 3,7%.

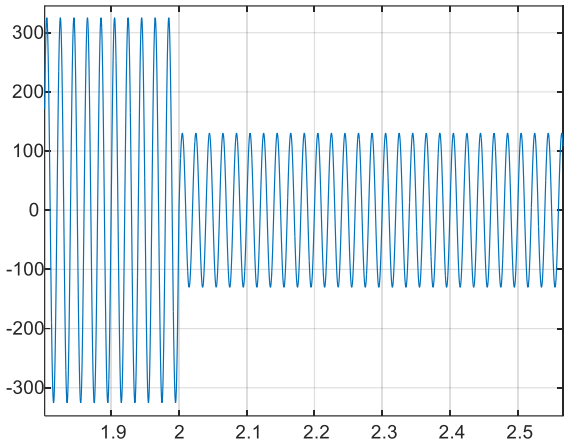

Figure 75 Grid voltage. Scales[Y: volts, X: seconds].

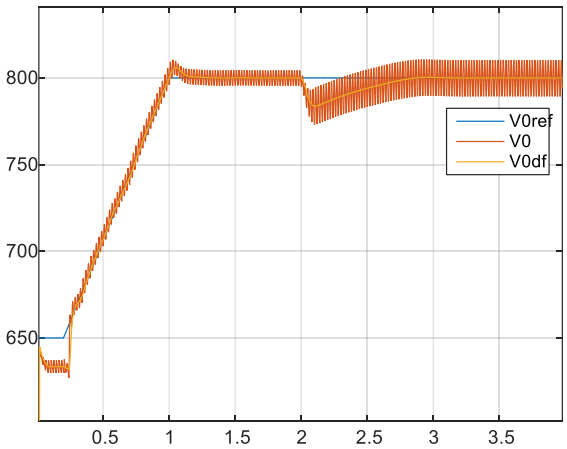

Figure 76 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

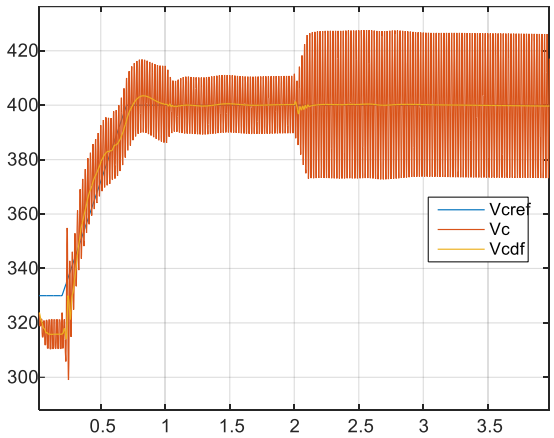

Figure 77 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

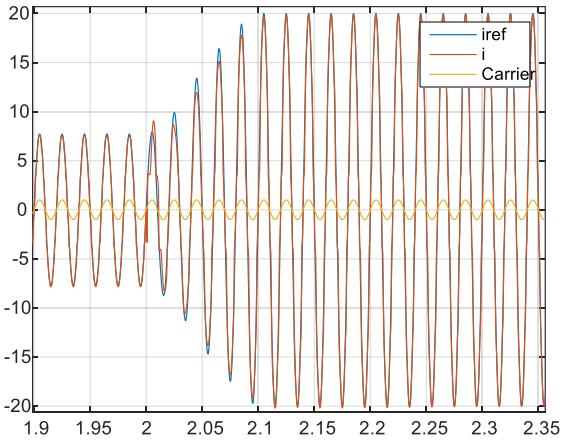

Figure 78 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps ,X: seconds].

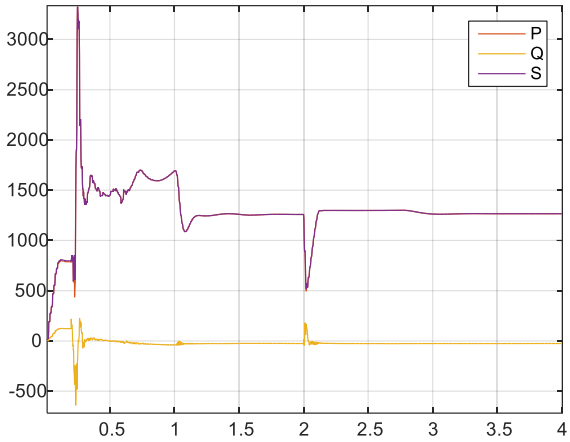

Figure 79 Real power (red), reactive power(yellow) and apparent power(violet) Scales[Y: Volt-Amps, X: seconds]

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$	THD[%]	PF[%]
430-370	775	20	3,7	97,29

Table 10 Measurements of overshoots, PF and THD.

4.7.5 Grid voltage with harmonic content

This test consists in supply a distorted grid voltage (IEC77A class1) to the converter with a full load connected. Figure 81 shows the shape of this signal, the distortion is quite obvious. The output and bias voltages have a transient similar to the full load test with sinusoidal grid voltage.

The input current preserves the sinusoidal shape in spite of the distorted grid voltage. In this case, the THD obtained is 2,62% compared to 2,21% with sinusoidal voltage. So, the controller attenuates properly the harmonic content of the grid voltage.

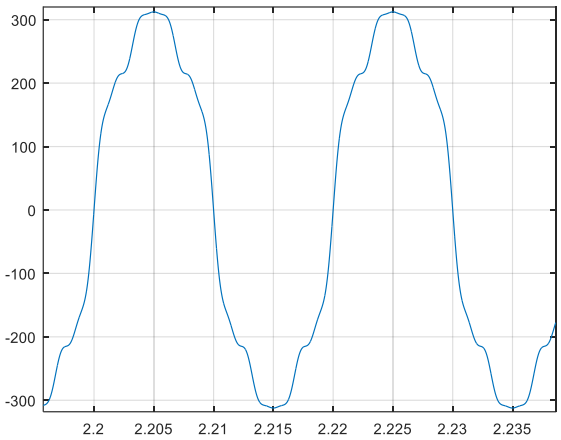

Figure 80 Grid voltage. Scales[Y: volts, X: seconds]

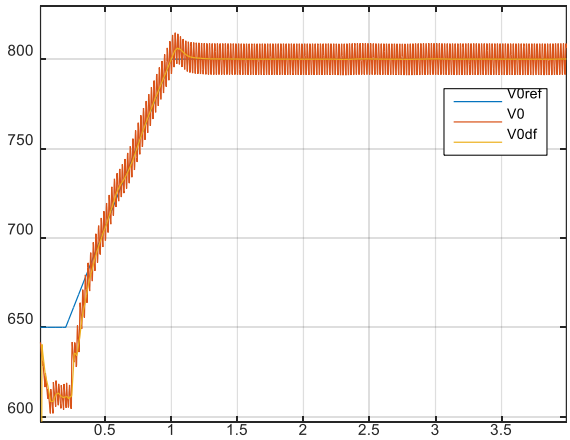

Figure 81 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

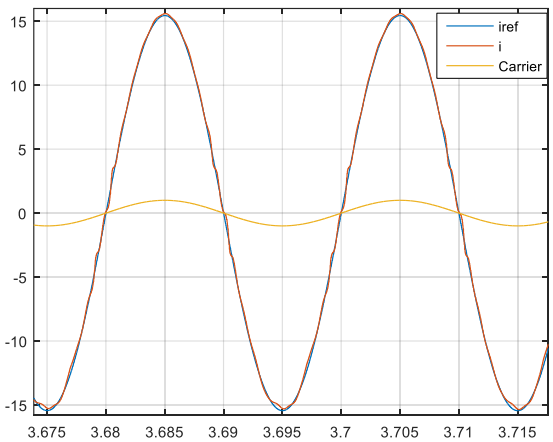

Figure 82 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps ,X: seconds].

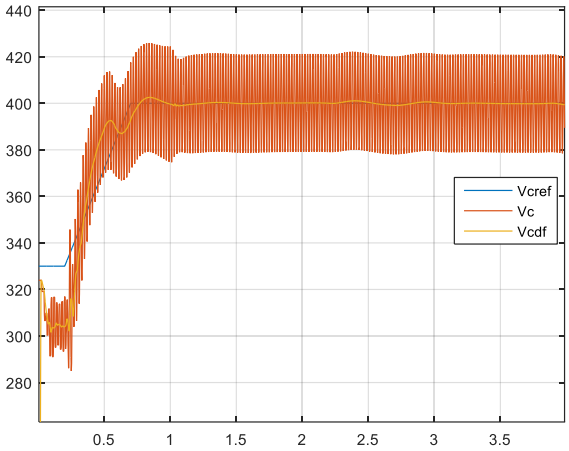

Figure 83 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

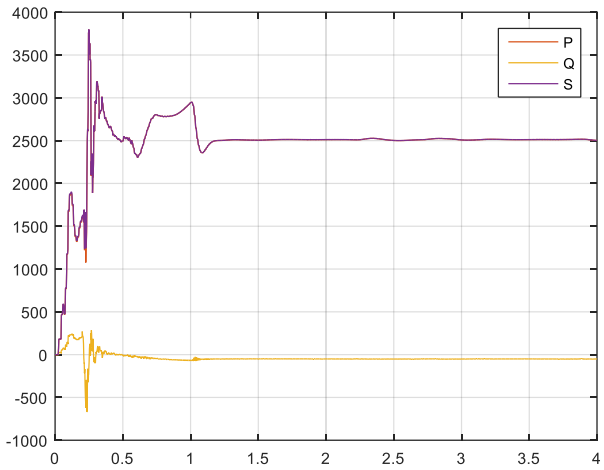

Figure 84 Active power (red), reactive power (yellow) and apparent power (violet). Scales [Y: Watts, Volt-Amps, X: seconds].

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$	THD[%]	PF[%]
415	810	16	2,62	98,54

Table 11 Measurements of overshoots, PF and THD

4.7.6 Grid voltage frequency variations

Now, some variations of frequency have been applied with full load condition. The next figure shows the values of the grid frequency with respect to time in the experiment.

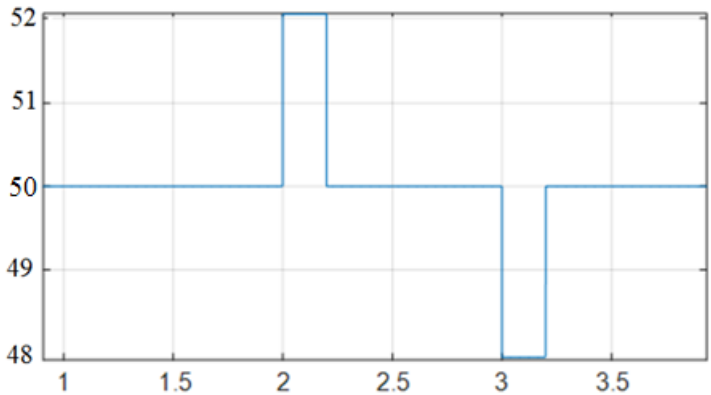

Figure 85 Frequency variations. Scales [Y: Hz, X: seconds].

The closed-loop system response to these disturbances is very good because, after the transient, the controlled variables recover the reference values. It is important to remark

that the frequency changes are of amplitude 2 Hz and in step. This value and the shape of the change are much harder than the ones usually found in power grids.

In the new frequency, when the system has reached the steady state, the power factor is 98,6% and the input current THD is 2,72%. These values are similar to the obtained at the nominal frequency of 50 Hz.

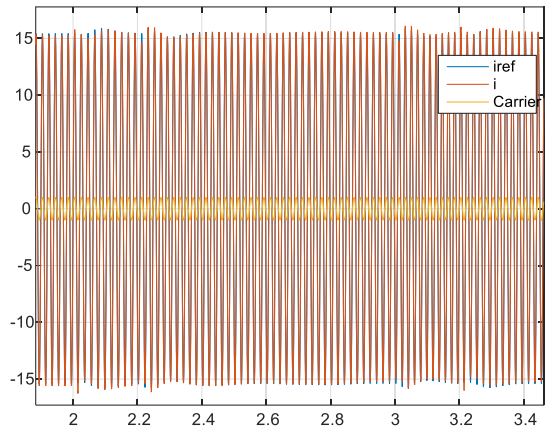

Figure 86 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

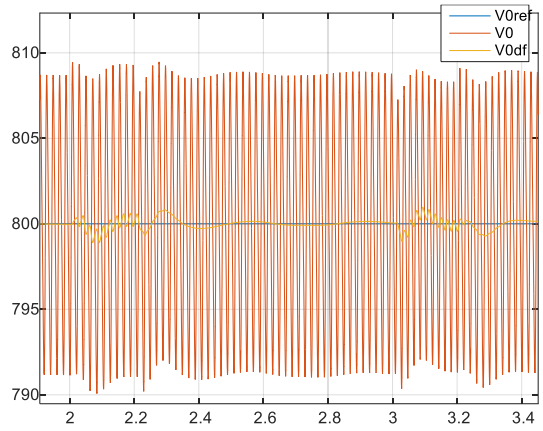

Figure 87 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

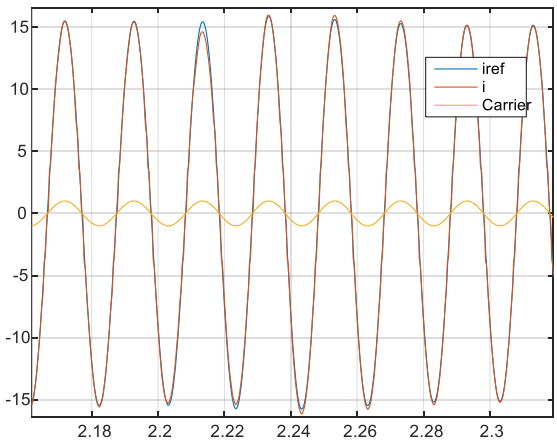

Figure 88 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps ,X: seconds].

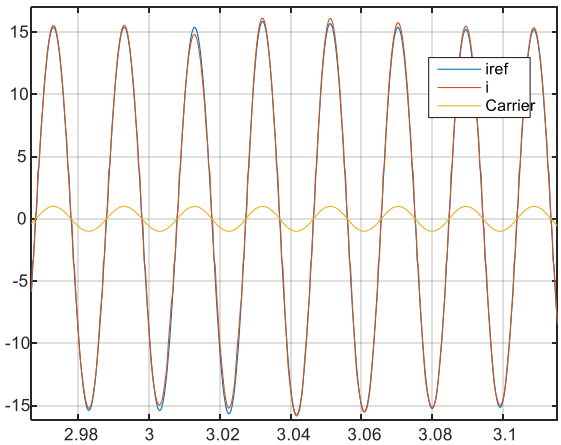

Figure 89 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

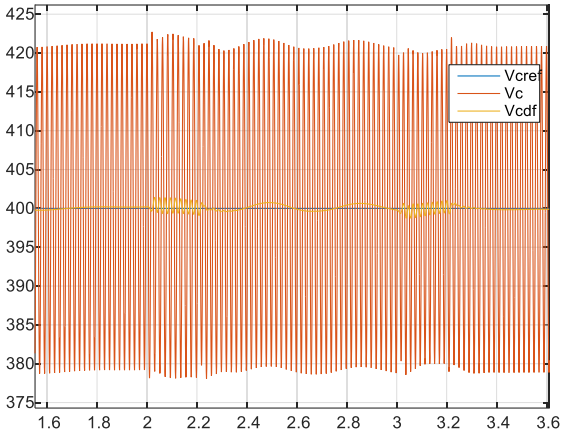

Figure 90 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

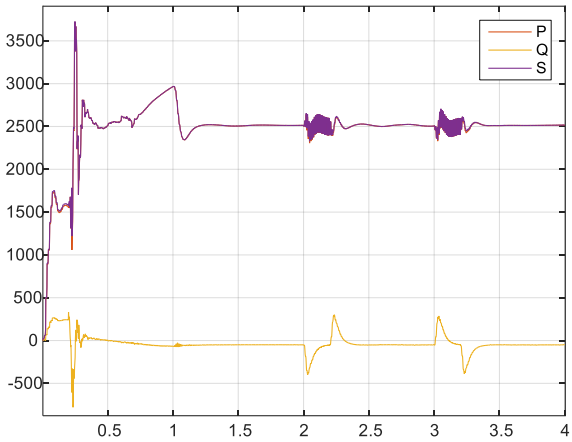

Figure 91 Active power (red), reactive power (yellow) and apparent power (violet). Scales [Y: Watts, Volt-Amps, X: seconds].

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$	THD[%]	PF[%]
422-380	808-793	16	2,72	98,59

Table 12 Measurements of overshoots, PF and THD

4.7.7 Grid voltage phase shifts

Last test consists in use a grid voltage with sudden phase shifts. This disturbance can appear in electrical grids due to the remote operation of protection elements. The following figures show the shape of these grid disturbances at different moments of the voltage period.

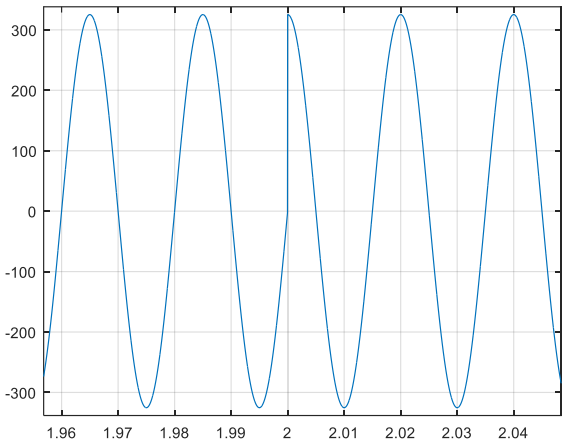

Figure 92 Grid voltage during the phase change 0º→90º. Scales [Y: volts, X: seconds].

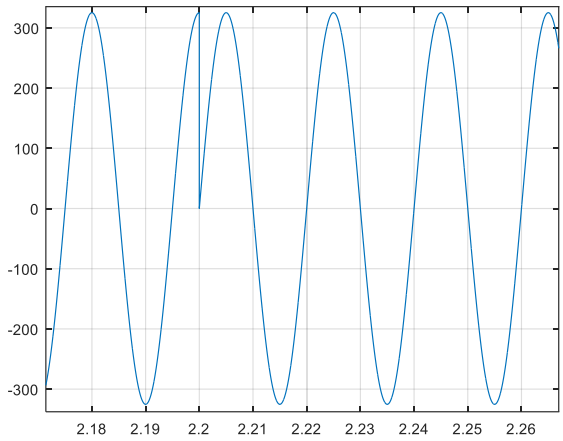

Figure 93 Grid voltage during the phase change 90º→0º. Scales [Y: volts, X: seconds].

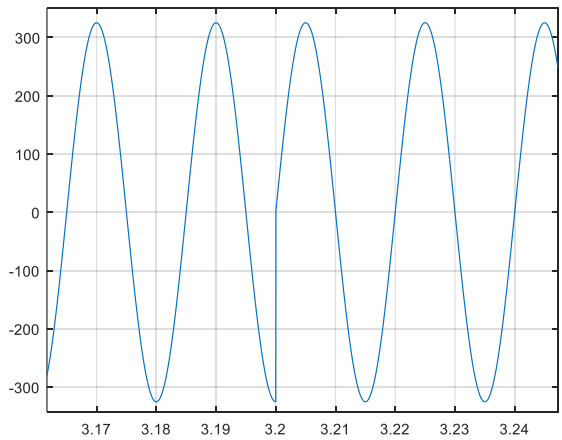

Figure 94 Grid voltage during the phase change -90º→0º. Scales [Y: volts, X: seconds].

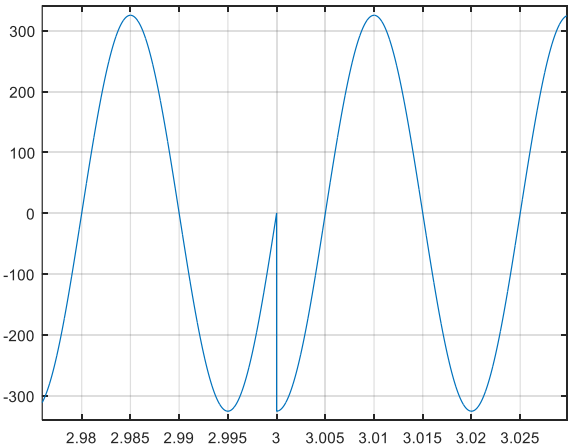

Figure 95 Grid voltage during the phase change 0º→-90º. Scales [Y: volts, X: seconds].

The output voltage and the bias voltage suffer from important transients in the phase shifts with overshoots of 20 V in the output voltage and 40 V in the bias voltage but the controlled system is able to cope these disturbances returning to the desired steady state. The same behaviour is observed in the input current with peaks of 35 A and -25 A. Obviously, these hard transients are reflected in the input powers but, as it can be observed, they return to the values previous to the shift changes without problems.

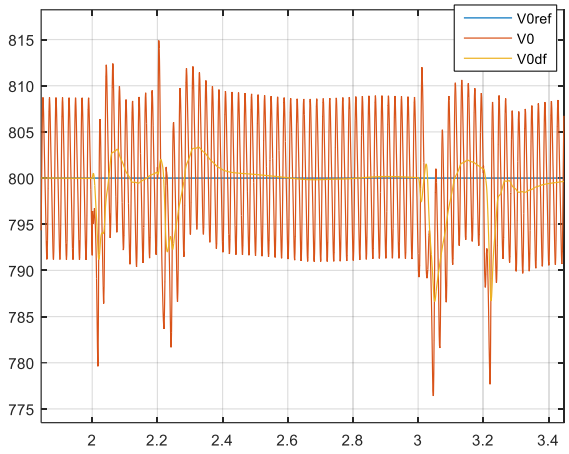

Figure 96 Output voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

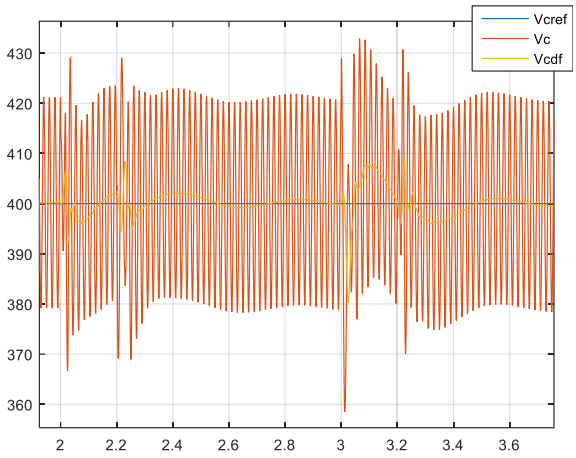

Figure 97 Bias voltage: reference (blue), measured (red) and measured mean (yellow). Scales [Y: volts, X: seconds].

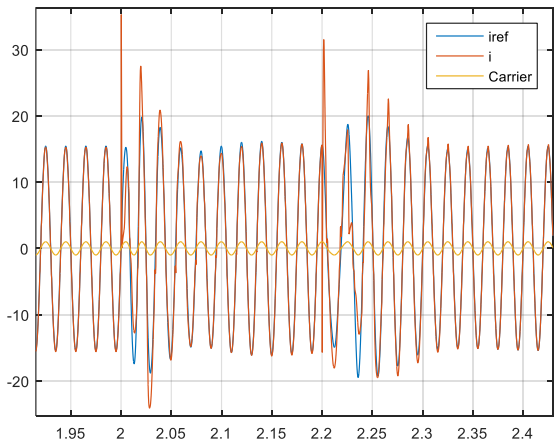

Figure 98 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

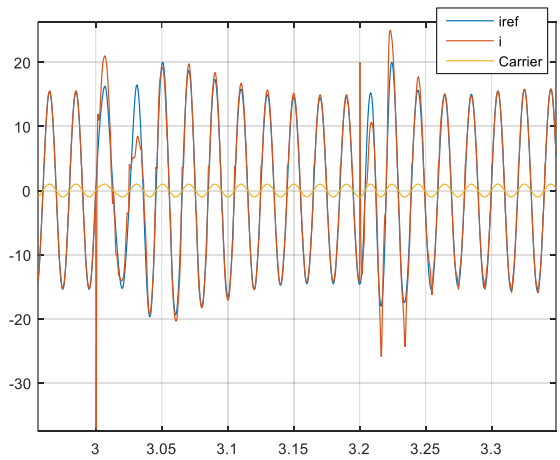

Figure 99 Input current: reference (blue) and measured (red). Carrier signal (yellow). Scales [Y: amps, X: seconds].

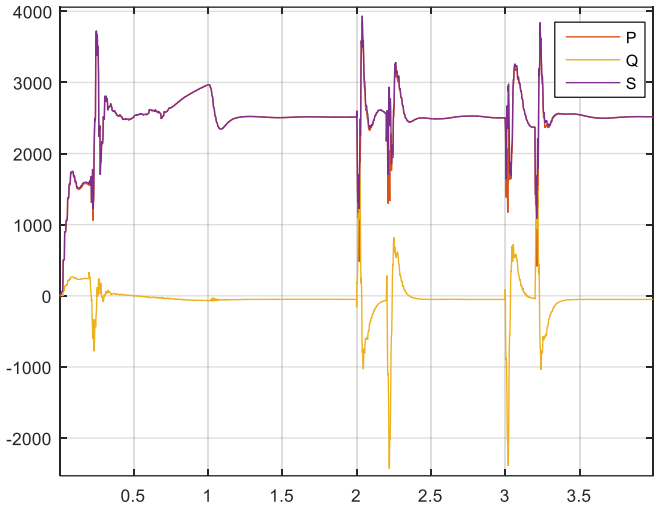

Figure 100 Active power (red), reactive power (yellow) and apparent power (violet). Scales [Y: Watts, Volt-Amps, X: seconds].

$V_c^{ov}[V]$	$V_0^{ov}[V]$	$i_p[A]$
435-358	815-776	35

Table 13 Measurements of overshoots.

5 Budget

Table 15 shows the cost to develop this project including tools of analysis. As it is observed on the table, it has been included the cost of a junior engineer doing the whole project, which consist of 900 hours assuming a cost of 15 €/h.

Components/development/Test	Cost [€]
Laptop(with office package included)	800
License Matlab	2000
Simpowersystem package	300
License Maple	1000
Working hours estimated	Cost [15€ per hour]
5hours·5days·36weeks=900H	13500
Total cost	17600

Table 14 Estimated budget to carry out the project

6 Conclusions and future development

This section concludes the thesis and presents the main contributions. Also, some suggestions of possible future lines of research are given based in the obtained results and experience.

6.1 Conclusions

The main reason for this new topology, in which a bias capacitor replaces the diode bridge that is normally used is that it reduces the distortion in the zero crossing of the input current.

Although it seems simpler, from a constructive point of view, in front of other topologies that use a diode bridge, its dynamics is rich enough to analyse it and to design a controller for all the relevant variables.

Analysing the obtained results, it can be argued that this new topology meets the expectations which, in particular, consist of achieving a converter with load regulation in a wide range and unity power factor at the input.

There are some experiments in which the THD of the current is slightly above 3%, but this only occurs under abnormal circumstances.

The final conclusion is that the designed digital controller meets the specifications when the converter is working at the nominal load. Besides, the behaviour of the controlled converter is good in front of variations of grid voltage amplitude, variations of grid frequency, grid voltage interruptions and load changes.

6.2 Future developments

This section describes some possible improvements that can be applied to the project or interesting topics to be investigated.

- Select the capacitor and inductance values taking into account characteristics as size, price and plant bandwidth. Probably doing a numerical optimization analysis.
- To perform a deeper analysis on the selection and tuning of the g_k gains used on the resonators, $R_k(z)$, of the current controller. This can be done using optimization techniques to maximize/minimize an appropriate objective function. This function can be build attending to different design concerns, determined by the specifications of the converter, such as desired performance, robustness, …
- Implement the controller developed in an experimental plant and verify its performance.
- The DC-DC boost converter on which the rectifier is based can be replaced by, for example, a DC-DC buck-boost converter to expand the range of output voltages and, therefore, its usefulness.

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Glossary

A list of acronyms and symbols and what they stand for.

Φ_k	Phase shift of the k^{th} resonator in rad.
C	Bias capacitor of the boost converter.
C_0	Output capacitor of the boost converter.
L	Inductance of the boost converter.
r	Parasitic resistance of the converter.
u	Control variable used.
PF	Power factor.
THD	Total harmonic distortion.
ov	Overshoot characteristic.
ss	Steady state of the signal.
$\mathrm{k_p}$	Gain of the proportional part.
$\mathrm{k_i}$	Gain of the integral part.
$\mathrm{k_d}$	Gain of the derivative part.
PWM	Pulse-width modulator.
$\mathrm{k_r}$	Gain of a resonator transfer function.
DT	Dead time.
PID	Proportional integral derivative (controller).
ZOH	Zero-order hold.
MP	Phase margin.
PLL	Phase-locked loop.
$\mathrm{F_s}$	Switching/sampling frequency.
$\mathrm{F_1}$	Grid frequency.
$\mathrm{T_s}$	Switching/sampling period.
PFC	Power factor correction.
AFC	Adaptive Feed-forward Cancellation.
Sag	Short duration reduction of voltage amplitude.
$Swell$	Short duration increase of voltage amplitude.