Imperial College London

Development of a sub-miniature acoustic sensor for wireless monitoring of heart rate

by

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Declaration of Authorship

I, Thanut Tosanguan, declare that this thesis entitled, 'Development of a sub-miniature acoustic sensor for wireless monitoring of heart rate' and the work presented in it is my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at Imperial College London.

- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, it has been referenced.

- Where I have consulted the published work of others, this is always clearly referenced.

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- I have acknowledged all main sources of help.

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Abstract

This thesis presents the development of a non-invasive, wireless, low-power, phonocardiographic (PCG) or heart sound sensor platform suitable for long-term monitoring of heart function. The core of this development process involves a study of the feasibility of this conceptual system and the development of a prototype mixed-signals integrated circuit (IC) to form the integral component of the proposed sensor.

The feasibility study of the proposed long-term monitoring sensor is divided into two main parts. The first part of the study investigates the technological aspect of the conceptual system, via a system level design. This is to prove the technological or operational feasibility of the system, where the system can be built completely using discrete, off-the-shelf electronics components to satisfy the size, power consumption, battery life and operational requirements of the sensor platform. The second part of the study concentrates on the post-processing of the heart sounds and murmurs or PCG data recorded. This is where a number of different de-noising algorithms are studied and their relative performance compared when applied to a variety of different noisy heart sound signals that would likely be acquired using the proposed sensor in everyday life. This was done to demonstrate the functional feasibility of the proposed system, where the ambient acoustic noise in the recorded PCG data can be effectively suppressed and therefore meaningful analysis of heart function i.e. heart rate, can be performed on the data.

After the feasibility of the conceptual system has been demonstrated, the final part of this thesis discusses the synthesis and testing of a 0.35 μm CMOS technology prototype mixed analog-digital integrated circuit (IC) to miniaturise part of this sensor platform outlined in the system level design, conducted in the earlier part of this thesis, to achieve the objective specifications – in terms of the size and power consumption. A new implementation of the multi-tanh triplet transconductor is introduced to construct a pair of 100 nW analogue 4th order Gm-C signal conditioning filters. Furthermore, a 7 μW digital circuit was designed to drive the analog-to-digital conversion cycle of the Linear Technology LTC1288 ADC and synchronise the ADC's output to generate the Manchester encoded data compatible with the Holt Integrated Circuit HI-15530 Manchester Encoder/Decoder.

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Chapter 1

Thesis Overview

This thesis presents a systematic development of a novel non-invasive, low-power, phonocardiographic (PCG) or heart sound sensor suitable for wireless long-term monitoring of heart rate. The core of this development process involves a study of the feasibility of this conceptual system, given a set of specifications – in terms of the operational or technological aspects, the functional aspects, and the development of a mixed-signal integrated circuit (IC) for the proposed sensor.

In the development process of any conceptual product or system, a feasibility study is normally sanctioned to ascertain if the product or system can electrically perform the operations required and whether these operations can be performed within the given specifications. Furthermore, the conceptual product or system must also meet its functional requirements. In this case, the sensor was designed to function as a monitor of a person's heart; therefore we must be able to recognise the locations where the heart sound is present in the PCG signal and to use the PCG signal received from the sensor to derive the heart rate of the wearer. Since this conceptual sensor will be subjected to ambient acoustic noise in real usage, thus for this sensor to be feasible functionally we must illustrate that the noise can be effectively suppressed. Once this feasibility study has shown that this conceptual sensor is both operationally and functionally viable, we can go on to realise the sensor itself. Hence, this thesis will be divided into three main parts.

Chapter 2 forms the first part and explains the background and the motivation behind the research presented in this thesis. This chapter also summarises the current monitoring systems that are available through commercial companies and those developed by research groups and university institutions. At the end of this chapter, the proposed conceptual sensor and the methodology to achieve it will be discussed.

Chapter 3 and 4 form the second part, where the feasibility of the proposed system is studied.

Chapter 3 deals with the system level design of the proposed monitoring system using strictly discrete, off-the-shelf components to meet the specifications of the sensor – in terms of size, power consumption, non-invasiveness, unobtrusiveness and wirelessness. This involves the formation of the main building blocks of the wireless system, an investigation into suitable technologies for each building block, the search for suitable batteries and discrete components necessary to perform the required operations of each block, and the detailed design of the analogue and digital circuit of each block to allow the overall sensor to operate as a system. Lastly, to illustrate the operational feasibility of the system as a whole the operation of each building block was tested.

Chapter 4 focuses on the study of the de-noising algorithms that can be or have been applied to suppress ambient noise in heart sound recordings. Five different noise cancellation techniques, including Wavelet Thresholding and a novel 2-channel algorithm based on the Spectral Subtraction algorithm, were used in this study to investigate their relative performance when applied to a number of different heart sounds. This chapter also discusses the recording system that was developed to obtain the simulated noisy PCG data in a controlled environment that was applied to the de-noising algorithms.

Chapter 5 forms the last main part of this thesis. This chapter explains the synthesis of and the testing of the prototype mixed-signal integrated circuit (IC) that forms the core of the proposed sensor. In the first half of this chapter, the development and the measured results of a pair of Gm-C filters, which forms part of the analogue signal conditioning block, is discussed. This development involves a transistor level design, simulation, and layout of a

Multi-tanh triplet transconductor, which was used repeatedly to construct the Gm-C filters. The second half of this chapter concentrates on the development and the measured results of the digital signal processing block. This development involves the digital timing diagram design, the functional block (flip-flops and logic gates) level design, simulation, and layout of the Manchester encoder and the synchronisation circuit, between the analog-to-digital converter (ADC) and the built-in Manchester encoder.

Chapter 6 summarises the specific achievements reported in this thesis and highlights a number of potentially valuable future research in this field.

Chapter 2

Background, Motivation and Objectives

2.1 Introduction

The heart is arguably the most important organ of the human body. This is because the heart is responsible for providing a vital transport mechanism for blood. Effective blood circulation is critical for the body's well-being because blood is responsible for transferring hormones, nutrients and waste products from one organ to another. Two of the most important blood contents are oxygen (O_2) and carbon dioxide (CO_2). The body, in a natural environment, requires the supply of O_2 to generate energy in an aerobic manner, where CO_2 is produced as a by-product. On the other hand, the CO_2 produced must also be removed from the body to prevent the build-up of CO_2 concentration, which is harmful to the body. Without O_2, the body is still able to produce energy, although in a less efficient way, using anaerobic respiration. Nevertheless, the harmful by-products produced in anaerobic respiration and the build-up of CO_2 will cause the body to seize functioning after a prolonged period of O_2 deprivation. Still, the heart is as vulnerable as any other major organ and can suffer from a variety of diseases and abnormalities. However, unlike most other organs the heart is required to work continuously, beating some 60 to 100 times per minute, thus any diseases and abnormalities that may impair or cause the heart to stop can be potentially life-threatening.

In this chapter, the anatomy of the heart, the techniques to diagnose the heart's condition, as well as the motivation and the objectives of this research will be discussed.

2.2 Anatomy of the Heart

The heart consists of four chambers (shown in Figure 2.1) – the left ventricle, the right ventricle, the left atrium, and the right atrium. The right ventricle is used to pump and transport de-oxygenated blood into the lungs, via the pulmonary arteries, where the vital exchange of carbon dioxide (CO_2) out of blood and oxygen (O_2) into blood occurs. The left atrium collects the newly oxygenated blood from the lungs before passing the blood to the left ventricle. The left ventricle is responsible for supplying this oxygenated blood to the rest of the body, where great pressure is required to achieve this. Thus, the left ventricle wall is thicker than the right ventricle wall. After the oxygen has been passed to the cells in the body, the de-oxygenated blood is collected at the right atrium, where the process starts over again.
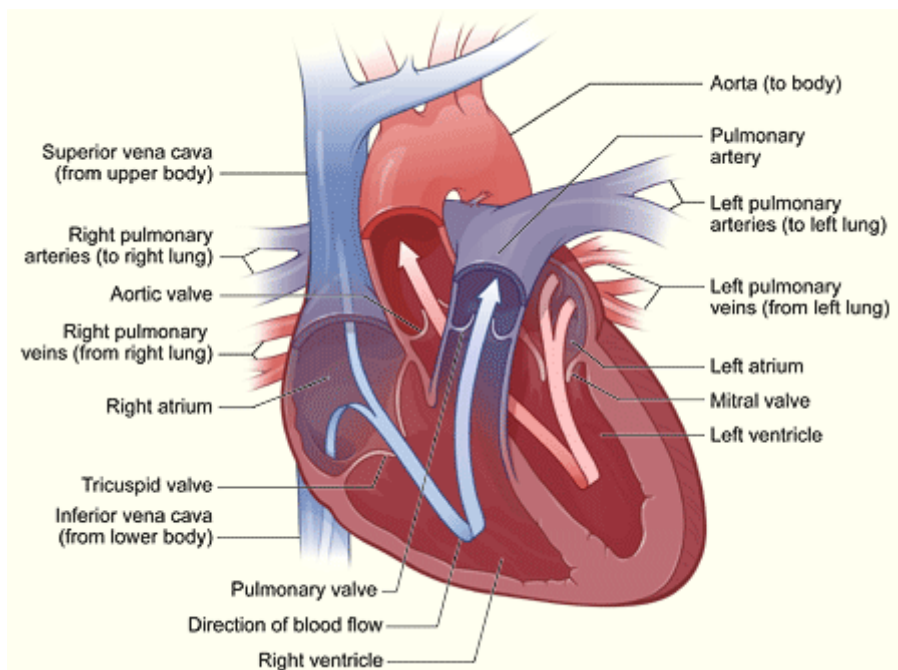
Figure 2.1: Anatomy of the heart [3].

The transfer of blood from the atria to ventricles and the ventricles to the aorta or pulmonary artery do not occur continuously. However, blood is transferred from the atria to the ventricles during atrial systole, where the contraction of the muscles in the atrial walls causes the pressure in the atria to increase and the valves partitioning the atria and the ventricles to open – the tricuspid valve for the right atria and ventricle and the mitral valve for the left atria and ventricle. Furthermore, blood is transferred from the ventricles to the aorta or pulmonary artery during ventricular systole, which occurs when the ventricle walls contract. The great pressure produced by the ventricle walls causes the aortic valve (left ventricle) and the

pulmonary valve (right ventricle) to open and the blood to be ejected from the ventricles. Prior to ventricular systole, both the mitral and the tricuspid valves close to prevent any backflow into the atria.

The timing of both the atrial and the ventricular systoles is controlled by the sinoatrial (SA) and the atrioventricular (AV) node. The SA node is responsible for generating the electrical impulses necessary to cause the contraction of the heart's muscles [31]. The electrical impulse passes through the atrial walls first causing the contraction of the atria or atrial systole. It then travels to the AV node where the conduction is delayed. This delay allows blood to fill the ventricles before the electrical impulse travels to the apex (bottom tip) of the heart, via the Bundle of His, and cause the almost instantaneous contraction of the ventricle walls from the apex upwards [31].

2.3 Heart Sound, Murmurs and Auscultation

The seriousness of heart diseases and abnormalities has prompted many physicians to find ways to diagnose the heart's condition. The first method conceived was to listen to the sounds that the heart produces. The first evidence of this was the invention of a medical instrument called the 'stethoscope' in 1816 by a French physician, Laennec [5]. The stethoscope has since established itself as a symbol of the doctor's profession and is normally the first medical tool to be used when diagnosing a patient.

2.3.1 Normal Heart Sounds

Although, the origin of heart sounds and murmurs is still being debated with more than 40 different mechanisms being proposed [41]. It has been universally accepted that there are up to four heart sounds in a cardiac cycle of a healthy subject. Figure 2.2 illustrates how the four heart sounds are related to the electric and mechanical events of the cardiac cycle. The first heart sound (S1) is believed to be caused by the acceleration and deceleration of blood during ventricular systole [13,41] or the closure of the mitral and tricuspid valves [9]. While, the intensity of sound is related to the force of the cardiac contraction [13]. The second heart sound (S2) is believed to be caused by the deceleration and reversal of flow in the aorta and the pulmonary artery with the closure of the aortic and pulmonary valves [15,41]. The third heart sound (S3) can be heard at maximal ventricular filling or the sudden termination of the rapid-filling phase of the ventricles from the atria, normally audible in children and in some adults [9,15,41]. The fourth heart sound (S4) is not audible but can be recorded with a

phonocardiogram. It occurs when the atria contracts and forces blood into the ventricles [15,41].
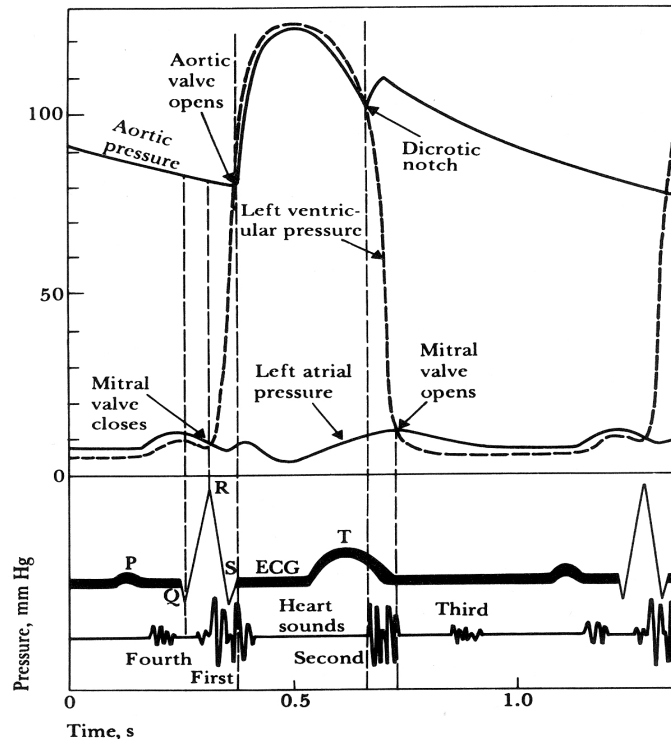
Figure 2.2: Time correlation of heart sounds with electrical and mechanical events in a cardiac cycle [41].

2.3.2 Origin of Murmurs

Murmurs are normally heard, in addition to normal heart sounds, as a result of turbulent blood flow. Usually murmurs are associated with abnormalities or diseases of the heart valves. However, some 'innocent' murmurs may be heard from a normal heart, in children. Thus, they are termed 'innocent' [9].

The two valves that are most susceptible to diseases and abnormalities are the mitral valve and the aortic valve. Both of these valves directly controls the flow of blood to (mitral) and from (aortic) the left ventricle. The most common congenital abnormality is associated with the aortic valve, which is made of three equal sized cusps. However in 1 to 2 per cent of the population, it is found that either the cusps are not equal in size or there are less than three cusps [9]. This abnormality of the aortic valve is more common in men than women. Conversely, the murmurs associated to the mitral valve is more common in women and is

normally indicative of a disease of the mitral valve or the reduced function of the left ventricle due to an ischaemic heart [9].

2.3.3 Auscultation

The diagnosis technique related with the stethoscope is known as auscultation. In auscultation, a physician listens to the heart sounds and murmurs through a stethoscope and uses his or her knowledge and experience to determine the heart's condition. Since heart sounds have to travel through the body to reach the body's surface and different tissues have different acoustic transmission properties, thus heart sounds will be attenuated to a varying degree depending on the listening location. Figure 2.3 shows the four basic chest locations where the intensity of sound from the four valves is maximised.
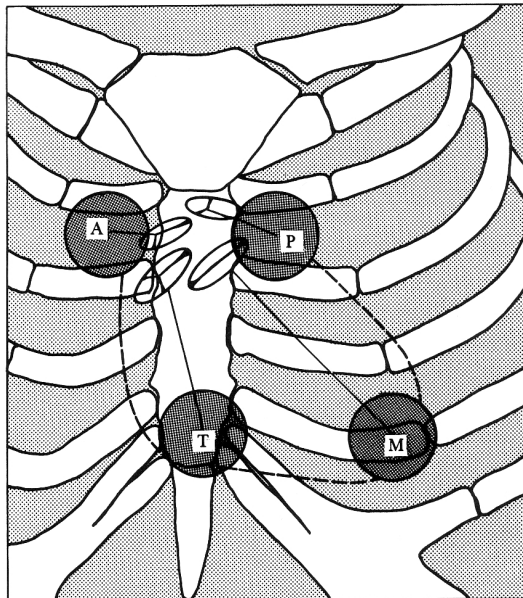
Figure 2.3: Chest areas for auscultation – A, aortic; P, pulmonary; T, tricuspid; and M, mitral areas [41].

2.4 Phonocardiogram (PCG) vs. Electrocardiogram (ECG)

Since the analysis of the heart functional integrity via auscultation is highly dependent on the listener's hearing capabilities, training, and experience, therefore this diagnosis technique is highly subjective and vital information can be overlooked or misinterpreted by a relatively inexperienced listener. Thus, the phonocardiogram (PCG) was invented to make an objective analysis of the heart sounds and murmurs, by producing a graphical representation of them. This further allows physicians to evaluate the timing of heart sounds and murmurs in relation to the electrical and the mechanical events in a cardiac cycle (as illustrated in Figure 2.2).

The electrical events within a cardiac cycle can be recorded using an electrocardiogram (ECG). The ECG is another objective technique that can be used to diagnose the heart's condition. This technique was first illustrated by Waller in the late 19th Century and later improved on by Einthoven [31]. This diagnosis tool is ideal for examining the electrical conduction system of the heart, however to achieve a recording two or more surface electrodes are required to be attached to the chest area of the body; the more the electrodes, the better the recording.

The mechanical events can be recorded via microphone systems to measure the indirect carotid pulse, jugular venous pulse, and/or the apex cardiogram. Once a recording is obtained, a cardiologist can identify abnormalities from the relative timing between different events [41].

Clearly, PCG is an excellent diagnosis tool, arguably more so than the ECG that only displays electric activity of the heart, however its use is fairly limited. This is mainly due to the susceptibility of PCG systems to ambient acoustic noise; and this remains to be the main obstacle to permit widespread use of PCG systems.

In the past, the inability to overcome this challenge has allowed the ECG to be widely adopted as a system of choice for diagnosis of patients with potential heart problems and monitoring of patients in intensive care units. However, times have changed. Following the recent and rapid development in electronic technologies and computer processing power, physiological data can be effortlessly and economically saved, processed, and stored in a digital format on a personal computer (PC). This combined with the advancement in signal processing techniques have uncovered new possibilities with regards to how heart sounds can be processed i.e. de-noised, segmented and analysed for cardiac abnormalities. All of these factors have restored the potential of PCG as a viable diagnosis and monitoring tool inside and possibly outside hospitals.

2.5 Long-term Monitoring – an emerging trend?

Today, even after years of research, heart disease continues to be the leading cause of death in the developed world, with coronary heart disease (CHD) accounting for the majority of fatalities – 105,000 in the UK (in 2004) and 1 in every 5 deaths or 653,000 in the US (in 2003) [6,35]. Furthermore, the implication of heart disease does not stop there; it is estimated that the health and non-health care cost associated with CHD is £7.9 billion (in 2004) and $142.5 billion (in 2006), for the UK and the US respectively [6,35]. In the UK, the cost of health care for CHD has more than doubled over the last five years.

However in an effort to tackle the rising cost in health care, there is an increasing interest in monitoring physiological signals, which has been routinely performed in acute care, for example in coronary care units, intensive care units and specialist neonatal care units, over long periods outside of hospitals to:

1. provide an indicator of heath status in chronic diseases,

2. provide clinicians with a track record of monitoring data,

3. permit better and faster treatment due to a track record of monitoring data,

4. decrease in-hospital stay; and thus

5. decrease the overall health and non-health care cost.

The anticipated benefits, as mentioned above, of such a monitoring system have been partly substantiated by Robinson in 2004 [32], where a randomised trial was conducted on over 400 patients with congestive heart failure. In the study, 5 minutes of physiological data were collected daily with a Philips handheld unit. Patients in this trial benefited from a decrease in total hospital stay because when they were admitted they were able to provide a track record of monitoring data, which eliminated the need for further monitoring prior to treatment.

2.5.1 Heart Rate Variability (HRV)

One parameter, in particular that is indicative of disease status, is the heart rate variability (HRV). For healthy people, the heart rate is not constant but varies with activity such as exercise and ambient conditions such as the temperature. In a resting state, the heart rate has been shown to exhibit a periodic fluctuation at three frequencies; high frequency (HF) around 0.25 Hz is associated with respiration; medium frequency (MF) around 0.1 Hz is associated with spontaneous vasomotor activity related to blood pressure regulation of the sympathetic nervous system; and low frequency around 0.05 Hz is associated with thermo-regulation (shown in Figure 2.4) [21].

Alterations in the HRV frequency content have been related to a number of medical conditions, including sudden infant death syndrome (SIDS) [14,16,30], heart failure [22], sudden cardiac death syndrome [24], diabetic neuropathy [28], and obstructive sleep apnea (OSA) [20,33]. Results from population-based follow-up studies suggested that lowered HRV is also associated with the risk of developing coronary heart disease (CHD) [24]. A depressed

HRV has been identified as a predictor of risk in patients after acute myocardial infarction (MI) and also an early warning sign of diabetic neuropathy [34]. The same study also found that the predictive value of depressed HRV increased with the length of the data set up to their maximum monitoring period of 24 hours. HRV has also been found to have prognostic value in the care of the elderly [38] and was found to be associated with all-cause mortality.
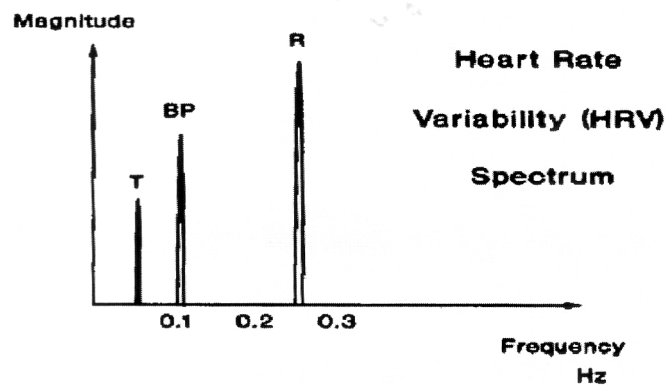
Figure 2.4: Heart Rate Variability (HRV) spectrum, where the T (temperature)-component relates to thermoregulation of the body, the BP (Blood Pressure)-component relates to the baroreceptor reflex to control the blood pressure, and the R (Respiration)-component relates to respiration [21].

Monitoring of HRV is usually done using specialised algorithms on ECG data. This is generally limited to 10-minute sequences obtained in hospitals and in special cases, a longer sequence of up to 24 hours may be obtained using a traditional belt-worn Holter monitors. Studies have shown that the predictive value of HRV increased with the length of monitoring and that monitoring during daily activities is beneficial. However, unobtrusive, longer-term monitoring with traditional systems is not practically plausible because of the battery-life limitations and the intrusive nature of ECG monitoring, where at least two leads are required to be placed on two different sites on the chest.

2.5.2 State of the Art

Many commercial companies have recognised the need for monitoring systems. Philips [2] and Docobo [4] have produced table-top home monitors for regular episodic monitoring (shown in Figure 2.5). There has also been work on a wrist mounted sensor, AMON [7], but this is not complete and is still relatively bulky (illustrated in Figure 2.6 a)). In general, the devices that have been developed are focused on recording a comprehensive set of physiological

parameters, although at a penalty of increased size and device complexity. One system that is suitable for long term monitoring is the Medtronic Reveal® Plus System (Figure 2.6 b)) [1]. This device continuously reads ECG signals and logs abnormal events; however it requires periodic downloading of data and more importantly, a surgical implantation.

a)   b)

Figure 2.5: a) Philips – Telemonitoring system [2], and b) Docobo - HealthHUB™ [4].

a)   b)
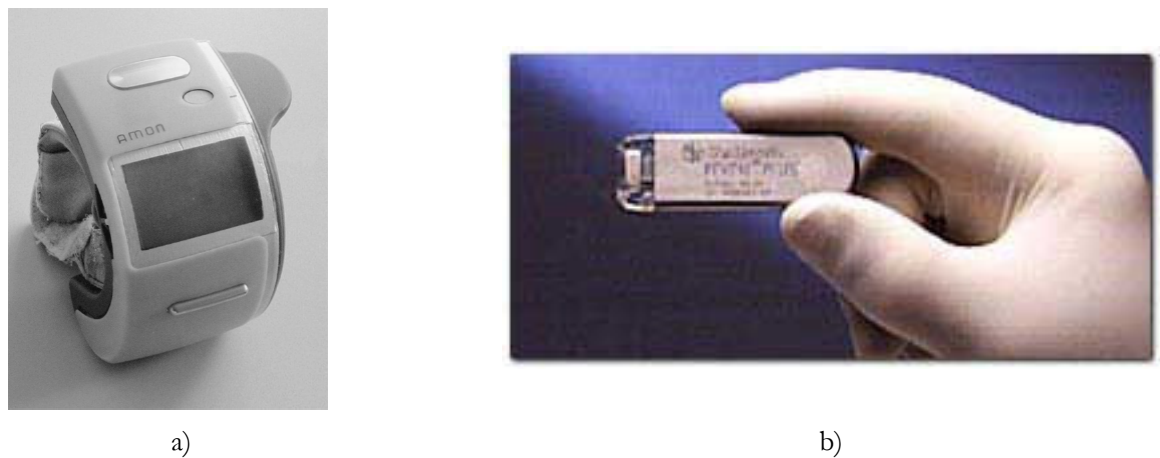
Figure 2.6: a) AMON prototype [7], and b) Medtronic Reveal® Plus System [1].

A number of university groups have been developing wireless PCG platforms for long-term monitoring [8,11,18,23,25,36,40]. Most of them have illustrated the feasibility of wireless PCG systems; however the details regarding the size and power consumption of these systems are sketchy at best. The most distinct idea was presented by Asada et al [8], where an array of wireless and battery-less "stethoscope", placed at various sites on the chest, are inductively coupled to a mobile phone (illustrated in Figure 2.7). The acoustic signals received by the phone can then be processed, stored, and transmitted over the mobile phone network to a

long-term storage site. Two studies by other groups have specifically focused on incorporating Bluetooth™ technology into the system for communication purposes [11,18]. In other cases, PDAs have also been used to display, store, and process PCG signals [10,18]. A good overview of current and up-coming wireless telemedicine systems is provided by Pattichis [29].

Figure 2.7: Smart Mole system introduced by Asada et al [8].

2.5.3 Challenges

The main technical requirements for all portable systems to monitor physiological parameters are size and power consumption. A system with low power consumption will allow a more compact battery to be used, or the battery life to be extended.
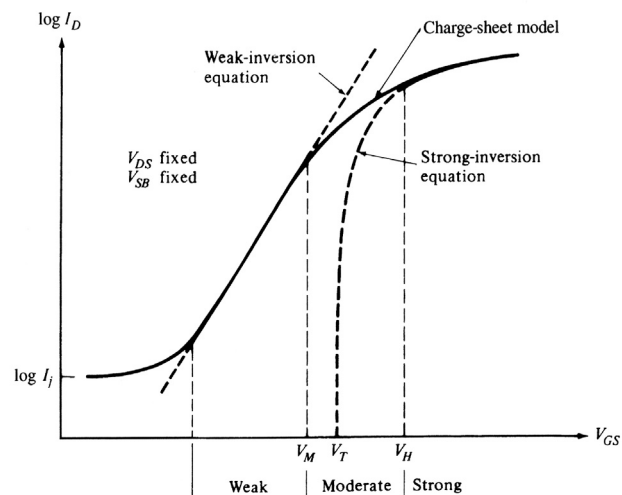
Figure 2.8: Current, I_D vs. Input voltage, V_{GS}, characteristics of MOS transistors for different operating regions [37].

Current devices use low power, but design techniques such as CMOS weak-inversion (Figure 2.8) operate at very low currents in the scale of nano-Amps or 10^{-9} Amps, due to the exponential response of the transistor when operating in the weak-inversion region. Thus, the power consumption of the circuit can be greatly reduced.

Furthermore for monitoring systems to be suitable for long term use, the sensor must be small enough to be completely unobtrusive so that it does not cause discomfort when mounted on the patient's skin or interfere with the wearer's daily activities. This issue of the sensor size can initially be addressed by miniaturising the electronics. However, the minimum sensor size will be restricted by how the heart function is monitored, the battery size, and the size of the radio module.

2.6 Research Objectives

The aim of this research is to develop a sub-miniature acoustic sensor based on PCG or heart sounds to monitor heart function, which is unobtrusive and suitable for long-term, wireless monitoring. The sensor will act as a digital stethoscope; whereby it will capture the acoustic signals produced by the heart and converts it into a digital electrical signal. This digital data can then be processed at a later stage to extract the HRV and other valuable physiological information to assist in the management of chronic diseases.

This device will fill the gap left by current devices, in that it will be sufficiently small to permit it to be mounted on the patients' skin, with minimal discomfort and minimal disruption to the wearer's daily activities. For the sensor to satisfy the size requirements, a PCG-based monitoring system is preferable over ECG. This is because ECG is not a single point measurement and requires an array of electrodes. Furthermore, reliable electrical contact cannot be guaranteed for a substantial period of time. Thus, ECG measurement is not compatible with miniaturisation and/or unobtrusive monitoring. The proposed transducer in this research is a miniature microphone to listen to the heart sound, known to give excellent information regarding the functional integrity of the heart, and has the advantage of being a single point measurement method. The data obtained from this microphone has been shown to be sufficient for recovering the heart rate and thus the HRV [27]. In addition, it has been demonstrated in other work that heart sound data can be used to diagnose valve problems as well as to assess the performance of prosthetic valves in patients who have undergone a valve replacement procedure [15].

The development of this proposed conceptual system will be presented in this thesis as a study of the system's feasibility and the realisation of a prototype mixed-signals integrated circuit (IC), which forms the core of the proposed sensor.

This feasibility study is sub-divided into two main parts. The first part of the study, presented in Chapter 3, involves the system level design of the conceptual monitoring system. This includes the formation of the system's building blocks, the detailed design of each building block built using only discrete, off-the-shelf components, and the measured result of each block's operational test from the selected components. In essence, this study will help verify the technologic or operational feasibility of the proposed system

The second part of the study, presented in Chapter 4, deals with a number of de-noising algorithms in post-processing, since PCG systems are very susceptible to ambient acoustic noise. Thus for the system to be functionally feasible, it must be able to effectively suppress noise from the PCG recordings to recover the original heart sound. Therefore, a comprehensive study of the de-noising algorithms will be presented in Chapter 4. This will involve a technique called 'Wavelet Thresholding', which several researchers have shown to be an effective technique at removing the ambient acoustic noise [12,17,19,26,39,42], and also a novel 2-channel de-noising technique devised by the author.

After the feasibility of the proposed conceptual system has been illustrated, the realisation of a prototype of the mixed analog-digital integrated circuit will be presented in Chapter 5. The aim of this is to minimise the size and power consumption of the proposed sensor, using very low power signal conditioning circuitry, that incorporates technologies such as CMOS weak-inversion and Gm-C filter topology. This will allow the system to be powered by a compact battery, while maintaining an acceptable battery-life.

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Chapter 3

System Level Design

3.1 Introduction

In this chapter, a system level design of the heart rate monitoring system that can be built using only discrete, off-the-shelf electronics circuitry on a printed circuit board (PCB) will be presented. There are many tasks that must be completed in a design of a conceptual system. In this thesis, the system level design process has been separated into three main tasks:

1. Formulate the proposed system using basic building blocks, define their role(s) in the system, and identify currently available technologies suitable for performing the specified role(s),

2. Conduct a detailed design for each building block in the proposed system, and

3. Test the operational feasibility of each block.

The structure of this chapter is organised according to the tasks of the system level design outlined above.

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3.2 The System

The proposed heart rate monitoring system consists of two parts: one is a wireless, battery-operated sensor and the other part is a receiver that will process and store the heart sound or PCG data. In simple terms, the tasks of the sensor can be outlined as follows:

a) It has to convert the mechanical vibrations caused by heart sounds and murmurs into an analogue electrical signal.

b) The heart sound or PCG data has to be converted into a digital format, using an analog-to-digital converter (ADC), for further processing and radio transmission, where it is more robust to noise.

c) Thus, the analogue electrical signal has to be amplified to a compatible level with the ADC and appropriately filtered to prevent aliasing in the digital data.

d) This digital PCG data has to be processed to either remove any ambient acoustic noise and/or prepare the data for radio transmission using a processor.

e) If a separate ADC and processor are used, then synchronisation is normally required to transfer the data from one building block to another.

f) Lastly, the processed PCG data has to be transmitted to the receiver for further processing and storage.

From the sensor's tasks outlined above, the block diagram of the proposed monitoring system was formulated as shown in Figure 3.1.
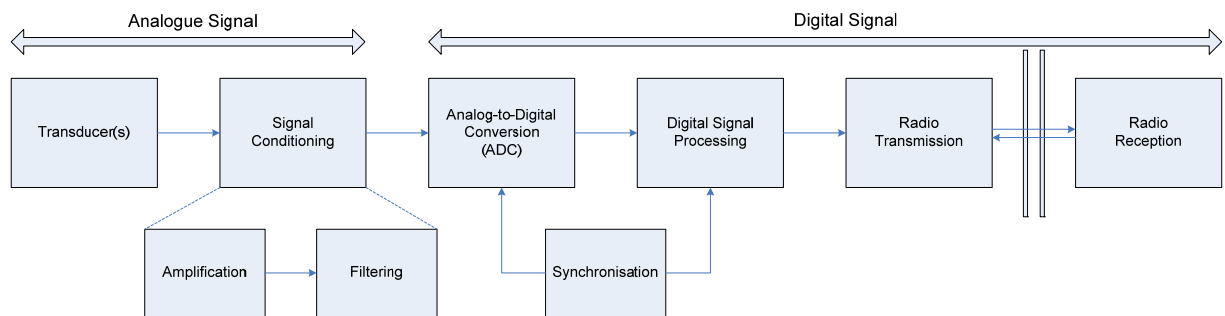
Figure 3.1: The block diagram of the conceptual monitoring system.

The aim of the first part of this chapter is to discuss the requirements of each building block, as well as explore the different design options with varying functionality, and present the solution that appears to be the most practical for long-term monitoring, in terms of miniaturisation, power consumption, or functionality. We will first define the sensor's physical characteristics; followed by the power supply requirements since the sensor will be battery operated; and then each of the building blocks of the sensor will be defined in turn.

3.2.1 Physical Characteristics

It was mentioned in the previous chapter that we are proposing to develop a sensor that will be unobtrusive in nature and will not interfere with the wearer's daily activities. Thus to satisfy this requirement, the sensor must be both small in size and light in weight.

A sensor that has been envisioned will have dimensions similar to a 50p coin (about 3 cm in diameter), although somewhat thicker – 1.5 to 2 cm thick. Additionally, the sensor should not weigh more than a hundred grams (g).

3.2.2 Power Supply

For the sensor to be mobile, it must be powered using a battery. Therefore, in this section, currently available battery technologies will be discussed. Battery technologies can be categorised into two main types:

1. Primary or non-rechargeable, and

2. Secondary or rechargeable.

Primary batteries are non-rechargeable and need to be replaced after they run out. However, they have two very desirable characteristics – a very high energy density compared to secondary batteries and a long storage time, translating to a good operational readiness.

Secondary batteries have become more increasingly used in recent times with the introduction of mobile electronics. In these applications, the batteries are used on a regular basis thus a lower cost of power is more practical. A single secondary battery can be recharged and re-used for hundreds of cycles, lasting for a year or even longer.

Since the proposed heart rate monitoring system will be operational almost continuously, therefore the use of secondary batteries are more suitable due to its low cost per recharge

cycle, reusability, and lower internal resistance (a requirement for digital and radio applications). The properties of secondary battery technologies are summarised in Table 3.1.

Table 3.1: General comparison of the properties for different secondary battery technologies [12]

	Nickel-cadmium	Nickel-metal-hydride	Lead-acid	Lithium-ion	Lithium-ion-polymer	Reusable alkaline
Gravimetric Energy Density (Wh/kg)	45-80	60-120	30-50	110-160	100-130	80 (initial)
Internal Resistance (includes peripheral circuits) in mΩ	100 to 200[1] 6V pack	200 to 300[1] 6V pack	<100[1] 12V pack	150 to 250[1] 7.2V pack	200 to 300[1] 7.2V pack	200 to 2000[1] 6V pack
Cycle Life (to 80% of initial capacity)	1500[2]	300 to 500[2,3]	200 to 300[2]	300 to 500[3]	300 to 500	50[3] (to 50% capacity)
Fast Charge Time	1h typical	2 to 4h	8 to 16h	2 to 4h	2 to 4h	2 to 3h
Overcharge Tolerance	moderate	low	high	very low	low	moderate
Self-discharge / Month (room temperature)	20%[4]	30%[4]	5%	10%[5]	~10%[5]	0.3%
Cell Voltage (nominal)	1.25V[6]	1.25V[6]	2V	3.6V	3.6V	1.5V
Load Current peak best result	20C 1C	5C 0.5C or lower	5C[7] 0.2C	>2C 1C or lower	>2C 1C or lower	0.5C 0.2C or lower
Operating Temperature[8] (discharge only)	-40 to 60°C	-20 to 60°C	-20 to 60°C	-20 to 60°C	0 to 60°C	0 to 65°C
Maintenance Requirement	30 to 60 days	60 to 90 days	3 to 6 months[9]	not required	not required.	not required
Typical Battery Cost[10] (US$, reference only)	$50 (7.2V)	$60 (7.2V)	$25 (6V)	$100 (7.2V)	$100 (7.2V)	$5 (9V)
Cost per Cycle (US$)[11]	$0.04	$0.12	$0.10	$0.14	$0.29	$0.10-0.50
Commercial use since	1950	1990	1970	1991	1999	1992
Toxicity	Highly toxic, harmful to environment	Relatively low toxicity, should be recycled	Toxic lead and acids, harmful to environment	Low toxicity, can be disposed in small quantities	Low toxicity, can be disposed in small quantities	Low toxicity, may contain mercury

1) Internal resistance of a battery pack varies with cell rating, type of protection circuit and number of cells. Protection circuit of lithium-ion and lithium-ion-polymer adds about 100mW.
2) Cycle life is based on battery receiving regular maintenance. Failing to apply periodic full discharge cycles may reduce the cycle life by a factor of three.
3) Cycle life is based on the depth of discharge. Shallow discharges provide more cycles than deep discharges.
4) The discharge is highest immediately after charge, and then tapers off. The capacity of nickel-cadmium decreases 10% in the first 24h, then declines to about 10% every 30 days thereafter. Self-discharge increases with higher temperature.
5) Internal protection circuits typically consume 3% of the stored energy per month.
6) 1.25V is the open cell voltage. 1.2V is the commonly used as a method of rating.
7) Capable of high current pulses.
8) Applies to discharge only; charge temperature range is more confined.
9) Maintenance may be in the form of 'equalizing' or 'topping' charge.
10) Cost of battery for commercially available portable devices.
11) Derived from the battery price divided by cycle life. Does not include the cost of electricity and chargers.

Batteries come in various shapes and sizes. The most widely used is the cylindrical cell (shown in Figure 3.2). It is easy to manufacture, offers the highest energy density, and provides good mechanical stability.
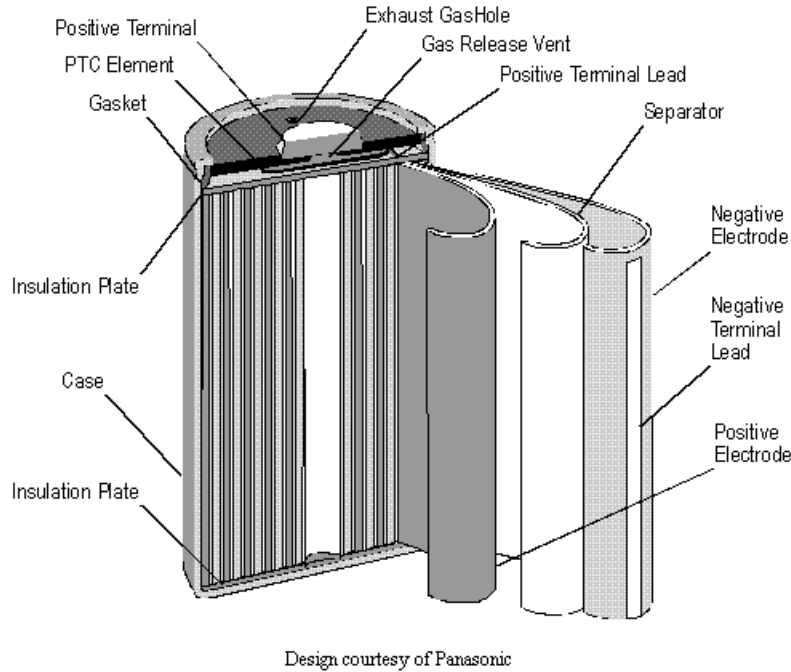
Figure 3.2: A cylindrical shaped battery cell [13].

Another type of packaging is in the form of a button or coin cell (shown in Figure 3.3). It is typically thin and can be stacked together to give a higher output voltage. These cells are normally used in watches, hearing aids, and memory back-up.
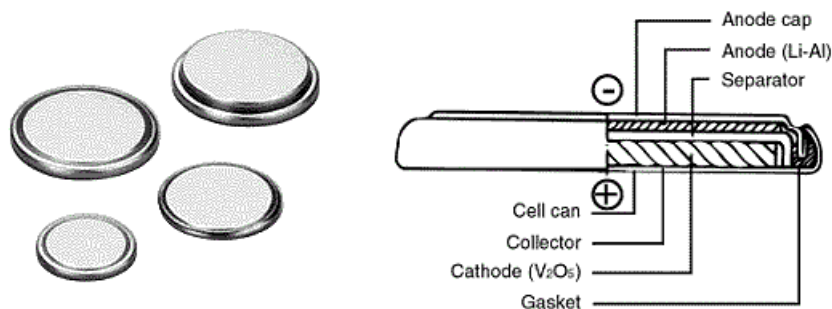
Figure 3.3: Button or Coin shaped battery cell [13].

Due to recent demands for ever thinner and more flexible cell dimensions, the prismatic (shown in Figure 3.4 a)) and pouch cell (shown in Figure 3.4 b)) were developed, both

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exclusive to the Li-Ion and Li-Ion-polymer technologies. Prismatic cells are made to order so there is no standard size. As for the pouch cell, the metallic enclosure is replaced by a heat-sealable foil allowing the cell to be tailored to the required shape and size. Hence, it has the best packaging efficiency of all the cell shapes. However, both of these cells have a relatively high manufacturing cost and a slightly reduced performance.
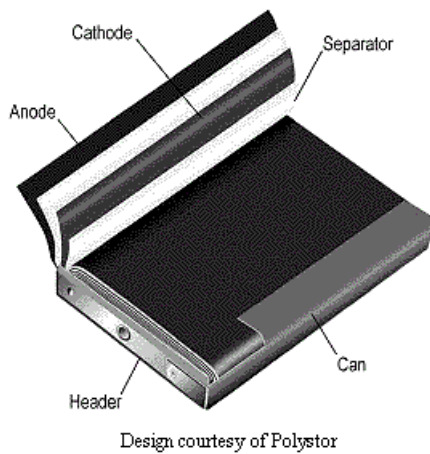
a)   b)

Figure 3.4: a) Prismatic battery cell and b) Pouch battery cell [13].

Following calls for ever thinner and lighter batteries, a thin and light all-polymer battery was developed by scientists at Johns Hopkins University [2]. This battery, illustrated in Figure 3.5, is rechargeable, highly flexible, has low temperature sensitivity, and can be shaped or moulded into the desired shape.
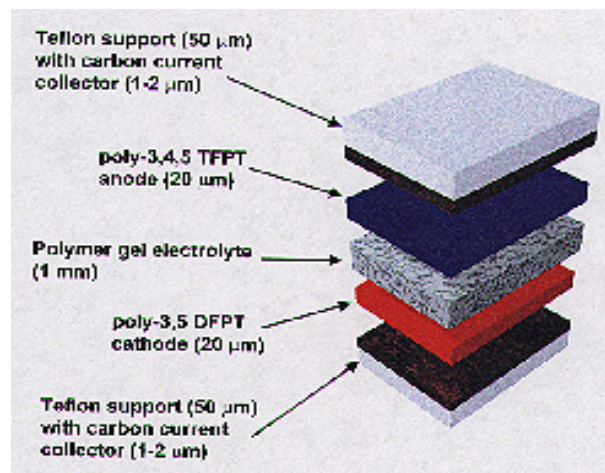
Figure 3.5: Different material content inside the all-polymer battery [2].

When selecting a battery technology for an application, we have to consider a number of factors on both the operational and the maintenance side. Operational issues include the cell voltage, the cell capacity versus its size, the maximum current of the circuit (i.e. the internal resistance), the cycle life, and the available shapes. Maintenance issues include the self-discharge, temperature sensitivies, the shelf-life, and the ease of charging.

Since our proposed system puts precedence on the size of the sensor, thus the size of the battery must be kept as small as possible. From this perspective, the button or coin shaped cell appears to be the most suitable. Furthermore, to effectively power the system, the cell voltage must be at least 3 Volts (V) to be suitable for low-voltage logic discrete components and have a high energy density to maximise the battery life to size ratio. The Li-Ion coin cell appears to be the most suitable with a cell voltage of 3.6V and energy capacities ranging from 10 to 200 milli-Ampere-hours (mAh), for cells with dimensions of 16 to 24.5 mm in diameter by 1.8 to 5.4 mm thick, and weight of 1.2 to 5.2 g.

In addition to having an energy source, it may be necessary to have a voltage regulator to stabilise the power supply so fluctuations in the cell voltage does not affect operation of the sensor's circuitry. This is because the cell voltage of a battery drops with increase usage or decreasing stored energy.

3.2.3 Phonocardiographic Transducer

In phonocardiography (PCG), an electrical representation of the heart sounds and murmurs is required. This can be obtained using a transducer to convert the mechanical vibrations into an electrical signal. The transducer should ideally reproduce the mechanical vibrations caused by the heart sounds and murmurs into an electrical form without any distortions and have equal sensitivities to vibrations at all frequencies i.e. a flat frequency response, especially at the lower end of the spectrum. This is because the normal heart sounds spectrum has spectra components at very low frequencies, <400 Hz, while the diseased heart sounds spectrum can have spectra components up to 1.2 kHz [28].

There are two main methods to record heart sounds: using air-coupled or direct coupled transducers [32]. In the air-coupled system, a small bell-shaped device, similar to the stethoscope head, is used to trap air when it is applied to the skin. This trapped air is used as the transmission medium between the chest surface and the mechano-electrical transduction membrane of the microphone. The air cavity created by the bell-shaped device increases the

surface area at the skin and helps to amplify the signal, due to the larger air volume. In the case of the direct-coupled system, a direct contact is made between the chest and the microphone. This method of recording is normally performed using a piezoelectric microphone [32] because a transduction membrane is not required. Thus, direct-coupled systems exhibit a better noise performance and higher sensitivity to low frequency vibrations. However the size of a piezoelectric microphone is relatively large (30 mm long by 12.5 mm wide) [28], thus it is unsuitable for miniaturisation. Still, due to recent advances in microphone technology, such as electret and MEMS silicon microphone, we are not only restricted to using the air-coupled method to obtain the PCG data.

In most of the developed PCG systems mentioned in the previous chapter, they have concentrated on using electret microphones in an air-coupled system [21,22,30] and condenser microphones in a direct-coupled manner [9]. For this research, a preliminary study was conducted into the ability to extract the heart rate information from PCG recordings [24]. The result from the preliminary study was favourable. The transducer that was used in that study was a miniature, surface-mount, silicon microphone manufactured by Knowles Acoustics, Model No. SPM0102NC3. This microphone is particularly small and more affordable than the condenser microphones of a similar size. Therefore, it was decided that the same type of transducer will be used. Furthermore, this type of microphones can exhibit higher sensitivity than other microphones, as an amplifier can be incorporated into the same silicon chip.

This silicon microphone has dimensions of 4.72 x 3.76 x 1.5 mm; and requires a supply voltage between 1.5V and 5.5V, a supply current between 0.1 mA and 0.25 mA, and has an output impedance of 100 Ohms (Ω). The heart sound recorded from the author's chest at the output of the microphone measured 5mV peak-to-peak, with a dc bias of 1.5V.

It has already been mentioned that PCG recording systems are particularly susceptible to ambient acoustic noise. Thus, an effective de-noising algorithm must be installed to remove any signal that may interfere with the quality of the recorded heart sounds. Many post-processing algorithms have been developed for various applications. These include techniques known as Spectral Subtraction [10,11], Beamforming [29], Adaptive Noise Filtering [19,26,33], and more recently Wavelet Transform [14,18,20,22,30,34]. As part of an effort to find a solution to minimise noise, a second microphone will be added to provide an additional signal source to facilitate some of the post-processing techniques mentioned above and also to allow us to experiment with different microphone configurations.

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3.2.4 Signal Conditioning

In the signal conditioning block, a number of operations are performed on the captured analogue heart sound signal. In the preliminary study, the signal captured by the transducer was pre-amplified, amplified, and filtered using a high-pass and a low-pass filter, as shown by the block diagram in Figure 3.6 and by the circuit diagram in Figure 3.7, before it is passed to the analog-to-digital conversion (ADC) block. Since the signal from the Signal Conditioning block will be fed into an analog-to-digital converter (ADC), thus we also need to consider the input requirements of the ADC.

In the preliminary study, the analog-to-digital conversion was performed by PC software, PicoLog ADC-40. The ADC-40 is an 8-bit ADC and has an analogue input range from -5V to +5V. Therefore, a 10 V peak-to-peak signal or smaller is required at the output of the signal conditioning block. The combined amplification stage was designed to provide a gain of 1950 or 3900 (about 66 to 72dB), with the pre-amplification stage providing a selectable gain (using a switch) of 50 or 100 (34 to 40dB) and the amplification stage providing 39 (~32dB) times gain. The cut-off frequencies for the filters were 67 Hz for the High-Pass Filter (HPF) and 2.5 kHz for the Low-Pass Filter (LPF). The resulting analogue heart sound output signal obtained was fluctuating between minimal value of -5V to a maximal value of +5V, as required.

The signal conditioning block was implemented using operational amplifiers (op-amp) as the main component (shown in Figure 3.7). The Texas Instrument NE5532 op-amp was used. This model of op-amp exhibits a very low input noise voltage, V_{noise} of $5\,nV/\sqrt{Hz}$ at 1 kHz. This parameter is very important in the pre-amplification stage because the noise figure of the overall circuit will be largely dictated by the noise figure of the first gain stage and since our transducer output signal is quite weak – 5mV peak-to-peak. Thus, we need the input noise voltage to be lower than our signal by at least one order of magnitude. This op-amp also displays excellent attributes in the input resistance, unity-gain bandwidth, slew rate, and common-mode rejection ratio. However, the device requires a supply voltage of 6V and an operational current of 4 mA per op-amp, which is not realistic for a battery-operated sensor. Therefore, a more suitable op-amp has to be identified, which can operate from a Li-Ion cell voltage of 3.6V and consume a much lower quiescent current, say less than 0.5mA each.
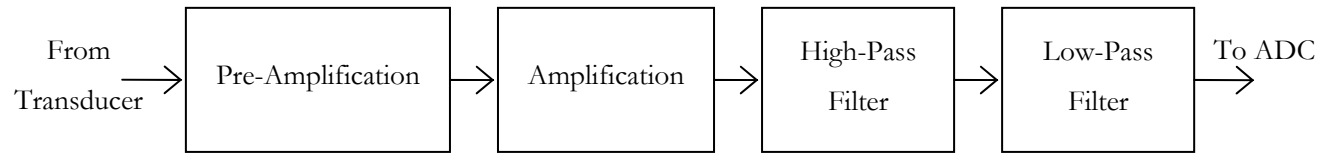
Figure 3.6: The block diagram of the Signal Conditioning circuit in the preliminary study.
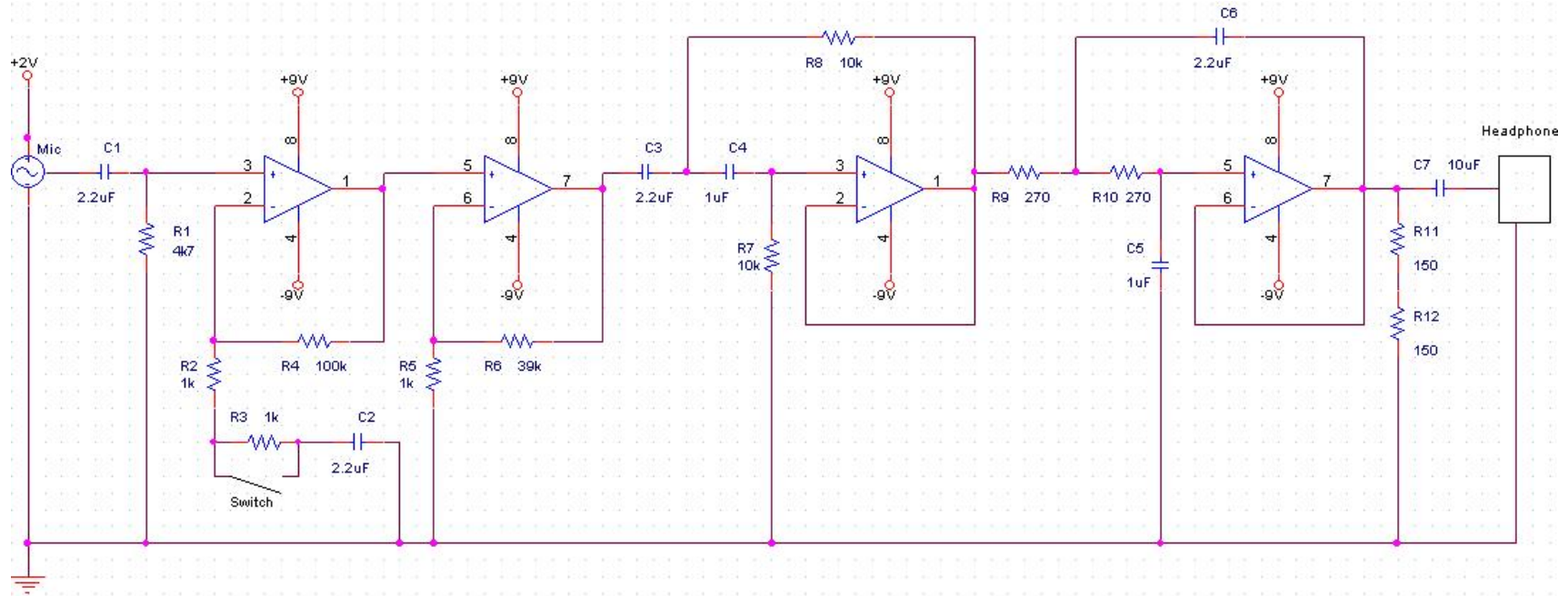
Figure 3.7: The circuit diagram of the Signal Condition block used in the preliminary study.

Furthermore, the V_{noise} should be less than $10\,nV/\sqrt{Hz}$ at 1 kHz for the first gain stage and no higher than $40\,nV/\sqrt{Hz}$ for the subsequent stages. The op-amp must display a high input resistance ($>1M\Omega$), a high unity-gain bandwidth (>100 kHz), a high slew rate ($>100V/ms$), a low input voltage offset ($<\pm0.5mV$), and a high common-mode rejection ratio ($>80dB$). Overall, the current consumption of this block should be minimised, to enhance battery life.

3.2.5 Analog-to-Digital Converter (ADC)

In the preliminary study, an 8-bit resolution ADC was employed to convert the analogue heart sound signal into a digital format for heart rate extraction. Although, the study showed that recording with 8-bit resolution was sufficient to deduce the heart rate, however it may be beneficial to have extra resolution. This is especially true when a complex digital processing task is performed on the signal, such as the de-noising operation of the heart sound data or the diagnosis of potential diseases using time-frequency analysis of heart sound (Figure 3.8). Therefore, an ADC with a 12-bit resolution will be used.
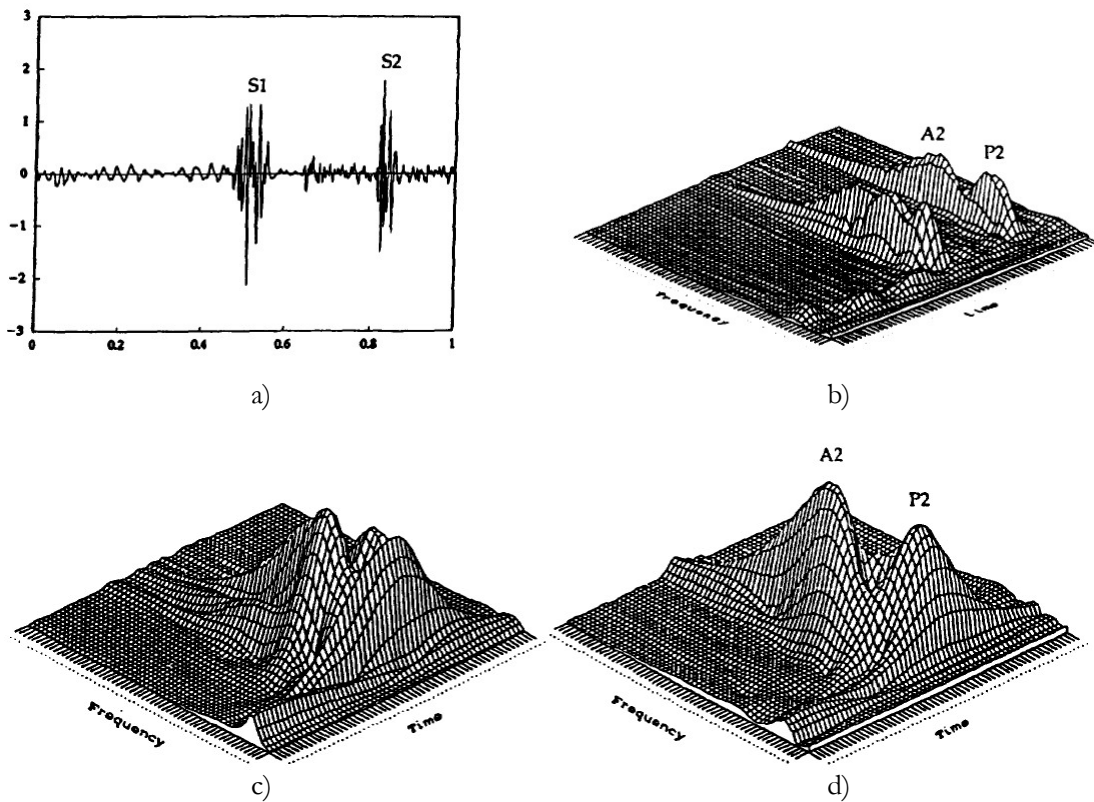
Figure 3.8: Wavelet Transform: a) One-second segment of a normal heart beat sound signal, b) Wavelet transform of (a), c) Wavelet transform of the first sound, S1, and d) Wavelet Transform of the second sound, S2 [23].

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Furthermore according to the Nyquist sampling theorem when sampling a continuous signal, the sampling frequency, f_s, must be at least twice the bandwidth or the maximum frequency, f_{max}, of the signal to be sampled for the continuous signal to be recoverable from the sampled data. In the preliminary study, the cut-off frequency for the low-pass filter (LPF) was 2.5 kHz, therefore the sampling frequency has to be at least 5 kHz or 5 ksps (kilo-samples per second). However, considering that a diseased heart can produce spectra components up to about 1 kHz [28], thus a sampling frequency of 2 ksps can be used without loss of diagnosis value.

There are many ADC architectures which include direct conversion, successive approximation, delta-encoded, ramp-compare, pipeline, and sigma-delta. A brief discussion of these architectures can be found in Appendix A.

At f_s = 2 ksps, the sampling rate is relatively low and most ADC architecture should have no problem performing this task. Thus, the crucial issue is to identify an off-the-shelf ADC that will perform the conversion using a 3.6V supply at a low current consumption – preferably less than 0.5mA. Furthermore, the ADC should exhibit an integral non-linearity (INL) of less than 1 Least Significant Bit (LSB), can be configured to have 2 inputs (one for each microphone), is small, and the digital inputs and outputs must be compatible with subsequent stages.

3.2.6 Digital Signal Processing

After the heart sound has been converted into a digital format, there are a number of options that can be considered, in terms of the level of signal processing onboard the sensor:

1. To send the data directly to the radio transmitter without any further processing,

2. To encode this digital data before radio transmission, and

3. To de-noise the data and/or to extract the heart rate before radio transmission.

To process the digital data, as in option 3, a programmable microcontroller (MCU) using code developed in a software suite on a PC is required. With today's powerful MCU, this feature would allow the sensor to perform a large variety of function including the de-noising operation, the heart rate extraction, and the encoding of data prior to radio transmission. In fact, the single-chip ADC can be removed as many microcontrollers now have an integrated ADC. Although, the integrated ADC is not as efficient in terms of power consumption as the

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single-chip ADCs, but by combining the ADC into the MCU this will help to conserve space on the PCB and the need for external synchronisation between the ADC and the MCU.

Even though, integrating an MCU into the sensor is advantageous in terms of functionality, however it was not included in this system level design because of the time constraints of this work. It was estimated that we would require up to 6 months to familiarise ourselves with the MCU, to effectively program, test, and integrate it into the sensor.

Therefore, a more practical choice must be made between option 1 and 2. Both options 1 and 2 will require much less time to develop the sensor. For this work, option 2 was chosen for its added benefit of having a data encoding scheme that allows for the detection of errors in the radio transmission process. In this option, the digital data is encoded using a simple Manchester encoding scheme, where a parity bit is used to detect errors. The Manchester encoding scheme is a widely accepted modulation scheme for low-cost radio frequency (RF) transmission of digital data [5]. It is essentially a form of binary phase shift keying (BPSK) that is very simple. It has two desirable characteristics – firstly, there are no long strings of continuous logic '0's or logic '1's that can be misinterpreted as an absence of signal, and secondly the encoding clock rate is embedded within the transmitted data. Both of these characteristics allow the use of inexpensive data-recovery circuits to decode the received data. The Manchester encoder converts the binary states of logic '0' and logic '1' into 2 binary bits '01' and '10' (as shown in Figure 3.9 a)) or '10' and '01' (as shown in Figure 3.9 b)).

a)   b)
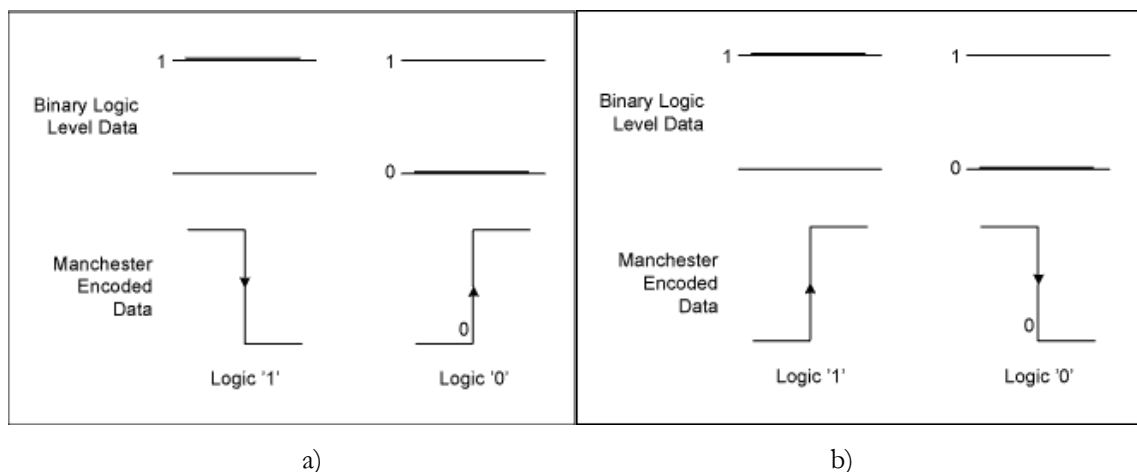
Figure 3.9: Equally valid alternate definitions of binary data as Manchester encoded information [5].

Using a Manchester encoder-decoder pair, error detection is made possible by ensuring that there are always an odd number of Manchester encoded data logic '1's in the Manchester encoded word. This is achieved by the introduction of a parity bit at the end of the

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Manchester encoded information to form a word. The parity bit is generated by counting the number of logic '1's in the binary data input; and if the number of logic '1's is *even*, then the parity bit will generate an extra Manchester encoded data logic '1'. However, if there are already an *odd* number of logic '1's in the binary data input, then the parity bit will generate a Manchester encoded data logic '0'. Thus, the error in the received data stream is detected when there are an *even* number of Manchester encoded data logic '1' in of Manchester encoded word.

Therefore, an off-the-shelf Manchester encoder-decoder pair is required to encode the digital heart sound data at the ADC's output, send the Manchester encoded data to the radio module for transmission, and also decode the data received by an RF receiver unit at a remote location. Once an encoder-decoder pair has been identified, the synchronisation between the ADC, the Manchester encoder, and the radio module will be considered. If an encoder-decoder pair cannot be found a microcontroller (MCU) can be used to generate the encoded data, although it would require more time to understand how to use and program the MCU.

Alternatively, the Manchester encoded word can be generated using an exclusive-OR (XOR) gate with the ADC output, of a specific data rate, at DATA IN input and a clock signal with the same frequency as the data rate of the ADC output at the CLOCK input, as illustrated in Figure 3.10. However, error detection is not possible in this case due to the absence of the parity bit.
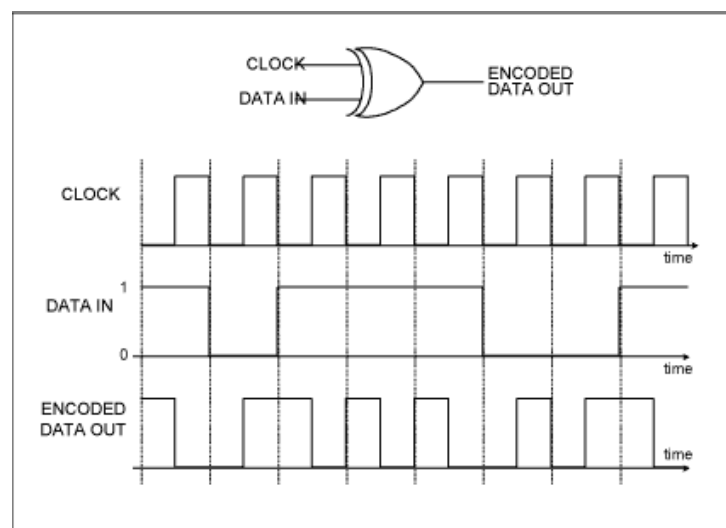
Figure 3.10: Manchester encoding by combining data-rate clock and serial data using an XOR gate [5].

3.2.7 Radio Communication

There are a number of possible radio communication technologies that can be utilised in the short and medium range transmission, as required by this application. This includes wireless technologies (and/or protocols) such as ZigBee, Bluetooth, RFIDs, and General ISM, which all operate in the globally unlicensed and unregulated ISM (Industrial, Science, Medical) bands, for example at 13.56 MHz, 433 MHz, 868 MHz (Europe), 915 MHz (North America), and 2.4 GHz.

Bluetooth (IEEE 802.15.1) is a well-established wireless technology. It operates in the 2.4 GHz ISM band, and is used for applications in mobile electronic devices. Since there are possibly many devices operating in the vicinity and the band is shared with Zigbee and WLAN, thus there is an issue with signal interference. Bluetooth deals with interference in two ways: one is to suppress interference by spreading the transmit signal over the whole ISM band i.e. Direct-Sequence (DS)-CDMA providing data rate up to 1 Megabits per second. Another method is called Frequency-Hopping (FH)-CDMA, where the interference is avoided by randomly changing the transmit frequency after each transmission packet. The range for Bluetooth is 10 metres without power amplifier [17].

ZigBee (IEEE 802.15.4 WPAN) is similar to Bluetooth and can operate in the 868 MHz (20kbits/s), 915 MHz (40kbits/s), and 2.4 GHz (250kbits/s) ISM bands. In all cases, the signal is transmitted using DS-CDMA with offset-quadrature phase shift keying (O-QPSK) for 2.4 GHz and binary phase shift keying (BPSK) at other lower frequencies. However, ZigBee is designed for lower data rate, low power point-to-point, and large (up to 254 nodes) wireless communication networks with range of 10-75 metres as standard [16,25].

RFID (Radio Frequency Identification) technology is very different from both Bluetooth and ZigBee. The main driving force for RFIDs is in the retail and logistics business, as this technology should eventually replace bar codes [31]. The simplest system consists of an interrogator or reader and a tag. The tags can either be passive (battery-less) or active (with internal battery). Passive tags can either be read-only or read and write by the reader. To read a passive tag, the reader must transmit enough energy to power it while this is not necessary for active tags. The advantage of this technology is its very low power consumption; however the range is reduced to a few metres or less, due to the nature of inductive coupling technique used for power transfer and communication.

General ISM radio modules are not application specific and some of them can be tailored to suit most needs with adjustable frequency bands, modulation schemes, and data rate.

A search of off-the-shelf radio transmitter must be completed to determine the most appropriate, in terms of the operating voltage that must be lower than the Li-Ion coin battery cell voltage of 3.6 V, current consumption that must be a few milli-Amps during transmission at most, data rate that must be 50 kbps or higher (2 channels x 12 bits x 2 k-samples per second = 48 kbps without encoding schemes, always on transmission) to allow data stream from both microphones to be transmitted to a remote location, and finally the small size to fit with the overall sensor's physical dimensions.

3.2.8 Antenna

Before an antenna can be chosen, the radio module must be selected first. This is because antennae are designed to work at a specific frequency, and this frequency must coincide or closely match the carrier frequency of the radio transmitter or receiver. Furthermore, the impedance of the antenna should also match that of the radio module's output impedance, which is normally 50Ω. Once both of these aspects are matched with the radio, the smallest and lightest available antenna will be used to minimise the dimension of the overall sensor. Please note that it may be useful to examine the directionality and gain of the antenna when comparing antennae of similar sizes.

3.2.9 Conclusion

In this section, a block diagram of the proposed monitoring system was formulated to represent the signal flow chart of the data acquisition chain. This consists of the transducer, the signal conditioning, the analog-to-digital conversion (ADC), the digital signal processing, the synchronisation, and the radio communication blocks. Furthermore, currently available off-the-shelf technologies and the specifications for each of these building blocks were discussed.

In the next section, the result of the search for the discrete, off-the-shelf components and the detailed design of the circuitry for each of the building blocks will be presented.

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3.3 Detailed Design

In this section, the detailed design of the circuitry for each of the building block of the sensor that were identified and discussed in the previous section is presented. Detail of the calculations and the criterion used for the selection of components are given. The main integrated circuit (IC) components were selected based on the system's specifications and their characteristics stated in datasheets. Other integrated circuit (IC) components were selected based on additional design needs for those blocks. Furthermore, any supporting components such as resistors and capacitors were selected based on the recommended design(s) given in the datasheets or fundamental design specifications such as providing gains for amplifiers and implementing cut-off frequencies for HPF and LPF.

The design process will begin from the voltage regulator to determine the regulated-supply voltage of the overall circuit, and will then proceed backwards from the radio communication block towards the transducer block to ensure that the output of the block before always satisfies the input of the next block. Please note that the full lists of components found in the initial search are documented in Appendix B of this thesis.

3.3.1 Voltage Regulator

Suitable voltage regulators, in terms of availability (at Farnell: uk.farnell.com) and output voltage close to 3.6V is presented in Table 3.2. There are many versions of the National Semiconductors LMS5214 and LP3982, which produce a different output voltage. The voltage regulators specified in Table 3.2 are the National Semiconductors LMS5214IMG-3.3 and LP3982IMM-3.3.

Table 3.2: Suitable voltage regulators found at Farnell (uk.farnell.com)

Manufacturer	Model No.	Output Voltage (V)	Current Output (mA)	Quiescent Current (µA)	Dimensions (mm)
National Sem.	LMS5214	3.3	80	70	2 x 2.4
National Sem.	LP3982	3.3	300	90	3 x 5

By comparing their attributes, the National Semiconductor LMS5214IMG-3.3 was selected for its superior (lower) quiescent current consumption and smaller size. Furthermore, it requires

less passive components (capacitors) to support its operations. The circuit that can be used to set-up the National Semiconductor LMS5214IMG-3.3 as a 3.3V voltage regulator from a 3.6V Li-Ion rechargeable battery is shown in Figure 3.11.
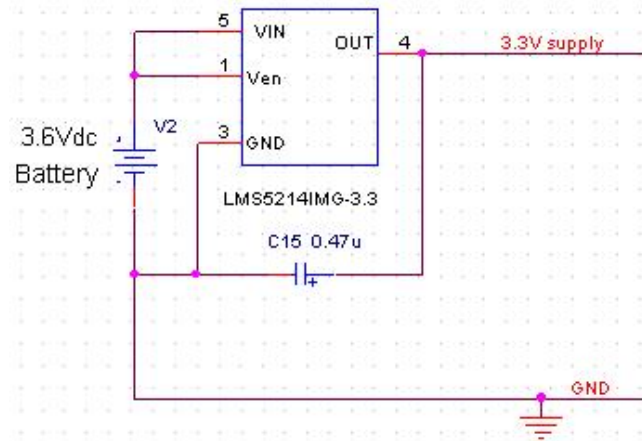
Figure 3.11: The voltage regulator circuit diagram with a 3.6V Li-Ion battery.

3.3.2 Radio Transmitter & Antenna

A wide search for off-the-shelf radio transmitters, receivers and transceivers was conducted at reputable manufacturers' internet site. Table 3.3 presents the radio transmitters and transceivers that were found to satisfy most of the system's specifications stated in the previous section.

Table 3.3: The radio transmitters and transceivers found to satisfy most of the system's specifications

Manufacturer	Model No.	Freq. (MHz.)	Data rate (kbps)	Modulation	Current Consumption TX (mA)	Dimensions (mm)
Analog	ADF7012	315/433/ 868/915	179/64	FSK, GFSK	16 @ 0dBm	7.8 x 6.4
Atmel	ATR2406	2.4 GHz.	1152	GFSK	0.5 @ 10kbps	5 x 5
Radiometrix	UHF TX2	433	160	FM	4 @ 0dBm	32 x 12 x 3.8
Radiometrix	UHF TX3A	869/914	64	FM	7.5 @ 0 dBm	32 x 12 x 3.8
			RFID			
Atmel	AT88RF001	13.56	106	n/a	0.44	10 x 6.2 x 1.

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The four radio modules at the top of Table 3.3 belong to the General ISM class of RF transmitter and transceivers, while the one at the bottom is specifically designed for RFID applications. Although, the RFID radio module appears to be an excellent choice with a very low current consumption – 0.44 mA. However, the datasheet was unclear about the modulation of the signal, the power consumption of the device at the specified data rate, and the range of the device, which in the worst case could be only a few centimetres.

The second best radio module appears to be the Atmel ATR2406 radio transceiver. However, this module operates in the 2.4 GHz range, which may experience significant interference from other wireless technologies, such as Wireless LAN and Bluetooth.

In the end, the Radiometrix UHF TX2 (shown in Figure 3.12), which operates at 433 MHz, was chosen for its ease of use (serial digital data can be directly applied to the TXD input without any control signals or synchronisation), low current consumption (4 mA @ 0dBm), and the support for high data rate (160 kbps). Although, the size of this radio transmitter module is quite large but this radio module can still be used at present to illustrate the feasibility of the proposed wireless sensor platform and can be easily replaced at a later stage.

a)   b)

c)
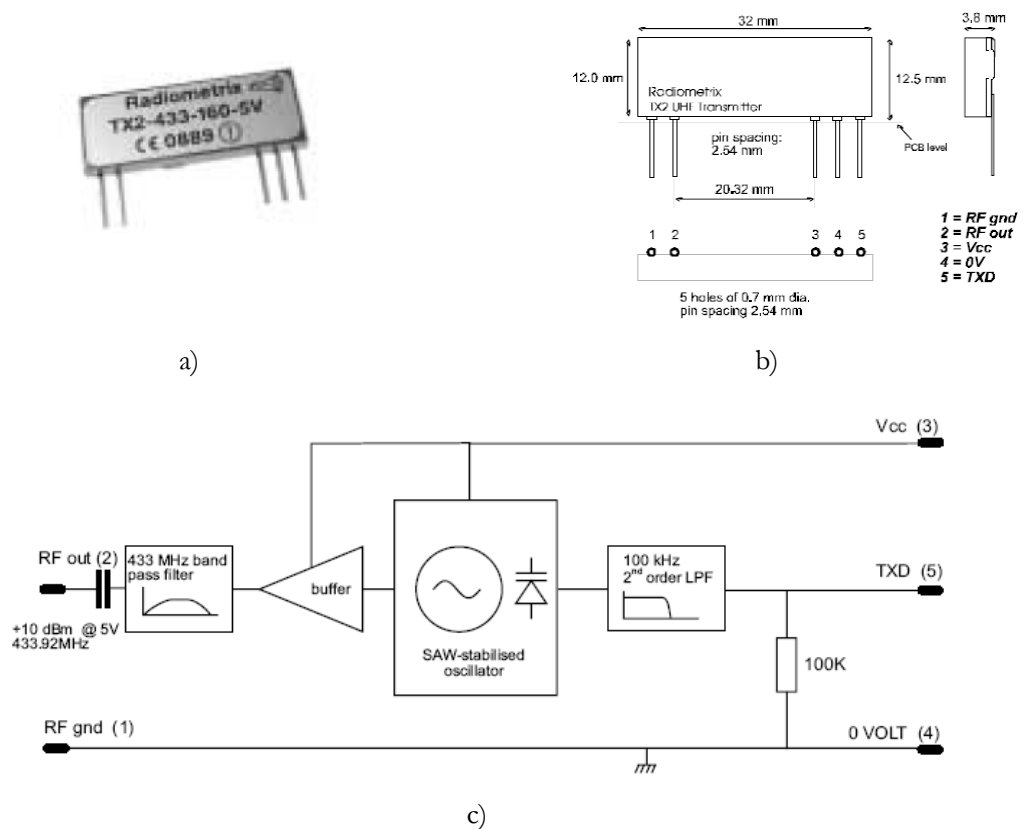
Figure 3.12: The Radiometrix UHF TX2 radio module – a) actual-size module, b) pin description, and c) block diagram [6].

Table 3.4 presents the search result of the antennae compatible with the Radiometrix UHF TX2's operating frequency of 433 MHz.

Table 3.4: Suitable antennae for operation at 433 MHz

Manufacturer	Frequency (MHz.)	Azimuth	Impedance (Ω)	Dimensions (mm)
PHYCOMP	433	Omni	50	6.8 x 37.5 x 0.90
Linx Tech.	433	n/a	50	28 x 13.7 x 1.6
Perseus Tech.	430	n/a	50	15 x 2 x 1.2
TriCome	433	Omni	50	30 x 7 x 1.8

Figure 3.13: The Tricome 433 MHz antenna (actual size) [3].

The antenna by Perseus Technology is the smallest out of all the suitable antennae, however it is not readily available therefore the antenna by Tricome (Figure 3.13), the second best in terms of size, was obtained from a local supplier.
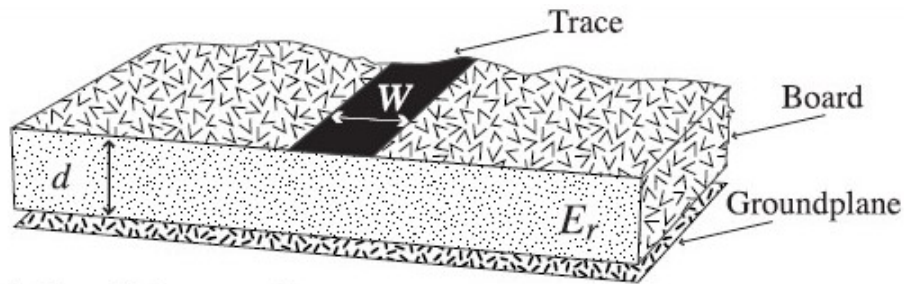
$$E_e = \frac{E_r+1}{2} + \frac{E_r-1}{2} \cdot \frac{1}{\sqrt{1+12d/W}}$$

$$Z_0 = \begin{cases} \dfrac{60}{\sqrt{E_e}} \cdot \ln\left(\dfrac{8d}{W} + \dfrac{W}{4d}\right) & \text{For } \dfrac{W}{d} \leq 1 \\[4mm] \dfrac{120\pi}{\sqrt{E_e} \cdot \left(\dfrac{W}{d} + 1.393 + 0.667 \cdot \ln\left(\dfrac{W}{d} + 1.444\right)\right)} & \text{For } \dfrac{W}{d} \geq 1 \end{cases}$$

Figure 3.14: The equations used for calculating the dimension of the microstrip [15].

In radio communication, maximum power transfer is important between the radio module and the antenna to maximise the communication performance versus the power consumption of the communication system. For maximum power transfer, the radio module and the antenna are normally connected using a transmission line to match the impedance of both the radio module's output and the antenna's input. The transmission line can be implemented on a PCB as a microstrip of a certain width depending on the PCB material (dielectric constant) and thickness. The width can be calculated using the equations shown in Figure 3.14. Furthermore, since the microstrip impedance is perfectly matched (in value) to both the radio module's output and the antenna's impedances, thus the network is considered to be 'perfectly broad-band matched' [31]. However, this is only required if the connection length exceeds one eighth of the wavelength of the transmission frequency inside the PCB medium (~4 cm for Er = 4.5). Since the expected connection length is only 1-2 cm for our design, therefore a microstrip line is not necessary.

Figure 3.15 illustrates the circuit diagram of the radio transmitter block with the Radiometrix UHF TX2 (TX2-433-160-3V) and the Tricome 433 MHz antenna.
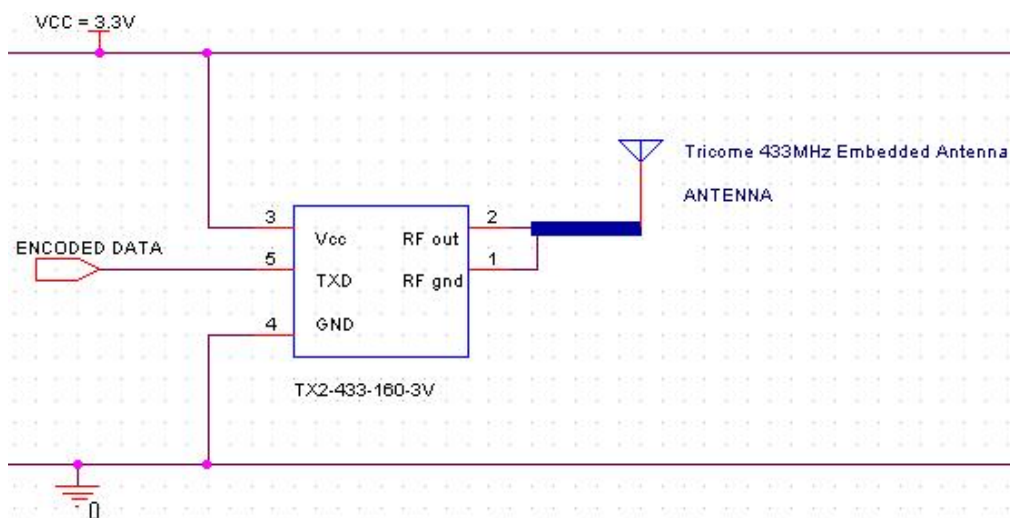
Figure 3.15: The circuit diagram of the radio transmitter block.

3.3.3 Analog-to-Digital Converter (ADC) & Manchester Encoder

After a thorough search for a discrete, off-the-shelf analog-to-digital converter (ADC), the Linear Technology LTC1285/8 series was chosen because it satisfies the system's specification discussed in the previous section. Also, it can be obtained relatively easily from the local supplier in the dual inline package (DIP), which is simple to test with. Table 3.5 summarises some of the Linear Technology LTC1285/8 properties as specified on its datasheet.

Table 3.5: A summary of the properties of the Linear Technology LTC1285/8

Manufacturer	Model No.	Max f_s (ksps)	No. of Channels	INL (LSBs)	Supply Volt. (V)	Current Consumption Active (mA)	Dimensions (mm)
Linear Tech.	LTC1285 /8	7.5 /6.6	diff (1285) /2 (1288)	0.75	2.7-6	0.04 @ 2ksps	3 x 3

For the Manchester encoder-decoder pair, only one suitable integrated circuit (IC) was found to operate at 3.3V. This was the Holt Integrated Circuit HI-15530, which contains both the encoder and the decoder in one IC. Fortunately, this IC came in both DIP and surface-mount packages. Similar devices to the HI-15530 were also found but they required a 5V supply, which is above the cell voltage of the Li-Ion rechargeable battery (3.6V).

3.3.4 Synchronisation Circuit

By examining the timing diagram of both the LTC1285/8 (shown in Figure 3.16) and the HI-15530 (shown in Figure 3.17), synchronisation is required between these two ICs. The ADC requires the following digital input signals:

1. The Chip Select, $\overline{CS}$, input to enable the conversion cycle,

2. A clock signal, CLK, to drive the ADC's operation, and

3. A Digital Input signal, D_{IN}, only for the LTC1288 to select an input.

The Holt Integrated Circuit HI-15530 Manchester encoder requires the following digital input signals:

1. The ENCODER ENABLE input to enable the encoder,

2. The SYNC SELECT input to express the type of information being encoded,

3. A clock signal, SEND CLK IN, that must be twice the data rate of the signal applied at the SERIAL DATA IN input, and

4. The input data to be converted, SERIAL DATA IN.
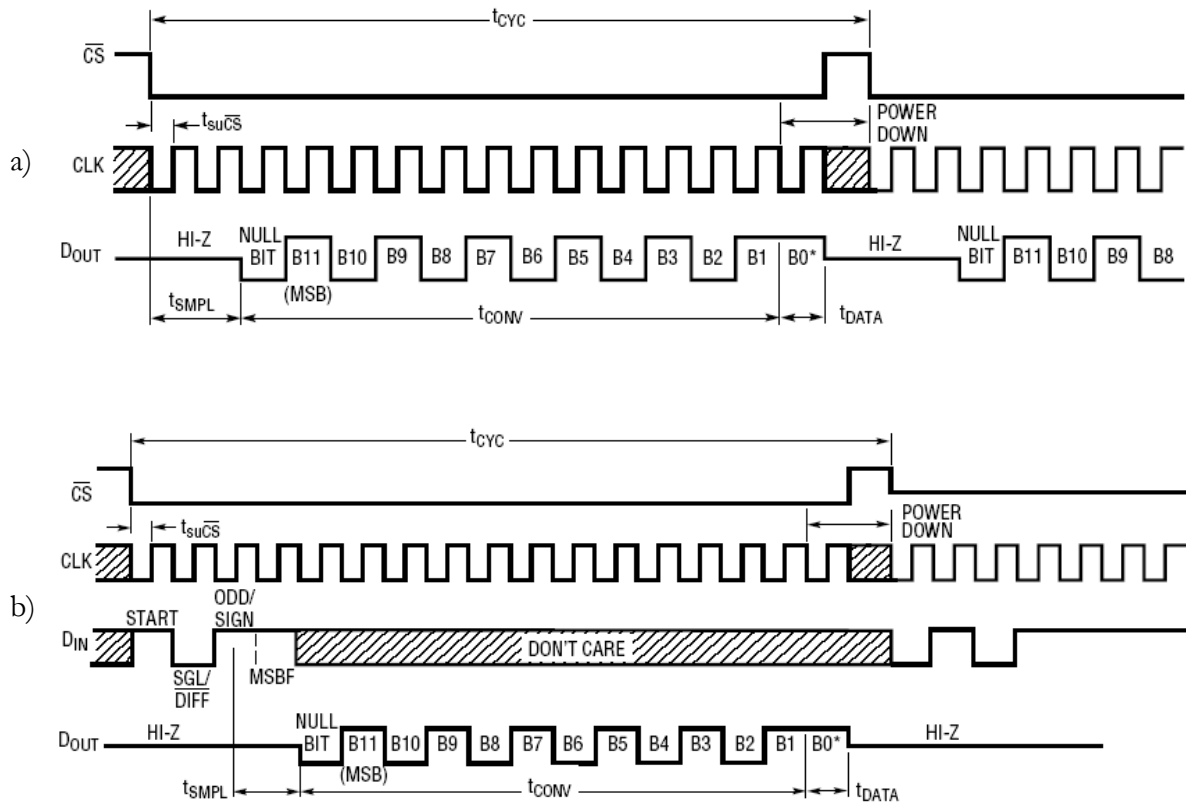
Figure 3.16: The Linear technology a) LTC1285 and b) LTC1288 operation timing diagrams [1].
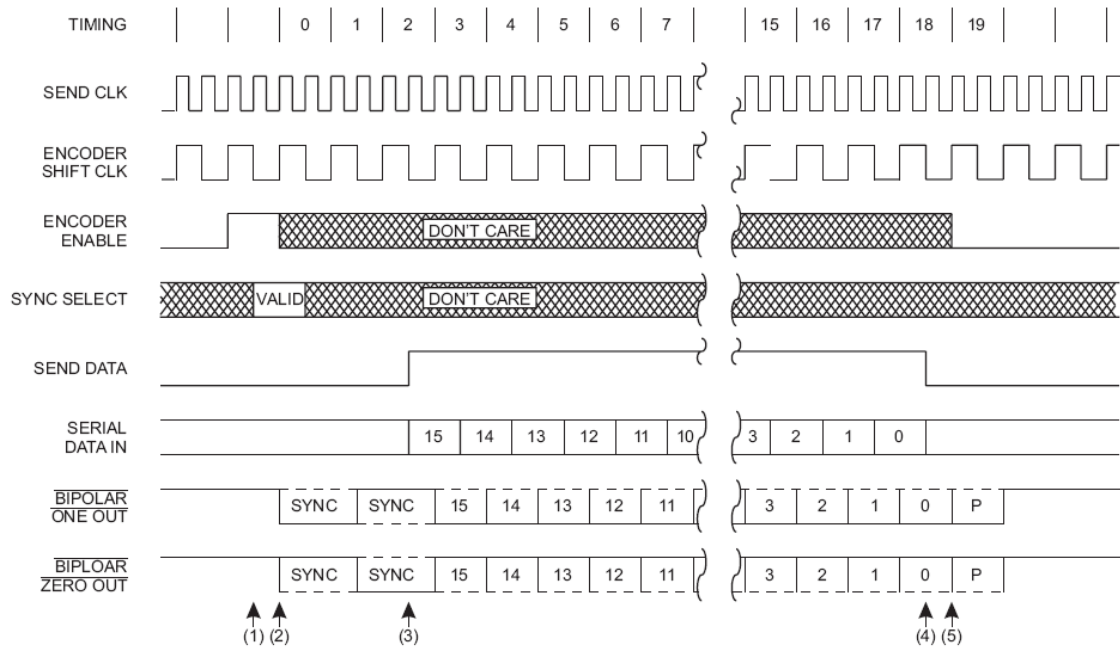
Figure 3.17: The Holt Integrated Circuit HI-15530 Manchester encoder operation timing diagram [4].

It should also be noted that the encoder requires a 16-bit data input word, while the ADC's output is only 12-bit. Therefore, a 16-bit encoder input must be generated. To achieve synchronisation, the control signals of both the ADC and the encoder must be co-ordinated in time with one another.

Clock Generation

A clock signal can be generated using crystal oscillators or oscillator circuits. However, the signal frequency generated by crystal oscillators are normally in the range of Mega-Hertz (MHz). For a 12-bit ADC with a sampling frequency of 2 ksps, the data rate at the output is only 2 ksps x 12 bits = 24 kbits per second (kbps) for one microphone, or 48 kbps for two microphones. If the crystal oscillator is going to be used, then the frequency of the crystal oscillator has to be divided by at least 20 times to bring it to tens of kHz.

From the operating characteristic of the Manchester encoder in Figure 3.17, it can be seen that each encoding cycle is 20 ENCODER SHIFT CLK cycles long, and one encoding is required for every analog-to-digital sample obtained. Thus, the frequency of the ENCODER SHIFT CLK needs to be 2 ksps x 20 ENCODER SHIFT CLK cycles = 40 kHz when only one microphone is sampled, and 80 kHz when both microphones are sampled. However, the ENCODER SHIFT CLK is an output generated by the encoder, through halving the frequency of the SEND CLK IN input. Therefore, the oscillator needs to generate an 80 or 160 kHz square wave for the SEND CLK IN input.

After a search of the local suppliers, the Linear Technology LTC6906 was found to be the most suitable. The LTC6906 is a resistor-controlled oscillator with an output frequency range between 10 kHz and 1 MHz. Furthermore, it consumes very little power - 12μA at 100 kHz on a 3.3V supply.

For simplicity, the detailed design process for the LTC1285 ADC will be illustrated. Thus, only one microphone or the difference between the two microphone signals can be sampled. Also by choosing the LTC1285, the SEND CLK IN frequency will be fixed at 80 kHz and the ADC's CLK input must be driven by a 40 kHz clock signal; therefore the ENCODER SHIFT CLK output of the encoder can be and will be used to drive the ADC's CLK input. Thus, the maximum data rate at the output of the ADC and the Manchester encoder will be 40 kbps and 80 kbps, respectively.

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Chip Select, $\overline{CS}$

Since the chip select control signal, $\overline{CS}$, directly times the ADC conversion during each Manchester encoding cycle, therefore it must repeat itself every encoding cycle or every 20 ENCODER SHIFT CLK cycles. To implement this repetitiveness, a ripple counter can be used to count the number of either the SEND CLK IN or ENCODER SHIFT CLK cycles with the counter resetting after 40 or 20 counts, respectively. For the current design, the ENCODER SHIFT CLK will be used to drive the counter.

The ADC's conversion cycle starts when the $\overline{CS}$ input is brought LOW (logic '0'). Additionally, the $\overline{CS}$ input must be held LOW until the conversion cycle is over. The most significant bit (MSB) or B11 is outputted first and appears 3 ENCODER SHIFT CLK cycles after $\overline{CS}$ goes LOW. If we align the timing so that the ADC's conversion cycle is complete on count 19, before the ripple counter is reset, we need $\overline{CS}$ to go LOW during the transition from count 4 to count 5 and returns HIGH (logic '1') when the counter is reset.

The Philips 7-bit ripple counter, 74HC4024, was found to be suitable (able to count up to 20) and locally available. The transition of the output Q with CLK input, for bit 1 (Q1) up to bit 5 (Q5), is illustrated in Figure 3.18.

This counter also has an asynchronous master reset (MR). A HIGH on the MR input clears all counter stages and forces all outputs LOW, regardless of the clock. Thus in our design, a HIGH will be applied to MR when the count is 20. This reset signal, R, can be formed by using an AND gate on the counter's output Q5 and Q3, which is true or HIGH for the first time at count 20 (see Figure 3.18). The AND operation is represented by a dot.

$$R = Q5 \cdot Q3 \tag{3.1}$$

To generate $\overline{CS}$, we require a device that will stay 'latched' in a state after it has been set and can be reset to a default state. A suitable device is the negative-edge triggered J-K flip-flop, M74HC107. Negative-edge triggered means that the transitions of the flip-flop occur on the falling edge of the clock signal. The truth-table for the negative-edge triggered J-K flip-flop and other digital functional blocks i.e. flip-flops and logic gates, are shown in Appendix C. The flip-flop can be reset by applying a LOW signal at the $\overline{R}$ input (an asynchronous input, which causes instantaneous transitions, independent of the clock signal).
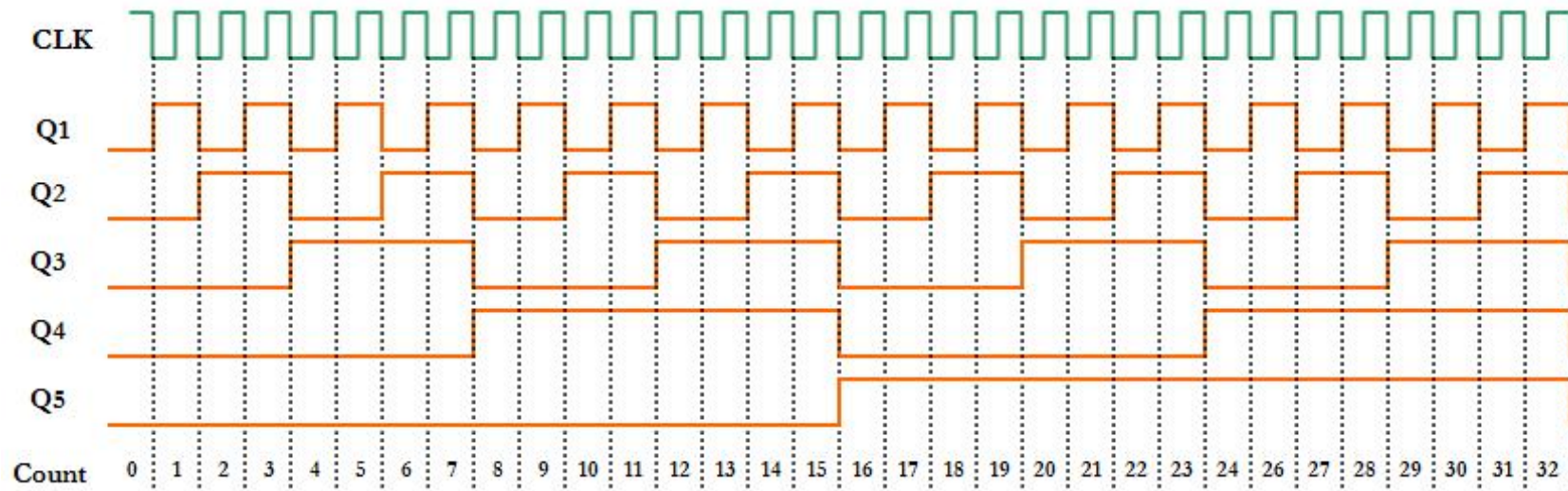
Figure 3.18: An illustration of the ripple counter's output transitions for bit 1, Q1, up to bit 5, Q5.

By examining its truth table and the counter's outputs, the digital circuit shown in Figure 3.19 can be used to generate the chip select signal, $\overline{CS}$, and the reset signal, R, using a 7-bit ripple counter, a negative-edge triggered J-K flip-flop, an AND gate, and a NOT gate. Figure 3.20 illustrates the timing diagram that is expected from the digital circuit in Figure 3.19.
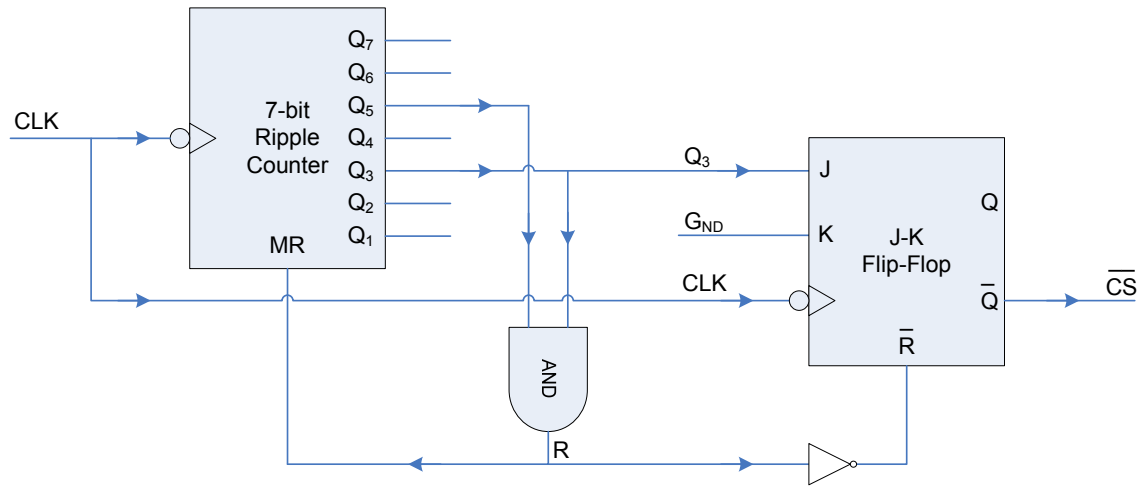
Figure 3.19: The digital circuit to generate the chip select signal, $\overline{CS}$, and the reset signal, R.
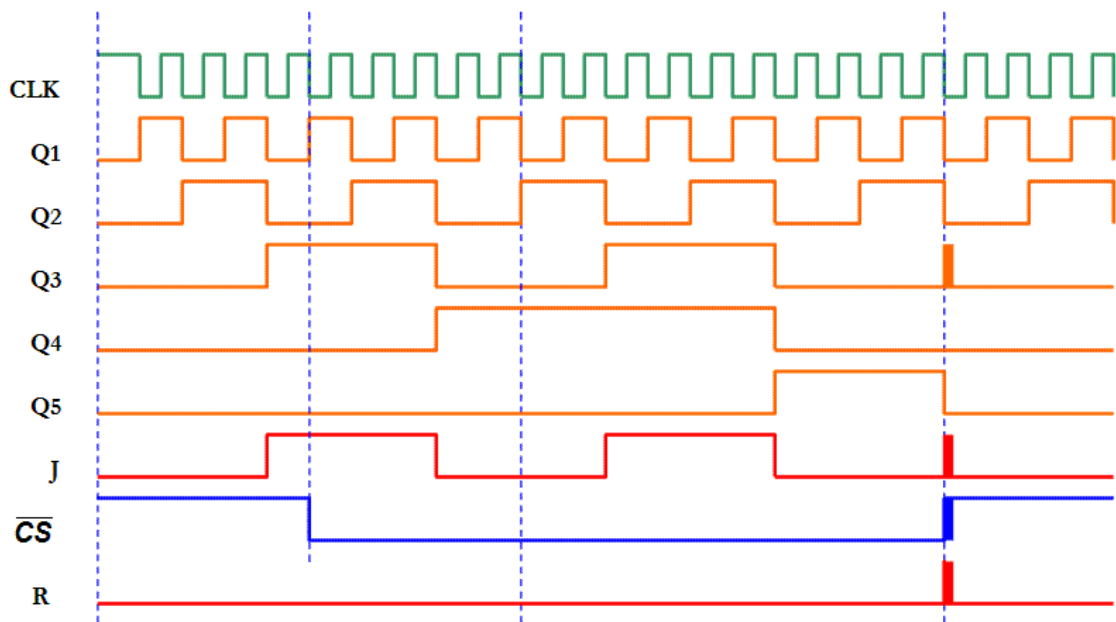
Figure 3.20: The expected digital timing diagram from the digital circuit in Figure 3.19.

Encoder Data Input (or BUFFERED DATA)

This signal is defined by the Holt Integrated Circuit HI-15530 Manchester encoder as a 16-bit word. To create this signal, we need to combine the 12-bit ADC output, D_{OUT}, signal with a 4-bit signal, say D_{IN}. As the ADC's output appears from count 8 to 19, we need to append 4 more bits from count 4 to 7 to the ADC's output. The easiest way to achieve this is by using logic gates with the truth table shown in Table 3.6. However to enable us to select between D_{IN} and D_{OUT}, an additional signal, CONV, has to be generated to determine whether the ADC is outputting signal or not. Thus, it is defined that when CONV is LOW, the ADC is outputting signals; and vice versa.

Table 3.6: Truth table used for generating BUFFERED DATA

CONV	D_{IN}	D_{OUT}	BUFFERED DATA
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

The truth table can be simplified using Karnaugh maps into the following Boolean equation:

$$\text{BUFFERED DATA} = \text{CONV} \cdot D_{IN} + \overline{\text{CONV}} \cdot D_{OUT} \qquad (3.2)$$

This Boolean expression can be constructed using AND (represented in the expression by a dot) and OR (represented in the expression by a '+' sign) gates as shown in Figure 3.21.
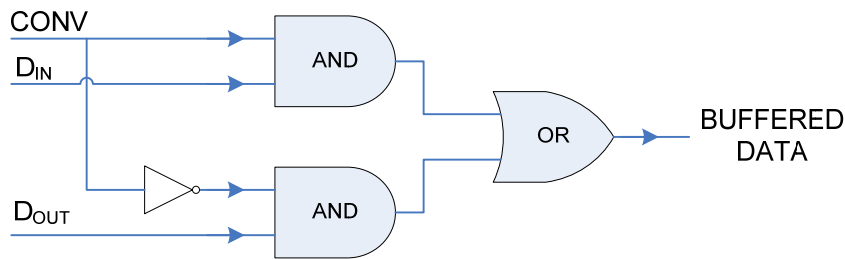
Figure 3.21: The digital circuit to generate the Encoder Data Input or BUFFERED DATA.

For the digital circuit in Figure 3.21 to select between the signals D_{IN} and D_{OUT} correctly, the signal CONV must be HIGH during count 4 to 7 for the BUFFERED DATA to be equal to D_{IN} during that period. Furthermore, CONV must be LOW during count 8 to 19 for BUFFERED DATA to be equal to D_{OUT}. Thus, the simplest way to generate CONV is for it to be HIGH between count 0 and 7 and LOW between count 8 and 19. Since Q4 is HIGH between count 8 and 15, and Q5 is HIGH between count 16 to 19, thus CONV can be generated by the following Boolean equation and thus the digital circuit shown in Figure 3.22:

$$CONV = \overline{Q5 + Q4} \tag{3.3}$$
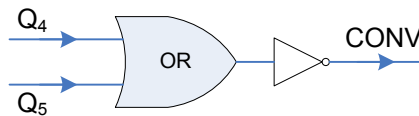
Figure 3.22: The digital circuit to generate the signal, CONV.
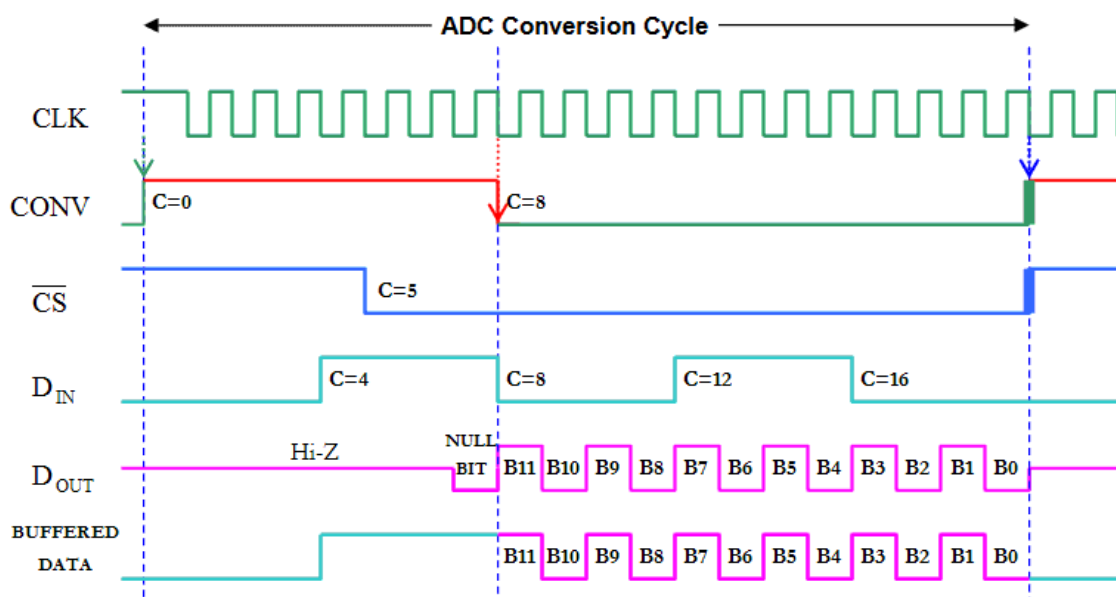
Figure 3.23: The expected digital timing diagram of the analog-to-digital converter (ADC).

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Figure 3.23 illustrates the expected digital timing diagram from the operation of the ADC with the synchronisation circuit designed thus far. It should be noted that the signal D_{IN} can actually be used to label the source of the data being transmitted, when we have two or more signal channels. However in the current design, the signal D_{IN} used will be the same as Q3.

ENCODER ENABLE

The timing of the ENCODER ENABLE signal is crucial in synchronising the operation of the Manchester encoder with the ADC. The encoding operation begins at the first instance when ENCODER ENABLE is HIGH, during a clock transition from HIGH to LOW or a negative-edge. Three ENCODER SHIFT CLK cycles after this, the SEND DATA output of the encoder goes HIGH and stays HIGH for 16 ENCODER SHIFT CLK-cycles.

Therefore to synchronise the encoder's operation with the ADC's, we must align this 16-bit 'HIGH' SEND DATA with the 16-bit BUFFERED DATA. Hence, the ENCODER ENABLE should become HIGH before count 1, so that the SEND DATA will be HIGH from count 4 to 19. To simplify things, we will set the ENCODER ENABLE signal to be HIGH at count 0 and remains HIGH thereafter.

SYNC SELECT

After the encoder is active on the falling edge of ENCODER SHIFT CLK, the logic level at the SYNC SELECT input is sampled, at the next rising edge of ENCODER SHIFT CLK, to determine the type of information being transmitted – either some data or a command. In our case, we are only dealing with the transmission of heart sound data, so the SYNC SELECT input will be permanently fixed at logic '0' or ground for data mode.

MASTER RESET

When the digital components power up, they do not start at a default state but from a random one. Furthermore, the devices that are most susceptible to the random starting position are the 7-bit ripple counter and the Manchester encoder. Since the counter directly controls the timing of the ADC and the Manchester encoder, therefore it is very likely that when the digital ICs are powered up, the encoder and the ADC will be out-of-sync.

Thus, a MASTER RESET circuit is required to synchronise the digital circuitry after the sensor is powered up. The circuit designed to do this particular job is a 'manual' reset that involves a push button and a J-K flip-flop. The Q output of this J-K flip-flop is then used to

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reset the counter, the J-K flip-flop for $\overline{CS}$, and the Manchester encoder. The $\overline{Q}$ output, on the other hand, will be used to supply the ENCODER ENABLE signal, because it becomes HIGH directly when MASTER RESET goes LOW at count 0.

Conclusion

The circuit diagram of the ADC and Manchester encoder can be viewed in Figure 3.24. The overall synchronisation circuit is shown in Figure 3.25. It requires 3 NOT gates, 3 OR gates, and 3 AND gates. For the OR and AND gates, standard Quad-OR and Quad-AND gates ICs were selected (74HC32 and 74HC08, respectively). However for the NOT gates, NAND gates were used instead (74HC00) because a NAND gate with its input tied together is equivalent to a NOT gate. Alternatively, both OR and AND gates can be constructed using NAND gates.

The expected full timing diagram of the digital circuitry is shown below in Figure 3.26.
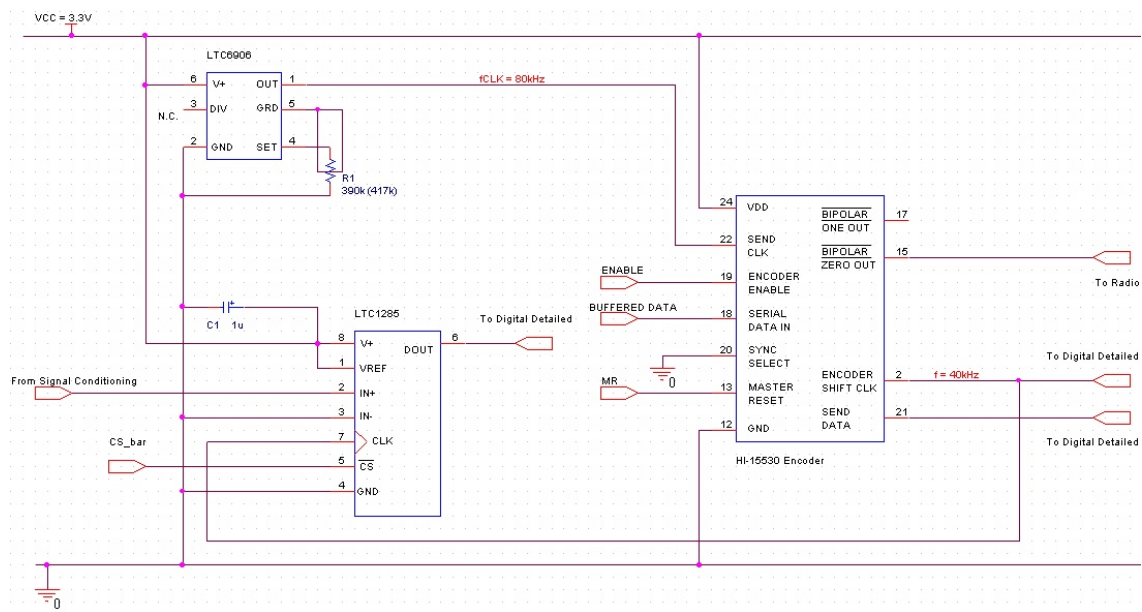
Figure 3.24: The circuit diagram of the ADC and the Manchester Encoder blocks.

3.3.5 Signal Conditioning

In the synchronisation section, it was decided that only one signal will be sampled by the ADC (LTC1285). So if we are going to perform 2-channel de-noising in the sensor, it can either be at the analogue stage or by using the differential inputs of the ADC. To de-noise at the ADC, two sets of signal conditioning circuits is required, one for each microphone. However for the analogue case, this may be reduced to one set by replacing an operational amplifier
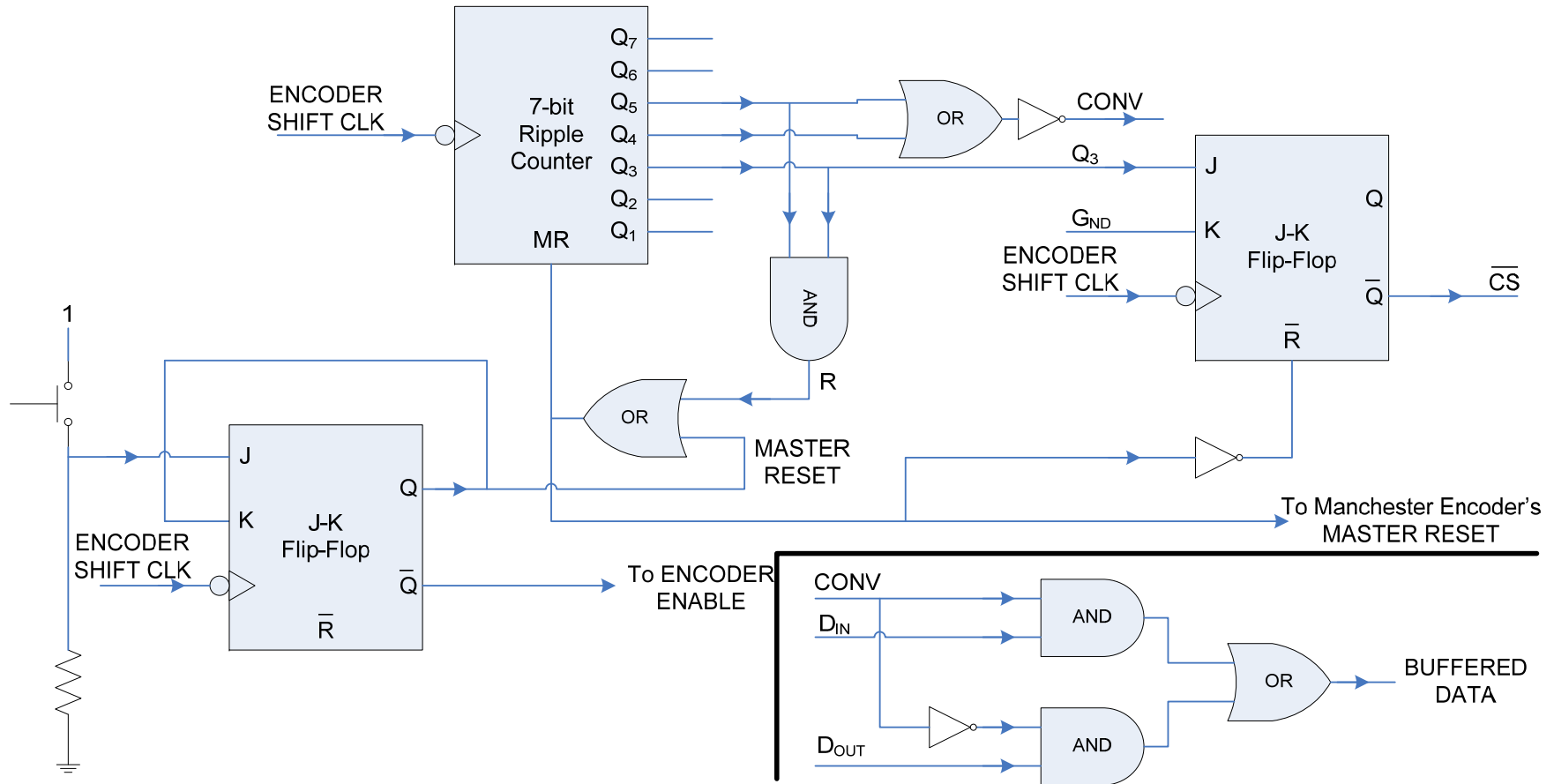
Figure 3.25: The overall digital circuit of the synchronisation circuit.

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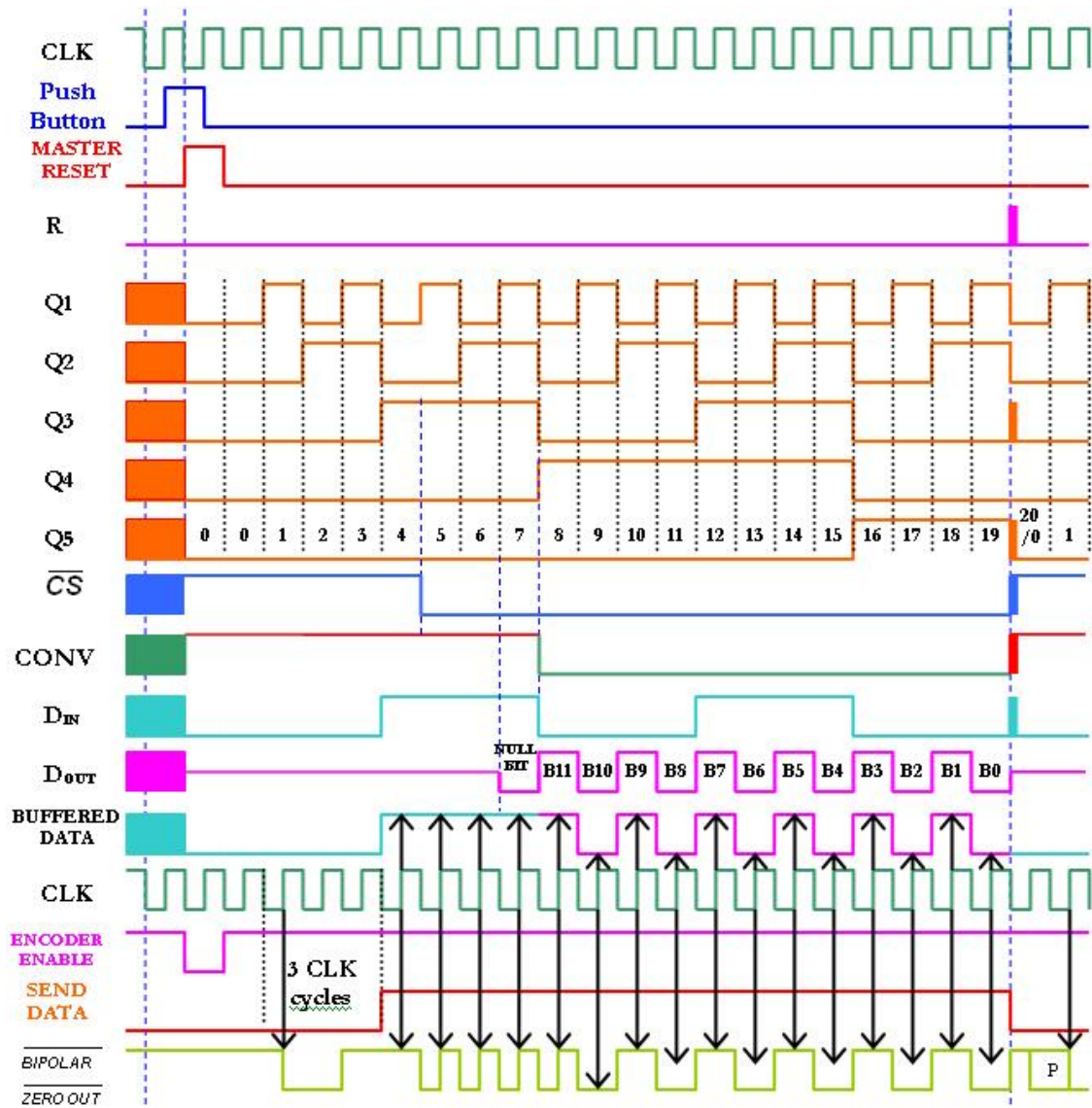
Figure 3.26: The expected timing diagram from the operation of the overall digital circuitry.

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with an instrumentation or differential amplifier, where the signal from each microphone is applied to a different input and the output is the difference of the two signals multiplied by some gain. The advantages of using an instrumentation amplifier (IA) are:

1. Superior stability and accuracy,

2. Very high common-mode rejection ratio (CMRR), and

3. Excellent electrical noise rejection in the supply (PSRR).

Thus in this design, an instrumentation amplifier (IA) will be used instead of operational amplifiers to amplify the differential signals from the two microphones to *potentially* de-noise the heart sound signal at the analogue front-end, which would allow us to use only one set of signal conditioning circuit. A number of suitable instrumentation amplifiers were found, but only one was available in the dual inline package (DIP). It was the Burr-Brown INA118 (shown in Figure 3.27), which has an input noise voltage, V_{noise} of $10\,nV/\sqrt{Hz}$ at 1 kHz, a maximum offset voltage of 50 μV, a bandwidth of 70 kHz at a gain (G) of 100, a slew rate of 900 V/ms, and requires less than 0.5mA of quiescent current.
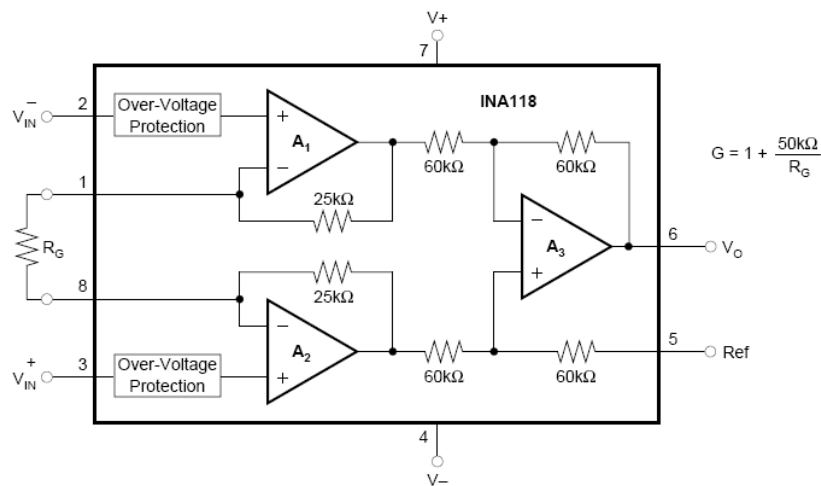
Figure 3.27: The pin-out and circuit diagram of the Burr-Brown INA118 [8].

The gain, G, of the Burr-Brown INA118 can be set by selecting the value of R_G, using the following equation:

$$G = 1 + \frac{50k\Omega}{R_G} \qquad (3.4)$$

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To amplify the heart sound signal received from the microphone (Knowles Acoustics SPM0102NC3, approximately 5 mV peak-to-peak) to a 3V peak-to-peak, this would require a gain of 700. This is a very high gain. Thus, an alternative model – SPM0103ND3, of the Knowles Acoustics microphone was considered. The alternative model has a higher sensitivity and a built-in amplifier which will help to reduce the gain required from the instrumentation amplifier. Thus, the value of R_G will not be determined at this point but after the heart sound signal level received from the Knowles Acoustics SPM0103ND3 has been determined.

It was decided that the input to both V_{IN}- and V_{IN}+ will be AC-coupled, as the microphone's output has a DC bias voltage, and biased by a common-mode voltage, V_{CM}, at about half the supply voltage or 1.65V. This bias voltage will also be applied at the Ref input (pin 5) to bias the output of the instrumentation amplifier, V_O.
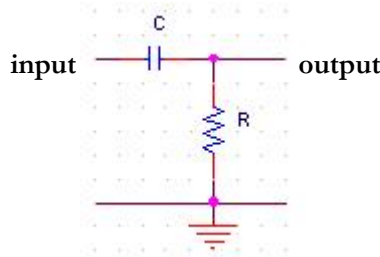
Figure 3.28: The RC network for AC Coupling.

An AC-coupling can be implemented using an RC network (shown in Figure 3.28). This has the effect of high-pass filtering the signal. We must make sure that the corner frequency of this does not affect our signal's spectrum. In the datasheet of the INA118, it states that an input bias current return path must be provided in the design. One example of this employs two 47kΩ resistors to connect each input terminal to ground. The corner frequency (CF) of the RC network in Figure 3.28 is given by:

$$CF = \frac{1}{2\pi RC} \tag{3.5}$$

Furthermore, the corner frequency should be much lower than 60 Hz, say 10 Hz. This gives a capacitance value, C, of about 0.33μF, given the resistor value of 47kΩ. A capacitance of 1μF was chosen instead because it was already in our possession; therefore the corner frequency with this capacitance value is approximately 3 Hz.

To effectively supply the common-mode voltage of 1.65V, a voltage regulator should be used. From a search, it was found that fixed voltage regulators can either supply 1.6 or 1.8V. A device that can operate with our input voltage level is the National Semiconductor LP3983. This device has models that can provide a regulated supply at 1.6, 1.8, and 2.5V from a 2.5V source, while drawing very little current and being very small (1 x 1.44 x 0.6 mm).

For the High-Pass and Low-Pass Filter, a search for a typical operational amplifier was conducted. The Maxim-Dallas MAX492 was found to have acceptable characteristics, with regards to current consumption, offset voltage, slew rate, and input noise voltage. The filters used in the preliminary study were Sallen-Key filters. Each Sallen-Key filter biquad requires two capacitors and resistors to generate two poles. The topologies for building a High-Pass (HPF) and a Low-Pass filter (LPF) are shown below in Figure 3.29. To achieve the correct cut-off frequencies, the component values for resistors and capacitors has to be calculated.

a)

b)
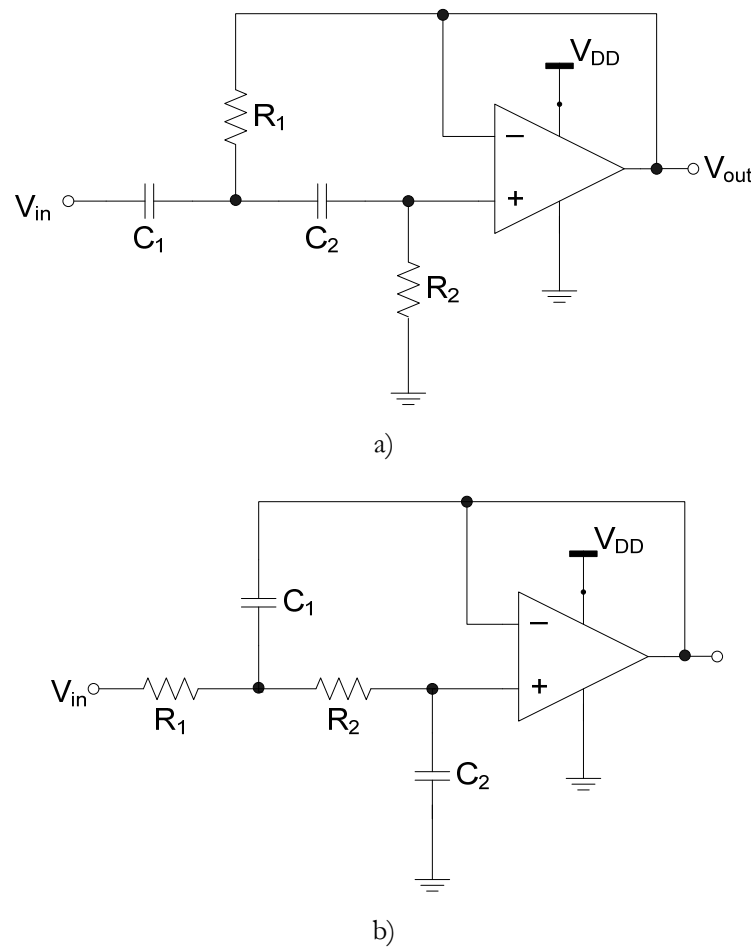
Figure 3.29: a) High-pass and b) low-pass Sallen-Key filter.

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Their cut-off frequencies, f_0, and quality factors, Q, of are given by:

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{3.6}$$

and

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{(R_1 + R_2)C_1} \tag{3.7}$$

While, the transfer function of the HPF and the LPF are:

$$H_{HPF}(s) = \frac{s^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \tag{3.8}$$

and

$$H_{LPF}(s) = \frac{\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \tag{3.9}$$

To build a Bessel band-pass filter using the above topologies, we need to determine the denominator coefficients for the HPF with a cut-off at 60 Hz and for the LPF with a cut-off at 1 kHz. The function *besself* in MATLAB was used to obtain the denominator coefficients. The coefficients for the HPF and LPF are [1, 652.97, 1.4212e+05] and [1, 10883, 3.9478e+07], respectively. If we set $R = R_1 = R_2$ and $C = C_1 = C_2$, and divide equation 3.6 by equation 3.7, we get:

$$\frac{\omega_0}{Q} = \frac{2\pi f_0}{Q} = \frac{2}{RC} \tag{3.10}$$

Thus, a design of equal-value resistors and capacitors is obtained. However, the value of Q determines the type of filter implemented, so Q can be controlled by making either $R_1 \neq R_2$ or $C_1 \neq C_2$. For the case of the LPF, it is decided that $C_1 = 4C_2 Q^2$; while for the HPF, it is $R_2 = 4R_1 Q^2$. This is necessary to minimise the sensitivity of these filters [27].

To calculate the component values of the HPF, the capacitors C_1 and C_2 were set at 10nF. Furthermore, by using equation 3.8 and the coefficients of the denominator obtained from MATLAB, we can calculate the value of ω_0 and Q:

$$\omega_0 = \sqrt{1.4212e + 05} \approx 377$$

$$Q = \frac{\omega_0}{652.97} \approx 0.577$$

Thus, the resistor values can be obtained using equation 3.6:

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \Rightarrow \omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\Rightarrow \omega_0 = \frac{1}{\sqrt{4 \cdot Q^2 \cdot R_1^{\ 2} C_1^{\ 2}}}$$

$$\Rightarrow R_1 = \frac{1}{2 \cdot Q \cdot \omega_0 \cdot C_1}$$

$$\Rightarrow R_1 \approx \frac{1}{2 \cdot 0.577 \cdot 377 \cdot 10 \times 10^{-9}} \approx 230\text{k}\Omega$$

$$\Rightarrow R_2 = 4 \cdot R_1 \cdot Q^2 \approx 4 \cdot 230\text{k}\Omega \cdot (0.577)^2 \approx 306\text{k}\Omega$$

Therefore, the component values of the HPF Sallen-Key filter are approximately $R_1 = 230\text{k}\Omega$, $R_2 = 306\text{k}\Omega$, with C1 and $C_2 = 10\text{nF}$. Using a similar procedure as shown above, the component values obtained for the LPF was $C_1 = 0.75\mu\text{F}$, $C_2 = 1\mu\text{F}$, with R_1 and R_2 set at approximately 183Ω. The nearest available component values are $220\text{k}\Omega$ and $330\text{k}\Omega$ for the HPF, and $1\mu\text{F}$ (both capacitors) and 180Ω (both resistors) for the LPF. The full circuit diagram of the signal conditioning block is shown in Figure 3.30.

3.3.6 Transducer

As mentioned in the signal conditioning section above, although the transducer that was used for the preliminary study, Knowles Acoustics SPM0102NC3 microphone, was found to be sufficient, however the heart sound signal that the microphone produces was very low at 5mV peak-to-peak, and therefore a large gain (= 700) is required to amplify it to a 3V peak-to-peak signal. Thus, another variant of the same microphone (SPM0103ND3) that has a higher sensitivity and also an integrated amplifier was chosen, instead. The same signal conditioning circuit can be used for this new microphone model; however the heart sound output signal level must be tested to determine the level of amplification required for this microphone.

3.3.7 Conclusion

In this section, the detailed design of the proposed sensor was conducted. The next task of the system level design is to perform an operational test on the circuit designed so far and fine tune these designs to overcome any problem that we may encounter in the testing process and was not foreseen at this detailed design stage.
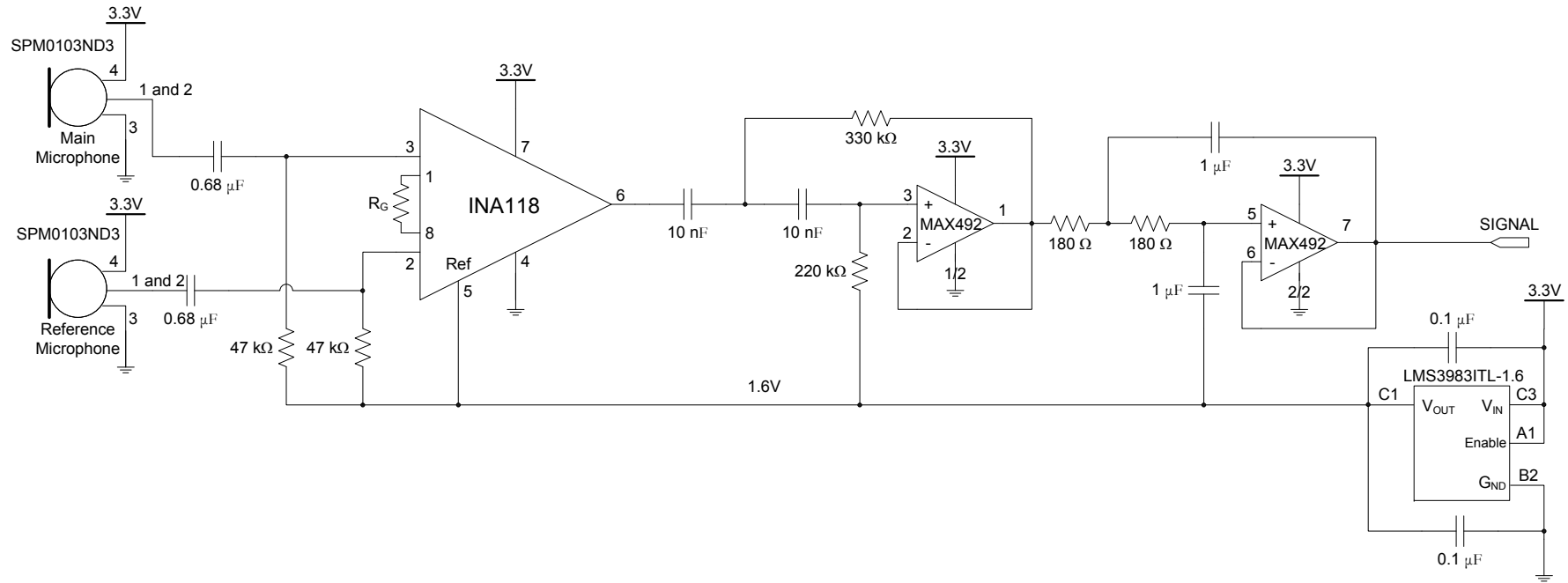
Figure 3.30: The overall circuit diagram of the Signal Conditioning block.

The operational testing results and the steps taken to eradicate any problem in the testing process will be presented in the next section of this chapter.

3.4 Measured Results & Discussion

An operational test was performed on the detailed design of the proposed sensor. In this section, the results of these tests will be presented along with a discussion on how the design can be improved based upon the problems encountered. We will first start with the microphone transducer block, and then move on to the signal conditioning, digital circuitry, and lastly the radio transmission blocks.

3.4.1 Microphone Transducer

Pin Output	
Pin #	Function
1	Output
2	Gain Control
3	Ground
4	Power
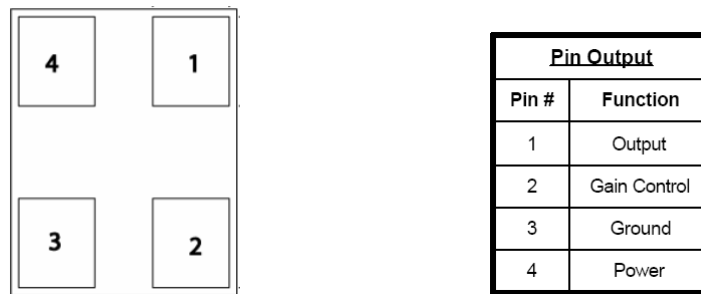
Figure 3.31: The pin-out of the Knowles Acoustics microphone, SPM0103ND3 [7].

The pin-out of the SPM0103ND3 microphone transducer, a variant of the SPM0102NC3 used in the preliminary study, is shown in Figure 3.31. As stated in the datasheet, the SPM0103ND3 microphone has a higher sensitivity (-22 dB @ 1kHz) than the SPM0102NC3 version (-42 dB @ 1kHz). Furthermore, it can be configured to provide up to 20dB of additional gain, which can be adjusted by adding R3 at terminal 2, as illustrated in Figure 3.32. While, C1 can also be put in to perform high-pass filtering with the corner frequency at:

$$CF = \frac{1}{2\pi(R2 + R3)C1} \tag{3.11}$$

In the test, the SPM0103ND3 was configured to provide a unity gain, where terminal 2 was connected directly to terminal 1, the output; terminal 4 was connected to a +3.3V supply; and

terminal 3 was connected to ground. The signal produced at terminal 1 was monitored using an oscilloscope.
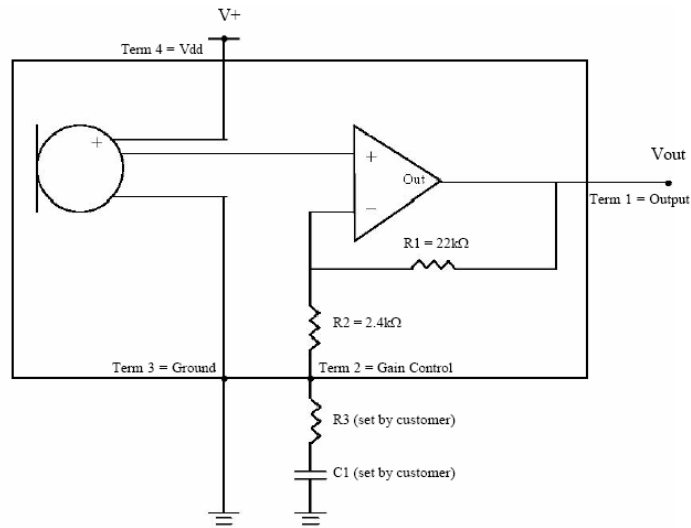
Figure 3.32: SPM0103ND3 Recommended Interface Circuit [7].

The author's heart sound signal was found to be about 25 mV peak-to-peak at rest (as shown in Figure 3.33), and can be up to 100 mV peak-to-peak after some exercise. With this microphone (Knowles Acoustics SPM0103ND3), the gain needed from the signal conditioning block to amplify a 100 mV peak-to-peak heart sound signal to a 3.3V peak-to-peak signal is only 33 times, compared to around 700 for the SPM0102NC3.
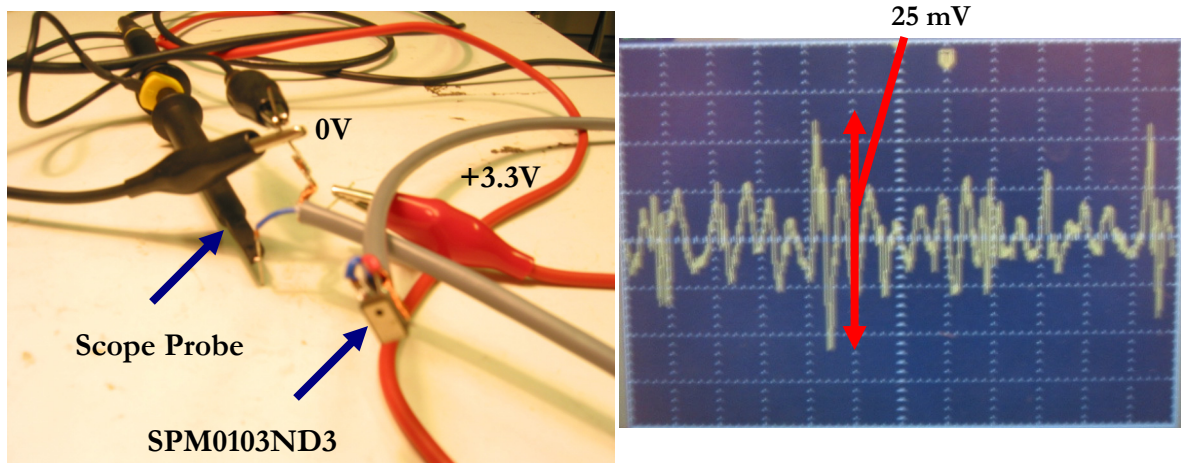
Figure 3.33: Knowles Acoustics SPM0103ND3 experimental set-up and result on the oscilloscope.

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3.4.2 Signal Conditioning

For the signal conditioning block, the instrumentation amplifier (Burr-Brown INA118) was tested on its own first with a signal generator as the input. After the instrumentation amplifier was operating in an expected manner, the microphones and the instrumentation amplifier were tested together. Next, the Sallen-Key filters were constructed and tested with a signal generator as the input first to obtain a plot the frequency response of the LPF and the HPF, before using the microphones as inputs to observe the signal conditioned heart sound signal at the output.

Instrumentation Amplifier

The instrumentation amplifier (Burr-Brown INA118) was set-up according to the circuit diagram shown in Figure 3.30; however the voltage regulators were replaced by bench power supplies. The set-up is shown in Figure 3.34. Firstly, the common-mode voltage, V_{CM}, was set at 1.65V and the gain at 10. A little experiment was conducted to determine the linear range of the instrumentation amplifier output. It was found that the amplifier becomes non-linear and exhibit clipping when the output voltage is above 2.76V or below 0.3V. Thus, the maximum swing that the instrumentation amplifier can provide is 2.73V, with a mean voltage of 1.665V.

$$V_{CM} = 1.65V$$
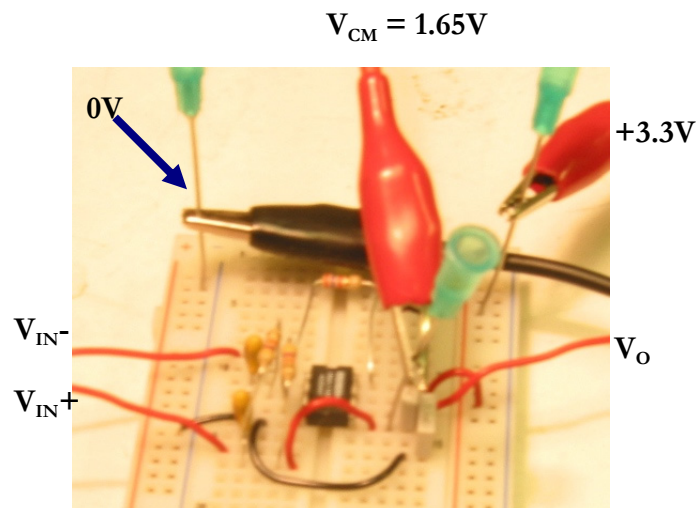
Figure 3.34: The set-up of the Instrumentation Amplifier, INA118.

Another experiment was completed to measure the common-mode voltage range for the output to remain linear, for different output swing and gain. The graphical result is shown in Figure 3.35.

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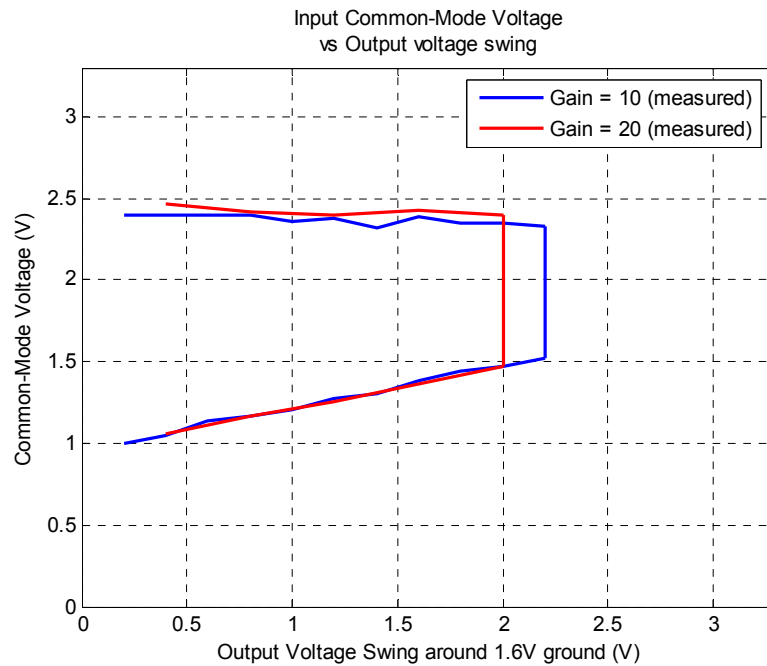
Figure 3.35: Common voltage, V_{CM}, range vs. output swing for linear operation.

From the graph in Figure 3.35, for a linear 2V output swing the common-mode voltage, V_{CM}, should be kept between 1.47V and 2.35V for a gain of 10 and between 1.47V and 2.4V for a gain of 20. When tested with the SPM0103ND3 microphones, the heart sounds were amplified by approximately the same amount set by the resistor, R_G, when the common-mode voltage was set at 1.65V.

From the results of the first two experiments, the greatest symmetrical output swing can be achieved by setting the common-mode voltage V_{CM} to 1.6V, using a voltage regulator. With this V_{CM}, the maximal symmetrical output swing is from 1.6V up to 2.76V and down to 0.44V, or 2.32V swing (compared to V_{CM} of 1.8V, maximal swing = 1.92V). However, some headroom should be provided so that the heart sounds signal is not distorted. Therefore, the final gain of the instrumentation amplifier was set to approximately 20 with R_G = 2.7 kΩ.

Sallen-Key Filters

The filters were set-up according to the circuit diagram shown in Figure 3.30. An experiment was performed to determine the frequency response of the HPF and LPF, the result of which is presented in Figure 3.36.
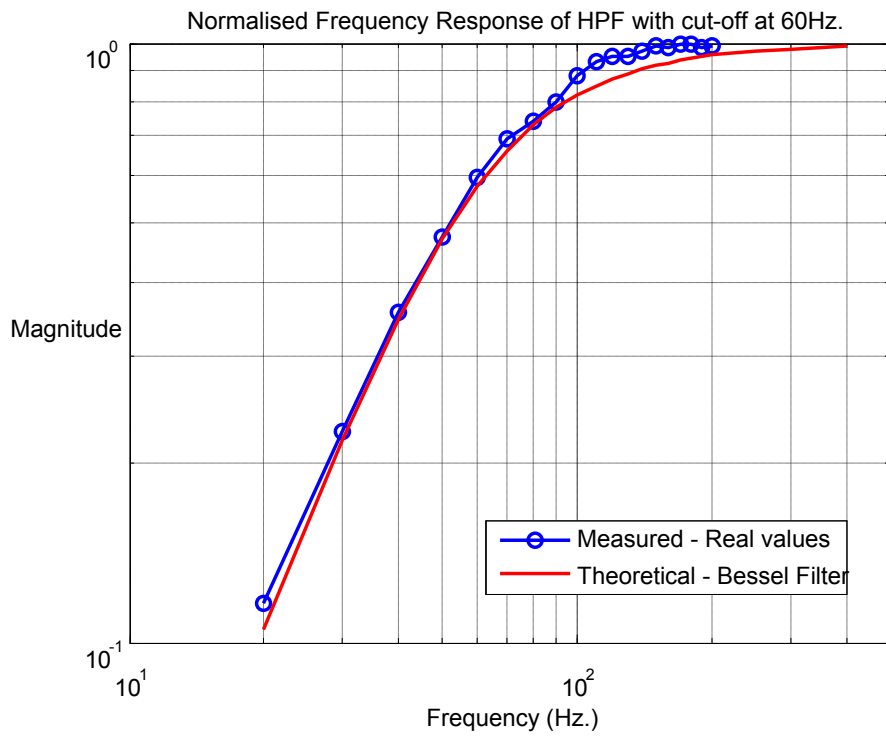
a)
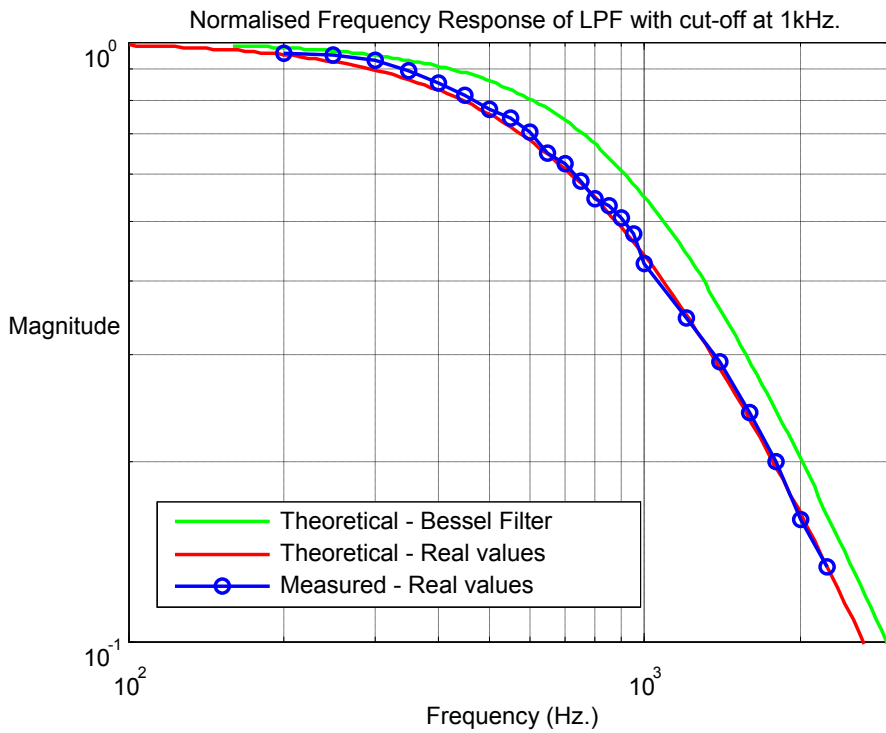
b)

Figure 3.36: Comparison between theoretical Bessel filter response and those obtained from experimental measurements a) for the high-pass filter (HPF), and b) for the low-pass filter (LPF).

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In Figure 3.36 a), the red line represents the theoretical response of the Bessel HPF, while the blue line represents the measured response. They are closely matched. In Figure 3.36 b), the green line represents the theoretical response of the ideal Bessel LPF; the red line represents the theoretical response with the real capacitor and resistor values; and the blue line was the measured response. The red and the blue line are closely matched. However, there is a significant difference between the measured response and the ideal Bessel response.

Furthermore, when the heart sound signal at the output of the Signal Conditioning block was observed, it was found that the heart sound was only amplified by a factor of 4 when the gain of the instrumentation amplifier was set at about 20. This implies that the filtering circuit was attenuating the heart sound signal by a factor of 5.

In a book edited by Webster [32], it stated that a PCG system must have a frequency response of 25 to 2000 Hz to reproduce heart sounds. Thus, the cut-off frequency of the HPF in the detailed design was too high (at 60 Hz) and needs to be lowered to 25 Hz or less. We decided to test two cut-off frequencies, 5 and 10 Hz, using different set of component values with fixed capacitance of 2.2µF, 1µF, and 10nF. Different sets were tested because in the initial testing there was a complication with using large capacitance value in the HPF circuit. The measured data are shown in Figure 3.37.
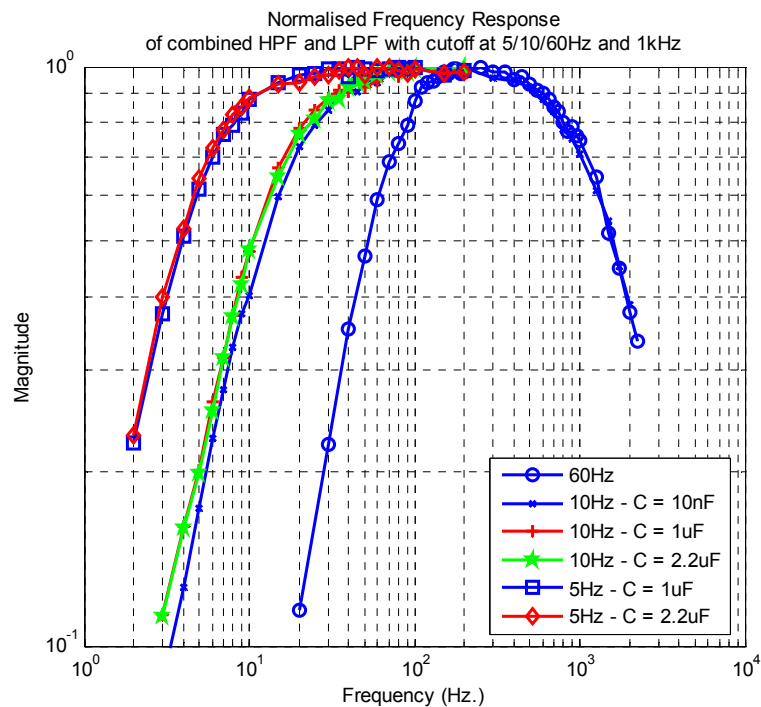
Figure 3.37: Comparison between the Bessel responses at different high-pass filter (HPF) cut-off frequencies - 5, 10 and 60 Hz.

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When the cut-off frequency is 10 Hz, the normalised frequency response at 25 Hz is approximately 0.8. While in the case of 5 Hz cut-off, it is very close to unity. When the heart sound signal was re-observed with a new HPF cut-off at 10 Hz, some attenuation could still be seen at the output although to a lesser degree, less than a factor of 2. It is unclear whether there would be any major benefit or drawback if the cut-off is reduced from 10 Hz to 5Hz.

On the LPF side, an improvement can be made to match the Bessel's response more closely. The theoretical frequency responses of a number of real and obtainable component sets were plotted in Figure 3.38. By comparison, the green line appears to be the best match to the ideal Bessel's response in red.

The measured total current consumption of the signal conditioning block and the microphones was about 2mA.
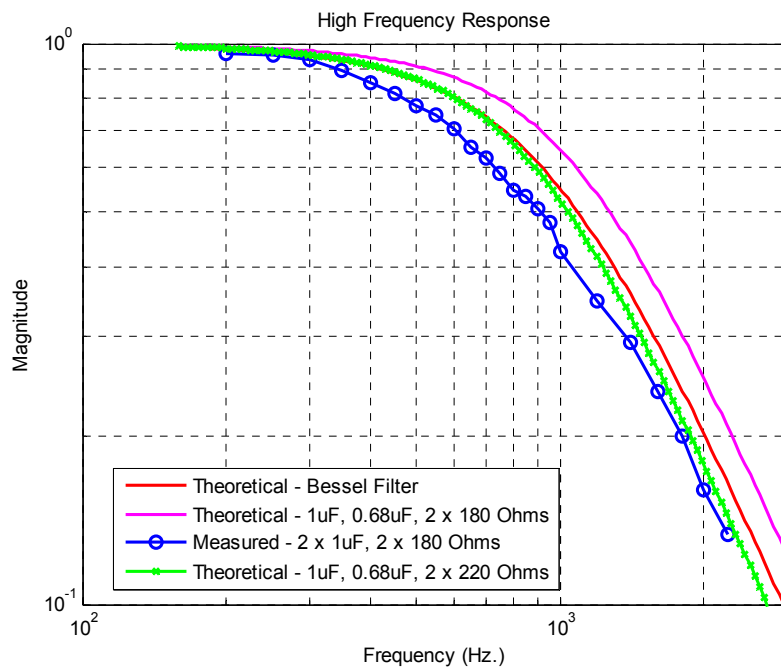
Figure 3.38: Comparisons of theoretical low-pass filter responses with different component values.

3.4.3 Digital Circuitry

The synchronisation circuit was assembled and tested first. The clock signal set at 40 kHz was produced by a signal generator. The circuit was able to generate all the required signals correctly and at the correct time – $\overline{CS}$, R, CONV, D_{IN}, and BUFFERED DATA (using a dummy D_{OUT} signal i.e. Q1), shown in Figure 3.39.

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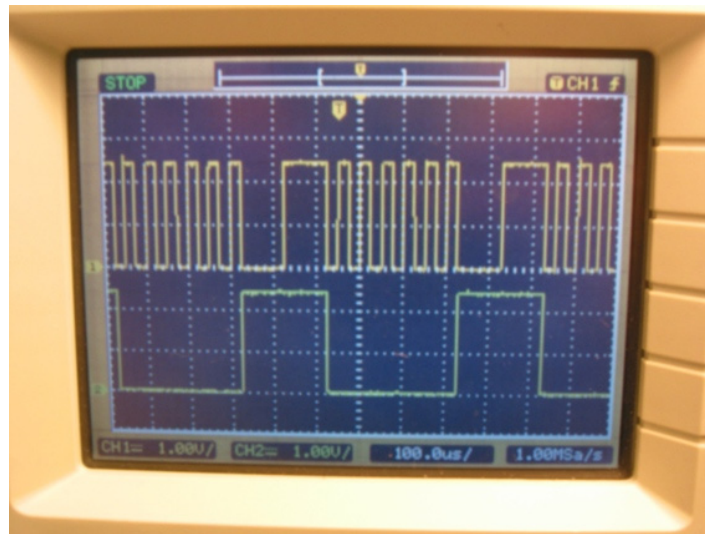
Figure 3.39: Oscilloscope plot of BUFFERED DATA (top) versus CONV (bottom).

Next, the Manchester encoder (Holt Integrated Circuit – HI-15530) was added to see if the dummy BUFFERED DATA will be correctly encoded by the encoder. The 80 kHz clock signal was produced using a signal generator and was fed into the SEND CLK IN input of the Manchester encoder. While the Manchester encoder's ENCODER SHIFT CLK output was used to drive the synchronisation circuit.

A problem was encountered when the push button was pressed to perform a master reset on the Manchester encoder and the synchronisation circuit. This is because the whole circuit stopped working. It was found that the MASTER RESET signal was stuck in logic '1' because there was no ENCODER SHIFT CLK signal to clock the J-K flip-flop and thus toggle the MASTER RESET to a logic '0'. This means that when a logic '1' was applied to the MASTER RESET input of the Manchester encoder, the ENCODER SHIFT CLK is also reset.

The solution was to clock the 7-bit ripple counter and the MASTER RESET's J-K flip-flop with the same clock as the Manchester encoder (through the SEND CLK IN input) at 80 kHz; so that the MASTER RESET's J-K flip-flop's clock does not depend on the operation of the Manchester encoder. By changing the design in this way, a number of changes to the circuit must be made. Firstly, the $\overline{CS}$ J-K flip-flop's clock must be driven by the Q1 output of the counter. Secondly, the logic gates inputs that were driven by Q5 must now be driven by Q6; inputs that were driven by Q4 must now be driven by Q5; likewise, for Q3, Q2, and Q1 (used as a dummy signal for D_{OUT}).

With the above changes, the MASTER RESET was no longer stuck at logic '1' once the push button was activated. Therefore, we could now test if the Manchester encoder can correctly encode the input data (shown in Figure 3.40). The test was conducted 10 times with the same procedure to ensure robustness of the synchronisation circuit:

1. Turn on the power supply (3.3V) and signal generator (80 kHz square wave),

2. Leave the circuit running for a few seconds,

3. Press the push button momentarily to synchronise the circuits,

4. Observe the $\overline{\text{BIPOLAR ZERO OUT}}$ output of the encoder with an oscilloscope and determine whether the encoding is correct or not, and

5. Turn the power supply off and then back on, and repeat the experiment.
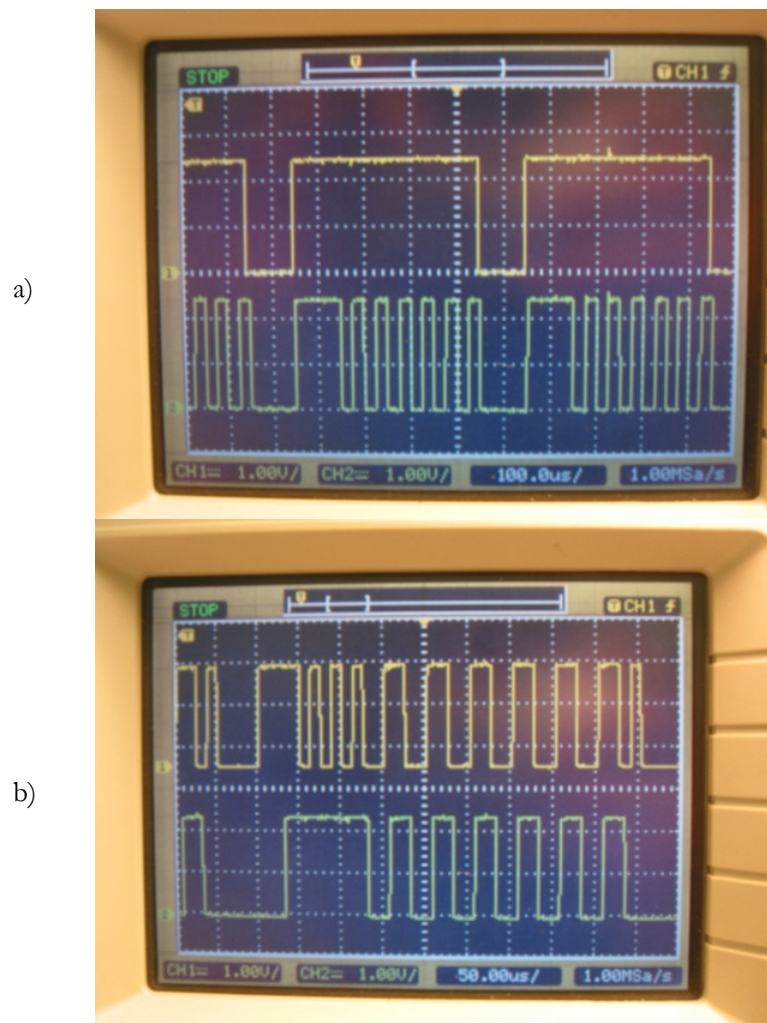
Figure 3.40: Oscilloscope plot of a) correct timing between SEND DATA (top) and BUFFERED DATA (bottom) and b) correct $\overline{\text{BIPOLAR ZERO OUT}}$ (top) for BUFFERED DATA (bottom).

For all 10 times, the combined digital circuit was able to produce the correct encoded data. However since the ADC was not included in the test, this only proves that the synchronisation circuit can work with the Manchester encoder.

Therefore, the next step is to include the ADC (Linear Technology - LTC1285) into the current set-up with the Manchester encoder and the synchronisation circuit, as shown in Figure 3.41. The D_{OUT} signal for this set-up is the actual output of the ADC, which is clocked by the Q1 output of the counter. The +IN analog input of the ADC was connected to a variable power supply, to test if its digital output changes according to the input, while the -IN analog input was connected to ground. The ADC operated correctly with the digital output D_{OUT} increasing or decreasing depending on the changes applied to the analog input. Similarly, the Manchester encoder's output $\overline{\text{BIPOLAR ZERO OUT}}$ did vary according to the changes in the digital output D_{OUT} of the ADC.

The measured total current consumption of the overall digital circuitry was about 12mA.
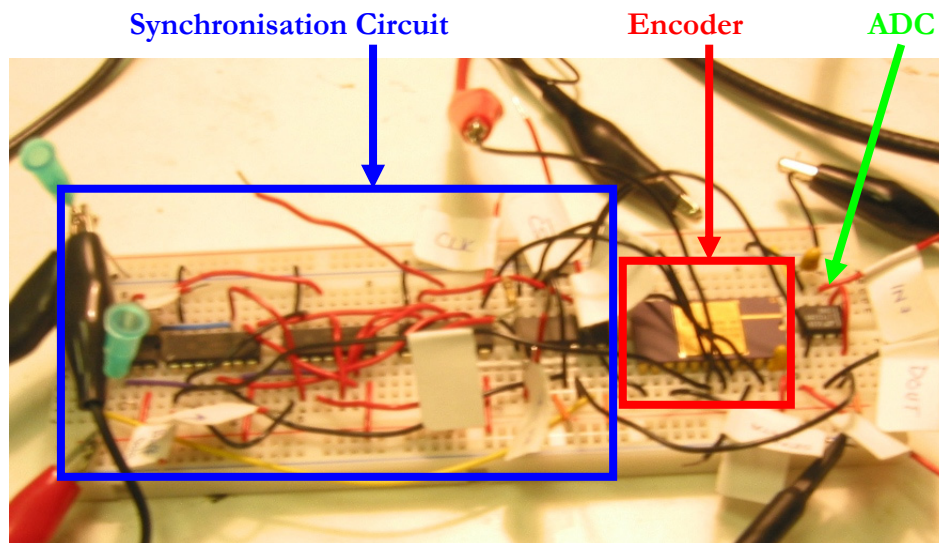
Figure 3.41: The overall set-up of digital circuitry.

3.4.4 Radio Transmission

To ensure that successful data transmission is achieved, it was decided to have an encoder (Holt Integrated Circuits HI-15530) and radio transmitter (Radiometrix UHF TX2) at the source, and the radio receiver (Radiometrix UHF RX2) and a decoder (Holt Integrated Circuits HI-15530) at the reception end. This is necessary to ensure that the received data can be decoded.

The main experiment conducted for the radio blocks is about range testing and RF power. Normally when the radio transmitter was connected to a 3.3V supply, the current drawn by the device is 7mA which translates to approximately +4 dBm. This is a lot of RF power. In this experiment, we will decrease the RF power by reducing the supply voltage.

The SERIAL DATA IN input of the encoder is connected to ground and the SEND CLK IN is connected to an 80 kHz square wave generated by a signal generator (shown in Figure 3.42 a)). At the receiver side shown in Figure 3.42 b), pin 3 of the radio receiver was connected to V_{CC}, while pin 7 is used to feed the UNIPOLAR DATA input of the decoder. The DECODER CLK is driven by another signal generator at 480 kHz. The experiment was conducted from a number of rooms.
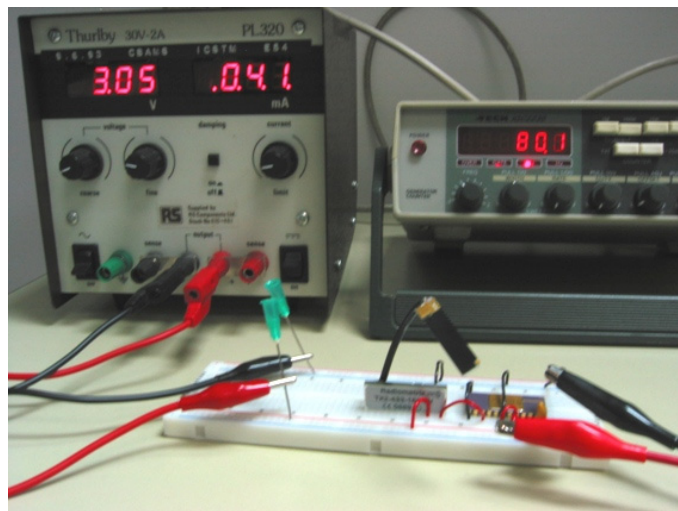
a)
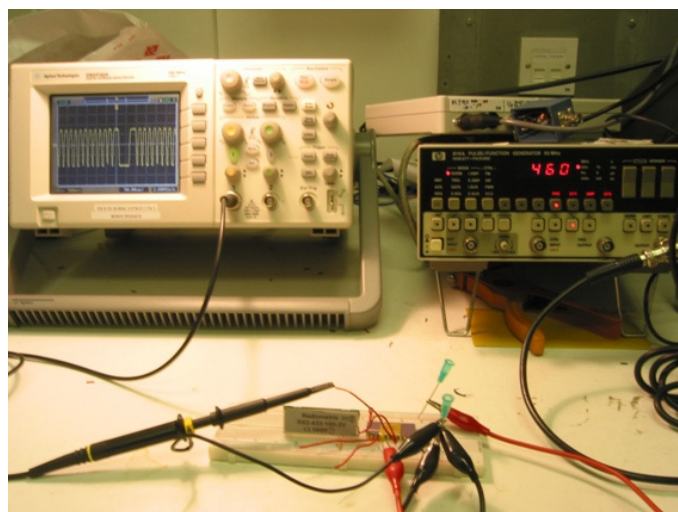
b)

Figure 3.42: The set-up for the range-testing - a) the transmitter and b) the receiver (without antenna).

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Firstly, the transmitter and the receiver were placed in different rooms with a range of approximately 3 metres. Good signals were received without an antenna at the receiver, when the transmitter is powered by a 2.5V supply. The signal could be decoded effectively. Alternatively, the transmitter and the receiver were placed on different floors of the same building, with a range of approximately 10 metres. The received signal could still be decoded without an antenna at the receiver, using a 2.5V supply at the transmitter.

However, the decoder started having difficulties when the transmitter supply voltage was reduced further to 2V.

3.5 Conclusion

In this chapter, the system level design of the proposed wireless heart rate monitoring system using only discrete, off-the-shelf electronics circuitry have been presented. The system level design process began by formulating the proposed system into a number of smaller building blocks. The technology required to perform the operation for each building block was examined and suitable discrete, off-the-shelf components were sought. A detailed design of the electronic circuitry was completed for the components selected. These designs were tested and improved to ensure their operational capabilities and compatibility.

Even though the operational feasibility of the proposed wireless system has been illustrated in this chapter, however the current design still has a relatively high current consumption (approximately 18 mA) and too many integrated circuits (IC), which takes up valuable space. This is especially true for the digital circuitry which requires 8 ICs and consumes 12 mA of current. Thus, the issue of current consumption and number of ICs has to be addressed further before the promise of the proposed long-term wireless heart rate monitoring sensor can be realised.

The final circuit diagram of each building block within the sensor can be found in the Appendix D of this thesis.

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Chapter 4

The Study of De-noising Algorithms

4.1 Introduction

In the last chapter, the initial phase to prove the feasibility of the proposed long-term heart rate monitoring system was demonstrated via the system level design of the sensor. This system level design has shown that it is *technologically* feasible to achieve the operational and size requirements of the proposed system. However, the system level design cannot illustrate the *functional* (performance) aspects of the system – in terms of the signal quality that will be obtained at the receiver end and whether the heart sounds can be effective distinguished from the ambient noise.

The main challenge of using PCG signals for long-term monitoring of heart function and possibly for diagnosing heart diseases lies in the ability to remove the ambient acoustic noise. The intensity and the frequency composition of this ambient acoustic noise can vary greatly from one environment to another posing a complex signal processing task. Thus if the heart sound cannot be distinguished from the ambient noise, then there is no point for us to pursue this system or continue using PCG to monitor heart function.

Therefore in this chapter, we will investigate and discuss the performance of a number of de-noising techniques and their relative performance when applied to a number of different heart sounds. Furthermore, a novel technique will be introduced that has been illustrated to work as well as and in some cases even better than the current leading technique in this field [17].

The first part of this chapter will discuss the system that was employed to record the heart sound signals used in this study. The second part of this chapter will then touches on the different de-noising algorithms. The third part will concentrate on the experimental results obtained when applying the de-noising algorithms to the recorded heart sounds. And finally, the last part of this chapter will discuss the relative performances of the de-noising algorithms obtained from the experimental results.

4.2 The Recording System

The specifications of the recording system were very important for this work. This is because the specifications of the recording system had a substantial effect on the range of noise cancellation techniques or de-noising algorithms that can be applied to the recorded heart sound signals or PCG data, and its overall complexity. The system level design and the specifications of the long-term monitoring sensor platform were described in the previous chapter. Consequently, the specifications of the recording system should be the same as the proposed sensor.

The number of signal channels in our recording system and the position in the data acquisition chain where the heart sound signal should be recorded (after the analogue signal conditioning, after the analog-to-digital conversion, or after the transmission and reception process) need to be set. It was decided to use 2 channels and to make the recording point as *early* as possible in the data acquisition chain to reduce the recording system's complexity, i.e. after the analogue signal conditioning. This is because a system with a lower complexity can be built faster. The justification(s) for choosing two signal channels will be discussed in the next section.

The recording system will consist of the following 5 main components (shown in Figure 4.1) that will provide the ability to simulate the effect of ambient acoustic noise:

1. the sensor,

2. the amplifier and filter unit,

3. the recording unit via a PC,

4. the heart sound generator, and

5. the ambient noise generator.
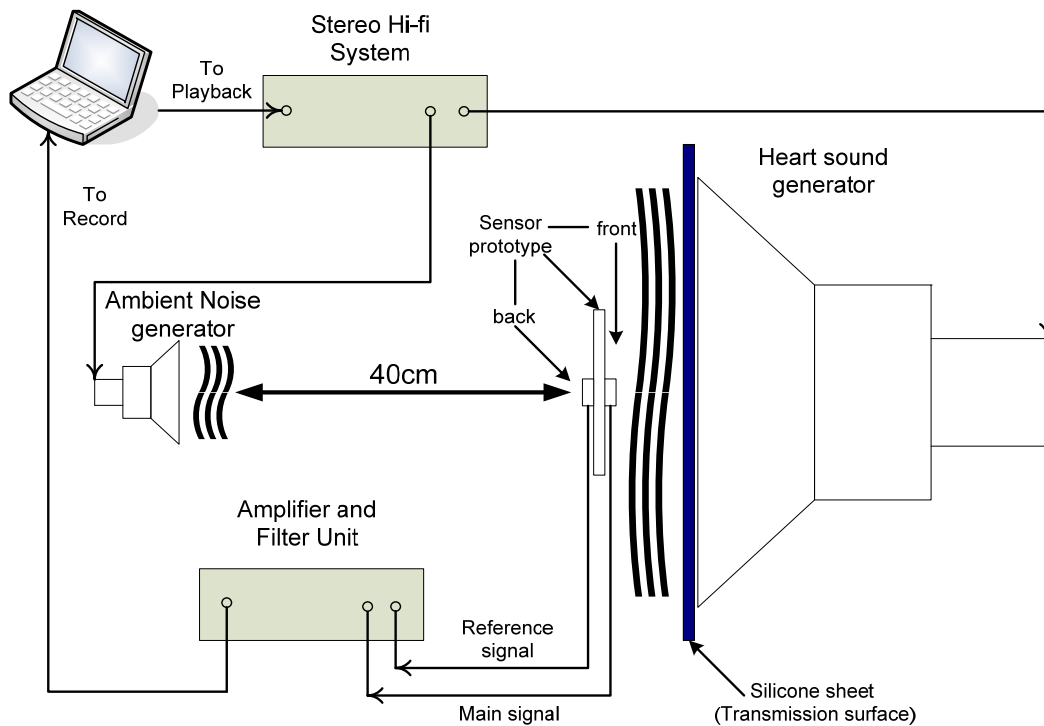
Figure 4.1: The overall recording system set-up.

4.2.1 Multi-Channel System & Directionality

Most publications on the development of PCG monitoring platform have concentrated on using a single transducer or a single-channel system [8-10,16]. However, a single-channel system leaves little room for flexibility and restricts the number of de-noising algorithms that can be applied to the recorded PCG data. Recently, a 2-channel PCG system was introduced by Varady along with a 2-channel de-noising algorithm [19,20]. Therefore, it would be advantageous to investigate the use of dual- or multi-channel recording systems in this study to permit the use of dual- or multi-channel signal processing techniques to de-noise PCG data.

The additional benefit of employing a dual- or multi-channel sensor system is the ability to differentiate the direction of the incoming signals. Directional microphones and microphone array noise reduction systems have been extensively studied in speech processing and the development of hearing aids [6,22]. The use of such systems is very important in hearing aid applications because speech is not easily distinguished, when there are multiple speakers. Thus, the directionality of the sound becomes very important. A specific direction can be selected, in a multi-channel system, using a technique called 'Beamforming' [18]. For PCG signals, directionality is also important but to a much lesser degree. This is because the heart sounds are very faint compared to the ambient noise and can only be picked up through a

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stethoscope cone or when the microphone is in direct contact with the skin. Therefore for PCG systems, the use of a 2-channel system, with a reference microphone to monitor the ambient noise in the environment, should suffice.

a)

b)
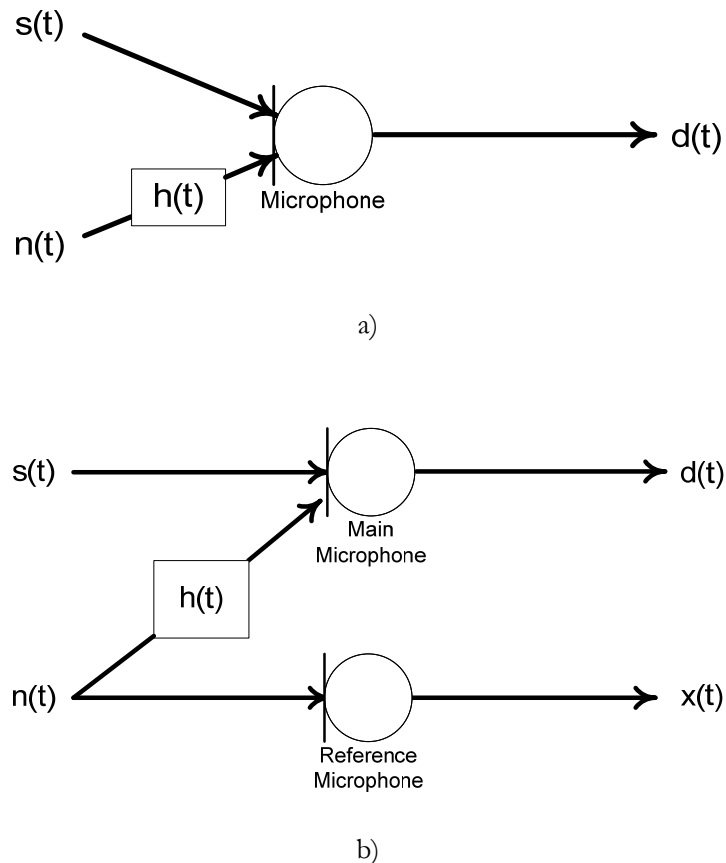
Figure 4.2: The signal flow chart of a) a single and b) a two-channel microphone system.

Furthermore, it has been shown that directionality can be more simply selected and noise rejection performance enhanced using different combinations of *omni-* and *uni-*directional microphones [4,5]. Thus in this chapter, the relative noise rejection performance comparison for a dual- or 2-channel microphone system with different combinations of *omni-* and *uni-*directional microphones will also be investigated and presented.

In any 2-channel system, there are two signals that can be utilised to recover the desired or wanted signal s(t) (shown in Figure 4.2). However when this signal is picked up by the main microphone d(t), it is corrupted by a version of the ambient noise n(t). The reference microphone x(t), on the other hand, is normally configured to receive only the ambient noise n(t). For a single-channel system, only the main microphone signal d(t) is available to us.

Assuming the microphones are ideal: (* denotes convolution)

$$d(t) = s(t) + n(t) * h(t) \qquad (4.1)$$

and
$$x(t) = n(t) \qquad (4.2)$$

where h(t) is the transmission path between the main and the reference microphone.

4.2.2 Sensor Prototypes

To experiment with different configurations of *omni-* and *uni-*directional microphones, a number of sensor prototypes for this recording system were made. They were built on printed circuit boards (PCBs), each measuring 45 x 40 x 2 mm (length x width x thickness), with one microphone soldered onto the front (main microphone) and back (reference microphone) sides. In this study, two types of microphone were used; both manufactured by Knowles Acoustics (see Table 4.1 for their specifications):

    i)   a surface-mount silicon, *omni-*directional microphone (SPM0103ND3), and

    ii)   an electret condenser, *uni-*directional (cardioid) microphone (MB6022USC-3).

A total of three sensor prototypes were produced C1, C2 and C4. However, a fourth configuration C3 can be achieved by flipping C2 over (see Table 4.2). A picture of a sensor prototype C1 is shown in Figure 4.3. When recording the front microphone was in contact with or close to the heart sound generator, while the back microphone was exposed directly to the ambient noise, as illustrated in Figure 4.1.

Table 4.1: The specification of the Knowles Acoustics microphones used

	SPM0103ND3	MB6022USC-3
Directionality	**Omni**	**Uni**
Sensitivity (0 dB = 1V/Pa)	-22dB @ 1kHz	-47dB @ 1kHz
Output Impedance	100 Ω @ 1kHz	2.2 kΩ @ 1kHz
SNR	59 dB (nom)	50 dB (min)
Current Consumption	0.1-0.35 mA	0.3-0.5 mA
Supply Voltage	1.5-5.5 V	1.5-3 V

Table 4.2: Location of the directional microphones for different sensor configurations

	Sensor Configuration			
	C 1	**C 2**	**C 3**	**C 4**
Front	Omni	Omni	Uni	Uni
Back	Omni	Uni	Omni	Uni
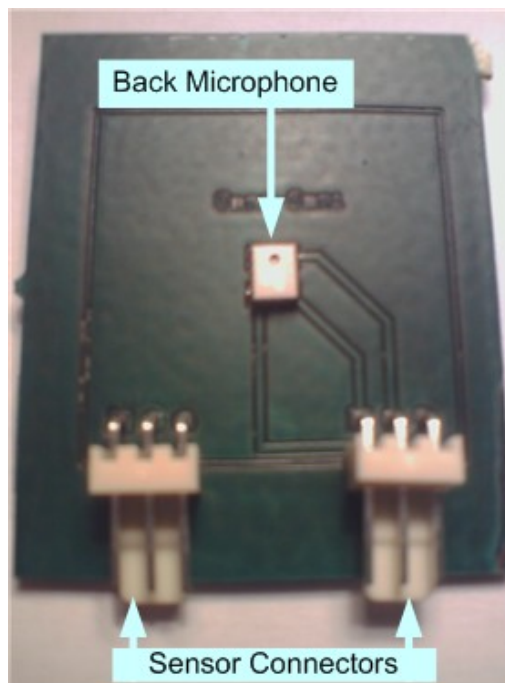
Figure 4.3: A picture of the sensor prototype with configuration C1.

4.2.3 Amplifier and Filter Unit

The amplifier and filter unit is a 2-channel device connected to a 3V power supply. Its operation is divided into two main parts: the amplification and the filtering stages (shown in Figure 4.4). The amplification stage is designed to provide a 26 dB-fixed gain to both the front (main) and back (reference) microphone channels. This is achieved using instrumentation amplifiers (Burr-Brown INA-118).

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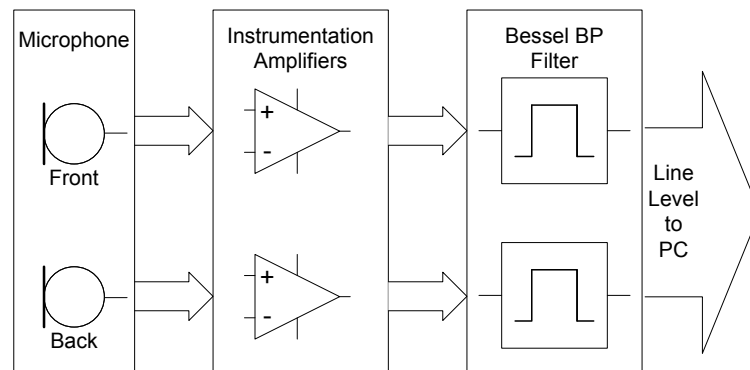
Figure 4.4: A block diagram of the amplifier and filter unit.

After each signal has been amplified, the signal is then fed into a 4th order, active, Bessel band-pass (BP) filter with the lower cut-off frequency, f_{min}, at 25 Hz and the higher cut-off frequency, f_{max}, at 1 kHz. This 2-channel signal is then passed on to a PC as a line level stereo signal. Figure 4.5 presents a picture of the constructed amplifier and filter unit. Figure 4.6 illustrates the full circuit diagram of this unit.
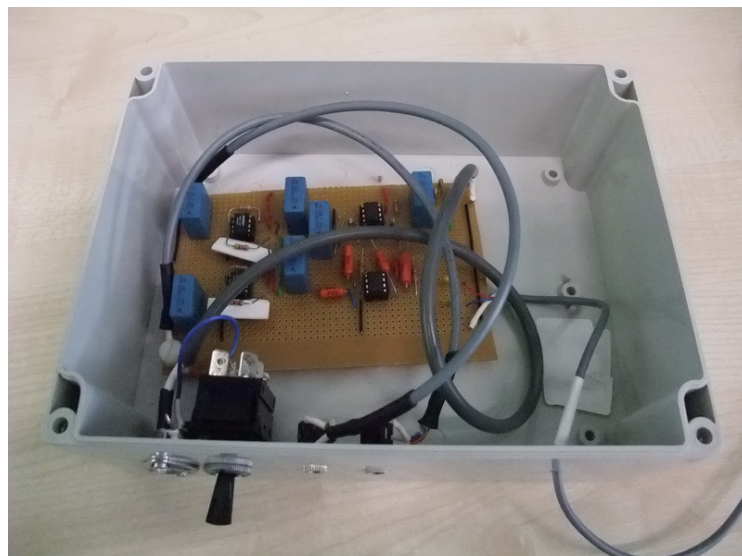
Figure 4.5: A picture of the constructed amplifier and filter unit.
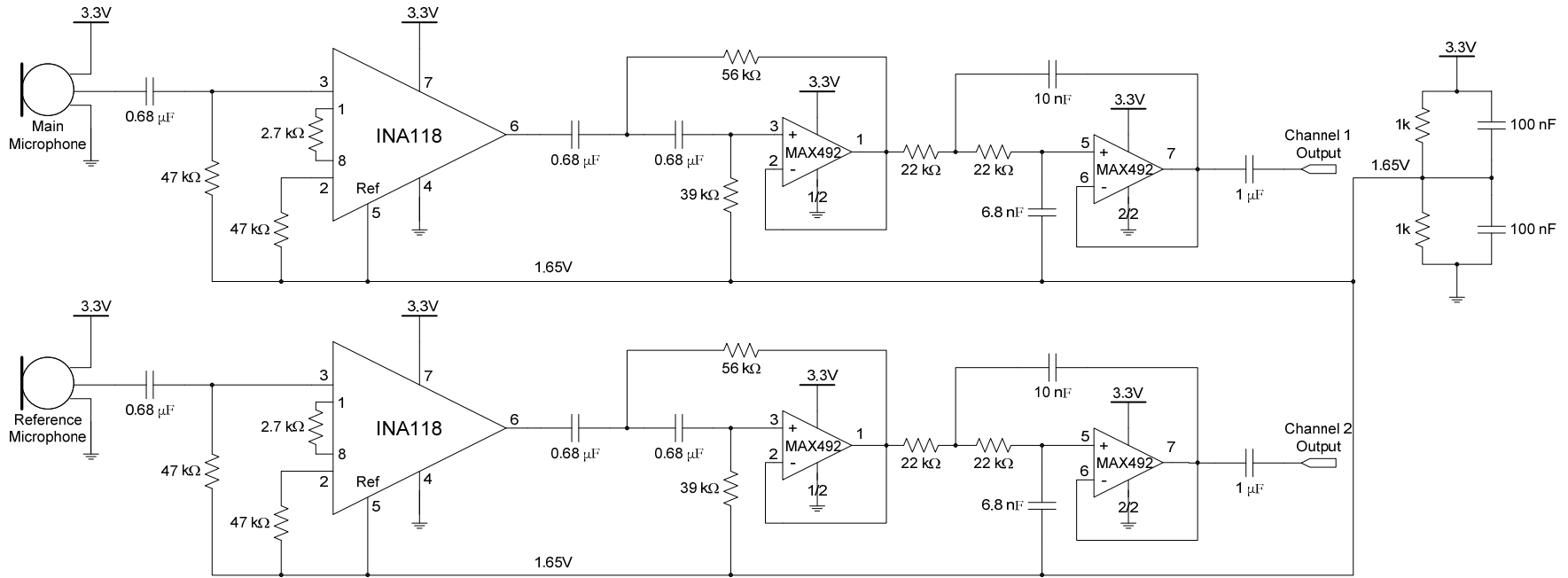
Figure 4.6: The full circuit diagram of the amplifier and filter unit.

4.2.4 Recording Unit (PC)

The 2-channel PCG line level signal was digitised and recorded using open-source software 'Audacity' (http://audacity.sourceforge.net) into WAV files on a PC (shown in Figure 4.7). The signals were recorded at 16-bit resolution and at a sampling frequency, f_s, of 44100 Hz.
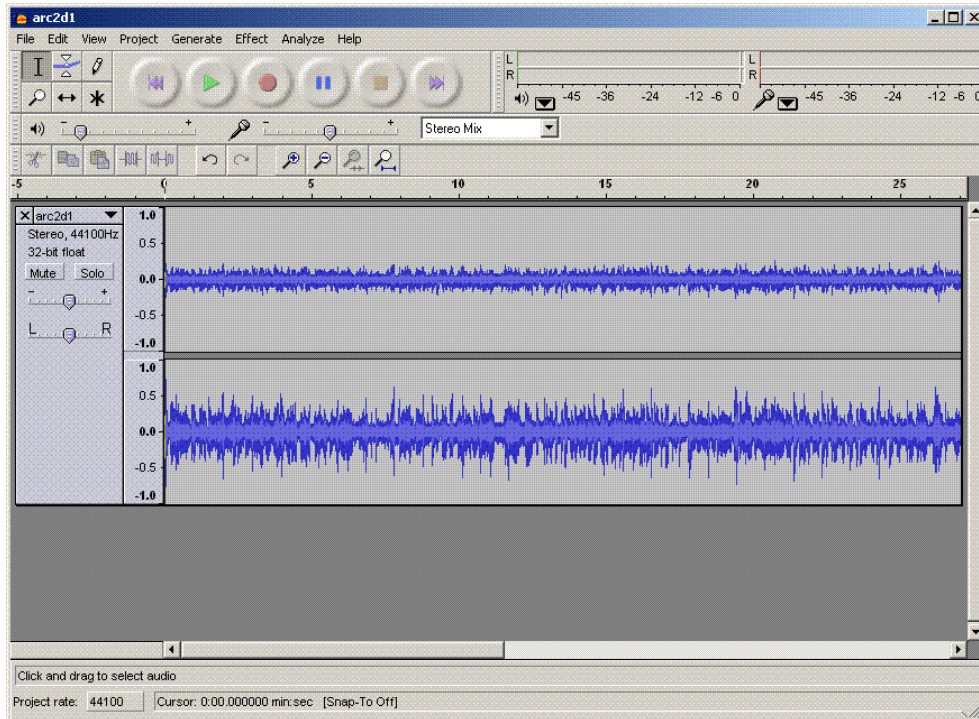
Figure 4.7: Open-source software 'Audacity' user interface.

The recordings of the PCG data were decimated 22 times before being inputted into the noise cancellation algorithms. In other words, the signals used in this experiment are effectively sampled at approximately 2 kHz. This is to minimise computational time when running the de-noising algorithms, while obeying the Nyquist condition $- f_s \geq 2 f_{max}$ [15].

4.2.5 Heart Sound Generator [3]

The heart sound generator was a 12-inch bass speaker connected to a Sony stereo hi-fi system, Model No. DHC-MD313, playing back audio clips of heart sounds. The front of the speaker was covered by a thin silicone sheet to mimic skin and to provide a transmission surface of the heart sound to the microphone.

Since the long-term monitoring platform that we are developing is meant to allow the analysis of the wearer's heart function and to potentially diagnose heart disease, it will have to deal with a wide range of heart sounds, especially when it is applied to people with a heart
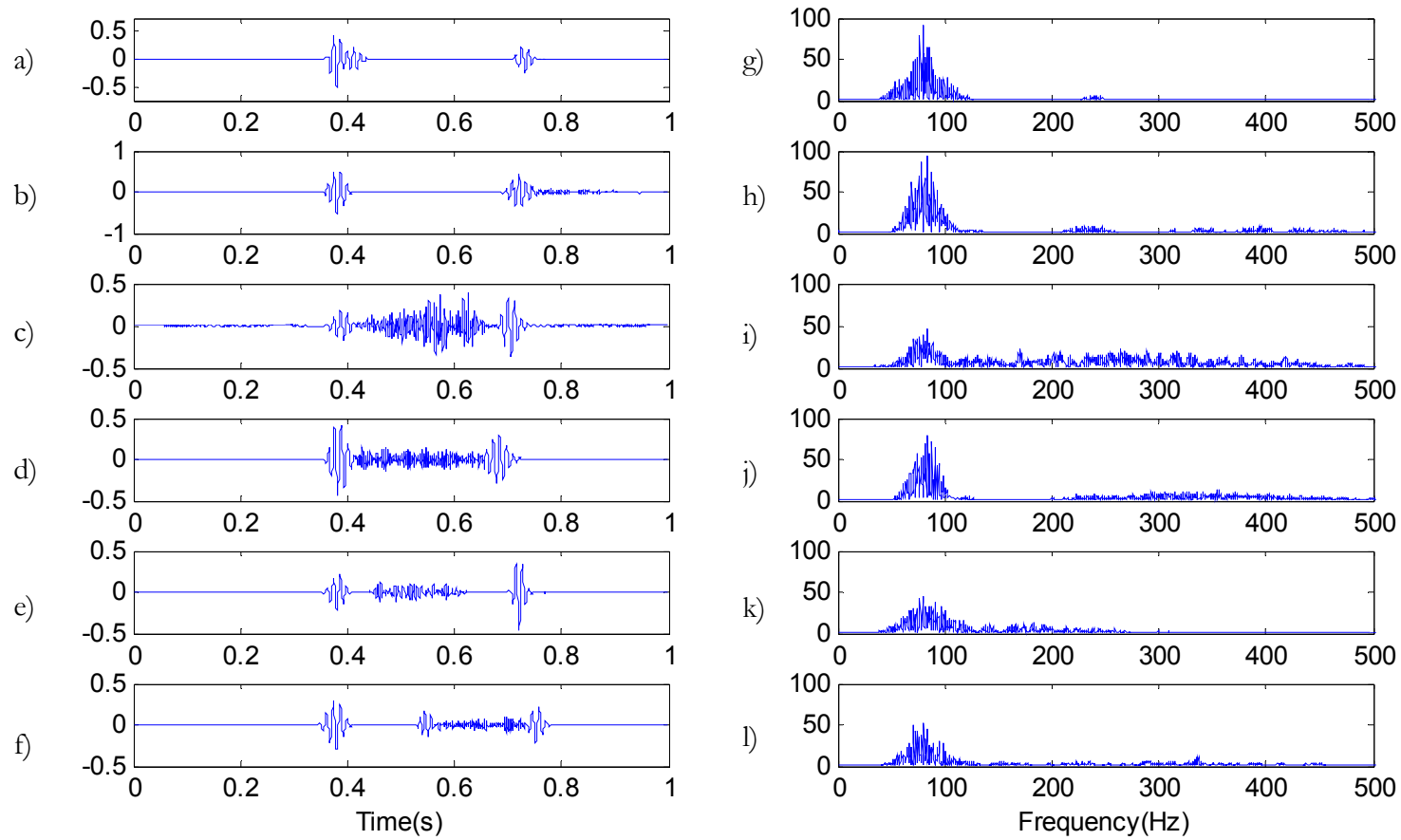
Figure 4.8: The time-domain waveform of a) a Normal heart sound (NORMAL), b) Aortic Regurgitation (AR), c) Aortic Stenosis (AS), d) Mitral Regurgitation (MR), e) Innocent Systolic Murmur (ISM), and f) Mitral Valve Prolapse (MVP) - and their corresponding frequency spectrum in g) − l), in the same order. (www.cardiosource.com)

condition. Thus, the de-noising algorithm should also be able to accommodate for these different heart sounds. Therefore, the relative performances of the de-noising techniques should be compared when they are applied to a range of heart sounds to determine their strengths and weaknesses, since each heart sound has a unique characteristic. A number of different heart sounds were obtained from www.cardiosource.com and used throughout this study. These include (see Figure 4.8):

- Normal heart sound (NORMAL),

- Aortic Regurgitation (AR),

- Aortic Stenosis (AS),

- Mitral Regurgitation (MR),

- Innocent Systolic Murmur (ISM), and

- Mitral Valve Prolapse (MVP).

4.2.5.1 Normal Heart Sound (NORMAL)

Normal heart sound contains two main audible components – the first (S1) and the second (S2) heart sounds. The appearance of the first heart sound (S1) coincides with the carotid pulse and represents the closure of both the mitral and the tricuspid valves. However, these events do not necessarily occur at the same time. The second heart sound (S2) represents the closure of the aortic and then the pulmonary valves. There are also the third and the fourth heart sounds, although they may not be audible.

4.2.5.2 Aortic Regurgitation (AR) and Aortic Stenosis (AS)

These heart sounds are associated with the abnormality of the aortic valve. This abnormality is present in 1 to 2 per cent of the population, where it is more common in men than women. Normally, the aortic valve is made of three equal sized cusps. Thus, abnormalities occur when these cusps are not of equal size or there are only 2 (bicuspid) or even in some cases 1 cusp. The abnormality of the aortic valve is the most common congenital heart defect.

4.2.5.3 Mitral Regurgitation (MR) and Mitral Valve Prolapse (MVP)

Mitral Regurgitation can be present in both adulthood and childhood. Although, it is more common in adulthood and is normally indicative of an ischaemic heart with reduced left

ventricular function or a valve disease. If this condition is left unchecked, the left ventricle may be volume loaded to an extent that myocardial infarction occurs.

Mitral Valve Prolapse (MVP) is caused by a disorder of the papillary muscles of the mitral valve that results in a lack of support to the leaflets of the valve. This disorder is more common in women and is present in 2 to 3 per cent of the population. People who exhibit mitral valve prolapse will also exhibit mitral regurgitation

4.2.5.4 Innocent Systolic Murmur (ISM)

Murmurs can some time appear even when the cardiac anatomy is normal. Thus, they are termed 'innocent' murmurs. This heart sound is also known as Still's murmur. This innocent murmur is very common in childhood and often heard from age 3 to adolescence. The exact cause of this murmur is still unknown.

4.2.6 Ambient Noise Generator

The noise generator was a Sony speaker, Model No. SS-MD313, connected to a stereo hi-fi system playing back audio clips of a recorded radio program, containing a mixture of speech and music. This speaker is positioned to be directly behind and facing the back microphone – 40 cm away from the heart sound generator.

4.2.7 Conclusion

A 2-channel recording system that was used for recording PCG data in a simulated noisy environment has been introduced. The benefit of constructing this recording system allows us greater flexibility to experiment with a number of different system set-ups in a controlled environment. Firstly, the system allows the performance of a number of different sensor prototype configurations to be compared. Secondly, the performance of the de-noising algorithms when applied to different heart sounds can also be studied to see the strong and weak points of each technique. Lastly, we may also compare the performance of the noise cancellation techniques and the different sensor prototypes with distance from the skin or, in this case, the silicone transmission surface.

In total, 48 recordings of the PCG data were taken using this 2-channel recording system, in an anechoic chamber. Each of these recordings is approximately one minute in length. These recordings correspond to 6 different heart sounds, 4 sensor prototype configurations and 2 recording distances. The first recording distance is when the front (main) microphone is in

contact with the transmission surface and the second is when the front microphone is one centimetre away from the transmission surface.

4.3 Standard De-noising Algorithms

There are many de-noising algorithms or noise cancellation techniques available for both single- and multi-channel systems. These algorithms vary greatly in their processing method and complexity. However, most noise cancellation algorithms operate in two manners. The first manner is where a special characteristic(s) of the desired signal, e.g. wave shape - Wavelet Thresholding, statistical properties - Spectral Subtraction, is sought and used to distinguish it from the ambient noise. This is the standard mode of operation for single-channel de-noising techniques because it does not have the benefit of additional signals to help with the de-noising process. The main advantage of this type of technique is that it allows for a less complex sensor to be used. However, the weakness of this type of noise cancellation techniques is when the ambient noise has similar characteristics to the wanted signal i.e. in hearing aid applications, or when the ambient noise environment changes quickly.

The second mode of operation of de-noising algorithms is relevant to systems with multiple channels. This is where the algorithm takes advantage of the additional signal(s) to more effectively estimate the ambient noise. This type of techniques is more flexible and can be applied to a wider range of situations because the noise cancellation is able to adapt to the changing noise environment e.g. Adaptive Least Mean Squares (LMS), and Adaptive Recursive Least Squares (RLS). Still the main drawback of multiple channel de-noising algorithms is the increased complexity of the sensor system, since there are more signals to acquire and process.

In this section, the de-noising algorithms that have been used in the study will be discussed. These include:

1. Simple Subtraction (SUB),

2. Adaptive Least Mean Squares (LMS) filter,

3. Adaptive Recursive Least Squares (RLS) filter,

4. Spectral Subtraction, and

5. Wavelet Thresholding (WLET).

The first three techniques are all 2-channel noise cancellation techniques. However, Spectral Subtraction and Wavelet Thresholding (WLET) are both single-channel algorithms.

For a 2-channel system (shown in Figure 4.2 b)), the required complexity of the de-noising algorithm depends largely on the relationship or transmission path h(t) between the main and the reference microphones. Since this relationship is normally unknown, it has to be calculated through experimentation or estimated by other means to derive the expected noise signal in the corrupted main signal. Unfortunately, this transmission path is normally highly non-linear and non-stationary. And to make matters worst, some of the main signal is often picked up by the reference microphone. Thus, simple addition or subtraction will often result in the corruption of the wanted signal.

4.3.1 Simple Subtraction (SUB)

In the last chapter, we have proposed the possibility of using two transducers in a single-channel system by performing a simple subtraction operation between their outputs through an instrumentation amplifier at the initial amplification stage (see Figure 3.30). Therefore, it would be interesting to study the practicality and the relative performance of this set-up with other more widely used techniques, considering that the simple subtraction (SUB) operation is very straightforward and requires minimal processing time.

For the simple subtraction (SUB) operation, the reference microphone x(t) will be directly subtracted from the main microphone signal d(t) which gives out an output signal o(t), as shown in Figure 4.9:

$$o(t) = d(t) - x(t) \qquad (4.3)$$

By using equation 4.1 and 4.2: (* denotes convolution)

$$o(t) = s(t) + n(t) * h(t) - n(t) \qquad (4.4)$$

Thus for the output signal o(t) to equal the desired or wanted signal s(t):

$$n(t) = n(t) * h(t) \qquad (4.5)$$

Therefore, $\qquad\qquad\qquad\qquad h(t) = 1 \qquad\qquad\qquad\qquad (4.6)$

Thus by using simple subtraction, we are assuming that the transmission path h(t) is *fixed* and equals to 1. In other words, we are assuming the ambient noise picked up by the main and the reference microphones are the same.
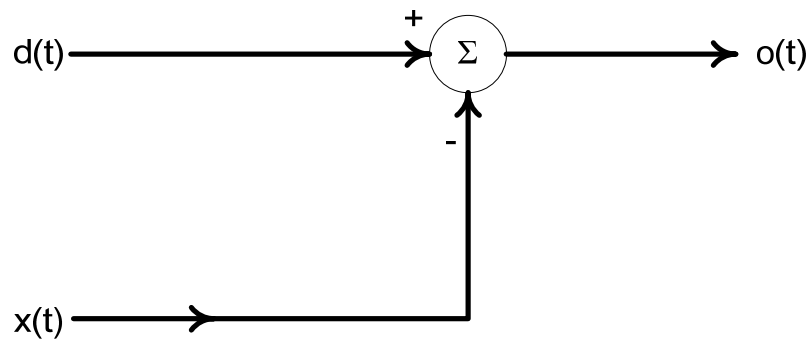
Figure 4.9: The signal flow graph of the simple subtraction de-noising technique.

4.3.2 Adaptive filter [13,15]
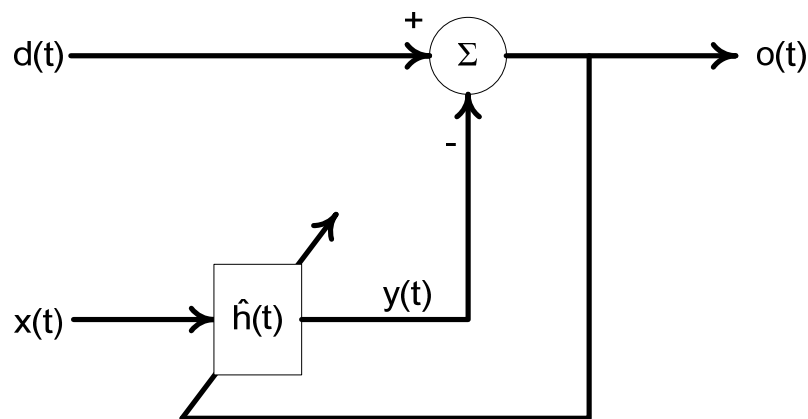
Figure 4.10: The adaptive filter concept.

The adaptive filter concept was introduced to deal with situations where a simple filter with a fixed transfer function or characteristics is not effective, due to a changing noise environment [21]. Therefore, the use of a fixed estimate of the noise's transmission path h(t), as in the simple subtraction case, is not sufficient and a variable one must be used. In an adaptive filter, the variable filter impulse response $\hat{h}(t)$ is used to estimate the transmission path h(t). The filter's coefficients and therefore its transfer function are updated using its output or error signal o(t) via an optimisation algorithm (see Figure 4.10), such as the steepest descent or least-squares criterion. The error signal o(t) is the difference between the main microphone signal d(t) and the noise estimate in the main microphone signal y(t), derived from the reference microphone signal x(t) and the estimate transmission path $\hat{h}(t)$. Thus, the adaptive filter can adjust itself to changing noise environments, without prior knowledge of the main signal and the noise:

$$o(t) = d(t) - y(t) = d(t) - x(t) * \hat{h}(t) \tag{4.7}$$

By using equation 4.1 and 4.2: (* denotes convolution)

$$o(t) = s(t) + n(t) * h(t) - n(t) * \hat{h}(t) \tag{4.8}$$

Thus for the output signal o(t) to equal the desired or wanted signal s(t):

$$n(t) * \hat{h}(t) = n(t) * h(t) \tag{4.9}$$

Therefore, $\qquad \qquad \qquad \hat{h}(t) = h(t) \tag{4.10}$

Thus, if the estimate impulse response $\hat{h}(t)$ and the transmission path h(t) are equal then the output or error signal o(t) will be equal to the wanted signal s(t). However for this to be true, it is required that the reference input x(t) contains none of the wanted signal component. Though, this may not always be possible especially when the overall size of the sensor, or the distance between the main and the reference microphones, is heavily constrained, which is the case for our sensor prototypes where the main and the reference microphones are placed back to back and separated only by a PCB.

In this study, two different adaptive algorithms were used and compared, namely – Least Mean Squares (LMS) and Recursive Least Squares (RLS). The difference between these two algorithms lies in the way the filter coefficients are adapted.

4.3.2.1 Least Mean Square (LMS) algorithm

The LMS filter employs the steepest descent method to minimise the mean square error (MSE) between the desired signal s(t) and the output signal or error signal of the filter o(t). If the discrete-time filter's output y[t] with a finite impulse response h[t] and (reference microphone) input x[t] is given by:

$$y[t] = \sum_{l=0}^{m-1} h[l]x[t-l] = \mathbf{x}[t]^T \mathbf{h} \tag{4.11}$$

where

$\mathbf{x}[t] = [x[t], x[t-1], \dots, x[t-m+1]]^T$, $\mathbf{h} = [h[0], h[1], \dots, h[m-1]]^T$

Then provided the desired signal is d(t), the cost function $\mathbf{J(h)}$ to minimise it is given by:

$$J(h) = E[(d[t] - y[t])^2] = E[(d[t] - \mathbf{x}[t]^T \mathbf{h})^2]$$
$$= \sigma_d^2 - \mathbf{p}^T \mathbf{h} - \mathbf{h}^T \mathbf{p} + \mathbf{h}^T R \mathbf{h}$$

(4.12)

where

$$R = E[\mathbf{x}[t]\mathbf{x}^T[t]] \qquad \mathbf{p} = E[\mathbf{x}[t]\mathbf{d}[t]]$$

By using the steepest-descent rule, the filter coefficients **h**[t] needs to be iteratively updated in the following manner:

$$\mathbf{h}[t+1] = \mathbf{h}[t] + \mu(\mathbf{p} - R\mathbf{h}[t])$$

(4.13)

This can be simplified further to give:

$$\mathbf{h}[t+1] = \mathbf{h}[t] + \mu\mathbf{x}[t]o[t]$$

(4.14)

where μ is the step size.

Careful consideration has to be given when choosing the value of the step size. This is because the rate of convergence depends on it. However, if the step size is too large the adaptation may not converge at all.

4.3.2.2 Recursive Least Squares (RLS) algorithm

To increase the convergence rate of an adaptive algorithm, the recursive least squares (RLS) algorithm was introduced. This algorithm is more computationally complex with more variables based on the least-squares criterion. Using the same discrete-time filter's output y[t] as given in equation 4.11, it was found that the coefficients minimising the least-squares error satisfy the normal equation:

$$R\mathbf{h} = A^H \mathbf{d}$$

(4.15)

where A is a data matrix, and

$$R = A^H A = \sum_{i=1}^{N} \mathbf{q}[i]\mathbf{q}^H[i]$$

with

$$\mathbf{q}[i] = \begin{bmatrix} \bar{x}[i] \\ \bar{x}[i-1] \\ ... \\ \bar{x}[i-m+1] \end{bmatrix}$$

The least-squares adaptive filter is achieved by updating the filter coefficients $\mathbf{h}[t]$ in the following manner:

$$\mathbf{h}[t] = R^{-1}[t]\mathbf{p}[t] \tag{4.16}$$

where

$$R[t] = \sum_{i=1}^{t} \mathbf{q}[i]\mathbf{q}^{H}[i] \qquad \mathbf{p}[t] = \mathbf{p}[t-1] + \mathbf{q}[t]d[t]$$

By using the Sherman-Morrison formula, the *recursive* least-squares filter coefficients can be obtained in equation 4.17. This is much less computationally demanding to calculate than the least-squares filter coefficients given in equation 4.16.

$$\mathbf{h}[t] = \mathbf{h}[t-1] + \mathbf{k}[t]\varepsilon[t] \tag{4.17}$$

where

$$\mathbf{k}[t] = \frac{P[t]\mathbf{q}[t]}{1 + \mathbf{q}^{H}[t]P[t-1]\mathbf{q}[t]} \tag{4.18}$$

$$P[t] = P[t-1] - \mathbf{k}[t]\mathbf{q}^{H}[t]P[t-1] \tag{4.19}$$

and
$$\varepsilon[t] = d[t] - \mathbf{q}^{H}[t]\mathbf{h}[t-1] \tag{4.20}$$

To start the adaptive RLS algorithm, the matrix P[t] and the filter coefficients $\mathbf{h}$[t] at t = 0 is initialised to:

$$P[0] = \delta^{-1}I \qquad \mathbf{h}[0] = 0$$

where δ is a small positive number.

In the adaptation of the filter coefficients of the adaptive recursive least squares (RLS) filter, the following sequence of computations is conducted:

1. $\mathbf{k}[t]$ using equation 4.18,

2. $\varepsilon[t]$ using equation 4.20,

3. $\mathbf{h}[t]$ using equation 4.17, and

4. $P[t]$ using equation 4.19.

4.3.2.3 Conclusion

Both the LMS and RLS adaptive filters can adjust their filter coefficients h[t] to deal with a changing noise environment. The LMS algorithm is relatively simple and requires less computation to achieve an adaptation, however the rate of convergence may be too slow and take many hundred of iterations. Therefore, the RLS algorithm was introduced to reduce the number of iterations required to achieve convergence, which can reduce the convergence time, in some cases, by 90%. However, the penalty for having such a fast rate of convergence is the increased computational complexity. The level of complexity is dependent on the number of filter coefficients M that we use for both the LMS and RLS adaptive filter.

The LMS and RLS algorithm that was used in this study was written by Moon [13]. This consists of four MATLAB functions – namely:

      i)   lms.m,

      ii)   lmsinit.m,

      iii) rls.m, and

      iv) rlsinit.m.

The MATLAB code for these function are presented in Appendix E. The number of filter coefficients used were 256 and 128, for the adaptive LMS and RLS filters respectively. The step size μ of the LMS algorithm was set at 0.01, while the δ value to initialise the matrix P[t] of the RLS algorithm was set at 1.

4.3.3 Spectral Subtraction

Another possible technique for removing noise in signals is Spectral Subtraction. Since its introduction in the 1970s, spectral subtraction has been successfully but strictly applied to speech processing in single-channel systems [1,2].

Spectral Subtraction is particularly useful in this field, even though speech is a non-stationary signal, because speech has some unique statistical properties. On average, speech is only present for 30% of the time. Furthermore, speech can be assumed to be stationary, if the time window is sufficiently short. Therefore, the noise spectrum can be estimated and assumed constant during that time window (see Figure 4.11).
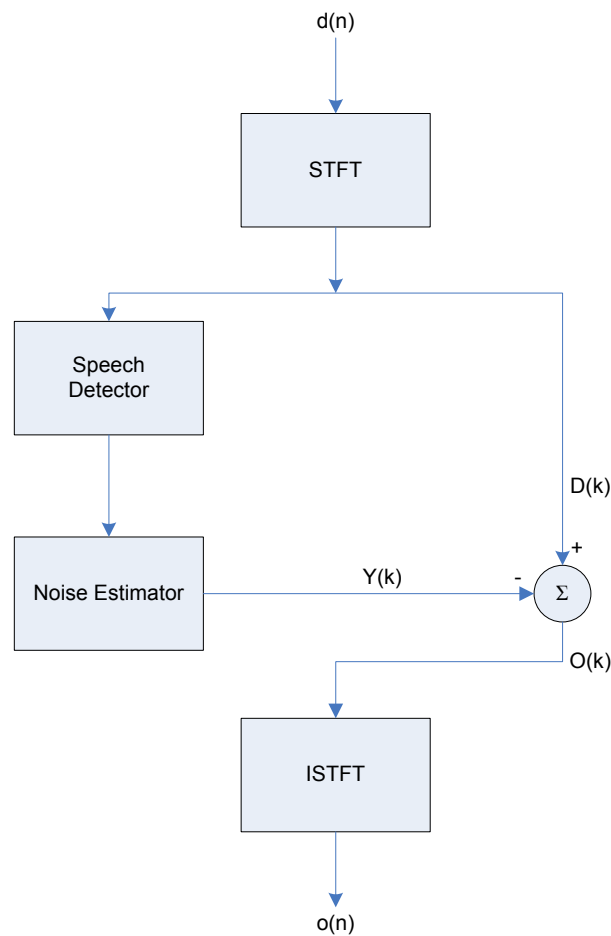
Figure 4.11: The concept of spectral subtraction technique.

4.3.3.1 Short-time Fourier Transform (STFT)

However, the Spectral Subtraction de-noising technique differs from most other techniques because all the operations – noise estimation and subtraction, are performed in the frequency domain. So a technique called Short-time Fourier Transform (STFT) is normally performed on the signal to convert the time-domain signal to and from the frequency-domain spectrum.

The STFT is a more specialised form of the Discrete Fourier Transform (DFT), where a window function w(n) of finite length is introduced to select the location in the time-domain signal, as well as regulating the amplitude of the signal within the window length. Furthermore, the shape of the window can be selected to reduce spectral leakage due to finite resolution of the Discrete Fourier Transform (DFT) [11,15]. The Discrete Fourier Transform (DFT) for a discrete-time signal x(n) of frame size N is given by:

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{\frac{-j2\pi nk}{N}}$$
(4.21)

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While, the inverse Discrete Fourier Transform (IDFT) is given by:

$$x(n) = \frac{1}{N}\sum_{k=0}^{N-1} X(k)e^{\frac{+j2\pi nk}{N}}$$ (4.22)

For a rectangular window ($w(n) = 1$), the Short-time Fourier Transform (STFT) and its inverse (ISTFT) is the same as the standard Discrete Fourier Transform (DFT) and its inverse (IDFT).

4.3.3.2 Speech Detector and Noise Estimator

Furthermore to estimate the noise in the Spectral Subtraction process, the time window or frame size of the STFT needs to be sufficiently small. Therefore, the frame size is normally kept small – tens of milli-seconds in length. The noise estimation is performed during the period where speech is absent from the signal. This detection is performed using a speech detector. A thresholding operation is normally used for this function. If the magnitude of a frequency bin, k, is below the threshold value, then it is assumed that there is no speech signal at that frequency bin.

The magnitude of the noise spectrum is normally estimated by finding the average input signal magnitude spectrum when no speech is present and the phase of the noise spectrum is assumed to be identical to the phase of the input signal spectrum. The use of multiple frames of data is required to find the estimate of the noise. Additionally, these frames are normally arranged to overlap each other by half, three quarters or more to allow the assumption of the stationarity of speech. This technique is called '**Magnitude Averaging**'. However, the noise estimator has to be reset after a period of time to accommodate for a changing speech signal.

Another technique that can be used to improve the performance of the spectral subtraction algorithm is the '**Half-wave Rectification**'. This occurs when the subtraction between the magnitude of the input and the magnitude of the estimated noise results in a negative value, where the output magnitude for that frequency bin is set to zero.

4.3.3.3 Conclusion

In this section, the Spectral Subtraction de-noising technique that has been developed for speech signals was presented. This technique was designed for single-channel systems and performs the main noise suppression operations in the frequency domain via a Short-time Fourier Transform (STFT). This technique has recently been shown to extend to multi-

channel systems [12] and forms the basis of the novel 2-channel de-noising technique that will be presented in the later part of this chapter.

4.3.4 Wavelet Thresholding (WLET)

The Wavelet Thresholding de-noising algorithm is based on the use of the Wavelet Transform (WT). The Wavelet Transform (WT) was originally introduced to deal with the short-comings of the Fourier Transform (FT), which has a fixed resolution in frequency and time [13,14]. Similarly to the Fourier Transform (FT) where a periodic signal can be represented by a sum of sinusoids at different frequencies, the Wavelet Transform (WT) can represent a signal $f_0(t)$ by a linear combination of the scaling $\varphi(t)$ and the wavelet $\psi(t)$ functions of a mother wavelet:

$$f_0(t) = \sum_n \langle f_0(t), \psi_{1,n}(t) \rangle \psi_{1,n}(t) + \sum_n \langle f_0(t), \varphi_{1,n}(t) \rangle \varphi_{1,n}(t) \tag{4.23}$$

If we say that:

$$f_1(t) = \sum_n \langle f_0(t), \varphi_{1,n}(t) \rangle \varphi_{1,n}(t) = \sum_n c_n^1 \, \varphi_{1,n}(t) \tag{4.24}$$

$$\delta_1(t) = \sum_n \langle f_0(t), \psi_{1,n}(t) \rangle \psi_{1,n}(t) = \sum_n d_n^1 \, \psi_{1,n}(t) \tag{4.25}$$

Thus,
$$f_0(t) = \delta_1(t) + f_1(t) \tag{4.26}$$

If we continue to try and obtain δ_j or d^j, the jth decomposition of the signal $f_0(t)$, we get:

$$f_0(t) = \sum_{j=1}^{J} \delta_j(t) + f_J(t) \tag{4.27}$$

Thus in Wavelet Transform (WT), a mother wavelet can be used to break the signal $f_0(t)$ to show different level of details or decomposition from 1 to $j^{th} - d^j$, their similarity to the mother wavelet, and the location of these similarities in time. This allows for a much higher resolution – in terms of, the frequency resolution via the similarity at each level of decomposition and the temporal resolution via the location where these similarities occur. Therefore, the shape of the mother wavelet is very important and should be selected to reflect the wave shape of the expected or desired signal i.e. PCG or heart sound. A mother wavelet can be selected from wavelet families such as the Coiflet and the Daubechies. At higher levels of decomposition, the detail of the signal is less and this represents the lower frequencies of the signal.

Wavelet Thresholding (WLET) is performed by applying a threshold to the decomposed signals d^1 to d^j. There are many algorithms that can be used to calculate the value of the threshold depending on the characteristics of the desired signal and the noise for each level of decomposition, or alternatively a fixed one can be applied to all levels i.e. fixed form threshold. Furthermore, there are two main ways that the thresholding operation can be performed (shown in Figure 4.12):

i) Soft-Thresholding [7] – this method is the same as the Half-wave Rectification method discussed for the spectral subtraction technique. This is where the magnitude of the decomposed signal at each location is subtracted by the threshold and if the magnitude of the resulting subtraction is less than zero, the magnitude of the decomposed signal at that location is set to zero.

ii) Hard-Thresholding – this technique is slightly different from the soft-thresholding where the thresholding operation is only performed on the locations where the magnitude of the decomposed signal is less than the threshold, which are set to zero.
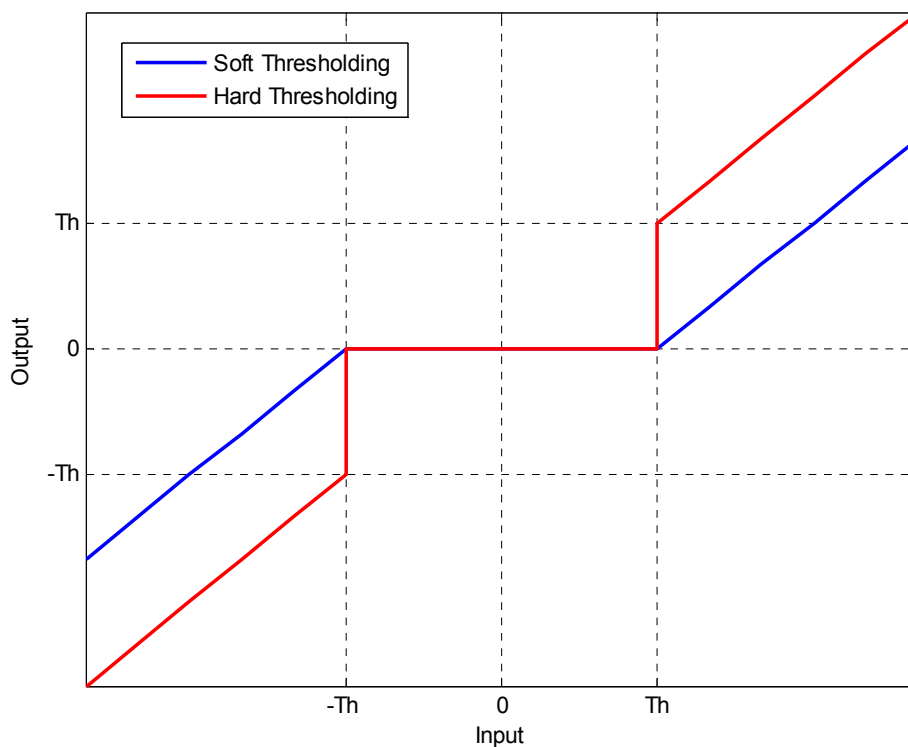
Figure 4.12: The input vs. output characteristics of the soft-thresholding (blue) and the hard thresholding (red) operations.

However, it has been found that the hard-thresholding operation introduces discontinuities in the signal because the locations where the magnitude exceed the threshold are left untouched. Thus, there is a large jump in the signal magnitude from the locations with magnitude below the threshold to those with magnitude above the threshold. Therefore, additional distortions are introduced to the reconstructed signal after the thresholding operation [11].

The Wavelet Thresholding (WLET) de-noising technique has emerged as the most popular noise-cancellation technique for heart sounds [8,11,19,20,23]. The results so far are very promising, therefore this technique will also be looked at in this study. The wavelet thresholding operation in this study was performed using the wavelet toolbox in MATLAB, via the *wavemenu.m* function (shown in Figure 4.13). The mother wavelet used is the Coiflet-2, as shown in Figure 4.14. A Soft-thresholding operation was applied to 8 levels of decomposition using a fixed form threshold for scaled white noise.
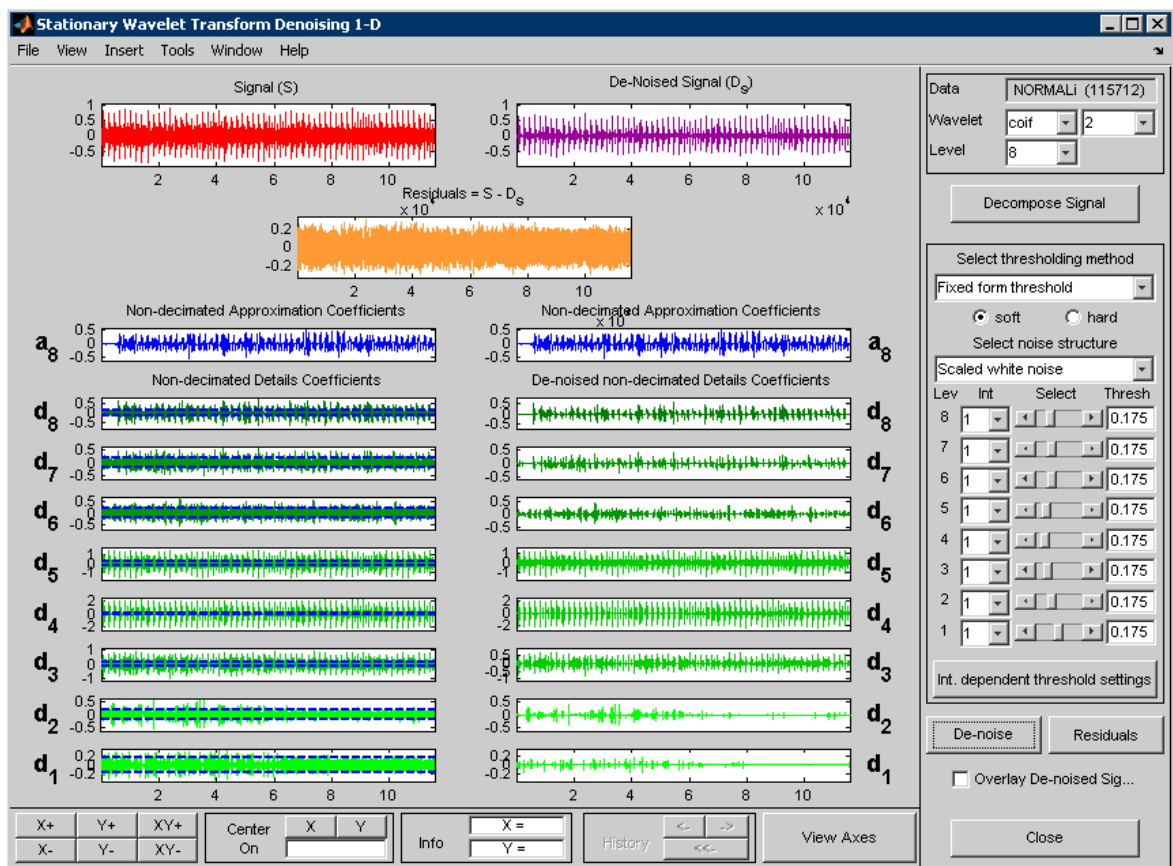
Figure 4.13: The user interface of the Stationary Wavelet Transform De-noising 1-D in MATLAB.
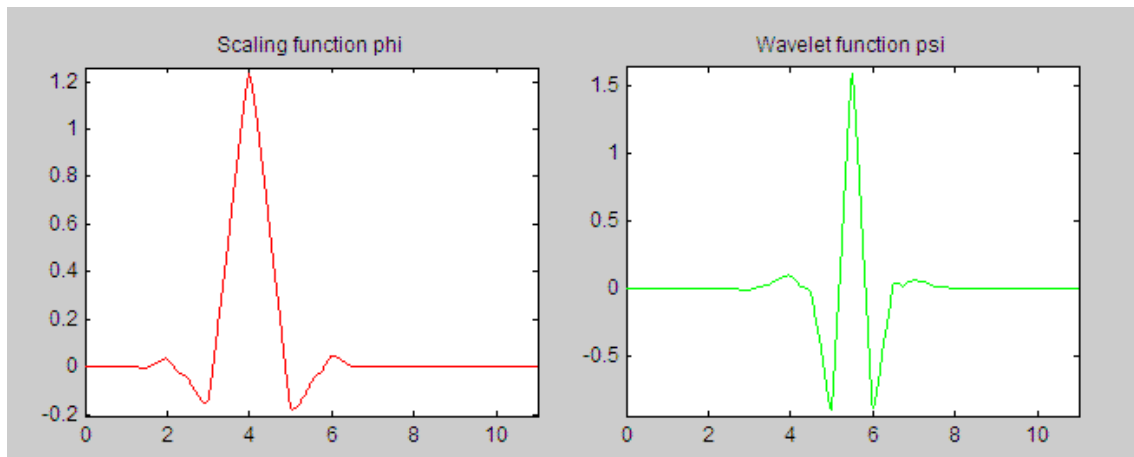
Figure 4.14: The Coiflet-2 scaling φ(t) and wavelet ψ(t) functions in MATLAB.

4.4 Novel Technique based on Spectral Subtraction: Inference Suppression via Spectral Comparison (ISSC)

In this section, we will propose a new algorithm for de-noising PCG data called Interference Suppression via Spectral Comparison (ISSC), based on Spectral Subtraction, that combines the main principles of both single-channel and multi-channel noise cancellation techniques discussed earlier in this chapter. This was achieved by finding a special characteristic that will distinguish the desired heart sound signal from the ambient acoustic noise and by using a reference microphone signal to help us better estimate the ambient noise or the ambient noise's spectrum.

By assuming that both the main and the reference microphones have the *same* sensitivity, the following can be deduced:

1. The intensity of the PCG or heart sound signal is *higher* in the main microphone than the reference microphone. This is because the heart sound is very faint and can only be heard when in direct contact or very close to the chest, near the heart.

2. When the main microphone is in contact with the skin, which has an attenuating effect on acoustic signals, the intensity of the ambient noise signal in the main microphone will be *lower* than the reference microphone. Thus, the magnitude spectrum of the ambient noise in the reference microphone signal will be *higher* than the same magnitude spectrum of the main microphone signal.

3. Therefore when the spectra of the main and the reference microphones, of the same time window, are compared, it should be easy to distinguish which frequency component belongs to the desired signal and which belongs to the noise. This is because the magnitude of the frequency bins that corresponds to the heart sound in the main microphone signal should be *higher* than in the reference microphone signal. While, the magnitude of the frequency bins that corresponds to the ambient acoustic noise in the main microphone signal should be the *opposite*.

The above rationale forms the basis of this novel noise cancellation technique, which allows us to discriminate the PCG signal components from noise. Furthermore, a manually variable threshold for comparison α was introduced, instead of a fixed one, to allow for more flexibility and optimisation.

The Interference Suppression via Spectral Comparison (ISSC) algorithm is shown in Figure 4.15. This algorithm first converts the discrete time-domain input signals of the main microphone d(n) and the reference microphone signal x(n) into their frequency domain representation using the Short-time Fourier Transform (STFT) with a rectangular window, w(n) = 1. Once their frequency spectra are obtained, the magnitude of each frequency bin, k, of the two spectra is compared. If the magnitude of the main microphone of a frequency bin is higher than the threshold (α)-scaled magnitude of the reference microphone, then that frequency bin is assumed to correspond to the PCG signal. Thus, the magnitude and phase of this frequency bin is kept and passed to the output O(k). However if the opposite occurs, then that frequency bin is assumed to correspond to the ambient acoustic noise. Thus, the magnitude of that frequency bin is attenuated by a factor β, where β « 1, but the phase is kept. After this process has been completed for all frequency bins, the resulting frequency spectrum O(k) is converted back into a discrete time-domain signal o(n) using the inverse Short-time Fourier Transform (ISTFT). It should also be noted that frame overlapping technique was not used. The first reason for this is because this will make the de-noising operation faster. But more importantly, frame overlapping is not required because the magnitude averaging operation of the normal spectral subtraction algorithm to estimate the noise is not necessary, since the noise can be estimated directly using the noise spectrum of the reference microphone signal.
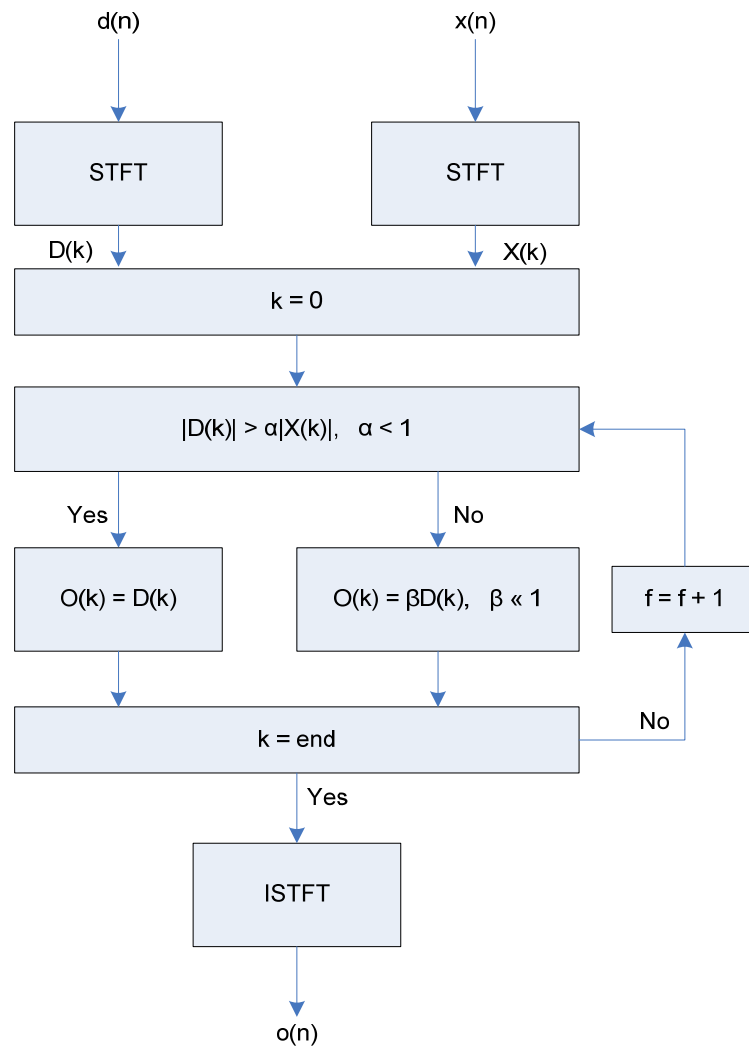
Figure 4.15: Flow chart of the novel technique based on spectral subtraction.

However when the spectra of the recordings were examined more closely, high intensity spikes were observed in the spectra of the main microphone at the mains power supply's frequency and its harmonics. Since the intensity of these spikes can be much higher in the main's than the reference's microphone spectra, so the present algorithm automatically assumed that these spikes are part of the PCG signal, which is not correct. Thus, an additional algorithm 'PeakRemove' was developed and embedded into the ISSC algorithm to remove these spikes. And further to this requirement, the PeakRemove was designed to suppress other spurious spikes within the main microphone's spectrum. This algorithm operates by looking at areas of large jumps in magnitude that exceed a threshold (thr) in the frequency spectrum from a base value and suppresses them. Figure 4.16 presents the effect of the PeakRemove algorithm on the frequency spectrum of the output signal and Figure 4.17 presents the effect of the algorithm in the time-domain.
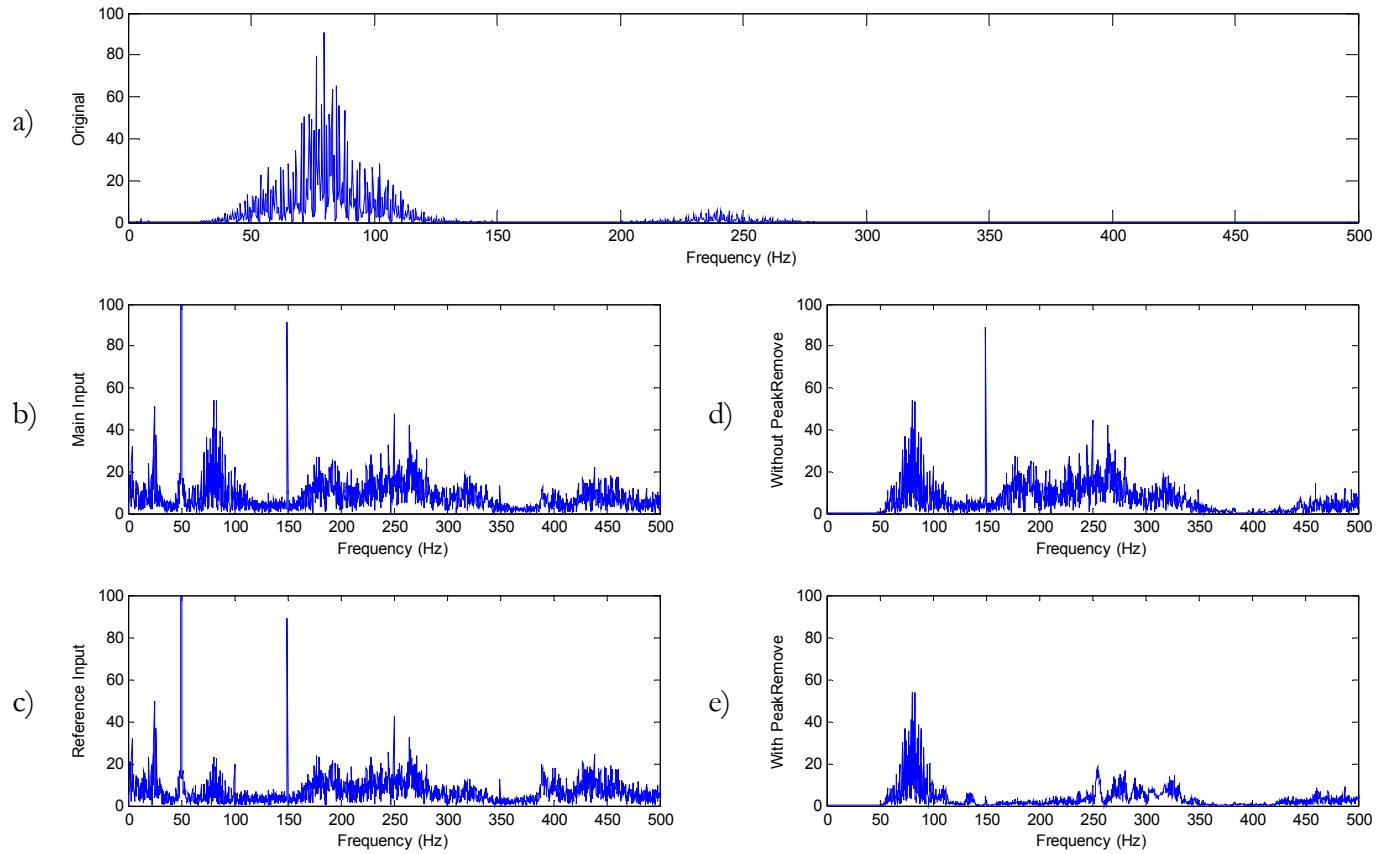
Figure 4.16: The effect of the PeakRemove algorithm on the frequency spectrum of the output signal ($\alpha = 1$, $\beta = 0.001$ and thr = 3), where a) represents the clean NORMAL heart sound, b) represents the recorded main microphone signal, c) represents the recorded reference microphone signal, d) represents the **output** signal *without* the PeakRemove algorithm, and e) represents the **output** signal with the PeakRemove algorithm.
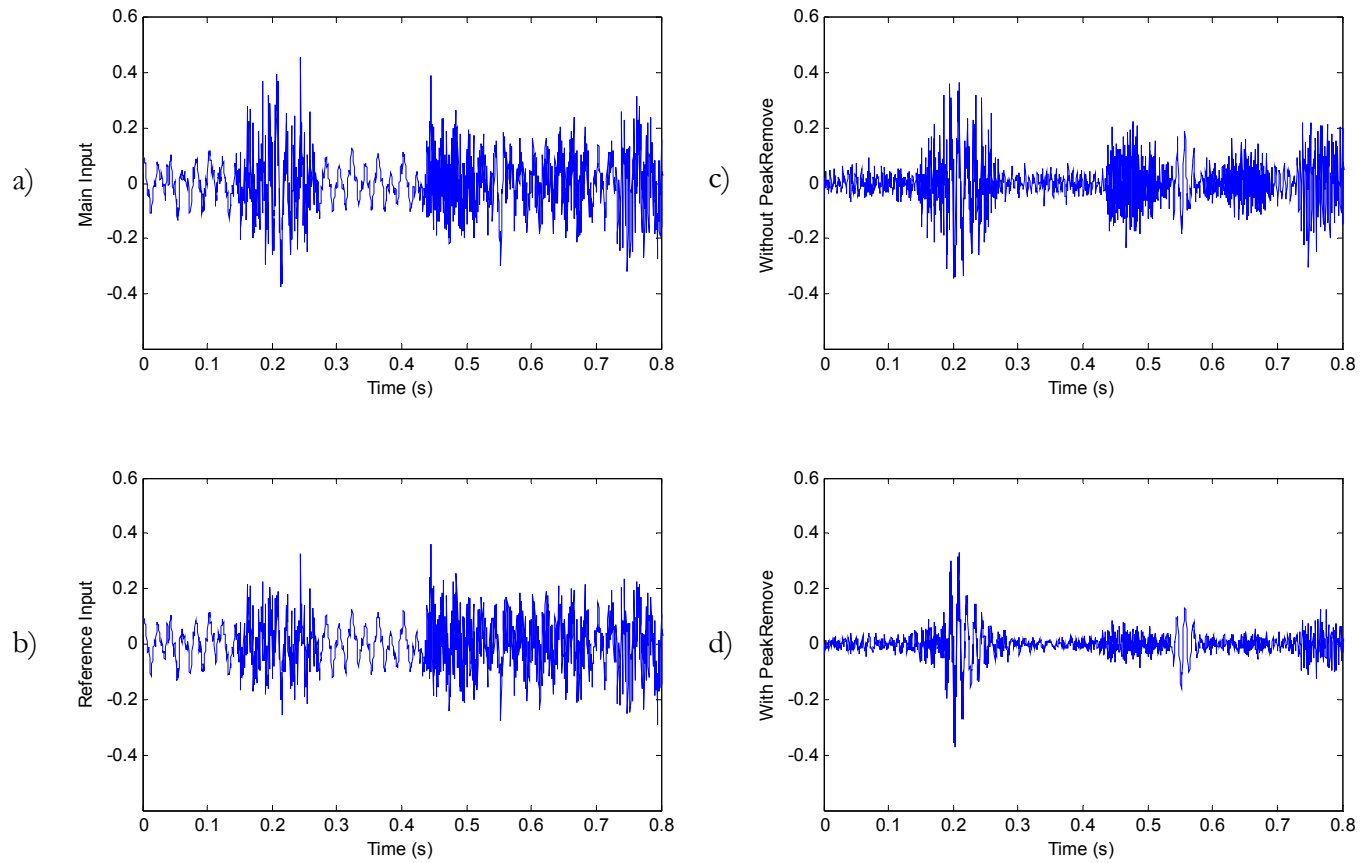
Figure 4.17: The effect of the PeakRemove algorithm on the time-domain output signal ($\alpha = 1$, $\beta = 0.001$ and thr = 3), where a) represents the recorded main microphone signal, b) represents the recorded reference microphone signal, c) represents the **output** signal *without* the PeakRemove algorithm, and d) represents the **output** signal with the PeakRemove algorithm.

4.5 Experimental Results

All 48 recordings were subjected to 5 different de-noising techniques in MATLAB (All the relevant MATLAB function and script files are shown in Appendix E):

(a) Simple subtraction (**SUB**) between the front and the back microphone,

(b) Adaptive LMS filtering (**LMS**) with 256 filter coefficients and $\mu = 0.01$,

(c) Adaptive RLS filtering (**RLS**) with 128 filter coefficients and $\delta = 1$,

(d) 1-channel Wavelet Thresholding (**WLET**) with Coiflet-2 as the mother wavelet and soft thresholding using 8 levels of decomposition (1-8) with a fixed form threshold for scaled white noise, and

(e) Interference Suppression via Spectral Comparison (**ISSC**) with $\alpha = 1.43$, $\beta = 0.001$, frame size $= 2048$, and thr $= 7.5$.

In this study, two measures of signal quality are used to compare the relative performance of the different de-noising algorithms (shown in Figure 4.18). The first measure is the signal-to-(noise plus) distortion ratio (SDR), derived from the mean square error (MSE) between the processed signals and the original 'clean' template signal in the time-domain:

$$SDR = 10 \cdot \log_{10}\left(\frac{\text{Power of the Original signal}}{\text{Mean Square Error}}\right) \tag{4.28}$$

This measure is termed as the signal-to-(noise plus) distortion ratio (SDR) rather than the signal-to-noise ratio (SNR) because any shift in phase, relative wave shape and amplitude differences should be strictly categorised as signal distortion rather than noise. To derive the SDR values, a correlation detector was used to locate the heart beats. The location with the maximum correlation is the place where the original 'clean' template signal maximally overlaps in time with the received or processed signal (* indicates complex conjugate):

$$R_{xy}(n) = \sum_{m=-\infty}^{\infty} y*(m)x(n+m) \tag{4.29}$$

The second measure is derived from a comparison between the signal power (in the regions where the heart sound signal is present) to the noise power (in the regions where there is no heart sound signal) in the time domain, which is a signal-to-noise ratio indicator (SNRi):

$$\text{SNRi} = 10 \cdot \log_{10} \left(\frac{\text{Power of Periods with signal present}}{\text{Power of ALL other periods}} \right) \tag{4.30}$$
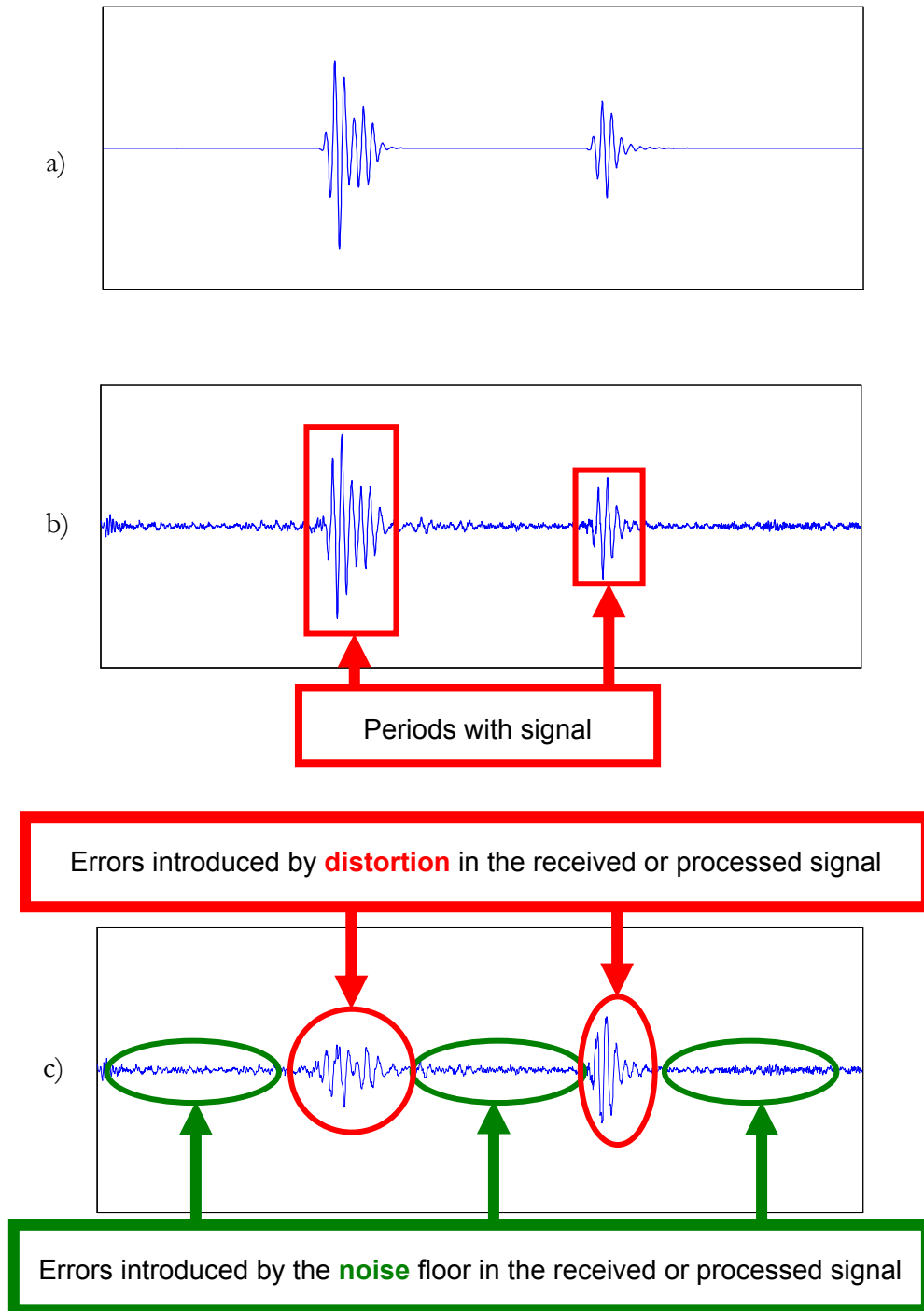
Figure 4.18: A diagram explanation of how the two measures of signal quality are obtained, where a) represents the original 'clean' template signal, b) represents the received or processed signal with red squares indicating the periods with heart sound signal, and c) the error between a) and b) used for calculating the mean square error (MSE).

4.6 Discussion

Table 4.3 and 4.4 present the full results of the experiment showing the received Signal-to-(noise plus) distortion ratio (SDR) of each recording and the SDR improvement when the heart sound or PCG data is passed through each of the de-noising algorithm.

Table 4.3: The full results of the received Signal-to-(noise plus) distortion ratio (SDR) and of the recordings with the front microphone in contact with the transmission surface and their improvement after the de-noising process. The best SDR improvement for that recording is highlighted in **blue**

		Received SDR (dB)	SDR Improvement (dB)				
			SUB	LMS	RLS	ISSC	WLET
C 1	NORMAL	**0.59**	4.30	1.75	2.87	**7.59**	5.91
	AR	**-3.21**	1.45	1.18	1.11	3.31	**3.69**
	AS	**-0.95**	0.45	0.44	0.35	-0.36	**1.07**
	MR	**-3.77**	-0.27	0.45	0.28	1.31	**2.36**
	ISM	**-4.78**	0.43	0.53	0.99	**2.20**	1.45
	MVP	**-2.30**	0.68	0.85	1.17	2.11	**2.76**
C 2	NORMAL	**-1.91**	-0.69	0.92	0.39	**4.54**	4.51
	AR	**-1.18**	-0.34	0.36	-1.05	1.62	**2.50**
	AS	**-0.99**	-0.22	0.21	-0.62	-0.27	**0.83**
	MR	**-2.37**	-0.29	-0.21	-1.45	1.33	**2.49**
	ISM	**-1.75**	-0.68	0.74	0.87	1.70	**2.20**
	MVP	**-1.11**	-0.33	0.75	0.31	2.08	**3.07**
C 3	NORMAL	**-1.27**	-2.46	1.74	0.22	-0.04	**2.63**
	AR	**-1.09**	-0.72	0.33	-1.51	-1.72	**1.38**
	AS	**-3.60**	-0.56	-0.36	-1.38	-1.42	**0.58**
	MR	**-1.97**	-0.52	0.14	-1.54	-1.45	**1.40**
	ISM	**-3.17**	-0.62	0.53	-0.03	-0.06	**1.25**
	MVP	**-2.12**	-0.68	0.22	-1.01	-0.83	**0.99**
C 4	NORMAL	**-0.05**	0.83	0.81	-1.26	**1.85**	0.71
	AR	**0.64**	**0.81**	0.23	-3.05	0.72	0.71
	AS	**-2.72**	0.21	0.24	**0.29**	0.01	0.19
	MR	**0.67**	0.44	-1.22	-4.35	0.72	**0.81**
	ISM	**-2.27**	0.32	0.30	0.28	**0.91**	0.44
	MVP	**0.34**	0.21	-1.06	-4.22	0.43	**0.47**

Table 4.4: The full results of the received Signal-to-(noise plus) distortion ratio (SDR) and of the recordings with the front microphone 1 cm away from the transmission surface and their improvement after the de-noising process. The best SDR improvement for that recording is highlighted in **blue**

		Received SDR (dB)	SNR* Improvement (dB)				
			SUB	LMS	RLS	ISSC	WLET
C 1	NORMAL	**-3.71**	3.43	0.97	1.40	**5.55**	4.63
	AR	**-2.91**	4.12	0.95	0.69	**6.68**	4.49
	AS	**-1.35**	**2.20**	0.82	1.00	1.22	2.17
	MR	**-2.99**	2.42	0.81	0.69	4.42	**4.48**
	ISM	**-4.09**	3.13	0.80	1.52	**4.83**	2.56
	MVP	**-2.21**	4.12	1.24	2.03	**4.99**	3.86
C 2	NORMAL	**-4.18**	-0.30	0.65	0.57	**3.21**	2.92
	AR	**-3.21**	-0.30	0.64	0.08	3.55	**3.59**
	AS	**-1.38**	-0.54	0.63	0.54	0.44	**1.93**
	MR	**-2.94**	-0.31	0.51	0.05	2.48	**3.98**
	ISM	**-4.11**	-0.39	0.57	0.82	**2.28**	2.06
	MVP	**-1.88**	-0.46	0.87	0.83	3.03	**3.62**
C 3	NORMAL	**-6.03**	0.09	**0.57**	0.27	-0.85	-0.01
	AR	**-4.16**	-1.56	**1.54**	1.22	-1.90	1.02
	AS	**-4.17**	-0.68	**0.84**	0.09	-1.50	0.26
	MR	**-4.57**	-1.37	**1.08**	0.39	-1.68	0.85
	ISM	**-5.25**	-0.47	**1.06**	0.79	-0.74	0.43
	MVP	**-5.03**	-0.97	**1.04**	0.73	-0.80	0.11
C 4	NORMAL	**-6.32**	**1.83**	0.19	0.44	1.77	-0.16
	AR	**-6.24**	2.16	0.20	0.49	**2.45**	-0.14
	AS	**-4.89**	**1.90**	0.56	1.22	1.59	-0.72
	MR	**-6.22**	**2.09**	0.20	0.46	1.49	-0.25
	ISM	**-6.30**	**1.59**	0.19	0.46	1.48	-0.28
	MVP	**-5.81**	2.08	0.35	0.76	**2.38**	-0.51
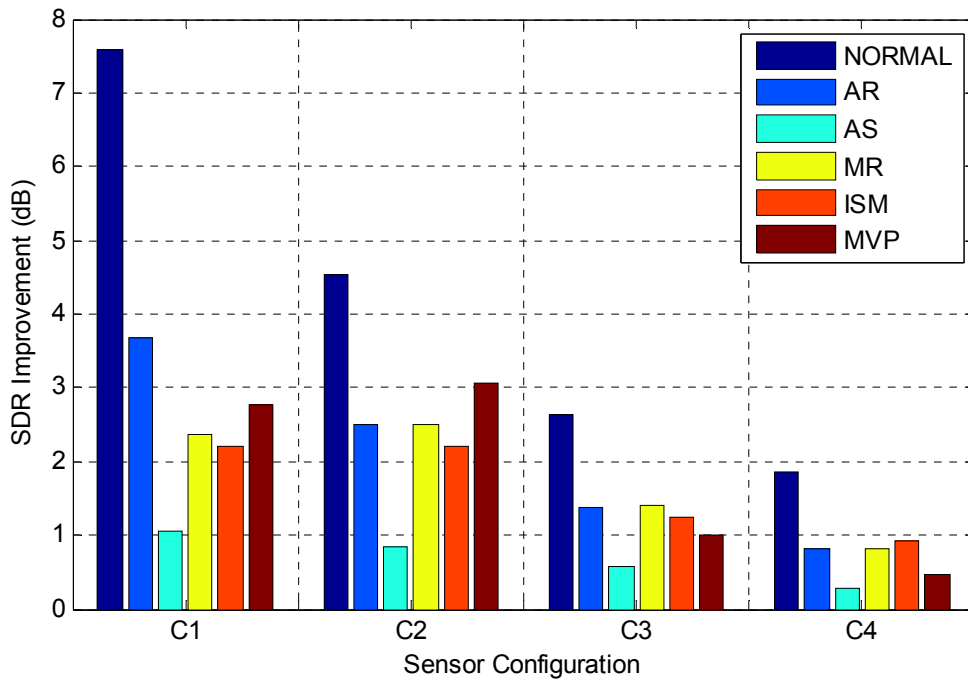
a)
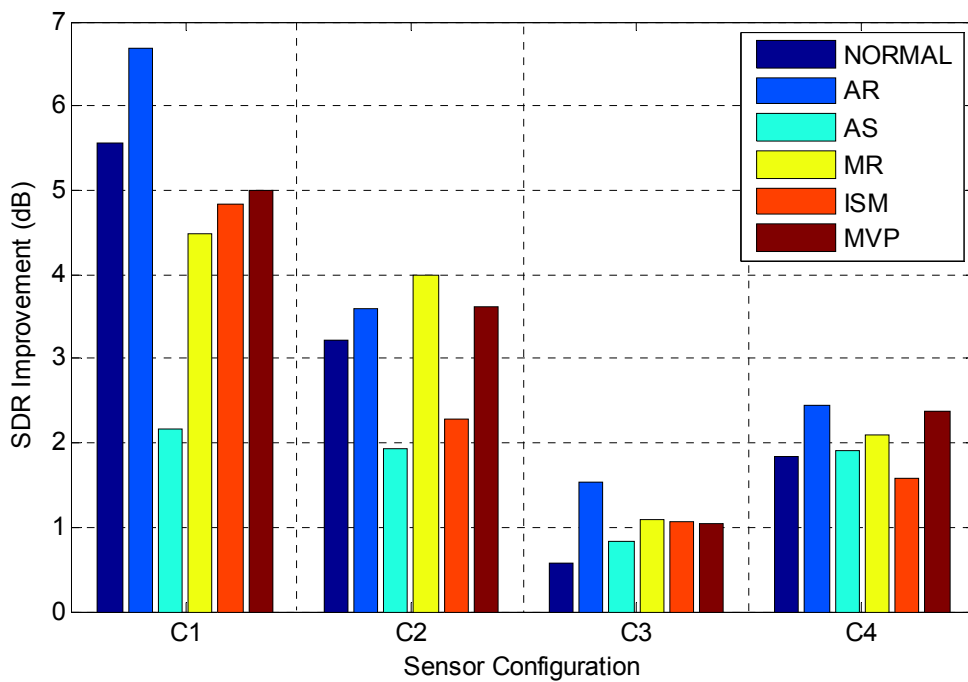
b)

Figure 4.19: The best SDR improvement for the different sensor configurations and heart sounds, when a) the front microphone is in contact with the transmission surface and b) the front microphone is 1 cm away from the transmission surface.

4.6.1 Comparing Sensor Configurations

Figure 4.19 a) and b) display the best SDR improvement obtained amongst the five different de-noising algorithms, for the four different sensor configurations C1 to C4 with the six different heart sounds. In both of these figures, it can be clearly seen that, in general, the sensor prototype configuration C1 out-performs all the other sensor configurations, for all six different heart sounds. The superior performance of this sensor prototype configuration is clearly seen in Figure 4.19 b) when the front microphone is one centimetre away from the transmission surface, which surprisingly also give a better SDR improvement for five of the six heart sounds.

Thus, the above figures indicate that the best sensor prototype configuration is C1 where the front and back microphones are both surface-mount silicon, *omni*-directional microphone (SPM0103ND3) made by Knowles Acoustics and that the de-noising algorithms perform best when the front microphone is one centimetre away from the transmission surface.

4.6.2 Comparing De-noising Algorithms

Since the sensor prototype configuration C1 provides the best de-noising performance of all the four sensor configurations, thus it would be best to discuss and compare the relative performances of the different de-noising algorithms for this sensor configuration. This is because this sensor configuration will most likely be implemented in the final sensor design. Figure 4.20 a) and b) display the SDR improvement obtained when using the five different de-noising algorithms on the six heart sounds recorded using sensor prototype configuration C1.

In Figure 4.20 a), the novel Interference Suppression via Spectral Comparison (ISSC) and the Wavelet Thresholding (WLET) techniques are the best two algorithms for de-noising PCG signals recorded when the front microphone was in contact with the transmission surface. The WLET technique performs best for 4 out of the six heart sounds – aortic regurgitation (AR), aortic stenosis (AS), mitral regurgitation (MR), and mitral valve prolapse (MVP). While the ISSC algorithm is best for normal (NORMAL) and innocent systolic murmur (ISM) heart sounds.

In Figure 4.20 b) where the front microphone was one centimetre away from the transmission surface, the novel Interference Suppression via Spectral Comparison (ISSC) performs best for 4 out of the six heart sounds – normal (NORMAL), aortic regurgitation (AR), innocent systolic murmur (ISM), and mitral valve prolapse (MVP). The Wavelet Thresholding (WLET)
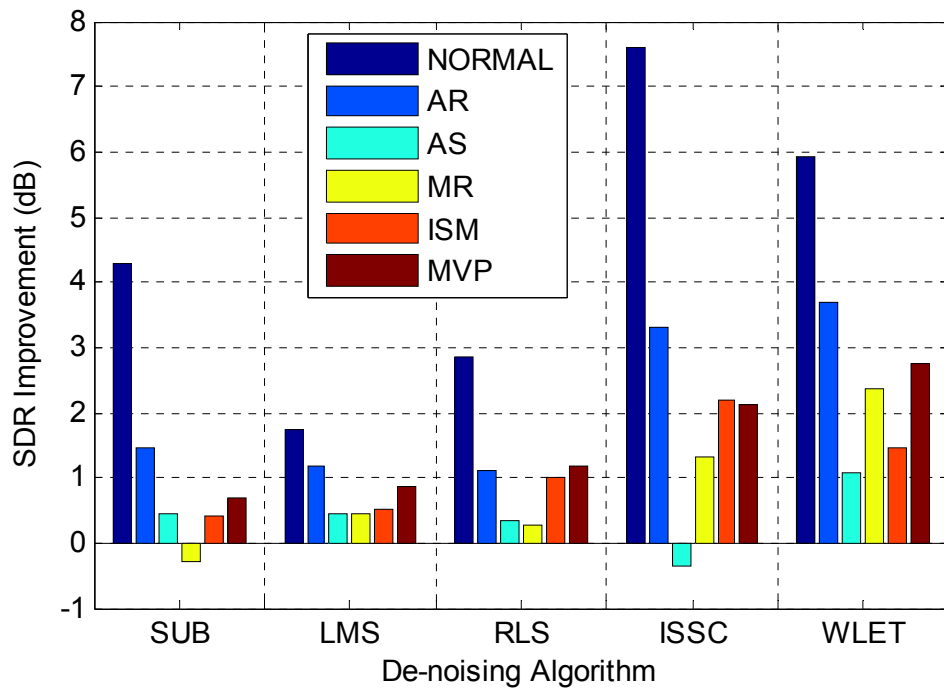
a)
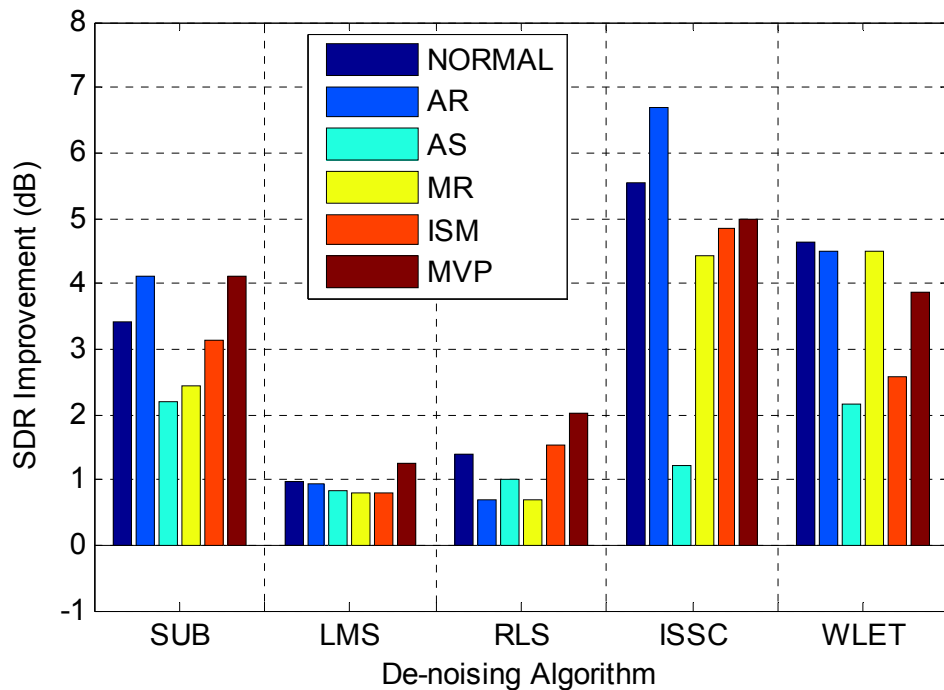
b)

Figure 4.20: The SDR improvement for the different de-noising algorithms and heart sounds for sensor configuration C1, when a) the front microphone is in contact with the transmission surface and b) the front microphone is 1 cm away.

algorithm is the best technique for mitral regurgitation (MR) heart sound and 2nd best noise cancellation technique. The simple subtraction (SUB) is the best technique for aortic stenosis (AS) heart sound and gives the 3rd best result in SDR improvement, with the two adaptive filters giving the worst result. It should also be noted that the simple subtraction (SUB) outperforms the WLET technique for three of the six heart sounds – aortic stenosis (AS), innocent systolic murmur (ISM), and mitral valve prolapse (MVP).

4.6.3 Comparing Heart Sounds

Out of the two most consistent de-noising techniques, namely the novel Interference Suppression via Spectral Comparison (ISSC) and the Wavelet Thresholding (WLET), the ISSC algorithm offers the best de-noising performance for normal (NORMAL) and innocent systolic murmur (ISM) heart sounds in Figure 4.20 a) and b).

For aortic regurgitation (AR), mitral regurgitation (MR), and mitral valve prolapse (MVP) heart sounds, the result is mixed. In Figure 4.20 a), the WLET technique performs better for all three heart sounds, but in Figure 4.20 b) the ISSC algorithm is clearly better for two heart sounds with the third showing a similar performance for both ISSC and WLET techniques.

As for the aortic stenosis (AS) heart sound, the Wavelet Thresholding (WLET) is the better algorithm compared to the novel Interference Suppression via Spectral Comparison (ISSC), which consistently struggles with this heart sound.

4.6.4 Comparing the Recording Set-ups

In this study of the de-noising algorithms, two recording set-ups were used – the first set-up was where the front microphone of the sensor prototype was in contact with the transmission surface and the second set-up was where the front microphone was one centimetre away from the transmission surface.

By inspecting the figures and the tables of SDR improvement values, it is clear that the first set-up (Figure 4.19 a) and Figure 4.20 a)) consistently produces a poorer SDR improvement than the second set-up (Figure 4.19 b) and Figure 4.20 b)). This is a surprising result because we would expect that when the microphone is closer to the heart sound source, we would have a higher received signal-to-noise ratio which should lead to higher signal-to-noise ratio improvements. However, this is not the case.

Up to this point the signal-to-noise ratio (SNR) values that have been presented, denoted by SDR, is a measure of the signal-to-noise plus distortion ratio. This is because it does not only compare the strength of the signal compared to the noise; but will also include any phase shift, relative wave shape and amplitude differences (i.e. distortion) in the processed signal as well. Therefore a second measure of signal quality, the signal-to-noise ratio indicator (SNRi) improvement, calculated by comparing the signal power (in the regions where the heart sound signal is present) to the noise power (in the regions where there is no heart sound signal), is introduced here to better represent the SNR for comparison with the SDR improvement for normal heart sound. This comparison is presented in Table 4.5.

Table 4.5: SNRi and SDR improvement comparison of the two recording set-ups for normal (NORMAL) heart sound

Algorithm	1st Set-up		2nd Set-up	
	SNRi	SDR	**SNRi**	SDR
ISSC	**20.29**	7.59	**12.26**	5.55
WLET	**18.94**	5.91	**13.79**	4.63
SUB	**15.12**	4.30	**9.33**	3.43
LMS	**4.56**	1.75	**2.22**	0.97
RLS	**8.33**	2.87	**3.64**	1.40

By comparing the SNRi and SDR improvement values of the novel Interference Suppression via Spectral Comparison (ISSC) case, it can be seen that the SDR is about 13 dBs lower than the SNRi in the 1st recording set-up and only about 7 dBs lower in the 2nd recording set-up. It is still unclear why this takes place. However, there appears to be extra distortion introduced when the front microphone is in contact with the transmission surface. This distortion can be more clearly observed in the frequency spectrum when comparing the recording of normal heart sound between the 1st and 2nd set-up, shown in Figure 4.21. This distortion remains even after the recorded heart sound signal is processed by the ISSC algorithm (shown in Figure 4.21 d)).
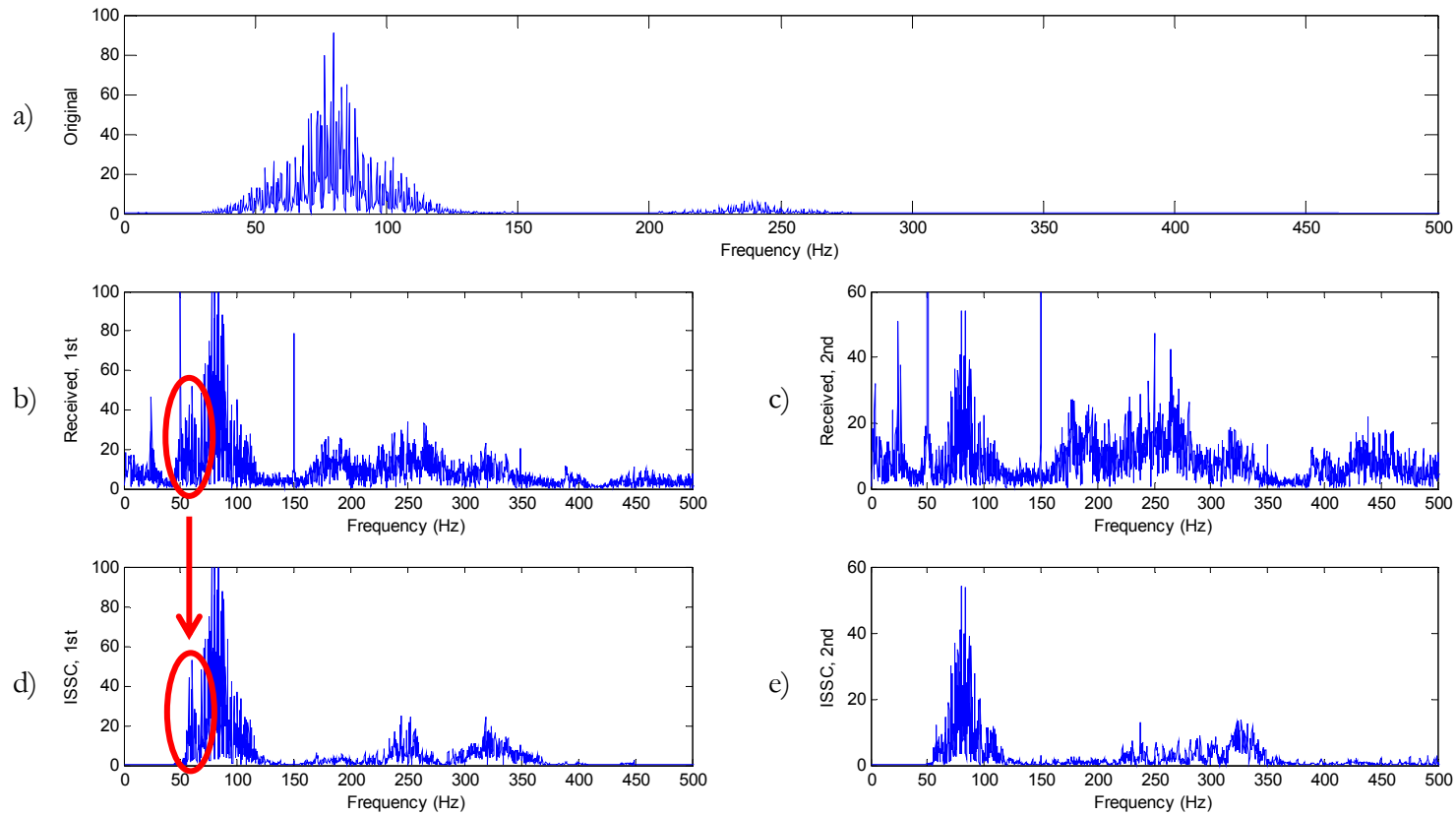
Figure 4.21: The frequency spectrum comparison of the recordings of normal (NORMAL) heart sound in the 1st set-up, showing the circle, and the 2nd set-up, where a) is the original clean heart sound, b) is the recording from the 1st set-up, c) the recording from the 2nd set-up, d) is the Interference Suppression via Spectral Comparison (ISSC) processed signal from the 1st set-up, and e) the ISSC processed signal from the 2nd set-up - extra distortion shown in **red** circles.

4.6.5 ISSC vs. WLET

Figure 4.22 presents an example of one beat of normal (NORMAL) heart sound that was recorded using sensor prototype configuration C1 where the front microphone is in contact with the transmission surface and after de-noising with the Interference Suppression via Spectral Comparison (ISSC) algorithm and the Wavelet Thresholding (WLET) algorithm.
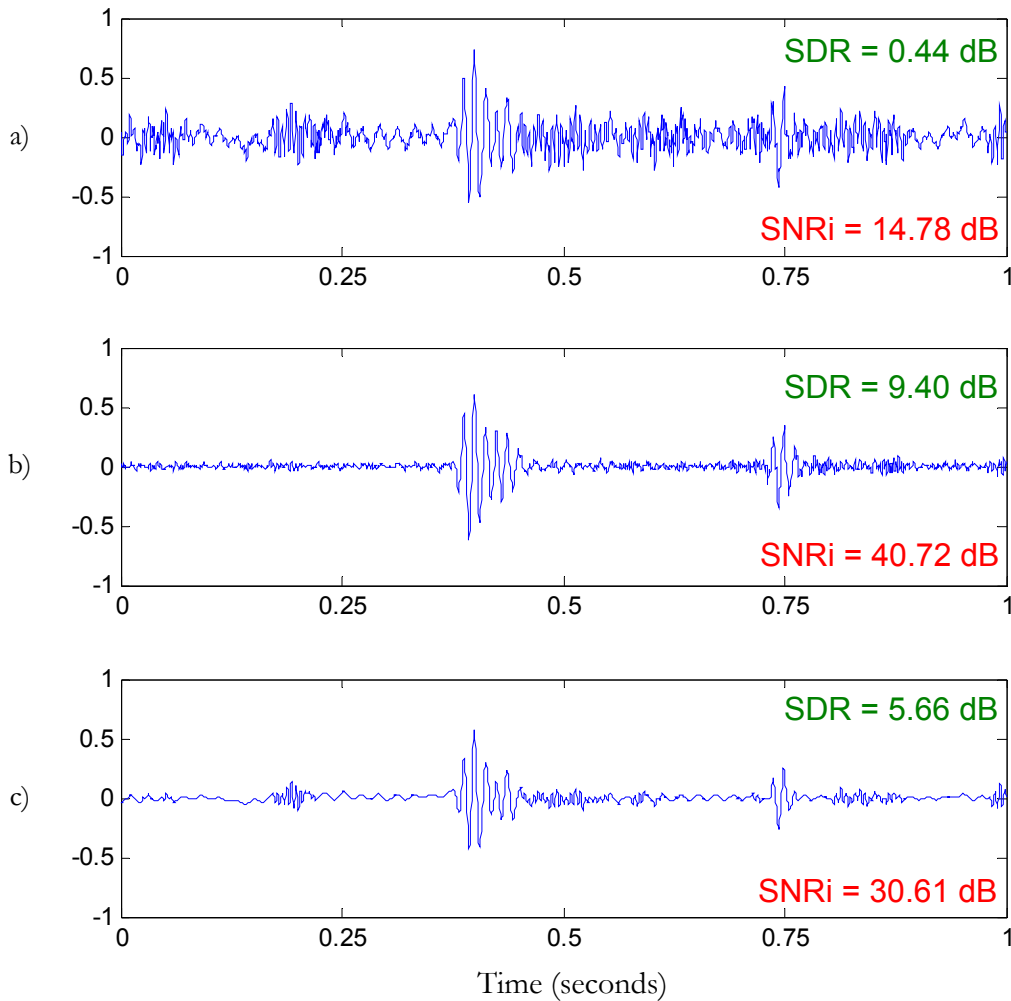
Figure 4.22: An example of one beat of normal (NORMAL) heart sound that was a) recorded using sensor prototype configuration C1 where the front microphone is in contact with the transmission surface and after de-noising with b) the Interference Suppression via Spectral Comparison (ISSC) algorithm and c) the Wavelet Thresholding (WLET) algorithm.

By inspecting Figure 4.22, it can be seen that the signal that has been processed with the WLET algorithm appears to have less noise than the ISSC processed signal. However, the

heart sound signal appears to be highly distorted by the WLET processing, especially towards the tail end of the 1st heart sound (S1) and both the front and back of the 2nd heart sound. These distortions would have contributed to increase the distortion in the heart sound and thus reduce the signal-to-(noise plus) distortion ratio, SDR, of the WLET processed signal. Furthermore, since the distortions introduced also reduce the amplitude of the heart sound signal of S1 and S2, therefore the SNRi is also lower for the WLET processed signal than the ISSC processed signal as indicated in Figure 4.22.

Thus, it should be noted that although the Wavelet Thresholding (WLET) de-noising technique is a very powerful and useful technique for suppressing noise in heart sounds, however this technique can be over-aggressive and can introduce significant distortions to the heart sound signal. The extent of how serious these added distortions affect the system is dependent on its application. If the monitoring system is used purely to monitor the heart rate of a person, there should not be any problem. However, if we would like to use such a system to diagnose heart disease, the Wavelet Thresholding (WLET) technique may not be suitable.

The novel Interference Suppression via Spectral Comparison (ISSC) algorithm is a better performer in terms of not introducing distortion during the de-noising process. This is because the heart sound wave shape is well-maintained and therefore produces a higher SNRi. However, its weakness compared to the WLET technique is its ability to deal with noise, since there are still some high frequency oscillations when the heart sound is absent. Still, the ISSC technique can suppress the noise enough to produce a higher SDR than the WLET technique.

4.6.6 α-scaled magnitude of ISSC

The threshold (α)-scaled magnitude comparison is made in the Interference Suppression via Spectral Comparison (ISSC) algorithm, as shown in Figure 4.15, instead of a straight forward one-to-one comparison because if we examine closely the magnitude of the frequency spectrum between the main and the reference microphone, as shown earlier in Figure 4.16 b) and c) respectively and below in Figure 4.23 a) and b), we will notice that the noise spectrum is surprisingly *stronger* in the main microphone than in the reference microphone. Thus, a one-to-one comparison of the magnitude of the main and the reference microphone will not succeed in removing the noise. Figure 4.23 illustrates the effect of varying the threshold α used for the magnitude comparison of the ISSC algorithm on the output frequency spectrum and the time-domain signal, for α = 1 and 1.43.
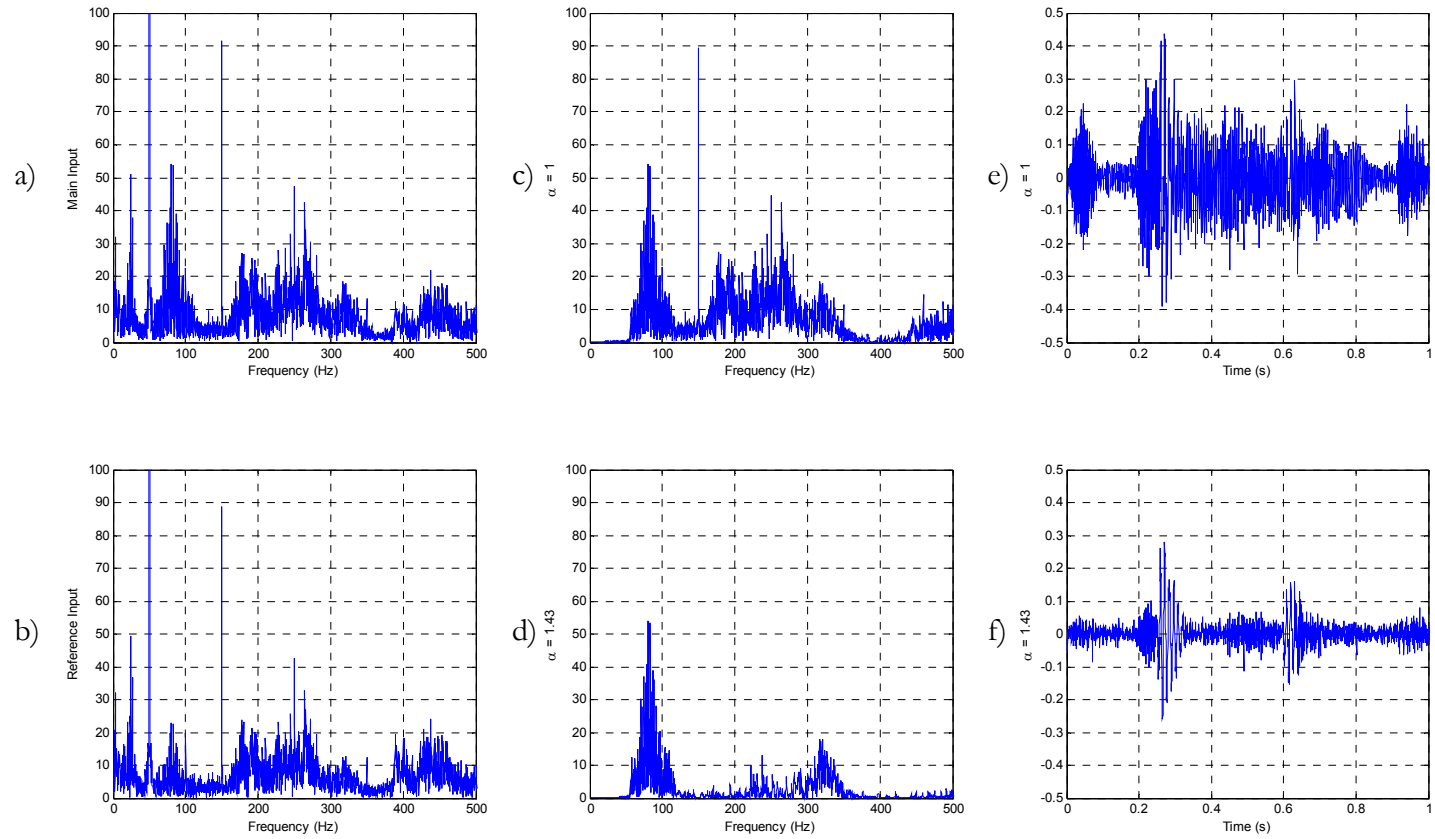
Figure 4.23: The effect of the threshold α on the output frequency spectrum and the time-domain signal, where a) is the frequency spectrum of the main microphone signal, b) is the frequency spectrum of the reference microphone signal, c) and d) are the frequency spectra of the output for α = 1 and 1.43 respectively, and e) and f) are the time-domain signals of the output for α = 1 and 1.43, respectively.

The higher noise spectrum in the main microphone signal compared to the reference is an unexpected behaviour since we have made an initial assumption in the introduction of the ISSC algorithm that the noise spectrum would be the opposite, due to the attenuating property of the skin. One of the possible attributing factors why this took place is that the transmission surface was not damped, so the noise generated by the speaker facing it could cause it to vibrate. Still, the reason why this behaviour occur is not clear, however by comparing Figure 4.23 c) & d) and e) & f), it can be clearly seen that by having an optimised variable threshold α (= 1.43) to scale the reference microphone spectrum in the ISSC algorithm, this unexpected behaviour can be dealt with and the noise strongly suppressed.

4.7 Conclusion

In this chapter, a study of the relative performance of five de-noising algorithms was conducted on six different heart sounds, four sensor prototype configurations and two recording set-ups. The algorithms considered include:

1. Simple Subtraction (SUB)

2. Adaptive Least Mean Square (LMS) Filter,

3. Adaptive Recursive Least Squares (RLS) Filter,

4. Wavelet Thresholding (WLET), and

5. The novel Interference Suppression via Spectral Comparison (ISSC) based on Spectral Subtraction.

Out of the four sensor prototype configurations (C1 to C4) used in the recording process, the best de-noising performance obtained, regardless of the algorithm that was used, was when the heart sounds were recorded using sensor configuration C1. This is where the front (main) and the back (reference) microphone are the same and have a high sensitivity (-22 dB compared to -47 dB for C4). The microphones used for configuration C1 are surface-mount silicon, *omni-directional* microphone (SPM0103ND3) made by Knowles Acoustics.

With respect to the de-noising algorithms, the Wavelet Thresholding (WLET) technique and the novel Interference Suppression via Spectral Comparison (ISSC) algorithm were found to deliver the best de-noising performance i.e. highest SDR improvement, in general, with the simple subtraction coming third.

Wavelet Thresholding (WLET) is a single-channel de-noising algorithm. It gave the best de-noising performance for four of the six heart sounds – aortic regurgitation (AR), aortic stenosis (AS), mitral regurgitation (MR), and mitral valve prolapse (MVP) for the 1st recording set-up, where the front microphone is in contact with the transmission surface, and for one of the six heart sounds – mitral regurgitation (MR) for the 2nd recording set-up, where the front microphone is one centimetre away from the transmission surface. Although, this technique was found at times to be too powerful and can introduce distortions to the heart sound signal.

The novel Interference Suppression via Spectral Comparison (ISSC) algorithm is a 2-channel de-noising algorithm based on the single-channel Spectral Subtraction technique, which performs the noise cancellation operation in the frequency domain. This algorithm was found to give the best de-noising performance for two of the six heart sounds – normal (NORMAL) and innocent systolic murmur (ISM) for the 1st set-up, and four of the six heart sounds – normal (NORMAL), aortic regurgitation (AR), innocent systolic murmur (ISM), and mitral valve prolapse (MVP) for the 2nd set-up.

The simple subtraction (SUB) technique is a very simple operation where the main and the reference microphone signals are subtracted from one another. This algorithm illustrated its potential when used with the 2nd set-up, where it gave the best de-noising performance for one of the six heart sounds – aortic stenosis (AS), as well as out-performing the Wavelet Thresholding (WLET) technique in two other heart sounds – innocent systolic murmur (ISM) and mitral valve prolapse (MVP).

However, in general, the 2nd recording set-up, where the front microphone is one centimetre away from the transmission surface, was found to give a superior (higher) SDR improvement than the 1st recording set-up, where the front microphone is in contact with the transmission surface. It is believed that this is associated with the additional distortion introduced when the microphone is in contact with the silicone material of the transmission surface, however this will require additional investigation.

Overall, we have shown that it is feasible to de-noise heart sound signals recorded in a controlled noisy environment and recover the heart sound pattern, which should be sufficient for the detection of the heart beat and thus, the computation of the heart rate. However, further studies are required to ascertain the effectiveness of these de-noising algorithms on real people, in real environments, and whether the heart sound obtained is sufficient for other applications, such as the diagnosis of heart diseases.

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Chapter 5

Mixed-Signals Integrated Circuit (IC) Design, Simulation, Layout and Testing

5.1 Introduction

Since the feasibility of the phonocardiography (PCG) long-term monitoring system concept has been demonstrated through:

1. The system level design, using only off-the-shelf components, in Chapter 3, and

2. The study of the de-noising algorithms and their performances when applied to heart sounds in Chapter 4.

Thus, the next phase in the development of this system is to miniaturise as much of the sensor electronics, analogue and digital, as practicable into a mixed-signals integrated circuit (IC).

The first half of this chapter will present the design rationale of the analogue front-end data acquisition circuit, the simulation results, the layout considerations and design, and the test results from the fabricated prototype ICs. The second half of this chapter will follow the same structure but for the digital circuitry.

The circuits presented in this chapter were designed and simulated in Cadence and fabricated on Austria Micro Systems 0.35 μm CMOS C35B4C3 3.3V 2P/4M technology with 4 metal layers and 2 poly-silicon layers

5.2 Analogue Circuit

Recalling the block diagram of the data acquisition chain of the sensor presented in Figure 3.1 and the result of the output transducer level in Figure 3.33 of Chapter 3, the analogue signal from the microphone transducer requires conditioning or amplification to a level compatible with the analog-to-digital converter (ADC) to maximally preserve the signal detail after quantisation. Furthermore, filtering of the transducer output signal is required to remove any out-of-band noise and to act as an anti-aliasing filter before the signal is sampled and digitised by the ADC, as outlined by the Nyquist sampling theorem $f_{sampling} \geq 2\ f_{max}$ [11].
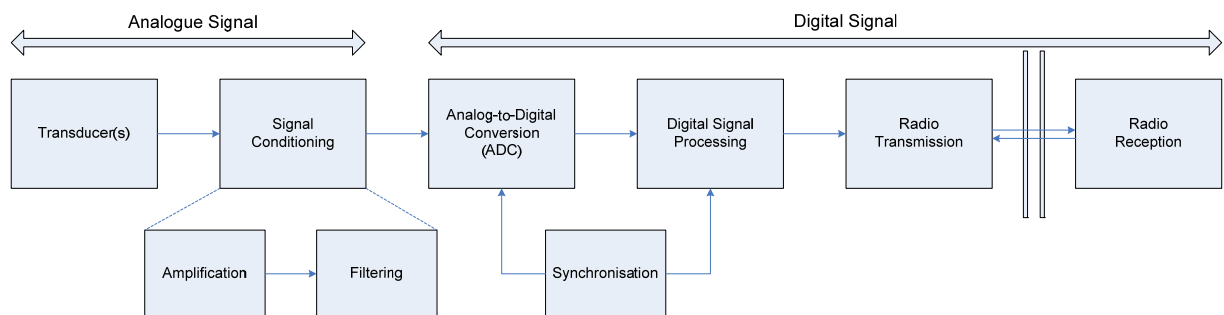
Recall Figure 3.1: The block diagram of the conceptual monitoring system.

For the study of the de-noising algorithms in Chapter 4, the heart sound captured by the microphone was amplified using an instrumentation amplifier (Burr-Brown INA118) and filtered using a cascade of two 2nd order, active, Sallen-Key, Bessel low-pass and high-pass filters.

Originally, it was intended for both the amplification stage and the filtering stage to be miniaturised on to an integrated circuit (IC). However due to time and funding constraints in this work, only the filtering stage was designed and fabricated as an integrated circuit (IC).

5.2.1 Analogue Circuit Design

5.2.1.1 Filter Topology

In order to construct a filter that best meet our specifications, we must consider all the possible types and topologies of filters available as well as the input signal level and the limitations imposed in integrated circuit (IC) design and the fabrication process.

Filter topologies can be divided into two main categories:

1. Passive, and

2. Active.

a)

b)

c)
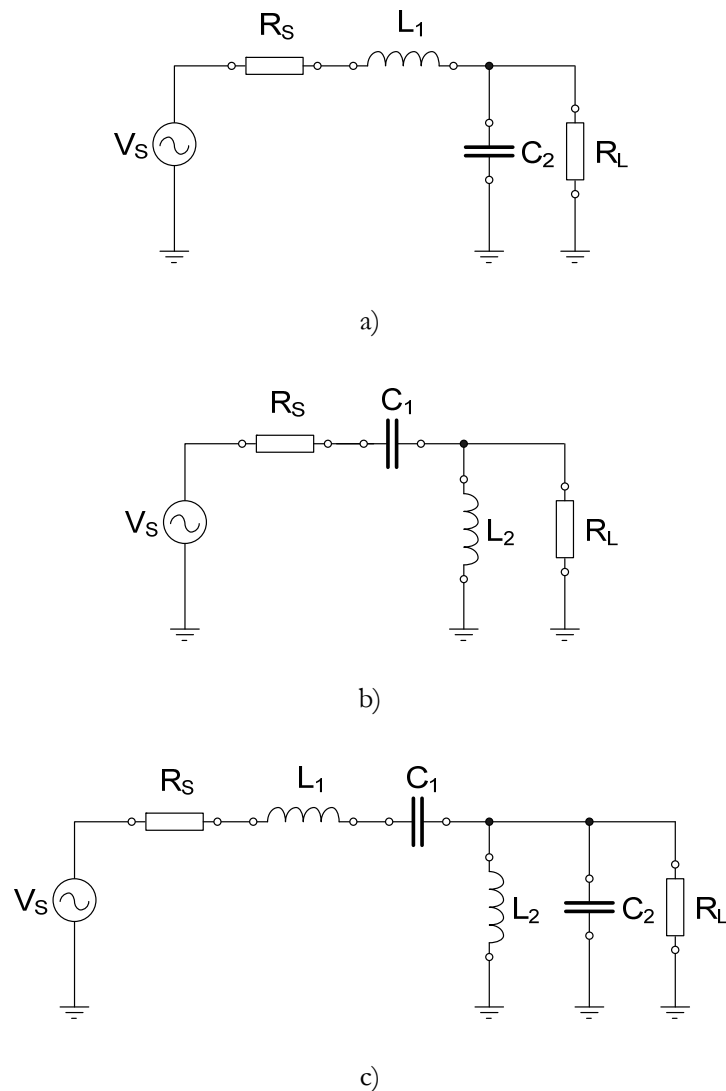
Figure 5.1: LC Ladder Network Structure for Bessel filters a) 2nd order low-pass, b) 2nd order high-pass, and c) 4th order band-pass.

Passive filters are constructed purely from passive components (resistors, R, capacitors, C, and inductors, L). The most commonly known topology is called the 'LC Ladder Network'. The LC structure is normally preferred over the RC structure because the resonance formed by the inductor and the capacitor allows the overall impedance to change rapidly, and thus causes a rapid change in the magnitude spectrum of the filter. Furthermore, the ladder structure allows higher order filters to be constructed by stacking more repetition of the basic

LC structure, terminated at both ends with a source R_S and a load resistance R_L. The ladder structures and normalised values of each capacitor and inductor are stated in tables for a specified order (1st, 2nd, 3rd, etc.) of **low-pass** filter, transfer characteristics (Butterworth, Chebyshev, Bessel and others) and ratio of source to load resistances (R_S:R_L). Additionally, different type of filtering can be achieved by exchanging the location of the capacitors and inductors (high-pass) or adding a series component in the signal path and a parallel component to ground (band-pass) so there is both a capacitor and an inductor in series in the signal path, and a capacitor and an inductor in parallel to ground. The LC ladder structure for these three types of filtering operation is shown in Figure 5.1. The real values for the capacitors and inductors can be calculated using the standard equations given (shown later).

The main advantage of the LC Ladder Network filter topology is that it has the best (least) sensitivity performance to the tolerances of the component values [14]. However, the disadvantage of passive filters is the reduction in the output signal compared to the input in the pass-band. This reduction is dependent on the source to load resistance ratio (R_S:R_L). If this ratio is very small (i.e. the load resistance is much larger than the source resistance), there will be no loss in the signal level. However, it is more likely that the ratio will be closer or equal to one, which is where maximal or 50% of the signal is lost in the pass-band.
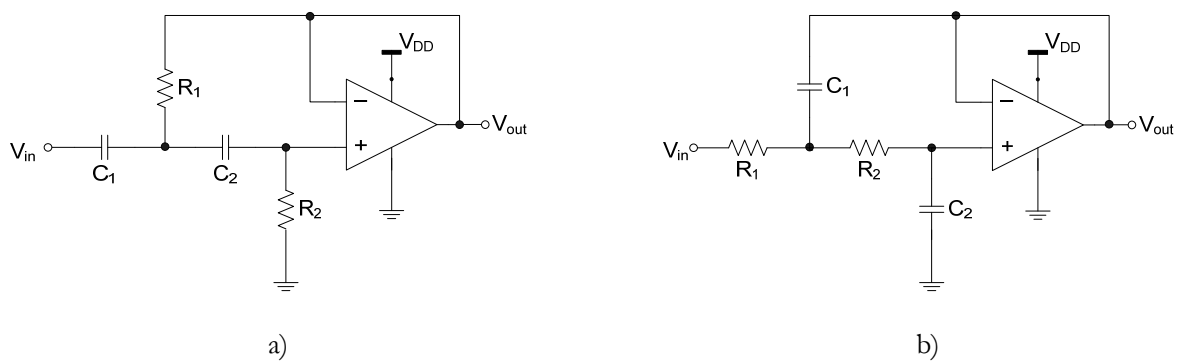
Recall Figure 3.29: a) A low-pass and b) a high-pass 2nd order Sallen-Key filter biquad.

Active filters, on the other hand, are constructed from both passive and active components. An active component is a component that requires a power source, and thus can act as a source of current and, in some cases, amplify the output signal of the filter. One such topologies, used in Chapter 4 for the study of de-noising algorithms, is called 'Sallen-Key filter' – a type of active RC filters. This filter topology involves the use of an operational amplifier (Op-Amp) as an active element, with some passive capacitors and resistors. A high-pass Sallen-Key filter can be constructed by exchanging the location of the resistors and

capacitors of the low-pass Sallen-Key filter. The structure for the 2nd order, low-pass and high-pass Sallen-Key filter biquads were shown in Figure 3.29 of Chapter 3. A band-pass Sallen-Key filter can be built by cascading the low-pass and the high-pass filter stages together.

The advantage of active filters is the ability to provide gain to the filtered signal. Furthermore, they are easy to understand and construct by cascading the biquads. However, this type of filter is more sensitive to tolerances in the component values.

5.2.1.2 Design of High-Order Filters [14]

In Chapter 4, a fourth order band-pass filter, which can be considered as a high-order filter, was constructed and employed for the filtering operation in the data acquisition chain. When we design high-order filters, the main point to contemplate is the sensitivity behaviour of the filter. There are three main methods that can be used to implement high-order filters of a transfer function, H(s):

$$H(s) = \frac{N(s)}{D(s)} = \frac{a_m s^m + a_{m-1} s^{m-1} + ... + a_1 s + a_0}{s^n + b_{n-1} s^{n-1} + ... + b_1 s + b_0} \tag{5.1}$$

where $n \geq m$ and $n > 2$

with acceptable sensitivity to tolerances in the passive component values [10,14]:

1. The cascade approach,

2. The multiple-loop feedback or coupled-biquad approach, and

3. The ladder simulation approach.

Cascade Realisation

The **cascade realisation** of the transfer function, H(s), (assuming the order of the filter is even) is achieved by factorising the transfer function into products of second-order or biquadratic functions.

$$H(s) = \prod_{i=1}^{n/2} T_i(s) = \prod_{i=1}^{n/2} k_i \frac{\alpha_{2i} s^2 + \alpha_{1i} s + \alpha_{0i}}{s^2 + s\,\omega_{0i}/Q_i + \omega_{0i}^2} \tag{5.2}$$

where, k_i is the gain constant

Each second-order function can be constructed using a biquad, and the overall transfer function can be achieved by cascading the biquads together. Although, this sounds very simple to do but there are three points that must be considered, especially with order of 6 or higher:

i) The pairing of the zeros and the poles for each biquadratic function,

ii) The order or sequence of the biquad cascade chain, and

iii) The gain distribution between the biquads.

Intuitively, these questions may not appear to be important because the cascade of the biquadratic functions forms the overall transfer function but the sensitivity and the dynamic range of the system is affected by these parameters. Figure 5.2 illustrates the structure of the cascade realisation for an nth-order filter.
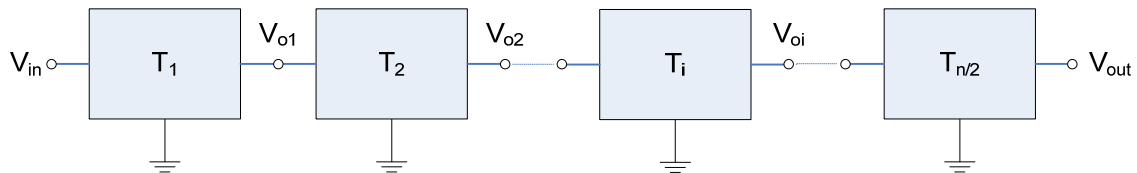
Figure 5.2: The structure of the cascade realisation for an nth-order filter.

Still this approach is popular with industry because of its ease of use – being modular, very easy to implement, tune, and efficient in its use of active components, as few as one operational amplifier per biquad. However, the disadvantage of this type of realisation lies in the fact that each critical frequency of the filter is *decoupled* from each other which, in some cases, makes cascade realisation too sensitive to tolerances in the component values for very high-order filters.

Multiple-Loop Feedback Realisation

The **multiple-loop feedback realisation** is an implementation that improves on the cascade realisation. It also requires factorisation of the transfer function into biquadratic functions, like the cascade realisation. However, each biquad is embedded in a resistive feedback configuration, rather than in a straightforward cascade manner. These feedback loops generate *coupling* between the biquads, where the pairing can be chosen to minimise the sensitivity of the overall filter to variations in the component values. Thus, this allows the designer to keep the modularity of the cascade realisation method while producing a reduced sensitivity in the pass-band. There are many feedback topologies available for designing this realisation, such as *follow-the-leader feedback* (FLF) and *leap-frog* (LF).

Ladder Simulation Realisation

The **ladder simulation realisation** is a result of the efforts to find an active circuit that would allow the superior sensitivity performance of the doubly terminated, passive LC ladder filter to be retained, by either emulating or simulating the passive circuit. In LC ladder filter topology, we need to incorporate inductors and capacitors on to the integrated circuit (IC). Although inductors can be constructed on integrated circuit (IC) from spirals of conductors, they are normally small in value and poor in quality due to substrate resistive losses and capacitive coupling [15]. Therefore, inductors are not normally built on integrated circuit (IC), especially for high-order filters. The ladder simulation was developed to overcome this issue and this approach can be divided into two sub-groups:

    i)   Element substitution, and

    ii)   Operational simulation.

Operational Simulation

a)

b)
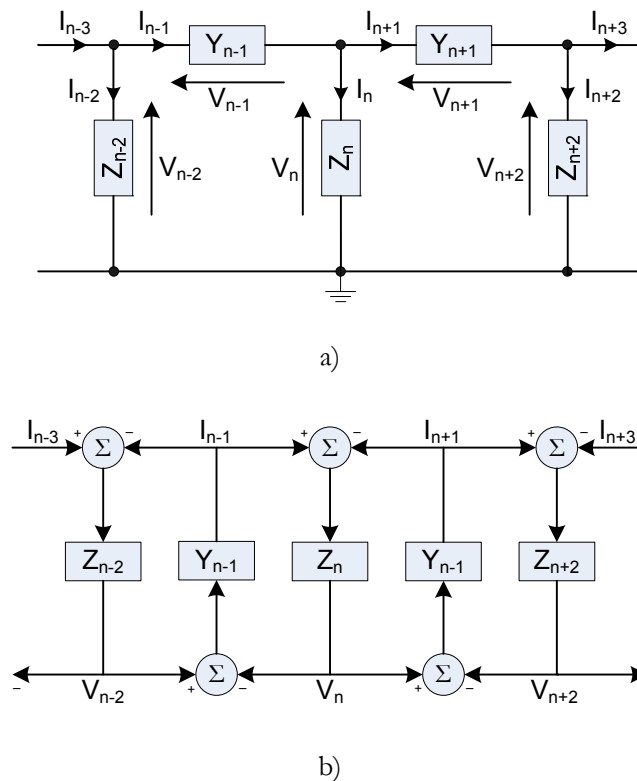
Figure 5.3: a) A section of a ladder network and b) its corresponding signal-flow graph representation.

For the operational simulation method, an active circuit must be designed to emulate the *internal operation* of the LC ladder prototype by simulating the equations describing the circuit's

performance i.e. Kirchhoff's voltage and current laws and the I-V characteristics of the ladder arms. Thus, essentially what the active circuit must perform is to simulate the signal-flow graph of the LC ladder for all voltages and currents. To perform this simulation, we need to design a number of analogue circuits to implement Kirchhoff's laws, by summing the currents and voltages and multiplying the currents or voltages with the impedance or admittance to obtain the voltage or current of each ladder arm. Figure 5.3 illustrates the signal-flow graph calculations required to simulate a section of a ladder prototype.

Element Substitution

In one of element substitution's implementations, inductors are removed altogether and replaced by an active circuit called 'capacitively loaded gyrator' [8]. The gyrator acts as an impedance inverter and make the input impedance of the circuit behaves as an inductor [14,17]. The simplest gyrator is made by connecting two transconductors back-to-back, where a transconductor is a differential voltage controlled current source with a gain or transconductance of g_m (Ampere/Volt). A block representation of a transconductor with a transconductance or gain of g_m is shown in Figure 5.4 and the relationship between the output current, I_O, and the two input voltages, V_+ and V_-, is given by:

$$I_O = g_m (V_+ - V_-) \tag{5.3}$$
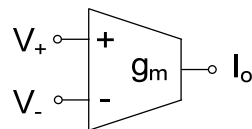
Figure 5.4: A block representation of a transconductor with a transconductance or gain of g_m

The capacitively loaded gyrator structures for reproducing the behaviour of grounded and floating inductors are shown in Figure 5.5 a) and b), respectively [6]. To prove that the capacitively loaded gyrator can mimic the behaviour of an inductor, we will examine the input impedance of the capacitively loaded gyrator structure in Figure 5.5 a). The input impedance Z_{IN} of a component is given by the relationship between its input voltage, V_{IN}, and its input current, I_{IN}:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \tag{5.4}$$

Thus, by tracing back the signal path to work out the input current I_{IN} when driving the capacitively loaded gyrator with a known input voltage V_{IN}, the input impedance Z_{IN} of the capacitively loaded gyrator structure in Figure 5.5 a) can be derived (see Appendix F). For a capacitor of value C (Farad), the input impedance, Z_{IN}, is:

$$Z_{IN} = j\omega \frac{C}{g_{m1} g_{m2}} \tag{5.5}$$

where, g_{m1} and g_{m2} are the transconductances of the 1st and 2nd transconductors.

a)

b)
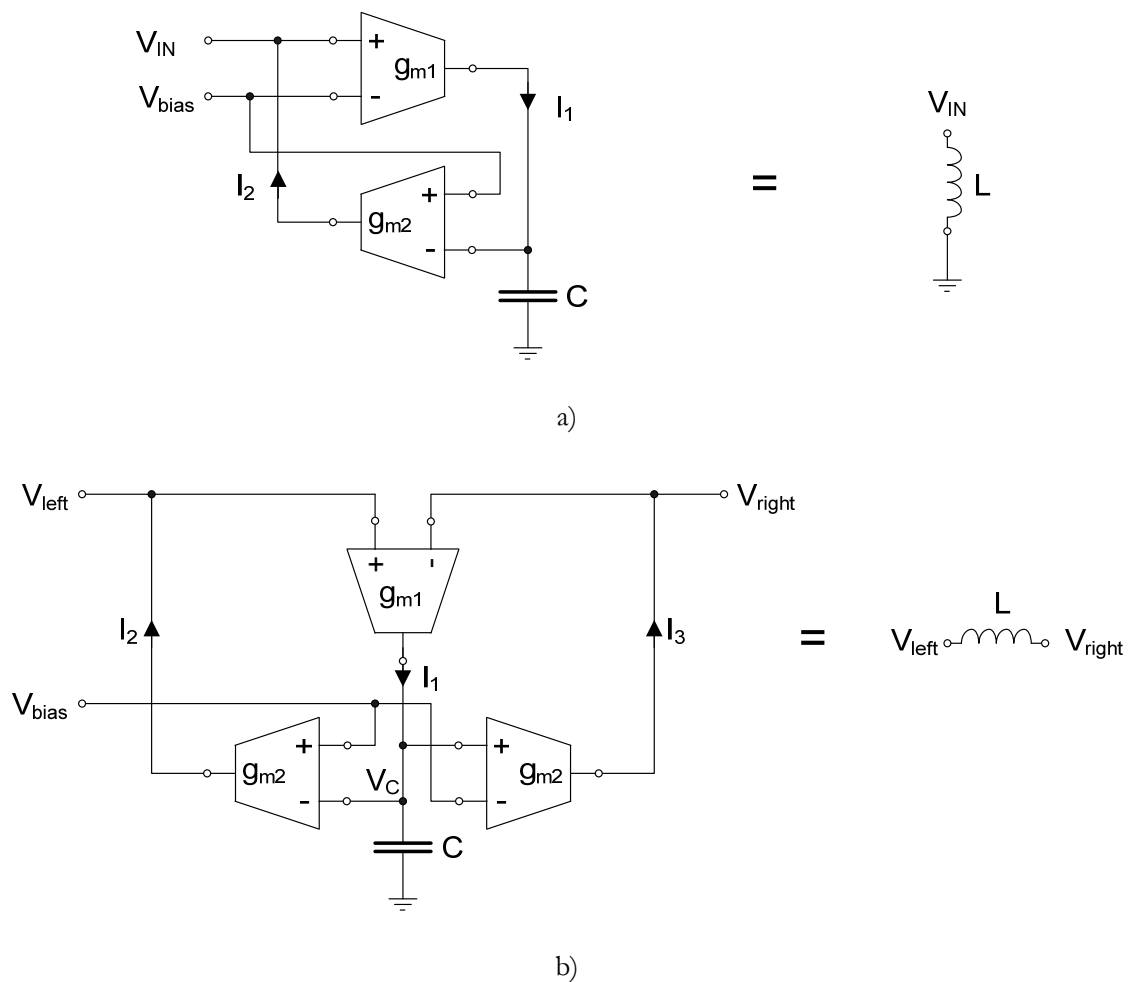
Figure 5.5: The capacitively loaded gyrator structures for reproducing the behaviour of a) grounded and b) floating inductors.

Since the impedance of an ideal inductor of value L (Henry) is given by:

$$Z = j\omega L \tag{5.6}$$

Therefore by comparing equations 5.5 and 5.6, it can be clearly seen that the capacitively loaded gyrator can be used to emulate the behaviour of an inductor with inductance:

$$L = \frac{C}{g_{m1}g_{m2}} \tag{5.7}$$

This ladder active filter topology is more commonly known as Gm-C filter.

As mentioned earlier, the advantage of the **ladder simulation** implementation is its superior sensitivity performance in the pass-band. However, the main disadvantage is that it requires many active elements compared to the other implementation methods. For example, the element substitution method would require five transconductors (three for the floating inductor and two for the grounded inductor) to construct a 4th order band-pass filter as shown in Figure 5.1 c) compared to approximately two operational amplifiers (Op-Amp) in the cascade or multiple-loop feedback implementations.

Conclusion

In this thesis, the element substitution of the ladder simulation approach was preferred over the other approaches. This is firstly because in integrated circuits (IC), the variations in the dimensions of any component are inherent in the fabrication process whether it is a transistor, a capacitor, a resistor or an inductor. Thus, variations in the component values are expected to occur even when all layout design considerations are followed. Therefore, it would be best to employ a filter topology which is least sensitive to tolerances or variations in the component values, to perform the filtering operation in the data acquisition chain. Secondly, a good transconductor design, with a wide linear range and fairly constant transconductance, is easier to achieve than a good operational amplifier (Op-Amp) design. Lastly, since we are only dealing with 4th order band-pass filters, the total number of transconductors would still be low for our application (10 for 2-channel, 4th order Bessel band-pass filter). Therefore the main focus of this analog circuit design section will be the design of the transconductor, which forms the basic building block of the capacitively loaded gyrator.

5.2.1.3 Transconductor Design

In this work, we are trying to acquire heart sound data via a microphone transducer to ascertain the patient's heart function, which produces a 25 mV peak-to-peak signal for a person at rest (from Chapter 3). This signal can increase by four or five folds (up to 125 mV peak-to-peak) when exercising. Since the quality of the audio signal can be greatly affected by

distortion, therefore it is necessary to pay extra attention to the linearity of the transconductor or the flatness of the transconductance over the peak-to-peak signal range. The linearity of a differential pair can be well-regulated for small input signals of a few milli-Volts. Thus, it is more practical to modify the data acquisition chain of our sensor to filter the microphone transducer signal (in milli-Volts) first before amplifying it to the required signal level of the ADC (in Volts). However, to just modify the data acquisition chain is not enough because the maximum expected peak-to-peak signal range at the microphone output is about 100-150 mV. Therefore, the techniques to increase or extend the linearity range of the transconductor must be found.

Basic Differential Pair

The simplest transconductor structure is a differential pair. A differential pair, shown in Figure 5.6 a), operates by using a difference in voltage between its two input terminals, V_+ and V_-, to generate a difference in current in its left and right branches of the circuit, I_+ and I_-, which results in the output current, I_O:

$$I_O = I_+ - I_-$$

(5.8)

or

$$I_O = g_m \left(V_+ - V_- \right)$$

(5.9)

where g_m is the transconductance.

The transconductance, g_m, of the differential pair is controlled by the tail or bias current of the differential pair, I_{bias}. The two differential pair structures shown in Figure 5.6 a) and b) both operate in the same manner, with the exception that the latter have a mirrored current output. The main advantage of the differential pair structure in Figure 5.6 b) over that in Figure 5.6 a) is that the output is allowed to swing more linearly over a larger range of voltage between the supply V_{DD} and ground (G_{ND}) or 0V. However, the main disadvantage of the structure in Figure 5.6 b) is that it will consume $2 \times I_-$ more current than the structure in Figure 5.6 a), as well as requiring four more transistors and therefore more integrated circuit (IC) area. Thus, there is always a trade-off to be made in circuit design. Still, the most important consideration is to produce a design that is best suited to the application.

a)

b)
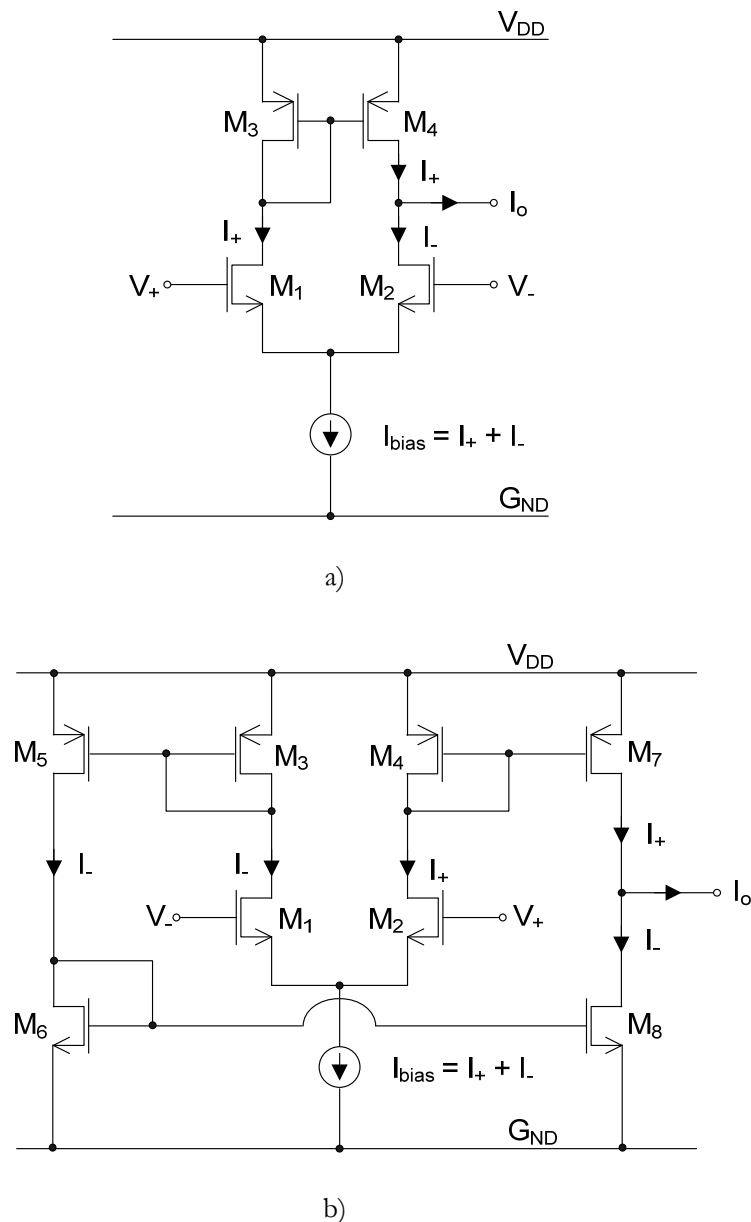
Figure 5.6: Differential pair structure with a) basic current output and b) mirrored current output.

Source Degeneration

One of the simplest technique to increase the linearity range is called 'source degeneration' or 'emitter degeneration' [5,12]. This is where a linear resistor or a diode-connected MOS transistor is added to each signal branch of the differential pair (shown in Figure 5.7). Source degeneration reduces the gain or the transconductance of the differential pair circuit by lowering the signal swing between the gate and the source of the transistor. With a large degeneration resistance R_E, the linear region of the differential pair is increased by approximately $I_{bias}R_E$ [5]. However in integrated circuit (IC) design, the diode-connected MOS

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transistor version is preferred because a high-quality resistor, which is hard to achieve in integrated circuit (IC), is required. Furthermore, in this technique there are trade-offs to be made between linearity, transconductance gain, resistive noise and power dissipation, due to the increase in the supply voltage V_{DD} to accommodate the voltage headroom required for the degeneration resistor or diode-connected transistor.
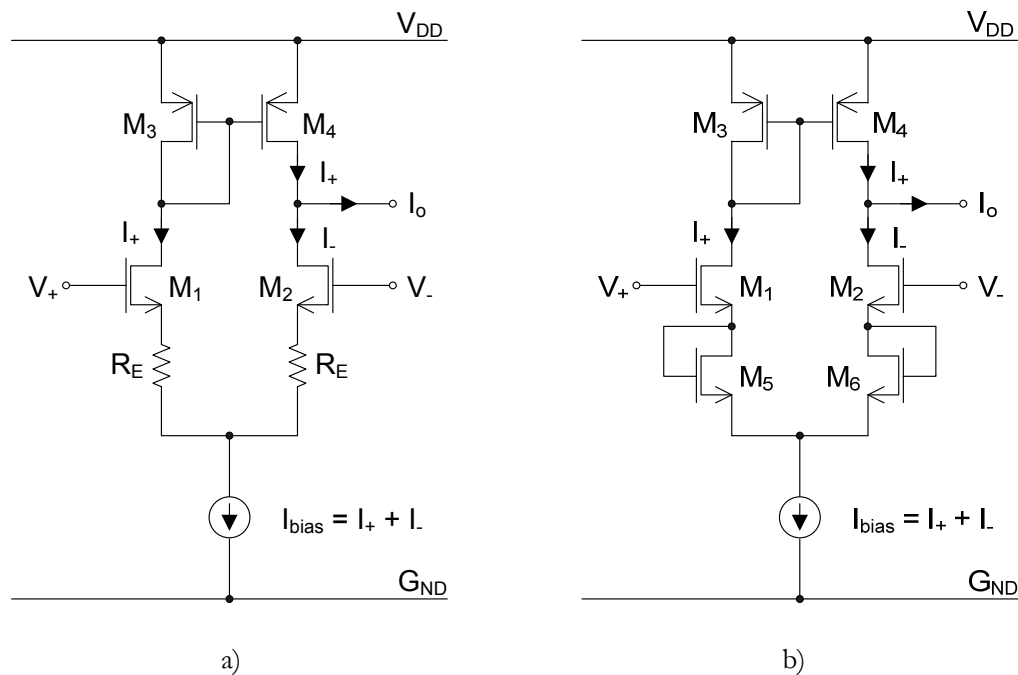
Figure 5.7: A source-degenerated differential pair a) with linear resistors and b) with diode connected MOS transistors.

Multi-Tanh Technique

Another technique that can be used is called 'Multi-Tanh'. This technique was first introduced in 1968 by Baldwin and Rigby using Bipolar Junction Transistor (BJT) technology [4]. This principle was further developed by Gilbert and others in the mid-1970s [4]. More recently, Kimura has introduced other more superior techniques termed 'super-multi-tanh' and 'ultra-multi-tanh' techniques, respectively [9]. Furthermore, this multi-tanh technique has been shown to work on CMOS technology [13].

The multi-tanh technique can be used to extend the linear range of a transconductor by having two or more differential pairs connected together and configured in a way so that each pair's transconductance adds up to form a super wide and flat transconductance or a super wide and linear transconductor. For BJT technology, the position and the value of each pair's transconductance can be tuned by varying the ratio of the emitter area and the tail current of

each differential pair, respectively; the same effect can be achieved in CMOS technology by varying the ratio of the sizes (normally the width, W) of the paired transistors and the tail or bias current, I_{bias}, of each differential pair, respectively. The CMOS multi-tanh transconductors and their transconductance characteristics are shown in Figure 5.8 for a doublet and Figure 5.9 for a triplet.
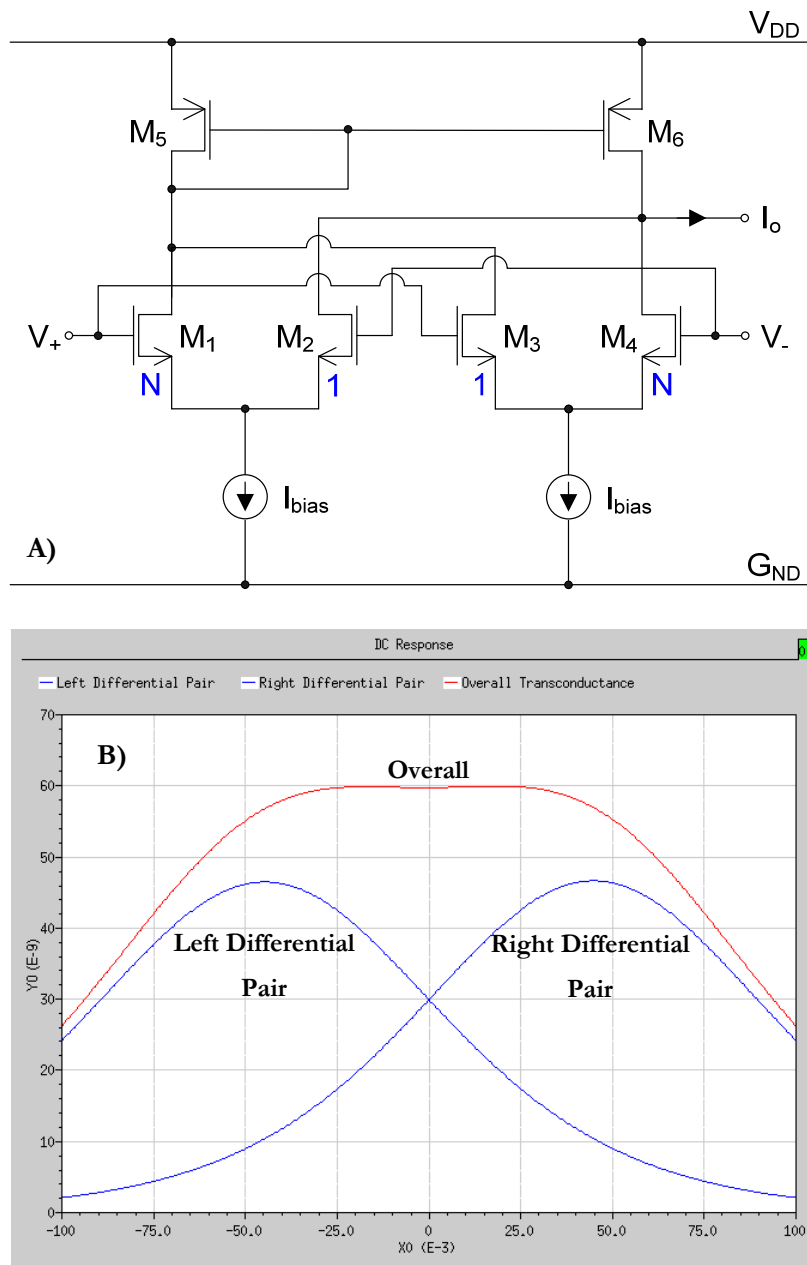
Figure 5.8: The CMOS a) doublet Multi-tanh transconductors circuit and b) its transconductance characteristic.
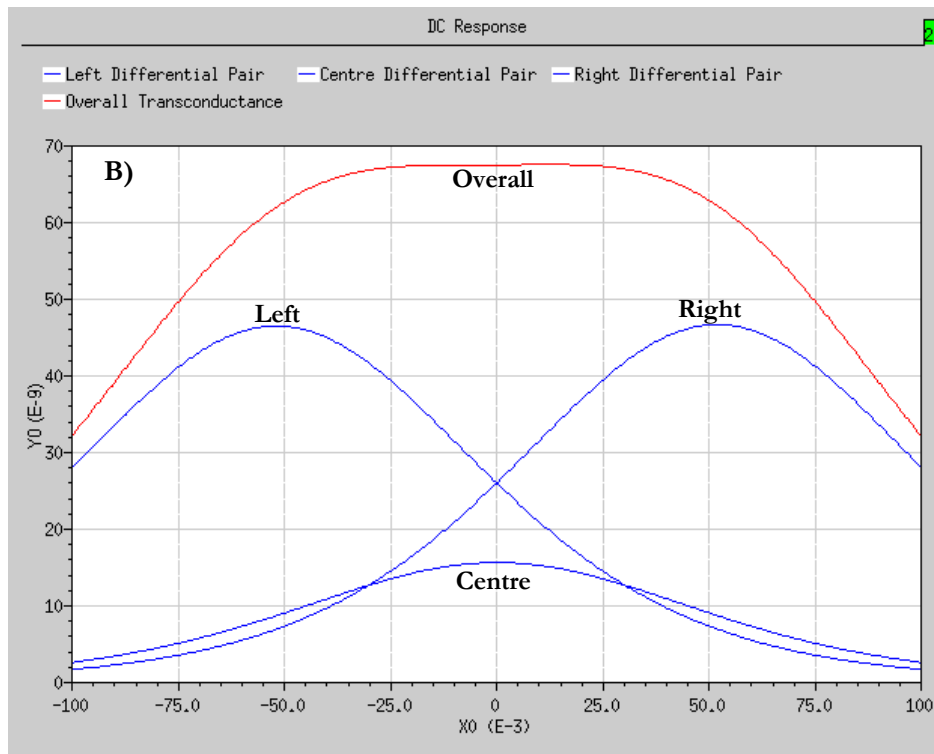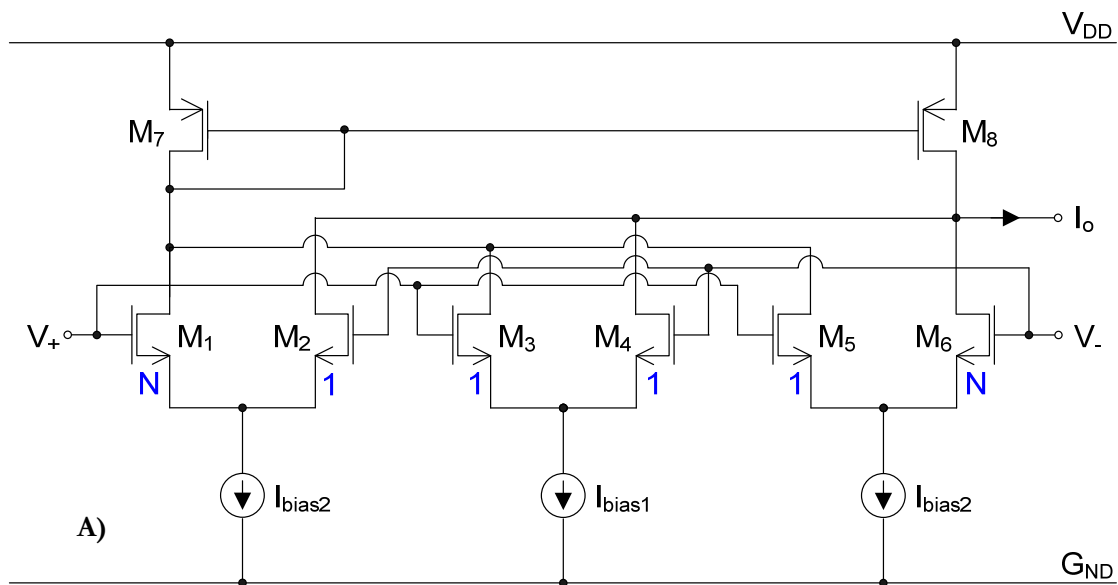
Figure 5.9: The CMOS a) triplet Multi-tanh transconductors circuit and b) its transconductance characteristic.

In this work, the **multi-tanh** triplet or 3 differential pairs as illustrated in Figure 5.9 was chosen. This is to ensure flatness of the transconductance in the linear region and a reasonably wide linear range. Figure 5.10 compares the linear region and the transconductance characteristics between the basic differential pair, the source-degenerated differential pair, and the multi-tanh triplet.

a)   b)
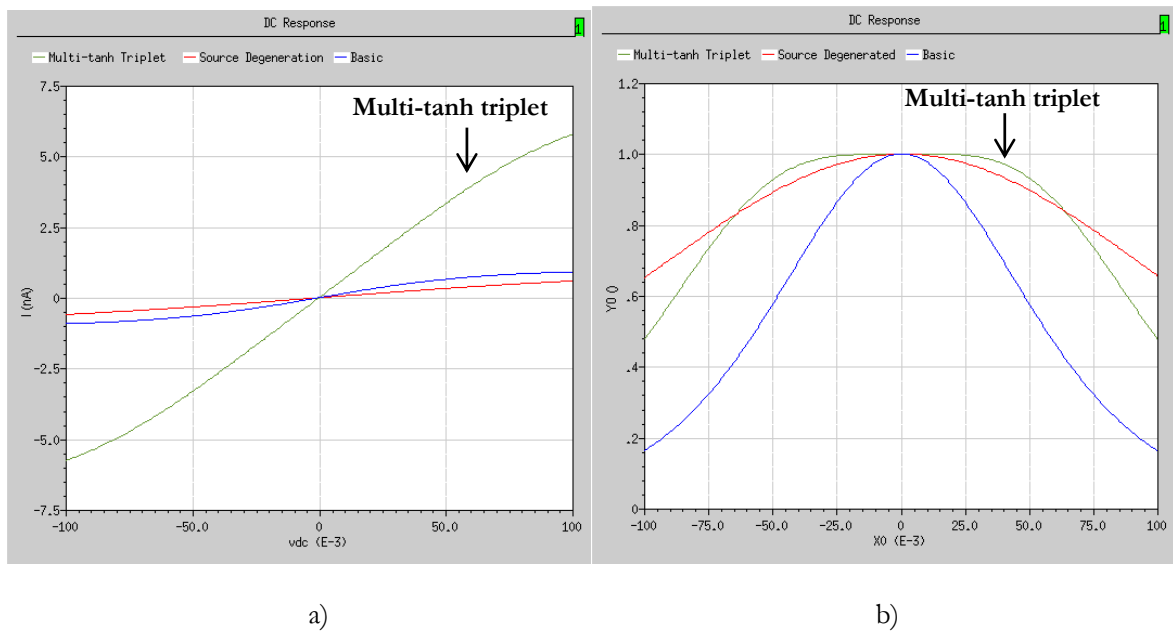
Figure 5.10: A graph comparing a) the I_O vs. V_{IN} characteristics and b) the normalised transconductance characteristics between a basic differential pair (blue), a source-degenerated differential pair (red) and the multi-tanh triplet (green).

Weak Inversion & Transistor Sizes

The next step of the transconductor design process is to tune the differential transistor width ratio, N, and the tail or bias current ratio, P, between the symmetric (width) centre pair and the two asymmetric (width) side pairs to achieve a maximally flat transconductance. Before this can be done, the standard transistor sizes for the NMOS and the PMOS must be chosen according to their region of operation. In our application, the sensor platform is designed for long-term monitoring of the patient's heart function. Therefore, the transconductor circuit must consume the minimum amount of power to extend the battery life of this monitoring platform before recharging of the battery is required. By operating the transistors in the weak-inversion region, minimal current consumption can be achieved. Furthermore, the supply voltage V_{DD} should be minimised to achieve low overall power consumption.

However, the matching of devices operating in the weak-inversion region is not as precise as devices operating in the strong-inversion region. Therefore, the sizes of these devices are required to be much larger than the transistors operating in strong-inversion to achieve good matching. Thus, the standard sizes were chosen to be 60 μm (width) by 5 μm (length) for the NMOS and 60 μm (width) by 10 μm (length) for the PMOS.

Transconductance Tuning

A parametric simulation in Cadence was conducted on the multi-tanh triplet circuit, shown in Figure 5.11 with a tail current I_{bias} of 1 nA, a common-mode voltage V_{bias} of 500 mV, and a single supply voltage V_{DD} of 1V. The result of this simulation is shown in Figure 5.12.
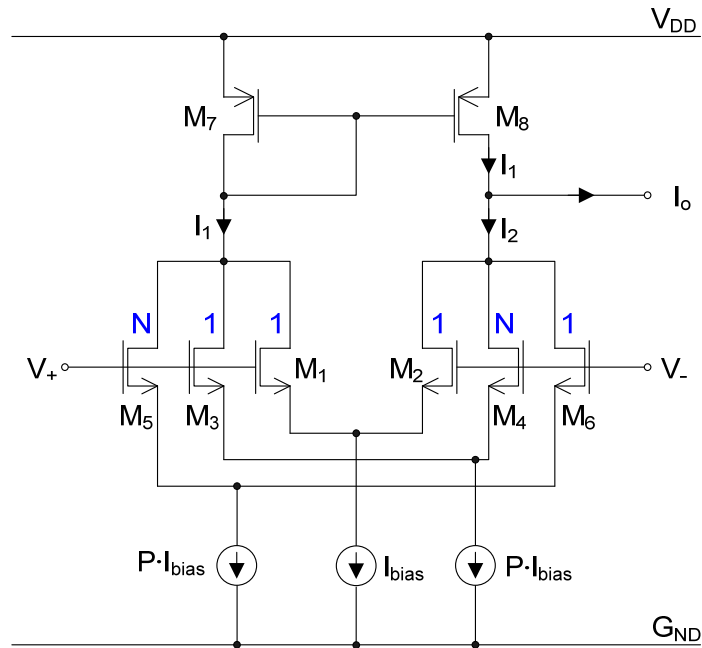
Figure 5.11: The multi-tanh triplet circuit with the width ratio, N, and tail current ratio, P, used in the transconductance tuning.

a)   b)
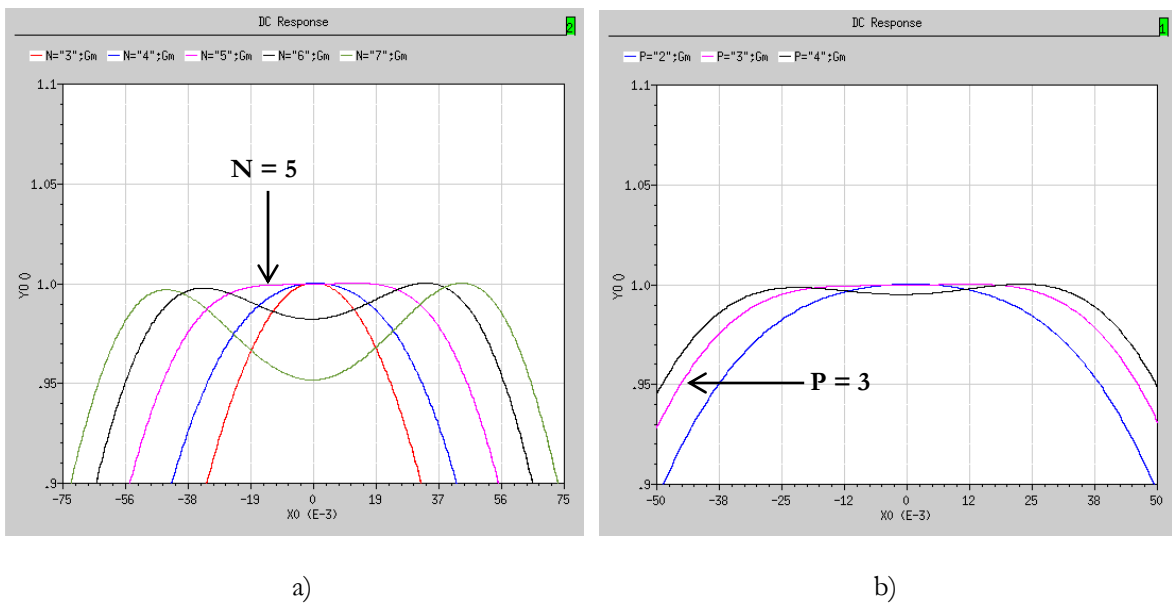
Figure 5.12: Graphs showing transconductance characteristics with a) variations in the width ratio, N, and b) variations in tail current ratio, P.

From the graphs in Figure 5.12 a) and b), we can deduce that the best transistor width ratio, N, was 5 and the tail current ratio, P, was 3. Only integer values of the ratios were considered because we have to bear in mind the layout considerations of MOS transistors in integrated circuit (IC) when optimising this transconductor.

Layout Considerations for MOS Transistors [7]

The main consideration in any design process of analogue circuits is good matching of the transistors. This is especially true when predictable and consistent reproduction of the circuit behaviour is required. One such example at a local level is a current mirror with multiple, scaled or identical output currents. Another example is where we require multiple channels of the same circuit to behave in a similar manner. The critical factor that will determine whether good matching is achieved, or not, is in the design of the layout of MOS transistors and any other circuit components, such as resistors and capacitors. In this section, we will only discuss the layout considerations for MOS transistors.

There are three main layout considerations when designing a circuit layout:

1. Geometric effects,

2. Diffusion and etching effects, and

3. Thermal and stress effects.

Geometric Effects

Geometric effects involve matching issues of MOS transistors with regards to their orientation, size and shape. Better matching results are obtained for transistors with the same orientation. This is because the etching rate is different along different axes of the silicon crystal, thus the resulting dimensions of the MOS transistors will be different for the different orientations. Additionally, due to channel length modulation MOS transistors with longer channel match better than shorter ones, since there are less fluctuation in the drain-to-source voltages. Furthermore, larger MOS transistor sizes match more closely than smaller ones because of better matching of the threshold voltages of the transistors. As discussed earlier, this matching is imperative for our circuit since the transistors are operating in the weak-inversion region.

Diffusion and Etching Effects

Etching effect needs to be considered because the etching of poly-silicon is not always uniform and will vary with the separation to other nearby poly-silicon structures. Areas with larger separation will experience a higher etching speed than areas with smaller separation. This is because the etchant ions will have more access to the sides and the bottom of the large openings. Since the outer-most MOS transistors will be exposed to these larger openings, thus dummy poly-silicon structures or gates should be introduced to ensure all MOS transistors experience nearly the same rate of etching (see Figure 5.13). Furthermore for a more precise matching, poly-silicon interconnection between the gates of MOS transistors should be avoided.
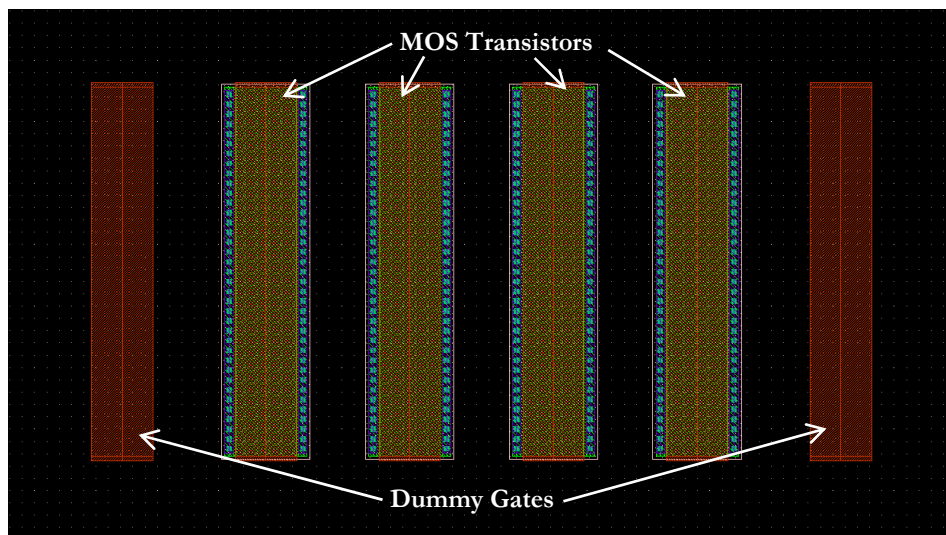
Figure 5.13: 4 MOS transistors with 2 dummy gates
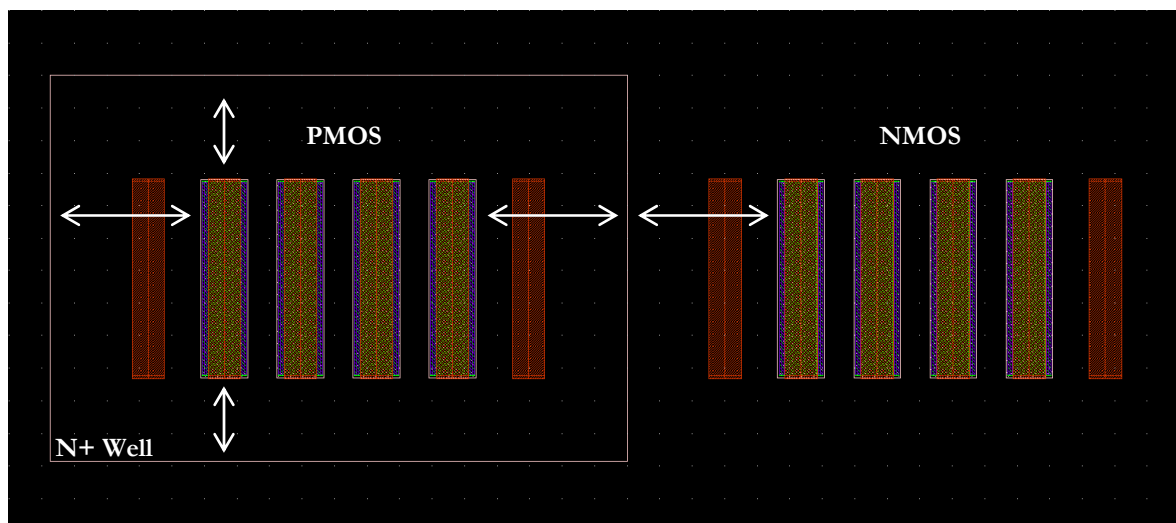
Figure 5.14: Spacing precautions of active areas to prevent deep diffusion.

Deep-diffusion effects can affect the matching of nearby MOS transistors. This could take place between the N+ well and the NMOS transistors (or P well and the PMOS transistors), where the excess dopants from the N+ well can cause a shift in the threshold voltage of the nearby NMOS transistors. Thus, to prevent any deep diffusion effect the N+ well should be placed at least 2 junction depths away from any matched NMOS transistors. This also applies to the matched PMOS transistors inside the N+ well region to prevent deep diffusion with the P well, as shown in Figure 5.14.

Thermal and Stress Effects

In an integrated circuit (IC) structure, there are mismatches that are introduced by non-uniformity, which causes thermal or stress *gradients* within the integrated circuit (IC) structure. **Stress effect** has a major impact on the carrier mobility within the active gate region of MOS transistors and the severity of this mismatch depends on the stress gradient experienced by each transistor. Thus, it is best to place the *centroid* of the matched transistors at the centre of the die where the stress is minimal. Furthermore, any metal routing over an active gate region of a MOS transistor will induce additional stress on it and should be avoided. **Thermal effect**, on the other hand, will affect the matching of the threshold voltages of the transistors, which will change by about -2mV/°C.

Common-Centroid Layout

Since there is no easy method to deal with both the stress and the thermal gradients, thus the best solution is to spread these effects evenly amongst the MOS transistors that we want to match. The technique to achieve this is called 'Common-Centroid Layout'. There are five important rules that should be followed for this design:

  a) **Coincidence**: the centroids of all matched MOS transistors should coincide.

  b) **Symmetry**: the array should be symmetric in both the X- and Y- axes about the centroid.

  c) **Dispersion**: each MOS transistor must be divided into segments and distributed uniformly over the design.

  d) **Compactness**: the design should be as small as possible to minimise gradient-induced effects and should be close to a square in shape, and

  e) **Orientation**: the matched transistors should have equal chirality.

Figure 5.15 illustrates an example of a common-centroid layout design for two matched MOS transistors M1 and M2, with each transistor divided into 2 segments.
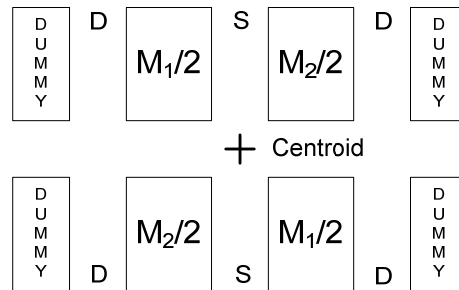
Figure 5.15: An example of a common-centroid layout design for two matched transistors M_1 and M_2.

Conclusion
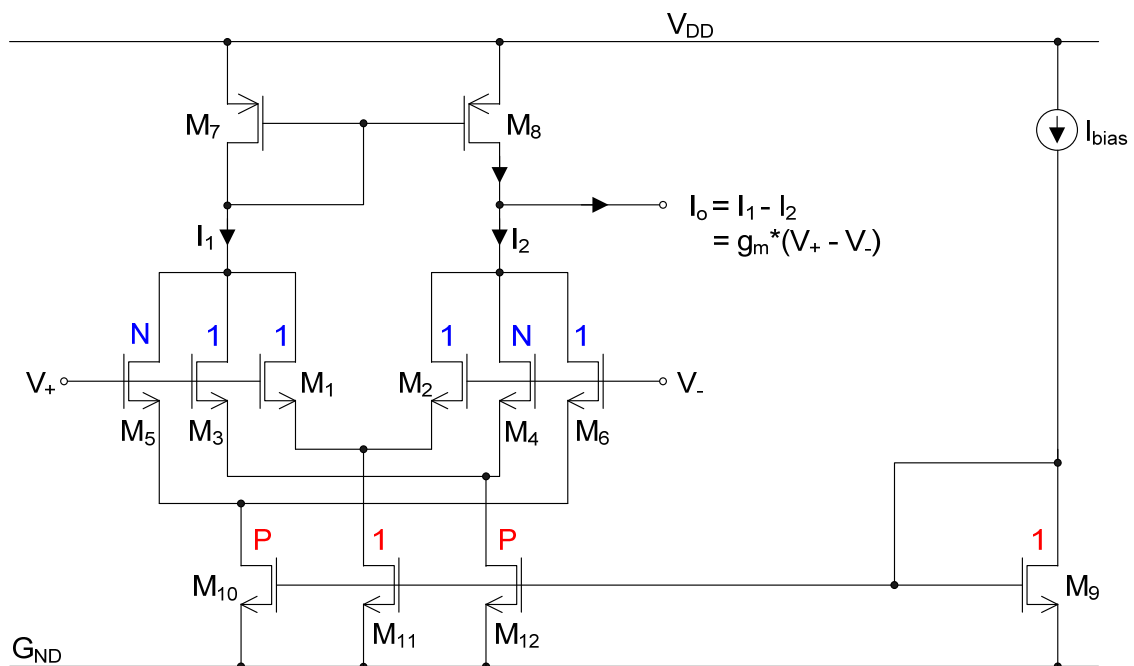
Figure 5.16: Final multi-tanh triplet transconductor circuit.

Since the common-centroid layout technique will be employed extensively in the layout design of the multi-tanh triplet transconductor, thus to obtain good matching between each differential pair's width – the asymmetric width pair of the multi-tanh triplet should be an integer multiple of the standard NMOS width, i.e. the width ratio N should be an integer. Furthermore, the three tail current sources of the Figure 5.11 can be replaced by just one control current source and a current mirror with one identical and two scaled, by the current ratio P, outputs. Thus to obtain good matching of the tail currents, the current ratio P should

also be an integer to make the width ratio of the NMOS current mirror an integer. Figure 5.16 presents the final multi-tanh triplet transconductor circuit with N = 5 and P = 3, with a standard NMOS width of 60 μm and length of 5 μm, a standard PMOS width of 60 μm and length of 10 μm, and I_{bias} = 1 nA.

5.2.1.4 Filter Synthesis

Since the design of the transconductor, with layout considerations in mind, has been completed, the next phase is to obtain the values for the capacitors and inductors from the table of normalised low-pass LC Ladder filter, and use the designed transconductor to construct the capacitively loaded gyrators and thus the Gm-C filter to our required specification. Once the inductor values are obtained, the capacitively loaded gyrators will be configured to match these values. The specifications of the Sallen-Key filter used in the recording system for the study of de-noising algorithms in Chapter 4 is shown in Table 5.1.

Table 5.1: Filter specification for the recording system

Filter Type:	Band-pass
Transfer Characteristic:	Bessel
Order:	4th
Lower cut-off frequency:	25 Hz
Upper cut-off frequency:	1 kHz

By looking up a filter synthesis book [19], we obtained that the LC Ladder Network required for the specification in Table 5.1 is as shown in Figure 5.1. The normalised component values for different source to load resistance ratio are shown in Table 5.2 and the formulas for converting the normalised values to real values are as follows [3]:

$$L_1 = \frac{R_L L_{N1}}{2\pi B} \tag{5.10}$$

$$C_1 = \frac{B}{2\pi f_0^2 C_{N1} R_L} \tag{5.11}$$

$$L_2 = \frac{R_L B}{2\pi f_0^2 L_{N2}} \tag{5.12}$$

$$C_2 = \frac{C_{N2}}{2\pi R_L B} \tag{5.13}$$

$$f_0 = \sqrt{f_1 \cdot f_2} \tag{5.14}$$

$$B = f_2 - f_1 \tag{5.15}$$

where, f_1 and f_2 are the lower and the upper cut-off frequencies, respectively. And B is the bandwidth of the filter.

Table 5.2: Normalised component values for 4th order Bessel band-pass filter

n	R_L/R_S	L_{N1} or C_{N1}	C_{N2} or L_{N2}
	1.0000	0.5755	2.1478
	1.1111	0.5084	2.3097
	1.2500	0.4433	2.5096
	1.4286	0.3801	2.7638
	1.6667	0.3191	3.0993
2	2.0000	0.2601	3.5649
	2.5000	0.2032	4.2577
	3.3333	0.1486	5.4050
	5.0000	0.0965	7.6876
	10.0000	0.0469	14.5097
	Inf	1.3617	0.4539

Capacitance Ratio in Integrated Circuit (IC)

For capacitors in integrated circuit (IC), there are three important points to consider. First is the value of the capacitance. The larger the capacitance, the larger the area required for that capacitor and as a rule of thumb: 10 μm x 10 μm poly-silicon capacitor have a capacitance of 89.44 fF. The second point is to minimise the ratio between the largest and the smallest capacitances, ideally this should not be greater than 10. The third point is the layout of the integrated poly-silicon capacitors and the techniques to achieve good matching between them.

By inspecting equations 5.11 and 5.13 for C_1 and C_2, it can be seen that the value of the two capacitances can be kept small by having a large load resistance, R_L. Also, the largest to smallest capacitance ratio can be obtained from the ratio of C_1 and C_2:

$$\frac{C_1}{C_2} = \frac{B^2}{f_0^2 C_{N1} C_{N2}} \tag{5.16}$$

We can see that the ratio is dependent on the lower and upper cut-off frequencies, f_1 and f_2 respectively. Equation 5.16 can be further simplified by saying that:

$$f_2 = (N+1) \cdot f_1 \tag{5.17}$$

Thus, equations 5.14, 5.15 and 5.16 become:

$$f_0 = \sqrt{(N+1) \cdot f_1^2} \tag{5.18}$$

$$B = N \cdot f_1 \tag{5.19}$$

$$\frac{C_1}{C_2} = \frac{N^2}{(N+1)C_{N1}C_{N2}} \approx \frac{N}{C_{N1}C_{N2}}, \text{ for large } N \tag{5.20}$$

Therefore, the capacitance ratio can be minimised by decreasing the value of N – the relative bandwidth or by finding a load to source resistance ratio (R_L/R_S) with the largest $C_{N1} \cdot C_{N2}$ value. Table 5.3 shows the variation of the inverse of $C_{N1} \cdot C_{N2}$ with the load to source resistance ratio.

Table 5.3: The largest to smallest capacitance ratio for different source to load resistance ratios

R_L/R_S	L_{N1} or C_{N1}	C_{N2} or L_{N2}	$1/C_{N1}C_{N2}$
1.0000	**0.5755**	**2.1478**	**0.8090**
1.1111	0.5084	2.3097	0.8516
1.2500	0.4433	2.5096	0.8989
1.4286	0.3801	2.7638	0.9519
1.6667	0.3191	3.0993	1.0111
2.0000	0.2601	3.5649	1.0785
2.5000	0.2032	4.2577	1.1558
3.3333	0.1486	5.4050	1.2450
5.0000	0.0965	7.6876	1.3480
10.0000	0.0469	14.5097	1.4695
Inf	1.3617	0.4539	1.6179

From Table 5.3, the best load to source resistance ratio (R_L/R_S) that minimises the largest to smallest capacitance ratio is 1. Thus, the largest to smallest capacitance ratio for f_1 = 25 Hz and f_2 = 1 kHz with the load to source resistance ratio (R_L/R_S) of 1 is 30.76. This is very high. Since the lower cut-off frequency, f_1, of the filter has to be kept at 25 Hz due to the nature of the heart sound, therefore the only way to reduce the largest to smallest capacitance ratio further is to reduce the relative bandwidth of the band-pass filter, N.

Layout Considerations for Integrated Capacitors

Before we can go on to alter the bandwidth of the band-pass filter, we must examine the layout techniques necessary to obtain good matching of the integrated poly-poly capacitors. If we imagine that the largest to smallest capacitance ratio is an integer, then it is possible for us to construct the largest capacitor by connecting many of the smallest capacitors in parallel. This is the norm in layout to achieve good matching of integrated poly-poly capacitors [7]. The layout considerations for integrated poly-poly capacitors are very much the same to those of MOS transistors. Thus when laying out these capacitors on an integrated circuit (IC), they would be arranged preferably in a square matched capacitor array grid, to minimise any gradient-induced effects. Furthermore to reduce the variation in the etching, dummy capacitors are used to surround the real capacitors and to shield the real capacitors from stray electrostatic fields (shown in Figure 5.17).
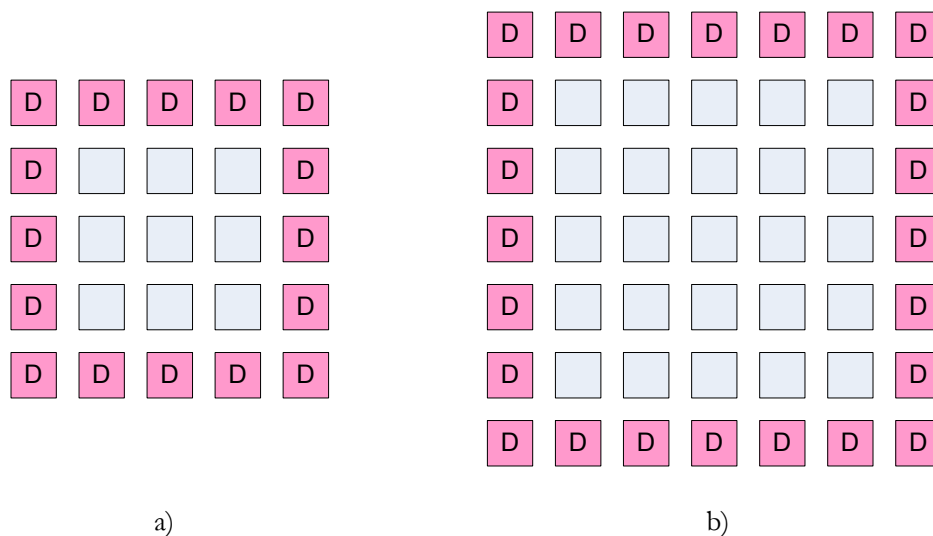
Figure 5.17: Examples of integrated capacitor grids with dummy (D) capacitors a) 3 x 3 and b) 5 x 5.

Thus for a square grid of capacitors, the largest to smallest capacitance ratio can range from $2^2-1 = $ **3**, $3^2-1 = $ **8**, $4^2-1 = $ **15**, or $5^2-1 = $ **24** for $f_2 < 1$ kHz. These ratios correspond to bandwidths, B, (and upper cut-off frequencies, f_2) of approximately 113 (138) Hz, 270 (295) Hz, 487 (512) Hz and 766 (791) Hz, respectively. The best compromise between maximising the bandwidth, minimising the largest to smallest capacitance ratio, and the capacitance grid size is the 5 by 5 grid i.e. largest to smallest capacitance ratio = 24 and N = 30.63.

We now have a new set of specification for the filter, what remains is for us to set the value for the load resistance, R_L, to minimise the capacitance values and calculate the inductance values that the capacitively loaded gyrators have to emulate. However, care is required in selecting the load resistance, R_L, value because even though the capacitance values are inversely proportional to R_L but the inductance values are directly proportional to R_L.

5.2.1.5 Filter Simulation

Since the capacitively loaded gyrators are not ideal inductors, so their behaviour is likely to be restricted by the limitations of the analog circuitry. Therefore, it was decided to try a number of load resistance, R_L, values and compare the simulation results in terms of the cut-off frequencies and the bandwidth, with the ideal filter. The load resistance, R_L, values chosen were 14.5 MΩ and 25 MΩ. The capacitance and inductance values required for each load resistance value are shown in Table 5.4.

Table 5.4: The capacitance and inductance values for load resistance values of 14.5 MΩ and 25 MΩ

$R_S = R_L$	14.5 MΩ	25 MΩ
C_1	738.8 pF	428.5 pF
C_2	30.78 pF	17.85 pF
L_1	1,734 H	2,990 H
L_2	41,620 H	71,759 H

Capacitively Loaded Gyrator Tuning

The inductance values shown in Table 5.4 are not practical as real components. However, these inductor values can be implemented using capacitively loaded gyrators because the simulated values are made up by the ratio between the capacitance values and the product of the transconductances of the two transconductors, as presented in equation 5.7. Thus, this is a further advantage of using active inductors for constructing filters on integrated circuit (IC), where only small capacitors are used.

To properly tune the capacitively loaded gyrator to the required value of inductance, there are two main matters that must be considered. This is because there are three main elements in

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this active inductor structure (shown in Figure 5.5) – a feed-forward transconductor g_{m1}, a capacitor C, and a feedback transconductor(s) g_{m2}. The first question is what value should we choose for the capacitor C and the second is how should we split the product of the transconductances between the two transconductors g_{m1} and g_{m2}.

The answer to the first question was approached by firstly having C equal to C_2, the smallest between C_1 and C_2. Furthermore, any subsequent (larger) values of C must be a multiple of C_2 to comply with the layout consideration for integrated capacitors. The answer to the second question was approached via simulation, by looking at how the transconductance of the feed-forward transconductor, which is controlled by its tail current I_{bias}, affects the DC voltage of the capacitor and the linearity of the capacitance voltage swing. The DC voltage of the capacitor is important because we need to set the voltage bias V_{bias} for the feedback transconductor(s) to this DC level. Ideally, the voltage bias V_{bias} for both the feed-forward and the feedback transconductors should be the same, as shown in Figure 5.5. Furthermore, the linearity of the capacitance voltage swing will affect how well the capacitively loaded gyrator simulates an actual inductor over the interested frequency range. If the transconductance of the feed-forward transconductor is too high, this can cause a slight distortion or even saturation in the capacitor's voltage swing. Thus, the tail current of the feed-forward transconductor, which controls its transconductance, should be fixed at a low value to maximise the linearity of the capacitively loaded gyrator.

Figure 5.18 shows the capacitively loaded gyrator circuit in a grounded inductor configuration (shown as a block) that was used for tuning the inductance. The tuning was done by performing AC analyses on the circuit with different capacitor values and tail currents of the feed-forward I_1 and feedback transconductors I_2, when the voltage bias V_{bias} was set to 0.5V. Figure 5.19 presents the inductance AC characteristics obtained from the capacitively loaded gyrator designed to match as closely as possible to the inductance values given in Table 5.4.

For the relatively smaller values (10^3 H) of inductance, the capacitively loaded gyrators can simulate their inductance well over the majority of the interested frequencies. However, for the larger values (10^4 H) of inductance, the value of the simulated inductance varies greatly over the pass-band with very high peaks of over ten million Henry. Table 5.5 presents the value of the capacitor C and the tail currents of the feed-forward transconductor I_1 and feedback transconductor I_2 used in Figure 5.19, and the value of the simulated inductance value obtained at 150 Hz in each case.
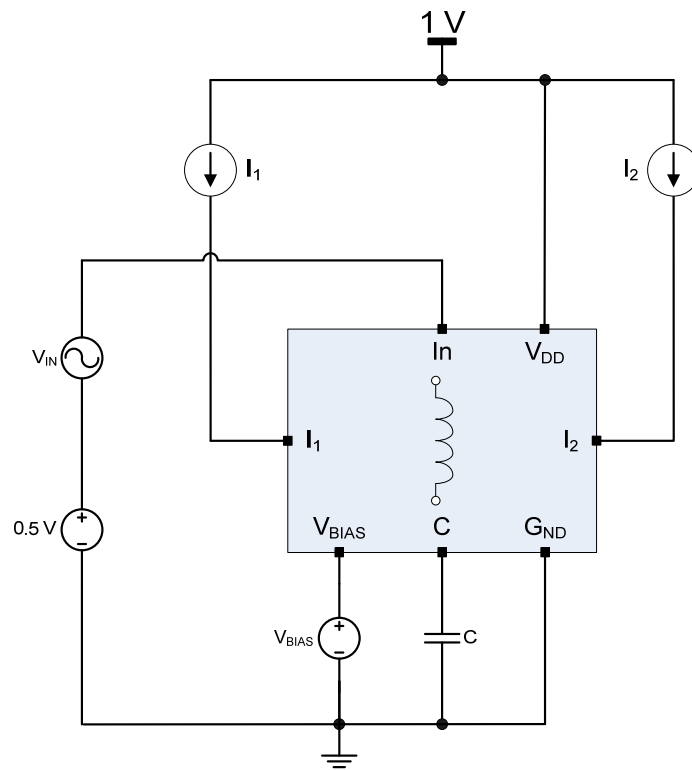
Figure 5.18: Capacitively loaded gyrator circuit used for the AC analyses to tune its inductance values.
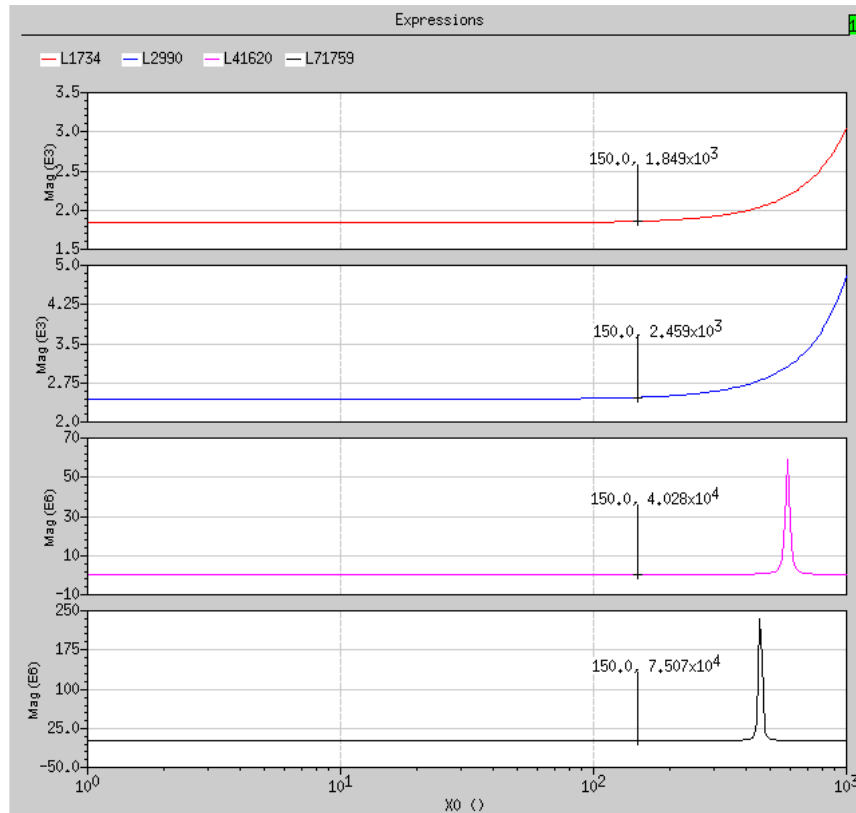
Figure 5.19: Inductance characteristics of the four differently tuned capacitively loaded gyrators.

Table 5.5: The values of the capacitor C and the tail currents of the feed-forward I_1 and feedback transconductors I_2 used for approximately simulate the inductance values in Table 5.4

Actual L	1,734 H	2,990 H	41,620 H	71,759 H
C	30.8 pF	17.9 pF	184.8 pF	304.3 pF
I_1	1 nA	1 nA	1 nA	1 nA
I_2	4 nA	1.5 nA	1 nA	1 nA
Simulated L @ 150 Hz	1,849 H	2,459 H	40,280 H	75,070 H

AC Analysis of the Filter

Since we now have all the parameters for the capacitively loaded gyrator to simulate the inductance values required by the LC ladder filter design for the two load resistance, R_L, values, given in Table 5.4, the overall frequency response of the two Gm-C filters can now be simulated and compared with its ideal passive version. Figure 5.20 shows the overall circuit diagram of the Gm-C filter that was use in the AC analysis to obtain the overall frequency responses. Figure 5.21 compares the frequency response of the ideal passive LC ladder filter with the Gm-C filter, for two different load resistances R_L of 14.5 MΩ and 25 MΩ.

As expected, both the ideal passive LC ladder filters have the same frequency response. This is the black line in Figure 5.21. However, the two Gm-C filters behave slightly differently from the ideal filter response. At the lower cut-off frequency, both the Gm-C filters and the ideal passive filters have an almost identical response. However at the high frequency end of the pass-band, the higher cut-off frequency of the Gm-C filters are lower than the ideal case and exhibit a higher roll-off than expected. The shifts in the cut-off frequencies are suspected to be caused by the inductance characteristics of the capacitively loaded gyrator, which does not produce a stable inductance over the pass-band frequency range.

This variation in the inductance value is especially strong for the higher inductance values (10^4 H). Furthermore, the scale and the location of the occurrence of this variation appears to increase and shift to a lower frequency with the increasing size of the inductance values, which could help explain why the roll-off of the Gm-C filters are higher than expected and also why higher cut-off frequency of the Gm-C filter with R_L = 25 MΩ is less than the Gm-C filter with R_L = 14.5 MΩ. Thus, overall the Gm-C filter with a load resistance R_L = 14.5 MΩ matches

more closely with the designed specifications. Table 5.6 compares the designed filter specifications with the filter parameters of the simulated Gm-C filters with a load resistance R_L = 14.5 MΩ and 25 MΩ.
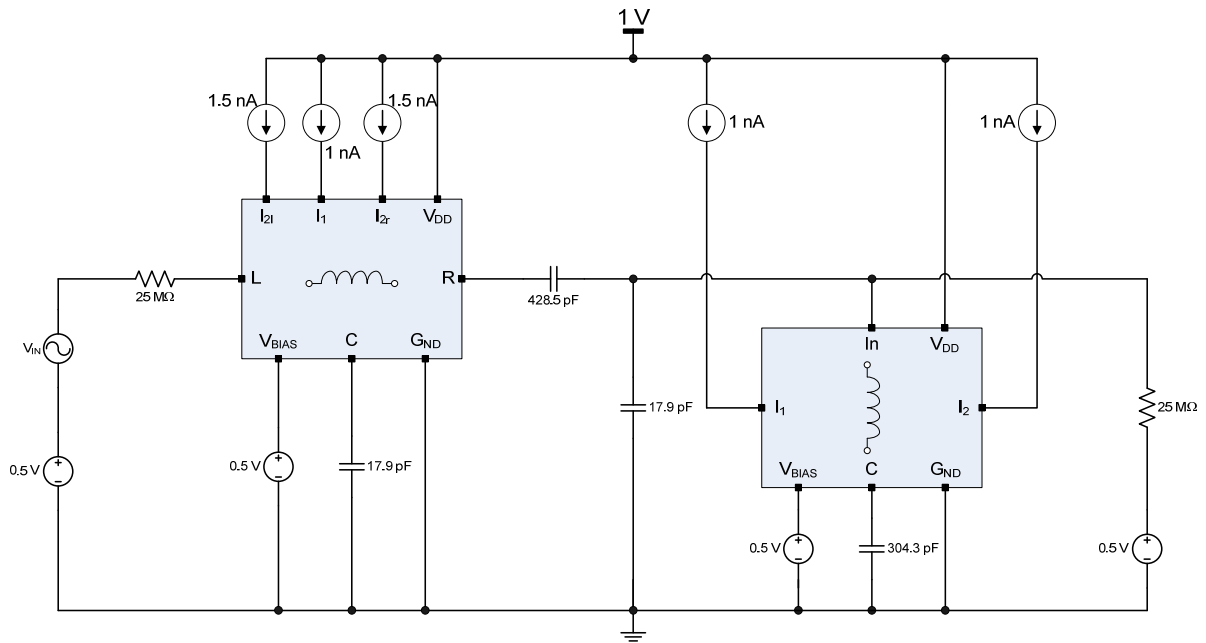
Figure 5.20: The overall circuit diagram of the Gm-C filter with R_L = 25 MΩ.
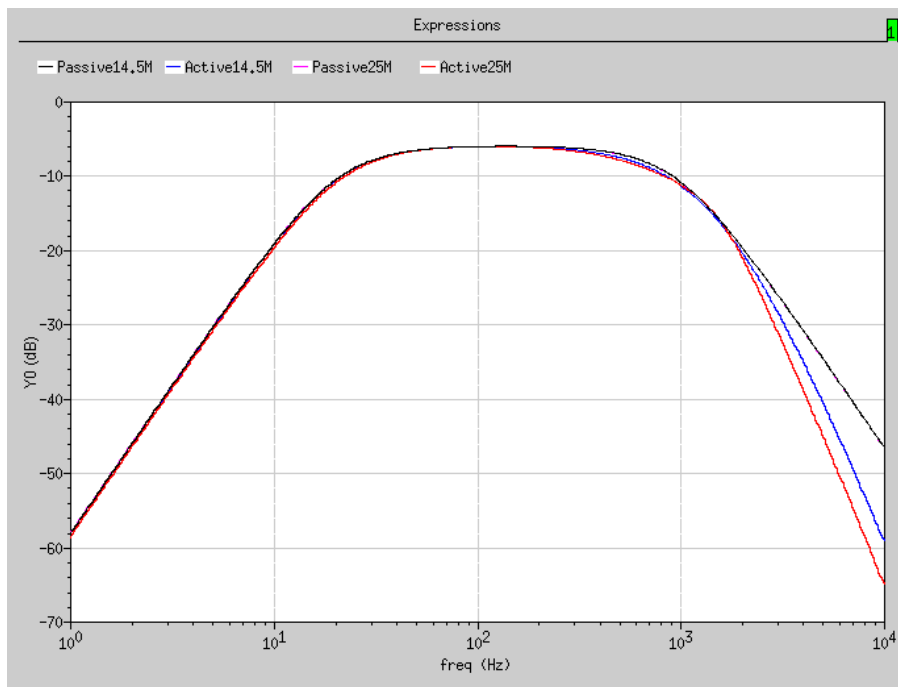
Figure 5.21: The frequency response comparison between an ideal passive LC ladder filter (black) and its Gm-C variant, with R_L = 14.5 MΩ (blue) and R_L = 25 MΩ (red).

Table 5.6: A table comparing the designed filter specification with the simulated filter parameters of the simulated Gm-C filters with a load resistance $R_L = 14.5$ MΩ and 25 MΩ

	Lower Cut-off	Upper Cut-off	Bandwidth
Ideal passive filter	**25.12**	**786.6**	**762**
Gm-C with $R_L = 14.5$ MΩ	25.57	722.7	697
Gm-C with $R_L = 25$ MΩ	26.65	679.9	653

Monte Carlo Simulation

Once the circuit that can produce the frequency response to meet the desired specification has been obtained, the circuit's robustness has to be tested. This was achieved by completing a Monte Carlo simulation of the AC analysis, using the manufacturer's specified variation for process and mismatch, on the designed filters to observe how their frequency response will be affected by any process variations and mismatches of the MOS transistors and passive components. Figure 5.22 presents the results of the Monte Carlo simulation for 500 runs of the Gm-C filters with $R_L = 14.5$ MΩ and 25 MΩ.
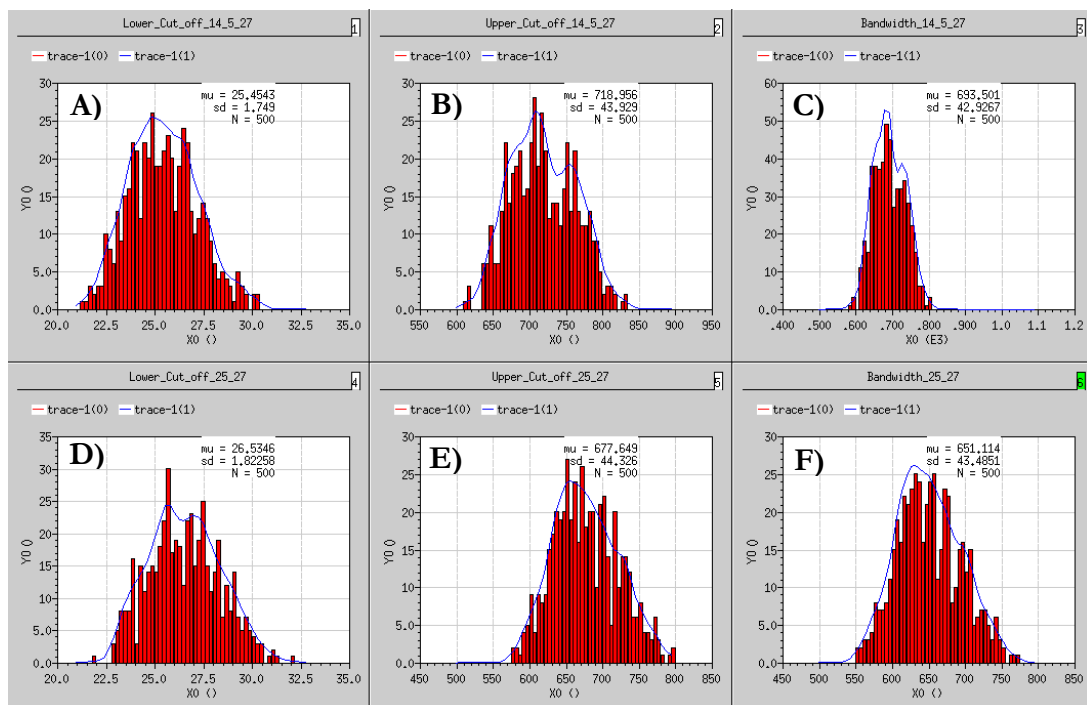
Figure 5.22: The Monte Carlo simulation results for 500 different runs of the circuit. The results show the histogram of a) the lower and b) upper cut-off frequencies, and c) the bandwidth of the Gm-C filter with $R_L = 14.5$ MΩ. The same is shown for the Gm-C filter with $R_L = 25$ MΩ in d), e) and f).

Statistically, both Gm-C filters with R_L = 14.5 MΩ and 25 MΩ have very similar standard deviations in the distribution of the lower cut-off frequency (σ ≈ 2 Hz), at about 25 Hz and 26 Hz, the upper cut-off frequency (σ ≈ 40 Hz), at about 719 Hz and 678 Hz, and the bandwidth (σ ≈ 40 Hz), at 694 Hz and 651 Hz respectively. Assuming that the variation roughly follows the normal distribution, 65% of the runs will exhibit less than ±10% variation in the lower cut-off frequency, the upper cut-off frequency and the bandwidth from the mean value. However, the Gm-C filter with a load resistance R_L = 14.5 MΩ has a frequency response characteristics closer to the desired in terms of the lower cut-off frequency, the upper cut-off frequency and the bandwidth.

Dynamic Range

To complete the design process, we need to work out the dynamic range of the designed filters. This was done by conducting a total harmonic distortion (THD) analysis and a noise analysis of the two Gm-C filters. The expression of the dynamic range of a circuit for a stated percentage of total harmonic distortion (THD) and input frequency is given by:

$$\text{Dynamic Range @ n\% THD} = 20 \cdot \log_{10}\left(\frac{\text{maximum input amplitude @ n\% THD}}{\text{input referred noise in V}/\sqrt{\text{Hz}}}\right)$$

Since the designed filter will be specifically applied to audio signals, thus it would be beneficial to keep the total harmonic distortion (THD) below 1% inside the pass-band. The maximum input amplitudes of the two filters for 1% THD were obtained using a transient analysis. The noise analysis was also conducted on both Gm-C filters to acquire their input referred noise over the pass-band frequencies. The values of both the maximum input amplitude and the input referred noise as well as the resulting dynamic range at 1% THD is given in Table 5.7.

Table 5.7: The maximum input amplitude, the input referred noise, and the resulting dynamic range at 1% THD is presented for Gm-C filters with R_L = 14.5 MΩ and 25 MΩ

R_L	14.5 MΩ	25 MΩ
Maximum Input Amplitude @ 1% THD	137.5 mV	131.9 mV
Input Referred Noise (mV/$\sqrt{\text{Hz}}$)	0.1034	0.1172
Dynamic Range @ 1% THD (dB)	62.11	62.02

The dynamic range at 1% THD of the two Gm-C filters are virtually the same and is unlikely to affect the final design decision. However, it should be noted that the Gm-C filter with R_L = 14.5 MΩ performs better than the alternative design in all areas, with a higher maximum input amplitude, a lower input referred noise, and a higher dynamic range @ 1% THD.

Overall Power Consumption

The last simulation conducted was to determine the quiescent DC current consumption of the two Gm-C filters. This is achieved by running a DC analysis and saving the DC operating point of the two filters. Table 5.8 presents the current consumptions of the simulated floating inductor, the simulated grounded inductor and the overall Gm-C filter, and also the overall power consumption of the Gm-C filter for both Gm-C filters.

Table 5.8: The current consumption of the simulated floating inductor, the simulated grounded inductor and the overall Gm-C filter, and also the overall power consumption of the Gm-C filter with a load resistances of R_L = 14.5 MΩ and 25 MΩ

	R_L	14.5 MΩ	25 MΩ
	Simulated Floating Inductor	79.52 nA	39.92 nA
Current Consumption	Simulated Grounded Inductor	15.99 nA	15.99 nA
	Overall Gm-C filter	95.58 nA	55.92 nA
Power Consumption	Overall Gm-C filter (1V supply)	95.58 nW	55.92 nW

Thus for a typical Li-Ion coin cell (CR2320) which can supply approximately 110 mAh at 3 V (1188 W in total), the battery life of the cell will be more than one million hours for the operation of the 2-channel Gm-C filter.

5.2.1.6 Conclusion

The rationale of the analogue circuit design and the simulation design has been presented. We have successfully obtained a design of the element substitution analogue circuit, or more specifically a Gm-C filter implementation, of the passive LC ladder filter, which exhibit the best sensitivity performance to tolerances of the component values in the pass-band compared to other filter topologies.

The simulation of the passive ladder filter is achieved via replacing real inductors with capacitively loaded gyrators, which is formed using at least two transconductors and a capacitor. The multi-tanh triplet was used to maximise the linear range of the transconductors and the flatness of the transconductance. This is to maintain low signal distortions, necessary for audio applications.

Two Gm-C filter designs, with the same specification, have been presented. The two designs use a different value of the load resistance R_L (14.5 MΩ and 25 MΩ) because the value of the load resistance affects the size of the capacitors required, with larger R_L giving smaller capacitors. However from the various simulation results, it is apparent that the Gm-C filter with a lower load resistance $R_L = 14.5$ MΩ out-performs the Gm-C filter with a higher load resistance, in terms of the lower cut-off frequency, the upper cut-off frequency, the bandwidth, as well as the dynamic range at 1% THD. The difference in performance is believed to be associated with the unstable inductance characteristics, especially at $L > 10^4$ H, where many orders of magnitude variation can be observed in the pass-band. Thus, the Gm-C filter with a load resistance $R_L = 14.5$ MΩ was preferred as the circuit to perform the filtering operation in the signal acquisition chain

However, the smallest capacitors required for this Gm-C filter is 30.8 pF. This equates to approximately 190 µm x 190 µm poly-poly capacitor. Since the largest to smallest capacitor ratio worked out in Section 5.2.1.4 is 24, thus the approximate total dimension to construct one smallest and one largest capacitor using a 5 x 5 matched capacitor array grid is 1000 µm x 1000 µm or 1 mm x 1 mm, without dummy capacitors. Furthermore the sensor platform being developed is a two channel device, therefore two of these matched capacitor array grids are required. The integrated circuit (IC) area required to construct these capacitors proved to be too large to be fitted on the die design that was sent for fabrication (area shared with another PhD student). Thus, discrete capacitors will be used instead of integrated capacitors to test the performance of the fabricated Gm-C filters.

5.2.1.7 Layout Design

The overall layout design of the Gm-C filter was split into 3 main parts, where the MOS transistor matching of each part is vital.

The first part concentrates on the matching of the width ratio of the three differential pairs in the multi-tanh triplet and the NMOS current mirrors which determine the tail currents for each differential pair. This is crucial for ensuring that all the transconductors will behave in a

similar manner. Figure 5.23 compares the multi-tanh triplet transconductor circuit with its layout design.
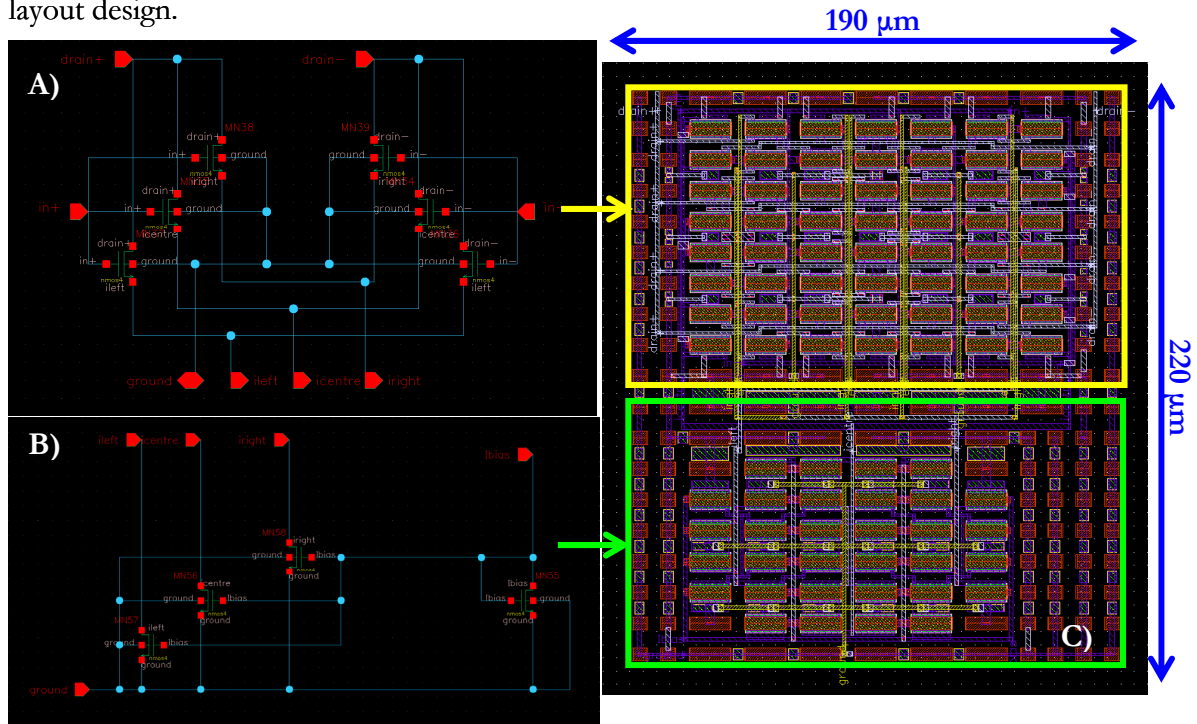
Figure 5.23: The circuit diagrams of a) the multi-tanh triplet differential pairs, b) the NMOS current mirrors and c) their layout design.
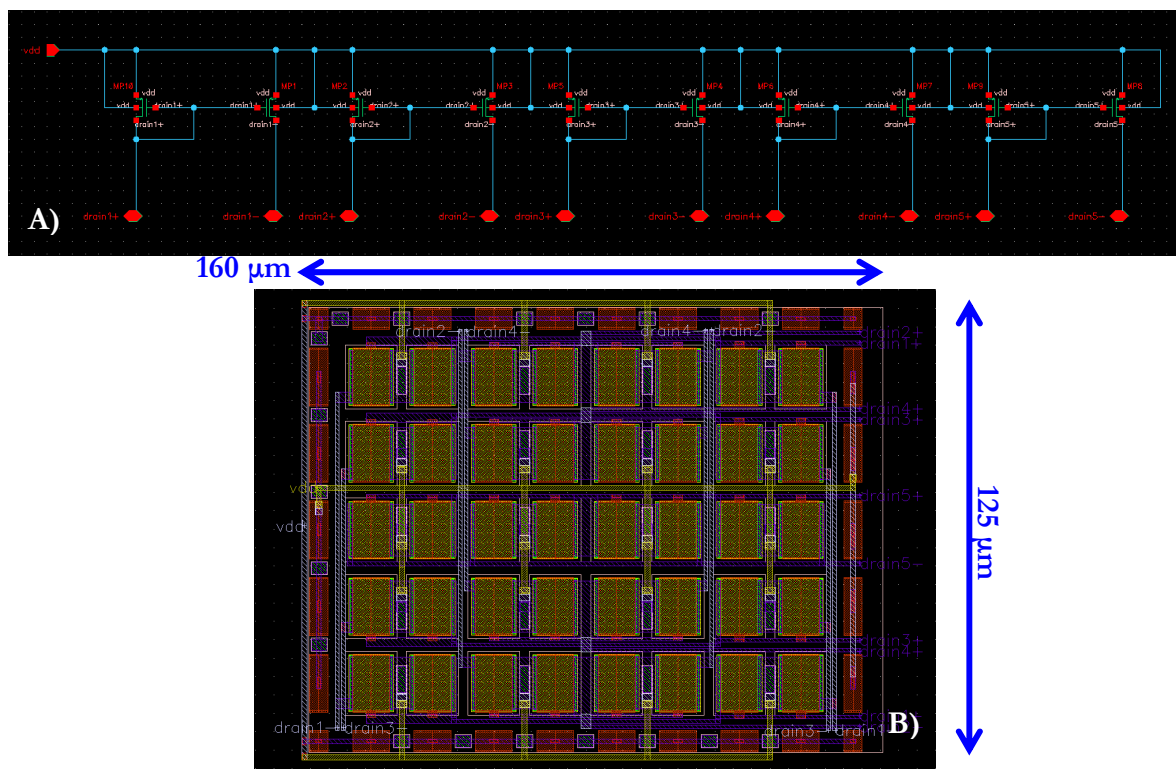
Figure 5.24: a) The circuit diagram of the PMOS current mirrors and b) its layout design.

The second part involves the matching of all the PMOS current mirrors for the five transconductors used in each Gm-C filter. The author believes that by grouping these PMOS transistors together, this will help minimise any deep diffusion effects from occurring by keeping the N+ well of the PMOS transistors away from the matched NMOS transistors. Figure 5.24 illustrates the circuit diagram of the 5 PMOS current mirrors and its layout design.

The third and last part was related to another PMOS current mirror circuit developed for controlling the tail currents of the five transconductors that were used for the Gm-C filter. This circuit is a single current mirror with five outputs, three with identical outputs and two with scaled (multiply by 4) outputs. This is to reduce the number of current sources that the filter requires to one per channel. Figure 5.25 shows the circuit diagram of the PMOS current mirror used for controlling the tail currents of the five transconductors of the Gm-C filter and its layout design.
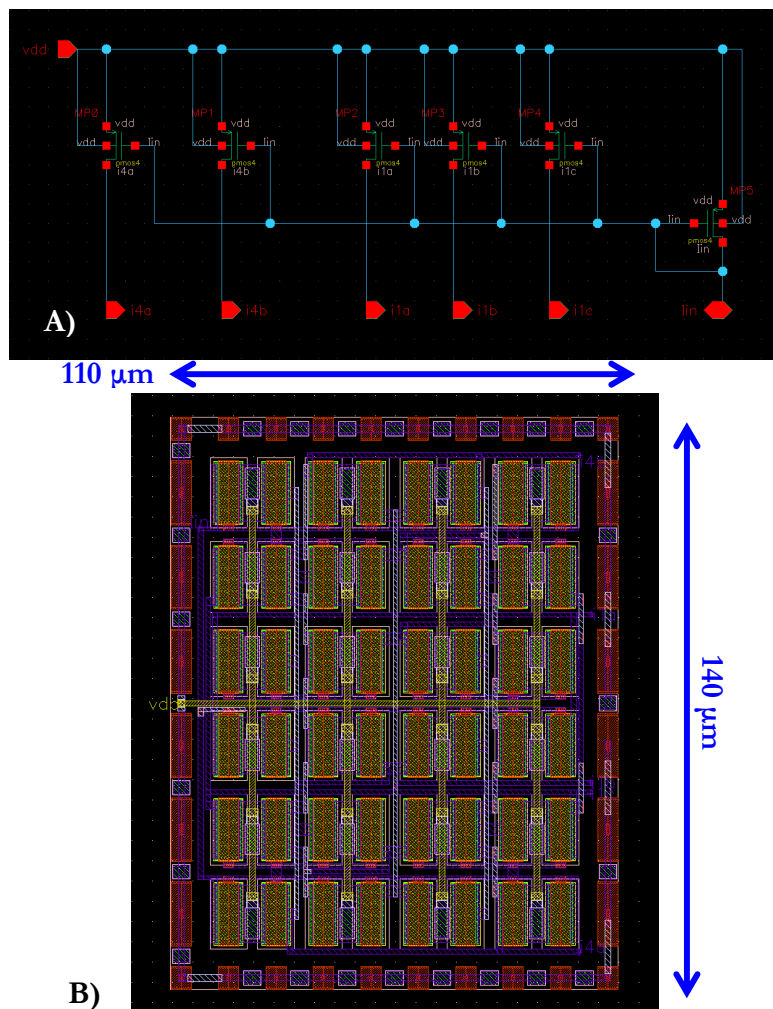
Figure 5.25: a) The circuit diagram of the PMOS current mirror used for controlling the tail currents of the five transconductors of the Gm-C filter and b) its layout design.

Lastly, Figure 5.26 presents the overall layout of the 2-channel filtering stage in the signal acquisition chain of the proposed sensor platform.
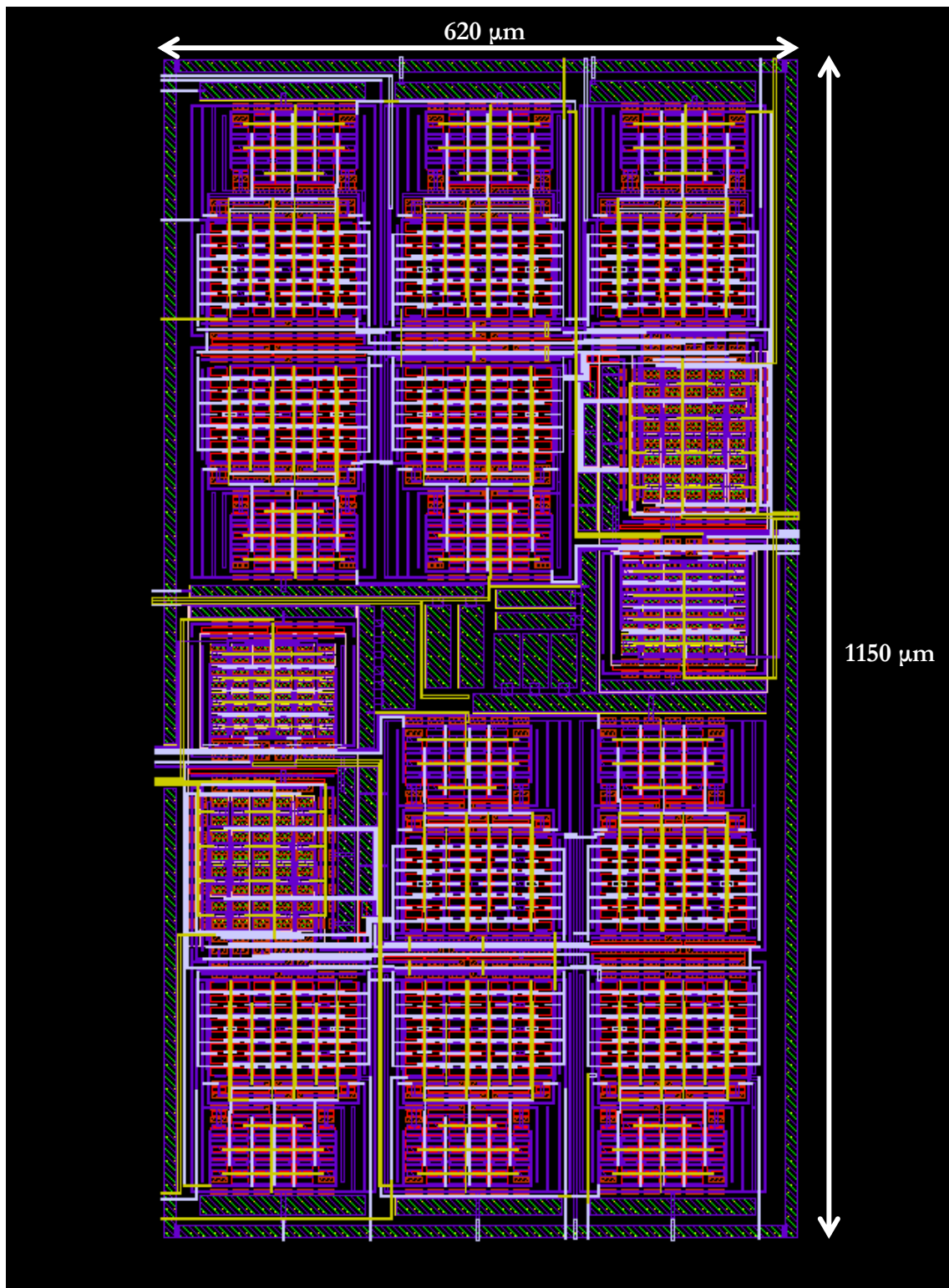
Figure 5.26: The overall layout design of the 2-channel filtering stage in the signal acquisition chain of the proposed sensor platform.

5.2.2 Integrated Circuit (IC) Testing & Results

The layout design of the 2-channel Gm-C filter presented in Figure 5.26 was sent out for fabrication on the Austria Micro Systems 0.35 μm CMOS C35B4C3 3.3V 2P/4M technology at Europractice IC Service. The integrated circuit (IC) was packaged in a 100-pin ceramic pin grid array, PGA100. The testing was conducted on a special PCB test-board that was designed by the Bio-inspired VLSI Group, Department of Bioengineering, Imperial College London.

The capacitors and the resistors required to complete the Gm-C filter circuit was manually soldered on the under-side of the test-board. The connections on the top side and to other external test equipments were made using SMA connectors and cables. The test equipments used in the testing of the fabricated integrated circuit includes:

1. Standard voltage sources,

2. Current Sources – Keithley 6220 DC Precision Current Source and Keithley 6221 AC and DC Current Source,

3. Oscilloscope – LeCroy WavePro, and

4. Signal Analyser – Stanford Research Systems SR785 Dynamic Signal Analyzer.

Further to the test equipments stated above, two voltage followers were used to read-out the filters' output voltages. This is because the output or load resistance of the two doubly terminated Gm-C filters are very high (14.5 MΩ) compared to the input resistance of the LeCroy WavePro (or oscilloscope) and Stanford Research Systems SR785 Dynamic Signal Analyzer (or signal analyser) – stated as 1 MΩ for both the oscilloscope and the signal analyser. These voltage followers were constructed from operational amplifiers (Op-Amp) made by Linear Technology, LTC1152, with the output of the filter connected to the +ve input pin of the Op-Amp and the –ve input pin of the Op-Amp connected to its output pin. The Op-Amp was powered using a 3.3 V single-supply. Figure 5.27 illustrates the circuit diagram showing the connections of the voltage follower constructed from the Linear Technology LTC1152 Op-Amp. Figure 5.28 shows the picture of the overall integrated circuit (IC) test set-up with the PCB test-board, the integrated circuit (IC) in PGA100 package and the purpose-built voltage followers on a breadboard.
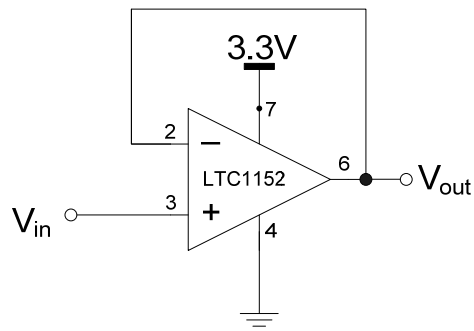
Figure 5.27: The circuit diagram of the voltage follower constructed from the Linear Technology LTC1152 Op-Amp.
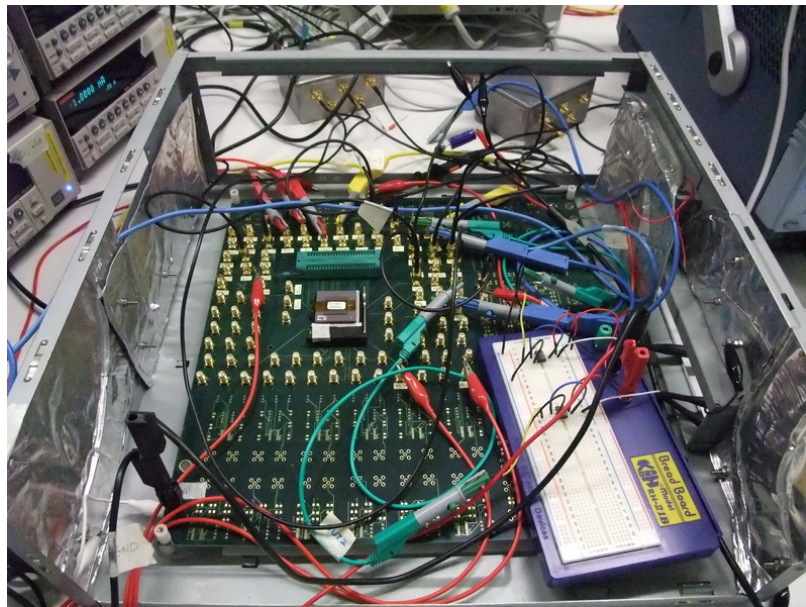
Figure 5.28: A picture of the overall integrated circuit (IC) test set-up.

The integrated circuit (IC) testing presented in this section will concentrate on the testing of the linearity, the inter-modulation distortion, and the frequency response of the Gm-C filters in the fabricated ICs. The bias current of the two Gm-C filters I_{IN1} and I_{IN2} was set at -1 nA, the bias voltage of the transconductors V_{bias} was set at 0.5 V, and the supply voltage V_{DD} was set at 1V.

5.2.2.1 Linearity

The linearity of the fabricated Gm-C filters were determined by examining the magnitude of the 2nd harmonic distortion (HD_2) in the frequency or the Fourier domain at the output, after the buffer or voltage follower stage. This test was conducted for the input amplitude range between 20 mV to 180 mV at a number of different frequencies (30, 100, 300 and 400 Hz)
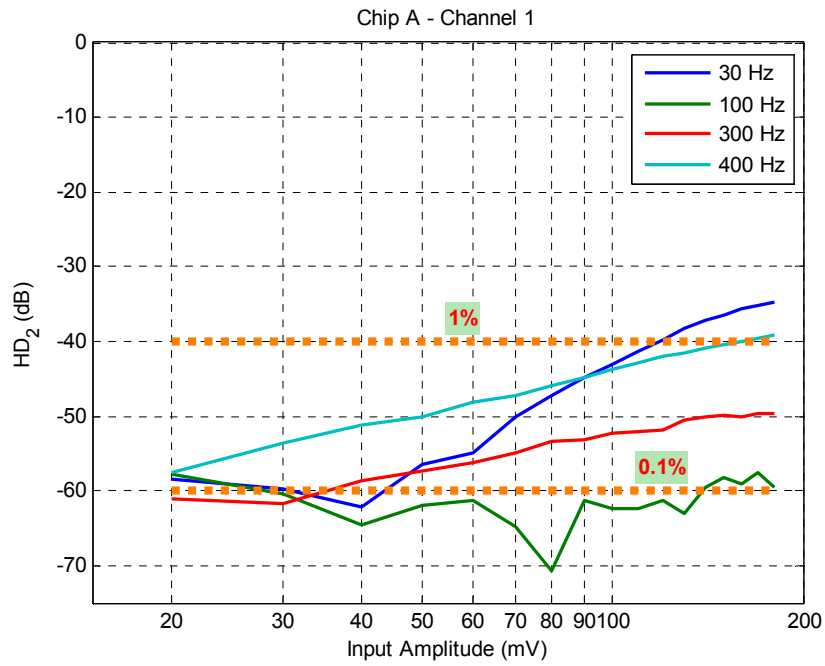
a)
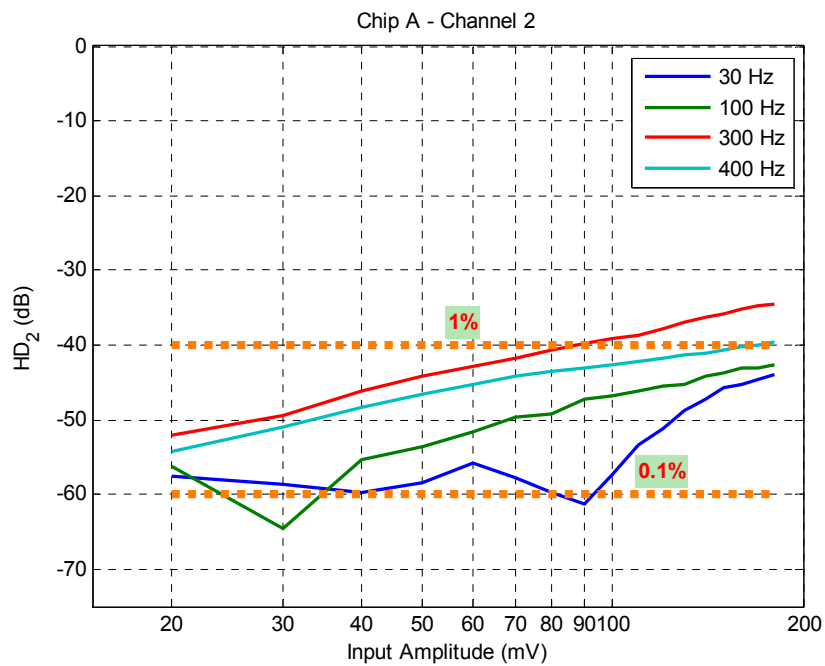
b)

Figure 5.29: The 2nd harmonic distortion (HD₂) plots of a) Chip A – channel 1, b) Chip A – channel 2, …
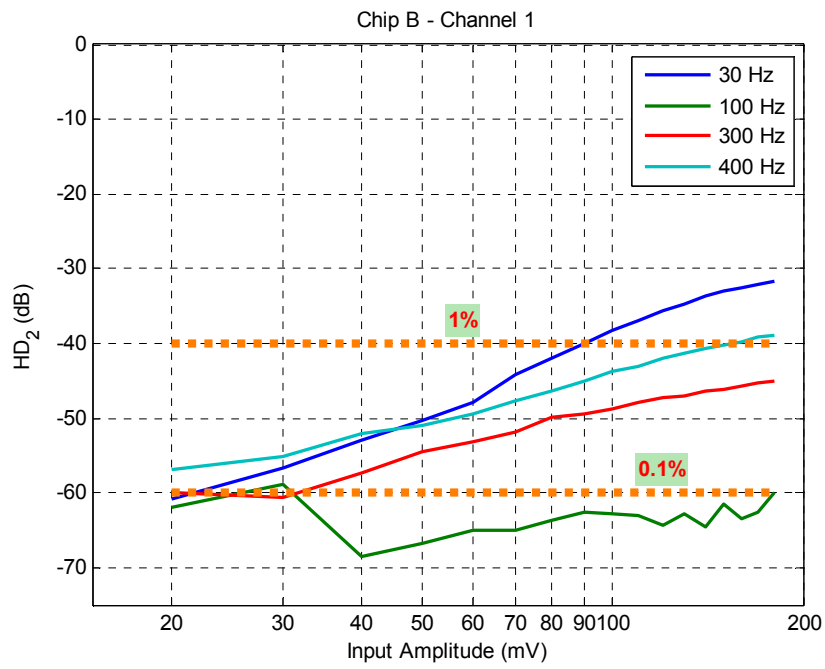
c)
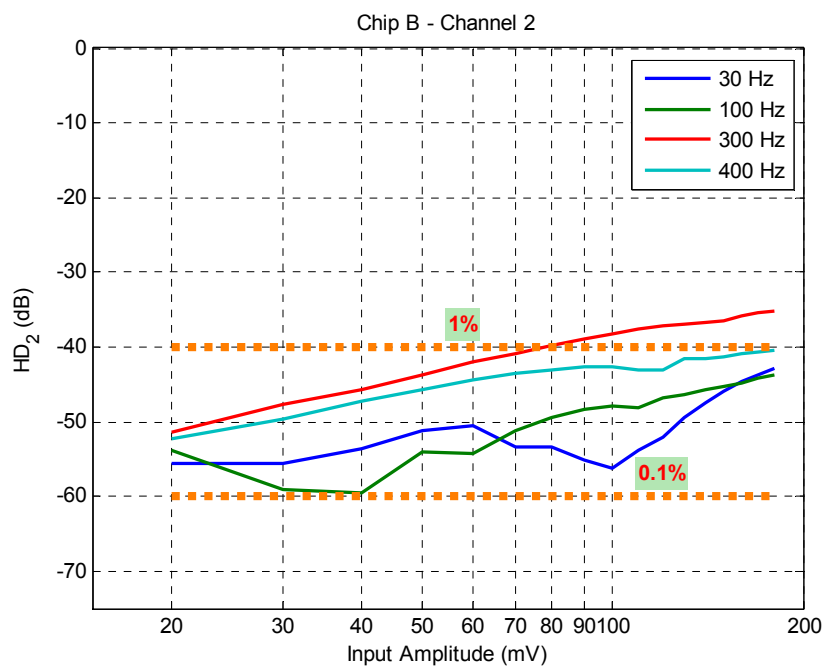
d)

Figure 5.29: The 2nd harmonic distortion (HD$_2$) plots of c) Chip B – channel 1, d) Chip B – channel 2, …
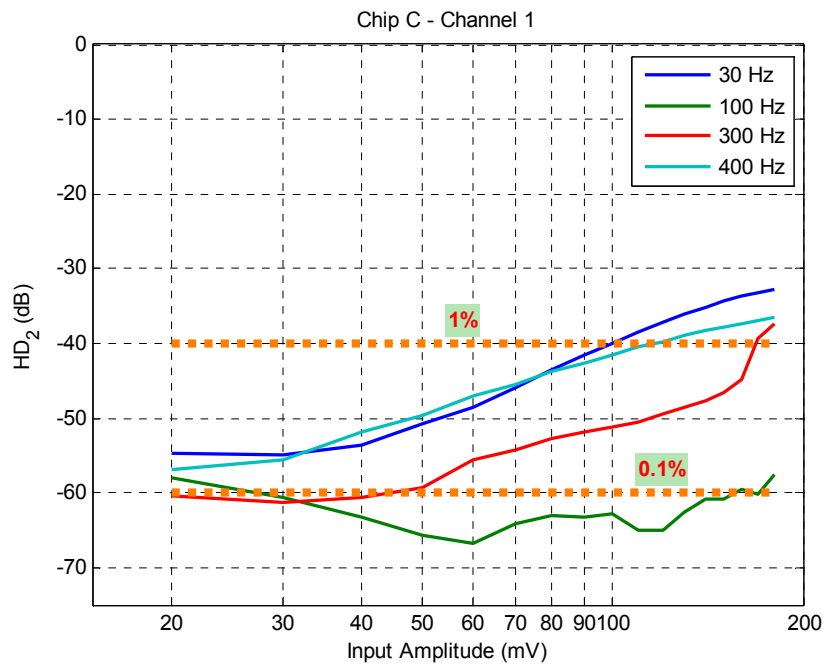
e)
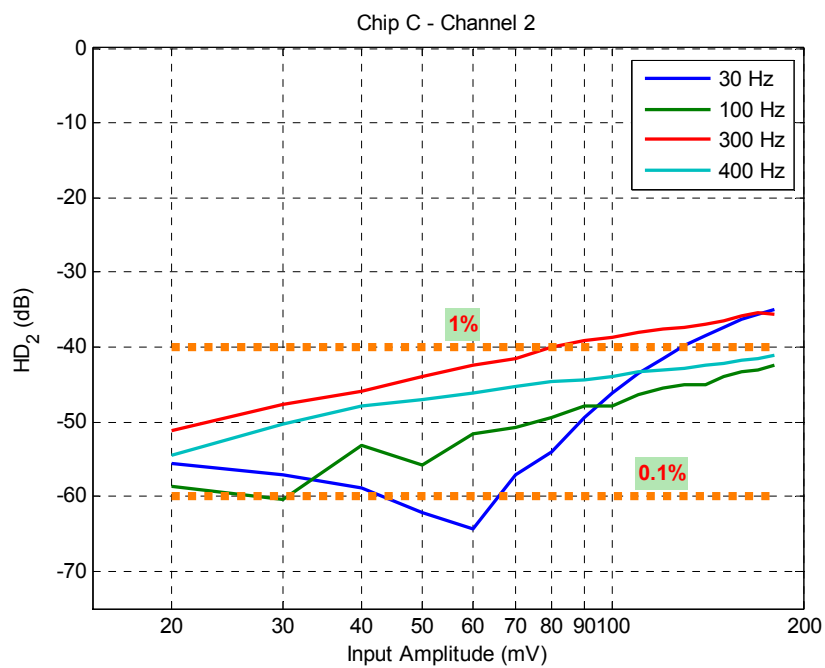
f)

Figure 5.29: The 2nd harmonic distortion (HD$_2$) plots of e) Chip C – channel 1, f) Chip C – channel 2, …
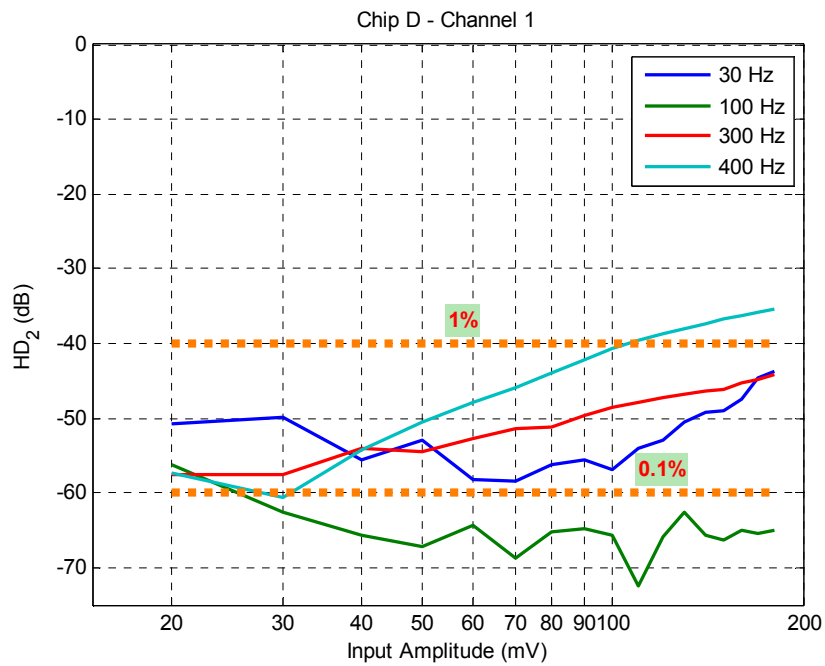
g)
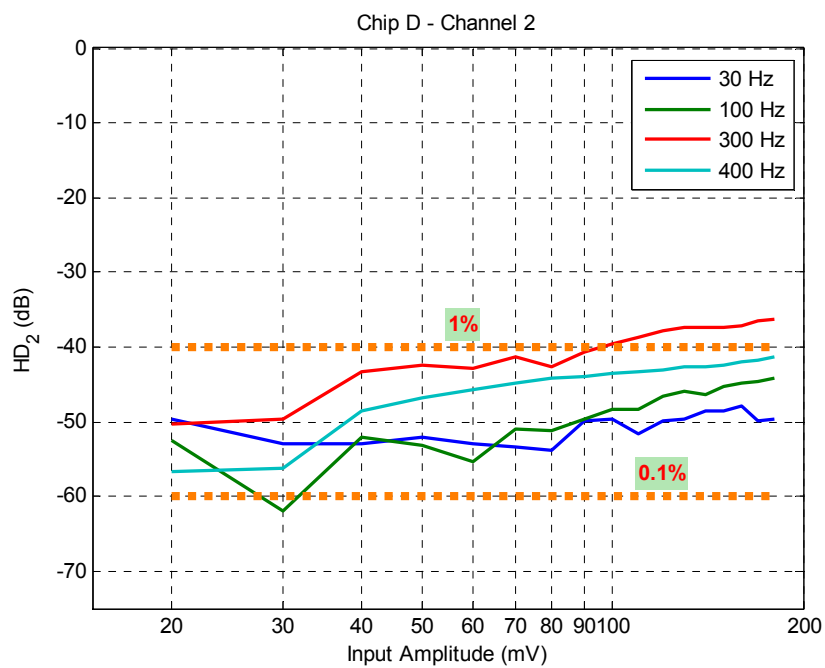
h)

Figure 5.29: The 2nd harmonic distortion (HD$_2$) plots of a) Chip A – channel 1, b) Chip A – channel 2, c) Chip B – channel 1, d) Chip B – channel 2, e) Chip C – channel 1, f) Chip C – channel 2, g) Chip D – channel 1, and h) Chip D – channel 2.

inside the pass-band. For each Gm-C filter, frequency and input amplitude, the magnitude in the frequency domain of the input signal frequency was compared to the magnitude in the frequency domain of its 2nd harmonic frequency i.e. for an input signal of 30 Hz, the 2nd harmonic frequency is 60 Hz. The difference between them is the 2nd harmonic distortion (HD_2). The Stanford Research Systems SR785 Dynamic Signal Analyzer was used to record the magnitudes in the frequency domain of the signal and its 2nd harmonic distortion.

This linearity analysis was completed for four different integrated circuits (ICs). For simplicity, they will be referred to as Chip A, Chip B, Chip C, and Chip D. Figure 5.29 presents the 2nd harmonic distortion (HD_2) plots for both channels of Chip A, B, C, and D.

In general, channel 1 of all four chips exhibit a better linearity performance or lower 2nd harmonic distortion (HD_2) than channel 2. Most of the channel 1 recording show less than 1% (or -40 dB) HD_2 distortion for 30 Hz and 400 Hz, for input amplitudes up to 100 mV and 110 mV respectively. Furthermore, channel 1 of all chips display consistently less than 0.1% (or -60 dB) HD_2 distortion for 100 Hz input and less than 1% HD_2 distortion for 300 Hz input. For channel 2, a 300 Hz input signal displays less than 1% HD_2 distortion for signal amplitudes up to 80 to 90 mV. As for other frequencies, they exhibit consistently less than 1% HD_2 distortion over the tested input signal amplitude range.

At the current level of minimum input amplitudes which gives below 1% HD_2 distortion (80 mV or 160 mV peak-to-peak), this should still be high enough to satisfy the expected input levels from the transducers for a person undergoing rigorous exercise, which is expected to be in the region of 125 to 150 mV peak-to-peak.

5.2.2.2 Inter-Modulation Distortion (IMD)

The inter-modulation distortion (IMD) test examines how well the filter performs when we have two signal sources that are very close in frequency. Inter-modulation is an undesirable behaviour especially in audio applications. It is caused by non-linearity within the signal processing chain. Thus, this test is required to ensure that our fabricated Gm-C filters do not exhibit the non-linear behaviour which causes this undesirable effect in the filtered signal. This test was carried out using the signal analyser which was able to act as two signal sources of different frequencies. The test was done for 100 Hz and 200 Hz, where the input frequencies were at 99 Hz and 101 Hz, and 198 Hz and 202 Hz, respectively. The results were obtained by comparing the magnitude in the frequency domain of the main input frequencies
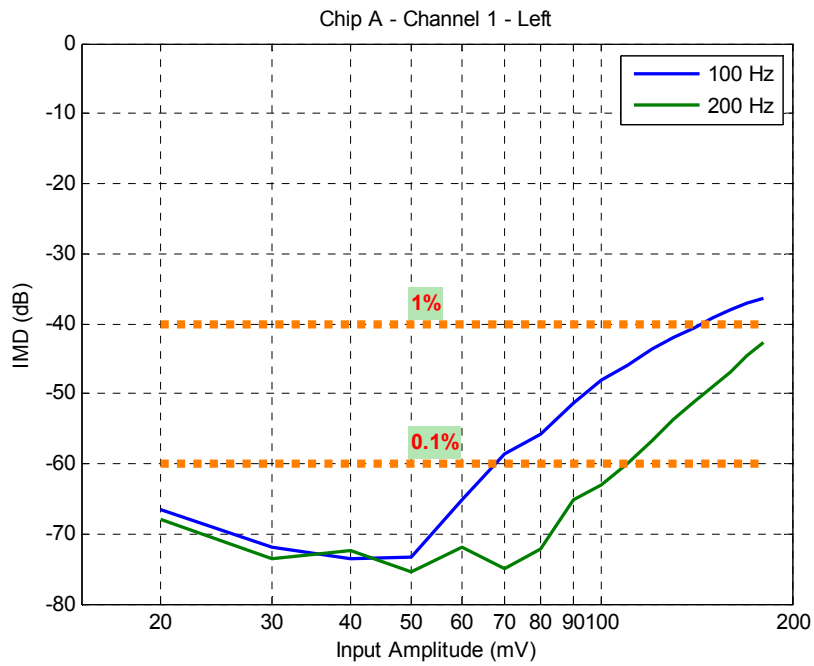
a)
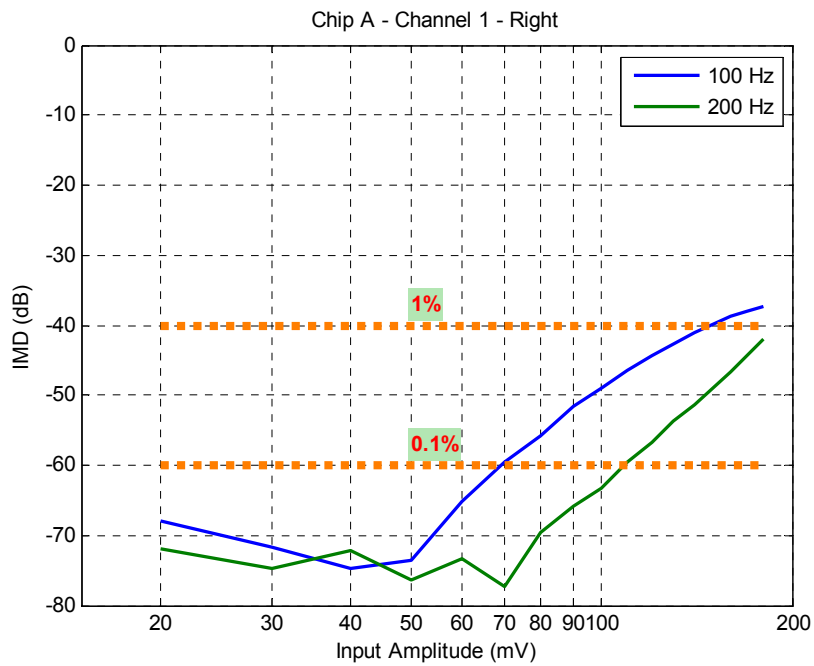
b)

Figure 5.30: The inter-modulation distortion (IMD) plots of a) Chip A – channel 1 – left, b) Chip A – channel 1 – right; 'left' indicates comparing 99 with 97 Hz and 198 with 194 Hz, while 'right' indicates comparing 101 with 103 Hz and 202 with 206 Hz …
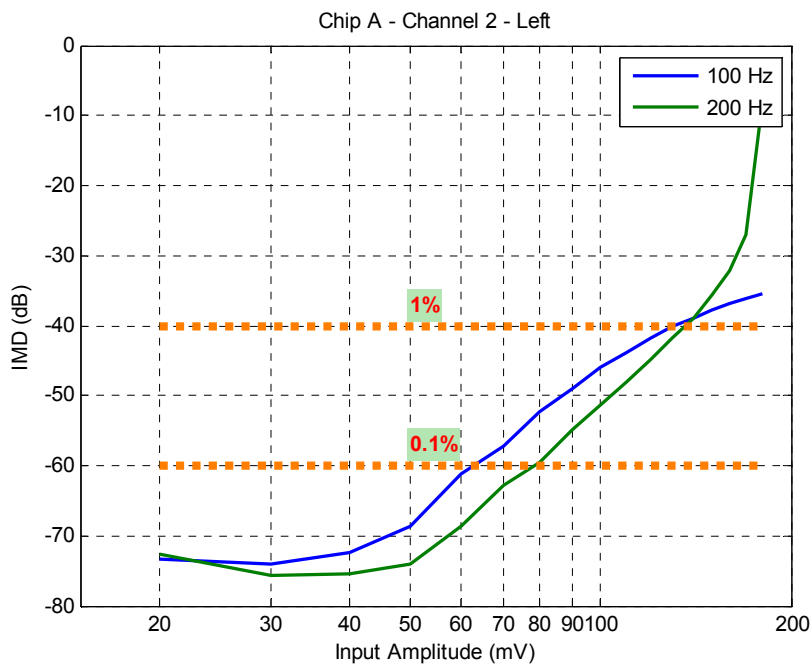
c)
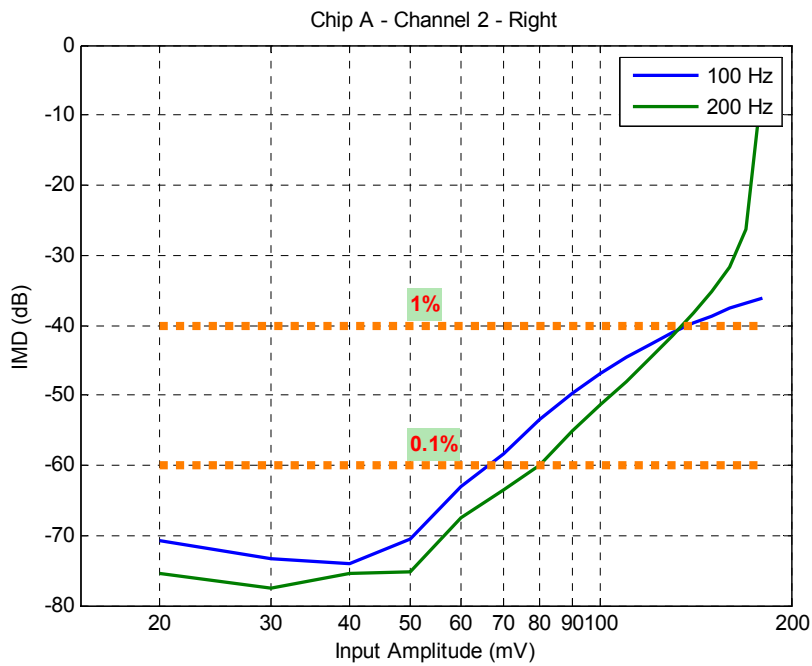
d)

Figure 5.30: The inter-modulation distortion (IMD) plots of c) Chip A – channel 2 – left, d) Chip A – channel 2 – right; 'left' indicates comparing 99 with 97 Hz and 198 with 194 Hz, while 'right' indicates comparing 101 with 103 Hz and 202 with 206 Hz …
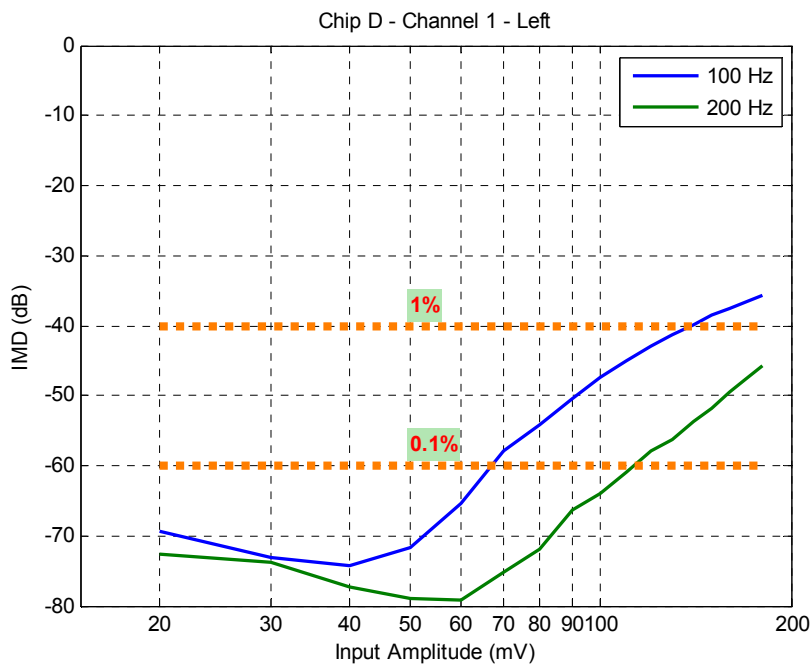
e)
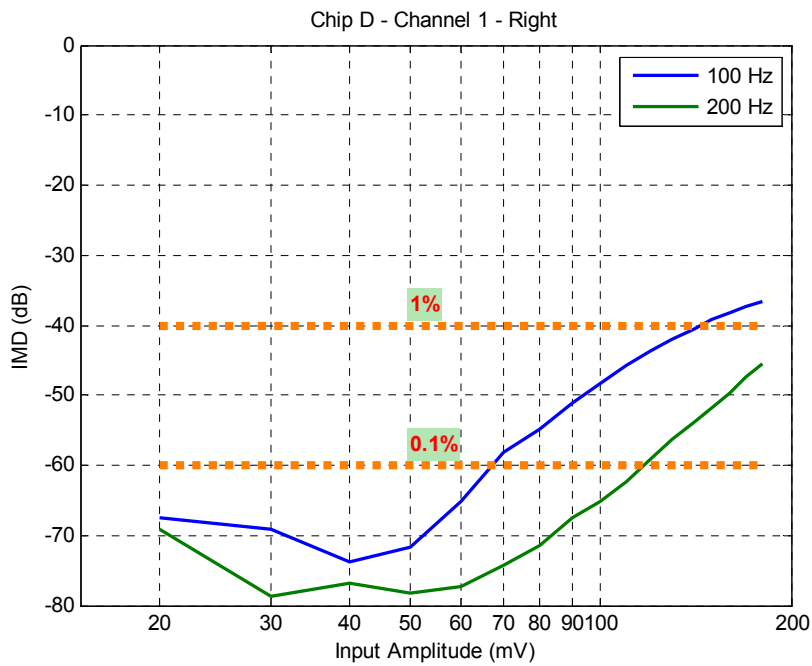
f)

Figure 5.30: The inter-modulation distortion (IMD) plots of e) Chip D – channel 1 – left, f) Chip D – channel 1 – right; 'left' indicates comparing 99 with 97 Hz and 198 with 194 Hz, while 'right' indicates comparing 101 with 103 Hz and 202 with 206 Hz …
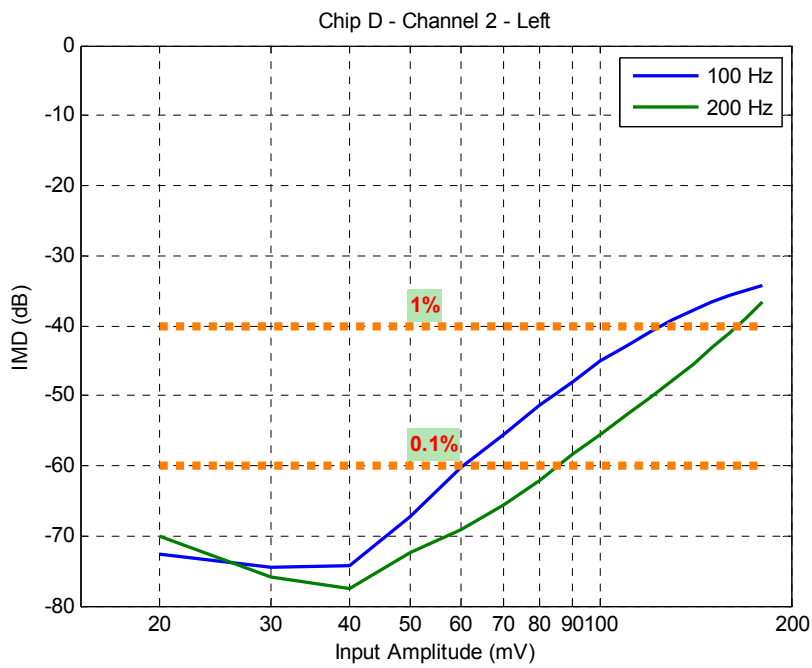
g)
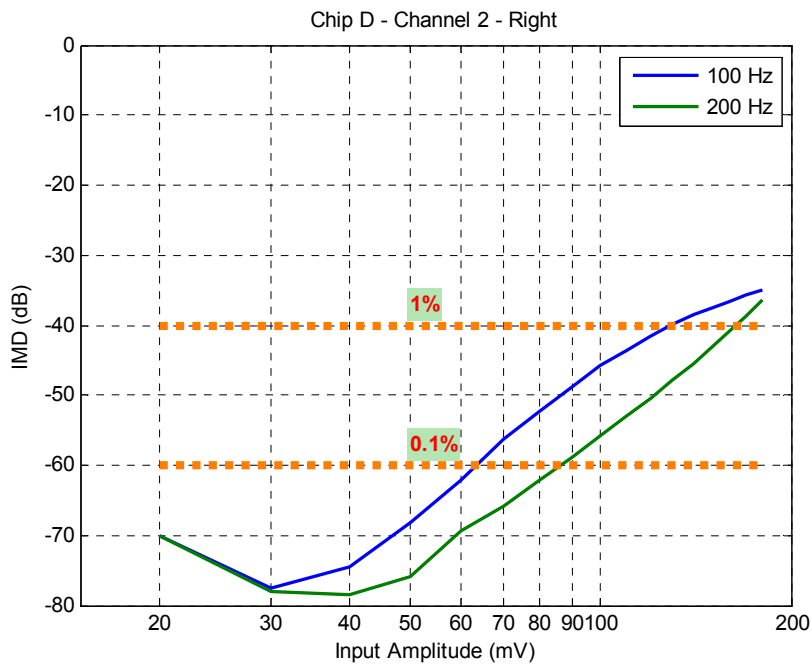
h)

Figure 5.30: The inter-modulation distortion (IMD) plots of a) Chip A – channel 1 – left, b) Chip A – channel 1 – right, c) Chip A – channel 2 – left, d) Chip A – channel 2 – right, e) Chip D – channel 1 – left, f) Chip D – channel 1 – right, g) Chip D – channel 2 – left and h) Chip D – channel 2 – right – 'left' indicates comparing 99 with 97 Hz and 198 with 194 Hz, while 'right' indicates comparing 101 with 103 Hz and 202 with 206 Hz.

(i.e. 100 Hz – 99 Hz and 101 Hz; 200 Hz – 198 Hz and 202 Hz) with the magnitude at the frequencies of the inter-modulates (i.e. 100 Hz – 97 Hz and 103 Hz; 200 Hz – 194 Hz and 206 Hz). The difference between them is termed 'Inter-Modulation Distortion (IMD)'.

The inter-modulation distortion test was conducted for two integrated circuits – Chip A and Chip D. Figure 5.30 presents the inter-modulation distortion (IMD) plots for both channels of Chip A and D for both the left (comparing 99 with 97 Hz and 198 with 194 Hz) and the right (comparing 101 with 103 Hz and 202 with 206 Hz).

Both channels of both chips produced very similar results with less than 0.1% IMD and 1% IMD even for input amplitudes of greater than 60 mV and 120 mV, respectively. Furthermore, 200 Hz input signals have a better (lower) IMD than its 100 Hz counter-part for input amplitudes up to 140 mV. This result is very encouraging when our expected input signal range is between 25 to 150 mV peak-to-peak, where we can expect less than -50 dBs of inter-modulation distortion (IMD).

5.2.2.3 Overall Frequency Response

The next step in determining the performance of the fabricated Gm-C filters is to compare their frequency responses with the designed specifications. The frequency response of the filters were obtained using the signal analyser in sweep mode from 1 Hz to 800 Hz. Figure 5.31 illustrates the frequency response of both channels of the fabricated Gm-C filters for Chip A, B, C, D, and E.

The fabricated Gm-C filters of both channels for all chips have a good matching to the Monte Carlo simulation averaged lower cut-off frequency (25 Hz) – ranging between 21 and 25 Hz. This represents about ±10% variation from the middle value. However, the filters exhibit some unexpected behaviours in the pass-band and near their upper cut-off frequency. Firstly, the frequency response of the Gm-C filters starts to fall steadily at around 50 Hz. The frequency response then reaches a minimum at around 250 Hz before a slight resonance is observed at the higher frequency end. Furthermore, the upper cut-off frequencies of the fabricated Gm-C filters differ quite significantly from the designed specification – dropping to between 401 Hz and 434 Hz – compared to the Monte Carlo simulation average of 719 Hz. Thus, the bandwidth has dropped to between about 380 Hz to 413 Hz from the Monte Carlo simulation average of 694 Hz. Still, the variation in the upper cut-off frequency and the bandwidth is around ±5% from the middle value.
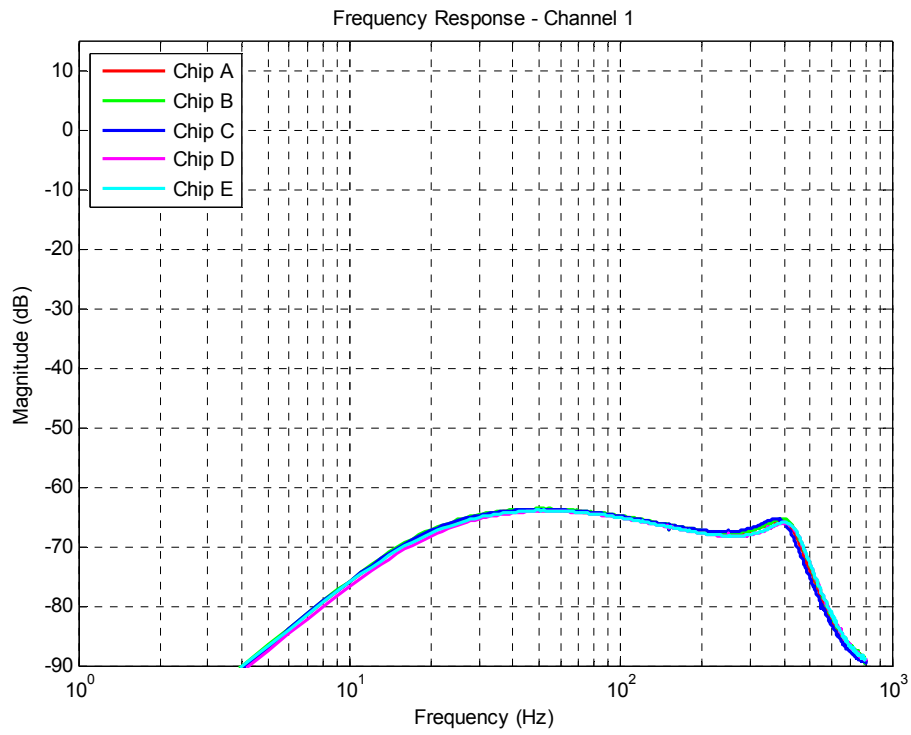
a)
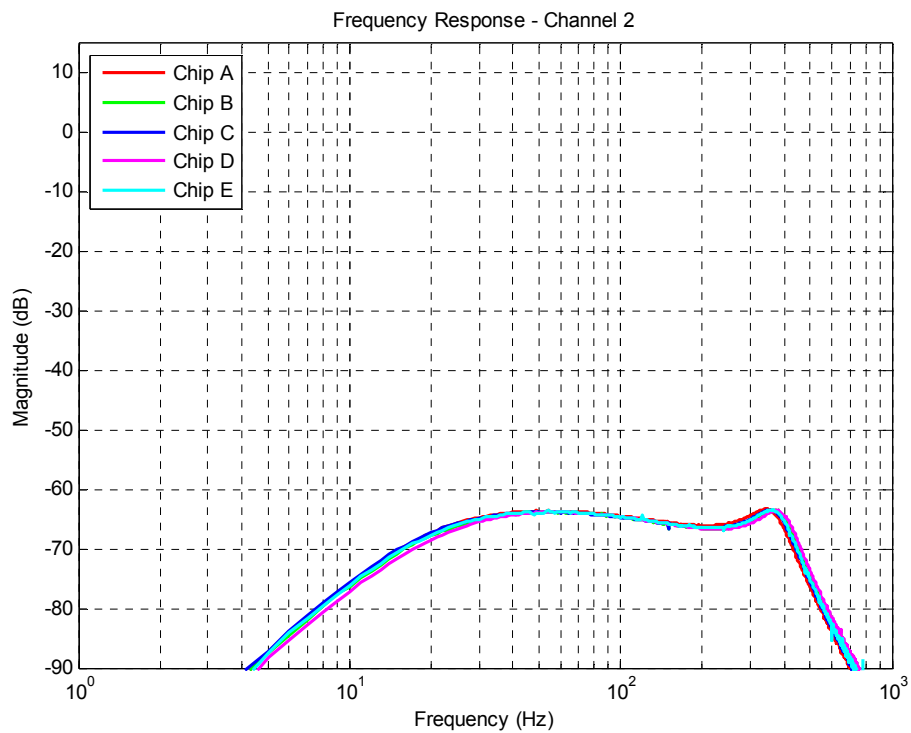
b)

Figure 5.31: The frequency response of the fabricated Gm-C filters compared to the designed for Chip A, B, C, D, and E for a) channel 1 and b) channel 2.

Tunable Filter

When the integrated circuit (IC) was laid out, a number of current inputs were added to all the PMOS current mirror outputs that controls the bias current of the multi-tanh triplet transconductors, shown in Figure 5.25. These current inputs were placed there, in the case where the fabricated Gm-C filters do not operate as we designed them to be. Since the pass-band characteristics and the upper cut-off frequency of the Gm-C filter are not as we would expect, thus we can use these current inputs to try and better understand the deficiencies of the current integrated design (IC). Thus, this section will examine the effects of sourcing or sinking currents into the five current inputs which alter the bias current of the transconductors in channel 1 of the Gm-C filter, in addition to the bias current of the Gm-C filter I_{IN1}, namely:

1. The currents controlling the simulated *floating* inductor (shown in Figure 5.5 b))

   a. I_{11A} – controls the bias current of transconductor g_{m1},

   b. I_{14A} – controls the bias current of the *left* transconductor g_{m2}, and

   c. I_{14B} – controls the bias current of the *right* transconductor g_{m2}.

2. The currents controlling the simulated *grounded* inductor (shown in Figure 5.5 a))

   a. I_{11B} – controls the bias current of transconductor g_{m1}, and

   b. I_{11C} – controls the bias current of transconductor g_{m2}.

Figure 5.32 illustrates the circuit diagram of the Gm-C filter designed with the current inputs I_{11A}, I_{14A}, I_{14B}, I_{11B}, and I_{11C}. Figure 5.33 presents the graphs of the filter's frequency response to the variations of the bias current of the Gm-C filter I_{IN1}, the currents controlling the simulated *floating* inductor I_{11A}, I_{14A}, and I_{14B}, and the currents controlling the simulated *grounded* inductor I_{11B} and I_{11C} – for channel 1 of Chip A.

At default, the current bias of the channel 1 Gm-C filter I_{IN1} is set to -1 nA. This means that the external current source is *sinking* 1 nA of current, which sets up three multi-tanh triplet transconductor in this channel with 1 nA of tail current for the centre symmetric differential pair of the triplet and 3 nA of tail current for each of the two asymmetric differential pairs of the triplet. Thus when I_{IN1} is set to -0.5 nA, the tail currents of these three transconductors will drop by to 0.5 nA and 1.5 nA, for the symmetric and asymmetric pair respectively.
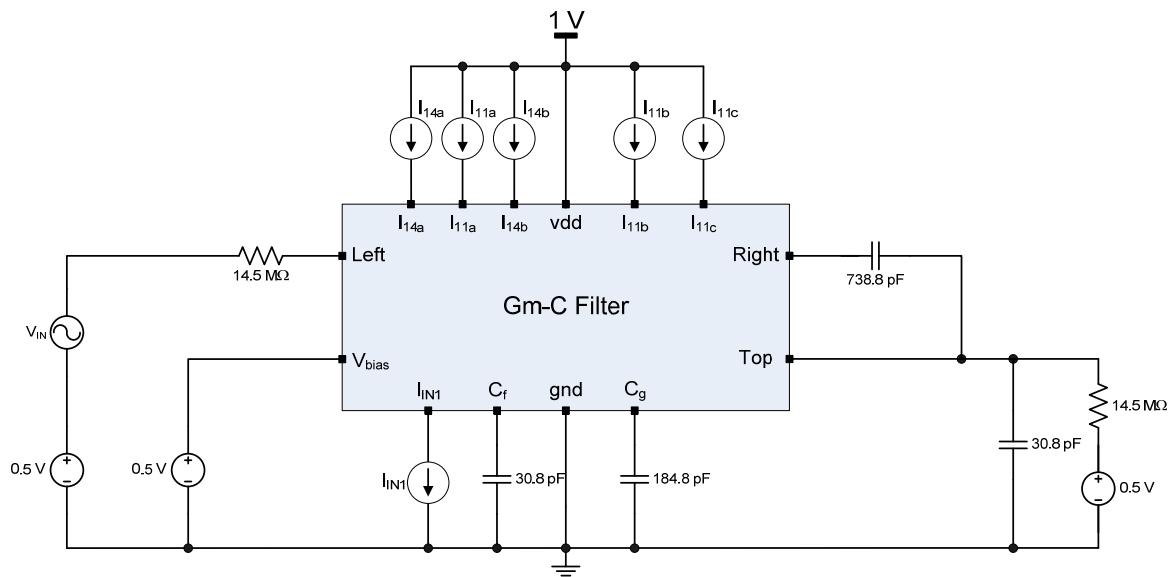
Figure 5.32: the circuit diagram of the Gm-C filter designed with the current inputs I_{11A}, I_{14A}, I_{14B}, I_{11B}, and I_{11C}.
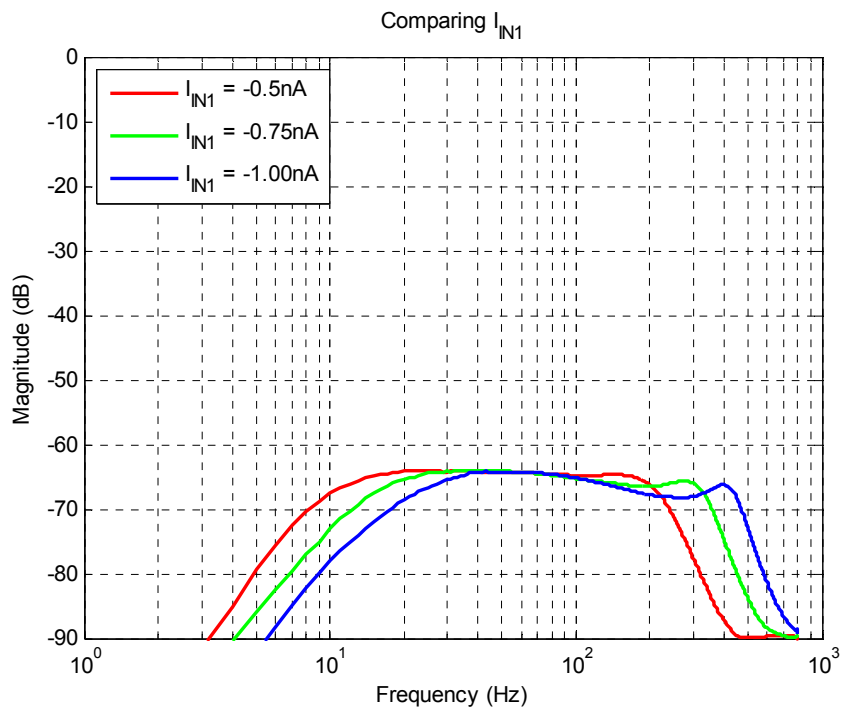
a)

Figure 5.33: The frequency responses of a Gm-C filter to variations of a) the bias current of the Gm-C filter I_{IN1}, …
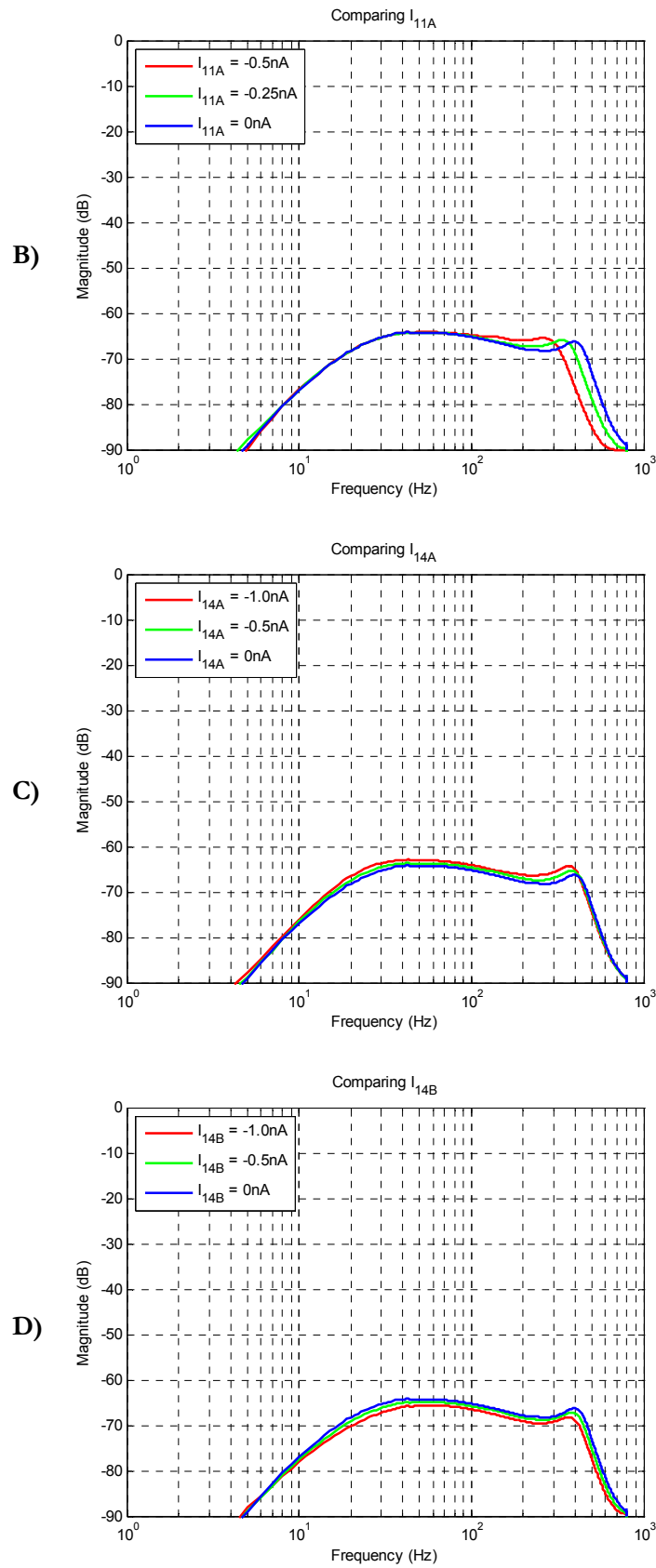
Figure 5.33: The frequency responses of a Gm-C filter to variations of the currents controlling the simulated *floating* inductor b) I_{11A}, c) I_{14A}, and d) I_{14B}, …
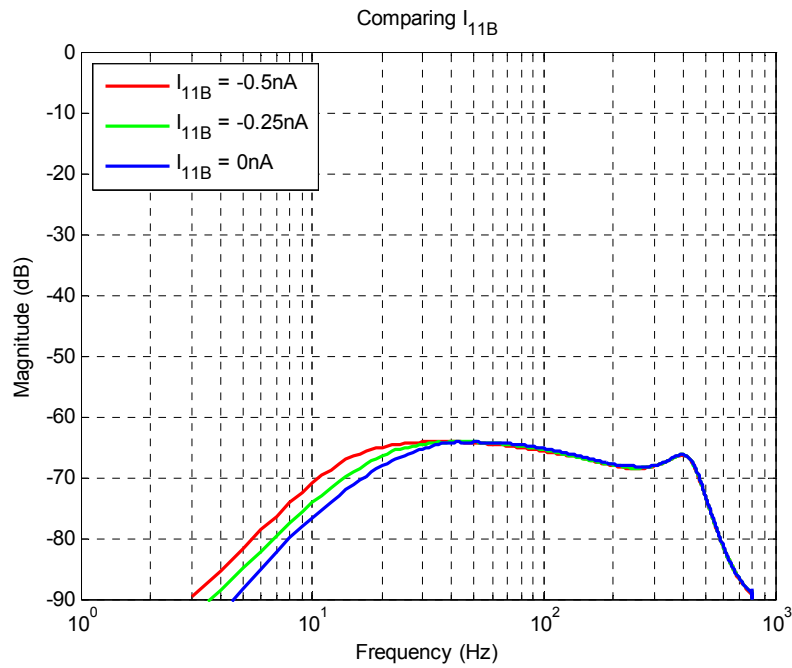
e)
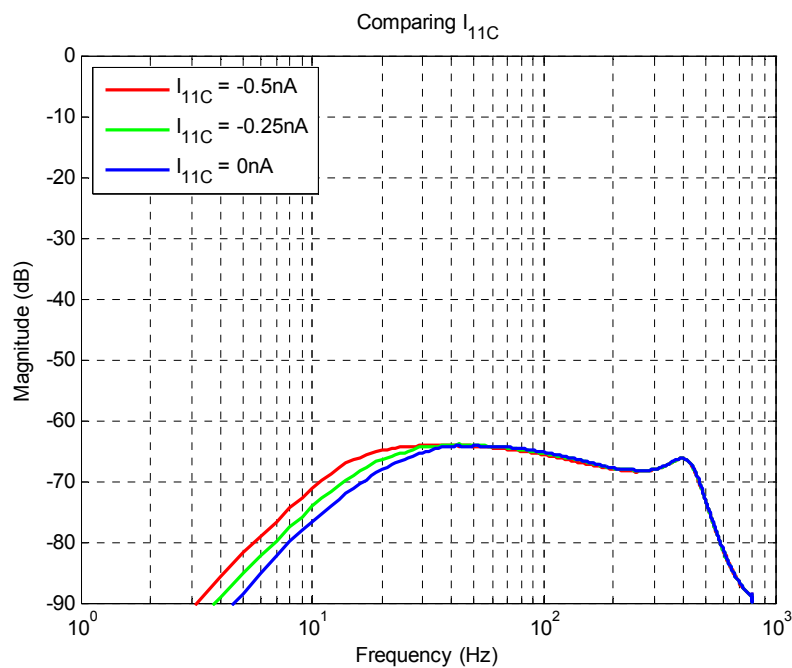
f)

Figure 5.33: The frequency responses of a Gm-C filter to variations of a) the bias current of the Gm-C filter I_{IN1}, the currents controlling the simulated *floating* inductor b) I_{11A}, c) I_{14A}, and d) I_{14B}, and the currents controlling the simulated *grounded* inductor e) I_{11B} and f) I_{11C} – for channel 1 of Chip A.

The reduction in all the tail currents (Figure 5.33 a)) produced a left shift in the frequency response of the filter. This introduces a drop of about 6 Hz to the lower cut-off frequency and about 110 Hz to the upper cut-off frequency, for every halving of the bias current I_{IN1}. Furthermore, the reduction of the bias current I_{IN1} results in a flatter response at the higher frequency end.

Since the current inputs I_{11A}, I_{14A}, I_{14B}, I_{11B}, and I_{11C} were not used in the initial testing of the Gm-C filters, thus their default values are 0. However the difference here to the bias current I_{IN1} is that by *sinking* from these current inputs i.e. negative current values, we are reducing the bias currents to the transconductors and thus the tail current of the differential pairs in the transconductors.

For the simulated *floating* inductor – by sinking current from input I_{11A} (Figure 5.33 b)), there is no effect on the response at the lower frequency end of the filter. However, there is a significant reduction in the upper cut-off frequency and a flattening of frequency response at the higher frequency end. The sinking of current from input I_{14A} (Figure 5.33 c)) results in a slightly higher frequency response and lower upper cut-off frequency. While doing the same for input I_{14B} (Figure 5.33 d)) results in a slightly lower frequency response and lower upper cut-off frequency.

For the simulated *grounded* inductor - by sinking current from input I_{11B} (Figure 5.33 e)), there is no effect on the response at the higher frequency end of the filter. However, there is a significant reduction in the lower cut-off frequency. The same result was obtained when sinking current from input I_{11C} (Figure 5.33 f)).

In general, the opposite effect can be applied to the frequency response of the Gm-C filter by *sinking* more than 1 nA of current for I_{IN1} or *sourcing* currents into the current inputs I_{11A}, I_{14A}, I_{14B}, I_{11B}, and I_{11C}. Therefore, it is possible to reasonably tune the frequency response of the fabricated Gm-C filter by altering those parameters.

5.2.3 Discussion

In the last section, a number of experiments were performed on the fabricated integrated circuits (ICs) each with two Gm-C filters. The experiments that were carried out were intended for determining the performance of the fabricated integrated circuit (IC) in relation to the designed specifications. These experiments include the test of linearity between the input and the output by measuring the 2nd harmonic distortion (HD$_2$), the inter-modulation

distortion (IMD) to ensure that non-linearity within the Gm-C filter does not introduce significant amount of the undesirable crosstalk between two close frequency sources, and the frequency response to compare it with the designed frequency response.

The linearity of eight (4 ICs x 2 channels) fabricated Gm-C filters (Figure 5.29) was found to be lower than expected (~130 mV in amplitude for 1% THD) for some frequencies in the pass-band. For channel 1, this behaviour is present for both the 30 Hz and the 400 Hz signals which can be as low as 90 mV in amplitude for 1% HD_2. Although, normally the 100 Hz and 300 Hz signals exhibit less than 1% HD_2 for input amplitudes up to 180 mV. For channel 2, only the 300 Hz signal exhibit this lower than expected input amplitude for 1% HD_2, with the lowest at 80 mV. The 30 Hz, 100 Hz, and 400 Hz signals remained below 1% HD_2 for input amplitudes up to 180 mV, in most cases. Still this should be adequate for our application where the maximum input amplitude of the heart sound is expected to be about 65 mV, for a person undergoing exercise.

The inter-modulation distortion (IMD) experiment (Figure 5.30) was conducted for four (2 ICs x 2 channels) fabricated Gm-C filters. They all exhibit less than 1% IMD for 100 Hz and 200 Hz signals for input amplitudes up to 120 mV and more significantly, less than 0.1% IMD for input signals up to 70 mV.

The frequency response of ten (5 ICs x 2 channels) fabricated Gm-C filters were recorded and presented in Figure 5.31. The response at the lower cut-off frequency of the band-pass filter matches well with the Monte Carlo simulation average of 25 Hz. However, there are some unexpected behaviours at the higher frequency end with lower than expected upper cut-off frequency at about 410 Hz (averaged) compared to the Monte Carlo simulation average of 719 Hz. This represents a drop of about 300 Hz. Furthermore, a drop in the response was observed in the pass-band before an occurrence of a resonance effect. Both of these behaviours are believed to be associated with the use of discrete capacitors and the integrated circuit pads which are used to connect the internal circuits to external pins.

The effects of pads can be easily studied via simulations in Cadence. By comparing the frequency response with and without pads in a simulation, shown in Figure 5.34, the upper cut-off frequency is reduced with pads to about 680 Hz from 719 Hz. This reduction in the upper cut-off frequency of about 40 Hz is significant but it is not comparable to a 300 Hz reduction seen in the fabricated ICs. Additionally from Figure 5.34 b), it can be seen that the integrated circuit pads causes the upper cut-off frequency to roll-off at a faster rate than usual.
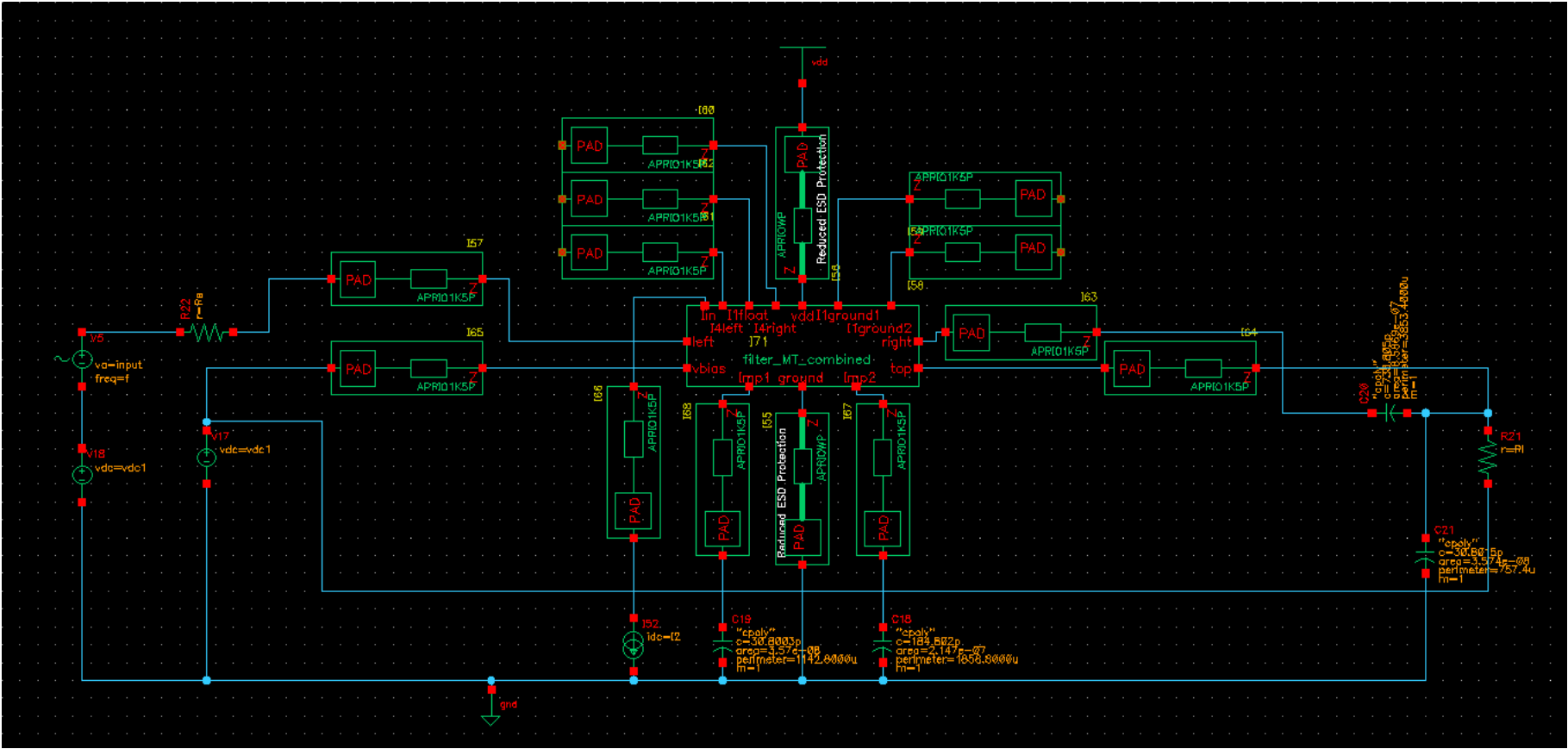
a)

Figure 5.34: a) The circuit diagram of the Gm-C filter with integrated circuit pads that are used to connect the internal circuit to the external pins, …
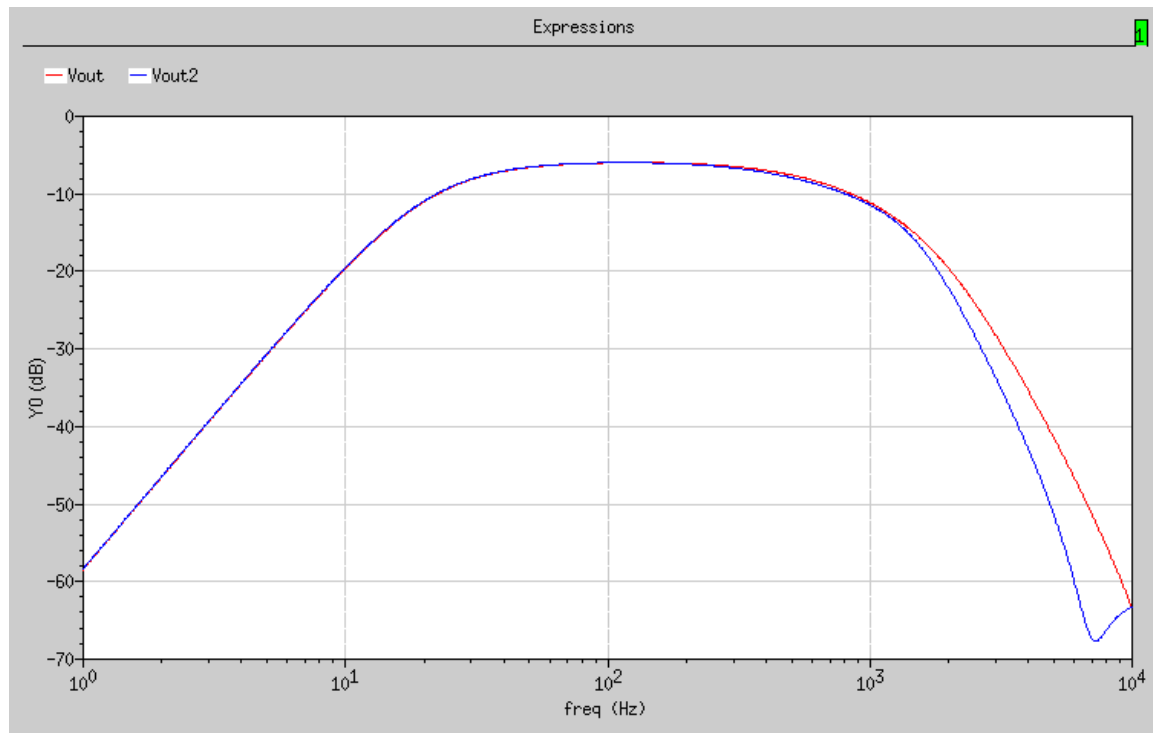
b)

Figure 5.34: a) The circuit diagram of the Gm-C filter with integrated circuit pads that are used to connect the internal circuit to the external pins and b) the frequency response comparison of the Gm-C filter - one with (blue) and one without pads (red).

Furthermore, all the capacitors required to build the Gm-C filters were constructed using discrete fixed and variable capacitors to get the values as closed to the design as possible. Since discrete capacitors are not ideal, this can have a significant impact on the simulated inductor values and thus the resonance frequencies formed by each LC branch or each combination of the capacitors and simulated inductors. From the results shown in Figure 5.33 b), c), and d), we can see that the change in the inductance of the simulated *floating* inductor due to the changes in the bias current of the transconductors controls the upper cut-off frequency or the higher frequency characteristics of the Gm-C filter.

Thus, it is believed that the discrepancies between the simulated response and the measured results are most likely to be mainly attributed to the non-ideality and tolerances of the capacitors, the effect of the capacitance and the inductance of the pads which is more pronounced than observed in the simulator, and the non-ideal behaviour of the capacitively loaded gyrator as an inductor.

5.3 Digital Circuit

In the data acquisition chain as shown in Figure 3.1 of Chapter 3, the processing of the heart sound signal is split into two parts. The first part involves the analogue front-end interfacing to obtain the signal and condition it for the second part. The second part concentrates on the digital signal processing of the heart sound signal to prepare it for the impending wireless transmission. This is performed by initially converting the analogue signal into a digital one using an analog-to-digital converter (ADC). Then the digital data was encoded to allow for error detection in the transmission process, using a Manchester encoder.

This digital signal processing block was looked at in Chapter 3, which consisted of three main parts:

      i)   The analog-to-digital converter (ADC),

      ii)   The Manchester encoder, and

      iii) The synchronisation circuit between the ADC and the encoder.

However in Chapter 3, only the single-channel system was examined in detail. And since the study of the de-noising algorithms in Chapter 4 indicated that a better performance and extra flexibility can be obtained by using a 2-channel system rather than a single channel one. Thus, the digital processing part should be extended to accommodate this requirement. Still, the main motivation behind the integration of the digital circuitry into the mixed-signal integrated circuit was not because of this further requirement, but lies mainly on two reasons:

1.   The synchronisation circuitry required to precisely time the operation of the Manchester encoder relative to the analog-to-digital converter (ADC) requires 5 off-the-shelf, discrete integrated circuits (ICs) and therefore too much space to achieve a compact size sensor.

2.   The off-the-shelf Manchester encoder is both too large and consume too much current (10 mA for normal operation) to achieve our desired objective of a sensor platform suitable for long-term monitoring of heart function.

In this thesis, only the integration of the synchronisation circuitry and the Manchester encoder will be discussed. The analog-to-digital converter (ADC) will remain as a discrete component.

All the logic gates' and flip-flops' circuit and layout design used to construct the synchronisation circuit and the Manchester encoder were provided by Austria Micro Systems (AMS) as part of its c35 core cells (http://asic.austriamicrosystems.com/databooks/c35/databook_c35_33/index.html). Only the overall digital circuit, layout and interconnections between these blocks that make up the synchronisation circuit and the Manchester encoder were designed by the author.

5.3.1 Timing Diagram for 2-channel system

A synchronisation circuit in the operation of all digital circuitry is required when digital data is being transfer from one location to another. This is because digital signals only consist of two possible states – ones and zeros, and by looking at a stream of digital signal (in a serial system) without knowing where the information in the stream start and where it ends would lead you to the wrong information. This is the same for our analog-to-digital converter (ADC) and Manchester encoder – if we do not have proper timing between them, the encoded data would be completely different to what we would actually want. Therefore, the first step to designing a synchronisation circuit is to compile a list of digital signals that are necessary for the operation of these components and draw up a timing diagram of their occurence.

5.3.1.1 Analog-to-Digital Converter (ADC)

In Chapter 3, a timing diagram was completed for a single channel system with Linear Technology LTC1285 12-bit analog-to-digital converter (ADC) and Holt Integrated Circuit HI-15530 Manchester encoder (and decoder). However, the Linear Technology LTC1285 analog-to-digital converter (ADC) has a *single* differential input, which is inadequate for a two-channel system. Therefore, the Linear Technology LTC1288 12-bit ADC with a software selectable 2-channel multiplexer input was selected, instead. The timing diagram of the LTC1288 ADC operation is shown in Figure 5.35 and it has the following digital input and outputs:

    1.   Linear Technology LTC1288 digital inputs:

        a. $\overline{CS}$ – the chip select input to enable the ADC conversion,

        b. D_{IN} – the digital data input to select the input to be converted, and

        c.   CLK – the clock which drives the conversion cycle of the ADC.

    2.   Linear Technology LTC1288 digital output:

a. D_{OUT} – the digital data output containing the converted information.
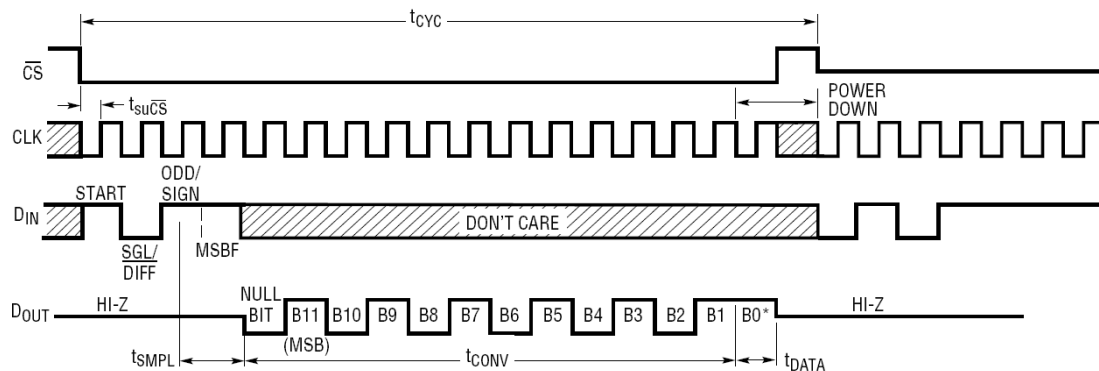
Figure 5.35: The timing diagram of the operation of the Linear Technology LTC1288 12-bit analog-to-digital converter (ADC) [2].

Chip Select Input, Clock Input and D_{OUT} Output

These inputs and output were discussed in detail in Chapter 3.

D_{IN} Input

The subject of the D_{IN} signal was touched briefly in Chapter 3, where the D_{IN} signal can be used to distinguish between channel 1 and 2 of the analog-to-digital converted signal. This was possible because the Manchester encoder can accommodate up to 16 bits of digital information. Thus, there are 4 bits that can be used to represent which channel the digital data belongs to. However in Chapter 3, the LTC1285 ADC does not require a control D_{IN} signal, thus it was left unchanged in a single-channel system.

For a 2-channel system, the D_{IN} signal has to change after each encoding cycle of the Manchester encoder or conversion cycle of the ADC, and control the multiplexer inside the LTC1288 ADC. Furthermore, due to the requirements of the Linear Technology LTC1288 ADC, the correct 4-bit control information must occur at a specific time [2]:

    i) START bit – the first logic '1' in the D_{IN} input after $\overline{CS}$ goes low. This tells the ADC to receive the next 3 bits that controls the operation of the ADC during its conversion cycle.

    ii) SGL/$\overline{DIFF}$ – this bit instructs the ADC to sample the selected input in single-ended (logic '1') or differential mode (logic '0'). **Single-ended mode** compares

the selected input with ground, while the differential mode compares the selected input with the other input.

iii) ODD/SIGN – this bit instructs the ADC to select the first input (CH0) or the second input (CH1). A logic '1' selects the first input; a logic '0' selects the second input.

iv) MSB First – this bit instructs the ADC how the converted data should be clocked out. A logic '1' will direct the ADC to only output in **Most-Significant-Bit (MSB) first format**. However, a logic '0' will direct the ADC to output the Least-Significant-Bit (LSB) first format after the MSB first format is complete.
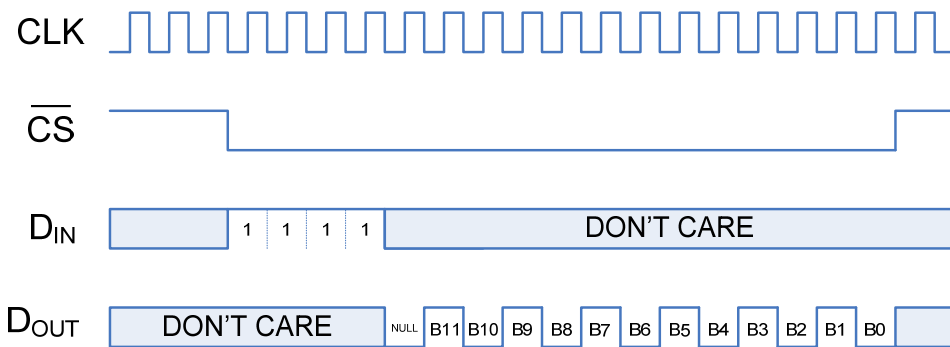
a)
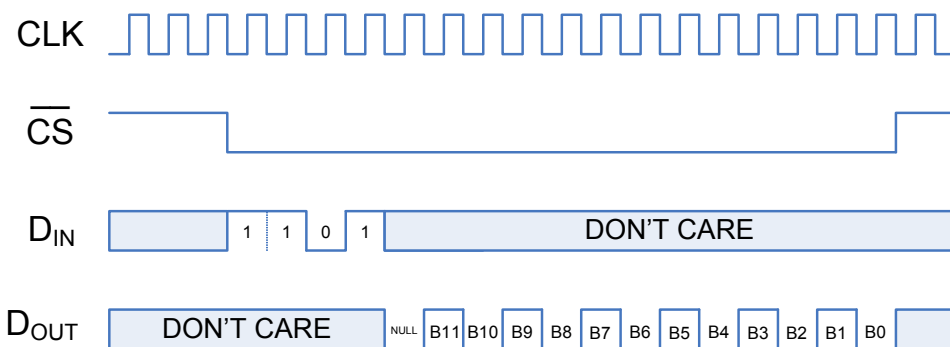
b)

Figure 5.36: A rough timing diagram for a) the 1st ADC conversion cycle and b) the 2nd ADC conversion cycle of the Linear Technology LTC1288 ADC.

From this information, we can derive the 4-bit control information that must be present in the D_{IN} signal for the two conversion cycles – one for channel 1 and the other for channel 2. By assigning the first input (CH0) to channel 1 and second input (CH1) to channel 2, the 4-bit control information to sample channel 1 in single-ended mode and output the converted information in MSB first format is '1111', while the corresponding 4-bit control digital signal is '1101'. However, it should be noted that the ADC requires one clock (CLK) cycle before the most significant bit (MSB) is outputted. Thus, a rough timing diagram for the ADC conversion cycle can be drawn up as shown in Figure 5.36.

5.3.1.2 Manchester Encoder

Since the Holt Integrated Circuit HI-15530 Manchester encoder will be replaced by a custom-built integrated Manchester encoder, thus to keep things simple we will maintain the output protocol ($\overline{BIPOLAR\ ZERO\ OUT}$) of the HI-15530 (as shown in Figure 3.17 in Chapter 3), so that the received signal from the radio transmission can be directly decoded using the HI-15530. The output protocol of the HI-15530 consists of three parts, which must be kept in synchronisation with the output of the ADC, D_{OUT}:

    i)   SYNC signal – to distinguish whether the information sent is data or a command,

    ii) The Manchester encoded information, and

    iii) The parity bit, P – to allow for error detection at the receiver end.

SYNC signal

The SYNC signal is probably the hardest signal to generate for this entire digital circuit. This is because it is 3 CLK cycles long but with a change in the middle of the 2nd CLK cycle. With only the current CLK signal being the highest frequency signal, the SYNC signal cannot be generated. Therefore a twice as fast 2xCLK signal is introduced to allow us to generate the SYNC signal. The SYNC signal must occur precisely 3 CLK cycles before the Manchester encoded information or 7 CLK cycles before the start of the ADC's D_{OUT}.

Manchester Encoded Information

The Manchester encoded information is an encoded version of the 16-bit information made up of parts of the 4-bit D_{IN} input signal and all of the 12-bit D_{OUT} output signal. The 16-bit

information only contain parts of the 4-bit D_{IN} input signal because there is a 1-bit delay between the end of the D_{IN} input signal and the start of the D_{OUT} output signal, therefore only the last 3 bits of the D_{IN} input signal is contained in the encoded 16-bit information. However, this should be sufficient to distinguish the source of the data because the last 3 bits of D_{IN} for the two ADC conversion cycle is different – being '111' and '101' for channel 1 and 2, respectively. The method for appending the D_{IN} and the D_{OUT} signals has been shown in Chapter 3.

Parity Bit, P

The parity bit is present to allow for error detection. This is possible by counting the number of logic '1's in the 16-bit information that has been encoded and ensuring that there are always an odd number of logic '1's in the Manchester encoded data in each encode cycle. Thus, if there is an even number of logic '1's in the 16-bit information, the parity bit will be a logic '1' Manchester encoded data. The parity bit occurs directly after the 16-bit Manchester encoded information.

5.3.1.3 Conclusion

From the above information of the Manchester encoder and the rough timing diagram of the ADC over two conversion cycles, an overall timing diagram of the digital circuit can be drawn up for both the ADC and the Manchester encoder, shown in Figure 5.37.

The main observation of the control signals of the ADC, the output of the Manchester encoder, and the RESET signal are as follows:

    a) ADC control signals:

        1) The chip select $\overline{CS}$ input is HIGH (logic '1') between count 0 to count 2 and goes LOW (logic '0') at the transition from count 2 to count 3, and remains low for the rest of the encode cycle.

        2) The D_{IN} signal is HIGH between count 3 to count 6 in the first encode cycle and is HIGH for count 3, 4 and 6, and LOW for count 5 in the second encode cycle. For the rest of the time within each encode cycle, we do not care about its state. However, the D_{IN} signal must toggle back and forth between the first and second encode cycle signal.
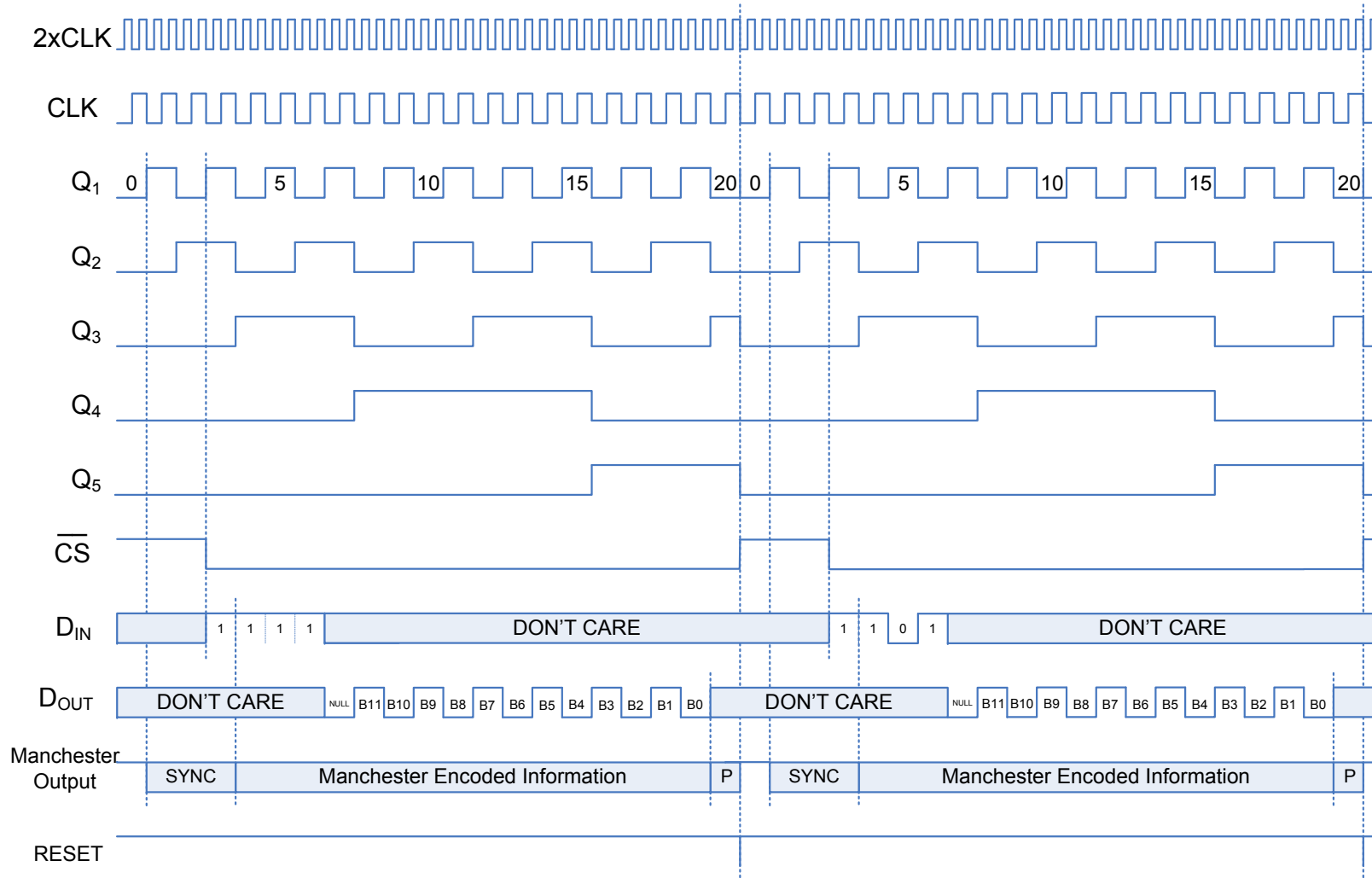
Figure 5.37: The overall timing diagram of the digital circuit for both the ADC and the Manchester Encoder.

b) Manchester encoder output, ENCODED:

1) The SYNC signal goes LOW at the transition between count 0 and count 1 and returns to a HIGH state in the middle of count 2 and stays high at least until the transition between count 3 and count 4.

2) The Manchester encoded information starts at the transition between count 3 and count 4 and finish at the transition between count 19 and count 20.

3) The parity bit begins at the transition between count 19 and count 20 and must be dependent on the number of logic '1's in the 16-bit information from D_{IN} and D_{OUT}.

c) RESET signal is set to occur at count 21 instead of count 20 in Chapter 3 because of the extra time required to complete the parity bit. This signal resets the synchronisation circuit for the next encode cycle.

5.3.2 Digital Circuit Design

Now that the timing diagram for the complete digital circuit has been established, the digital synchronisation circuit can be designed to generate the control signals for the Linear Technology LTC1288 ADC and the output components of the Manchester encoder. The truth table of all the digital functional blocks – flip-flops and logic gates, are shown in Appendix C of this thesis.

5.3.2.1 Chip Select of the ADC
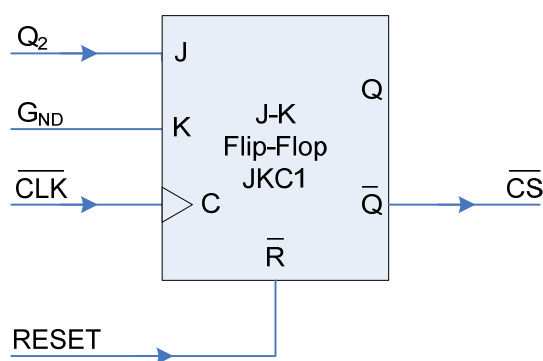
Figure 5.38: The chip select signal generator.

The modification to the chip select $\overline{CS}$ signal in Chapter 3 is that the transition from HIGH to LOW now occurs at the transition from count 2 to count 3, instead of count 4 to count 5

in the single-channel system. Thus instead of connecting the Q_3 output of the ripple binary counter to the J input of the J-K flip-flop, we connect the Q_2 output, instead (shown in Figure 5.38). The J-K flip-flop is reset at the end of each conversion cycle by the RESET signal.

5.3.2.2 D_{IN} of the ADC

As discussed earlier, the D_{IN} signal has to toggle back and forth and provide two different inputs for each two consecutive encode cycle. This signal was generated using a toggle (T) flip-flop (TFC1) to toggle between the two different encode cycles via the RESET signal – one for channel 1 and the other for channel 2. The output of the T flip-flop, Q, will toggle between a logic '1' in the first encode cycle and a logic '0' in the second encode cycle.

By connecting the output of this flip-flop, Q, to one input of an OR gate, we can have a signal with a logic '1' for one encode cycle. The signal for the other cycle will be determined by the other input to the OR gate.

By inspecting the timing diagram of the signals Q_1 and Q_3 of the binary ripple counter and using and exclusive-OR (XOR) gate, the output of the XOR gate will be HIGH for count 3, 4 and 6 and LOW for count 5, irrespective of the encode cycle. Thus, this can be used to generate D_{IN} for the alternate encode cycle.

Furthermore, an OR gate can be constructed using NAND gates through its NAND equivalent circuit which can be proven through Boolean algebra [18]. The Boolean algebra for an OR gate is shown below:

$$O = A + B = \overline{\overline{A} \cdot \overline{B}}$$
(5.21)
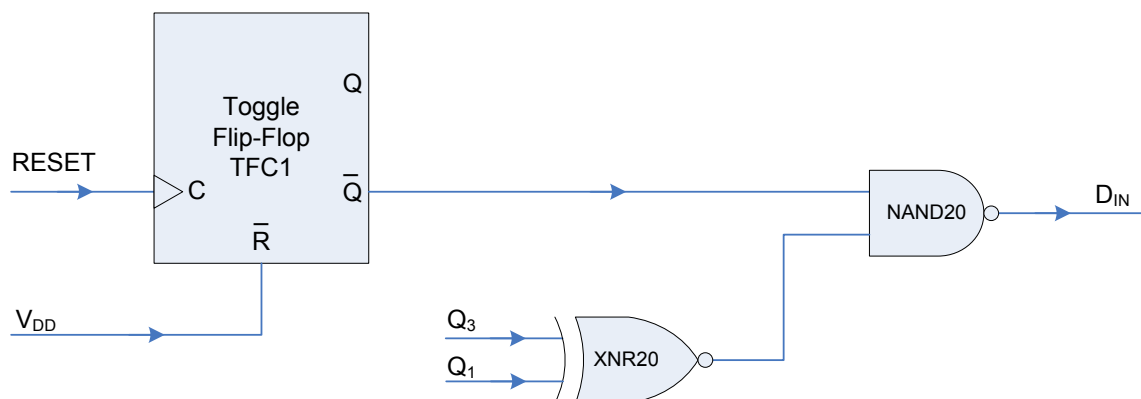
Figure 5.39: D_{IN} digital circuit.

Thus, A **or** B is equivalent to (**not** A) **nand** (**not** B). Since a NOT gate can be replaced by a NAND gate with its input tied together, therefore an OR gate can be built using three NAND gates or one NAND gates with two **not** inputs. Through this equivalence, we can connect the $\overline{Q}$ (**not** Q) output of the flip-flop to an input of a NAND gate and the other input connected to an exclusive-**N**OR (XNOR) gate between the Q_1 and Q_3 of the binary ripple counter. Therefore, the D_{IN} signal can be generated by the digital circuit shown in Figure 5.39.

5.3.2.3 16-bit ADC Data Buffer (B_DATA)

a)

b)
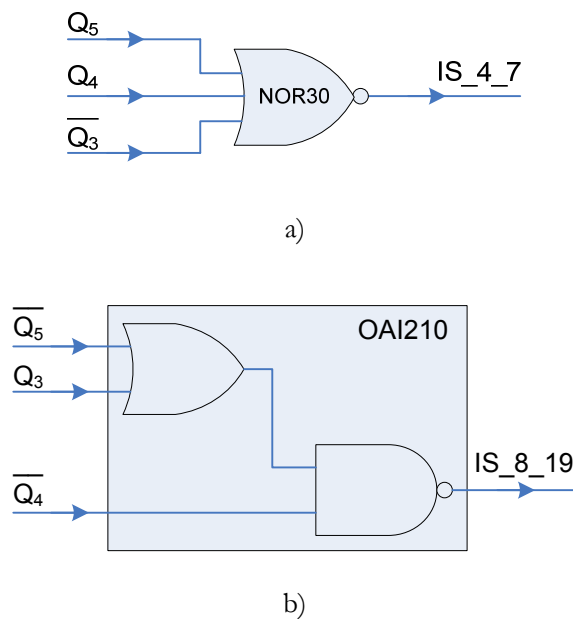
Figure 5.40: The digital circuit to verify that the binary ripple count is between a) 4 & 7 (IS_4_7) and b) 8 & 19 (IS_8_19).
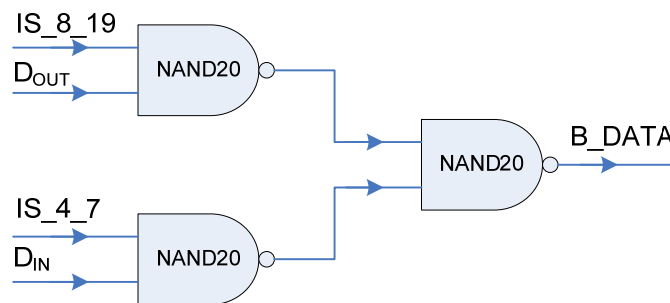
Figure 5.41: The 16-bit ADC data buffer (B_DATA) digital circuit.

The 16-bit ADC data buffer (B_DATA) was also mentioned in Chapter 3 as BUFFERED DATA. However in this section, some modification is made to ensure that the data is only present during these 16-bit period. Since the D_{IN} signal is present from count 3 to 6 and D_{OUT}

signal is present from count 8 to count 19, therefore to preserve all the converted data from the analogue signal the 16-bit ADC data buffer must be active between count 4 to 19. The data buffer was split into count 4 to 7 for the D_{IN} signal and count 8 to 19 for the D_{OUT} signal. The digital circuit to verify that the binary ripple count is between 4 & 7 (IS_4_7) and 8 & 19 (IS_8_19) is shown in Figure 5.40.

By using Boolean algebra, we can see that IS_4_7 is only HIGH (logic '1') when Q_3 is HIGH and both Q_4 and Q_5 are LOW (logic '0') and this only occurs between count 4 to 7 for each encode cycle, from the timing diagram in Figure 5.37.

$$IS\_4\_7 = \overline{\overline{Q_3} + Q_4 + Q_5} = Q_3 \cdot \overline{Q_4} \cdot \overline{Q_5} \tag{5.22}$$

The same can be similarly done for IS_8_19:

$$IS\_8\_19 = \overline{(Q_3 + \overline{Q_5}) \cdot Q_4} = (\overline{Q_3} \cdot Q_5) + Q_4 \tag{5.23}$$

The expression in the bracket of equation 5.23 is LOW until Q_5 goes HIGH at count 16. However Q_3 only remains LOW until count 20, so the expression in the bracket goes LOW at count 20 as well. Therefore, the expression in bracket will give a HIGH between count 16 to 19. While, Q_4 goes HIGH at count 8 and goes low at count 16, thus the overall gives a HIGH between count 8 to 19.

The 16-bit ADC data buffer (B_DATA) can be constructed similarly to the BUFFERED DATA in Chapter 3 with a modification. The digital circuit for this is shown in Figure 5.41.

5.3.2.4 SYNC Generator of the Manchester Encoder
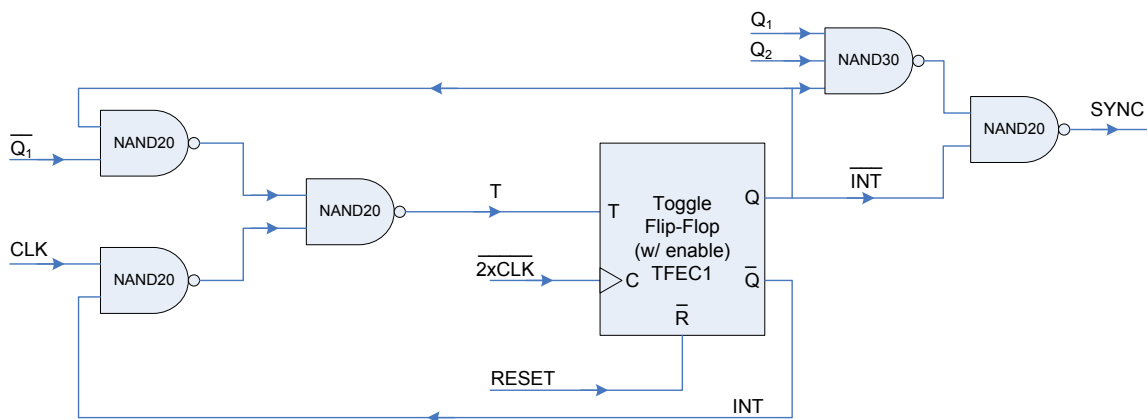
Figure 5.42: The SYNC generator digital circuit using only NAND gates and a toggle flip-flop with an active high enable (TFEC1).

The SYNC signal as discussed earlier starts by forcing the output of the Manchester encoder that is initially HIGH to LOW at the transition between count 0 and 1. This signal then remains LOW for one and a half count and then goes HIGH for another one and half count. Thus, it is clear that we need to construct an oscillator with at least an ON or OFF period of one and a half count. This was done using a toggle flip-flop, with an active high enable and an asynchronous reset (TFEC1), and a feedback loop. This oscillator is reset for every encode cycle. Figure 5.42 presents the digital circuit used to generate the SYNC signal.

$$SYNC = \overline{\overline{(Q_1 \cdot Q_2 \cdot Q)} \cdot Q} = (Q_1 \cdot Q_2 \cdot Q) + \overline{Q} \tag{5.24}$$

The SYNC signal was generated using equation 5.24. The signal from the $\overline{Q}$ output of the flip-flop between count 0 to 2 was used as the base for the SYNC signal. However, the SYNC signal must remain HIGH in count 3, therefore the expression in the bracket was introduced in equation 5.24 to generate the following at count 3 ($Q_1 = Q_2 = $ HIGH):

$$SYNC = Q + \overline{Q} = 1 \tag{5.25}$$

5.3.2.5 Buffer Encode of the Manchester Encoder

It has been shown in Chapter 3 that the Manchester encoded signal (B_ENCODED) can be generated simply by using an exclusive-OR (XOR) logic gate with the data that you want to encode at one input i.e. the 16-bit ADC Data Buffer or B_DATA, and a clock signal that has the same frequency as the data rate at the other input i.e. CLK. The digital circuit diagram of the Buffer Encode stage is shown in Figure 5.43.

Figure 5.43: The digital circuit of the Buffer Encode of the Manchester Encoder.

5.3.2.6 Parity Generator of the Manchester Encoder

The Parity bit of the Manchester encoder, as discussed earlier, is generated to ensure that there are always an odd number of logic '1's in each encoded information. Thus, a toggle flip-flop with an active high enable (TFEC1) was used to count the number of logic '1's in the 16-bit

ADC Data Buffer or B_DATA. If there are an even number of logic '1's in B_DATA, the $\overline{Q}$ of the flip-flop will be HIGH and thus a logic '1' is generated for the Parity bit. The digital circuit of the Parity Generator circuit is shown in Figure 5.44.
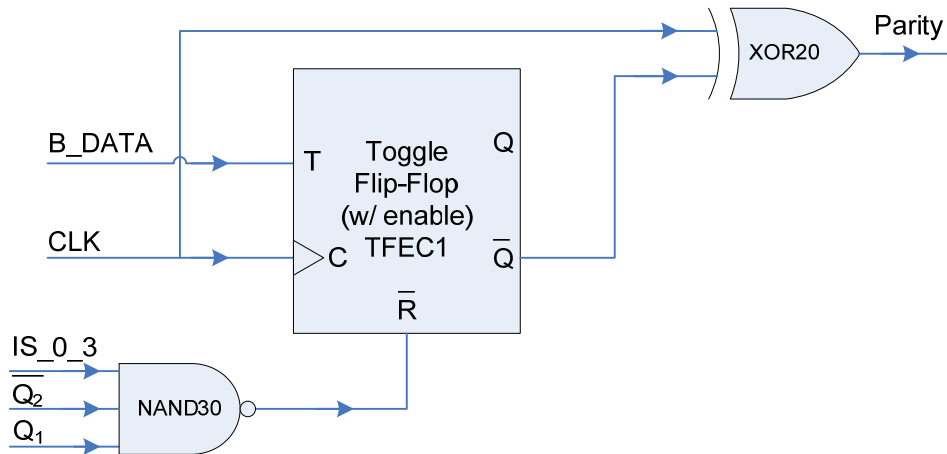
Figure 5.44: The digital circuit of the Parity Generator of the Manchester Encoder.

The Parity Generator is reset after each encoding cycle using a NAND gate with three inputs, given by the following equation:

$$\overline{R} = \overline{Q_1 \cdot \overline{Q_2} \cdot IS\_0\_3} \tag{5.26}$$

This can be further simplified to give:

$$R = Q_1 \cdot \overline{Q_2} \cdot IS\_0\_3 \tag{5.27}$$

Thus, the reset occurs during the time when only Q_1 is HIGH between count 0 to 3, or during count 1. The digital circuit to generate IS_0_3 is shown in Figure 5.45.
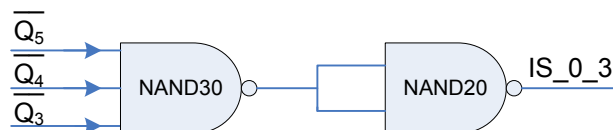
Figure 5.45: The digital circuit to verify that the ripple counter is between count 0 and 3.

5.3.2.7 Encode Out of the Manchester Encoder
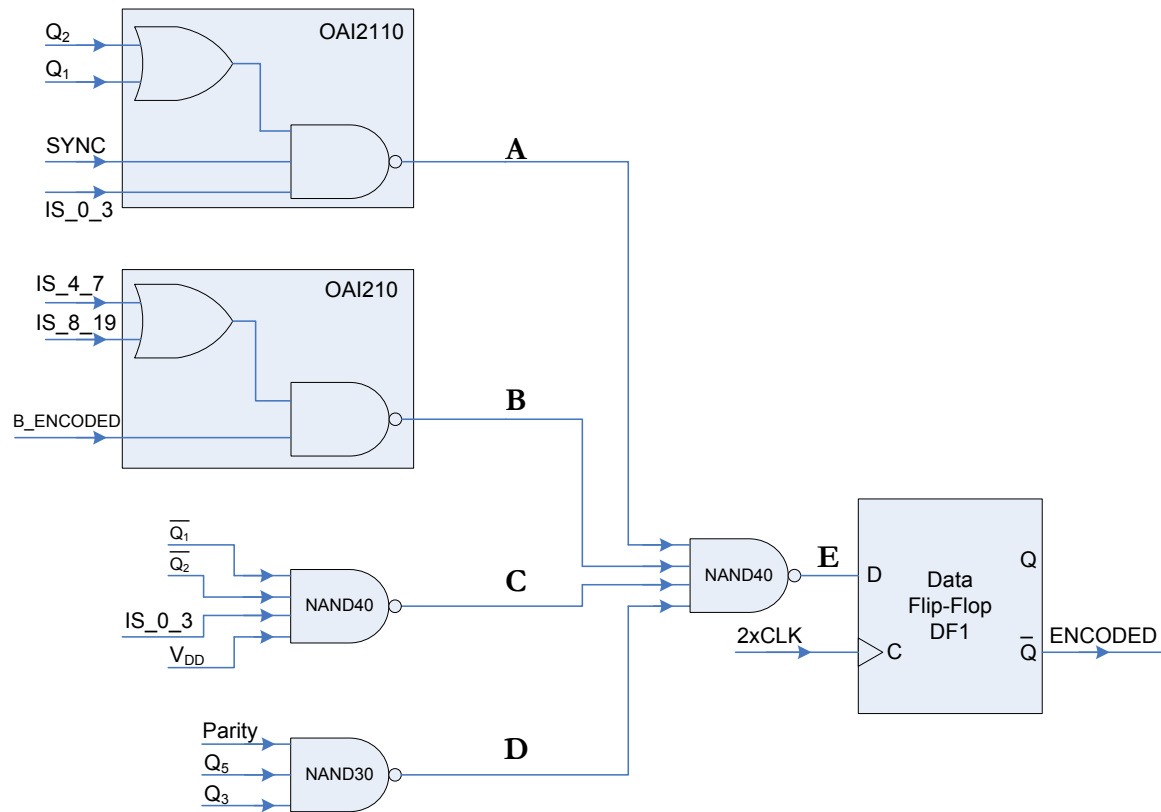
Figure 5.46: The digital circuit of Encode Out of the Manchester Encoder.

Since all the signals necessary to construct the output of Manchester encoder have been generated, the natural next step is to combine them to form the overall output of the Manchester encoder. The digital circuit to perform this 'Encode Out' function is illustrated in Figure 5.46. Let's imagine that the four signal branches in Figure 5.46 are denoted by A, B, C and D. Thus, the expression for the input of the Data flip-flop, E, is given by:

$$\text{E} = \overline{A \cdot B \cdot C \cdot D} = \overline{A} + \overline{B} + \overline{C} + \overline{D} \tag{5.28}$$

Since, A is given by:

$$A = \overline{(Q_1 + Q_2) \cdot \text{IS\_0\_3} \cdot \text{SYNC}} \tag{5.29}$$

Thus,

$$\overline{A} = (Q_1 + Q_2) \cdot \text{IS\_0\_3} \cdot \text{SYNC} \tag{5.30}$$

Therefore, the top or the A signal branch is used for appending the SYNC signal to the Manchester encoder output during count 1 to 3.

Similarly for B, C and D:

$$\overline{B} = (\text{IS\_4\_7} + \text{IS\_8\_19}) \cdot \text{B\_ENCODED} \tag{5.31}$$

$$\overline{C} = \overline{Q}_1 \cdot \overline{Q}_2 \cdot \text{IS\_0\_3} \cdot \text{V}_{DD} \tag{5.32}$$

$$\overline{D} = Q_3 \cdot Q_5 \cdot \text{PARITY} \tag{5.33}$$

Hence, the B signal branch appends the buffer encoded signal (B_ENCODED) to the Manchester encoder output during count 4 to 19; the C signal branch is used to force the Manchester encoder output HIGH during count 0; and lastly, the D signal branch is used to attach the Parity bit to the Manchester encoder output during count 20. Thus, the Manchester encoder output is completely filled between the ripple counter count 0 to 20.

However, since the digital signal at E, before the data flip-flop, is constructed from the transition of many signals so it may not be clean of unwanted transition changes (or glitches) during each encode cycle. Thus, a data flip-flop (DFC1) is used to clock out the Manchester encoded output to remove any potential glitches in this digital signal.

5.3.2.8 Ripple Counter & RESET Signal

The most crucial element in any synchronisation circuit is a counter, which keeps track of the timing in an encode cycle. After each encode cycle is completed the clock is reset to time the next encode cycle. A negative-edge triggered binary ripple counter, Philips 74HC4024, was used in the synchronisation circuit implemented in Chapter 3. From the logic diagram in its datasheet, a binary counter could be constructed using toggle flip-flops and some NOT gates [1]. Thus, the overall digital circuit of the ripple counter was designed and is illustrated in Figure 5.47. The ripple counter is triggered using the MAIN_CLK signal.

The ripple counter used is a negative-edge triggered, 7-bit ripple counter. The negative-edge triggering is achieved by using a NOT-configured NAND gate at the input. Both the CLK and 2xCLK are incorporated into the ripple counter to ensure total synchronisation of the digital block. This is because some blocks in this digital design are triggered using the 2xCLK signal or its inverse which may cause the digital circuit to go out of synchronisation, especially when the resetting of the ripple counter is performed.
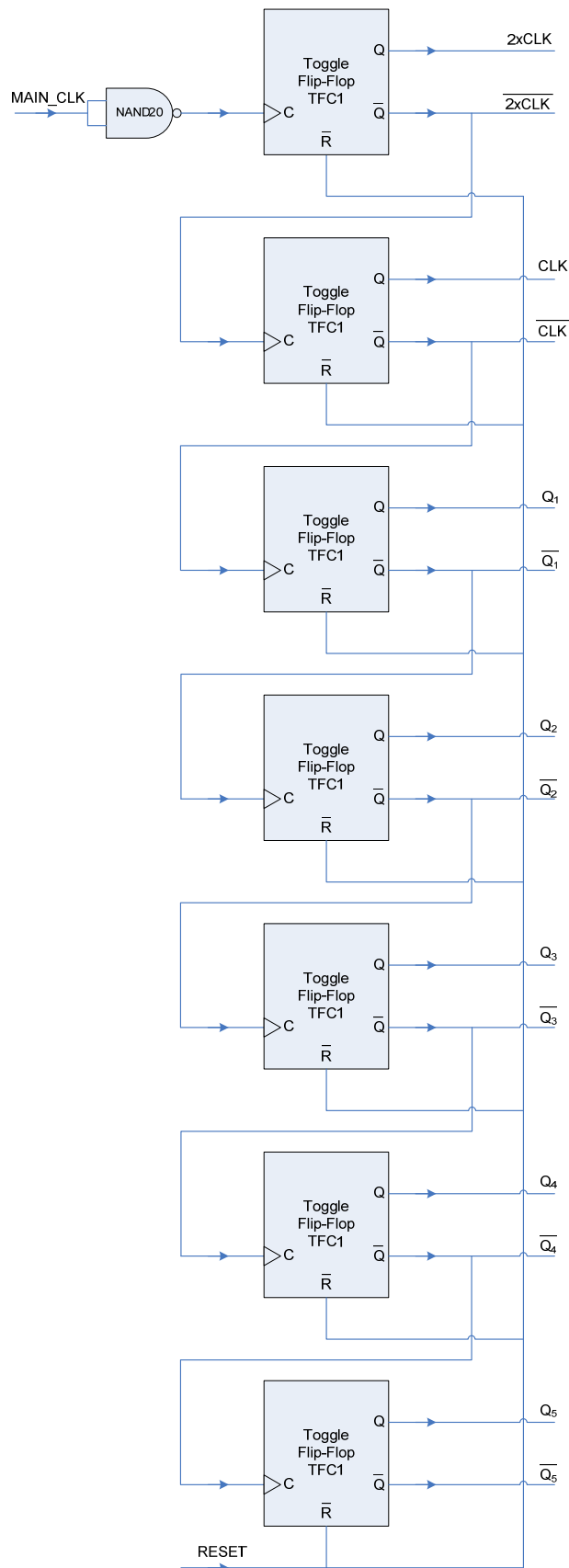
Figure 5.47 : The digital circuit of the ripple counter.

The reset of the encoding cycle is performed when the ripple counter reaches the count of 21. This corresponds to $Q_1 = Q_3 = Q_5 = $ HIGH, however since the flip-flops are reset using a logic '0'. Thus, we require a digital circuit to verify that the ripple count is **not** 21. This is shown in Figure 5.48.
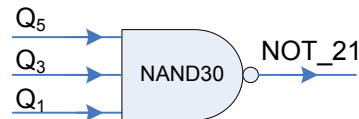
Figure 5.48 : The digital circuit to verify that the ripple count is **not** 21.

However by using only this circuit in Figure 5.48, the simulation shows that some flip-flops did not get reset due to a very short logic '0' duration of NOT_21. Thus, to extend this duration a data flip-flop is used to generate the RESET signal by holding the NOT_21 signal for one MAIN_CLK cycle (shown in Figure 5.49).
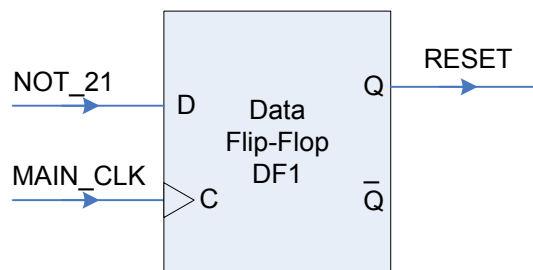
Figure 5.49 : The digital circuit used to create the RESET signal.

Furthermore, by considering that the required sampling frequency, f_s, of the heart sound signal is 2 kHz or kilo-samples per second. Thus, the MAIN_CLK signal frequency must be at least 320 kHz. This is derived from 2 signal channels and 20 bits per encoding cycle, giving 80 kHz for the CLK signal. While, MAIN_CLK signal is 4 times faster than the CLK signal. Using this MAIN_CLK frequency, the maximum frequency of the Manchester Encoder output is 160 kHz.

5.3.3 Simulation Results

A transient simulation of the overall digital circuit was conducted for 600 µs (just over 2 encode cycles) to verify the operation of the digital synchronisation circuit and the built-in Manchester encoder.

5.3.3.1 Ripple Counter, Ripple Count Verifiers, and RESET signal

Figure 5.50 illustrates the result of the transient simulation obtained for the 7-bit ripple counter designed. The input to the ripple counter is the MAIN_CLK signal – a 320 kHz square wave. The outputs are 2xCLK, CLK, Q_1, Q_2, Q_3, Q_4, Q_5, and their inverses. The red dotted line confirms the expected negative-edge trigger behaviour of the ripple counter, while the green dotted lines indicates the transition from count 20 to count 21, where the reset operation of the encoding cycle is expected to occur.

Figure 5.51 presents the result for the ripple count verifiers and the RESET signal, with respect to the ripple counter output Q_1. All the ripple count verifiers – IS_0_3, IS_4_7, IS_8_19 and NOT_21, all occurs at the correct locations, although with minor glitches in the digital output signal (indicated on the figure in red circles). The RESET signal also occurs at the correct location, from the NOT_21 logic '0' signal getting clocked into a data flip-flop by a positive-edge of the MAIN_CLK, and remains for one MAIN_CLK cycle.

5.3.3.2 ADC Control Signals & Data Buffer (B_DATA)

Figure 5.52 shows the result of the transient simulation for the analog-to-digital converter (ADC) control signals – the chip select $\overline{CS}$ and the digital input D_{IN}, and the 16-bit ADC Data Buffer signal (B_DATA), when the ripple counter output Q_1 is used to simulate the digital output signal D_{OUT}.

Both the ADC control signals and the 16-bit ADC Data Buffer signal occur at the expected locations and have the correct output patterns, for the input used.

5.3.3.3 Built-in Manchester Encoder

Figure 5.53 illustrates the result of the transient simulation for the built-in Manchester encoder, with the SYNC signal, Buffer Encode (B_ENCODED), the Parity bit, and the overall output (ENCODED) displaying the expected behaviour.
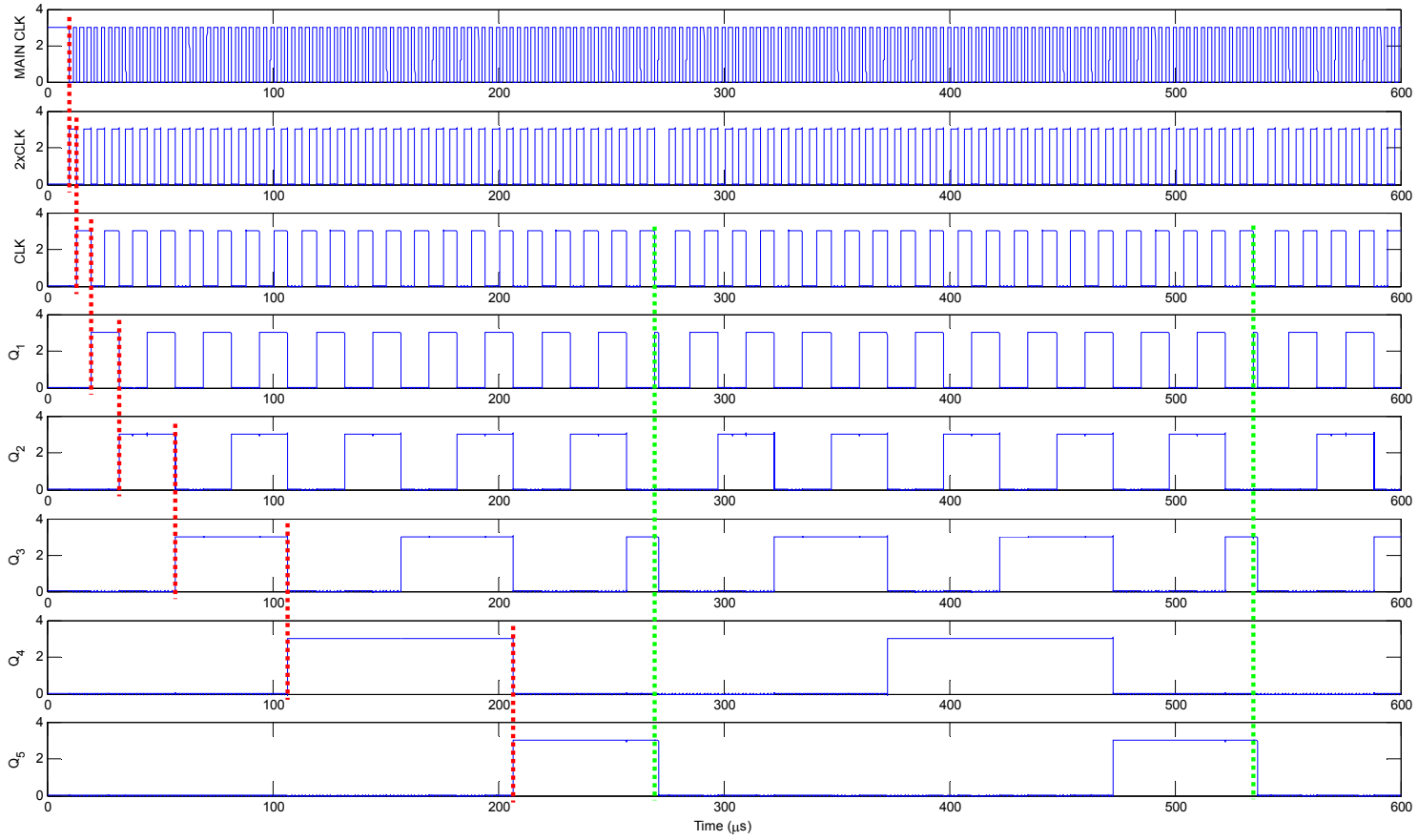
Figure 5.50: The transient simulation result of the designed 7-bit ripple counter for MAIN_CLK input and 2xCLK, CLK, Q_1, Q_2, Q_3, Q_4, and Q_5 outputs.
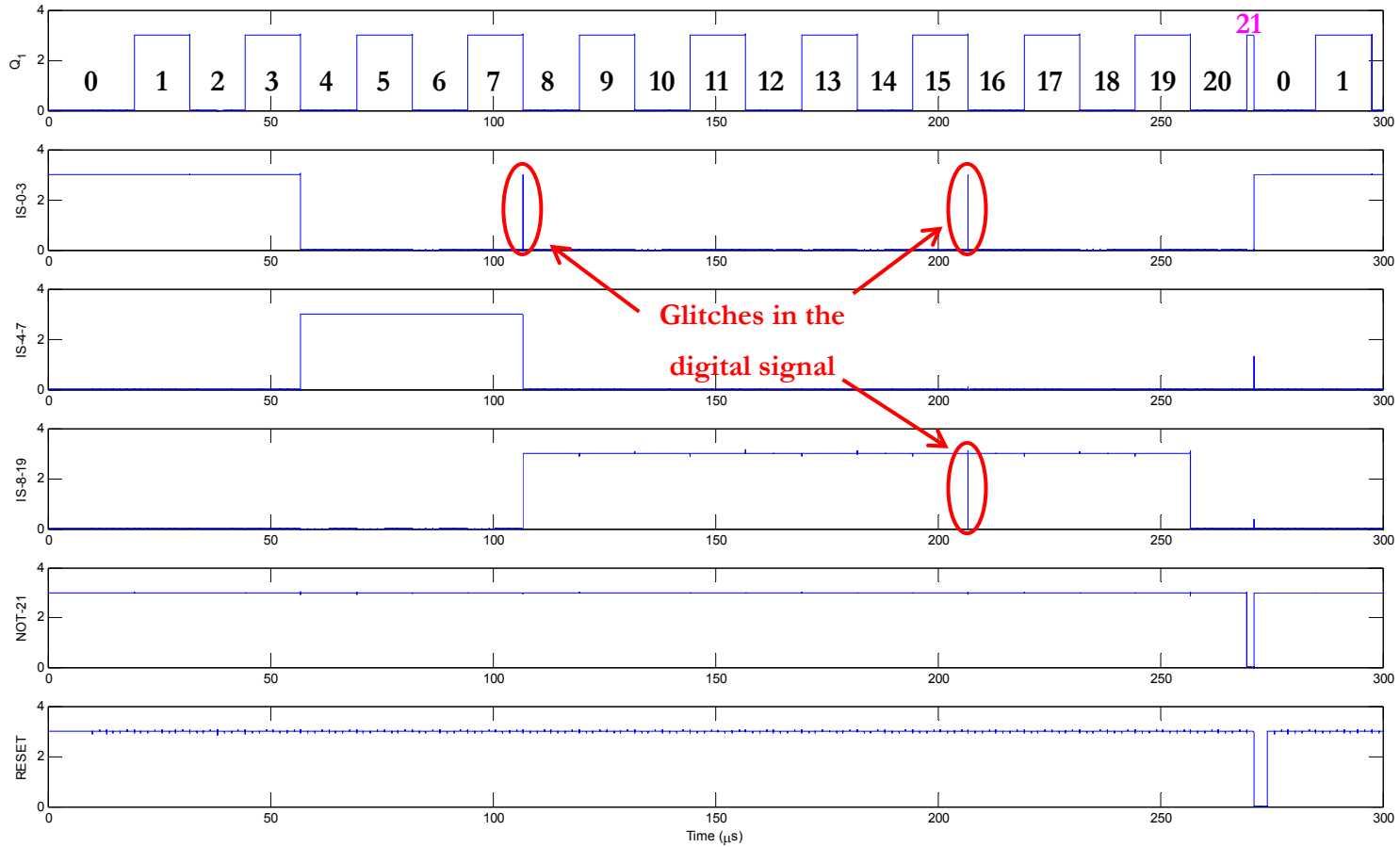
Figure 5.51: The transient simulation results of the designed ripple count verifiers IS_0_3, IS_4_7, IS_8_19 and NOT_21, and RESET signal. The red circles indicate the minor glitches observed in the digital signals.
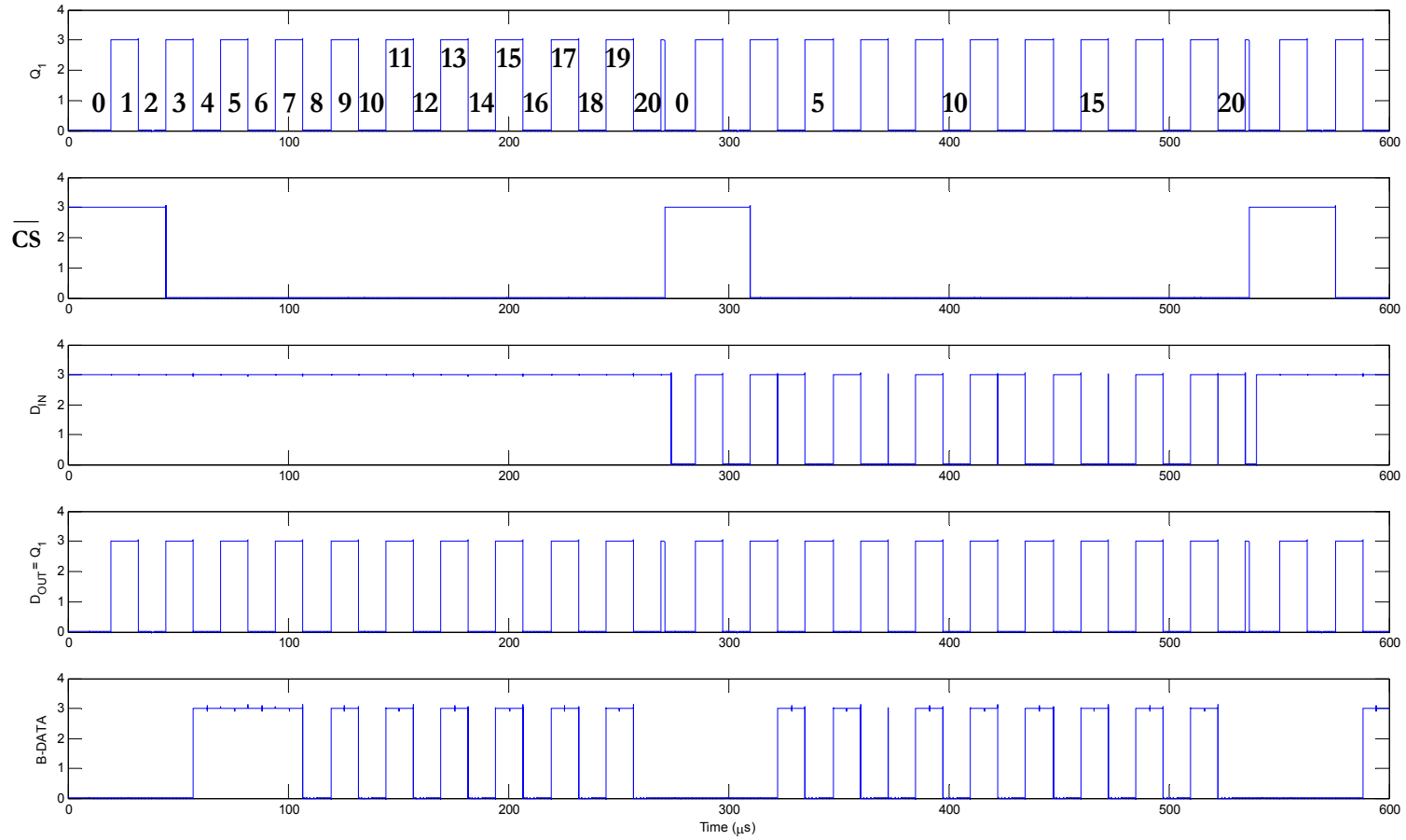
Figure 5.52: The transient simulation results of the ADC control signals – chip select $\overline{CS}$ and the digital input D_{IN}, and the 16-bit ADC Data Buffer (B_DATA), when the ripple counter output Q_1 is used to simulate the digital output signal D_{OUT}.
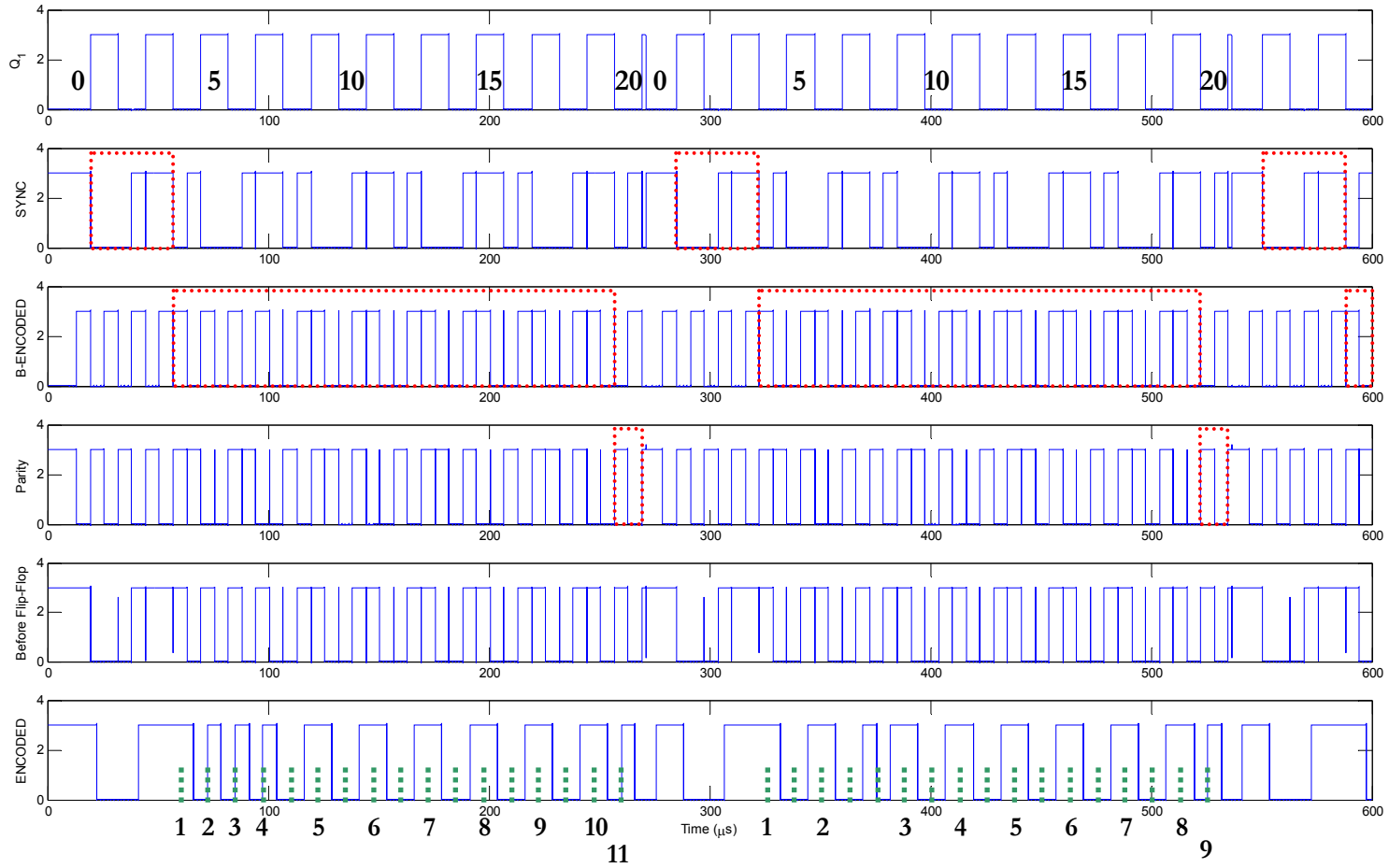
Figure 5.53: The transient simulation results of the built-in Manchester Encoder, with the portion of the interest indicated by red rectangles in SYNC, B_ENCODED and Parity. These portions forms the Manchester Encoder output signal (ENCODED), which contains many glitches before the flip-flop.5.53

The Manchester encoder output (ENCODED) is generated by appending the red rectangles portions of the SYNC, B_ENCODED and the Parity signals together. The ENCODED signal can be seen to be slightly delayed from the other signals because a data flip-flop was used to clock the signal out. The benefit of this is that the minor glitches seen in the signal prior to the data flip-flop were removed. However, there is a slight lag in ENCODED signal returning to a logic '1' after the encode cycle is completed, which is caused by a glitch in the signal point just prior to the data flip-flop which coincide with the time the flip-flop is being clocked.

The Parity bit is able to provide the extra logic '1' in both encode cycle. This is verified at the bottom of Figure 5.53, where the numbers of logic '1's were counted. In the 1st encode cycle, the B_ENCODED has 10 logic '1's with the 11th provided by the Parity bit. Similarly for the 2nd encode cycle, the B_ENCODED has 8 logic '1's with the 9th provided by the Parity bit.

5.3.4 Layout Considerations and Design

The layout design of each digital functional block was obtained from Austria Micro Systems (AMS) as part of its c35 core cells, as mentioned at the beginning of this section. However in digital circuit, we are dealing with logic '1's and '0's or V_{DD} and zero volts, thus no matching of the transistors are necessary. Therefore, the layout considerations of the MOS transistors mentioned in the analogue circuit design are not important for digital transistors.

However when we have a mixed-signal integrated circuit (IC) or where the analogue and digital circuits are integrated on to the same die, the important consideration is the interference between them. Since the switching of the digital circuitry causes a sudden change in voltages and currents, therefore considerable electrical noise and electromagnetic interference is generated at these transitions of the digital signal and can be coupled into the substrate. Furthermore, the voltages and currents used in the analogue parts are normally very small, thus they are especially vulnerable to noise from the digital part of the IC.

The issues and the layout techniques for mixed-signals ICs is discussed in detail by Tsividis [16]. In this thesis, only a few of the recommended techniques were employed to reduce any possible interference between the analogue and the digital part of the circuit:

1) Common power supply and ground buses were avoided,

2) Power supply and ground pads and metal tracks were wider than normal, and

3) Both p^+ and n-well guard rings were introduced.
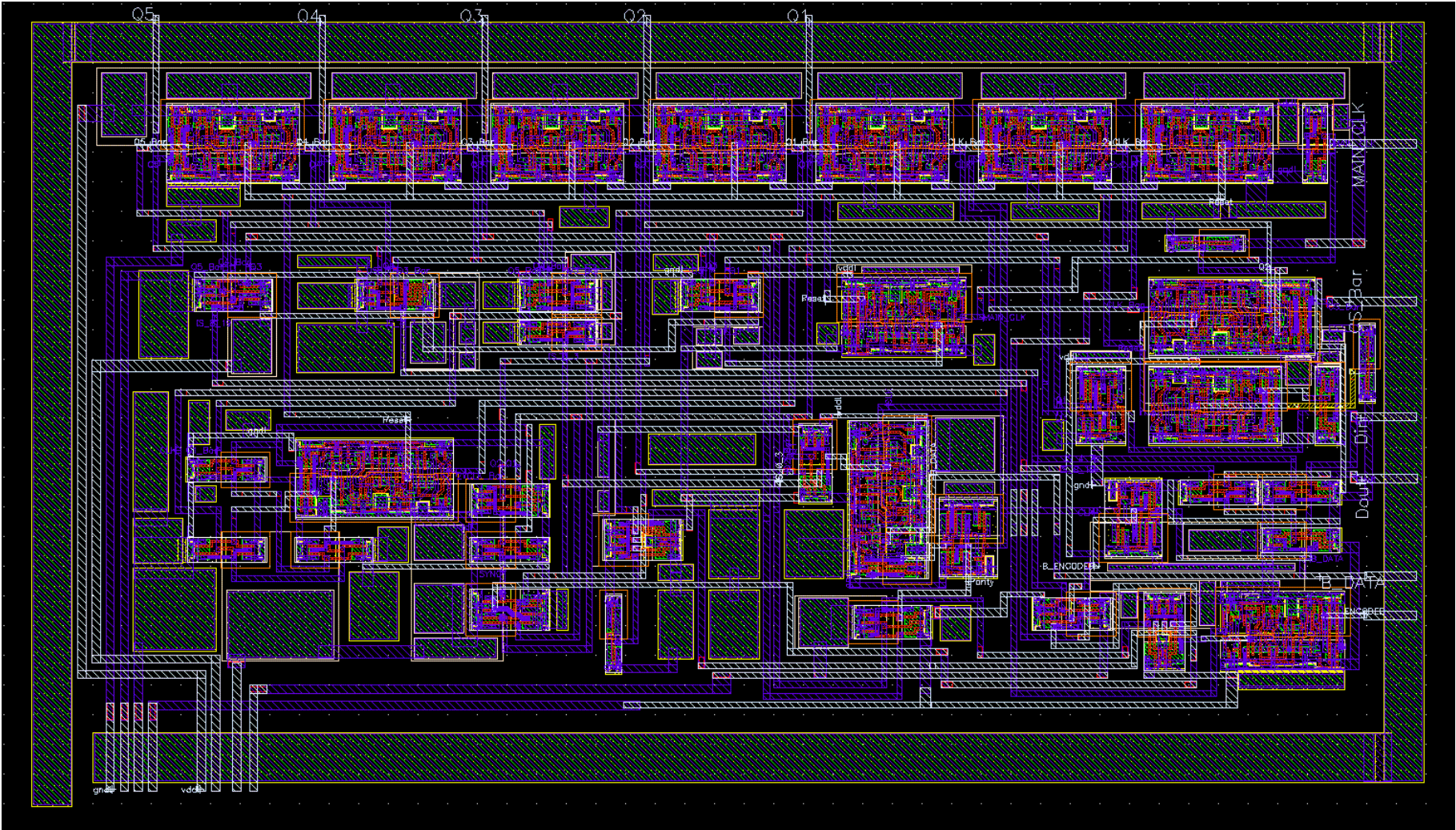
Figure 5.54: The overall layout design for the digital synchronisation circuit and the built-in Manchester Encoder, with a p$^+$ guard ring surrounding it.
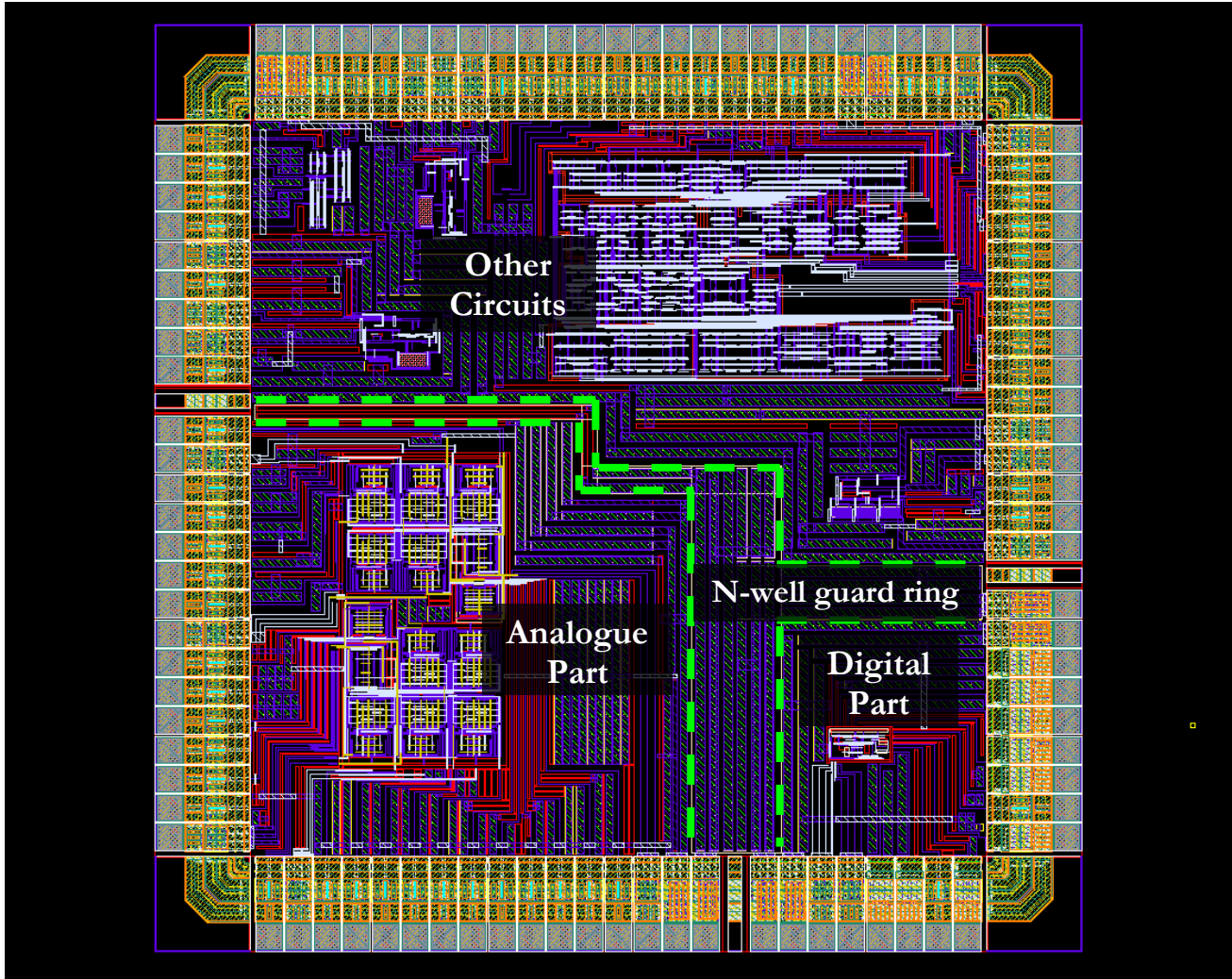
Figure 5.55: The overall layout design of the whole mixed-signals chip and the locations of the (partial) n-well guard rings highlighted in green.

The power supply and ground to the digital and the analogue circuit were connected to different pads and in a different section of the chip. This is important to prevent the noise in the digital supply and ground, caused by fast digital switching, from affecting the analogue supply and ground. In our case, the power supply of the digital and the analogue parts were naturally separated because they are of different voltages – the analogue supply was 1 V, while the digital supply was 3 V.

Furthermore, the wide variant of the zero ohm bonding pad and wider metal tracks inside the chip were used to interface between the external power supply and ground, and the IC's internal circuit. This is to minimise the resistance path between them.

The guard rings were introduced to guard against the effect of capacitive substrate coupling. This capacitive coupling can be caused by varying voltages, wiring and pads. By having grounded p^+ guard ring near the source and the receiver of the interference, this greatly reduces their resistance path to ground at the source and the receiver and thus the interference observed at these locations. Figure 5.54 illustrates the overall layout design for the digital synchronisation circuit and the built-in Manchester Encoder, with a p^+ guard ring.

Additionally, an n-well guard ring can also be introduced to stop the flow of surface substrate currents. In this mixed-signals IC, a full n-well ring, similar to the p^+ guard ring illustrated in Figure 5.54, was not used. However, a 3 V, partial n-well guard ring was implemented to partition the digital circuit and the analog circuit from each other and from other circuits on the chip. Figure 5.55 shows the overall layout design of the whole mixed-signals chip and the locations of the (partial) n-well guard rings constructed highlighted in green.

5.3.5 Integrated Circuit (IC) Testing & Results

The digital circuit presented in Figure 5.54 was sent for fabrication alongside the analogue circuit. The only test that was completed on the digital circuit is the timing test for the ADC control signals – the chip select $\overline{CS}$ and the digital input D_{IN}, the 16-bit ADC Data Buffer signal (B_DATA), and the Manchester encoder output (ENCODED). This test was conducted on four different ICs – Chip A, B, C and D. All four ICs produce the same results.

Figure 5.56 presents the result obtained from the timing test. It is a picture of the oscilloscope screen, showing the time trace for four signals. The top, yellow trace is the chip select $\overline{CS}$ signal. The pink trace is the digital input D_{IN}; the cyan trace is the Manchester encoder output (ENCODED); and the bottom, green trace is the 16-bit ADC Data Buffer signal (B_DATA).
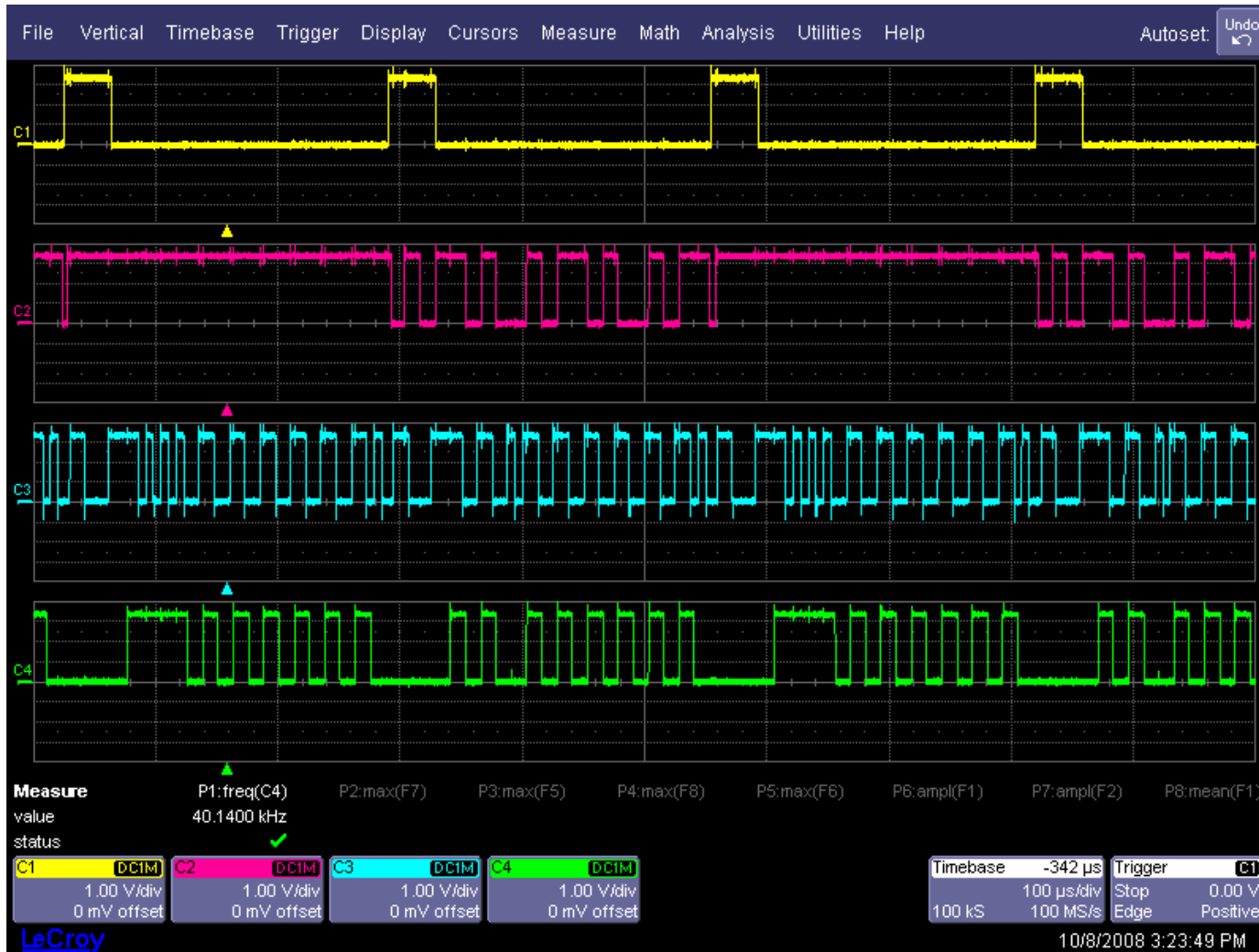
Figure 5.56: The result of the timing test of the fabricated digital circuit, where the yellow, cyan, pink and green traces represent the chip select $\overline{CS}$ signal, the digital input D_{IN}, the Manchester Encoder output (ENCODED), and the 16-bit ADC Data Buffer signal (B_DATA), respectively.

By comparing the traces in Figure 5.56 with the simulated results in Figure 5.52 and 5.53, it can be seen that the fabricated digital circuit can reproduce the simulated digital behaviour for the ADC control signals and the Manchester Encoder output, when the ripple counter output Q_1 is used to simulate the digital output D_{OUT} of the ADC.

5.4 Conclusion

In this chapter, a novel mixed analog-digital integrated circuit (IC) has been designed in Cadence, fabricated on Austria Micro Systems (AMS) 0.35 μm CMOS C35B4C3 3.3V 2P/4M technology and tested. The analogue component of this chip is a pair of 4th order Gm-C filters with off-chip capacitors. While the digital component is a synchronisation circuit designed to control the analog-to-digital conversion of the analogue heart sound data using the Linear Technology LTC1288 ADC and to perform the Manchester encoding on the digital output of the ADC.

A new implementation of a CMOS weak-inversion multi-tanh triplet transconductor was presented in this chapter to construct the Gm-C filter for the signal conditioning of heart sounds and murmurs. This CMOS weak-inversion multi-tanh triplet transconductor operates from a 1V power supply and consumes 8 nA of current when the bias current, I_{bias}, of the transconductor is 1 nA. Five of these transconductors were required to construct each Gm-C filter – three of which is used to construct a capacitively loaded gyrator to simulate a floating gyrator and two to simulate a grounded inductor. In total, the power consumption is less than 100 nW per Gm-C filter.

The fabricated 4th order Gm-C filters exhibit good low frequency response, linearity (2nd harmonic distortion (HD_2)) and inter-modulation distortion (IMD). However, the measured upper cut-off frequency (400 Hz) is reduced dramatically from the simulated value (about 700 Hz). This is believed to be associated with the non-ideal and tolerances of the off-chip capacitors, the capacitance and the inductance of the integrated circuit pads required to connect the Gm-C filter with external components, and the non-ideal simulation of inductors by the capacitively loaded gyrators. Nevertheless, the upper cut-off frequency of 400 Hz is acceptable for heart rate monitoring.

The digital component was constructed using logic gates and flip-flops circuit and layout design provided by Austria Micro Systems (AMS) as part of its c35 core cells. The logic gates,

flip-flops, their total number used, and the approximate power consumption when operating at 320 kHz is presented in Table 5.9. A total of 37 digital functional blocks was required to construct the digital circuit, which requires a total of 6.72 μW of power, when all the functional blocks are running at 320 kHz. Thus, the overall power consumption of the fabricated integrated circuit is expected to be less than 10 μW. The testing of the fabricated digital circuit showed that it behaves in the same manner as in the simulation.

Figure 5.57 presents a picture of the fabricated prototype mixed-signals integrated circuit (IC) designed and tested in this chapter.

Table 5.9: The digital functional blocks used in the digital circuit, the total number of each block used and the total estimated power consumption at 320 kHz

Digital Functional Blocks	Total Number used	Power Consumption at 320 kHz (μW)
2-input NAND (NAND20)	10	0.58
3-input NAND (NAND30)	5	0.34
4-input NAND (NAND40)	2	0.15
3-input NOR (NOR30)	1	0.09
2-input XOR (XOR20)	2	0.22
2-input XNOR (XNR20)	1	0.08
2-input OR into 2-input NAND (OAI210)	2	0.08
2-input OR into 3-input NAND (OAI2110)	1	0.08
Data flip-flop (DF1)	2	0.73
J-K Flip-Flop with active LOW clear (JKC1)	1	0.41
Toggle Flip Flop with active LOW clear (TFC1)	8	3.12
Toggle Flip Flop with active HIGH enable and active LOW clear (TFEC1)	2	0.84
TOTAL	**37**	**6.72**
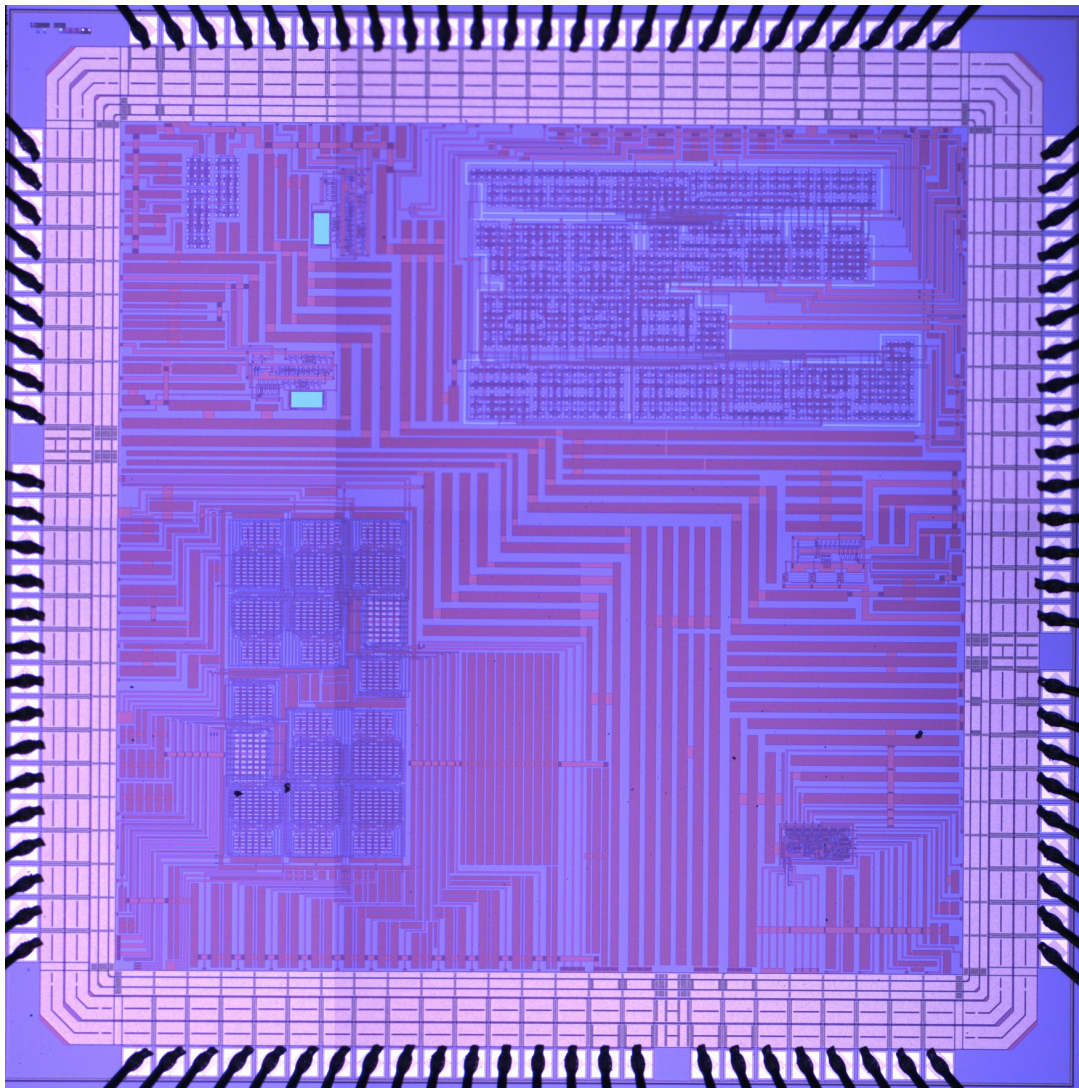
Figure 5.57: A microscope picture of the fabricated prototype mixed-signals integrated circuit (IC) designed and tested.

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Chapter 6

Conclusion

6.1 Contributions

In this work, the development of a novel non-invasive, low-power, phonocardiographic (PCG) or heart sound sensor suitable for wireless long-term monitoring of heart rate has been presented. Since the aim of this sensor is for it to be suitable for long-term monitoring, thus the development process has focused extensively on its power consumption and size (similar to a 50p coin), as well as the ambient acoustic noise which remains a major obstacle in the field of PCG.

To tackle the issue of ambient acoustic noise, a novel 2-channel de-noising algorithm, called Interference Suppression via Spectral Suppression (ISSC) based on the 1-channel Spectral Subtraction algorithm, was introduced in Chapter 4. This noise cancellation algorithm was able to compete and in many cases provide a superior performance compared to the Wavelet Thresholding technique, which has become widely used and studied on heart sound recordings by many researchers, on a variety of heart sounds tested.

Furthermore, the issue of power consumption and size was addressed in Chapter 5 where a prototype of a mixed analog-digital integrated circuit (IC) was designed, fabricated and tested. The analogue part of the IC consists of a pair of 4th order Gm-C analogue signal conditioning filters. These Gm-C filters were build using a new implementation of the multi-tanh triplet transconductors, fabricated on Austria Micro Systems (AMS) 0.35 μm CMOS C35B4C3 3.3V

2P/4M technology, that are combined to form capacitively loaded gyrators that mimic the behaviour of inductors. Each of these Gm-C filters consumes about 100 nW of power, and has a dynamic range of 62 dBs at 1% of total harmonic distortion (THD). By integrating these two analogue signal conditioning filters into the IC, the space for 4 operational amplifiers was saved, along with about 2 mW of power. The space and power consumption saving is even more pronounced in the digital part of the IC, where the space taken up previously by 6 discrete, off-the-shelf ICs is saved, along with about 36 mW of power. The digital part of the IC consists of the digital synchronisation circuit, that drives the operation of the analog-to-digital converter (ADC) – the Linear Technology LTC1288, and the Manchester encoder, that allows for error detection in the radio transmission process. The integrated digital circuit is estimated to consume less than 7 µW of power at the operating frequency of 320 kHz.

However, it should be noted that the designed and fabricated mixed-signals IC was not tested with the system level design of the sensor platform and thus the overall operation of the sensor with the fabricated IC has not been verified.

6.2 Publication

[1]   T. Tosanguan, R. J. Dickinson, and E. M. Drakakis, "Modified spectral subtraction for de-noising heart sounds: Interference Suppression via Spectral Comparison," in *Biomedical Circuits and Systems Conference, 2008. BioCAS 2008. IEEE* 2008, pp. 29-32.

6.3 Future Work

Although, this work has examined a number of aspects with regards to the development of the non-invasive, wireless, long-term sensor for monitoring of heart rate, however a number of other aspects have been overlooked due to the constraints within this work. The possible areas that the author believes that further work can be done are as follows:

- The development of the proposed sensor is still incomplete with the final sensor yet to be manufactured, thus no in-situ testing has been done to identify any potential problems in the interfacing between the sensor and the human chest either when the person is at rest or in motion. Therefore, substantial contributions can be made in this area to perfect the physical interfacing of the sensor to allow good sound transmission and minimal effect from motion (such as motion artefact) while maintaining a small size and unobtrusiveness nature of the sensor.

- The de-noising algorithm can be looked at in more detail. This may include the use of real heart sounds from patients to ascertain and compare the performances of the different noise cancellation techniques, the extension to include more noise cancellation techniques such as the 2-channel Wavelet Thresholding and the independent component analysis technique (ICA), the comparison of the relative performances of different noise cancellation techniques when the recording is done in real environments such as in a bus, on a tube, on a street, or in a hospital bed. Furthermore, the possibility of integrating these de-noising algorithms into a micro-controller for real-time noise cancellation at the sensor can also be examined.

- The aspect of radio communication can be investigated in greater detail. This is because the radio communication block has a large implication on both the power consumption and the size of the sensor, since it is now the most power hungry device after the integration of the signal conditioning filters, the digital synchronisation circuit and the Manchester encoder into the IC. Also, the minimum size of the sensor is restricted by the size of the antenna. This may result in a development of a specialised, shorter range (in tens of metres) radio transmitter or transceiver that consume less than 1-2 mA of current.

- Furthermore, the miniaturisation of the whole sensor can be examined, to include the phonocardiographic (PCG) transducers or the microphones on to MEMS, the instrumentation amplifiers, and the 12-bit analog-to-digital converter (ADC), in addition to the signal conditioning Gm-C filters, the digital synchronisation circuit and the Manchester encoder performed in this work.

- Additionally, it may be beneficial to examine the networking aspects of long-term monitoring systems – the transfer of information and the data storage. Since the benefit of long-term monitoring can only be reaped if the information is stored to build up a track record of the patient, reviewed, and used by medical staff to assist in the diagnosis or treatment of medical conditions. This will likely involve, for heart sounds, the determination of the minimum number of bits ADC and the sampling frequency which will allow simple heart rate monitoring, useful diagnosis of heart sounds and murmurs, and the monitoring of replacement valves; the tradeoffs and recommendations between these different configurations; and the likely potential application of long-term heart sound monitoring systems.

Appendix A

Analog-to-Digital Converter Architectures

There are many ADC architectures which include direct conversion, successive approximation, delta-encoded, ramp-compare, pipeline, and sigma-delta:

Direct-conversion or flash ADCs (Figure 1) are very fast, but usually have a low resolution of 8 or less because it requires large and expensive circuit to drive [2]. They are often used for video or other fast signals.

a)
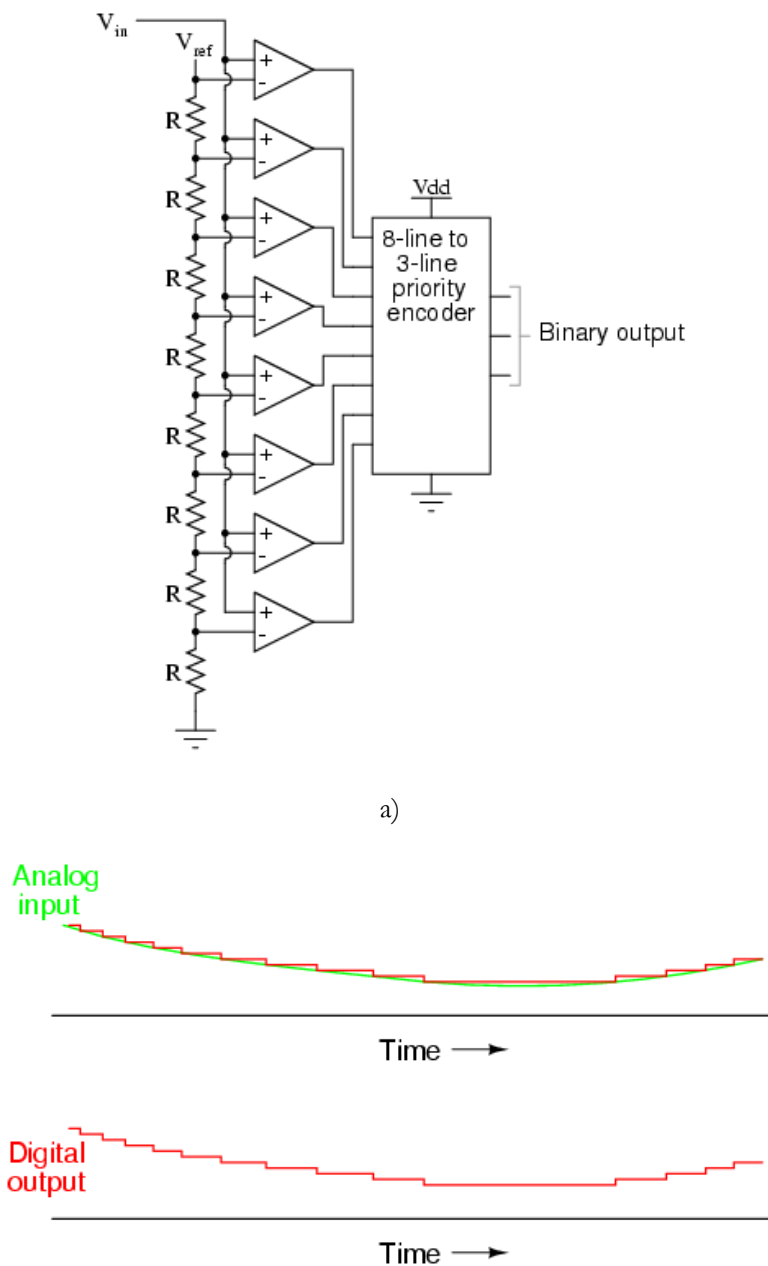
Figure 1: a) A 3-bit Flash ADC circuit, and b) Operation of Flash ADC [1].

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Successive approximation (SAR) ADCs are very popular in data-acquisition systems, especially when multiple channels require input multiplexing [3]. The input signal is held constant by a sample-and-hold (SHA) circuit (Figure 2 a)) during the conversion cycle. A number of comparisons are performed between the input and an internally generated signal to produce the digital output. The basic algorithm used in the successive-approximation ADC conversion process can be traced back to the 1500s. It is related to the solution of a useful mathematical puzzle—the determination of an unknown weight by a minimal sequence of weighing operations (Figure 2 b)).
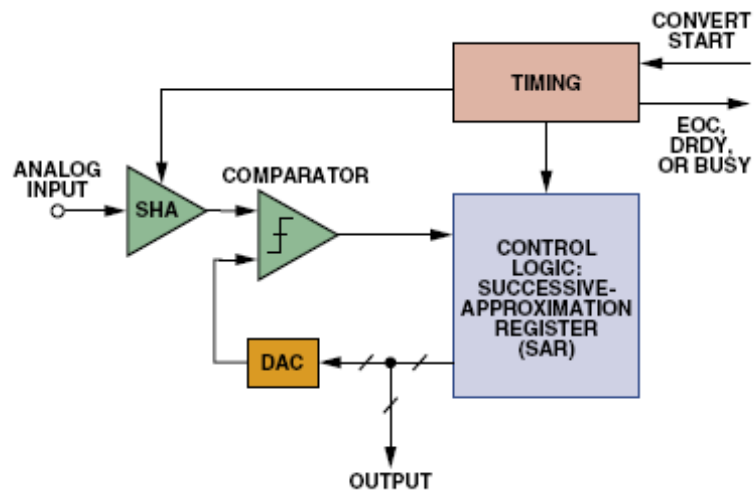
a)
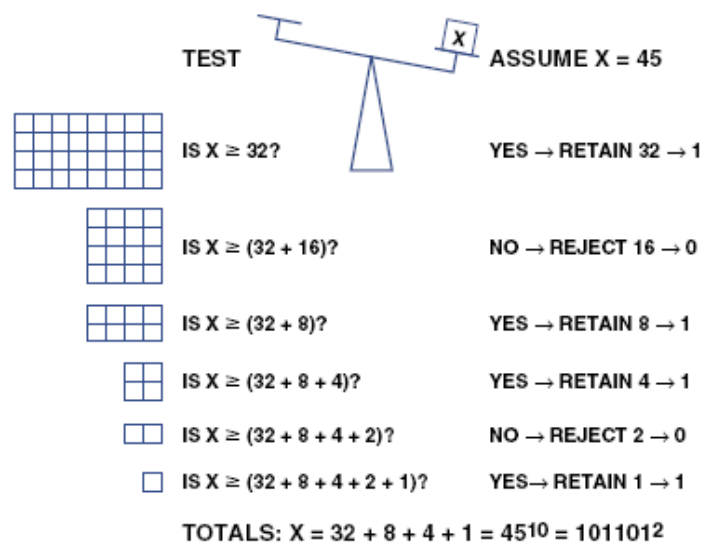
b)

Figure 2: a) Block diagram of a basic Successive Approximation ADC, b) Successive-approximation ADC algorithm for a balance scale and binary weights [3].

Delta-encoded ADCs have very wide ranges and high resolution, but the conversion time is not fixed and is input dependent, though the worst case is stated and is guaranteed [2]. This architecture is suitable for slowly changing signal or they can be combined with a SAR to perform on faster signals.

Ramp-compare or integrating ADCs utilises an integrator op-amp circuit to generate a saw-tooth waveform which is compared to the input signal. A timer is started when the ramp starts and once the amplitude of ramp is equal to the input, the timer is stopped and read out. However, due to the nature of this ADC the sampling frequency is not constant and depends on the input signal, like the delta-encoded case.

Pipeline ADCs divides the input signals into at least two subranges. A coarse conversion is first performed on the signal, followed by a finer comparison of the input with an internal digital-to-analog converter (DAC). The results are then combined (Figure 3). This type of ADCs is very fast (>1Msps) and has a high resolution, though due to its design a minimum sampling frequency is also stated.
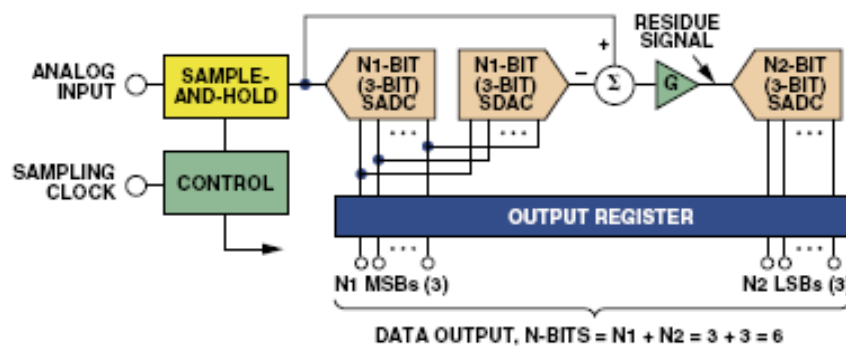
Figure 3: 6-bit, two-stage subranging - Pipeline ADC [3].

Sigma-Delta ADCs have in general replaced the ramp-compare ADCs, with regards to applications requiring high resolution and sampling frequency of a few hundred Hz [3]. Normally in an over-sampling ADC, the input is oversampled by a large factor so that the quantization noise is uniformly spread over the bandwidth. And because the bandwidth sampled is larger than signal bandwidth so the quantization noise inside the signal bandwidth is less. In a Sigma-Delta ADC, a sigma-delta modulator is used to oversample the input signal; this has the effect of shaping the quantization noise towards the higher frequencies (Figure 4).
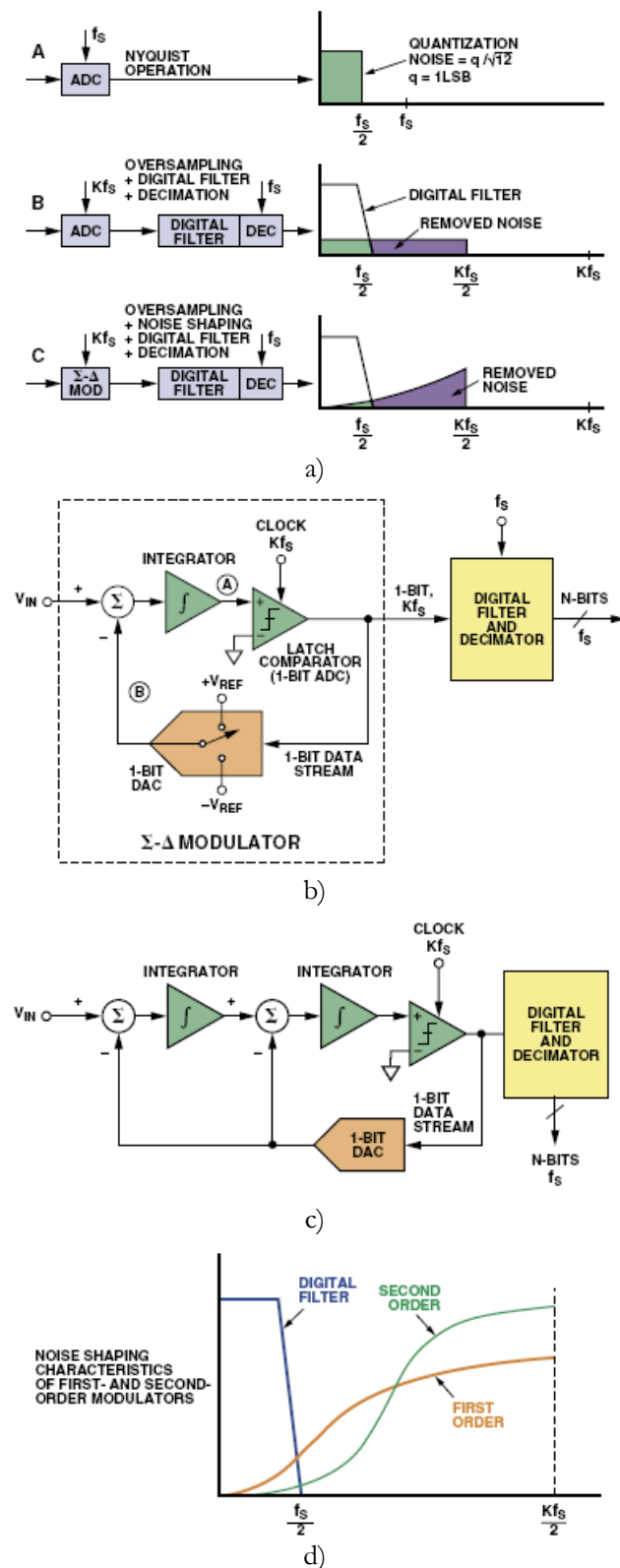
Figure 4: a) Quantisation noise comparisons between a normal ADC, oversampling ADC, and Sigma-Delta ADC, b) First order Sigma-Delta (modulator) ADC, c) Second order Sigma-Delta (modulator) ADC, and d) Noise shaping characteristics of First order and Second order modulator [3].

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Appendix B

Components Identified in the System Level Design

1. Radio Modules

General ISM

Manufacturer	Model No.	Description	Freq. (MHz.)	Data rate (kbps)	Range (m)	Modulation	Operating Voltage (V)	Current Consumption			Dimensions (mm)
								TX (mA)	RX (mA)	Sleep (μA)	
Chipcon	CC1150	Transmitter*	315/433/868/915	1.2-500	n/a	2-FSK, GFSK, MSK,	1.8-3.6	15.9 @ 0dBm	n/a	200 nA	4 x 4
Chipcon	CC1100	Transceiver	315/433/868/915	1.2-500	n/a	and ASK/OOK	1.8-3.6	28.8 @ 10dBm	15.6 (433)	400 nA	4 x 4
Texas Instr.	TRF6903	Transceiver	315/433/868/915	64/32	n/a	FSK, OOK	2.2-3.6	30 @ -2dBm	20 (315)	0.6	5.5 x 5.5
Analog	ADF7020	Transceiver	433/868/915	200/64	n/a	FSK, GFSK, ASK, OOK, GOOK	2.3-3.6	19.1 @ 0dBm	19/21	0.1	7 x 7
Analog	ADF7025	Transceiver	433/868/915	384	n/a	FSK, GFSK	2.3-3.6	19.3 @ 0dBm	19/21	0.1	7 x 7
Analog	ADF7011	Transmitter*	433/868	76/9.6	n/a	FSK, GFSK, ASK, OOK	2.3-3.6	19 @ 0dBm	n/a	0.2	7.8 x 6.4
Analog	ADF7012	Transmitter*	315/433/868/915	179/64	n/a	FSK, GFSK, ASK, OOK, GOOK	2.3-3.6	16 @ 0dBm	n/a	0.1	7.8 x 6.4
Analog	ADF7901	Transmitter*	369/395	50	n/a	OOK, FSK	3	21 @ 10dBm	n/a	0.2	7.8 x 6.4
Chipcon	CC2250	Transmitter*	2.4 GHz.	1.2-500	n/a	2-FSK, MSK	1.8-3.6	22.8 @ 0 dBm	n/a	200 nA	4 x 4
Chipcon	CC2200	Transceiver	2.4 GHz.	1.2-500	n/a	2-FSK, MSK	1.8-3.6	21.6 @ 0 dBm	15.6	500 nA	4 x 4
Atmel	ATR2406	Transceiver	2.4 GHz.	1152	n/a	GFSK	2.9-3.6	500 μA	625 μA	<1	5 x 5
								@ 10kbps	@ 10kbps		
Nordic	nRF9E5	SOC	433/868/915	50	n/a	GFSK	1.9-3.6	19 @ 2 dBm	12.5	<2.5	5 x 5

Radio Modules (continued)

General ISM

Manufacturer	Model No.	Description	Freq. (MHz.)	Data rate (kbps)	Range (m)	Modulation	Operating Voltage (V)	Current Consumption			Dimensions (mm)
								TX (mA)	RX (mA)	Sleep (µA)	
Radiometrix	UHF TX2	Transmitter*	433	160	75/300	FM	2.2-4 or 4-6	4 @ 0dBm	n/a	n/a	32 x 12 x 3.8
Radiometrix	UHF TX3A	Transmitter*	869/914	64	75/300	FM	2.2-16	7.5 @ 0 dBm	n/a	n/a	32 x 12 x 3.8
Radiometrix	UHF RX2	Receiver	433	n/a	75/300	FM superhet	3-6	n/a	13	n/a	48 x 17.5 x 4.5
Radiometrix	UHF RX3A	Receiver	869/914	n/a	75/300	FM superhet	2.7-16	n/a	11	n/a	48 x 17.5 x 4.5
Radiometrix	UHF BiM2	Transceiver	433	160	50/200	FM	3.3 or 5	14 @ 10dBm	18	<1	33 x 23 x 4
Radiometrix	UHF BiM3A	Transceiver	868	64	50/200	FM	2.7-6	8.2 @ 2.5dBm	10.6	<10	33 x 23 x 5

Bluetooth

Manufacturer	Model No.	Description	Freq. (MHz.)	Data rate (kbps)	Range (m)	Modulation	Operating Voltage (V)	Current Consumption			Dimensions (mm)
								TX (mA)	RX (mA)	Sleep (µA)	
Texas Instr.	BRF6150	Single Chip	2.4 GHz.	1Mbps	n/a	n/a	2.7-5.4	25	37	30 (shut 6)	4.5 x 4.5
Texas Instr.	BRF6300	Single Chip	2.4 GHz.	2-3Mbps	n/a	DQPSK, 8PSK	1.7-5.4	n/a	n/a	n/a	4.5 x 4.5
CSR	BlueCore4	SOC	2.4 GHz.	2-3Mbps	n/a	DQPSK, 8PSK	1.8-3.6				6 x 6

Radio Modules (continued)

Zigbee

Manufacturer	Model No.	Description	Freq. (MHz.)	Data rate (kbps)	Range (m)	Modulation	Operating Voltage (V)	Current Consumption			Dimensions (mm)
								TX (mA)	RX (mA)	Sleep (μA)	
Chipcon	CC2420	Transceiver	2.4 GHz.	250	??	DSSS	2.1-3.6	17.4 @ 0dBm	19.7	1	7 x 7
CompXs	CX1540	Transceiver	2.4 GHz.	250	??	O-QPSK	2.4 - 3.0	56	57	1	7 x 7
Freescale Sem.	MC13192/3	Transceiver	2.4 GHz.	250	??	O-QPSK	2.0-3.4	30 @ 0dBm	37	1 (hibernate)	5 x 5

RFID

Manufacturer	Model No.	Description	Freq. (MHz.)	Data rate (kbps)	Range (m)	Modulation	Operating Voltage (V)	Current Consumption			Dimensions (mm)
								TX (mA)	RX (mA)	Sleep (μA)	
Texas Instr.	TMS37126	Transceiver	120-140 kHz	4	2	AM	1.8-3.6	28μA	28μA	5.3	7.8 x 4.4 x 1.15
EM Micro	EM4083	Receiver	115-140 kHz	4	>2.5	AM	3	<2μA	<2μA	<2μA	5 x 6.4 x 1.1
Atmel	U3280M	Transceiver	100-150 kHz	10	2	AM	2-6.5	40μA	40μA	0.4	5 x 6 x 1.7
Atmel	AT88RF001	Transceiver	13.56 MHz	106	2	BPSK	2.1-2.5	130-240μA	130-240μA	130-240μA	10 x 6.2 x 1.75

2. Antennae

Manufacturer	Frequency (MHz.)	Azimuth	Impedance (Ohm)	Dimensions (mm)
PHYCOMP	433	Omni	50	6.8 x 37.5 x 0.90
PHYCOMP	868	Omni	50	16.5 x 14 x 0.90
PHYCOMP	2450	Omni	50	8.0 x 3.5 x 0.90
PHYCOMP	2450	Omni	50	7.35 x 5.5 x 1.3
Linx Tech.	315/418/433/868/916	n/a	50	1.102" x 0.54" x 0.062"
Linx Tech.	2450	Omni	50	6.5 x 2.2 x 1.0
TriCome	315	Omni	50	
TriCome	433	Omni	50	30 x 7 x 1.8
TriCome	868	Omni	50	30 x 7 x 1.8
TriCome	2450	Omni	50	16 x 5 x 1.8
Perseus Tech.	430		50	15 x 2 x 1.2
Perseus Tech.	2450	Omni	50	5.2 x 2 x 1.32
	RFIDs			
Premo	125 kHz		n/a	various
Neosid	125 kHz		n/a	15.5 x 15.5 x 3.5
Copytag	13.56 MHz		n/a	35 x 34

3. Analog-to-Digital Converters

Manufacturer	Model No.	Description	Max Fs. (ksps)	Resolution (bits)	No. of Channels	INL (LSBs)	Operating Volt. (V)	Internal Reference	Current Consumption Active (mA)	Sleep (μA)	Dimensions (mm)
					Single, Dual						
Linear Tech.	LTC1860/1L	1-/2-channel	150	12	1 (1860L), 2 (1861L)	1	2.7-3.6	N	0.02 @ 2ksps	10	3 x 4.9 MSOP
Maxim-Dallas	MAX1287/9	2 or True diff.	150	12	2 (1287), diff (1289)	1	2.7-3.6	N	0.002 @ 1ksps	0.2	3 x 3
Maxim-Dallas	MAX144/145	2 or Pseudo-diff	108	12	2 (144), diff (145)	0.5	2.7-5.25	N	0.02 @ 2ksps	0.2	3 x 5
Maxim-Dallas	MAX1241	Single	133	12	1	0.5	2.7-5.25	2.5V	0.04 @ 2ksps	5	5 x 6.2
Microchip	MCP3201	differential	50 @ 2.7V	12	1	1	2.7-5.5	N	0.2	0.5	3 x 4.9 TSSOP
Analog	AD7466	Single	200	12	1	1.5	1.6-3.6	N	0.01 @ 10ksps	0.1	3 x 3 SOT23
Analog	AD7457	Pseudo Diff.	100	12	pseudo diff	1	2.7-5.25	N	0.1 @ 20ksps	1	3 x 3
Analog	AD7992	I2C Interface	188	12	2 channel	1	2.7-5.5	N	0.15	1	3 x 4.9
Burr-Brown	ADS7866	Single	200 @ 1.6V	12	1	1.5	1.2-3.6	N	0.04 @ 20ksps	0.008	3 x 3
Burr-Brown	ADS1286	differential	20	12	1	1	4.5-5.25	N	0.045 @ 2ksps	3	5 x 6.2
Burr-Brown	ADS7822	Pseudo Diff.	75	12	1	0.25 C	2-3.6	N	0.006 @ 2ksps	3	3 x 5 MSOP
Burr-Brown	ADS7829	Pseudo Diff.	125	12	1	0.4 (IB)/0.8	2-3.6	N	<0.02 @ 7.5ksps	3	3 x 3

Analog-to-Digital Converters (continued)

Manufacturer	Model No.	Description	Max Fs. (ksps)	Resolution (bits)	No. of Channels	INL (LSBs)	Operating Volt. (V)	Internal Reference	Current Consumption Active (mA)	Sleep (μA)	Dimensions (mm)
					Multi						
Linear	LTC1594/8L	optional filter	10.5	12	4 (1594L), 8 (1598L)	3	2.7-3.6	N	0.04 @ 2ksps	n/a	10 x 6.2
Maxim-Dallas	MAX1245	uni- or bi-polar	100	12	8-single or 4-diff	0.5	2.375-3.3	N	0.1 @ 2ksps for 8	1	7 x 7.8
Microchip	MCP3204/8	single or diff.	50 @ 2.7V	12	4 (3204), 8 (3208)	1 (B)	2.7-5.5	N	0.2	0.5	10 x 6.2
Analog	AD7994	I2C Interface	188	12	4 channel	0.5	2.7-5.5	N	0.15	1	5 x 4.5
Analog	AD7998	I2C Interface	188	12	8 channel	0.5	2.7-5.5	N	0.15	1	5 x 4.5
Burr-Brown	ADS7844	single or diff.	200	12	8-single or 4-diff	1	2.7-5	N	0.08 @ 2ksps for 8	3	6.5 x 8.2 QSOP
Burr-Brown	ADS7870	data acquisition	52	12	8-single or 4-diff	2	2.7-5.5	1.15/2.0/	0.6 @ 2ksps for 8	1	6.5 x 8.2 SSOP
Burr-Brown	ADS7828	I2C Interface	50	12	8-single or 4-diff	1	2.7-5.5	2.5	0.15	0.4	3.1 x 6.6

4. Operational Amplifiers

Manufacturer	Model No.	Comment	GBP	Slew Rate	Voffset	Vnoise	Operating	Current Consumption	
				V/ms	±µV	nV/rtHz.	Volt. (V)	Active (µA)	Shutdown (µA)
Maxim-Dallas	MAX4197	Single Instrument.	3.1 kHz @ -3db (Gain = 100)	60	50-225	8.7 @ 10kHz	2.7-7.5	93	8
	MAX4091/2/4	Single/Dual/Quad	500 kHz.	200	30-1400	12 @ 10kHz	2.7-6	165 per	n/a
	MAX4199	Single Differential	45 kHz @ -3db (Gain = 10)	70	15-400	38 @ 10kHz	2.7-7.5	42	6.5
	MAX4162/3/4	Single/Dual/Quad	200 kHz	115	500-3/4/5000	80 @ 1kHz	2.7-10	25 per	n/a
	MAX480	Single	20 kHz	5-12	25-140	70 @ 1kHz.	1.6-3.6	15 max	n/a
	MAX478/9	Dual/Quad	50 kHz	25	30-90/30-120	49 @ 1kHz	2.2-30	17 max per	n/a
	MAX4240-4	Single-Quad	90 kHz	40	200-1400	70 @ 1kHz.	1.8-5.5	10 per	1 per
	ICL761/2/3/4X	S/D/T/Q	44 kHz	16	2000	100 @ 1kHz	2-16	15 max per	n/a
	MAX4464/74	Single/Dual	40 kHz	20	500-7000	150 @ 1kHz	1.8-5.5	0.6 per	n/a
	MAX4289	Single	17 kHz	6	200-2000	n/a	1-5.5	9	n/a
	MAX409/17/19	Single/Dual/Quad	150 kHz	80	500/3000/4000	150 @ 1kHz	2.5-10	1.2	n/a
Linear Tech.	LT6013/4	Single/Dual	1.4 MHz	200	10-35	9.5 @ 1kHz	2.7-36	145 per	n/a
	LTC6078/9	Dual/Quad	750 kHz	50	7-25	18 @ 1kHz	2.7-5.5	54 per	n/a
	LT1466/7L	Dual/Quad	120 kHz	40	110-390	45 @ 1kHz	2-10	75 max per	n/a
	LT2078/9	Dual/Quad	200 kHz	70	30-70/35-110	28 @ 1kHz	(2.2)-30	50 max per	n/a
	LT2178/9	Dual/Quad	85 kHz	40	30-70/35-110	49 @ 1kHz	(2.2)-30	17 max per	n/a

Operational Amplifiers (continued)

Manufacturer	Model No.	Comment	GBP	Slew Rate V/ms	Voffset ±µV	Vnoise nV/rtHz.	Operating Volt. (V)	Current Consumption Active (µA)	Shutdown (µA)
Linear Tech.	LT1672/3/4	Single/Dual/Quad	12 kHz	1.6-5	200-475	185 @ 100Hz	2.2-30	2 max per	n/a
	LT1636	Single	200 kHz	70	50-225	52 @ 1kHz	2.7-44	42	n/a
	LT1490/1A	Dual/Quad	180 kHz	60	110-500	50 @ 1kHz	2.0-44	40 per	n/a
	LT1077	Single	250 kHz	80	9-40	27 @ 1kHz	2.2-30	48	n/a
ST Micro	TS931/2/4	Single/Dual/Quad	100 kHz	50	2000 max	75	2.7-10	20 per	n/a
	TS1851/2/4	Single/Dual/Quad	480 kHz	180	1000 max	40	1.8-6	120 per	n/a
	TS941/2/4	Single/Dual/Quad	10 kHz	3-4.5	2000 max	n/a	2.5-10	1.2 per	n/a
National	LMV751	Single	4.5 MHz	2000	50-1500	6.5 @ 1kHz	2.7-5	500	n/a
	LMV771/2/4	Single/Dual/Quad	3.5 MHz	1400	300-850	7.5 @ 10 kHz	2.7-5	550	n/a
	LMC6572/4	Dual/Quad	220 kHz	10-30	3500 max	45 @ 1kHz	2.7-3	40 per	n/a
	LMV422	Dual	27 kHz (low)	8-14	4000 max	60 @ 1kHz	2.7-5.5	2 per	n/a
	LMC6022/4	Dual/Quad	350 kHz	110	9000 max	42 @ 1kHz	5-15	40 per	n/a
Analog	OP777/27/47	Single/Dual/Quad	700 kHz	200	20-100// 30-160	15 @ 1kHz.	2.7-30	300 max per	n/a
	OP8603/7/9	Single/Dual/Quad	400 kHz	100	12-50	25 @ 1 kHz	1.8-5	50 max per	n/a
	OP281/481	Dual/Quad	95 kHz	25	1500 max	75 @ 1kHz	2.7-12	4 max per	n/a

Operational Amplifiers (continued)

Manufacturer	Model No.	Comment	GBP	Slew Rate	Voffset	Vnoise	Operating	Current Consumption	
				V/ms	±μV	nV/rtHz.	Volt. (V)	Active (μA)	Shutdown (μA)
Analog	OP193/293/493	Single/Dual/Quad	35 kHz	15	75/100/125 max	65 @ 1kHz	1.7-36	15 per	n/a
	OP290	Dual	20 kHz	12	125-500	n/a	1.6-36	20 max per	n/a
Texas Instr.	TLV2460-5	Single/Dual/Quad	5.2 MHz	1600	500-1500	11 @ 1kHz	2.7-6	500 per	n/a
	TLV2242	Dual	46 kHz	20	300-2000	23 @ 1kHz	2.7-10	50 per	n/a
	TLV2252/4	Dual/Quad	187 kHz	100	200-850	19 @ 1kHz	2.7-8	34 per	n/a
	OPA4/2/244	Quad/Dual/Single	430 kHz	100	1500 max	22 @ 1kHz	2.2-36	50 per	n/a
	TLV2711	Single	56 kHz	25	400-3000	21 @ 1kHz	2.7-10	11 per	n/a
	OPA2/349	Dual/Single	70 kHz	20	2000-10000	300 @ 1kHz	1.8-5.5	1 per	n/a
	LPV321/358/324	Single/Dual/Quad	152 kHz	100	1200-7000	178 @ 1kHz	2.7-5	9 per	n/a
	TLV2381/2	Single/Dual	160 kHz	100	500-4500	90 @ 1kHz	2.7-16	7 per	n/a
	TLV2322/4	Dual/Quad	27 kHz	20	1100-9000	68 @ 1 kHz	2-8	12 per	n/a
	TLC1078/9C	Dual/Quad	85 kHz	32	160-450	68 @ 1kHz	1.4-16	20 per	n/a
	TLC252	Dual	12 kHz	100	2000 max	25 @ 1kHz	1.4-16	300 per	n/a
	TLV2401/2/4	Single/Dual/Quad	5.5 kHz	2	1500 max	800 @ 1kHz.	2.5-16	<1 per	n/a

5. Microphones

Manufacturer	Model no.	Directivity	Supply	RF Filtering	Sensitivity	Noise	Output Imp.	Max. Current	Frequency	Dimension
			Voltage		(dB re 1V/Pa)	dBA SPL	(Ohm)	Drain (mA)	Range	(mm)
Knowles	SPM0102ND3	Omni	1.5-5.5V	Standard	-42	<35	<100	0.25	?	4.72 x 3.76 x 1.50
Acoustic	SPM0102NE3	Omni	1.5-5.5V	Enhanced	-42	<35	<100	0.25	?	4.72 x 3.76 x 1.50
	SPM0103ND3	Omni	1.5-5.5V	Standard	-22	<35	<100	0.35	?	4.72 x 3.76 x 1.50
	SPM0103NE3	Omni	1.5-5.5V	Enhanced	-22	<35	<100	0.35	?	4.72 x 3.76 x 1.50
	MBXXYYASC-1	Omni	1.5-3V	?	-42 to -40	n/a	<2.2k	0.5	100-10,000	XX (dia) x YY (thickness)
	MBXXYYUSC-1	Uni	1.5-3V	?	-47 to -42	n/a	<2.2k	0.5	100-10,000	XX (dia) x YY (thickness)
	MBXXYYNSC-1	Noise Canceling	1.5-3V	?	-45 to -42	n/a	<2.2k	0.5	100-10,000	XX (dia) x YY (thickness)
	FG-3329/3629	Omni	0.9-1.6V	Some	-33	<30	2.8k-6.8k	0.05	100-10,000	2.565 (dia) x 2.565
	FG-3742	Omni	0.9-1.6V	Some	-43	<30	2.8k-6.8k	0.05	100-10,000	2.565 (dia) x 2.565
	NR-3158/60/5994	Bi-directional	1.5-10V	Noise Canceling	-38/-44/-38	<30	4.4k	0.05	100-10,000	5.56 x 3.98 x 2.26
	NR-3159	Bi-directional	1.5-10V	Noise Canceling	-52	<30	2.5k	0.2	100-10,000	5.56 x 3.98 x 2.26
	EL	Cardiod, Super-C	1.5-10V			<26				4 x 5.59 x 2.28

Microphone (continued)

Manufacturer	Model no.	Directivity	Supply	RF Filtering	Sensitivity	Noise	Output Imp.	Max. Current	Frequency	Dimension
			Voltage		(dB re 1V/Pa)	dBA SPL	(Ohm)	Drain (mA)	Range	(mm)
Sonion	SiMic	Omni	1.6-3.65V		-40	<35	5k	0.35	50-8,000	2.4 x 1.35 x 0.89
	100M Series	Omni	0.9-10V	Yes	-33	<26	2k-6k	0.05	100-10,000	many config
	Series 93/94M	Omni	0.9-10V	Yes	-36	<27	2.8k-6.8k	0.05	100-10,000	5.15 x 3.63 x 2.28
JL World	HBC06A/B/C	Noise Cancelling	3-10V	n/a	-45	n/a	Low	0.5	100-10,000	6 (dia) x 2.7 ©
	HBC10A	Noise Cancelling	1.5-10V	n/a	-45	n/a	Low	0.5	100-10,000	9.7 (dia) x 5
	HMC05A	Noise Cancelling	3-10V	n/a	-45	n/a	Low	0.5	100-10,000	4.5 (dia) x 3
	HMC06A/B/C	Noise Cancelling	3-10V	n/a	-45	n/a	Low	0.5	100-10,000	6 (dia) x 1.6 (D)
	HBO06B/K/L	Omni	3-10V	n/a	-45	n/a	Low	0.5	50-16,000	6 (dia) x 1.8 (L)
	HBO06G/H	Omni	3-10V	n/a	-45	n/a	Low	0.5	50-16,000	6 (dia) x 2.7 (H)
	HBO06Q	Omni	3-10V	n/a	-44	n/a	Low	0.5	50-16,000	8.8 (dia) x 1.6
	HMO05A	Omni	3-10V	n/a	-45	n/a	Low	0.5	100-10,000	4.5 (dia) x 3
	HBO0603B-60	Omni	3-10V	n/a	-40	n/a	Low	0.5	30-16,000	6 (dia) x 3.5
	HBU06A/B/C	Uni	3-10V	n/a	-45	n/a	Low	0.5	100-10,000	6 (dia) x 2.7 ©
	HMU06A/B/C	Uni	3-10V	n/a	-45	n/a	Low	0.5	100-10,000	6 (dia) x 2.7 ©
	HMU08A	Uni	3-10V	n/a	-45	n/a	Low	0.5	100-10,000	8 (dia) x 5

Appendix C

Truth Tables of the Digital Functional Blocks

1. Flip-flops

1.1 J-K flip-flops with active LOW clear

Negative-edge triggered J-K flip-flops
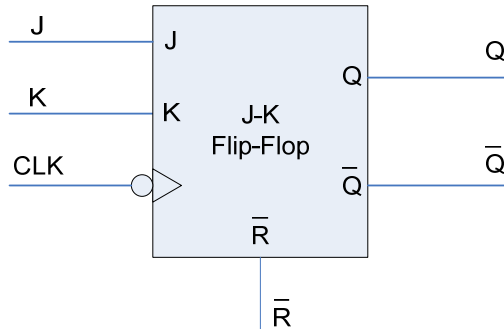
Inputs				Outputs	
J	K	CLK	$\overline{R}$	Q_n	$\overline{Q}_n$
0	0	⌐⌐	1	Q_{n-1}	$\overline{Q}_{n-1}$
0	1	⌐⌐	1	0	1
1	0	⌐⌐	1	1	0
1	1	⌐⌐	1	$\overline{Q}_{n-1}$	Q_{n-1}
X	X	X	0	0	1

Key:

    X – Don't Care

Positive-edge triggered J-K flip-flops
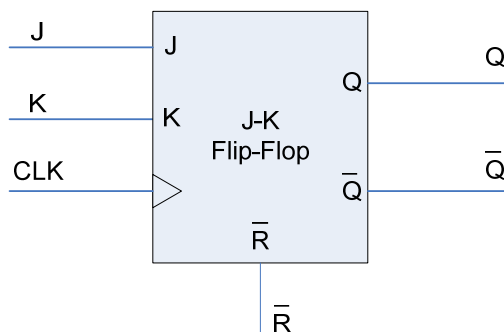
The above truth table also applies for the positive-edge triggered flip-flop, however the transition occurs at the positive edge ⌐ of the CLK.

1.2 Toggle flip-flops with active HIGH enable and active LOW clear
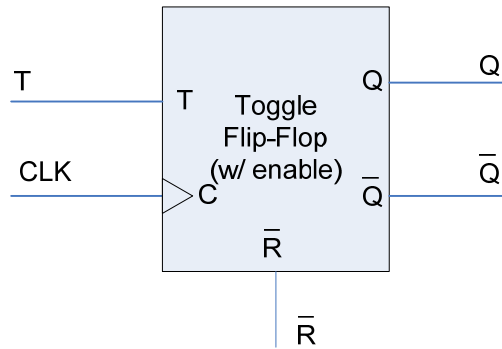
Inputs			Outputs	
T	CLK	$\overline{R}$	Q_n	$\overline{Q}_n$
0	⭡	1	Q_{n-1}	$\overline{Q}_{n-1}$
1	⭡	1	$\overline{Q}_{n-1}$	Q_{n-1}
X	X	0	0	1

1.3 Toggle flip-flops with active LOW clear
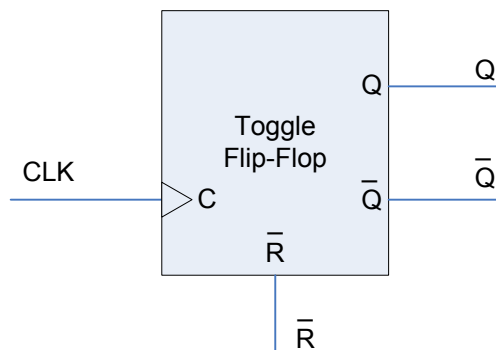
Inputs		Outputs	
CLK	$\overline{R}$	Q_n	$\overline{Q}_n$
⭡	0	$\overline{Q}_{n-1}$	Q_{n-1}
X	1	0	1

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1.4 Data flip-flops
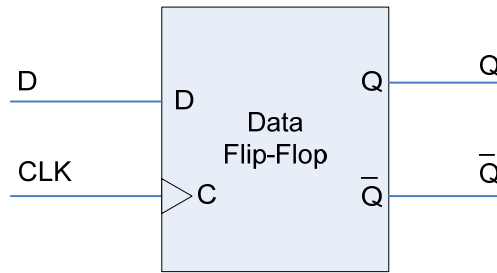
Inputs		Outputs	
D	CLK	Q_n	$\overline{Q}_n$
0	⤒	0	1
1	⤒	1	0

2. Logic Gates

2.1 AND gates
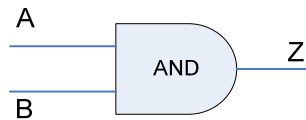
Inputs		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

The principle of the 2-input AND gate can be applied to multi-input AND gate, where the output will only be logic '1' when ALL the inputs are logic '1's.

2.2 NAND gates
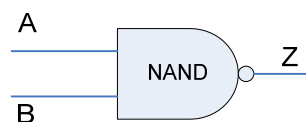
Inputs		Output
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

The principle of the 2-input NAND gate can be applied to multi-input NAND gate, where the output will only be logic '0' when ALL the inputs are logic '1'.

2.3 OR gates
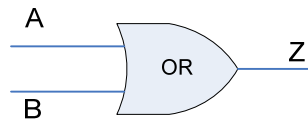
Inputs		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

The principle of the 2-input OR gate can be applied to multi-input OR gate, where the output will be a logic '1' when at least one of the inputs is a logic '1'.

2.4 NOR gates
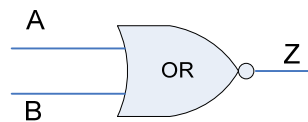
Inputs		Output
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

The principle of the 2-input NOR gate can be applied to multi-input NOR gate, where the output will be a logic '0' when at least one of the inputs is a logic '1'.

2.5 Exclusive-OR (XOR) gates

Inputs		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

2.6 Exclusive-NOR (XNOR) gates
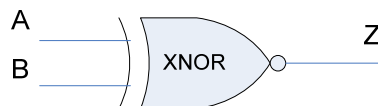
Inputs		Output
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

2.7 NOT gate
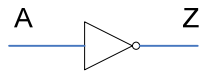
Input	Output
A	Z
0	1
1	0

Appendix D

Final Circuit Diagram of the System Level Design

1. 3.3V Regulated Power Supply

2. Signal Conditioning Block

SPM0103ND3

3.3V

Main
Microphone

0.68 μF

SPM0103ND3

3.3V

Reference
Microphone

0.68 μF

2.7 kΩ

INA118

Ref

47 kΩ   47 kΩ

3.3V

1 μF   1 μF

18 kΩ

3.3V

MAX492

15 kΩ

1/2

1.6V

220 Ω   220 Ω

1 μF

3.3V

MAX492

0.68 μF

2/2

0.1 μF

3.3V

LMS3983ITL-1.6

C1   V$_{OUT}$ V$_{IN}$ C3

Enable   A1

G$_{ND}$ B2

0.1 μF
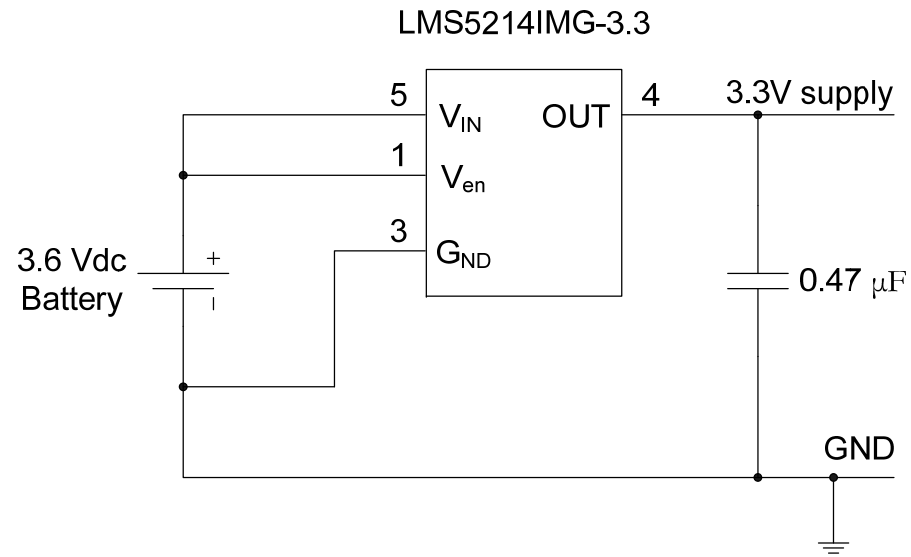
SIGNAL
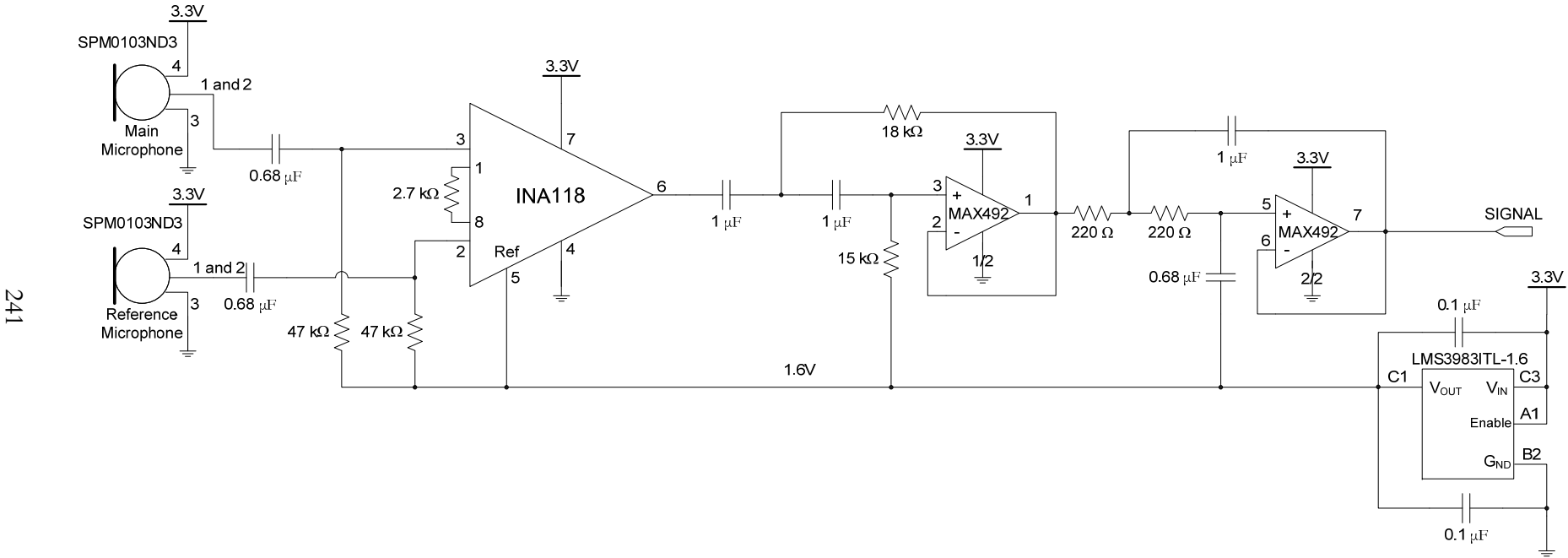
3. Clock generator, Analog-to-Digital Converter and Manchester Encoder

LTC6906

3.3V

6 V+ OUT 1   fCLK = 80 kHz   MAIN CLK

N.C. — 3 DIV GRD 5

2 GND SET 4

390 kΩ

3.3V

HI-15530 Encoder

24 VDD $\overline{\text{BIPOLAR}}$ 17
     $\overline{\text{ONE OUT}}$

22 SEND CLK

ENABLE   19 ENCODER ENABLE $\overline{\text{BIPOLAR}}$ 15   ENCODED DATA
     $\overline{\text{ZERO OUT}}$

BUFFERED DATA   18 SERIAL DATA IN

20 SYNC SELECT

MR   13 MASTER RESET

12 GND   SEND DATA 21   SEND DATA

3.3V

LTC1285

8 V+ D_{OUT} 6   DIGITAL DATA

1 VREF

SIGNAL   2 IN+

1 μF   3 IN-

Q1   7 CLK

$\overline{\text{CS}}$ 5 $\overline{\text{CS}}$

4 GND
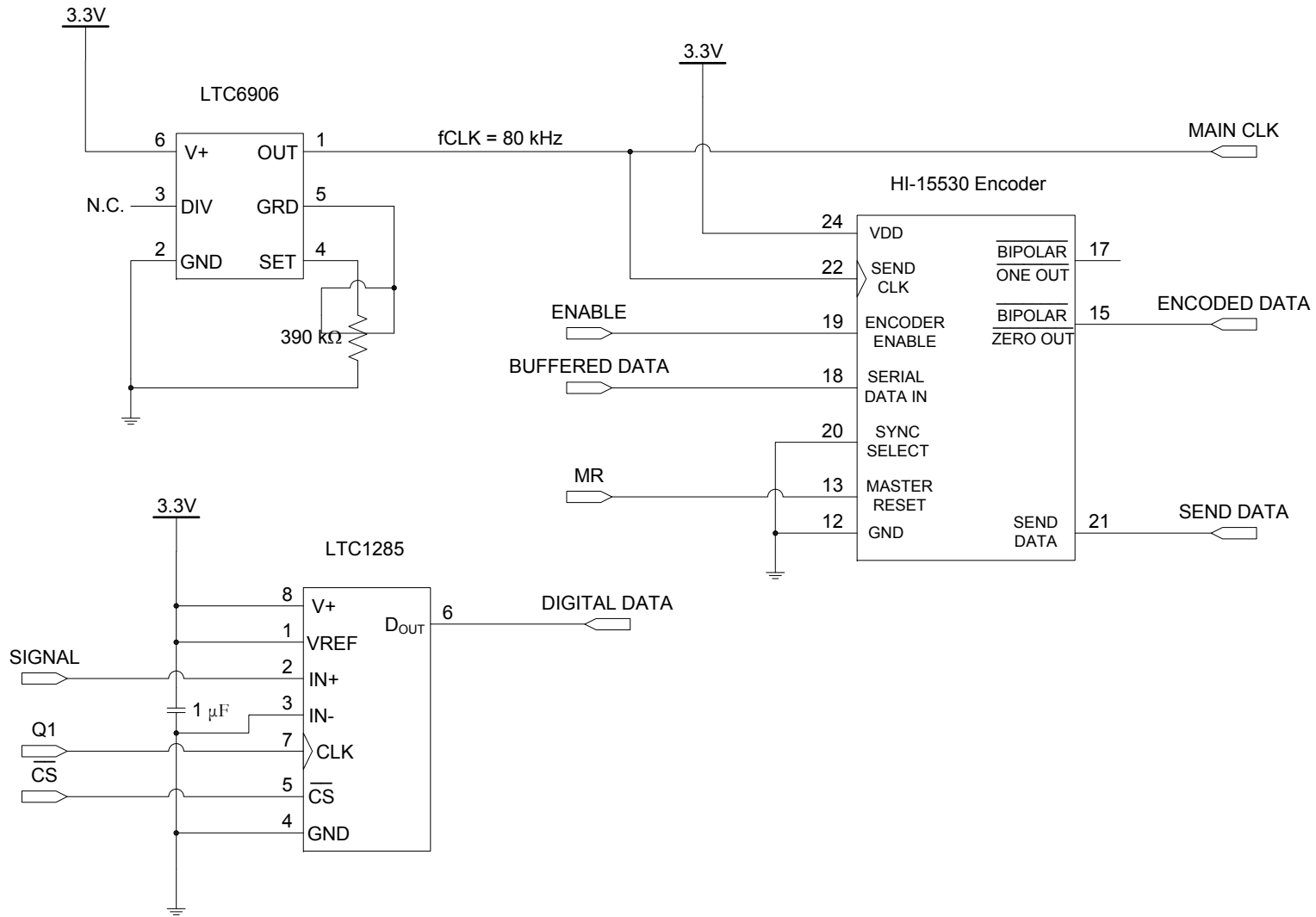
4. Synchronisation Circuit
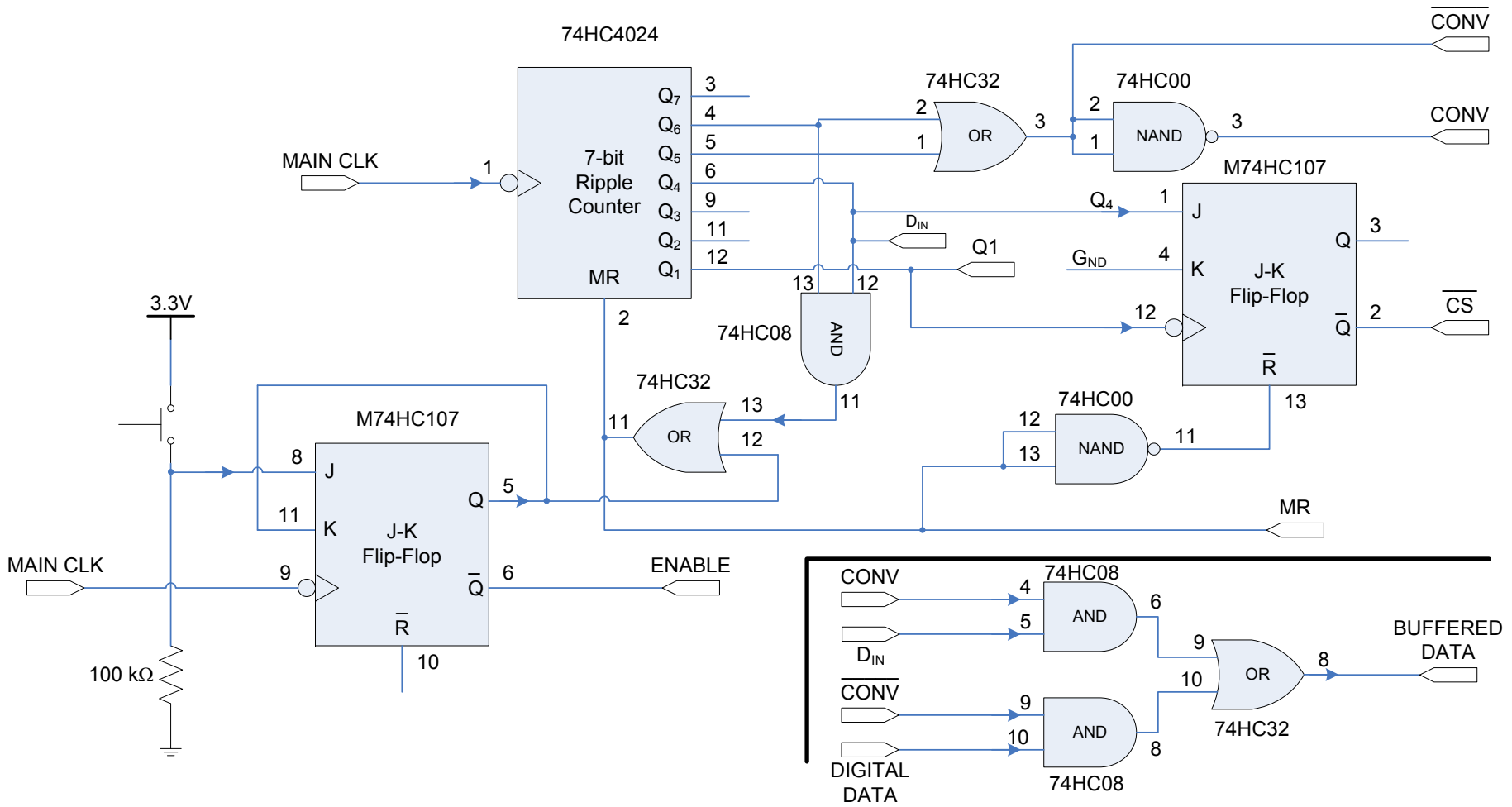
5. Radio Transmitter

6. Radio Receiver

3.3V

3.3V

f = 480 kHz
clock signal

Tricome 433 MHz
Embedded Antenna

Microstrip Line

HI-15530 Decoder

5	Vcc	CD	3
1	RF in		
2	RF gnd	RXD	7
4	GND	AF	6

RX2-433-160-3V

24	VDD	VALID WORD	1
5	DECODER CLK	TAKE DATA	3
8	UNIPOLAR DATA IN	SERIAL DATA OUT	4
12	GND	COMMAND/ DATA SYNC	10

To a controller

To a controller

To a controller

To a controller
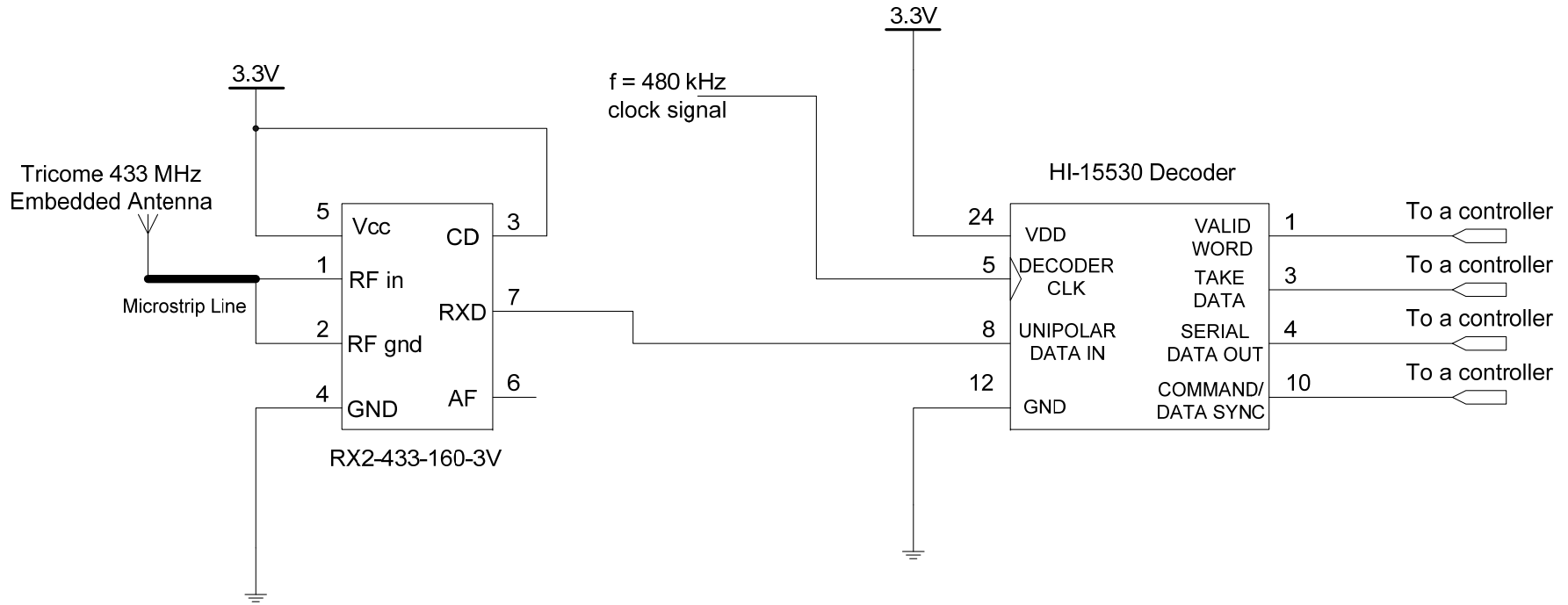
Appendix E

MATLAB Codes in the Study of De-noising Algorithms

```matlab
function Dcompile(HStype)

% This function opens the main microphone signal in file1 and the
% reference microphone signal in file2. The two signals the undergoes a
% number of different de-noising algorithms, namely:
%    - Simple Subtraction,
%    - Adaptive LMS filter,
%    - Adaptive RLS filter,
%    - Wavelet Thresholding (loaded from file3), and
%    - Interference Suppression via Spectral Comparison.
%
% At the end of the process, the output files of the de-noising
% operations are stored in file4.
%
% Input:
%    HStype - a string stating the sensor configuration and heart sound
%             e.g. c1dcNORMAL = Configuration 1 with front microphone in
%                               contact with the transmission surface with
%                               normal heart sound.
%                  c2d1AS     = Configuration 2 with front microphone 1 cm
%                               away from the transmission surface with
%                               Aortic Stenosis heart sound.
%
% Output:
%    'file4'.mat - a MATLAB data file containing all the inputs and
%                  outputs for all the de-noising operations. The filename
%                  is dependent on the input HStype e.g. c1dcNORMALr.mat
%                  and c2d1ASr.mat.
%
% Author:   Thanut Tosanguan
% Date:     12 December 2007
%

file1 = [HStype,'i'];
file2 = [HStype,'n'];
file3 = [HStype,'n'];
file4 = [HStype,'r'];

signal1 = load(file1);
signal2 = load(file2);

len = length(HStype);
rt = [];
Fn = 2004;

s1 = signal1.(file1(5:len+1));
s2 = signal2.(file2(5:len+1));
clear signal1 signal2

c = openwave2(file1(5:len));
c = c(:,1)';

%% Simple Subtraction
SUB = s1-s2;

%% Adaptive LMS
LMS = aLMS(s1,s2,256,0.01,Fn);
```

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```matlab
%% Adaptive RLS
RLS = aRLS(s1,s2,128,1,Fn);


%% Wavelet
signal3 = load(file3);
WLET = signal3.(file3);


%% Interference Suppression vi Spectral Comparison
SSF = ssf(s1,s2,.7, Fn, 7.5);
SSF=SSF';


%% Save into a .mat file

t = 1/Fn:1/Fn:length(SUB)/Fn;
save(file4, 's1', 's2', 'c', 'SUB', 'LMS', 'RLS', 'SSF', 'WLET', 't')
clear all
```

```matlab
function output = aLMS(signal1,signal2,n,mu,Fn)

% This function performs an Adaptive LMS filter on signal1 using signal2
% to estimate the noise.
%
% Inputs:
%   signal1 - Main microphone signal,
%   signal2 - Reference microphone signal,
%   n       - Number of filter coefficients,
%   mu      - Step size of the LMS adaptation, and
%   Fn      - Number of signal samples per second.
%
% Output:
%   output - Adaptive LMS filtered output
%
% Author: Thanut Tosanguan
% Date:   18th January 2007
%


%% Adaptive LMS filtering

len = length(signal1);
rep = floor(len/Fn);

for i = 1:rep
    lmsinit(n, mu);
    for j = 1+(i-1)*Fn:i*Fn
        [h,e(j)] = lms(signal2(j),signal1(j));
    end
end

output = e;
```

```matlab
function lmsinit(m,mu)
%
% Initialize the LMS filter
%
% function lmsinit(m,mu)
%
% m = dimension of vector
% mu = lms stepsize

% Copyright 1999 by Todd K. Moon

global hlms;
global mulms;
global xlms;
hlms = zeros(m,1);      % the filter weight
xlms = zeros(m,1);      % the data vector
mulms = mu;
```

```matlab
function [h,eap] = lms(x,d)
%
% Given a (real) scalar input signal x and a desired scalar signal d,
% compute an LMS update of the weight vector h.
% This function must be initialized by lmsinit
%
% function [h,eap] = lms(x,d)
%
% x = input signal (scalar)
% d = desired signal (scalar)
%
% h = updated LMS filter coefficient vector
% eap = (optional) a-priori error

% Copyright 1999 by Todd K. Moon

global hlms; global mulms; global xlms;

xlms = [x;xlms(1:length(xlms)-1)];
eap = d - hlms'*xlms;  % a priori error
hlms = hlms + mulms*xlms*eap;
h = hlms;
```

```matlab
function output = aRLS(signal1,signal2,n,delta,Fn)

% This function performs an Adaptive RLS filter on signal1 using signal2
% to estimate the noise.
%
% Inputs:
%   signal1 - Main microphone signal,
%   signal2 - Reference microphone signal,
%   n       - Number of filter coefficients,
%   delta   - The value to initialise the matrix P, and
```

```matlab
%   Fn      - Number of signal samples per second.
%
% Output:
%   output - Adaptive RLS filtered output
%
% Author: Thanut Tosanguan
% Date:   18th January 2007
%

%% Adaptive RLS filtering

len = length(signal1);
rep = floor(len/Fn);

for i = 1:rep
    rlsinit(n, delta);
    for j = 1+(i-1)*Fn:i*Fn
        [h,e(j)] = rls(signal2(j),signal1(j));
    end
end

output = e;
```

```matlab
%-------------------------------------------------------------------------------

function rlsinit(m,delta)
%
% Initialize the RLS filter
%
% function rlsinit(m,delta)

% m = dimension of vector
% delta = a small positive constant used for initial correlation inverse

% Copyright 1999 by Todd K. Moon

global hrls;
global Prls;
global xrls;
hrls = zeros(m,1);      % the filter weight
xrls = zeros(m,1);      % the data vector
Prls = 1/delta*eye(m);  % the correlation matrix
```

```matlab
%-------------------------------------------------------------------------------

function [h,eap] = rls(x,d)
%
% Given a scalar input signal x and a desired scalar signal d,
% compute an RLS update of the weight vector h.
%
% This function must be initialized by rlsinit
%
% function [h,eap] = rls(x,d)
%
% x = input signal
```

```matlab
% d = desired signal
%
% h = updated filter weight vector
% eap = (optional) a-priori estimation error

% Copyright 1999 by Todd K. Moon

global hrls;  global Prls; global xrls;


xrls = [conj(x);xrls(1:length(xrls)-1)];
k = Prls*xrls/(1+xrls'*Prls*xrls);  % gain vector;
eap = d - xrls'*hrls;  % a priori error
hrls = hrls + k*eap;
Prls = Prls - k*xrls'*Prls;
h = hrls;



-----------------------------------------------------------------------------------------------------
function [outn] = ssf(signal1,signal2,level, Fn, thr)

% This function performs an Interference Suppression via Spectral
% Comparison (ISSC) de-noising operation on signal1 using signal2 as an
% estimate of the noise.
%
% Inputs:
%   signal1 - Main microphone signal,
%   signal2 - Reference microphone signal,
%   level   - The inverse of 'alpha', the variable threshold used for
%             distinguishing the signal and the noise frequency bins
%   Fn      - Number of signal samples per second, and
%   thr     - Threshold of the PeakRemove algorithm
%
% Output:
%   outn - ISSC processed output with no overlapping of frames
%
% Author: Thanut Tosanguan
% Date:   24th March 2007
%
%


%% Interference Suppression via Spectral Comparison (ISSC) Technique

global basel
global peak
global gpos
global rheightl

% Initialisation
len = 2048;
l = length(signal1);
rep = floor(l/len);

outn = zeros(rep*len,1);

f=0:Fn/len:Fn-Fn/len;
```

```matlab
%% ISSC processing one frame at a time
for i = 1:rep
    % perform FFT on the input signals
    I = fft(signal1(1+(i-1)*len:(i)*len));
    I2 = fft(signal2(1+(i-1)*len:(i)*len));

    S = I;

    % Initialise variables for PeakRemove algorithm
    peak  = 1;
    gpos = false;
    temp = (f>70)&(f<90);
    p = max(abs(I(find(temp == 1))));
    basel = find(f > 55,1)-1;
    k = find(f > 97,1)-1;

    % ISSC is processed for half of the frequency spectrum
    for j = 1:len/2
        if (f(j) < 55)
            S(j) = I(j)/1000;
        else
            if abs(I2(j)) > level*abs(I(j))
                S(j) = I(j)/1000;
            end

            if j==k
                basel = k;
            end


            % Perform PeakRemove algorithm
            if (f(j) >=55 & f(j) <70)|(f(j)>97)
                S = peakremove(I,S, j, thr);
            end
        end
    end

    % The 2nd half of the spectrum is symmetrical, but has different
    % phase
    for j = 2:len/2
        S(j+1024) = abs(S(1026-j))*I(j+1024)/abs(I(j+1024));
    end

    % Perform IFFT on the processed spectrum
    s = real(ifft(S))';

    % Place the processed signal at the correct location
    outn(1+(i-1)*len:(i)*len) = s;
    plot(outn)

end
```

```matlab
function O = peakremove(S, O, j, thr)

% This function performs the PeakRemove operation during the Interference
% Suppression via Spectral Comparison (ISSC) de-noising operation. This
% looks for spurious spikes within the magnitude spectrum of the signal
% S.
%
% Inputs:
%   S   - The main microphone spectrum,
%   O   - The ISSC processed spectrum up to this point,
%   j   - The frequency bin tracker
%   thr - The threshold of the PeakRemove algorithm
%
% Output:
%   O - The PeakRemove processed output
%
% Author: Thanut Tosanguan
% Date:   24th March 2007
%

global basel
global peak
global gpos
global rheightl


%% PeakRemove Algorithm
dI = abs(S(j))-abs(S(j-1));
if (dI>0) & (gpos==false) & ((abs(S(j-1))/abs(S(peak)) < .5)|(basel==1))
& ((abs(S(j-1))) < min(abs(S(j+1:j+3))))
    if peak ~= 0
        baser = j-1;

        mx = max(abs(S(basel+1:baser-1)));
        peak = basel+find(abs(S(basel+1:baser-1))==mx);
        rheightr = (abs(S(peak))-abs(S(baser)))/abs(S(baser));
        rheightl = (abs(S(peak))-abs(S(basel)))/abs(S(basel));
        if (rheightr+rheightl)/2 >thr
            O(basel+1:baser-1) = (abs(S(basel))+abs(S(baser)))*...
                             S(basel+1:baser-1)/(2*abs(S(peak)));
        end
    end
    basel = j-1;
    gpos = true;
elseif (dI<0) & (gpos==true) & ((abs(S(j-1))) > max(abs(S(j+1:j+3))))
    peak = j-1;
    gpos = false;
end
```

```matlab
function [SNRas, SNRs] = SNRf(input, o1, o2, o3, o4, o5, template, P)

% This function prepare the SDR or Signal-to-(Noise plus) Distortion
% Ratio calculation - the SNR from the mean square error (MSE) between
% processed signal and original signal. The MSE is calculated when both
% the processed signal and the template signal has the same power.
```

```matlab
%
% Input:
%   input             - Received Signal
%   o1, o2, o3, o4 and o5 - The De-noised Signals
%   template          - Original 'Clean' Signal
%   P                 - number of detection cycles before shifting is
%                       required for correct SDR calculcation.
%
% Output:
%   SNRas - Average SDR improvement
%   SNRs  - Raw SDR (Row 1 = Received, R2 = o1, ..., R6 = o5)
%
% Author: Thanut Tosanguan
% Date:   20th July 2007
%

len = [length(o1), length(o2), length(o3), length(o4), length(o5)];
l = min(len);
N = floor(l/2004);
rep = floor(N/P); % No. of P repeats of SNR calculations


SNRs = zeros(6, rep*P);
SNRas = zeros(6,1);
shift = zeros(1, rep*P);

% Move template peak to 1050
[template] = inishiftsignal(template, 1050, 2004, 1);

for i = 1:rep
    A = input((i-1)*P*2004+1:l);
    O1 = o1((i-1)*P*2004+1:l);
    O2 = o2((i-1)*P*2004+1:l);
    O3 = o3((i-1)*P*2004+1:l);
    O4 = o4((i-1)*P*2004+1:l);
    O5 = o5((i-1)*P*2004+1:l);


    % Move first heart sound peak to 550 if not between 500 and 600
    [O1, O2, O3, O4, O5, A] = shiftsignalc(O1, o1, O2, o2, O3, o3, O4,...
                        o4, O5, o5, A, input, template, 750, 2004, i);

    [SNRs(:,1+P*(i-1):P*i),shift(1+P*(i-1):P*i)] = SNRcal(A, O1, O2, ...
                                        O3, O4, O5, template, P);

end

for i = 2:6
    SNRas(i) = mean(SNRs(i,:)-SNRs(1,:));
end
```

```matlab
function  [X] = inishiftsignal(x, loc, N, q)

% This function shifts the highest peak of the signal x to a specified
% location, loc.
%
% Input:
%   x   - signal to be shifted,
%   loc - location of the highest peak,
%   N   - the search area for peaks, and
%   q   - number of detection cycles
%
% Output:
%   X - the output with the highest peak in the search area moved to loc
%
% Author: Thanut Tosanguan
% Date:   18th July 2007
%


k  =length(x);
% Find peak locations in the q quadrants of N
for i = 1:q
    p(i) = find(x == max(x((i-1)*floor(N/q)+1:i*floor(N/q)/2)),1);

    if x(p(i))> 4*sqrt(mean(x(1:N/q).^2))
        p(1) = p(i);
        break
    end
end

if (p(1)<loc-50)||(p(1)>loc+50)
    if (p(1)<loc)
        sh = loc-p(1);
        X = [zeros(1, sh),x];
    else
        sh = p(1)-550;
        X = [x(1,sh:k), zeros(1,sh)];
    end
else
    X = x;
end
```

```matlab
function  [X, X1, X2, X3, X4, Y] = shiftsignalc(x, origx, x1, origx1, x2,
origx2, x3, origx3, x4, origx4, y, origy, template, loc, N, j)

% This function shifts signal x's and y to a specified
% location, loc.
%
% Input:
%   x's      - The segmented de-noised signals to be shifted,
%   origx's  - The full de-noised signals for signal reconstruction,
%   y        - The segmented main microphone signal,
%   origy    - The full main microphone signals,
%   template - Original 'Clean' signal,
%   loc      - Location to move peak to,
%   N        - The search area for the peak in the segmented signal, and
```

```matlab
%   j         - The SNR calculation cycle no.
%
% Output:
%   X's - The shifted output of the segmented de-noised signals,
%   Y   - The shifted output of the segmented main microphone signal.
%
% Author: Thanut Tosanguan
% Date:   18th July 2007
%

len = [length(x), length(x1), length(x2), length(x3), length(x4)];
k = min(len);


% Find location of highest correlation between the two signals
c = xcorr(x(1:1.5*N), template(1:N));
shift = (length(c)+1)/2 - find(c == max(c));


p(1) = 1050 - shift;

% shift signal
if (p(1)<loc-50)||(p(1)>loc+50)
    if (p(1)<loc)
        sh = loc-p(1);
        if j == 1
            Y = [zeros(1, sh),y];
            X = [zeros(1, sh),x];
            X1 = [zeros(1, sh),x1];
            X2 = [zeros(1, sh),x2];
            X3 = [zeros(1, sh),x3];
            X4 = [zeros(1, sh),x4];
        else
            Y = [origy((j-1)*5*2004-sh:(j-1)*5*2004), y];
            X = [origx((j-1)*5*2004-sh:(j-1)*5*2004), x];
            X1 = [origx1((j-1)*5*2004-sh:(j-1)*5*2004), x1];
            X2 = [origx2((j-1)*5*2004-sh:(j-1)*5*2004), x2];
            X3 = [origx3((j-1)*5*2004-sh:(j-1)*5*2004), x3];
            X4 = [origx4((j-1)*5*2004-sh:(j-1)*5*2004), x4];
        end
    else
        sh = p(1)-loc;
        Y = [y(1,sh:k), zeros(1,sh)];
        X = [x(1,sh:k), zeros(1,sh)];
        X1 = [x1(1,sh:k), zeros(1,sh)];
        X2 = [x2(1,sh:k), zeros(1,sh)];
        X3 = [x3(1,sh:k), zeros(1,sh)];
        X4 = [x4(1,sh:k), zeros(1,sh)];
    end
else
    Y = y;
    X = x;
    X1 = x1;
    X2 = x2;
    X3 = x3;
    X4 = x4;
end
```

```matlab
function [SNRs, shift] = SNRcal(input, o1, o2, o3, o4, o5, template, N)

% This function calculates the raw SDR data for each second of heart
sound
% by calculating the MSE between the processed and the template signal
% in each second
%
% Input:
%   input - Received Signal
%   outputs - De-noised Signal - o1, o2, o3, o4, o5
%   template - Original Signal
%   N - number of detection cycles
%
% Output:
%   SNRs - The Raw SDR (Row 1 = input, R2 = o1, ... R6 = o5)
%   shift - shift between original and recorded signal for each second
%
% Author: Thanut Tosanguan
% Date:   20th July 2007
%


SNRs = zeros(6,N);
c = template(1:2004);
shift = zeros(1, N);

for i = 1:N
    % Initialise input signals for scaling
    A = input(1+(i-1)*2004:(i)*2004);

    O1 = o1(1+(i-1)*2004:(i)*2004);

    O2 = o2(1+(i-1)*2004:(i)*2004);

    O3 = o3(1+(i-1)*2004:(i)*2004);

    O4 = o4(1+(i-1)*2004:(i)*2004);

    O5 = o5(1+(i-1)*2004:(i)*2004);


    % find shift between original signal and recorded signal
    x = xcorr(O1, c);
    shift(i) = 2004 - find(x == max(x));
    if sign(shift(i)) == 1
        C = template(1+shift(i):2004+shift(i));
    else
        sh = abs(shift(i));
        C = template(1:2004);
        A = input(1+(i-1)*2004+sh:i*2004+sh);
        O1 = o1(1+(i-1)*2004+sh:i*2004+sh);
        O2 = o2(1+(i-1)*2004+sh:i*2004+sh);
        O3 = o3(1+(i-1)*2004+sh:i*2004+sh);
        O4 = o2(1+(i-1)*2004+sh:i*2004+sh);
        O5 = o3(1+(i-1)*2004+sh:i*2004+sh);
    end
```

```matlab
    % Calculates the power of each signal
    pC = mean(C.^2);
    pA = mean(A.^2);
    po1 = mean(O1.^2);
    po2 = mean(O2.^2);
    po3 = mean(O3.^2);
    po4 = mean(O4.^2);
    po5 = mean(O5.^2);

    % Power-Scaling
    aa = sqrt(pC/pA).*A;
    oo1 = sqrt(pC/po1).*O1;
    oo2 = sqrt(pC/po2).*O2;
    oo3 = sqrt(pC/po3).*O3;
    oo4 = sqrt(pC/po4).*O4;
    oo5 = sqrt(pC/po5).*O5;

    SNRs(1, i) = 10*log(pC/mean((aa-C).^2));
    SNRs(2, i) = 10*log(pC/mean((oo1-C).^2));
    SNRs(3, i) = 10*log(pC/mean((oo2-C).^2));
    SNRs(4, i) = 10*log(pC/mean((oo3-C).^2));
    SNRs(5, i) = 10*log(pC/mean((oo4-C).^2));
    SNRs(6, i) = 10*log(pC/mean((oo5-C).^2));

end


%-------------------------------------------------------------------------------------------------------

function [SNRas, SNRs] = SNRf2(input, o1, o2, o3, o4, o5, template, P)

% This function prepare the SNRi or Signal-to-Noise ratio Indicator
% calculation - the SNR from comparing the signal power of the processed
% signal and original signal when heart sound is present and absent.
%
% Input:
%   input                - Received Signal
%   o1, o2, o3, o4 and o5 - The De-noised Signals
%   template             - Original 'Clean' Signal
%   P                    - number of detection cycles before shifting is
%                          required for correct SNRi calculcation.
%
% Output:
%   SNRas - Average SDR improvement
%   SNRs  - Raw SDR (Row 1 = Received, R2 = o1, ..., R6 = o5)
%
% Author: Thanut Tosanguan
% Date:   5th September 2007
%

len = [length(o1), length(o2), length(o3), length(o4), length(o5)];
l = min(len);
N = floor(l/2004);
rep = floor(N/P);

SNRs = zeros(6, rep*P);
SNRas = zeros(6,1);
shift = zeros(1, rep*P);
```

```matlab
% Move template peak to 1050
[template] = inishiftsignal(template, 1050, 2004, 1);

for i = 1:rep
    A = input((i-1)*P*2004+1:l);
    O1 = o1((i-1)*P*2004+1:l);
    O2 = o2((i-1)*P*2004+1:l);
    O3 = o3((i-1)*P*2004+1:l);
    O4 = o4((i-1)*P*2004+1:l);
    O5 = o5((i-1)*P*2004+1:l);


    % Move first heart sound peak to 550 if not between 500 and 600
    [O1, O2, O3, O4, O5, A] = shiftsignalc(O1, o1, O2, o2, O3, o3, O4,...
                              o4, O5, o5, A, input, template, 750, 2004,
i);

    [SNRs(:,1+P*(i-1):P*i), shift(1+P*(i-1):P*i)] = SNRcal2(A, O1, O2,...
                                     O3, O4, O5, template, P);

end

for i = 2:6
    SNRas(i) = mean(SNRs(i,:)-SNRs(1,:));
end




%-----------------------------------------------------------------------

function [SNRs, shift] = SNRcal2(input, o1, o2, o3, o4, o5, template, N)

% This function calculates the raw SNRi data for each second of heart
sound
% by calculating the signal power of the processed and during the time
% when heart sound is present and when it is not.
%
% Input:
%    input - Received Signal
%    outputs - De-noised Signal - o1, o2, o3, o4, o5
%    template - Original Signal
%    N - number of detection cycles
%
% Output:
%    SNRs - The Raw SNRi (Row 1 = input, R2 = o1, ... R6 = o5)
%    shift - shift between original and recorded signal for each second
%
% Author: Thanut Tosanguan
% Date:   5th September 2007
%



SNRs = zeros(6,N);
SNRu = zeros(6,N);
c = template(1:2004);
shift = zeros(1, N);
```

```matlab
for i = 1:N
    % Initialise input signals for scaling
    A = input(1+(i-1)*2004:(i)*2004);

    O1 = o1(1+(i-1)*2004:(i)*2004);

    O2 = o2(1+(i-1)*2004:(i)*2004);

    O3 = o3(1+(i-1)*2004:(i)*2004);

    O4 = o4(1+(i-1)*2004:(i)*2004);

    O5 = o5(1+(i-1)*2004:(i)*2004);


    % find shift between original signal and recorded signal
    x = xcorr(O1, c);
    shift(i) = 2004 - find(x == max(x));
    if sign(shift(i)) == 1
        C = template(1+shift(i):2004+shift(i));
    else
        sh = abs(shift(i));
        C = template(1:2004);
        A = input(1+(i-1)*2004+sh:i*2004+sh);
        O1 = o1(1+(i-1)*2004+sh:i*2004+sh);
        O2 = o2(1+(i-1)*2004+sh:i*2004+sh);
        O3 = o3(1+(i-1)*2004+sh:i*2004+sh);
        O4 = o2(1+(i-1)*2004+sh:i*2004+sh);
        O5 = o3(1+(i-1)*2004+sh:i*2004+sh);
    end

    % Define signal and noise area
    Y = find(C == max(C));
    N1 = Y-35;
    S1 = N1+1;
    S2 = Y+176;
    N2 = S2+1;
    N3 = Y+661;
    S3 = N3+1;
    S4 = Y+881;
    N4 = S4+1;

    pC = mean(C.^2);          % Power of original

    pA = mean(A.^2);
    po1 = mean(O1.^2);
    po2 = mean(O2.^2);
    po3 = mean(O3.^2);
    po4 = mean(O4.^2);
    po5 = mean(O5.^2);

    % Power-Scaling
    aa = sqrt(pC/pA).*A;
    oo1 = sqrt(pC/po1).*O1;
    oo2 = sqrt(pC/po2).*O2;
    oo3 = sqrt(pC/po3).*O3;
```

```
    oo4 = sqrt(pC/po4).*O4;
    oo5 = sqrt(pC/po5).*O5;

    SNRs(1, i) = 10*log(mean([aa(S1:S2), aa(S3:S4)].^2)/mean([aa(1:N1),
aa(N2:N3), aa(N4:2004)].^2));
    SNRs(2, i) = 10*log(mean([oo1(S1:S2),
oo1(S3:S4)].^2)/mean([oo1(1:N1), oo1(N2:N3), oo1(N4:2004)].^2));
    SNRs(3, i) = 10*log(mean([oo2(S1:S2),
oo2(S3:S4)].^2)/mean([oo2(1:N1), oo2(N2:N3), oo2(N4:2004)].^2));
    SNRs(4, i) = 10*log(mean([oo3(S1:S2),
oo3(S3:S4)].^2)/mean([oo3(1:N1), oo3(N2:N3), oo3(N4:2004)].^2));
    SNRs(5, i) = 10*log(mean([oo4(S1:S2),
oo4(S3:S4)].^2)/mean([oo4(1:N1), oo4(N2:N3), oo4(N4:2004)].^2));
    SNRs(6, i) = 10*log(mean([oo5(S1:S2),
oo5(S3:S4)].^2)/mean([oo5(1:N1), oo5(N2:N3), oo5(N4:2004)].^2));

end
```

Appendix F

Capacitively Loaded Gyrator as an Inductor
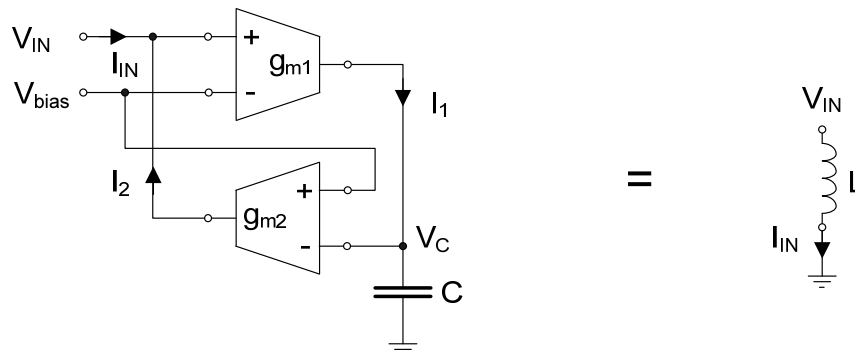
The 'ideal' capacitively loaded gyrator shown above (on the left) can behave like an 'ideal' grounded inductor (on the right) because the gyrator is an impedance inverter. Thus, the gyrator inverts the impedance of the capacitor C and makes the overall structure's input impedance appears as an inductor.

The input impedance of an ideal grounded inductor (on the right) is given by:

$$Z_{IN} = \frac{v_{IN}}{I_{IN}} = j\omega L \qquad \text{(F.1)}$$

And by working out the input impedance of the ideal capacitively loaded gyrator, a similar expression can be obtained. This can be done by calculating the input current I_{IN}, which requires us to calculate I_1, V_C and I_2.

$$I_1 = g_{m1} v_{IN} \qquad \text{(F.2)}$$

and
$$I_2 = -g_{m2} v_C \qquad \text{(F.3)}$$

where, $V_{IN} = v_{IN} + V_{bias}$ and $V_C = v_C + V_{bias}$

The input impedance of an ideal grounded capacitor is given by:

$$Z_{IN} = \frac{v_{IN}}{I_{IN}} = \frac{1}{j\omega C} \qquad \text{(F.4)}$$

Since $v_C = v_{IN}$ and $I_1 = I_{IN}$ for the above grounded capacitor, thus:

$$v_C = \frac{I_1}{j\omega C} \qquad (F.5)$$

By substituting equation F.2 into equation F.5 and the resulting expression into equation F.3, we obtain the following expression:

$$I_2 = \frac{-g_{m2}g_{m1}v_{IN}}{j\omega C} \qquad (F.6)$$

But $I_2 = -I_{IN}$, therefore:

$$Z_{IN} = \frac{v_{IN}}{I_{IN}} = \frac{j\omega C}{g_{m1}g_{m2}} \qquad (F.7)$$

Thus, an ideal capacitively loaded inductor with an ideal capacitor C behave as if it is an ideal inductor with inductance, L:

$$L = \frac{C}{g_{m1}g_{m2}} \qquad (F.8)$$

A same result can be obtained for the below 'ideal' capacitively loaded gyrator structure, which can be used to behave as an 'ideal' floating inductor, where the input impedance expression is given by:

$$Z_{IN} = \frac{v_{left} - v_{right}}{I_{IN}} = j\omega L \qquad (F.9)$$