AALTO UNIVERSITY
SCHOOL OF ELECTRICAL ENGINEERING
Master's Programme in Automation and Electrical Engineering

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IMPROVING THE FAULT CLEARING CAPABILITY OF A UPS DEVICE

Thesis submitted in partial fulfilment of the requirements for the degree of Master of Science (Technology)

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Abstract

UPS devices are utilized to ensure a constant and undisturbed power supply for critical loads. If a fault occurs in the AC grid that normally supplies the load, the UPS device will instantly begin to supply power from its batteries via the inverter to the load. However, if a fault, such as a short circuit, occurs in the load side of the UPS when the UPS is supplying power from its batteries, the UPS must be able to supply enough fault current to clear the circuit breaker closest to the fault location and isolate the fault before the UPS itself trips to overcurrent. The maximum output current of the UPS is intentionally limited in time and magnitude to prevent power semiconductor components of the UPS inverter from suffering overcurrent damages. The problem is that UPS devices must be often oversized in terms of rated power so that a sufficient fault clearing capability of the UPS to clear respective circuit breakers in the load side is achieved. Thus, the spare power which results from oversizing the UPS is dispensable during normal operation of the UPS.

This thesis aims to find economical ways to improve the fault clearing capability of a UPS device. Hence, a simulation model is developed which can be used to estimate how much the fault clearing capability of a UPS device may be improved by installing IGBTs and diodes in parallel to the main circuit of the UPS inverter. Current limit values of the UPS inverter and number of parallel connected IGBTs and diodes in the main circuit of the inverter are adjustable in the simulation model. Power losses and junction temperatures of IGBTs and diodes are calculated based on input data which may be obtained from datasheets of IGBTs and diodes. The solution to improve the fault clearing capability of a UPS device by adding IGBTs and diodes in parallel to the main circuit of the inverter is compared from economical and technical point of view to the use of an external fault clearing circuitry which is another worthy solution to improve the fault clearing capability of a UPS device.

Cost comparison conducted between the two solutions revealed that improving the fault clearing capability of a 20 kW UPS device by adding IGBTs and diodes in parallel to the main circuit of the inverter may result in 20–30% higher costs than using the fault clearing circuitry. Furthermore, the fault clearing circuitry may be technically a more feasible solution to be applied for existing UPS devices than the change in IGBT and diode configuration.

Keywords UPS, fault clearing, inverter, IGBT, diode, circuit breaker, power losses

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Tiivistelmä

UPS-laitteita käytetään varmistamaan jatkuva ja häiriötön sähkönsyöttö kriittisille kuormille. UPS-laite alkaa välittömästi syöttää sähköä akustostaan vaihtosuuntaajan kautta kuormalle, jos kuormaa normaalisti syöttävässä vaihtosähköverkossa syntyy vika. Jos UPS laitteen kuormapuolella syntyy kuitenkin vika, kuten oikosulku, kun UPS laite syöttää sähköä kuormalle akustostaan, UPS-laitteen täytyy pystyä syöttämään tarpeeksi vikavirtaa, jotta lähinnä vikapaikkaa oleva katkaisija avautuu ja erottaa vian ennen kuin UPS-laite katkaisee sähkönsyötön ylivirran vuoksi. UPS-laitteen maksimilähtövirta on tarkoituksellisesti rajoitettu ajalliselta kestoltaan ja suuruudeltaan, mikä ehkäisee UPS-laitteen vaihtosuuntaajassa olevien tehopuolijohdekomponenttien vaurioitumista ylivirran vuoksi. Ongelmana on, että UPS-laitteita joudutaan ylimitoittamaan nimellisteholtaan, jotta niille saadaan riittävän korkea vian erotuskyky laukaisemaan kuormapuolen katkaisijat vikatilanteessa. Tällöin UPS-laitteen ylimitoittamisesta syntyvä lisäteho on kuitenkin tarpeetonta UPS-laitteen normaalin toiminnan aikana.

Tämän työn tarkoituksena on löytää taloudellisia keinoja parantaa UPS-laitteen vian erotuskykyä. Työssä kehitettiin simulointimalli, jolla voidaan arvioida, kuinka paljon UPS-laitteen vian erotuskykyä voidaan parantaa kytkemällä IGBT- ja diodikomponentteja rinnan UPS-laitteen vaihtosuuntaajan pääpiiriin. Vaihtosuuntaajan virtarajoja ja rinnankytkettävien IGBT- ja diodikomponenttien määrää voidaan säädellä simulaatiomallissa. IGBT- ja diodikomponenttien tehohäviöiden ja liitoslämpötilojen laskenta perustuu niiden datalehdistä saataviin tietoihin, jotka syötetään simulaatiomallille. Ratkaisua, jossa UPS-laitteen vian erotuskykyä parannetaan kytkemällä IGBT- ja diodikomponentteja rinnan vaihtosuuntaajan pääpiiriin, verrataan taloudellisesta ja teknisestä näkökulmasta ulkoiseen vian erotuspiiriin, joka on toinen varteenotettava ratkaisu, jolla UPS-laitteen vian erotuskykyä voidaan parantaa.

Ratkaisuille tehtiin kustannusvertailu, josta selvisi, että parantamalla nimellisteholtaan 20 kW:n UPS-laitteen vian erotuskykyä lisäämällä IGBT- ja diodikomponentteja rinnan vaihtosuuntaajan pääpiiriin lisää se kustannuksia 20–30% verrattuna ulkoisen vian erotuspiirin käyttöön. Vian erotuspiirin kytkeminen on lisäksi teknisesti helpompi toteuttaa jo olemassa oleviin UPS-laitteisiin verrattuna siihen, että niihin tehtäisiin vaadittavat IGBT- ja diodikomponenttien laitekokoonpanomuutokset.

Avainsanat UPS, vian erotus, vaihtosuuntaaja, IGBT, diodi, katkaisija, tehohäviöt

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I feel enthusiastic and at the same time wistful to leave my status as a student behind and move into working life. I am excited to meet with challenges that the future offers.

Espoo, 15.4.2018

Oskari Mikkola

LIST OF SYMBOLS

B	Magnetic flux density
C	Capacitance
E_{on}	Turn-on energy loss of an IGBT
E_{off}	Turn-off energy loss of an IGBT
E_{rec}	Reverse recovery energy loss of a diode
f	Frequency
f_{res}	Resonance frequency
f_{sw}	Switching frequency
H	Magnetic field intensity
i	Current
i_{max}	Maximum current limit
i_{min}	Minimum current limit
I_c	Collector current of an IGBT
I_{cu}	Rated ultimate breaking capacity of a circuit breaker
I_F	Forward current of a diode
I_n	Rated current
I_{prr}	Peak reverse recovery current of a diode
I_s	Selectivity limit current
L	Inductance
m	Modulation index
u	Voltage
U_d	DC link voltage of an inverter
U_{GE}	Gate-to-emitter voltage of an IGBT
U_{CE}	Collector-to-emitter voltage of an IGBT
U_F	Forward voltage of a diode
U_{FP}	Peak forward voltage of a diode
U_{prr}	Peak reverse recovery voltage of a diode
U_R	Reverse voltage
$\hat{u}_r$	Peak value of the reference wave in pulse width modulation
$\hat{u}_c$	Peak value of the carrier wave in pulse width modulation
P_{cond}	Conduction power loss
P_{sw}	Switching power loss
P_{tot}	Total power loss
Q_{rr}	Reverse recovery charge of a diode
$R_{th(j-c)}$	Thermal resistance between junction and case
$R_{th(j-a)}$	Thermal resistance between junction and ambient
s	Softness factor of a diode
T	Cycle time
T_{sw}	Cycle time of a switching sequence waveform
T_{half}	Cycle time of a half-cycle
T_c	Case temperature
T_h	Heatsink temperature
T_j	Junction temperature
T_{vj}	Virtual junction temperature
t	Time
t_{fall}	Fall time of a waveform
t_{rise}	Rise time of a waveform

t_{cond}	Conduction time of an IGBT
t_{on}	Turn-on time of an IGBT
t_{off}	Turn-off time of an IGBT
t_{dead}	Dead time period
t_{d_cond}	Conduction time of a diode
t_{d_on}	Turn-on time of a diode
t_{d_off}	Turn-off time of a diode
t_{rr}	Reverse recovery time of a diode
X_c	Capacitive reactance
X_L	Inductive reactance
$Z_{th(j-c)}$	Thermal impedance between junction and case
$Z_{th(c-h)}$	Thermal impedance between case and heatsink
$Z_{th(j-a)}$	Thermal impedance between junction and ambient
μ	Permeability

LIST OF ABBREVIATIONS

AC	Alternating current
CB	Circuit breaker
CPLD	Complex programmable logic device
DC	Direct current
IEC	International electrotechnical commission
IGBT	Insulated gate bipolar transistor
MCB	Miniature circuit breaker
MCCB	Molded case circuit breaker
MOSFET	Metal-oxide-semiconductor field-effect transistor
NPC	Neutral point clamped
PWM	Pulse width modulation
SCR	Silicon controlled rectifier
THD	Total harmonic distortion
TIM	Thermal interface material
UPS	Uninterruptible power supply
VSI	Voltage source inverter

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1 INTRODUCTION

Data centers are facilities which process, store and transmit digital information. They may include tens of thousands of servers, storage devices and network appliances which must operate continuously hour after hour and day after day. A data center may consume from one to over 500 megawatts of electrical power depending on its size. Operations of data centers are dependent on electricity all the time and blackouts may cause considerable financial damage to companies. Therefore, they can be considered as critical loads from a power supply point of view. Power grid companies strive to transfer power to their customers, such as data centers, as undisturbed as possible and without interruptions. However, it is a mission that can not be perfectly reached at least for the time being. Power failures do occur occasionally due to different environmental and technical reasons. Uninterruptible power supply (UPS) systems, however, ensure that power is supplied to critical loads constantly in a case of power failure in the grid. They provide temporary backup power from their batteries for loads until generators are turned on to operate as main backup power supply. In addition, hospitals and factories are examples of facilities where the power failure would have serious consequences. Thus, UPS devices are used in hospitals and factories to increase the reliability of power supply and to maintain the power quality of supply power on a sufficient level.

The reliability of UPS devices is a significant issue, since in grid fault situations they may be the only power supply for critical loads. A UPS failure could lead to a total blackout of a system. The UPS may trip due to a fault in the load side, such as a short circuit or a ground fault, which may cause a large overcurrent. Furthermore, an internal fault of the UPS may bring on the UPS failure, however, internal faults are not in the scope of this thesis and therefore they are not discussed in more detail.

In electric power systems, loads are typically protected from overcurrent with circuit breakers or fuses. Circuit breakers are nowadays more commonly used in the industry than fuses and therefore fuses are not studied in detail in this thesis. Circuit breakers are coordinated in a selective way which means that the breaker closest to the load would trigger quickest in overcurrent situation and isolate the fault location from other parts of the circuit. When the fault is isolated, other parts of the circuit may continue normal operation.

The UPS draws its supply power from batteries when it is operating in stored-energy mode. Stored-energy mode is used if AC grid voltage is not available. If a short circuit happens in the load side when the UPS is operating in stored-energy mode, the UPS device is able to supply only limited short circuit current for a limited time to the fault location. The current and time is intentionally limited to prevent semiconductor devices of the UPS, such as insulated gate bipolar transistors (IGBT), from suffering overcurrent damages. Typically, the current limit is adjusted in UPS devices to a value which is few times the UPS rated current and the UPS may be regulated to operate at current limit for

a few hundreds of milliseconds in maximum. If the maximum operating time at current limit exceeds, the UPS will trip and all loads connected to the UPS output will hence lose the power supply.

Circuit breakers, however, require a sufficient overcurrent to act instantaneously. The current threshold for instantaneous tripping of the circuit breaker is dependent on rated current of the circuit breaker and its time-current characteristics. For this reason, the UPS will close the bypass switch and connect the load directly to the AC grid in fault situations if the UPS is overloaded to its current limit. When the load is connected to the AC grid, the rating of a bypass fuse primarily limits the available fault current. Nevertheless, the magnitude of the fault current that can be drawn from the AC grid through the bypass switch may be over ten times higher than the rated current of the UPS device. Thus, it is clearly more than the maximum output current that the UPS can draw from its batteries. This operating principle increases the probability that a selective protection of the load functions correctly and hence circuit breakers may isolate faults quickly.

However, the foregoing operating principle is practicable only when the AC grid is available. During power outages, the UPS device must supply fault current on its current limit to the fault location until the circuit breaker trips and fault is cleared. The circuit breaker must trip before the UPS itself trips to the overload so that selectivity of the protection is remained. Because the current limit of the UPS is known, UPS manufacturers guarantee in the specification of the UPS device, which size and type of a circuit breaker the UPS is able to trigger when the UPS is operating on its current limit. This is referred to as a fault clearing capability of the UPS device.

The aim of this thesis is to find economical ways to improve the fault clearing capability of a UPS device. Observed solutions for the problem comprise changing IGBT and diode configuration in the main circuit of a UPS inverter or using an external fault clearing circuitry. Improving the fault clearing capability means that output current of a UPS operating at current limit is increased to a value that triggers larger circuit breakers instantaneously when the UPS is drawing power from its batteries.

Improving the fault clearing capability is important for UPS manufacturers as their customers usually have circuit breakers of their loads installed or selected beforehand. Therefore, the customer must select a suitable UPS according to the fault clearing capability so that the UPS is able to trigger respective circuit breakers when it is operating at current limit. A problem is that customers must often acquire a UPS with higher current and power ratings than required for the normal operation of the load just to achieve an adequate fault clearing capability. In normal operation, the spare power capacity is useless and therefore non-profitable. Problem could be avoided if customers would change their circuit breakers smaller and more sensitive to match the fault clearing capability of the UPS. However, the changing of circuit breakers may be challenging and expensive for customers. In some cases, it is neither possible to change circuit breakers if the load requires certain time-current characteristics for the breaker.

For example, if the customer has a load with 20 kW rated power, the UPS device with 20 kW rated power may be sufficient in terms of rated power and current ratings.

However, the 20 kW UPS has the fault clearing capability to trigger certain type and size of circuit breakers stated in the device specification. Whether the customer has installed larger circuit breakers to protect the load than stated in the specification, the 20 kW UPS is no longer a valid solution. In that case the customer must acquire a UPS with a higher power rating, such as a 30 kW UPS, which has the fault clearing capability to trigger larger circuit breakers in terms of current rating. Oversizing the UPS device only due to the insufficient fault clearing capability, however, generates spare capacity with no purpose in normal operation. With better fault clearing capability of the UPS, larger circuit breakers may be triggered and thus the gap between the rated power of the UPS and the load may be reduced.

The reference UPS device studied in this thesis is a 20 kW double conversion three-phase three-level UPS. The first target in this thesis is to discover how much the output current of the UPS operating at current limit could be increased by changing the present IGBT and diode configuration of the UPS inverter to a new configuration which has a higher current-carrying capacity. In addition, costs of new configurations which may improve the fault clearing capability of a UPS device are analysed and compared with each other. The study is performed by creating a simulation model which simulates the operation of the UPS inverter at current limit and calculates average power losses and junction temperatures of IGBTs and diodes in the main circuit of the UPS inverter when the UPS is operating at current limit. The configuration of IGBTs and diodes in the main circuit of the inverter can be changed which denotes that IGBTs and diodes can be added in parallel in the simulation model. Power losses of IGBTs and diodes in the main circuit of the inverter are calculated with different configurations of IGBTs and diodes when a UPS device operates at current limit. Finally, the fault clearing capability of a UPS device with new IGBT and diode configurations is evaluated based on simulation results.

Another target in this thesis is to consider whether an external fault clearing circuitry could be a possible and economical solution to increase the fault clearing capability of a UPS device. The cost of the external fault clearing circuitry is studied and compared to the cost of the solution where IGBT and diode configuration of the UPS inverter is changed. The idea in the fault clearing circuitry is that in a fault situation it would supply enough fault current to clear the respective circuit breaker in the load side of the UPS device.

Chapters 2, 3 and 4 in this thesis provide background knowledge and theory for the subject of the thesis. They are utilized in implementing the simulation model which calculates power losses and junction temperatures of IGBTs and diodes in the main circuit of the inverter when the UPS operates at current limit. In Chapter 2, different topologies of UPS devices are presented. In Chapter 3, main circuit topology of a three-phase three-level UPS inverter is presented. Furthermore, characteristics of IGBTs, diodes and LC filter of the inverter are discussed in Chapter 3. In Chapter 4, subjects related to fault clearing are discussed. Thus, it comprises discussing about faults, operating principle of the UPS device at current limit, circuit breakers and the fault clearing circuitry. Finally, in Chapter 5 the simulation model implemented in this thesis and simulation results are

revealed. Chapter 6 concludes this thesis and aims to give an answer to the research problem on solutions to economically improve the fault clearing capability of a UPS device.

2 UNINTERRUPTIBLE POWER SUPPLIES

Sudden power outages or grid disturbances may cause severe damage to sensitive and vital electrical loads. These kinds of loads can be found for example from hospitals, data centers and factories. Uninterruptible power supply (UPS) devices serve as power supply backup systems for critical loads. The UPS device is typically located between the supplying power grid and the critical load or loads. The UPS may consist of several power modules connected in parallel which makes the system modular and increases the overall reliability of the UPS system. In a case of power grid failure, the UPS provides continuous and high-quality input power for the load connected to the UPS device. Accordingly, the UPS provides time to switch off critical loads in a controlled way when a power cut occurs. If the UPS is linked with a generator, it can be used to supply power to the load during the time required to turn on the generator. In addition to power failure, UPS devices can protect loads from voltage sag, voltage surge, undervoltage, overvoltage, electrical noise, frequency variation, switching transients and harmonic distortion. The extent of protection capabilities is dependent on topology of the UPS device. (1,2)

UPS types can be categorized into three different types: static, rotary and hybrid static/rotary. The key difference between rotary and static UPS systems is that the rotary UPS comprises a motor-generator contrary to the static UPS. However, only static UPS systems are discussed in this thesis as they are the most frequently used UPS systems. Three main topologies of static UPS systems are passive standby topology, line-interactive topology and double conversion topology. These three topologies and their basic structures are presented more closely in this chapter. (1)

2.1 Passive standby topology

Passive standby topology, also known as off-line UPS, is the most common UPS topology used to protect personal computers. The off-line UPS is able to protect the connected load from power failures, voltage sags and voltage surges (2). The off-line UPS consists of an AC/DC rectifier, a battery bank, a DC/AC inverter and a static switch. The topology is presented in Figure 1.

During the normal mode of operation, the static switch is on and hence the load gets its supply power directly from the AC grid. To improve the power quality, the DC/AC inverter may be used to correct the power factor or as an active filter to reduce the harmonics of the supply current, however, generally the DC/AC inverter stays in standby when operating in normal mode and hence is not affecting the power quality of the supply power. The AC/DC rectifier converts alternating current of AC grid to direct current adequate for the battery bank and thus the rectifier charges the battery bank. (1)

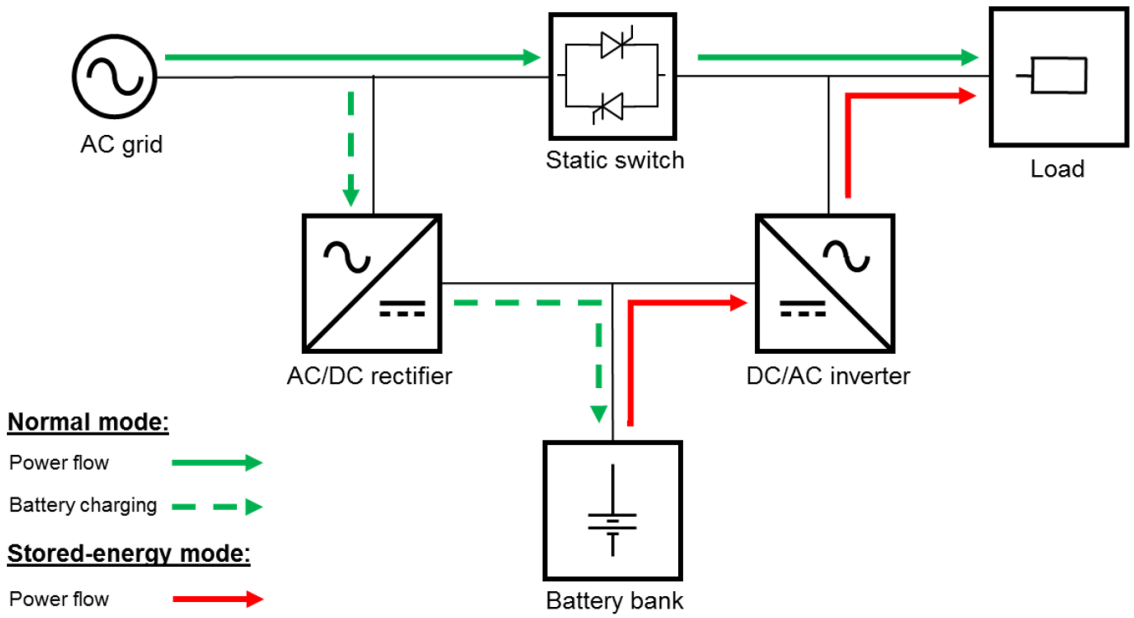

Figure 1: *Structure of passive standby topology and its operating modes.*

If the incoming supply voltage from the AC grid falls or rises beyond the preset permissible voltage level or is not available at all the off-line UPS system switches its operating mode from normal to stored-energy mode of operation. In stored-energy mode the UPS supplies power to the load from the battery bank. The power is supplied from the battery bank via the DC/AC inverter. The inverter converts direct current delivered by the batteries to alternating current applicable for the load. The off-line UPS operates in stored-energy mode for the backup time, which is dependent on the capacity of the battery bank or until the voltage of AC grid is restored within the permissible values. (1)

The main advantages of passive standby topology are low cost, high efficiency and small size, which makes this topology suitable for home and office environments where the supply voltage does not include frequent disturbances or have low quality. However, disadvantages of this topology are that the off-line UPS is not able to regulate the output voltage and a certain transfer time is required for the UPS to detect the lost grid voltage and to change the operating mode from normal to stored-energy mode. Transfer time may be for instance 25 milliseconds and during that time the supply voltage for the load is zero which is not acceptable for all kind of critical loads. Nevertheless, the transfer time is sufficient for most office applications such as personal computers. (1,3)

2.2 Line-interactive topology

A line-interactive UPS topology is used to protect low-power applications. A line-interactive UPS consists of a static switch, a series inductor, a bidirectional converter and a battery bank. The topology is presented in Figure 2. A line-interactive UPS is able to protect the load from power outage, voltage sag, voltage surge, undervoltage and overvoltage (2).

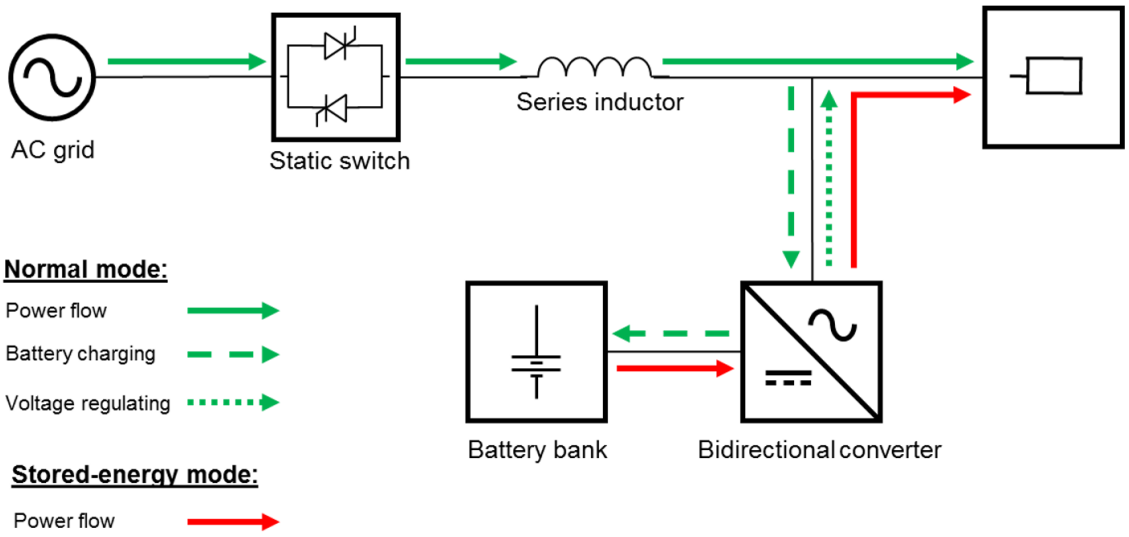

Figure 2: *Structure of line-interactive topology and its operating modes.*

In normal mode of operation power flows to the load through the static switch and the series inductor. The bidirectional converter operates both as AC/DC rectifier which charges the battery bank and as DC/AC inverter which regulates the output voltage of the UPS. The voltage regulation in this case means that the inverter supplies reactive power to the load during undervoltage situations and consumes reactive power during overvoltage situations. In this way, the input voltage for the load is kept relatively stable despite voltage fluctuations in the AC grid. Furthermore, the input voltage is kept in phase with the input current and thus the power factor is close to unity.

The series inductor is required in this topology for implementing the control of the voltage regulation. The voltage drop over the series inductor is detected and it is applied for adjusting the amount of reactive power supplied or consumed by the inverter. The amount of supplied or consumed reactive power by the inverter should be such that the power factor for the UPS load is kept close to unity and input voltage for the load stable. The desired inverter output voltage phasor is achieved by subtracting the series inductor voltage phasor from the AC grid voltage phasor. The magnitude and angle of series inductor voltage phasor depends on current flowing through the series inductor. Thus, the series inductor current phasor can be derived from the series inductor voltage phasor by dividing the series inductor voltage phasor with impedance of the series inductor and making the current phasor to lag the voltage phasor by 90º. The desired inverter output current phasor is achieved by subtracting the load current phasor from the series inductor current phasor as the series inductor current is the current supplied from the AC grid. Consequently, the required amount for the inverter to supply or consume reactive power is obtained by a control device as the grid voltage and voltage over the series inductor are known. The inverter adjusts its output voltage to the desired value by pulse width modulation (PWM). Active power is not required in the voltage regulation and therefore it does not consume the charge of the battery bank. (1) (4)

In a case where the AC grid voltage increases or drops beyond the permissible voltage level the UPS switches its operating mode to stored-energy mode of operation.

Consequently, the static switch disconnects the load from the AC grid and the inverter supplies power to the load from the battery bank. Similarly, as the passive standby UPS, the line-interactive UPS requires a transfer time for switching the operating mode from normal to stored-energy. Nevertheless, the transfer time is shorter in line-interactive UPS than in standby UPS. (5)

2.3 Double conversion topology

Double conversion UPSs, which are also called as on-line UPSs, are able to protect the load from all nine power problems: power failure, voltage sag, voltage surge, undervoltage, overvoltage, electrical noise, frequency variation, switching transients and harmonic distortion. It consists of AC/DC rectifier, a battery bank, DC/AC inverter and a static bypass switch. The double conversion topology is presented in Figure 3.

In normal mode of operation, the static bypass switch is in off state and power is supplied through the AC/DC rectifier and the DC/AC inverter into the load. Besides supplying power for the inverter, the AC/DC rectifier also charges the battery bank and thus it has the highest power rating of the system. The DC/AC inverter is rated to entirely fulfil the power demand of a nominal load. (1)

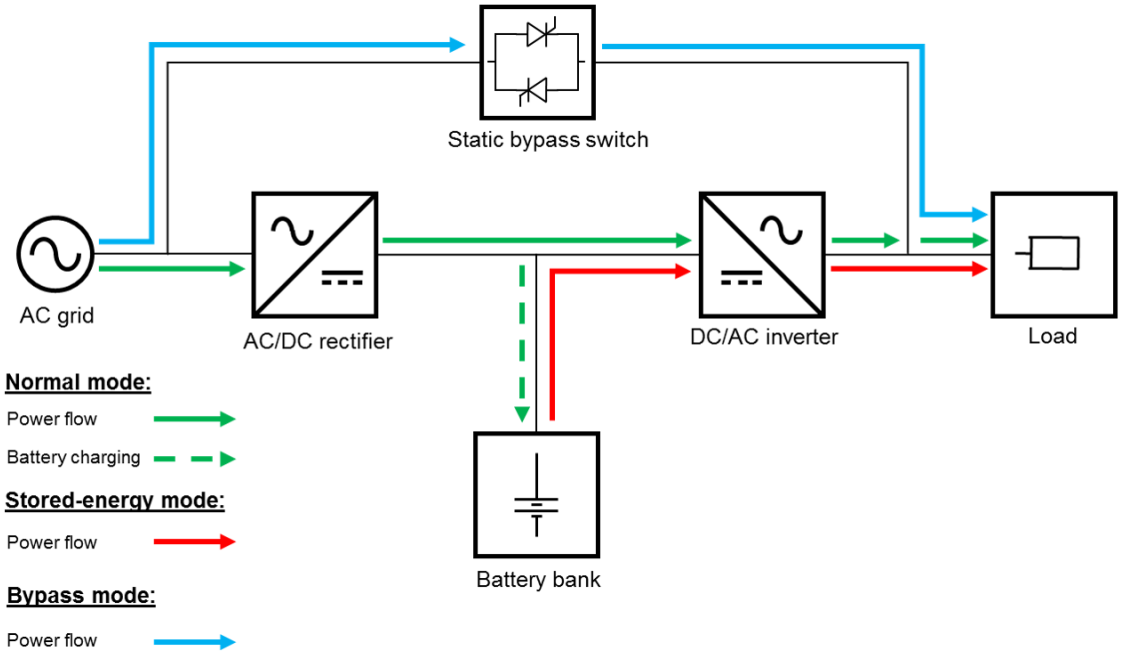

Figure 3: *Structure of double conversion topology and its operating principle*

During the normal mode of operation, on-line UPSs has good line conditioning characteristics and they can compensate or filter disturbances in AC grid from not being injected to the load. Furthermore, if the AC grid voltage is outside the permissible input voltage tolerance, on-line UPS can switch its operating mode to stored-energy mode without a transfer time because the DC/AC inverter is supplying the load all the time. (1)

In the stored-energy mode the inverter supplies power to the load from the battery bank similarly as other topologies. The absence of a transfer time is a clear advantage in double conversion topology compared to other UPS topologies and therefore they can be used to protect any type of electrical load. However, because power flows through the rectifier and the inverter in normal mode, power losses are generated which decreases the efficiency of this topology compared to other topologies. (1,2)

In addition to normal and stored-energy mode, double conversion UPSs have also a third operation mode called bypass mode. The double conversion UPS switches to bypass mode in the case of an internal fault or overcurrent. Overcurrent may develop, for example, as result of a short circuit in the load. In the bypass mode, the bypass switch closes and the UPS interrupts the power supply to the load. Thus, all the power is supplied to the load straight from the AC grid. This operational principle ensures that fault clearing is effective as short circuit current can be drawn more from the AC grid than from the UPS. When the short circuit current is high enough, it is more likely that a selective load protection, implemented with fuses or circuit breakers, acts correctly. Furthermore, switching to bypass mode also protects the UPS from damages which the overcurrent may cause to the UPS itself. (1)

However, if the UPS is operating in stored-energy mode because of power failure in AC grid, the UPS should have the ability to supply enough short circuit current to clear the fuse or circuit breaker closest to the fault location for the selectivity of overcurrent protection to remain. The selectivity of overcurrent protection is discussed in Chapter 4.3.3.

3 THREE-LEVEL VOLTAGE SOURCE INVERTER IN DOUBLE CONVERSION UPS

A two-level inverter topology has been traditionally used in low-power voltage source inverters (VSI) to convert DC voltage to sinusoidal AC voltage. The two-level VSI has two voltage levels: positive and negative. The AC voltage is generated by switching the inverter output either to positive or negative DC voltage. Insulated gate bipolar transistors (IGBT) are generally used as power switching devices and pulse width modulation (PWM) technique is applied to control the switching sequence so that as sinusoidal as possible voltage will be produced. Three-phase two-level VSIs have in total eight different combinations for switching states which are used in modulation.

A three-level neutral point clamped (NPC) voltage source inverter was first introduced in 1981 (6). At present, three-level NPC inverters are widely used in UPS systems starting from 5 kVA power rating. They are developed from the two-level topology by adding a zero-potential level besides the positive DC and negative DC voltage levels which results in three voltage levels. In three-phase three-level inverters 27 different combinations for IGBT switching states are used in modulation. As a result, the harmonic content in the three-level inverter output is reduced compared to the harmonic content produced by the conventional two-level topology. Hence, the sinusoidal output voltage is closer to pure sine wave with three-level inverters when a proper PWM is applied. Furthermore, due to the added zero voltage level, the voltage stress across IGBTs in three-level topology may be approximately half of the voltage stress that IGBTs experience in two-level topology. Thus, the maximum voltage withstand levels required for IGBTs are smaller in three-level inverters than in two-level inverters with equivalent DC link voltage. The DC link voltage is the potential difference between positive and negative DC bus voltages. In addition, the reduced harmonics of three-level inverter give a possibility to reduce the size of a LC filter which is used at inverter output to filter the harmonic content of voltage and current. (7)

On the other hand, the three-level VSI implementation requires higher number of diodes and IGBTs in the inverter main circuit and two capacitors in the DC link. Added components increase the price and complexity of the three-level inverter compared to the two-level inverter. Nevertheless, the reduced harmonics and lower voltage stress across IGBTs provide advantages in the component sizing and in the efficiency due to less losses. Those factors make the three-level inverter a more reasonable solution than the two-level inverter especially in high-power UPS applications. (8)

In section 3.1 a topology of the three-phase three-level NPC inverter is presented. In subsection 3.1.1 operating principle and power loss calculation of IGBTs is presented. In subsection 3.1.2 operating principle and power loss calculation of diodes is presented

and in subsection 3.1.3 operating principle and characteristics of LC filter in the output of a UPS inverter is presented.

IGBTs in the inverter main circuit are principal components which limit the fault clearing capability of a UPS device. An LC filter is discussed more closely since in short circuit situations of a UPS load, the inductor of the LC filter limits the rate of output current change besides the fault inductance. In section 3.2 the principle for thermal calculation of IGBTs and diodes is presented. In section 3.3 a commonly used pulse width modulation technique in UPS inverters based on triangular carrier wave is presented.

3.1 Topology of the three-phase three-level NPC inverter

The topology of the three-phase three-level NPC inverter is presented in Figure 4. The direction of power flow is from DC to AC when the UPS is supplying a load. The inverter has 12 IGBTs T_1-T_{12} connected with anti-parallel diodes D_{T1}-D_{T12} which act as free-wheeling diodes. Diodes D_{T1}-D_{T12} are copacked within the IGBT. When the inverter is feeding an inductive load, anti-parallel diodes provide a current path for the load current at the times when the direction of the current is such that IGBTs are not conducting current. By providing a current path for the load current, they also protect IGBTs from suffering high voltage peaks which may otherwise emerge as a result of IGBTs turn off.

External diodes D_7-D_{12}, marked with a dashed line in Figure 4, are optional anti-parallel diodes used in some configurations to minimize power losses in copacked diodes D_{T1}-$D_{T12.}$ Power loss reduction in diodes D_{T1}-D_{T12} results in lower temperature rise of IGBTs during operation. Because a single external diode is connected in parallel with two series connected copacked diodes, forward voltage over a single copacked diode is smaller than forward voltage over the corresponding external diode. Thus, most of the reverse current flows through external diodes D_7-D_{12} instead of diodes D_{T1}-D_{T12} as forward voltage over diodes D_{T1}-D_{T12} may not be large enough to switch them on properly. Lower current which flows through diodes D_{T1}-D_{T12} leads to lower power loss in them.

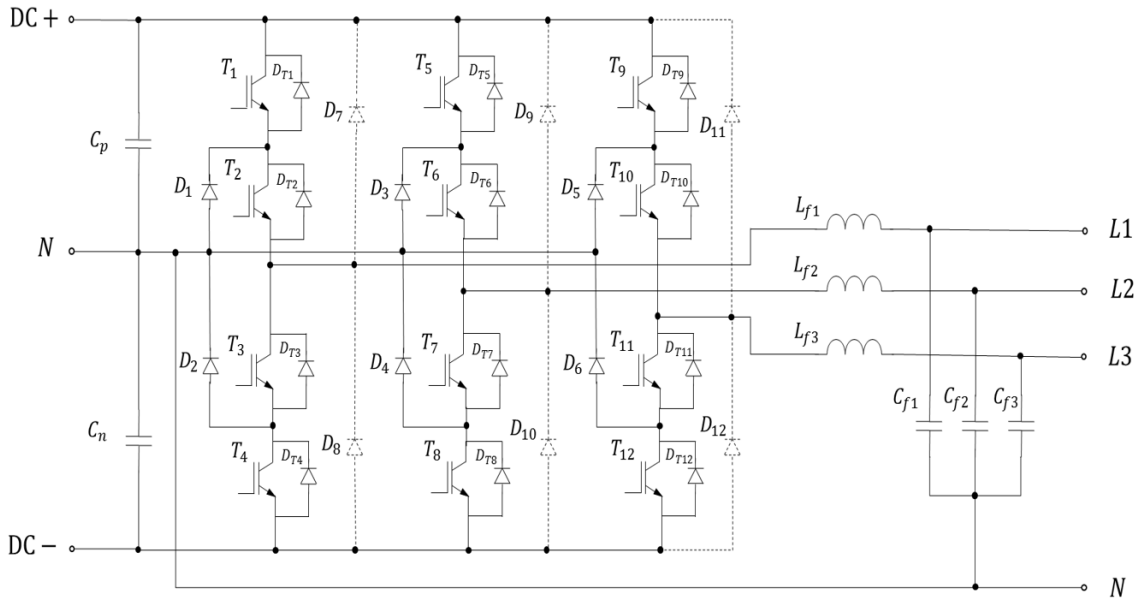

Figure 4: *Topology of the three-phase three-level NPC inverter. Optional diodes D_7-D_{12} are marked with a dashed line.*

Diodes D_1-D_6 are clamp diodes which enable the connection of output phases L1, L2 and L3 to the neutral point N of the inverter. The capacitor C_p is connected between the positive DC bus voltage and the neutral point and the capacitor C_n between the negative DC bus voltage and the neutral point. Capacitors C_p and C_n are called DC link capacitors and they maintain a constant DC bus voltage level and suppress the ripple in DC voltage. An LC filter is located in the inverter AC side. It mitigates harmonic current and voltage components of the inverter output and hence enhances the quality of the power supplied by the UPS.

3.1.1 IGBT and its power losses

An insulated gate bipolar transistor (IGBT) is a voltage-controlled power semiconductor switch. They are widely used in high power inverters due to their high voltage and current ratings compared to other power semiconductor switches such as metal-oxide-semiconductor-field-effect transistors (MOSFET) or bipolar junction transistors. Furthermore, IGBTs have a reasonable maximum switching frequency for power conversion purposes, varying usually between 5 kHz–150 kHz, and they are easy to control. (9)

The IGBT has three terminals: collector, emitter and gate. A circuit symbol of the IGBT with an anti-parallel diode is presented in Figure 5a, where C represents collector terminal, G represents gate terminal and E is the emitter terminal. Voltage applied to the gate terminal creates a potential difference U_{GE} between gate and emitter terminals. The gate-to-emitter voltage U_{GE} is used to control a conductance path between collector and emitter. When a positive voltage U_{GE} is applied to the gate terminal of the IGBT, the collector current I_c starts to flow in forward direction from collector to emitter. However, voltage U_{GE} has to be above the gate-to-emitter threshold voltage so that collector current

I_c will flow. Current I_c can not flow in reverse direction from emitter to collector due to the structure of P- and N-type semiconductor layers in the IGBT. In the P-type layer, charge carriers have a positive charge and in N-type they have negative. Therefore, IGBTs require anti-parallel connected diodes so that current can flow in both directions.

In Figure 5b is sketched theoretical waveforms of collector-to-emitter voltage U_{CE}, collector current I_c and gate-to-emitter voltage U_{GE} during a turn-on period t_{on}, a conduction period t_{cond} and a turn-off period t_{off} of the IGBT. In waveforms of Figure 5b, it is assumed that while the IGBT is not conducting and thus $I_c = 0$, the negative current from an inductive load flows through the anti-parallel diode. Figure 5b is illustrative and thus the scale may differ from reality.

During the turn-on period t_{on}, the collector current I_c begins to rise after the gate-to-emitter voltage U_{GE} has increased above the gate-to-emitter threshold voltage. Hence, the current begins to commutate from the anti-parallel diode to the IGBT of lower or upper branch in the main circuit. The spike in I_c waveform before stabilization to the constant load current value is caused by the reverse current of the anti-parallel diode which is developed due to the diode switching off. The reverse current of the diode is discussed more closely in Chapter 3.1.2. By adjusting the magnitude of $U_{GE,}$ the conductivity of the IGBT may be controlled and thus the stabilization value of I_c may be regulated. However, regulating the stabilization value of I_c by adjusting the magnitude of U_{GE} may cause significant power losses and heating of the IGBT. Thus, the aim is usually to switch on IGBTs properly by supplying enough U_{GE} voltage so that collector current I_c is not regulated. Flatten parts in U_{GE} waveform during t_{on} and t_{off} occur due to the internal structure of the IGBT as collector and gate has a capacitive connection. The collector-to-emitter voltage U_{CE} decreases when I_c increases and the decrease in U_{CE} becomes steeper after the peak in I_c as the diode reverse current begins to decrease. (9)

During conduction period t_{cond} the current I_c is constant if the load draws constant current through the IGBT and the value of U_{CE} is the voltage drop over the IGBT. The magnitude of the voltage drop over the IGBT in conduction state depends on the collector current I_c and junction temperature T_j.

When the IGBT switches off, the gate to emitter voltage U_{GE} is decreased. Shortly after the U_{GE} has started to decrease, the collector-to-emitter voltage U_{CE} begins to rise. After the voltage U_{GE} has dropped below the required level to sustain the collector current $I_{c,}$ the collector current decreases rapidly. The spike in U_{CE} during collector current cut-off results from stray inductances in the circuit. After the voltage U_{CE} has stabilized, collector current I_c still remains and causes losses. Thus, IGBT is not fully switched off until all the collector current has vanished. (9)

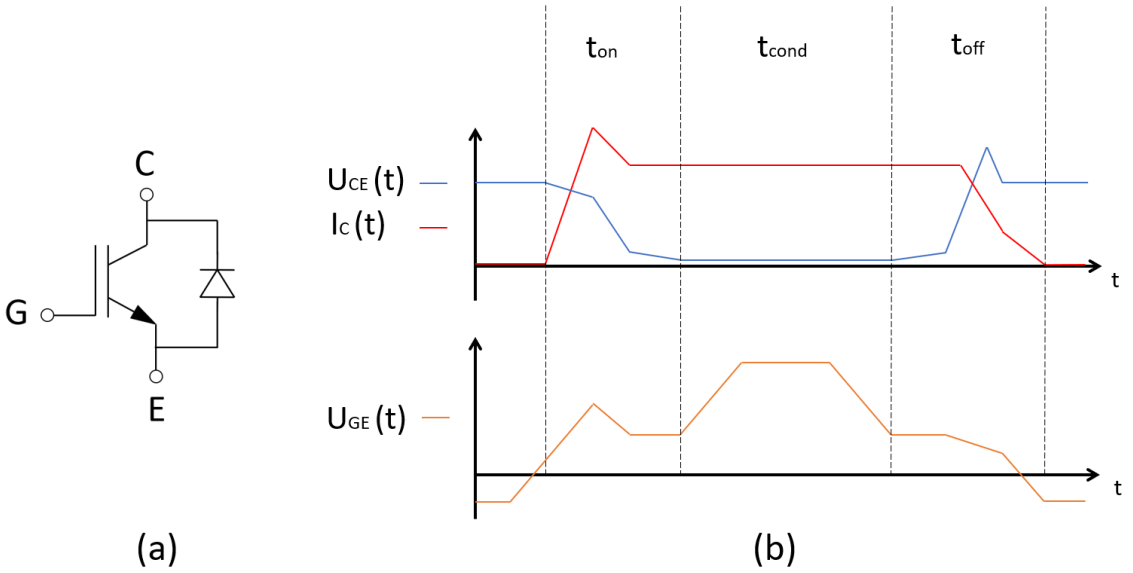

Figure 5: *a) Circuit symbol of the IGBT with an anti-parallel diode. b) Theoretical current and voltage waveforms of an IGBT during turn-on (t_{on}), conduction state (t_{cond}) and turn-off (t_{off}).* (9)

IGBTs produce power losses during conduction period t_{cond} and switching periods t_{on} and t_{off} because the collector current I_c is above zero and at the same time there is a voltage drop U_{CE} across the IGBT. Hence, total power losses of the IGBT are divided into switching losses and conduction losses. Power losses produce heating of the IGBT and the IGBT may overheat whether cooling of the IGBT is insufficient. Overheating may result into destruction of the IGBT. Therefore, when the current limit of UPS inverter is increased, a loss calculation of IGBTs is essential. With the loss calculation, it can be ensured, whether the junction temperature of the IGBT is within the ranges given by the IGBT manufacturer when maximum output current of the inverter flows through the IGBT.

Switching losses of the IGBT are composed of turn-on losses, which occur during t_{on}, and turn-off losses, which occur during t_{off}. In inverter circuits, the amount of IGBT power loss during a single switching event depends on collector current, DC bus voltage, gate drive resistance, junction temperature and stray inductances. The gate drive resistance and stray inductances affect on switching delays and current rise time. As consequence of longer switching delays and current rise time, switching losses will grow. IGBT manufacturers offer usually graphs of switching losses in IGBT datasheets. Switching losses are usually presented as a function of collector current at certain collector-to-emitter voltage, junction temperature and gate drive resistance. The collector-to-emitter voltage is approximately equal to the DC bus voltage when the IGBT is in non-conducting state in inverter circuit. The average switching power loss of the IGBT over cycle T can be expressed as

$$P_{sw} = \frac{1}{T}\sum_{i=1}^{Tf_{sw}}\left[E_{on}(t_i) + E_{off}(t_i)\right], \quad (1)$$

where f_{sw} is the switching frequency, E_{on} is the energy consumption of turn-on at switching time instant t_i, E_{off} is the energy consumption of turn-off at switching time instant t_i and Tf_{sw} is equal to number of switchings during one cycle. (10)

The average conduction power loss of IGBT over cycle T can be expressed as

$$P_{cond} = \frac{1}{T}\int_0^T U_{CE}(t)I_c(t)\,dt\,. \tag{2}$$

The higher the junction temperature is, the higher the conduction losses are as voltage drop U_{CE} over the IGBT increases with increasing junction temperature. (10)

The average total power loss of IGBT over cycle T is expressed as the sum of conduction and switching losses in Equations (1) and (2)

$$P_{tot} = P_{cond} + P_{sw}, \tag{3}$$

where P_{tot} is the average total power loss of IGBT.

In Figure 4, IGBTs T_2, T_3, T_6, T_7, T_{10} and T_{11} experience higher conduction losses than other IGBTs during normal operation of the inverter and during operation at current limit. This is because of they are in conductive state when the output phase is connected to negative or positive DC bus but also when the output phase is connected to the neutral. Therefore, current ratings of above mentioned IGBTs in the inverter main circuit designs are often scaled higher than current ratings of other IGBTs which has to conduct only when the output phase is connected either to negative or positive DC bus.

3.1.2 Diode and its power losses

Diodes are two-terminal semiconductor components, often made of silicon, and they consist of two electrodes: anode and cathode. They are uncontrolled components which let current to flow in forward direction from anode to cathode but block the reverse signed current flow from cathode to anode. Characteristics of the diode result from the structure of the diode. The anode is doped with charge carriers of positive charge, yielding a P-type semiconductor region, and cathode is doped with charge carriers of negative charge, yielding an N-type semiconductor region. Hence, they are called pn-diodes. In power diodes, an i-type region, which is slightly doped with negative charge carriers, is added between p- and n-type regions to enhance the voltage rating of the diode and thus they are called pin-diodes. Pin-diodes are used in high power applications where current and voltage ratings of general pn-diodes are insufficient. Circuit symbol of the diode and structure of the pin-diode in principle are presented in Figures 6a and 6b, where the character A depicts anode and K depicts cathode. (9)

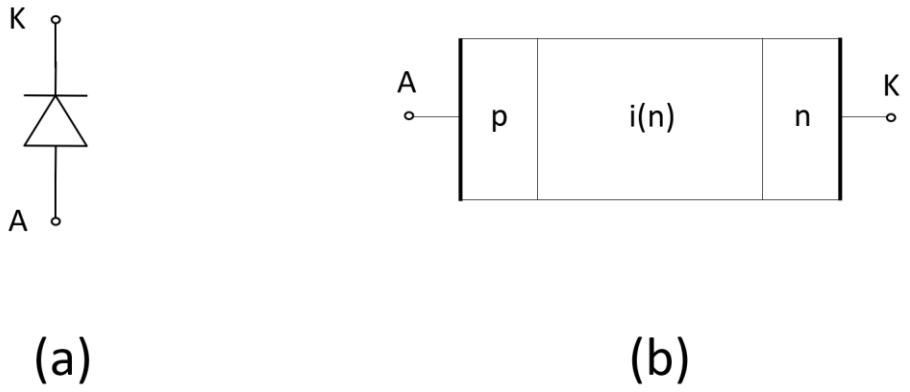

Figure 6: *a) Circuit symbol of the diode b) Structure of the pin-diode in principle*

Similar to IGBTs discussed in Chapter 3.1.1, diodes have also conduction, turn-on and turn-off losses which cause heating of the diode. When a voltage, which is above diode's threshold voltage, is applied to the diode in forward direction, current will start to flow through the diode from anode to cathode. The diode is fully turned on after the turn-on delay and the forward current and voltage will stabilize to their final values. Current I_F flowing through the diode causes a voltage drop U_F in the diode due to the internal resistance of the diode. Figure 7 illustrates current and voltage waveforms of the diode during turn-on of the diode t_{d_on}, conduction state t_{d_cond} and turn-off t_{d_off}.

During turn-on, the resistivity of the diode is high which results in a spike in diode's voltage which is shown in Figure 7 as U_{FP}. However, the turn-on delay is typically very low and therefore turn-on losses of the diode are negligible compared to turn-off and conduction losses. Thus, turn-on losses may generally be omitted in loss calculations of the diode as their influence on total losses is low. Waveforms in Figure 7 are illustrative and thus the scale may differ from reality. (9)

In conduction state, the average power losses of the diode over cycle T are calculated according to equation

$$P_{cond,diode} = \frac{1}{T}\int_0^T U_F(t) I_F(t)\, dt\,. \tag{4}$$

In addition to current I_F and voltage drop U_F, junction temperature of the diode affects to conduction losses. Voltage drop U_F increases as the forward current I_F increases. However, the increase in junction temperature may reduce the voltage drop U_F in silicon diodes and therefore conduction loss of the diode may decrease at higher junction temperatures. (10)

In inverters, diodes are turned off by forced commutation when current commutates from the diode to the IGBT. Thus, a reverse voltage is applied to the diode and current decreases rapidly in the diode when it commutates to the IGBT. However, when the current decreases rapidly and reaches the zero value, the number of charge carriers in

the I-region of the diode has not decreased to zero yet and hence the diode has low resistance. It leads to a negative current during turn-off as shown in Figure 7. This negative current is called the reverse recovery current of the diode. The negative peak in reverse recovery current I_{prr} causes also a peak in reverse recovery voltage U_{prr} before the reverse voltage stabilizes to its final value U_R. The magnitude of the I_{prr} depends on the rate of change of the decreasing current $\frac{di}{dt}$. The steeper the slope is, the higher is the magnitude of the peak reverse recovery current I_{prr}. The value of $\frac{di}{dt}$ is defined by the characteristics of the IGBT where the current commutates from the diode because the current decreases in the diode at the same rate as it increases in the IGBT. Thus, the gate drive resistance of the IGBT and stray inductances define the value for diode $\frac{di}{dt}$. (9)

In Figure 7, the time t_{rr} is the reverse recovery time. It is measured from the zero point of the current, when the sign of the current changes from positive to negative, to the point at which the straight line drawn through the peak reverse recovery current I_{prr} and point 0,25* I_{prr} crosses the zero. Diode manufacturers declare often in the datasheet of a diode a value for Q_{rr} which is a reverse recovery charge. It is defined as the area under the current curve defined by I_{prr} and t_{rr} as shown in Figure 7 with slash lines.

Reverse recovery energy E_{rec} is the energy loss which occurs in the diode during a single turn-off. The magnitude of forward current of the diode before turn-off, reverse voltage U_R, rate of change of the current $\frac{di}{dt}$ and junction temperature influence the magnitude of the reverse recovery energy. When turn-on losses of the diode are omitted, the average switching loss of the diode over cycle T can be expressed as

$$P_{sw,diode} = \frac{1}{T} \sum_{i=1}^{Tf_{sw}} E_{rec}(t_i)\,, \tag{5}$$

where f_{sw} is the switching frequency, $E_{rec}(t_i)$ is the reverse recovery energy, or turn-off energy loss, at time instant t_i when the diode turns off and Tf_{sw} is equal to number of switchings during one cycle. However, the reverse recovery energy E_{rec} is not always given in the datasheet of the diode. Nevertheless, E_{rec} may be estimated by means of reverse voltage U_R and reverse recovery charge Q_{rr} which is usually given in the datasheet of the diode.

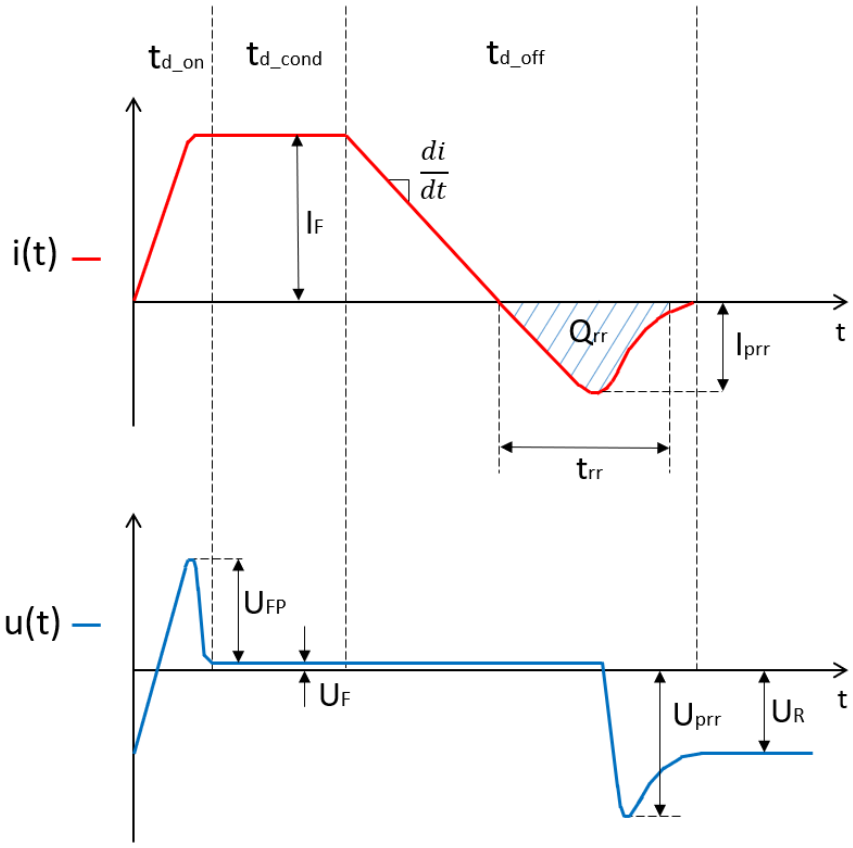

Figure 7: *Current and voltage waveforms of a diode during turn-on (td_on), conduction state (td_cond) and turn-off (td_off).*

In (11) is proposed, that the area of Q_{rr} in Figure 7 may be estimated by approximating the reverse recovery current waveform and calculating the area of a triangle which height is I_{prr} and base t_{rr} as shown in Figure 8. The area of the triangle can be divided into sections Q_s and Q_f according Figure 8, where $Q_{rr} = Q_s + Q_f$ and $t_{rr} = t_a + t_b$. The charge Q_f during t_b advances the reverse recovery energy E_{rec} because E_{rec} may be approximated by multiplying the charge with the reverse voltage. The reverse voltage affects across the diode after the peak in reverse current I_{prr} occurs and thus the reverse recovery energy E_{rec} is increasing during t_b. Therefore, the charge Q_s during t_a does not have influence on E_{rec} as the reverse voltage across the diode is zero. Thus, Q_f has to be extracted from Q_{rr} when the reverse recovery energy E_{rec} is approximated.

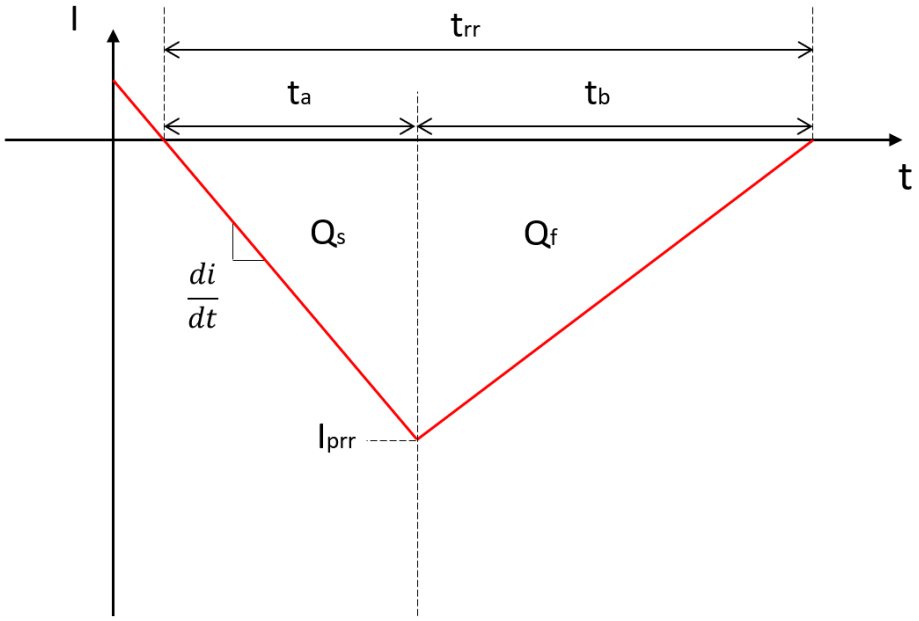

Figure 8: *Approximated reverse recovery current waveform.*

Reverse recovery energy can then be calculated as

$$E_{rec} = Q_f U_R = \frac{s}{s+1} Q_{rr} U_R, \tag{6}$$

where U_R is the reverse voltage and $s = \frac{Q_f}{Q_s}$ is a softness factor of the diode. In soft-recovery diodes the softness factor s is high and thus the slope of the reverse current during t_b is lower than in diodes which recover abruptly. Therefore, soft-recovery diodes cause smaller voltage spikes in the circuit than abruptly recovering diodes as the induced voltage in the circuit, due to the stray inductances and rate of change of the current, is lower. However, soft-recovery diodes generally have lower maximum reverse voltage values than abruptly recovering diodes as the i-region is doped irregularly in soft-recovery diodes. (9,11)

Diodes can be divided into normal rectifier diodes and fast diodes according to the reverse recovery time t_{rr}. In the industry, some manufacturers specify the diode fast when its reverse recovery time is below 500 ns. Fast soft-recovery diodes are generally used in inverter circuits. They withstand higher switching frequencies than normal rectifier diodes which have a longer reverse recovery time. However, conduction losses are generally higher in fast diodes than in rectifier diodes which limit the current carrying capability of fast diodes. (9)

3.1.3 LC filter

The LC filter consists of three filter inductors L_{f1}, L_{f2} and L_{f3} and three filter capacitors C_{f1}, C_{f2}, C_{f3} which can be seen from Figure 4. Inductors are connected in series with the

inverter and load and capacitors are connected on the grid side between inverter output phases and neutral. The LC filter reduces the total harmonic distortion (THD) of the inverter output voltage and current by attenuating high frequency voltage and current components which are developed due to the pulsating IGBT switching.

The impedance of filter inductors comprises mainly from inductive reactance X_L which increases directly proportional to the frequency f according to equation

$$X_L = 2\pi f L, \tag{7}$$

where L is the inductance of the inductor. Thus, inductors L_{f1}, L_{f2} and L_{f3} provide a low impedance path for the current component of fundamental frequency and high impedance path for high frequency current components. This results in attenuation of high frequency current and voltage components. If a short circuit or a low-impedance ground fault occurs in the load side of the UPS and UPS starts to operate at current limit, the inductance of the filter inductor is the only factor which limits the rate of change of the current whether other inductances in the circuit are negligible. Correspondingly, the rate of change of the current affects on power losses of IGBTs and diodes in the inverter when UPS operates at current limit. The rate of change of the current affects to power losses because it affects to lengths of conduction periods and to switching frequencies of IGBTs and diodes. Thus, the inductance of the filter inductor must be considered in power loss calculations of IGBTs and diodes. The impact of filter inductor on the rate of change of the current is discussed more closely in Chapter 4.1.

The impedance of capacitors comprises mainly from capacitive reactance X_c which decreases inversely proportional to the frequency f according to equation

$$X_c = \frac{1}{2\,\pi f C}\,. \tag{8}$$

Hence, capacitors C_{f1}, $C_{f2,}$ C_{f3} shunt high-frequency current components by constituting them a low impedance current path and they are directed away from the UPS output. Due to filter capacitors the size of filter inductors may be reduced and more effective filtering may be reached compared to a filter solution where only filter inductors would be used. Reduction in filter size results in lower inductance and inductive reactance on fundamental frequency and thus voltage losses are cut. Therefore, the capacitance of capacitor should be as high as possible and the inductance of inductor minimized to achieve as low as possible voltage loss on fundamental frequency due to the filtering. Consequently, a trade-off between capacitance and inductance values should be found when designing the LC filter. (12,13)

The LC filter starts to attenuate harmonics with a rate of 40 dB/decade on frequencies after the resonance frequency f_{res} (12). The resonance frequency is dependent on inductance L and capacitance C values of the filter according to equation

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} . \quad (9)$$

However, the LC filter amplifies harmonics near the resonance frequency f_{res} due to the resonance effect which is caused since the impedance of inductor and capacitor cancel each other on the resonance frequency. Thus, the resonance frequency of the filter should be adjusted on frequencies where the voltage harmonics are inherently low. In addition, it has been presented that the resonance frequency should be clearly above the fundamental frequency of the system but clearly under the switching frequency of the inverter according to equation

$$10\, f_{fund} < f_{res} < 0{,}5 f_{sw}, \quad (10)$$

where f_{fund} is the fundamental frequency and f_{sw} is the switching frequency. (12,14)

3.2 Thermal calculation of IGBTs and diodes

A careful thermal design is indispensable when power semiconductor devices are selected for an inverter. Heating of IGBTs or diodes occurs always as a result of power losses when IGBTs or diodes are conducting current. The temperature is increased the most in the junction area of the IGBT or diode because the power dissipation originates in the junction. However, the increase of the junction temperature reduces the expected lifetime of an IGBT or a diode (15). IGBTs or diodes may suffer serious damages leading to failures in their operation if the maximum operating junction temperature is exceeded. Maximum operating junction temperatures of IGBTs and diodes are typically on the order of 150ºC or 175ºC. For minimizing the temperature rise in the junction, heat should be conducted away from the junction as effectively as possible. Thus, air or liquid cooled heatsinks are mounted on cases of IGBTs and diodes in inverters. Heatsinks are usually made from copper or aluminum due to good heat conduction characteristics of them. Heat dissipation in the junction is conducted to the case of the IGBT or diode and from the case into the heatsink which has a high thermal capacity. Accordingly, the rise of the junction temperature may be restricted compared to the situation where heatsinks are not used as heat transfer from the case to the heatsink may be significantly greater than from the case to the ambient air.

Typically, heat conduction characteristics between junction and case and between junction and ambient are described in datasheets of IGBTs and diodes as thermal resistances $R_{th(j\text{-}c)}$ and $R_{th(j\text{-}a)}$. In addition, thermal response from junction to case as a function of time of a current pulse is given in datasheets as transient thermal impedance curve $Z_{th(j\text{-}c)}(t)$. Values given in the $Z_{th(j\text{-}c)}(t)$ curve may be used in thermal calculations of IGBTs and diodes when IGBTs and diodes are conducting current transiently and duration of a single pulse is short, typically below 1 second. When duration of a single current pulse

draws nearer to 1 second, the $Z_{th(j-c)}$ *(t)* curve may saturate to a value which is equal to the value of thermal resistance $R_{th(j-c)}$. Thus, $R_{th(j-c)}$ is the maximum value of $Z_{th(j-c)}$ *(t)* curve and the value of $R_{th(j-c)}$ may be used in thermal calculations when IGBTs or diodes are powered continuously or for a longer current pulse time.

Junction temperatures of IGBTs and diodes can not be directly measured. However, they can be evaluated by measuring the collector to emitter voltage U_{CE} of the IGBT or forward voltage U_F of the diode by supplying small measurement current through the IGBT or diode when they are cooling down after being loaded by a constant power P_L. Magnitudes of U_{CE} and U_F are temperature dependent and thus junction temperatures can be evaluated by measuring U_{CE} or U_F values. With above mentioned indirect junction temperature measurements, power semiconductor manufacturers may create $Z_{th(j-c)}$*(t)* curves for datasheets of IGBTs and diodes. Junction temperature values achieved by indirect measurements may be referred to virtual junction temperatures T_{vj}, because they represent average temperature values in the junction. In truth, temperature may differ within the junction and local hot spots may exist. (16,17)

The thermal behavior of power semiconductor components may be sketched with two different thermal equivalent circuit models: with a Cauer model and a Foster model. In the Cauer model it is necessary to know physical properties and construction of materials in all layers between the points where the thermal impedance is desired for being solved. Hence, when the temperature difference is calculated, for example, between the junction and case of the IGBT, thermal capacitances of all material layers and thermal resistances between them must be known if the Cauer model is applied. Material layers in this case may denote silicon, solders, metals and ceramic which may lie between the junction and case inside the IGBT. On the other hand, the Cauer model makes it also possible to calculate temperatures in internal layers. The equivalent thermal circuit between junction and case implemented as Cauer model is presented in Figure 9 where R denotes thermal resistance, C denotes thermal capacitance, T_j is the temperature in the junction and T_c is the temperature on the case. (17)

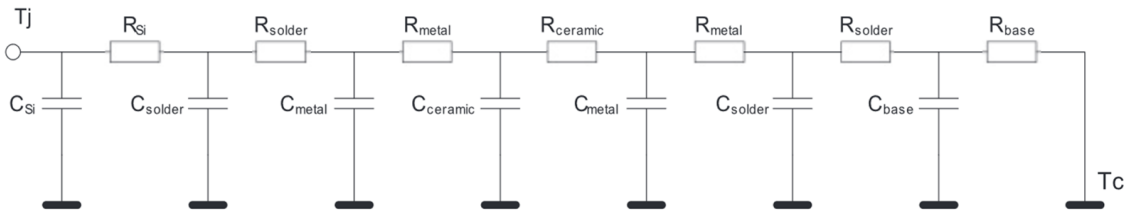

Figure 9: *Cauer model of thermal impedance between junction and case.* (17)

Contrary to the Cauer model, in the Foster model values of thermal resistance R and thermal capacitance C do not have any physical meaning. Instead the values for R and C are selected in a manner that the analytical function described as

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right), \tag{11}$$

where t is the length of the current pulse in seconds, n is the number of RC-terms and τ_i is equal to $R_i * C_i$, is fitted to the $Z_{th(j-c)}$ curve which is attained by measurements in a way explained earlier in this Chapter. The experimentally achieved $Z_{th(j-c)}$ graph is commonly presented in datasheets of IGBTs and diodes. Furthermore, parameters for R and C terms required in the Foster model may be afforded besides the $Z_{th(j-c)}$ graph. As a result, values for $Z_{th(j-c)}$ at different current pulse lengths may be calculated analytically according to Equation (11). The number of RC-terms required in Foster model varies, however, usually the number of terms shall be four or more so that the accuracy of the Foster model is sufficient (18). The equivalent thermal circuit between junction and case implemented as Foster model is presented in Figure 10. Number of RC-terms in Figure 10 is three and T_j denotes temperature in the junction while T_c stands for temperature on the case. (17)

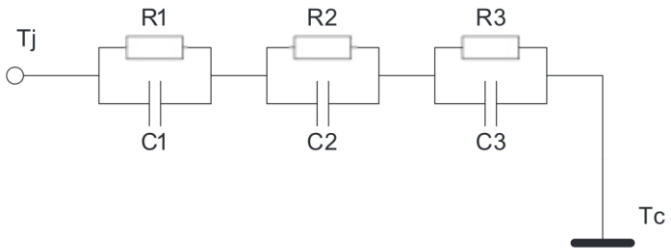

***Figure 10**: Foster model of thermal impedance between junction and case when the number of RC-terms is three.* (17)

Cauer and Foster models may also be connected in series for calculating the temperature, for example, between the junction and air. Then, if heatsink is used, thermal impedances between the case and heatsink and between heatsink and air must be solved. A thermal interface material (TIM) such as thermal grease is usually used between the case and heatsink for achieving a proper thermal connection. Then thermal characteristics of TIM and firmness of the coupling determine the thermal impedance between the case and heatsink. (17)

Temperatures at opposite ends of the thermal equivalent circuit model can be calculated when temperature at the other end, magnitude of the power loss of the semiconductor component and thermal impedances of the thermal equivalent circuit model are known. Thermal impedances are summed together if they are series connected in the model. Thus, for example, the junction temperature of a semiconductor component may be calculated with the following equation when the temperature of the heatsink is known

$$T_j(t) = P_L(t) * \left(Z_{th(j-c)}(t) + Z_{th(c-h)}(t)\right) + T_h(t), \tag{12}$$

where P_L is the power loss of the semiconductor component, $Z_{th(j-c)}$ is thermal impedance between junction and case, $Z_{th(c-h)}$ is thermal impedance between the case and the heatsink

and T_h is the heatsink temperature at time instant t. In the simulation part of this thesis, average junction temperatures of IGBTs and diodes are evaluated according to Equation (12). Average power loss calculated for an IGBT or diode over one cycle is used as P_L and heatsink temperature T_h is assumed to be constant. The maximum value of $Z_{th(j-c)}(t)$ curve in the IGBT or diode datasheet or thermal resistance $R_{th(j-c)}$ is used as $Z_{th(j-c)}(t)$ value. A value for $Z_{th(c-h)}(t)$ is calculated according to the data gained from the specification of TIM. (16)

3.3 Pulse width modulation

Pulse width modulation techniques are employed in inverters for controlling the output voltage and frequency of the inverter. In three-phase three-level NPC inverters, each output phase may be connected either to positive or negative DC bus voltage or to zero potential depending on which IGBTs and diodes are in conducting state. A pulse width modulator controls switching sequences of IGBTs by producing a control signal which in this thesis has a value of 1, 0 or -1. The control signal value is given as input for a complex programmable logic device (CPLD) which turns on and off certain IGBTs according to the signal value. The signal value determines on which of the three potential levels the CPLD connects output phases of the inverter. Thus, the control signal forms a pulse sequence and the width of single pulses determines, how long the output phase is connected to positive or negative DC bus voltage or to zero potential. In three-phase inverters, three control signals are required since switchings of IGBTs at each output phase are controlled by a separate control signal.

In this thesis, a pulse width modulation technique based on a triangular carrier wave comparison is presented. In this PWM method, a triangular carrier wave is compared to a sinusoidal reference waveform which has the same frequency as desired for the AC voltage at inverter output. The frequency of the carrier wave is equal to the switching frequency of the inverter which is limited by characteristics of IGBTs. The frequency of the carrier wave should be clearly above the fundamental frequency of the reference waveform so that the quality of the output voltage of the inverter is maintained. The higher the switching frequency is, the less the output voltage of the inverter contains harmonic distortion, however, switching losses of IGBTs may increase. When the triangular wave is used as carrier wave instead of the sawtooth wave, less harmonics are produced as a result of modulation. (19)

In three-phase three-level inverters, where the PWM technique based on the triangular carrier wave comparison is used, two triangular carrier waves and three sinusoidal reference waveforms are compared in the modulation. Two carrier waves are required in the modulation due to the three potential levels of the three-level inverter. The first carrier wave may have values between zero and one and the second may have values between zero and minus one. Reference waveforms have a 120º phase shift between each other.

Carrier waves may be in phase with each other or may have 180º phase shift between each other but frequencies of carrier waves shall be equal. (19)

The principle of the modulation is, that when the reference waveform is higher than either of the triangular carrier waves, the modulator produces a control signal with a value of one. In that case, the respective output phase of the reference waveform will be connected to the positive DC bus voltage. For example, when the phase L1 in Figure 4 is connected to the positive DC bus voltage, IGBTs T_1 and T_2 are turned on, whereas IGBTs T_3 and T_4 are in non-conducting state. Thus, when the direction of the positive current is towards the load, the positive current may flow through IGBTs T_1 and T_2. Whether the current is negative, the current may flow through diodes D_{T1} and D_{T2} to the positive DC link capacitor C_p. If optional diodes are applied, the negative current may flow through the diode D_7.

When the value of the reference waveform is smaller than the first triangular carrier wave but higher than the second triangular carrier wave, the modulator outputs a control signal with a value of zero. Then, the respective output phase of the reference waveform will be connected to the neutral N. It denotes that when, for example, the phase L1 is connected to the neutral N, IGBTs T_2 and T_3 in Figure 4 are turned on and IGBTs T_1 and T_4 are in off state. Consequently, positive current may flow through the IGBT T_2 and the diode D_1 to the load and negative current through the IGBT T_3 and the diode D_2 to the ground.

At the times, when the value of the reference waveform is below both carrier waves, the respective output phase of the reference waveform will be connected to the negative DC bus voltage. Hence, in the case of phase L1, for instance, IGBTs T_3 and T_4 are turned on while IGBTs T_1 and T_2 are in non-conducting state. The positive current towards the load may flow through diodes D_{T3} and D_{T4}. Whether optional diodes are used, positive current may flow through the diode D_8. Negative current to the negative DC link capacitor C_n may flow through IGBTs T_3 and T_4.

When an output phase is switched from a potential level to another, a delay occurs between switchings of IGBTs. This delay is called a dead time and its magnitude is usually a few microseconds. In three-level inverters, the dead time may prevent IGBTs from being exposed to overvoltage. For example, when the L1 phase is switched from the positive DC voltage level to zero voltage level, the IGBT T_1 is first turned off and the IGBT T_3 is not turned on until the dead time has elapsed after the T_1 turn-off. This will protect the IGBT T_4 from overvoltage. Whether, IGBTs T_1, T_2 and T_3 would momentarily be in conductive state at the same time, the whole DC link voltage would influence over the IGBT T_4. Thus, the IGBT T_4 may be damaged if the DC link voltage exceeds the collector-to-emitter breakdown voltage of T_4.

The output voltage of the inverter may be controlled by changing the modulation index which is expressed as

$$m = \frac{\hat{u}_r}{\hat{u}_c}, \tag{13}$$

where $\hat{u}_r$ is the peak value of the reference wave and $\hat{u}_c$ is the peak value of the carrier wave. The inverter operates in a linear modulation region, when the peak value of the reference wave is below the peak value of the carrier wave. Thus, the maximum value for the modulation index is $m = 1$ in the linear modulation region. Whether the peak value of the reference waveform exceeds the peak value of the carrier wave and thus $m > 1$, inverter operates in an overmodulation region. Output voltage of the inverter may be increased when the inverter operates in the overmodulation region, however, the total harmonic distortion of the output voltage may increase. (20,21)

Sinusoidal reference phase-to-neutral voltage waveforms for three phases L1, L2 and L3, which are required in the modulation, may be expressed as

$$u_{rL1}(\omega t) = m \sin(\omega t) \tag{14}$$

$$u_{rL2}(\omega t) = m \sin\left(\omega t - \frac{2}{3}\pi\right) \tag{15}$$

$$u_{rL3}(\omega t) = m \sin\left(\omega t - \frac{4}{3}\pi\right), \tag{16}$$

where m is the modulation index and ω is the angular frequency of the reference waveform. Reference waveforms u_{rL1}, u_{rL2} and u_{rL3} with two triangular carrier waves are presented in Figure 11 for one cycle T. The modulation index is 0.9 in graphs of Figure 11. In addition, respective control signals u_{cL1}, u_{cL2} and u_{cL3}, which determine the voltage level where the output phase is connected at different times, are presented. (20)

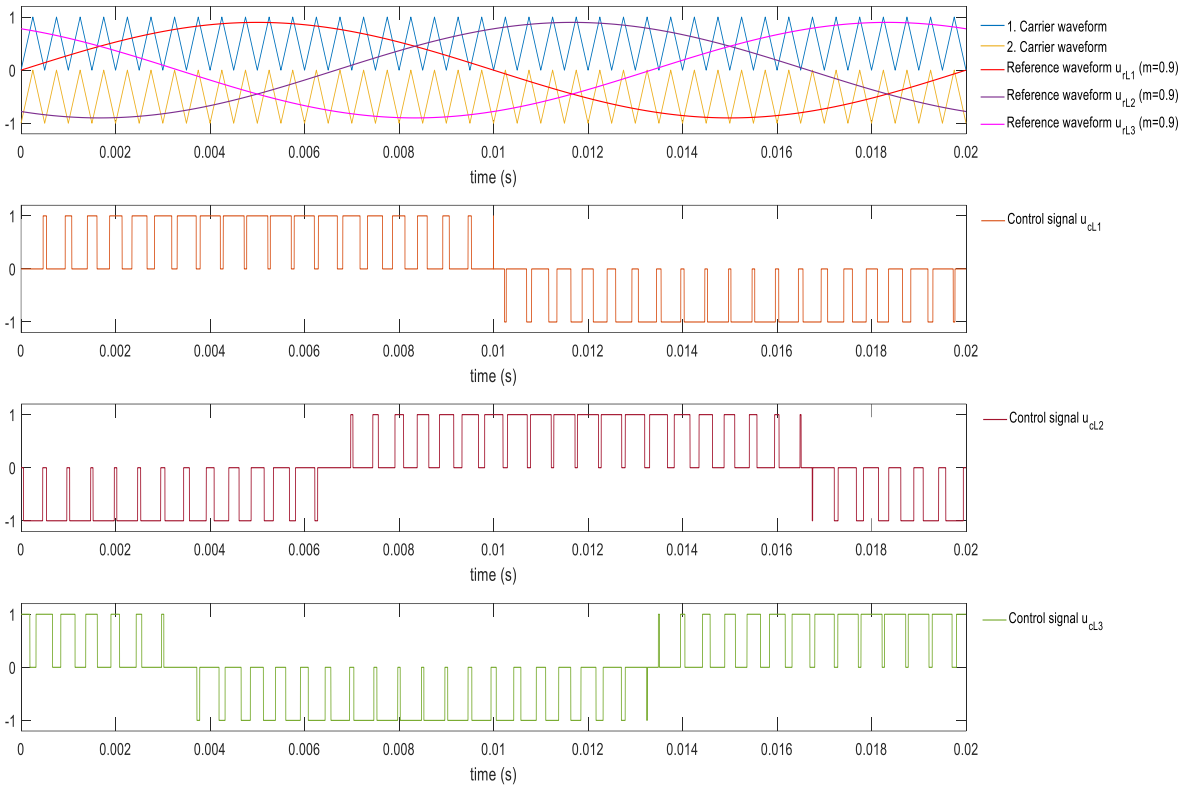

Figure 11: *Principle of the pulse width modulation technique based on carrier wave comparison for a three-phase three-level inverter.*

When the inverter operates in linear modulation region, the amplitude of the fundamental frequency component of the phase-to-neutral voltage is equal to

$$U_{ph,fund} = m\frac{U_d}{2}, \tag{17}$$

where U_d is the DC link voltage of the inverter and m is the modulation index. (20) Thus, the highest amplitude of the fundamental frequency component of the phase-to-neutral voltage in the linear modulation region is $\frac{U_d}{2}$, which is achieved when $m = 1$. Then the maximum phase-to-phase voltage of the inverter is equal to $\frac{\sqrt{3}}{2}U_d$. (22)

In (22) is disclosed that approximately 15.5- percent increase in the amplitude of the fundamental frequency component of the phase-to-neutral voltage is achieved in the linear region by adding a third harmonic component to the sinusoidal reference voltage waveforms. The added third harmonic component have an amplitude which is one-sixth of the amplitude of the fundamental component. Hence, the peak amplitude of the increased fundamental frequency component $\frac{2}{\sqrt{3}} \approx 1{,}1547$ is diminished by $\frac{1}{6} \approx 0{,}166$ and the reference phase-to-neutral voltage waveform stays in linear region when $m \leq 1$. Nevertheless, the whole DC link voltage can now be utilized in the phase-to-phase voltage of the inverter as $\frac{\sqrt{3}}{2} * \frac{2}{\sqrt{3}}U_d = U_d$. When the third harmonic component is added similarly to all phase-to-neutral voltages, they cancel each other from phase-phase voltages and

from phase voltages in three-phase loads. Therefore, adding the third harmonic component does not increase the total harmonic distortion of phase-to-phase voltages. However, if a three-phase UPS is feeding one-phase loads, this kind of modulation technique may not be advised as the third harmonic voltage component remains between the phase and neutral. Reference phase-to-neutral voltage waveforms, where the third harmonic component is added may be expressed as

$$v_{rL1}(\omega t) = \frac{2}{\sqrt{3}} m \left(\sin(\omega t) + \frac{1}{6}\sin(3\omega t)\right) \tag{18}$$

$$v_{rL2}(\omega t) = \frac{2}{\sqrt{3}} m \left(\sin\left(\omega t - \frac{2}{3}\pi\right) + \frac{1}{6}\sin(3\omega t)\right) \tag{19}$$

$$v_{rL3}(\omega t) = \frac{2}{\sqrt{3}} m \left(\sin\left(\omega t - \frac{4}{3}\pi\right) + \frac{1}{6}\sin(3\omega t)\right), \tag{20}$$

where $m \leq 1$ when the inverter operates in linear modulation region. (20,22)

4 FAULT CLEARING

This chapter discusses different faults and magnitudes of fault currents which may occur at the UPS output, operation principle of the UPS inverter operating at current limit and circuit breakers which are used in the load side of the UPS to isolate faults from other parts of the grid. The operating principle of the UPS inverter at current limit determines the shape of the output current waveform of the UPS device if a short circuit or ground fault occurs in the UPS output. Therefore, the operating principle of the UPS inverter is presented in detail in this chapter as the algorithm of the simulation model developed in this thesis is based on the shape of the current waveform. In addition, a fault clearing circuitry which may be installed externally beside a UPS device to improve the fault clearing capability of a UPS device is presented in this chapter.

4.1 Short circuits and ground faults

Short circuits are electrical faults where a low impedance path for current occurs between phases or neutral in AC systems or between positive and negative poles in DC systems. Due to the low impedance path, current may rise rapidly to high values. In three-phase AC systems short circuits can be divided into phase-to-phase faults, where short circuit happens between two phases, and three-phase faults, where short circuit happens between three-phases. In addition, the short circuit can happen in three phase systems between one or more phases and neutral if there is a neutral conductor. Typically, UPS devices have a neutral terminal in the output. In single-phase AC systems short circuit can happen between the phase and neutral. An example which may cause a short circuit fault in UPS output would be a metallic tool forgotten between phase conductors in equipment or device that serves as UPS load. In that case, the metallic tool acts as a low impedance current path between phases when the UPS is started to supply power to the load.

Ground faults are electrical faults, where a conductive path occurs between a live conductor and ground. Thus, current flows to ground as not intended. The difference in fault current between short circuits and ground faults is that, the magnitude of fault current may not always rise to high current values in ground faults. The magnitude of fault current depends on impedance in the fault current path both in short circuits and ground faults. However, in ground faults the fault impedance may be significantly higher than the fault impedance in short circuits and thus the magnitude of fault current may be lower in ground faults than in short circuits. Ground faults may emerge, for example, due to the degradation of electrical insulation in UPS load equipment. Because of the insulation failure, current may flow to ground via the grounded equipment frame.

Short circuits can be depicted with equivalent resistive-inductive (RL) circuits as shown in Figure 12, where U is a constant voltage from the source, such as a DC-link voltage of the inverter. In Figure 12, the short circuit occurs between points A and B and

the respective fault current path is drawn between them. Resistance *R* and inductive reactance X_L of the fault circuit result from resistivity and inductivity of conductors and filter inductor of the inverter. In addition, the fault location may contain inductance and resistance which has to be considered when fault current waveform is evaluated. However, in short circuits impedance of the fault location may be very small and thus negligible. (23)

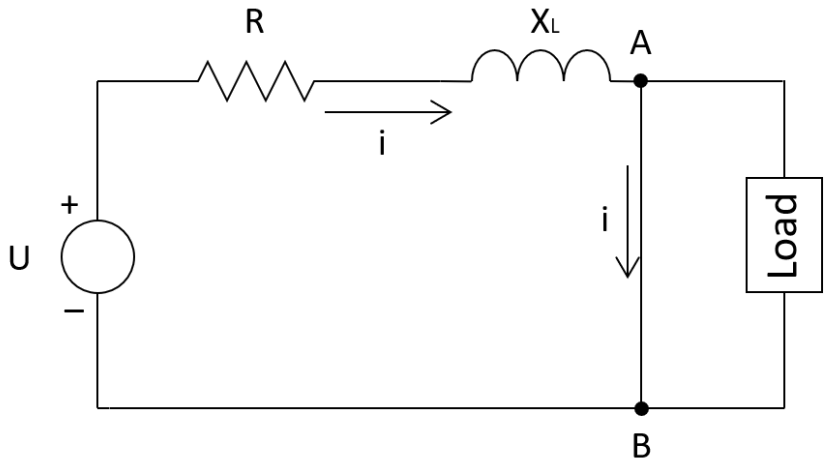

Figure 12: *Equivalent circuit model of short circuit which occurs between points A and B with DC voltage source.*

Voltage equation for the circuit in Figure 12 can be written according to Kirchhoff's voltage law

$$u = Ri + L\frac{di}{dt}\,. \tag{21}$$

By solving the differential equation, the fault current magnitude at time instant *t* can be evaluated as

$$i = \frac{u}{R}\left(1 - e^{-\frac{t}{T}}\right), \tag{22}$$

where $T = \frac{L}{R} = \frac{X_L}{2\pi f R}$ and e is Euler's number. In Equation (22) is assumed that the initial current of the fault is zero. If the initial current is not equal to zero, the DC offset current expressed as

$$i_{dc} = i(0) * e^{-\frac{t}{T}}, \tag{23}$$

where *i(0)* is the initial current of the fault, should be summed to Equation (22) to get the total fault current magnitude at time instant *t*. The DC offset component is characterized by the ability of inductor to store energy. (23) Hence, the total fault current magnitude at time instant *t* can be expressed as

$$i_{tot} = \frac{u}{R}\left(1 - e^{-\frac{t}{T}}\right) + i(0) * e^{-\frac{t}{T}}. \quad (24)$$

If a short circuit or a low-impedance ground fault happens in the load side of a UPS when the supply grid is not available, a UPS inverter starts to operate at current limit. The UPS inverter operation at current limit is presented in Chapter 4.2. The UPS inverter limits the output current by switching the faulted phase alternately between positive DC bus, neutral, and negative DC bus in a way that current does not exceed preset current levels. Thus, Equation (24) can not be directly applied for inverter short circuit calculations as inverter controls the current magnitude by switching sequences which is not considered in Equation (24). Nevertheless, Equation (24) for current magnitude is valid between single switching sequences when current either increases, is constant or decreases.

Total inductance L of the fault circuit can be expressed as the sum of inductance of conductors L_g and inductance of the filter inductor L_f. If the fault circuit resistance R is assumed to be very small, as it in short circuits usually is, inductances L_g and L_f in the fault circuit and the voltage U affect on the rate of change of the fault current supplied by the inverter according to equation

$$\frac{di}{dt} = \frac{u}{L_g + L_f}\ . \quad (25)$$

The voltage U is in fault situations either positive DC bus voltage, negative DC bus voltage or zero voltage depending on which bus the output phase is connected via IGBTs or diodes. The inductance L_g is dependent on the length and cross-sectional area of cables between the UPS and the fault location. The longer the cable is, the higher the inductance is but by enlarging the cross-sectional area of the cable, the inductance may be diminished (24). However, the UPS is often located near the load and hence the inductance of the filter inductor L_f may usually have larger influence on the rate of change of the fault current than inductance of conductors L_g.

The inductance of the filter inductor L_f for a 20 kW UPS varies from few dozens of microhenries to few hundreds of microhenries depending on the current flowing through the inductor. The inductor consists of a coil which is wrapped around a core. The core material used in filter inductors of UPS devices is usually iron-silicon (Fe-Si) powder or iron-silicon-aluminum (Fe-Si-Al) powder. Fe-Si powder core provides better DC bias characteristics and lower losses than a powder core made only from iron. DC bias characteristics of the core material denotes the dependency between permeability μ in the core

material and the magnetic field intensity H which acts as a magnetizing force for the core. (25)

A growing current through the inductor creates a growing magnetic field intensity H inside the inductor as H is directly proportional to the current magnitude and number of turns in the coil. The increasing magnetic field intensity H increases the magnetic flux density B in the core material. However, at a certain point, which is dependent on the core material, the magnetic flux density B saturates in the core when H is raised. After the saturation, the magnetic flux density B in the core does not increase significantly anymore even though magnetic field intensity H is increased by increasing the current. When B approaches saturation in the core due to increasing H, the permeability μ in the core material decreases because μ is defined as the ratio of magnetic flux density B and the magnetic field intensity H according to equation

$$\mu = \frac{B}{H} . \tag{26}$$

Inductance of the filter inductor L_f is not a constant as it is directly proportional to the permeability μ in the core. Thus, when high currents flow through the inductor, for example due to a short circuit, the inductance L_f of the filter inductor decreases as the permeability μ decreases in the core. It leads to a weakened ability of the inductor to resist changes in the current magnitude which leads to higher $\frac{di}{dt}$ values at high currents according to Equation (25). (26)

In (24) is derived an equation to calculate the self-inductance of a straight conductor. According to the equation, for example, a 15 m copper cable with a cross-sectional area of 6mm^2 would result in self-inductance of 27,7 µH. Hence, the maximum total inductance resisting current changes in fault situation may be usually only around few hundreds of microhenries for a 20 kW UPS. Therefore, very high values of $\frac{di}{dt}$ will be generated in short circuits or low-impedance ground faults as the DC bus voltage is usually on the order of several hundreds of volts.

4.2 UPS inverter operation at current limit

The inverter in a UPS device is adjusted to limit the maximum output current that may be supplied to the load. Therefore, if a short circuit happens in the UPS output or the UPS is overloaded, the UPS may not be able to supply as much output current as the load or faulty circuit would inherently draw. Particularly in short circuit situations, the UPS has to limit the output current as the output current would otherwise rise rapidly to high values due to a low impedance path.

The output current of the inverter must be limited since high currents flowing through IGBTs or diodes in the inverter main circuit may increase the junction temperatures of IGBTs or diodes above permissible levels. Consequently, IGBTs or

diodes may be damaged or destroyed. Thus, maximum operating junction temperatures of IGBTs and diodes are major factors limiting the maximum collector or forward currents of IGBTs and diodes. The maximum collector or forward current may be usually increased by sufficient cooling of IGBTs and diodes. Increasing the magnitude of the collector or forward current increases also power losses in the IGBT or in the diode which results in heating of the IGBT or diode. However, by cooling, the heating may be compensated. Thus, defining the magnitude of the current limit for the inverter is always case-specific which depends on cooling of the semiconductor devices and switching frequency of IGBTs and diodes since switching losses also increase junction temperatures of IGBTs and diodes. In addition to junction temperatures, IGBT and diode manufacturers apprise safe operating areas for IGBTs and diodes according to their maximum current and voltage carrying capabilities. Maximum operating currents and voltages of IGBTs and diodes must not be exceeded even though junction temperatures of IGBTs and diodes would be kept within the allowed area by efficient cooling.

The current limit for the inverter is usually determined by estimating the highest current magnitude that IGBTs and diodes can carry for a limited time without exceeding their maximum operating junction temperatures or safe operating areas declared by manufacturers of semiconductor components in datasheets. The switching frequency and the effect of cooling must be taken into account when an adequate current limit value for the inverter is estimated. It is also a common practice to leave a certain safety margin between estimated junction temperatures and maximum junction temperatures declared by semiconductor device manufacturers when the current limit is defined. Hence, the risk that the current limit value is defined too high due to an error in the estimation of the junction temperature may be diminished. Furthermore, maximum junction temperature values announced by IGBT and diode manufacturers may be optimal since those values may be verified at specific test conditions. Thus, they may not be suitable for being directly applied to varying real-world conditions.

When the UPS operates at current limit, IGBTs are switched on and off in a way that the current flowing through IGBTs of an output phase does not exceed the pre-determined maximum or minimum current limit values of a half cycle. A comparator compares the magnitude of the current flowing through IGBTs with the maximum and minimum current limit values. If a short circuit happens in the UPS output, currents in corresponding output phases may rapidly increase and the rate of change of the current is only limited by the impedance of the fault circuit. When the current reaches the maximum current limit value in a three-level inverter of a UPS, the output phase will be connected to the opposite voltage level via the zero-voltage level.

For example, in the case of the three-level inverter topology presented in Figure 4, if a short circuit happens between L1 and L2 phases when the output phase L1 is connected to the positive DC bus voltage level, the current in phase L1 may increase rapidly through IGBTs T_1 and T_2. Eventually, the current may reach the maximum current limit value adjusted for the inverter. When the maximum current limit value is reached, the phase L1 will be connected to the zero-voltage level which means that the IGBT T_1 in

Figure 4 is switched off and IGBT T_3 is switched on. The principle on how the output phase may be connected to different voltage levels is explained more closely in Chapter 3.3. When the output phase is connected to the zero-voltage level, the positive current may flow through the IGBT T_2 and diode D_1. The phase L1 is kept connected to the zero-voltage level for the time of a dead time t_{dead} as illustrated in Figure 14. If it is assumed that the impedance of the fault circuit consists only of inductive reactance and hence the circuit has zero resistance, the current will be constant when the output phase is connected to the zero-voltage level according to Equation (21). In the real world, of course, the small amount of resistance caused by for example non-ideal conductors and output filter inductor of the UPS, will cause the current gradually to decrease when the output phase is connected to the zero-voltage level.

After the dead time t_{dead} has elapsed, the phase L1 will be connected to the negative DC bus voltage level by turning off the IGBT T_2 and turning on the IGBT T_4. Consequently, the positive current starts to decrease rapidly and, whether external diodes are used, current may flow through the diode D_8. If external diodes are not used in the configuration, the positive current would flow through diodes D_{T3} and D_{T4}. The positive current will decrease for the time t_{fall} until the minimum current limit value of the positive half-cycle is reached as shown in Figure 14. Then the phase L1 will be connected again to the zero-voltage level and, after a dead time t_{dead} has passed, L1 will be connected again to the positive DC bus voltage level until the current reaches the maximum current limit value after a current rise time t_{rise} as illustrated in Figure 14. Current rise and decrease times are dependent on DC bus voltages and impedance of the fault circuit according to Equation (25). In addition, of course, the difference between respective maximum and minimum current limit values affects on magnitudes of t_{rise} and t_{fall}.

The switching sequence described above is continued when the fundamental reference waveform of the PWM is on the positive half cycle. The illustrative waveform of the current flowing through the filter inductor of the inverter during inverter operation at current limit with a 50 Hz fundamental frequency is presented in Figure 13. Maximum and minimum current limit values during positive half cycle are depicted as i_{max} and i_{min} and corresponding current limits during negative half cycle as $-i_{max}$ and $-i_{min}$. The purpose of Figure 13 is only to be explanatory and thus the switching frequency in Figure 13 is smaller than typically in UPS inverters where it may be dozens of kilohertz. Figure 14 presents a more detailed graph of current waveform with corresponding switching sequences of semiconductor devices when the UPS operates at current limit on positive half cycle. Abbreviations T_1, T_2, D_1, D_8, D_{T3} and D_{T4} depict equivalent components stated in Figure 4. In current waveforms of Figures 13 and 14 it is assumed that the fault circuit has a zero resistance and a constant inductance. If the variation of the inductance along with the change of the current magnitude would be considered, shapes of current waveforms in Figures 13 and 14 would be more curved instead of straight.

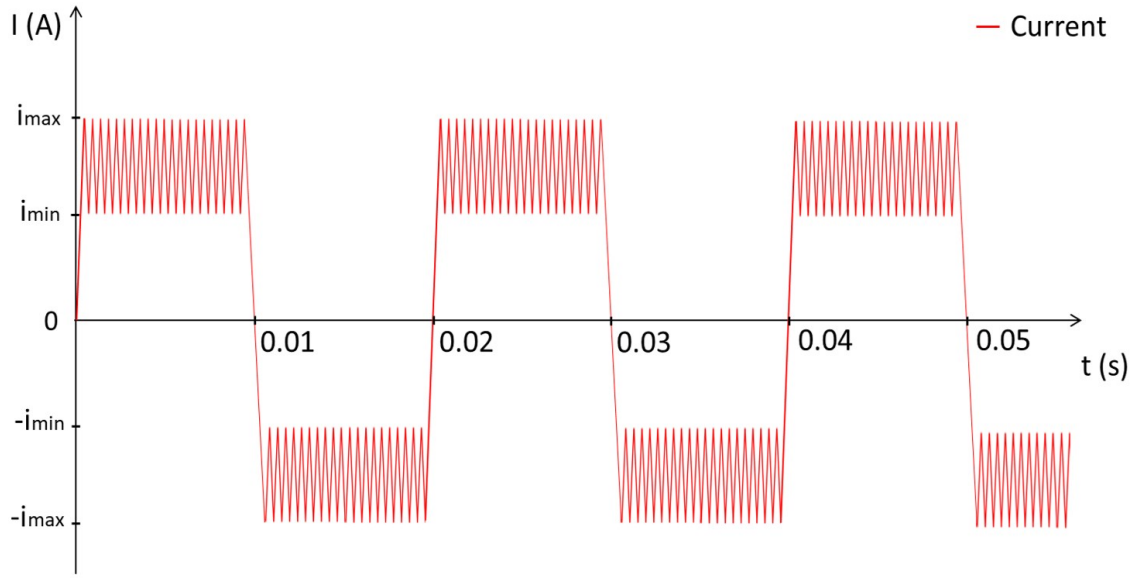

Figure 13: *Illustrative waveform of the current flowing through the filter inductor when the inverter operates at current limit.*

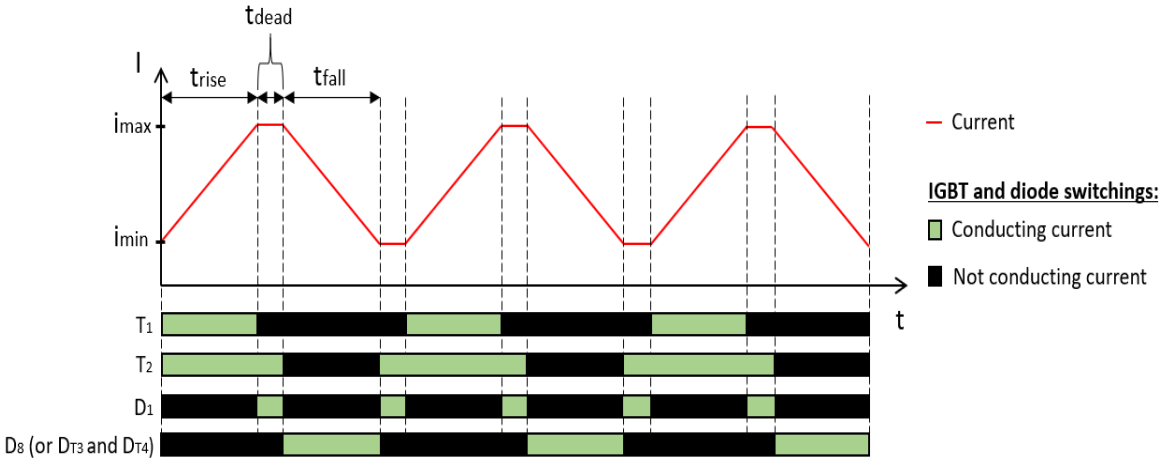

Figure 14: *Detailed graph of the current waveform on positive half-cycle when UPS inverter operates at current limit with corresponding IGBT and diode switchings.*

When the current is on the negative half cycle, it may flow through opposite semiconductor components than in the case of positive half cycle. It denotes that the output phase is connected to the negative DC bus voltage until the negative current through IGBTs T_3 and T_4 attains the maximum negative current limit value. Then the output phase will be connected to the positive DC bus voltage level via the zero-voltage level in a manner described in Chapter 3.3. Accordingly, the current will start to approach the minimum negative current limit value. The UPS inverter will operate at current limit until the faulty network is cleared or in maximum for a pre-set current limit time which is typically a few hundreds of milliseconds.

The maximum current limit value should be adjusted to be as high as possible since during AC grid fault situations, a high fault current contributes a selective fault

clearing with overcurrent protective devices in the network supplied by the UPS. However, as the maximum current limit value is often adjusted close to the ultimate performance values of power semiconductor devices, power semiconductor devices are exposed to high thermal stress. Therefore, a time for the inverter to operate at current limit must be limited to prevent IGBTs or diodes from falling into thermal runaway. Whether, the maximum time limit for the inverter to operate at current limit is exceeded the UPS may trip and disconnect itself from the supplied network. If the fault is cleared by the overcurrent protective device when the UPS is operating at current limit, the UPS may cease the operation at current limit and continue to supply remaining UPS loads with conventional current magnitudes.

4.3 Circuit breakers in general

Overcurrent is defined as current flowing in the circuit which exceeds the rated current value of conductors or electrical equipment in the circuit. Short circuits and ground faults are examples of incidents which may cause overcurrent. Furthermore, overcurrent occurs in overload situations. As a result, overcurrent may lead to overheating of conductors and malfunction of the electrical equipment in the circuit. Overheat in conductors may result in deterioration of insulation materials, melting of conductor and in worst case it may lead to fire. Circuit breakers and fuses are used to protect conductors and electrical equipment from overcurrent conditions. A difference between fuses and circuit breakers is that fuses must always be replaced with a new one after they are blown. Circuit breakers, however, can be reset after they are tripped and hence be operated again. Furthermore, circuit breakers can be used as manual on-off switches in circuits which is not possible with fuses. (27,28)

A circuit breaker is defined in the standard (29) as “a mechanical switching device, capable of making, carrying and breaking currents under normal circuit conditions and also making, carrying for a specified duration and breaking currents under specified abnormal circuit conditions such as those of short circuit”. Circuit breakers come in different classes according their voltage and current ratings. In Chapter 4.3.1 miniature circuit breakers, which belong to molded case circuit breaker class (MCCB) are introduced. Tripping characteristics of the miniature circuit breaker determines a delay on how quickly the circuit breaker operates in different overcurrent situations. Tripping characteristics of miniature circuit breakers are presented in Chapter 4.3.2 and co-ordination of circuit breakers so that selective overcurrent protection is ensured, is discussed in Chapter 4.3.3. (30)

4.3.1 Miniature circuit breakers

The International Electrotechnical Commission (IEC) is a worldwide organization for standardization in the electrical field. It provides in its standard IEC 60898 requirements for circuit breakers used in households and similar installations for overcurrent protection. In industry and in colloquial language these circuit breakers are also known as miniature

circuit breakers (MCB). MCBs are molded case circuit breakers with a pole width of 25.4 millimetres (1 inch) or less and their current ratings are 125 A or below. Number of poles varies from single-pole circuit breakers to four-pole circuit breakers. They are commonly used in residential applications at phase voltages varying from 120VAC to 240VAC. Maximum current breaking capacity of a typical MCB is between 5 – 15 kA. MCBs protect the connected load and conductors mechanically from overcurrent. Depending on the magnitude of the overcurrent, thermal trip unit or magnetic trip unit is triggered in MCB to break the overcurrent. High overcurrent, which usually results from short circuit or ground fault, triggers the magnetic trip unit and lower overcurrent, which may result from overload, usually triggers the thermal trip unit. Magnetic tripping is instantaneous whereas thermal tripping has a delay. Figure 15 represents a simplified structure of a MCB and its parts. (27,30)

Thermal trip unit is made up of a bimetal strip which consists of two metals having different rate of heat expansion coupled together. When current flows through the bimetal, the bimetal strip is heated and it bends towards a trip bar because two metals expand at different rate. A prolonged overload eventually leads to contacts opening when the bimetal strip bends and pushes the trip bar which opens the latch to separate the contacts. The higher the current is and the longer time the current flows the more the bimetal heats because of the bimetal's impedance. Thus, both time and current magnitude affect to thermal tripping. (27)

Magnetic trip unit is an electromagnet which is often made up of a coil twisted around a ferromagnetic material. Current, which flows through a circuit breaker, flows also through the coil which creates a magnetic field attracting an armature. The armature is attached to the trip bar and hence the trip bar turns when a magnetic force pulls the armature. A short circuit or ground fault may cause a rapidly increasing overcurrent through the circuit breaker and an electromagnet directs an increasing magnetic force to the armature and finally the bended trip bar triggers the latch to separate the contacts. Generally, the larger the overcurrent the quicker the circuit breaker trips and breaks the current flow when magnitude of the overcurrent is within the limits of circuit breaker's rating. (27,30)

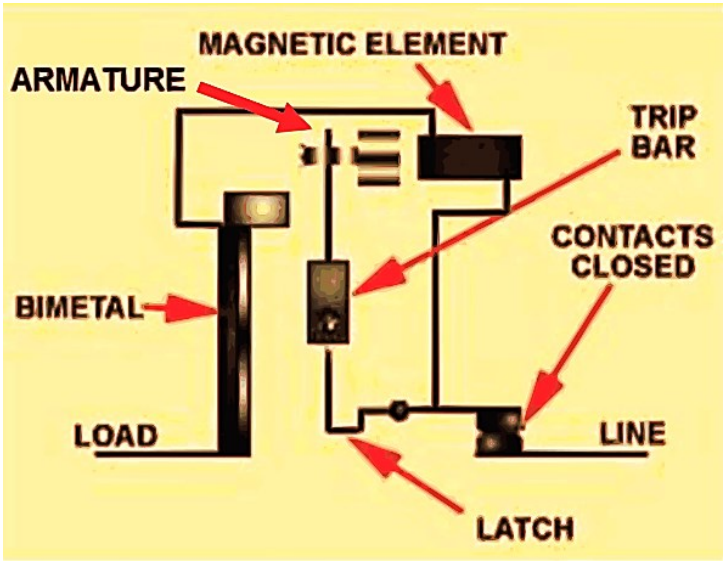

Figure 15: *Structure of a typical miniature circuit breaker (adapted from IEEE P1458 draft* (27)*)*

4.3.2 Tripping characteristics of MCB

The IEC standard 60898 divides miniature circuit breakers into three different types according to ranges of instantaneous tripping: B, C and D. Instantaneous tripping, also known as magnetic tripping, is triggered by a magnetic trip unit of a circuit breaker and therefore it requires always an overcurrent which is several times the rated current of the circuit breaker. Figure 16 shows typical tripping curves of B, C and D type circuit breakers. Time is illustrated on the y-axis and current on the x-axis as multiples of the circuit breaker's rated current I_n. Magnetic tripping zone starts from point 3 I_n for B-type circuit breakers, from 5 I_n for C-type and from 10 I_n for D-type. Those starting points can be seen from Figure 16 as points where the tripping curve of each type drops vertically downward. Thermal tripping zone of each type is the zone starting from point 1,13 I_n to the point where the magnetic tripping zone of each type begins. Thermal tripping is triggered by a thermal trip unit. (31,32)

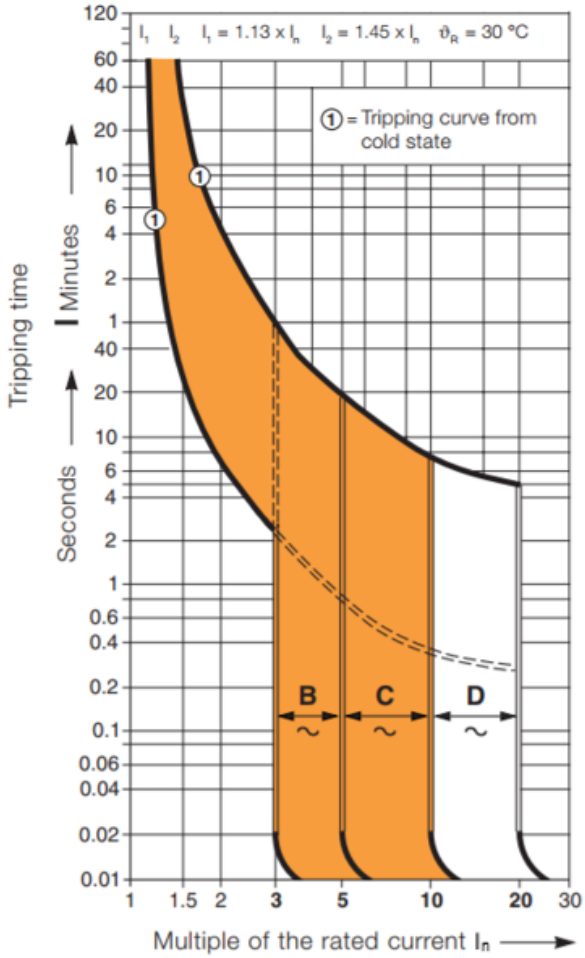

Figure 16: *Typical time-current characteristics of B-, C- and D -type circuit breakers (adapted from* (31)*).*

Table 1 lists current thresholds for type B, C and D circuit breakers as multiples of rated current I_n which are required in the standard concerning the instantaneous tripping of the circuit breaker. For instantaneous tripping, the standard sets two different current thresholds for each type of circuit breaker with the difference of required tripping time. For the lower current threshold, it is required that a circuit breaker shall not trip in less than 0,1 s and for the higher current threshold it is required that a circuit breaker must trip in less than 0,1 s.

The magnetic tripping zone, which is the area between these current thresholds, can be considered as a tolerance for instantaneous tripping. The instantaneous tripping of different circuit breakers may differ within the tolerance even though they would be same type and comply with the IEC 60898 standard. The standard requires only that the instantaneous tripping, in less than 0,1 s, should occur within the tolerance or at least on the higher current threshold. Therefore, when examining and choosing a circuit breaker from the fault clearing point of view, the higher current threshold of magnetic tripping is usually a point of interest because the instantaneous tripping operation is most reliable on the higher threshold or above. For example, C-type miniature circuit breakers, which comply with the IEC 60898 standard, will trip in less than 0,1s when the current is 10 times the

rated current of the circuit breaker or above. Practically, the more the current is above the threshold the faster and more reliable the circuit breaker operates to interrupt the current. However, the overcurrent value must be less than the rated short circuit capacity of a circuit breaker so that circuit breaker can reliably interrupt the current. (32)

It is notable to consider that circuit breakers, in accordance with the IEC 60898 standard, are designed to operate with sinusoidal 50 Hz or 60 Hz current and rated currents of circuit breakers and their multiples are specified as rms values. Thus, a circuit breaker may not operate as intended if the current is other shape than sinusoidal such as square wave shaped or pure DC. The instantaneous tripping of a circuit breaker is commonly designed to operate in accordance with the peak value of a sinusoidal current. The rms value of a square wave is the same as the peak value of the square wave whereas the peak value of a sinusoidal wave is $\sqrt{2}$ times the rms value of a sinusoidal wave. Therefore, a circuit breaker may not operate similarly with square wave shaped current and sinusoidal current even though both currents would have the same rms value. Generally, the current thresholds in Table 1 should be multiplied with a factor $\sqrt{2}$ if the circuit breaker is used with pure DC or square wave shaped current so that instantaneous tripping acts correctly. (32)

Table 1: *Instantaneous tripping requirements in accordance with IEC 60898 standard.*

Tripping time	B-type CB	C-type CB	D-type CB
> 0,1s	3 I_n	5 I_n	10 I_n
< 0,1s	5 I_n	10 I_n	20 I_n

The standard IEC 60898 sets uniform tripping time and current characteristic requirements for B, C and D type circuit breakers with same rated current when current is in the thermal tripping zone. However, exceptions do exist depending on whether the rated current of the circuit breaker is more or less than 63 A or 32 A. The standard sets three current thresholds and tripping or non-tripping time requirements for thresholds and they are presented in Table 2. The standard requires that B, C and D type circuit breakers with rated current 63 A or less must not trip in less time than one hour when conventional non-tripping current 1,13 I_n is flowing through the circuit breaker. The same non-tripping time requirement is less than 2 hours for CBs with rated current over 63 A. (32)

If conventional tripping current 1,45 I_n is passed through the circuit breaker, CBs with rated current 63 A or below should trip in less than 1 hour and CBs with rated current above 63 A should trip in less than 2 hours. Table 2 shows that the tripping time should be between 1 s and 60 s or 1 s and 120 s depending on the rated current when the current passed through the CB is 2,55 I_n. At these current thresholds circuit breakers in accordance with the IEC 60898 standard generally interrupt the current flow by means of triggering the thermal trip unit.

Current thresholds are valid when ambient air temperature is 30 °C. Lower ambient temperatures increase current thresholds and higher temperatures decrease current thresholds. Typically, miniature circuit breakers are rated for temperatures between -5 °C and 40 °C. The standard requires that CBs in the ambient temperature of -5 °C should trip at current value of 1,9 I_n within the conventional time which is 1 hour for CBs of rated current 63 A or below and 2 hours for CBs of rated current above 63 A. In the ambient temperature of 40 °C circuit breakers should not trip within the conventional time when the rated current I_n is passed through the circuit breaker. (32)

Table 2: *Time-current characteristic requirements in accordance with IEC 60898 standard.*

Current	B, C, D –type CBs
1,13 I_n (conventional non-tripping current)	No tripping, $t \leq 1$ h (for CBs with $I_n \leq 63$ A) No tripping, $t \leq 2$ h (for CBs with $I_n > 63$ A)
1,45 I_n (conventional tripping current)	Tripping, $t < 1$ h (for CBs with $I_n \leq 63$ A) Tripping, $t < 2$ h (for CBs with $I_n > 63$ A)
2,55 I_n	Tripping, 1 s $< t <$ 60 s (for CBs with $I_n \leq 32$ A) Tripping, 1 s $< t <$ 120 s (for CBs with $I_n >$ 32A)

4.3.3 Selective co-ordination of circuit breakers

Electric systems in households, in factories or in similar facilities are often built in a way that power is supplied from a single main line to several branch lines which supply loads. In networks with a UPS, the UPS may be installed on the main line. Thus, the UPS supplies several parallel connected loads via branch lines. Each branch line and the main line is equipped with a circuit breaker or a fuse to protect wires and loads from overcurrent. Miniature circuit breakers are often used in branch lines as downstream protective devices. (33)

Selectivity of overcurrent protection means that protection devices are co-ordinated in a way that in fault situations the protection device, which is closest to the fault location, regarded from the supply side, operates first and breaks the fault current while other protection devices do not operate. Hence, the fault is isolated and other parts of the circuit or network may continue normal operation. Figure 17 illustrates the fulfilment of selective overcurrent protection in a UPS network where the UPS supplies two parallel connected loads via branch lines. When the fault, such as a short circuit, occurs in the marked location in Figure 17, only the downstream protective device marked with red outlines trips while other protective devices do not trip.

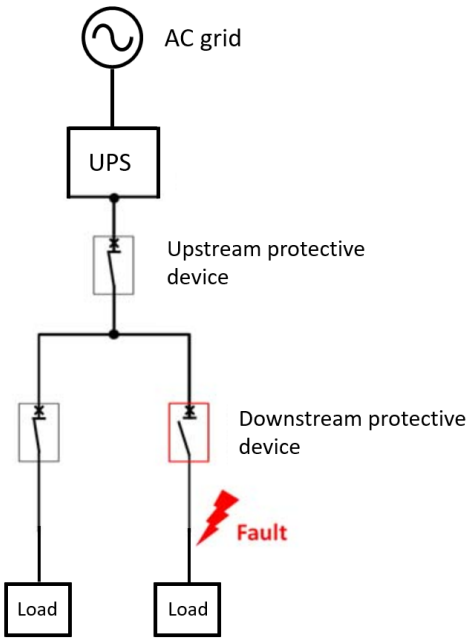

Figure 17: *Selective overcurrent protection. Only the downstream protective device marked with red outlines trips (adapted from* (33)*).*

Circuit breakers or fuses, however, may not be able to break the current above their rated ultimate breaking capacity I_{cu} which is defined as the rms value of AC current. Therefore, back-up protection is required. Back-up protection is implemented with circuit breakers or fuses in the upstream side which has higher rated ultimate breaking capacity than overcurrent protection devices in the downstream. Consequently, the protection device in the upstream may break the fault current if the protection device in the downstream fails to break the current. In this case, of course, the selective overcurrent protection is not reached. Nevertheless, the back-up protection provided by the upstream protective device may prevent the fault current from causing severe damage to conductors and other circuit equipment or danger to persons close to the faulted electrical equipment. (33)

Operating characteristics of overcurrent protective devices in the network are selected such that the overcurrent selectivity and back-up protection are ensured. Selectivity can be divided into total selectivity and partial selectivity. Total selectivity is a situation, where the selectivity is ensured up to the ultimate breaking capacity I_{cu} of the downstream breaker. Thus, it is the optimal situation. However, it requires that the fault current or prospective short circuit current of the circuit is below the value of I_{cu}. The prospective short circuit current is defined as "the current that would appear in a short-circuit without any other change of the supply conditions" (29). In addition, non-current limiting circuit breakers, whose tripping time is delayed in the magnetic tripping zone, must be used as upstream breakers. (33)

Short-time delay is the time that circuit breaker will carry short circuit current in magnetic tripping zone before tripping. For example, such molded case circuit breakers, which have electronic trip units, allow the adjustment of a short-time delay. Hence, they are suitable to be used as upstream breakers to ensure the back-up protection and enable the total selectivity when their tripping time is adjusted to be delayed. (33)

Current-limiting circuit breakers, which operate fast and without additional delay in magnetic tripping zone, are often used as downstream circuit breakers. Thus, they reduce the duration of fault current and prevent fault current to reach its peak value. Miniature circuit breakers are, for example, current-limiting circuit breakers. The fulfilment of total selectivity can be evaluated by comparing tripping curves of downstream and upstream protective devices. Their tripping curves shall not cut each other, as shown in Figure 18, so that total selectivity may be possible.

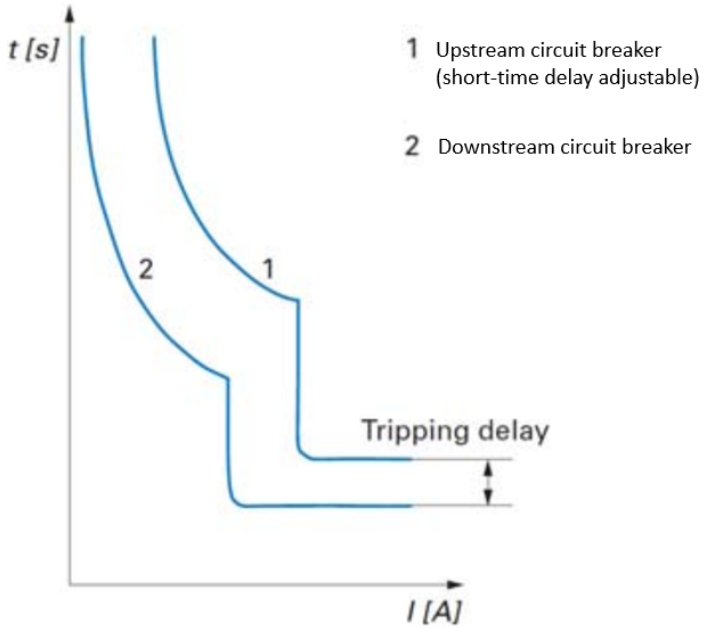

Figure 18: *Tripping curves of upstream and downstream protective devices. Total selectivity may be possible, however, it can be verified only by testing (adapted from* (33)*).*

Partial selectivity is a situation where the selectivity is ensured up to the value of selectivity limit current I_s. The selectivity limit current I_s is the current value of the intersection between tripping curves of upstream and downstream protective devices as shown in Figures 19a and 19b. In circuits, where the prospective short-circuit current or fault current does not exceed the value of I_s, partial selectivity may be an adequate solution and there is no essential purpose to implement the overcurrent protection according to total selectivity requirements. (33)

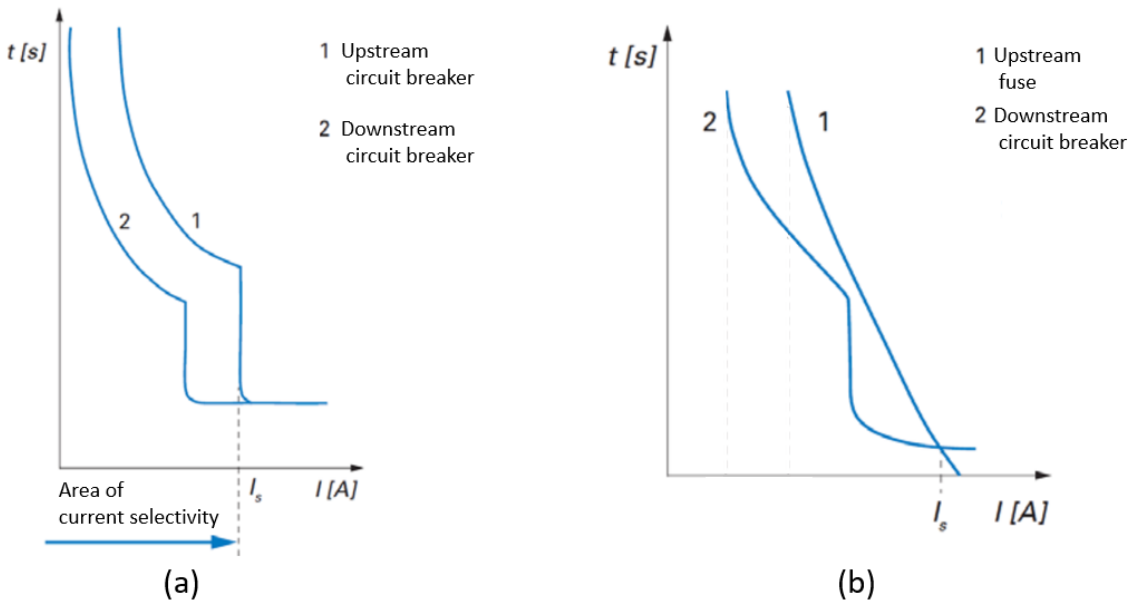

Figure 19: *Tripping curves of a downstream circuit breaker and an upstream circuit breaker (a) or a downstream circuit breaker and an upstream fuse (b) when overcurrent protection selectivity is partial (adapted from* (33)*).*

It has to be noted that short-time delays of miniature circuit breakers, discussed in Chapter 4.3.2, are not adjustable and their tripping curves in thermal tripping zones are very similar as can be seen from Figure 16. Therefore, using miniature circuit breakers both as upstream and downstream protective devices in the network may not provide selectivity at all. Hence, miniature circuit breakers are often applicable to be used only as downstream overcurrent protection devices. Nowadays, fuses are rarely used as downstream protective devices but instead they are well suitable to be used as upstream protective devices for back-up protection due to their high ultimate breaking capacity I_{cu}. (33). If the UPS supplies power from the batteries in fault situations, when AC grid is not available, the maximum fault current is equal to the current limit of the UPS. Fault current should be high enough to trip the downstream protective device.

4.4 Use of external fault clearing circuitry

The aim of this thesis is to find economical ways to improve the fault clearing capability of a UPS by making changes to an IGBT configuration in the inverter main circuit. However, another solution, which has to be considered for increasing the magnitude of fault current that may be supplied by the UPS in stored-energy mode, is the use of external fault clearing circuitry besides the UPS. The fault clearing circuitry may produce a current pulse in a case of a fault, such as a short circuit, at the load side of the UPS. The object is that the current pulse injected into the faulted output phase by the fault clearing circuitry would be high enough to clear the circuit breaker closest to the fault instantaneously. Thus, the fault clearing capability of the UPS may be improved without making changes

to the IGBT configuration in the inverter main circuit. The required magnitude of fault current to clear the circuit breaker will be produced by the fault clearing circuitry.

In (34) is presented different configurations of fault clearing circuitries which may be employed to improve the fault clearing capability of the UPS when the UPS operates in stored-energy mode. The proposed fault circuitries may be installed at the UPS output so that the fault clearing circuitry is extracted from the main circuit of the inverter. In addition, fault clearing circuitries that may be integrated to the main circuit of the inverter are proposed, however, only a fault clearing circuitry which may be installed externally at the UPS output is presented in this thesis.

A fault clearing circuitry which may be parallel connected to a single output phase of the UPS is presented in Figure 20. The fault clearing circuitry in Figure 20 consists of four diodes, two silicon controlled rectifiers, two inductors, two capacitors, two charging resistors and a control and drive circuit. The fault clearing circuitry may be able to provide a current pulse high enough to clear the respective circuit breaker when a fault occurs during a positive or negative half cycle of pulse width modulated current.

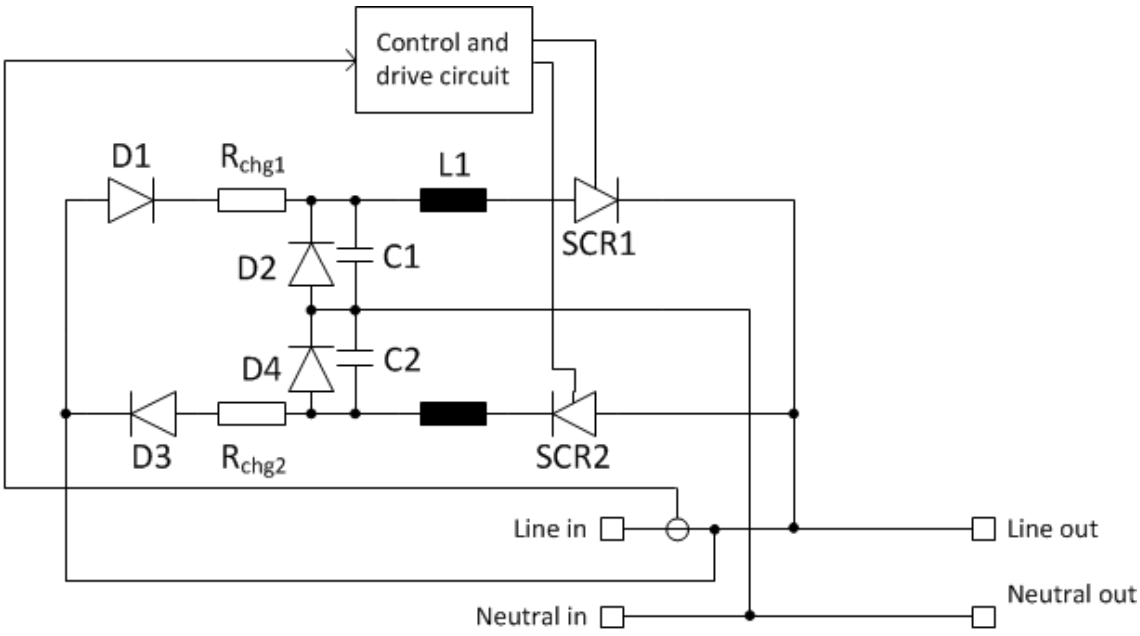

Figure 20: *Circuit diagram of the fault clearing circuitry which may be employed for improving the fault clearing capability of a UPS device.*

Operating principle of the fault clearing circuitry is such that the electrical energy stored in a capacitor C1 or C2 will be discharged into the output line via a silicon controlled rectifier SCR1 or SCR2 when a fault in the output line is indicated. A fault situation is indicated by the control and drive circuit which monitors the magnitude of the current in the output line with a current sensor. If the current magnitude in the output line exceeds a certain current threshold, the control and drive circuit will fire a gate current pulse into the gate of the silicon controlled rectifier SCR1 or SCR2 which results in turning on of the respective silicon controlled rectifier. If a fault, such as a short circuit, occurs in the output line during positive half cycle of the current waveform, the gate current pulse will

be fired to the SCR1. A fault occurring during negative half cycle of the current will cause the gate current pulse to be fired to the SCR2. Thus, the electrical energy stored in the capacitor C1 or C2 will be discharged into the output line as turning on of the silicon controlled rectifier SCR1 or SCR2 will form a closed circuit between poles of the respective capacitor in a short circuit situation. The capacitor C1 may be discharged when the SCR1 is turned on and the capacitor C2 may be discharged when the SCR2 is turned on. An inductor L1 limits the current rise through the SCR1 or and inductor L2 limits current rise through SCR2 if the fault circuitry is triggered. The aim is that the current which arises from discharging of the capacitor C1 or C2 would be high enough for magnetic tripping of the circuit breaker in the output line. Current produced by the fault circuitry is, however, limited in time and magnitude by capacity of the discharging capacitor, inductance of the inductor through which the current flows and impedance of the fault. The capacitor C1 may be charged with positive current through the diode D1 and charging resistor R_{chg1} and capacitor C2 may be charged with negative current through the diode D3 and charging resistor R_{chg2}. Diodes D2 and D4 which are connected in parallel with the capacitors C1 and C2 are applied to protect the respective capacitor from a reverse polarity.

5 SIMULATIONS OF UPS INVERTER OPERATION AT CURRENT LIMIT

Simulation modelling is a method to digitally simulate the operation and behaviour of a real-world physical system or phenomenon. Simulations are based on models and assumptions which may be simplifications of their real-world counterparts. Assumptions may cause difference between simulation results and results achieved in the real world, however, simplifications and assumptions are often essential to use as modelling a real-world system perfectly may be extremely complicated or impossible due to numerous variables affecting each other. Nevertheless, the target is that a simulation model is accurate enough in modelling the investigated real-world system or occasion. A practical method to evaluate the accuracy of the simulation is to compare simulation results to test results achieved by real-world measurements. A major advantage of simulation modelling is that, for example, the behaviour of an investigated system at different situations may be quickly and safely simulated by just reconfiguring simulation parameters. Thus, it may be clearly cheaper, easier and faster than performing same actions with a real-world system. Consequently, simulation models are usually applied as tools to determine whether the investigated system is profitable to be implemented physically in the real-world.

A simulation model, simulating average power losses and average junction temperatures of IGBTs and diodes when a three-level inverter of a UPS device is operating at current limit, is created in this thesis. IGBTs and diodes, which power losses are simulated, are located in the main circuit of the inverter. The simulation model is constructed with Microsoft Excel 2016 which is a spreadsheet application released by Microsoft initially in 2015. Simulations are also run in Microsoft Excel 2016.

The simulation model created in this thesis may be used as a tool when suitability of different IGBTs and diodes in the main circuit of a UPS inverter are evaluated. It is designed to simulate temperatures and power losses of IGBTs and diodes when a fault occurs in the UPS output leading to the UPS to start operating at current limit. The current limit operation is inevitable during a fault situation whether AC grid is not available or if the static bypass switch of the UPS is not managed to be switched on. Due to the current limit operation of a UPS inverter, the assumption for the shape of the current waveform at the UPS output is explicitly fixed in the simulation model created in this thesis. The assumed current waveform complies with the shape of current waveforms presented in Figures 11 and 12. However, the effect of filter and fault inductance may be considered in the simulation model which makes the lines of current waveform curvier than in Figures 11 and 12. Hence, this simulation model may not be suitable in evaluating power losses of IGBTs and diodes when the UPS is operating in other than current limit mode as the shape of the current waveform may in that case differ from the assumed waveform. The shape of the current waveform can not be changed in the simulation model by the user.

Current limit values of the UPS inverter are adjustable in the simulation model. Thus, the simulation model makes it possible for the user to asses how much the maximum current limit value of a UPS could be increased, for example, by using different IGBTs or diodes in the main circuit of the inverter. Furthermore, influence of the switching frequency, DC bus voltage, the dead time and inductance magnitude on total power losses of IGBTs and diodes may be estimated. Moreover, the simulation model allows adding IGBTs and diodes in parallel in the main circuit of the inverter. It makes the use of the simulation model worthwhile, for example, in cases when it is investigated whether it is technically and economically more reasonable to use several lower rated IGBTs or diodes in parallel instead a single higher rated IGBT or diode. However, it should be highlighted, that the simulation model may be used as a tool for technical and economical comparison of IGBTs and diodes only when the fault clearing capability of the UPS is considered. Hence, the simulation model does not provide valid information for comparison of IGBTs and diodes in other situations. All the data of IGBTs and diodes required to run the power loss calculation in the simulation model is usually available in datasheets of IGBTs and diodes offered by IGBT and diode manufacturers.

Section 5.1 introduces how the simulation model is used and Section 5.2 presents in detail how the simulation model is built and designed. In this thesis eight simulation cases were performed where improvement of fault clearing capability of a UPS device was investigated with different configurations of IGBTs and diodes in the main circuit of the inverter. Simulation results of the simulation cases are disclosed in Section 5.3. Additionally, cost comparison and cost analysis of solutions to improve the fault clearing capability of a UPS device is presented in Section 5.3.

5.1 Use of the simulation model

The simulation model is designed to calculate power losses and junction temperatures of IGBTs and diodes in the main circuit of the inverter when the UPS is operating at current limit. Thus, the simulation model requires data about IGBTs, diodes, filter inductor, fault circuit and thermal impedances between the junction and case or between the junction and heatsink to perform power loss and thermal calculations. The fault circuit denotes in this case the closed circuit after the filter inductor when, for example, two phases are short-circuited in the output of a three-phase three-level UPS. In addition, if a heatsink is used, the temperature of the heatsink is assumed to be constant and hence the user is required to give a constant temperature value of the heatsink as input to the simulation model so that thermal calculation of IGBTs or diodes may be performed. Operation characteristics of the inverter during operation at current limit are defined by maximum and minimum current limit values of the inverter which must be inserted to the simulation model. Furthermore, the duration of dead time may be determined in simulations.

User must select which IGBT or diode in the main circuit of the inverter is being studied. This is conducted by selecting the right component symbol “o”, “i”, “Dc” or “Da” from the drag-down menu in the simulation model. Corresponding power semiconductors with the component symbols are presented in Figure 21 which depicts topology of one

output phase of the inverter. Component symbol “o” depicts outer IGBT of the inverter leg, “i” depicts the inner IGBT of the inverter leg, “Dc” depicts a clamp diode and “Da” depicts an anti-parallel diode. Component symbols are represented in Figure 21 for upper branch of the inverter leg. However, they may be applied also with power semiconductors of the lower branch. When similar power semiconductors are used in the upper and lower branch and their switching sequence is similar power losses caused by power semiconductors in the lower branch during negative half-cycle are equal to power losses caused by power semiconductors in the upper branch during positive half-cycle. Due to the drag-down menu, the simulation model offers for the user a possibility to compare quickly how much power losses and junction temperature of an IGBT or diode is changed if location of the component is changed. The performance of IGBTs may be quickly compared whether they are used as outer or inner IGBTs in the inverter main circuit and performance of diodes may be evaluated whether they are used as clamp diodes or anti-parallel diodes. Furthermore, IGBTs or diodes may be added in parallel in the simulation model with a parameter change and thus investigate power losses and junction temperatures of IGBTs or diodes if they are added two or more in parallel into the main circuit of the inverter.

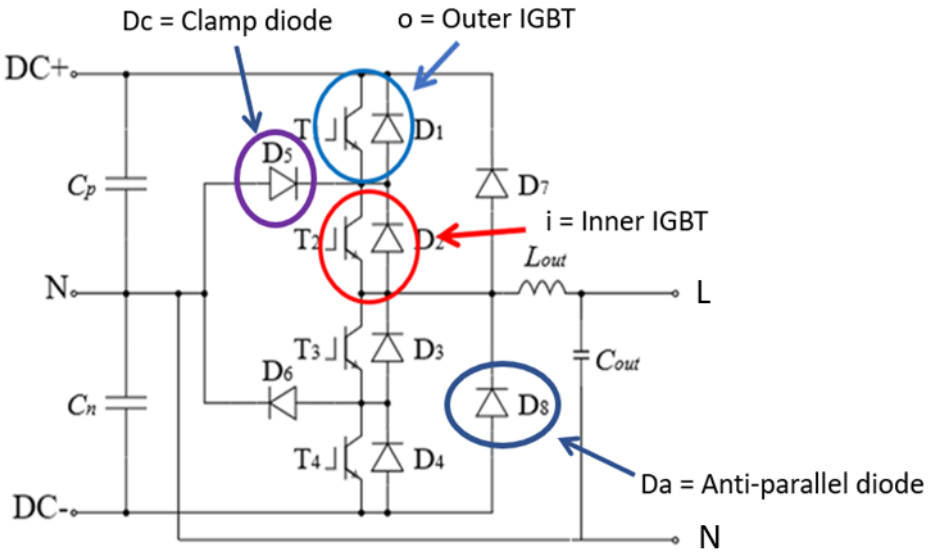

Figure 21: *Component symbols “o”, “i”, “Dc” and “Da” of the simulation model and their counterparts in the main circuit of the inverter.*

For the power loss calculation, the essential information required for the user to enter as input to the simulation model comprises: output voltage and current characteristics of the IGBT or diode, switching losses of the IGBT or reverse recovery energy loss of the diode and inductance of the filter inductor and fault circuit. However, if the average junction temperature of the IGBT or diode is also desired to be calculated, the user must enter the thermal impedance between the junction and case or between the junction and heatsink into the simulation model. If the thermal impedance between the junction and heatsink is

entered into the simulation model, the user must also enter the constant heatsink temperature into the model. Respectively, if only the thermal impedance between junction and case is entered, the case temperature must be assumed constant and fed into the model. Other parameters of the simulation model such as DC bus voltage, grid frequency, number of IGBTs or diodes connected in parallel and current limit and dead time values of the inverter are adjustable by the user. Grid frequency refers to the fundamental frequency of the current at the inverter output. Above mentioned user adjustable parameters allow the user to simulate power losses and junction temperatures of IGBTs or diodes at different situations.

The simulation model gives as output the simulation results which contain: average conduction losses of the IGBT or diode, average switching losses of the IGBT or diode, average total losses of the IGBT or diode, switching frequency of the IGBT and average junction temperature of the IGBT or diode.

In the simulation model, it is assumed that the resistance of the filter inductor and the fault circuit is zero and they can not be changed in the model. Thus, the impedance of the system, which affects to the shape of current waveform according to Equation (25), consists only of inductance of the filter inductor and inductance of the fault circuit. Inductance of the filter inductor and fault circuit are entered as separate parameters into the simulation model. Inductance of the filter inductor may be entered into the simulation model as a function of current in tabular form or as a constant value. However, the inductance of the fault circuit may be entered only as a constant value. The worst case situation relative to the junction temperature of the IGBT or diode is the case when the inductance of the fault circuit is assumed to be zero. This is an imaginary situation as the fault circuit always retains some inductance, for example, from the cables in the real world. However, the fault circuit inductance may still be low in real world short circuit situations. When the inductance of the fault circuit is assumed to be zero, only the inductance of the filter inductor resists the rate of change of the current. It results in increased switching frequency of IGBTs if other parameters which affects to the switching frequency are kept constant. Consequently, the increased switching frequency leads to increased switching losses of IGBTs or diodes and therefore the worst case situation occurs when the inductance of the fault circuit is assumed to be zero.

Output characteristics of the IGBT or diode which are required in the simulation model are usually available from graphs offered in datasheets of IGBTs and diodes. The data of collector current I_c as a function of collector to emitter voltage U_{CE} is required when conduction losses of an IGBT are calculated. Respectively, the data of forward current I_F as a function of forward voltage U_F is required when conduction losses of a diode are calculated. These data are often presented as graphs in IGBT or diode datasheets and can be digitized with a digitizer program into a tabular form. When the data is in tabular form, it can be inserted to the simulation model.

Usually output characteristics of IGBTs and diodes are presented in datasheets separately for conditions where the case or junction temperature is 25ºC and 175ºC.

Sometimes case or junction temperature of 150ºC is used instead of 175ºC. Output characteristic curves of the IGBT or diode may be inserted in tabular form to the simulation model both at higher case temperature, such as 175ºC, and at lower case temperature, such as 25ºC. Then the simulation model can interpolate output characteristics at a desired temperature value between 175ºC and 25ºC. In simulation results of this thesis, output characteristics of IGBTs and diodes are applied at the highest case temperature value which is 175ºC or 150ºC because power losses of IGBTs are greatest on highest case temperature values.

In addition, switching losses of IGBTs are commonly presented as a function of collector current in datasheets of IGBTs. Graphs of switching losses as a function of collector current may be digitized into a tabular form and inserted to the simulation model separately as turn-on and turn-off losses. Switching losses are usually apprised in datasheets of IGBTs at case temperatures of 25ºC and 175ºC or sometimes at a case temperature of 150ºC. In the simulation results of this thesis, switching loss data at the case temperature of 175ºC or 150ºC is used because switching losses increase with increasing case temperature. Thus, the highest switching losses occur at highest case temperature values and worst case scenarios may be simulated when the maximum case temperature value is used. Alternatively, switching losses of IGBTs may also be entered into the simulation model as constant turn-on and turn-off values if switching losses data as a function of collector current is not available.

For diodes, the reverse recovery energy loss is required to be entered as a constant value into the simulation model. Hence, only turn-off losses of diodes are considered in the simulation model when current commutates from a diode to the IGBT. Turn-on losses of diodes are considered to be negligible and therefore they are not entered in the simulation model. However, reverse recovery energy losses of diodes may not be directly announced in datasheets of diodes. Nevertheless, reverse recovery time, reverse recovery charge and peak reverse recovery current are often declared in datasheets. A calculation tool which may calculate the reverse recovery energy loss of a diode based on reverse recovery time, reverse recovery charge or peak reverse recovery current, is integrated with the simulation model. It may be used for quick approximation of the reverse recovery energy loss of the diode if a more accurate value for reverse recovery energy loss is not available. The calculation tool for calculating reverse recovery energy loss of diodes is presented more closely in Section 5.2.3.

After the required input parameters are inserted to the simulation model, different simulation results may be achieved by adjusting DC bus voltage, fundamental output frequency of the UPS inverter, maximum current limit value, minimum current limit value, dead time and number of IGBTs or diodes connected in parallel in the main circuit of the inverter. When the fault clearing capability of the UPS device is investigated, the greatest interest falls upon adjusting the maximum and minimum current limit values. It may be approximated that the average between maximum and minimum current limit values represents the fault clearing capability of the UPS device. In addition, it is worthwhile that the simulation model allows adding IGBTs or diodes in parallel into the main circuit.

Thus, it may be solved, how much the fault clearing capability may be increased when IGBTs or diodes are connected in parallel instead of using single components. Maximum operating junction temperatures and switching frequency of IGBTs define conditions for the maximum fault clearing capability which can be adjusted for the UPS device. Switching frequency of IGBTs is usually limited by the clock frequency of the control circuit of the inverter.

Furthermore, output characteristics of IGBTs may be presented in datasheets at different gate to emitter voltage magnitudes. In simulation results of this thesis, the gate to emitter voltage is assumed to be 15 V for all IGBTs whose power losses and junction temperatures are calculated.

5.2 Design and implementation of the simulation model

The simulation model is implemented with Microsoft Excel 2016 spreadsheet software. Power loss calculation of IGBTs and diodes in the simulation model is based on Equations (1),(2),(3),(4) and (5). The filter and fault circuit inductance affect to the rate of change the current according to Equation (25) and thus to the shape of the fault current waveform. Thermal calculation of IGBTs and diodes in the simulation model is based on Equation (12). In this section is disclosed in detail how the simulation model is implemented and designed to achieve the simulation results.

5.2.1 Principle of conduction loss calculation in the simulation model

Output voltage and current characteristics data of IGBTs and diodes form the basis of the conduction loss calculation. The voltage and current data is digitized from a datasheet and inserted in a table format to the simulation model so that current and voltage values are in separate columns. Thus, discrete points from output characteristics curve of the IGBT or diode are entered as input to the simulation model. Similarly, inductance of the filter inductor as a function of magnetizing current may be digitized and inserted to the simulation model in table format so that inductance and current values are in separate columns. In the simulation model, the magnitude of DC bus voltage, inductance of the filter inductor and inductance of the fault circuit affect to the rate of change of the current according to Equation (25). Thus, they also affect to the conduction losses of IGBTs and diodes as they affect to the shape of the current waveform. However, a more considerable influence on magnitudes of conduction losses results from output characteristics of the IGBT or diode, number of IGBTs or diodes connected in parallel, selected maximum and minimum current limit values and the magnitude of dead time.

In Figure 22 is presented an illustration of the digitizing process when output characteristics curve of an IGBT is digitized by using Engauge Digitizer software. The user shall perform digitizing with an external digitizing software as digitizing feature is not included in the simulation tool. Collector current I_c and collector-to-emitter voltage U_{CE}

values are inserted to the simulation model at target points which are depicted in Figure 22 as blue crosses. The simulation model will then interpolate linearly current values between target points at 0,003 V intervals. It means that current values are calculated at 0,003 V intervals on a straight line which is drawn between target points. Thus, as for accuracy of the digitizing, it does not matter how many target points are employed in digitizing. However, it is important that the straight line drawn between target points lies on the output characteristics curve that is being digitized. Thereafter the simulation model stores interpolated current values and their respective voltage values to a database in the simulation model. Next the simulation model multiplies respective current and voltage values together. It results to a new table which indicates discrete power loss values which the IGBT or diode may have.

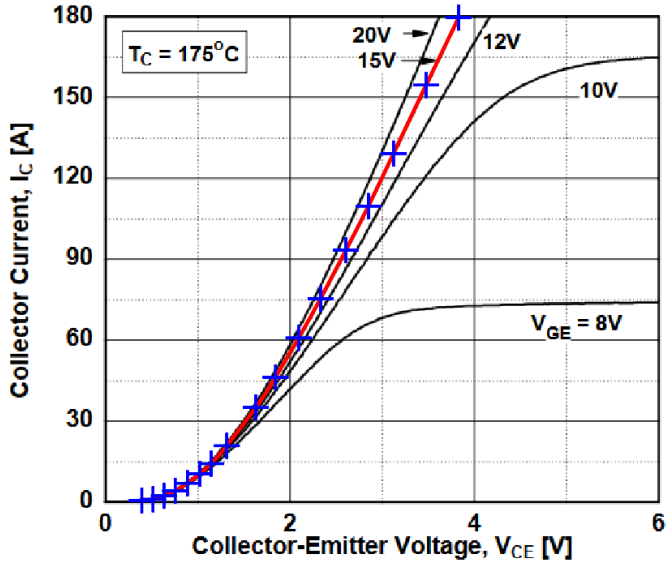

Figure 22: *Output characteristics curve of an IGBT digitized when 15V gate-to-emitter voltage is used and the case temperature is 175°C.*

Similarly, the user may digitize the inductance curve of the filter inductor as a function of current and insert it to the simulation model if such curve is provided by the filter manufacturer. Then the simulation model interpolates inductance values of the filter inductor at equivalent current points where discrete power loss values of the IGBT were calculated previously. Thereafter the simulation model calculates the rate of change of the current at those current points by using Equation (25) as inductance values of different current points are known. Consequently, time instances, when discrete power loss values of IGBTs or diodes occur, may be calculated. At last the energy loss between two adjacent discrete power loss instances are calculated in the simulation model by exploiting trapezoidal rule which is a numerical integration method.

The principle of the trapezoidal rule is presented in Figure 23. Figure 23 is purely illustrative and does not relate to simulation results achieved with this simulation model in this thesis. The absolute power loss is depicted with red curve. The discrete power loss values at time instances t_i are known and they are depicted as vertical black lines in Figure 23. The energy loss can be calculated by integrating power loss over time. Thus, the

energy loss between adjacent time instances t_i and t_{i+1} may be approximated by calculating the area of the trapezoid, where time values t_i and t_{i+1} form the base of the trapezoid and power loss values $p(t_i)$ and $p(t_{i+1})$ the height of the trapezoid. When areas of single trapezoids are chained and summed together, the energy loss over the desired power loss curve may be approximated. The approximation is the more accurate, the shorter is the difference between time instances t_i and t_{i+1} which leads to higher number of individual trapezoids summed together.

In the simulation model the time difference between t_i and t_{i+1}, or width of single trapezoid, is defined at intervals, when voltage U_{CE} changes 0,003V as a result of increase or decrease in current I_c. When the IGBT or diode is conducting, areas of trapezoids are calculated and summed together over positive half cycle. As a result, the total conduction energy loss over one cycle is achieved because the IGBT or diode conducts only during the other half cycle. Thus, it is enough to calculate conduction losses for the other half cycle only. Finally, the average conduction power loss over one cycle is achieved by dividing the total conduction energy loss over one cycle with a duration of the cycle. Conduction periods during positive half cycle differ between IGBTs and diodes and applying conduction loss calculation for IGBTs and diodes based on their conduction periods is discussed in Chapter 5.2.2.

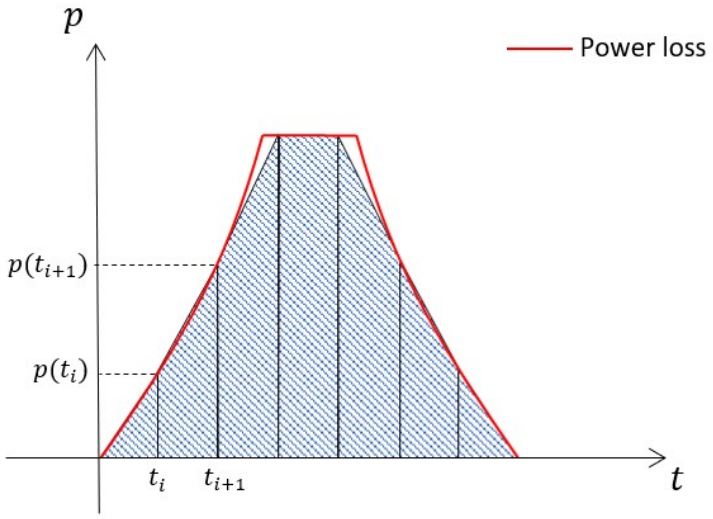

Figure 23: *Principle of trapezoidal method which is used in the simulation model when power loss curve is integrated numerically.*

5.2.2 Application of conduction loss calculation technique to IGBTs and diodes

The simulation model calculates total energy losses of IGBTs and diodes over a half-cycle according to their conduction sequences and conduction times which are presented in Figure 14. The simulation model is built such that, based on user input values, it will always calculate energy losses for all four IGBTs and diodes which are depicted in the

simulation model as symbols “o”, “i”, “Dc” or “Da”. Thus, power loss and junction temperatures are calculated in the simulation model for all components whose location is presented in Figure 21 regardless of which symbol the user has chosen from the drag-down menu. However, simulation results are showed only for the IGBT or diode which symbol the user has chosen from the drag-down menu in the simulation model. Maximum and minimum current limit values i_{max} and $i_{min,}$ as well as the magnitude of dead time t_{dead}, are user adjustable parameters in the simulation model. They define limits for the energy loss calculation.

The IGBT T_2 in Figure 14 is depicted as inner IGBT and the IGBT T_1 is depicted as outer IGBT in the simulation model. Inner and outer IGBTs conduct always when current increases towards maximum current limit value as can be seen from Figure 14. Furthermore, they conduct in the beginning of half cycle when current rises from zero to the value of i_{max} which must be considered in the conduction loss calculation.

When the current rises from i_{min} to i_{max}, conduction losses for inner and outer IGBTs are computed in the simulation model by calculating first the conduction loss when current rises from zero to the value of i_{max}. Next the simulation model counts the conduction loss when current rises from zero to the value of i_{min}. Then the two calculated conduction loss values are subtracted from each other which results in conduction loss value when current rises from i_{min} to i_{max}. The conduction loss during current decrease from i_{max} to i_{min} is calculated in the same principle and thus conduction losses for anti-parallel diode, or diode D8 in Figure 14, may be solved. Respectively, conduction losses of the anti-parallel diode are calculated in the end of half-cycle when current decreases from i_{max} to zero.

In the simulation model it is assumed that the power is constant when clamp diodes are conducting current according to Figure 14, because current through a clamp diode remains constant during its conduction periods. Hence, conduction energy losses of clamp diodes are calculated by multiplying the dead time with constant power values when current is at its maximum and minimum limit. Furthermore, as inner IGBTs are conducting also when clamp diodes are conducting, the power loss of inner IGBTs during dead time periods must be calculated and added to the power losses which occur in them during the increase of current from i_{min} to i_{max}.

The switching frequency of the inverter is calculated in the simulation model based on rise time, fall time and dead time periods of the current waveform. In Figure 14 is shown the principle how rise time t_{rise}, fall time t_{fall} and dead time t_{dead} periods are determined in the simulation model. The switching frequency of the inverter is derived as

$$f_{sw} = \frac{1}{T_{sw}} = \frac{1}{t_{fall} + t_{rise} + 2 * t_{dead}}\ , \tag{27}$$

where T_{sw} is cycle time of switching sequence waveform. The current waveform which arises from IGBT switchings between i_{max} and i_{min} and includes dead time periods is called as switching sequence waveform in this thesis.

Total conduction energy loss of IGBTs and diodes during positive half-cycle is obtained by calculating the number of single conduction times of IGBTs and diodes during positive half cycle and multiplying that with conduction losses of IGBTs and diodes during respective single conduction periods. Losses during single conduction periods of IGBTs and diodes are calculated with trapezoidal method explained in Section 5.2.1.

Calculation of single conduction times of IGBTs and diodes during positive half-cycle is based on dividing the cycle time T_{half} of positive half-cycle with the cycle time T_{sw} of switching sequence waveform. However, both the time $t_{0\text{-}imax}$ required for the current to increase from zero to i_{max} in the beginning of half-cycle and the time $t_{imax\text{-}0}$ required for the current to decrease from i_{max} to zero in the end of half-cycle must be subtracted from T_{half} before executing the division. Periods $t_{0\text{-}imax}$ and $t_{imax\text{-}0}$ are equal as inductance affecting to the rate of change of the current is equal during increase and decrease of current. Thus, the number of cycles N_{sw} of switching sequence waveform during positive half-cycle is solved in the simulation model according to equation

$$N_{sw} = \frac{T_{half} - t_{0-imax} - t_{imax-0}}{T_{sw}}. \tag{28}$$

In Figure 24 is illustrated the determination of T_{half}, T_{sw}, $t_{0\text{-}imax}$ and $t_{imax\text{-}0}$ on current waveform during positive half-cycle when a UPS inverter operates at current limit. Figure 24 is only explanatory and thus relation between lengths of T_{half}, T_{sw}, $t_{0\text{-}imax}$ and $t_{imax\text{-}0}$ periods may differ from reality. Lines of the current waveform are curvy as the inductance of the filter inductor varies as a function of current and thus the current rate of change is not constant.

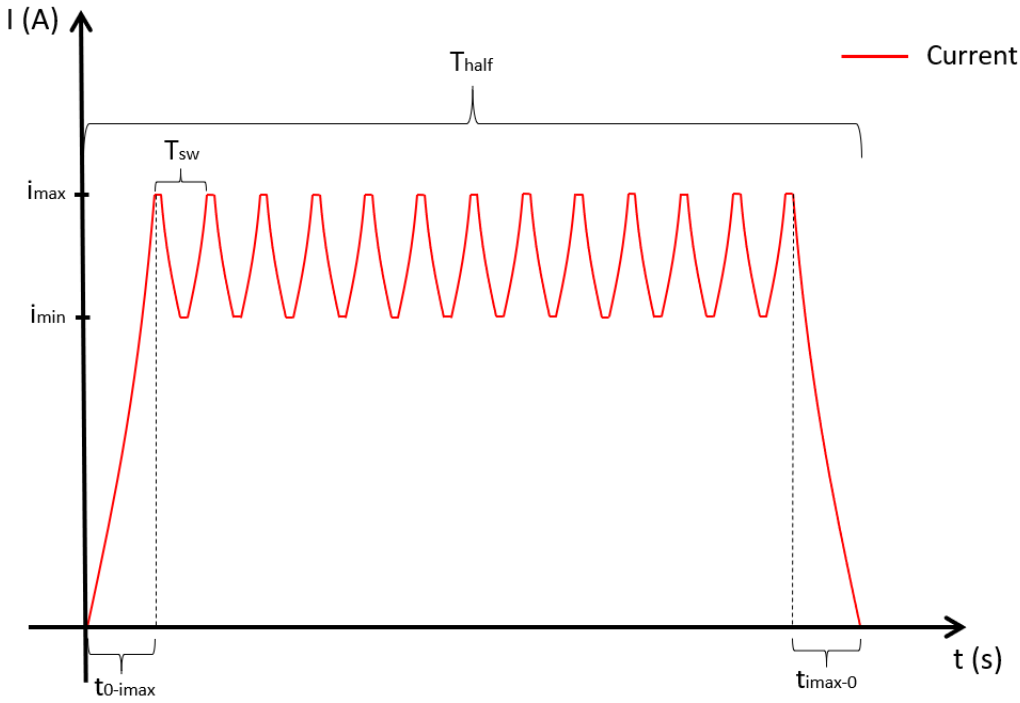

Figure 24: *Current waveform during operation of a UPS inverter at current limit with time periods which are used to determine number of cycles of switching sequence waveform during positive half-cycle.*

Conduction losses of the IGBT or diode over half-cycle T_{half} is derived by multiplying conduction losses during one cycle T_{sw} of switching sequence waveform with number of cycles N_{sw} of switching sequence waveform during positive half-cycle. Furthermore, when conduction losses of inner and outer IGBTs are calculated, conduction losses occurring in them during time period $t_{0\text{-}imax}$ must be considered. Respectively, conduction losses of the anti-parallel diode during $t_{imax\text{-}0}$ must be considered when its conduction losses during half cycle T_{half} is being calculated. The proportion between magnitudes of T_{half}, $t_{0\text{-}imax}$ and $t_{imax\text{-}0}$ have a minor effect on average conduction power loss of IGBTs and diodes as it affects to the value of N_{sw}. Thus, increasing the fundamental frequency of the output current of the inverter, which is referred to as grid frequency in the simulation model, will slightly decrease average conduction losses as the magnitude of $t_{0\text{-}imax}$ and $t_{imax\text{-}0}$ will increase in proportion to the magnitude of T_{half}.

5.2.3 Switching losses calculation and a tool for calculating reverse recovery energy loss of diodes

Inner and outer IGBTs both switches once on and once off during one cycle T_{sw} of the switching sequence waveform which can be seen from conduction periods of IGBTs T_1 and T_2 presented in Figure 14 where $T_{sw} = t_{rise}+t_{fall}+2*t_{dead}$. Reverse recovery energy loss occurs one time for both clamp diode D_1 and anti-parallel diode D_8 when current commutates from the diode to the IGBT.

Switching losses graph of IGBTs may be digitized and inserted to the simulation model in table format as a function of current. Then the simulation will automatically

search for correct switching loss values from the data table according to inserted maximum and minimum current limit values. Both inner and outer IGBTs switch on at minimum current limit value and off at maximum current limit value. The simulation model exploits interpolation for retrieving the exact switching on and off loss value from the data table according to current limit values. Hence, if current limit values are changed, the simulation model will automatically change also the switching loss values to match with new current limit values.

Additionally, the switching voltage for the switching losses graph is presented in datasheets of IGBTs as switching losses of IGBTs are dependent on magnitude of switching voltage. Thus, the user must enter as input the switching voltage which is valid for the inserted switching loss data. The simulation model will then form a scaling factor for the switching losses according to the inserted DC bus voltage parameter value as it is equal to the switching voltage magnitude used in the simulation. The scaling factor is formed by dividing the DC bus voltage used in the simulation with the valid switching voltage of the inserted switching loss data. Values of inserted switching loss data are then multiplied with the scaling factor so that switching loss values match with the switching voltage used in the simulations.

However, if a graph of switching losses of the IGBT is not available, switching loss values may be inserted manually to the simulation model. In that case the simulation model will resemble the user with a pop-up window to change also switching loss values when current limit values are changed as switching losses of IGBTs may be current sensitive variables. The pop-up window may prevent invalid simulation results from occurring due to a user mistake.

Switching losses during one cycle T_{sw} of switching sequence waveform are calculated by multiplying the number of switchings during T_{sw} with switching losses of respective single switchings. Total switching losses of IGBTs during half-cycle T_{half} are calculated by multiplying switching losses during one cycle of switching sequence waveform T_{sw} with number of cycles N_{sw} of switching sequence waveform during half-cycle. Similarly as in conduction loss calculations, increasing the grid frequency will slightly reduce the average switching power loss of IGBTs and diodes as the value of N_{sw} is diminished.

Reverse recovery energy losses of diodes are considered as switching off losses of diodes in the simulation model and they shall be inserted manually to the simulation model. However, as reverse recovery energy losses of diodes are rarely apprised directly in datasheets of diodes, a tool for approximating reverse recovery loss of a diode is integrated to the simulation model.

The tool calculates the reverse recovery energy loss a diode according to Equation (6). The tool requires the rate of change of the current $\frac{di}{dt}$, which shown in Figure 8, always as input for the calculation. Then the user must insert peak reverse recovery current I_{prr} and reverse recovery charge Q_{rr} or peak reverse recovery current I_{prr} and reverse recovery time t_{rr} or reverse recovery charge Q_{rr} and reverse recovery time t_{rr} to the calculation tool. With one of those three combinations, the tool calculates the area of Q_f in

Figure 8 which is required in calculation of reverse recovery current according to Equation (6). In addition, the magnitude of reverse voltage U_R which is equal to DC bus voltage of the inverter must be inserted to the calculation tool. The calculation tool gives as output an approximation of reverse recovery energy loss of a diode which is multiplied with a safety factor 1,2. The safety factor is used to prevent the tool from outputting too ideal reverse recovery energy losses if values I_{prr}, t_{rr} or Q_{rr} apprised in diode datasheets would be misjudged by the diode manufacturer. Furthermore, the tool draws an illustrative graph of the reverse recovery current as a function of time. The validity of reverse recovery energy losses may be evaluated from the graph. Similarly to IGBTs, total switching losses of diodes during half-cycle T_{half} are calculated by calculating first reverse recovery energy losses of diodes during T_{sw} and multiplying that with the number of cycles N_{sw} of switching sequence waveform during half-cycle.

5.2.4 Parallel connection and thermal calculation of IGBTs and diodes

A key factor, which makes the simulation model useful in investigating the fault clearing capability of UPS inverter, is that the number of IGBTs and diodes connected in parallel in the main circuit of the inverter may be changed easily with a parameter change. Thus, it may be investigated how much current limit values, or fault clearing capability of the inverter, can be raised when diodes or IGBTs are added in parallel. The user may choose an unlimited number of IGBTs or diodes connected in parallel in the main circuit of the inverter and the simulation model will calculate power losses and junction temperatures of single IGBTs and diodes. However, it is assumed that the parallel connected IGBTs or diodes are similar and that current is divided equally between them.

Power loss calculation of single parallel connected IGBTs or diodes is implemented in the simulation model by calculating the maximum and minimum current limit values and rate of change of the current that flows through single IGBTs or diodes. Maximum and minimum current limit values of the current flowing through single parallel connected IGBTs or diodes are calculated by dividing the maximum and minimum current limit values of the inverter with the number of IGBTs or diodes connected in parallel. Thus, for example, if the used maximum current limit value of the inverter is 120 A and minimum current limit is 90 A and three IGBTs are connected in parallel, the maximum current limit of the current flowing through a single IGBT is 40 A and minimum current limit 30 A. Thus, switching of IGBTs occur at current magnitudes of 40 A and 30 A. The rate of change of the current must be also calculated separately for the single parallel connected IGBT or diode as the number of parallel connected IGBTs or diodes must not affect to the switching frequency of the IGBTs. Thus, the inductance data of the filter inductor and fault circuit is multiplied with the number of IGBTs or diodes connected in parallel. As a result, the rate of change of the current that flows through a single parallel connected IGBT or diode is divided by the number of parallel connected IGBTs or diodes. Hence, the resultant current waveform which arises from current waveforms of single parallel connected IGBTs or diodes is the output current of the inverter.

Calculation of the average junction temperature of IGBT or diode is based on Equation (12). Average conduction and switching power loss of the IGBT or diode during one cycle of the inverter output current waveform are summed together which results in average total power loss P_L of the IGBT or diode. User must insert a constant heatsink temperature T_H to the simulation model if heatsink is used or a constant case temperature T_C of the IGBT or diode if heatsink is not used. Furthermore, a constant value for the thermal impedance between the junction and case of the IGBT or diode, which is apprised in IGBT or diode datasheet, must be entered as input to the simulation model. Usually, the thermal impedance of the thermal interface material between case and heatsink is apprised in relative to the contact area of TIM. Thus, the user may insert the contact area of the TIM and the thermal impedance of the TIM relative to the contact area to the simulation model. Then the simulation model may calculate a constant thermal impedance value between case and heatsink. Consequently, the average junction temperature of IGBT or diode may be calculated.

It must be noticed that as the junction temperature calculation is based on average total power loss of IGBT or diode over one cycle, the average junction temperature outputted from the simulation model does not describe the maximum junction temperature that may occur momentarily. The higher the current deviation through the IGBT or diode is, the more the maximum junction temperature may differ from the average junction temperature calculated with the simulation model. Thus, a certain gap shall be left between the maximum allowed operating junction temperature of the IGBT or diode and average junction temperature of the IGBT or diode achieved from simulation results.

5.2.5 Summary of simulation parameters dependency on each other

In Figure 25 is presented an explanatory chart about the calculation algorithm on how the simulation model is implemented. Figure 25 summarizes parameters which the user must enter as input to the simulation model and the relevant parameters to be adjusted when the fault clearing capability of a UPS inverter is investigated. Arrows declare dependencies between parameter values and simulation result values. Changing the parameter value from where an arrow begins will have an influence on value of the simulation result which the arrow points at. In previous sections 5.2.1, 5.2.2, 5.2.3 and 5.2.4 is explicated that why and how input parameter values influence on respective simulation results.

Dotted lines indicate that changing the parameter value from where the dotted line starts has only minor relative influence on a value of the pointed simulation result. Thus, their significance on the pointed simulation result value is minor. Parameters from where a continuous line is drawn to point at the simulation result has a more significant effect on the simulation result value. Colours of the arrows indicate which simulation result parameter is being affected when respective input parameter is changed. From Figure 25 can be seen that changing any of the input parameters or user adjustable parameters will have at least some influence on average junction temperature of the IGBT or diode.

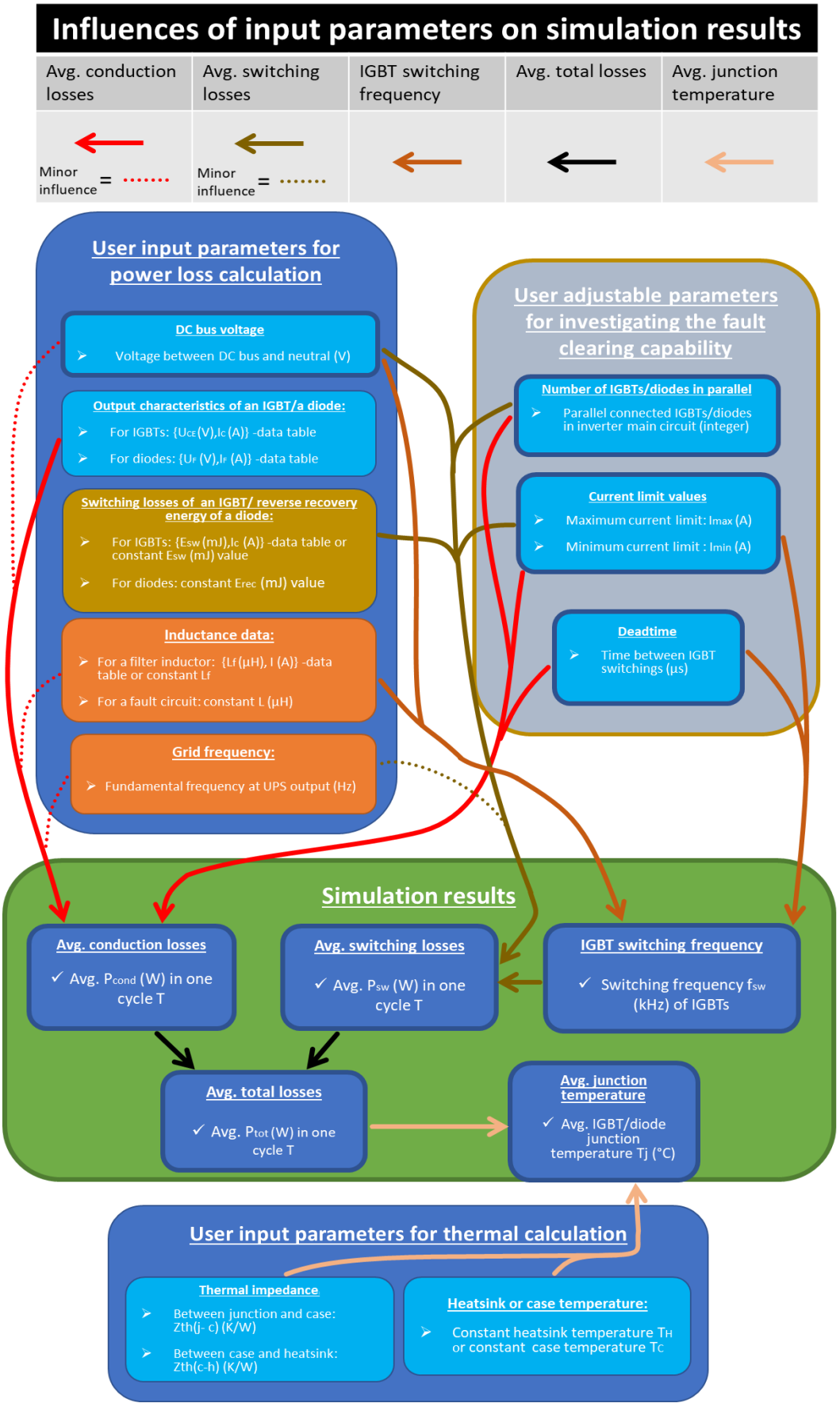

Figure 25: *Calculation algorithm of the simulation model and parameter dependencies on each other.*

5.3 Simulations with different IGBT and diode configurations

A target in simulations of this thesis is to investigate how much the fault clearing capability of a UPS device could be increased if several IGBTs or diodes are connected in parallel in the main circuit of a UPS inverter. The IGBTs and diodes, which are under examination are used originally as single components in main circuits of 15 kW and 20 kW UPS inverters. The greatest interest of completing simulations is to solve what kind of parallel configuration of IGBTs and diodes may be required so that the UPS inverter is able produce an output fault current that may clear a C16 miniature circuit breaker instantly.

At present, when single IGBTs and diodes are used in the main circuit of 20 kW UPS inverter, the inverter is able to provide enough fault current to clear a C6 miniature circuit breaker instantly if a fault occurs at UPS output. However, inventors of the fault clearing circuitry, which is presented in Chapter 4.4, have tested that the fault clearing circuitry may provide enough fault current to clear a C16 miniature circuit breaker instantly whether a short circuit happens in the load side of the UPS. Thus, the aim is to figure out the parallel configuration of IGBTs and diodes in the main circuit of inverter that may clear the C16 miniature circuit breaker instantly without exceeding safe operating areas of IGBTs and diodes. Eventually, when the targeted parallel configuration of IGBTs and diodes is found out, a cost comparison between the cost of the fault circuitry and the cost of components required to be added in parallel to the main circuit of the inverter is executed. Hence, it may be estimated, whether it is economically more reasonable to improve the fault clearing capability of a UPS device by adding power semiconductors in parallel to the main circuit of the inverter or by installing the external fault clearing circuitry beside a UPS device. Simulations performed in this thesis consist of several cases, where IGBT and diode configurations and current limit settings of the inverter are varied. Current limit values are adjusted to achieve the highest fault clearing capability of the UPS inverter which fulfils preconditions.

Components and preconditions applied in the simulations are presented in Section 5.3.1, simulation results are presented in Section 5.3.2 and cost comparisons between possible solutions to improve the fault clearing capability of a UPS device to clear C16 circuit breakers are presented in Section 5.3.3.

5.3.1 Components and preconditions of simulations

In simulations of this thesis it is assumed that the inductance of the filter inductor is the only parameter limiting the rate of change of the current. The inductance curve of the filter inductor, which is used in all simulation cases of this thesis, is presented in Figure 26 as a function of DC magnetizing current. The inductance curve is digitized and entered as input to the simulation model. Thus, the current rate of change is equal in all simulation cases as the applied positive and negative DC bus voltage is also a constant 350 V in all simulation cases.

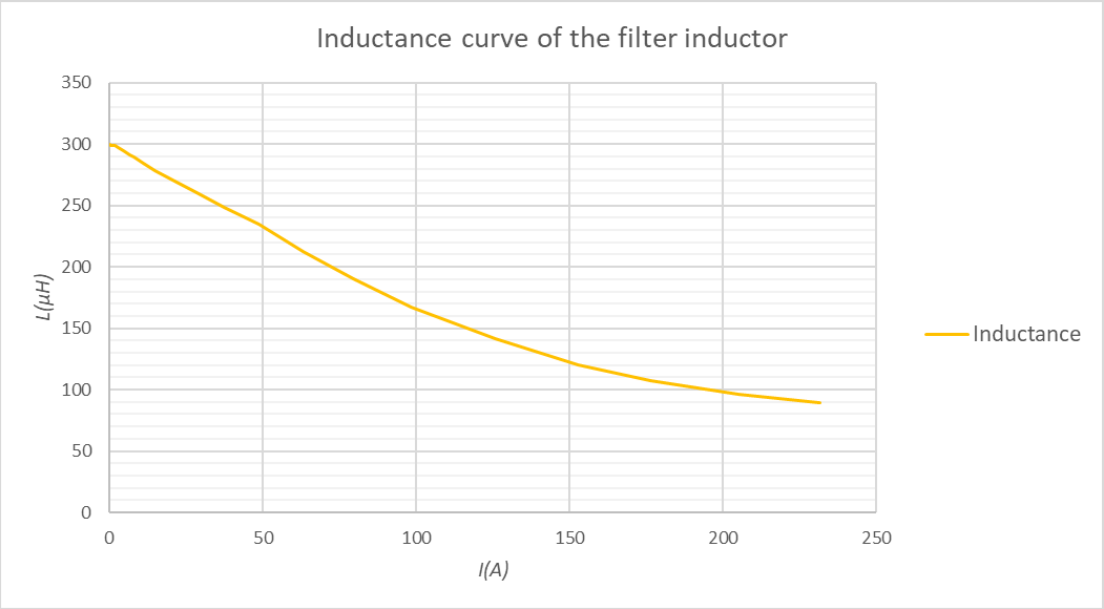

Figure 26: *Inductance curve of the filter inductor as a function of DC magnetizing current.*

IGBTs and diodes, which performances are investigated in this thesis during current limit operation of a UPS device, are presented in Table 3. IGBTs and diodes presented in Table 3 are used currently as single components in existing 20 kW and 15 kW UPS inverters. The investigated IGBTs and diodes are identified only according to their rated currents and voltages. Their locations in the main circuit of the inverter can be checked from Figure 21 and they conduct during positive half-cycles of current. Similar components are used in lower branch of the inverter at respective places and they conduct during negative half-cycles of current. Thus, losses of components in upper and lower branches of the inverter main circuit are assumed to be equal. Therefore, losses and junction temperatures of components in other branch only are required to be calculated for solving losses and junction temperatures of all components in the main circuit of the inverter.

Table 3: *IGBTs and diodes whose performance is evaluated in simulations of this thesis. IGBTs and diodes are identified according to their rated currents and voltages.*

	20 kW UPS inverter component	**15 kW UPS inverter component**
Outer IGBT	IGBT 600V 60A	IGBT 650V 40A
Inner IGBT	IGBT 650V 75A	IGBT 650V 50A
Clamp diode	Diode 600V 75A	Diode 600V 60A
Anti-parallel diode	Diode 1200V 60A	No component

Two preconditions, which must be fulfilled in all simulation cases of this thesis, are that the switching frequency of IGBTs must be below 18 kHz and junction temperatures of IGBTs and diodes must be kept below 150°C. Therefore, maximum and minimum current limit values are adjusted in the simulation model so that above mentioned preconditions

are fulfilled. The reason of using preconditions is to ensure that operation of IGBTs and diodes is kept within their safe operating areas. However, the average between maximum and minimum current limit values should be maximized to achieve the highest possible fault clearing capability for the UPS inverter. Obviously, it must be considered, that the maximum current limit value does not exceed maximum current ratings apprised in datasheets of IGBTs and diodes or current ranges of graphs presented in IGBT and diode datasheets. Otherwise, a high risk for destruction of IGBTs or diodes may exist.

It should be noted that the maximum fault current flowing through the miniature circuit breaker in the load side is not equal to the maximum current limit value of the inverter, or the maximum current flowing through IGBTs and diodes, as the filter capacitor shunts high frequency current components and thus cuts peaks in fault current waveform at the load side. Therefore, an average of maximum and minimum current limit values is a good approximation of current magnitude flowing through the miniature circuit breaker.

Besides inductance and DC voltage values, other settings of the simulation model which are applied as equal in all simulation cases of this thesis are heatsink settings, the magnitude of dead time and the used grid frequency which is the fundamental frequency of the output fault current waveform. The magnitude of dead time used in simulations is 1,1 µs and the grid frequency is 50 Hz. The used constant temperature of the heatsink is below 100°C and the thermal impedance between case and heatsink is 0,399 °C/W. The thermal impedance value between the case and heatsink is assumed to be same in all components. Thus, the used thermal interface material and contact area between the case and heatsink are equal in all IGBTs and diodes presented in Table 3 as they are encapsulated into same packages. Furthermore, the output characteristics data of IGBTs and diodes and switching losses data are taken from datasheets according to 175°C junction temperature value and according to 15 V gate-to-emitter voltage value. Reverse recovery energy losses, which are switching losses of diodes, are calculated with the calculation tool which is integrated to the simulation model. Thermal resistance values used in the simulations between junction and case correspond with steady-state condition values apprised in IGBT and diode datasheets.

In first simulation cases of this thesis, power losses and junction temperatures of IGBTs and diodes are calculated according to known semiconductor configurations and current limit adjustments of existing 15 kW and 20 kW UPS devices. Thus, the validity of simulation results and input parameters may be verified when junction temperatures of IGBTs and diodes which the simulation model gives as output may be compared to general estimations of real IGBT and diode junction temperatures which are valid in respective UPS devices. In addition, it may be verified that above mentioned preconditions are fulfilled when same current limit values are used in the simulation model as are used in their real world counterparts.

5.3.2 Simulation results

In this thesis, eight different simulation cases were performed in total where the fault clearing capability of the UPS inverter was investigated with different configurations of IGBTs and diodes in the main circuit of the inverter. The investigated configurations of the eight simulation cases are listed in Table 4. Cases 1 and 2 represent configurations which are currently used in 20 kW and 15 kW UPS inverters. In cases 3–5 components are added in parallel and it is investigated how much the output current of the UPS may be increased as a result of parallel connections. In cases 6–8 switching frequency of the inverter was decreased from around 18 kHz and its influence on power losses and junction temperatures of IGBTs and diodes was investigated.

Table 4: *Investigated simulation cases and their configurations.*

	IGBTs of 20 kW UPS inverter		IGBTs of 15 kW UPS inverter		Diodes of 20 kW UPS inverter		Diode of 15 kW UPS inverter
	IGBT 600V 60A	**IGBT 650V 75A**	**IGBT 650V 40A**	**IGBT 650V 50A**	**Diode 600V 75A**	**Diode 1200V 60A**	**Diode 600V 60A**
Case 1	Outer: single	Inner: single	-	-	Clamp: single	Anti-parallel: single	-
Case 2	-	-	Outer: single	Inner: single	-	-	Clamp: single
Case 3	Outer: two in parallel	Inner: two in parallel	-	-	Clamp: two in parallel	Anti-parallel: two in parallel	-
Case 4	-	-	Outer: two in parallel	Inner: two in parallel	Clamp: single	Anti-parallel: single	-
Case 5	-	-	Outer: three in parallel	Inner: three in parallel	Clamp: two in parallel	Anti-parallel: two in parallel	-
Case 6 (lower switching frequency)	Outer: single	Inner: single	-	-	Clamp: single	Anti-parallel: single	-
Case 7 (lower switching frequency)	Outer: two in parallel	Inner: two in parallel	-	-	Clamp: two in parallel	Anti-parallel: two in parallel	-
Case 8 (lower switching frequency)	-	-	Outer: two in parallel	Inner: two in parallel	Clamp: single	Anti-parallel: two in parallel	-

In the first simulation case, which results are disclosed in Table 5, the simulation was performed according to current limit values of the inverter and configurations of IGBTs and diodes which are valid in the existing 20 kW UPS device. The simulation results in Table 5 confirm that the simulation model gives reasonable results with current limit adjustments and configurations of power semiconductor devices which are used in the existing UPS device.

Table 5: *Results of the first simulation case where IGBTs, diodes and their configuration are chosen as they are used in the 20 kW UPS device currently.*

INVERTER CURRENT LIMIT ADJUSTMENTS					
Max. Current limit:	110 A	**Avg. current:**	84.5 A	**Fault clearing capability:**	C6 miniature circuit breaker
Min. Current limit:	59 A				
Switching frequency:	17,799 kHz				

PERFORMANCE OF POWER SEMICONDUCTOR DEVICES						
Location	**Component**	**Configuration**	**Avg. Conduction losses**	**Avg. switching losses**	**Avg. total losses**	**Avg. junction temperature**
Outer IGBT	IGBT 600V 60A	Single	49,24 W	32,13 W	81,37 W	< 150 ℃
Inner IGBT	IGBT 650V 75A	Single	35,03 W	44,19 W	79,22 W	< 150 ℃
Clamp diode	Diode 600V 75A	Single	2,29 W	3,42 W	5,71 W	< 150 ℃
Anti-parallel diode	Diode 1200V 60A	Single	35,67 W	18,42 W	54,09 W	< 150 ℃

The switching frequency is below 18 kHz and thus it fulfils the precondition. In addition, it is known that total power losses of IGBTs should be around 80 W which results in average IGBT junction temperature that is below 150 ºC. The fault clearing capability of the UPS device is estimated in the simulation results according to average current value which is calculated as an average between the maximum and the minimum current limit values. Thus, it equals approximately the peak magnitude of the output current because the filter capacitor shunts high frequency current components at the UPS output. Hence, the current waveform fed through the circuit breaker resembles the shape of a square waveform. Magnitude of the average current during negative and positive half-cycles of the fault current is the same and only the direction of the current is opposite.

The fault clearing capability is announced for C-type miniature circuit breakers in this thesis. The rated current value of the circuit breaker is chosen such that the average output current of the UPS is high enough to clear the circuit breaker instantly. The output current of the UPS shall be clearly in the magnetic tripping zone of the circuit breaker to ensure instant tripping. Therefore, one size smaller circuit breaker in terms of magnitude of the rated current is preferred if output current of the inverter is closer to lower current threshold of the magnetic tripping zone than the higher current threshold. Magnetic tripping zones of different circuit breaker types are shown in time-current characteristic curves in Figure 16 and it shall be remembered that current thresholds of miniature circuit breakers should be multiplied with a factor $\sqrt{2}$ when square wave shaped current is fed through them as described in Chapter 4.3.2.

According to the simulation results of Table 5, the UPS device may produce an output fault current of 84,5 A. However, in the specification of 20 kW UPS device is announced that the 20 kW UPS device may produce an output current of 72A in a short circuit situation. The value announced in the device specification is based on results achieved from short circuit tests which are performed with the existing device. Hence, it shall be considered that the simulation model may give ideal results compared to real world situations since in the simulation model is assumed, for instance, that the fault resistance is zero and that the inductance is comprised only from the filter inductance. Furthermore, it is assumed that the filter capacitor filters high frequency current components from the UPS output current so that the average between maximum and minimum current limit values is the peak current which is fed to the circuit breaker. This coarse assumption may also add error to simulation results and thus the simulation model may give higher output currents than occurs in the real world. Nevertheless, the fault clearing capability of C6 miniature circuit breaker which is achieved from simulation results is equal with the fault clearing capability announced in the 20 kW UPS device specification.

In the second simulation case, which results are presented in Table 6, the simulation parameters were adjusted according to IGBTs, diodes and current limit values which are used in the existing 15 kW UPS device. Diodes D_1,D_2,D_3 and D_4 in Figure 21 which are integrated within IGBTs act as anti-parallel diodes because in this configuration diodes D_7 and D_8 of Figure 21 are not applied in the main circuit of the inverter. In this case, it was also noticed that the average output current 66 A given by the simulation

model was 12 A higher than value 54 A announced in the device specification of 15 kW UPS.

Table 6: *Results of the second simulation case where IGBTs, diodes and their configuration are chosen as they are used in the 15 kW UPS device currently.*

INVERTER CURRENT LIMIT ADJUSTMENTS						
Max. Current limit:	89 A	Avg. current:	66 A	Fault clearing capability:	C6 miniature circuit breaker	
Min. Current limit:	43 A					
Switching frequency:	17,475 kHz					
PERFORMANCE OF POWER SEMICONDUCTOR DEVICES						
Location	Component	Configuration	Avg. Conduction losses	Avg. switching losses	Avg. total losses	Avg. junction temperature
Outer IGBT	IGBT 650V 40A	Single	36,02 W	24,40 W	60,42 W	< 150 °C
Inner IGBT	IGBT 650V 50A	Single	41,45 W	32,67 WW	74,12 W	< 150 °C
Clamp diode	Diode 600V 60A	Single	1,63 W	8,63 W	10,26 W	< 150 °C
Anti-parallel diode	No component	-	-	-	-	-

However, based only on two simulation cases a generic conclusion about the size of the difference in simulation results and real world results can not be drawn in a reliable way. Thus, it can be only concluded that the simulation model may give higher output currents than which are valid in real world situations and it must be considered when the fault clearing capability of the inverter is determined according to simulation results. When the main circuit of the inverter is built with IGBTs, diodes and their configuration as per they are used in 15 kW UPS device, the fault clearing capability of the inverter is high enough to clear C6 miniature circuit breakers instantly according to simulation results of Table 6. An equal fault clearing capability is also announced for the 15 kW UPS device in its specification.

In the third simulation case, IGBTs and diodes of 20 kW UPS device were added two in parallel to the main circuit of the inverter. Current limits of the inverter were adjusted so that preconditions concerning the switching frequency and junction temperatures of IGBTs and diodes were fulfilled. Diodes must be added also two in parallel because if single diodes would be used the forward current of the diode would have exceeded the safe operating area announced in datasheets of diodes. Results of the third simulation case are shown in Table 7. According to simulation results, average output current of 173,5 A may be able to be drawn from the UPS device in short circuit situations when each IGBT and diode are installed two in parallel in the main circuit. Thus, output fault current of the inverter may be high enough to clear C16 circuit breaker.

However, C16 circuit breakers would need a momentary peak current of 226 A to ensure their operating in under 0,1s and thus it is the higher current threshold of magnetic tripping zone. The lower current threshold of magnetic tripping zone in C16 miniature circuit breakers is at 113 A and thus the current 173,5 A is located approximately in the middle of the magnetic tripping zone. Due to the wide magnetic tripping tolerance of C16 circuit breaker, it can not be verified that the current 173,5 A is always enough to clear C16 circuit breakers in few hundreds of milliseconds before the UPS trips. It may depend on manufacturer and item of the circuit breaker whether 173,5 A may clear C16 circuit breaker in under 300 ms which is the time limit how long 15 kW and 20 kW

UPS devices can operate at current limit before tripping. If a full reliability of fault clearing is desired to be ensured C10 circuit breakers should be used with this configuration even though clearing C16 circuit breakers may be possible.

Table 7: *Results of the third simulation case where IGBTs and diodes of 20 kW UPS device are installed two in parallel in the main circuit of the inverter.*

INVERTER CURRENT LIMIT ADJUSTMENTS						
Max. Current limit:	216 A	Avg. current:	173,5 A	Fault clearing capability:	C16 miniature circuit breaker	
Min. Current limit:	131 A					
Switching frequency:	17,761 kHz					
PERFORMANCE OF POWER SEMICONDUCTOR DEVICES						
Location	Component	Configuration	Avg. Conduction losses	Avg. switching losses	Avg. total losses	Avg. junction temperature
Outer IGBT	IGBT 600V 60A	two in parallel	50,83 W	33,56 W	84,39 W	139,73 °C
Inner IGBT	IGBT 650V 75A	two in parallel	36,05 W	45,96 W	82,02 W	148,86 °C
Clamp diode	Diode 600V 75A	two in parallel	2,33 W	3,56 WW	5,89 W	89,35 °C
Anti-parallel diode	Diode 1200V 60A	two in parallel	36,77 W	19,12 W	55,89 W	124,61 °C

In the configuration of fourth simulation case, IGBTs of 15 kW UPS device were added two in parallel to the main circuit and diodes of 20 kW UPS device were used as single components. Results of the fourth simulation case are shown in Table 8. With this configuration the output fault current is 130 A according to simulation results and it may clear a C10 circuit breaker. However, it should be noticed that the junction temperature of the anti-parallel diode may increase close to 150°C as shown in Table 8. Therefore, it may be reasonable to add them also two in parallel which would increase the reliability of anti-parallel diodes when the UPS operates at the current limit even though it is not compulsory as temperature is kept below 150°C according to the simulation results of Table 8.

Table 8: *Results of the fourth simulation case where IGBTs of 15 kW UPS device are installed two in parallel and diodes of 20 kW UPS device as single components in the main circuit of the inverter.*

INVERTER CURRENT LIMIT ADJUSTMENTS						
Max. Current limit:	164 A	Avg. current:	130 A	Fault clearing capability:	C10 miniature circuit breaker	
Min. Current limit:	96 A					
Switching frequency:	17,704 kHz					
PERFORMANCE OF POWER SEMICONDUCTOR DEVICES						
Location	Component	Configuration	Avg. Conduction losses	Avg. switching losses	Avg. total losses	Avg. junction temperature
Outer IGBT	IGBT 650V 40A	two in parallel	34,76 W	24,46 W	59,22 W	144,14 °C
Inner IGBT	IGBT 650V 50A	two in parallel	39,72 W	35,84 W	75,56 W	148,36 °C
Clamp diode	Diode 600V 75A	Single	4,28 W	3,91 W	8,19 W	91,05 °C
Anti-parallel diode	Diode 1200V 60A	Single	66,83 W	23,46 W	90,29 W	148,98 °C

Results of the fifth simulation case are shown in Table 9. In this case, three IGBTs of 15 kW UPS device were added in parallel and two diodes of 20 kW UPS device in parallel. Thus, the average output current of the inverter could be raised to 185,5 A without exceeding preconditions or safe operating areas of the power semiconductor devices. In fact, the maximum current limit value must be constrained in simulations to 230 A as the

inductance data of the filter inductor ended in 230 A as can be seen from the graph in Figure 26. The minimum current limit was then adjusted so that the switching frequency was settled to be slightly below 18 kHz. With this configuration, it may be possible to achieve a fault clearing capability of the inverter to clear C16 circuit breakers instantly. However, similarly as in the third simulation case, it can not be verified that the 185,5 A will always clear a C16 circuit breaker as it is still clearly below 226 A which is the higher current threshold value of magnetic tripping zone in C16 circuit breakers. Nevertheless, 185,5 A may be enough to clear C16 breakers but if reliability of the fault clearing is wanted to be confirmed C10 circuit breakers should be used.

Table 9: *Results of the fifth simulation case where IGBTs of 15 kW UPS device are installed three in parallel and diodes of 20 kW UPS device two in parallel in the main circuit of the inverter.*

INVERTER CURRENT LIMIT ADJUSTMENTS					
Max. Current limit:	230 A	Avg. current:	185,5 A	Fault clearing capability:	C16 miniature circuit breaker
Min. Current limit:	141 A				
Switching frequency:	17,85 kHz				

PERFORMANCE OF POWER SEMICONDUCTOR DEVICES						
Location	Component	Configuration	Avg. Conduction losses	Avg. switching losses	Avg. total losses	Avg. junction temperature
Outer IGBT	IGBT 650V 40A	three in parallel	32,25 W	23,01 W	55,27W	140,19 ℃
Inner IGBT	IGBT 650V 50A	three in parallel	36,60 W	33,94 W	70,54 W	144,16 ℃
Clamp diode	Diode 600V 75A	two in parallel	2,58 W	3,67 W	6,25 W	89,61 ℃
Anti-parallel diode	Diode 1200V 60A	two in parallel	40,58 W	20,07 W	60,66 W	127,98 ℃

During simulations it was noticed, that when the switching frequency of the inverter was decreased, by increasing the difference between maximum and minimum current limit values, average output current of the inverter could be somewhat increased without causing significant increase in junction temperatures of IGBTs. The reason for that results from the decreased average switching losses of IGBTs when the switching frequency is decreased. Thus, of course, the conduction losses of IGBTs and diodes increase as conduction times and current magnitudes increase due to the lowered switching frequency. However, the switching losses of IGBTs may decrease more than conduction losses increase when the switching frequency is lowered a certain amount. Therefore, a possibility to increase the average output current of the inverter may be realized.

Practically, however, changing the switching frequency may not be easily realizable in existing 15 kW and 20 kW UPS devices which are used as reference devices. This originates from control systems of the UPS devices which may be adjusted to function only at certain clock frequencies such as 18 kHz and they may not be easily modified. Nevertheless, in sixth, seventh and eighth simulation cases were investigated average output currents and fault clearing capabilities of UPS inverters when the switching frequency is lowered from around 18 kHz.

Table 10 shows simulation results for the sixth simulation case where the main circuit of the inverter is implemented according to power semiconductor components which are used currently in 20 kW UPS device. However, the switching frequency of the inverter is lowered from 17,8 kHz to 15,6 kHz. When results in Table 5 and in Table 10

are compared, it is seen that the average output current of the inverter may be increased from 84,5 A to 89 A when the switching frequency is lowered. This may not increase the fault clearing capability of the inverter to one size larger circuit breaker, however, the higher output current increases the probability that the C6 circuit breaker may be cleared instantly in its magnetic tripping zone if a short circuit occurs at the load side of the UPS. The maximum current limit value is limited to 119 A as otherwise the safe operating area of IGBTs would be exceeded in the configuration.

Table 10: *Results of the sixth simulation case where a lower switching frequency is used and IGBTs, diodes and their configuration are chosen as per they are applied in the 20 kW UPS device currently.*

INVERTER CURRENT LIMIT ADJUSTMENTS						
Max. Current limit:	119 A	Avg. current:	89 A	Fault clearing capability:	C6 miniature circuit breaker	
Min. Current limit:	59 A					
Switching frequency:	15,619 kHz					
PERFORMANCE OF POWER SEMICONDUCTOR DEVICES						
Location	Component	Configuration	Avg. Conduction losses	Avg. switching losses	Avg. total losses	Avg. junction temperature
Outer IGBT	IGBT 600V 60A	Single	53,35 W	31,24 W	84,59 W	139,87 ℃
Inner IGBT	IGBT 650V 75A	Single	37,38 W	41,58 W	78,96 W	146,48 ℃
Clamp diode	Diode 600V 75A	Single	2,19 W	3,00 W	5,19 W	88,83 ℃
Anti-parallel diode	Diode 1200V 60A	Single	38,48 W	16,16 W	54,64 W	123,72 ℃

In the seventh simulation case, the configuration of IGBTs and diodes is the same as in the third simulation case, where components of 20 kW UPS device are added two in parallel to the main circuit. However, the switching frequency is lowered from 17,8 kHz to 15,9 kHz. Simulation results in Table 11 show that with a lowered switching frequency output current of the inverter may be increased from 173,5 A to 181 A when results in Table 11 are compared to results in Table 7. Lowering the switching frequency may therefore consolidate the probability that the UPS device has the fault clearing capability to clear C16 circuit breakers.

Table 11: *Results of the seventh simulation case where IGBTs and diodes of 20 kW UPS device are added two in parallel to the main circuit and the switching frequency is lowered.*

INVERTER CURRENT LIMIT ADJUSTMENTS						
Max. Current limit:	230 A	Avg. current:	181 A	Fault clearing capability:	C16 miniature circuit breaker	
Min. Current limit:	132 A					
Switching frequency:	15,9 kHz					
PERFORMANCE OF POWER SEMICONDUCTOR DEVICES						
Location	Component	Configuration	Avg. Conduction losses	Avg. switching losses	Avg. total losses	Avg. junction temperature
Outer IGBT	IGBT 600V 60A	two in parallel	54,31 W	32,51 W	86,82 W	141,32 ℃
Inner IGBT	IGBT 650V 75A	two in parallel	38,04 W	43,37 W	81,41 W	148,39 ℃
Clamp diode	Diode 600V 75A	two in parallel	2,23 W	3,19 W	5,42 W	89,00 ℃
Anti-parallel diode	Diode 1200V 60A	two in parallel	39,17 W	17,11 W	56,27 W	124,88 ℃

In the eighth simulation case, IGBTs of 15 kW UPS device are added two in parallel, the clamp diode of 20 kW UPS device is used as a single component and anti-parallel diodes

of 20 kW UPS device are added two in parallel to the main circuit of the inverter. Results of the eighth simulation case are shown in Table 12.

Table 12: *Results of the eighth simulation case where IGBTs of 15 kW UPS device are added two in parallel, clamp diode of 20 kW UPS device is used as a single component and anti-parallel diodes of 20 kW UPS device are added two in parallel to the main circuit. Furthermore, switching frequency of the inverter is lowered from 18 kHz.*

INVERTER CURRENT LIMIT ADJUSTMENTS						
Max. Current limit:	190 A	Avg. current:	143 A	Fault clearing capability:	C10 miniature circuit breaker	
Min. Current limit:	96 A					
Switching frequency:	13,793 kHz					
PERFORMANCE OF POWER SEMICONDUCTOR DEVICES						
Location	Component	Configuration	Avg. Conduction losses	Avg. switching losses	Avg. total losses	Avg. junction temperature
Outer IGBT	IGBT 650V 40A	two in parallel	40,01 W	21,57 W	61,59 W	146,51 °C
Inner IGBT	IGBT 650V 50A	two in parallel	45,76 W	30,30 W	76,06 W	148,79 °C
Clamp diode	Diode 600V 75A	single diode	3,91 W	3,04 W	6,96 W	90,14 °C
Anti-parallel diode	Diode 1200V 60A	two in parallel	27,74 W	12,84 W	40,58 W	113,76 °C

The switching frequency of the inverter is 13,8 kHz and thus output current of 143 A may be drawn from the inverter without exceeding safe operating areas of IGBTs and diodes. The configuration is nearly the same as in the fourth simulation case presented in Table 8. However, anti-parallel diodes must be added two in parallel in the eighth simulation case due to the 143 A output current of the inverter as if single anti-parallel diodes would be used the junction temperature in them would raise over 150ºC. The increase in the output current can be seen by comparing simulation results of Table 8 and Table 12. With the configuration and switching frequency of the eighth simulation case, the fault clearing capability of the inverter to clear C10 circuit breakers may be consolidated compared to the fourth simulation case where output current of the inverter is 13 A lower. On the other hand, anti-parallel diodes are required two more per one inverter leg of a three-level UPS inverter in the configuration of the eighth simulation case.

As a consequence, it can be concluded according to simulation results presented in Tables 10,11 and 12 that output currents of UPS devices operating at current limit may be increased 5–10% by optimizing the switching frequency of the UPS inverter.

5.3.3 Cost comparison of solutions to improve the fault clearing capability of a UPS device

One of interests in this thesis is to study the cost of required modifications in IGBT and diode configuration so that the UPS device may have a fault clearing capability to clear C16 miniature circuit breakers and compare it to the cost of the fault clearing circuitry which may also clear C16 circuit breakers. Cost comparisons are applied for a three-phase three-level UPS inverter. Thus, when IGBTs and diodes are added in parallel to the main circuit of the inverter, they are added to all three phases on upper and lower branches of inverter legs. Similarly, the fault clearing circuitry, which is based on the circuit diagram

presented in Figure 20, is applied at the output of a three-phase UPS device. Therefore, the number of silicon controlled rectifiers in Figure 20 must be tripled which results in six silicon controlled rectifiers which are required in total in the fault clearing circuitry of a three-phase UPS device.

From results of simulation cases presented in Chapter 5.3.2 it is seen that IGBT and diode configurations which are used in the third and fifth simulation case may have the capability to clear a C16 circuit breaker. A configuration in the third simulation case comprises of two IGBTs of 20 kW UPS device connected in parallel and two diodes of 20 kW UPS device connected in parallel. In the fifth simulation case, three IGBTs of 15 kW UPS device are connected in parallel and two diodes of 20 kW UPS device are connected in parallel. Simulation results for the third and fifth simulation cases are presented in Tables 6 and 8. From results can be seen that 12 A higher output current is achieved by applying the configuration of IGBTs and diodes which is used in the fifth simulation than which is used in the third simulation case. Thus, a probability that the maximum output current achieved with the configuration suffices to clear C16 circuit breakers instantly is higher in the fifth simulation case.

However, as explained in Chapter 5.3.2, it can not be guaranteed that output currents of configurations in both simulation cases are high enough to clear C16 circuit breakers instantly in all cases before the UPS device itself trips to overcurrent. Therefore, a full certainty for the UPS inverter to clear C16 circuit breakers with IGBT and diode configurations of the third and fifth simulation cases can not be provided. It should be considered when technical applicability of configurations in the third and fifth simulation case to improve the fault clearing capability of UPS device is discussed. Nevertheless, in simulations of this thesis, configurations in the third and fifth simulation cases provided the greatest probability to clear C16 breakers. The lack of the filter inductance data prevented executing simulation cases with a higher maximum current limit value than 230 A. Extrapolating the filter inductance data further from 230 A would have weakened the scientific reliability of simulation results and therefore it was not performed in this thesis.

Table 13 presents a cost comparison between estimated costs of configuration changes which are required to be implemented to the original main circuit of the inverter in the third and fifth simulation cases. Thus, costs are calculated in Table 13 according to the cost of IGBTs and diodes which are added in parallel with single IGBTs and diodes of the original main circuit of the inverter. The original main circuit of the inverter denotes in these cases the main circuit which consists only of single IGBTs and diodes.

The original main circuit of the inverter in the third simulation case is equal with the main circuit of the inverter used in 20 kW UPS device which consists of single components presented in Table 3. The original main circuit of the inverter in the fifth simulation case consists of single IGBTs of 15 kW UPS inverter and single diodes of 20 kW UPS inverter. Therefore, the original main circuit of the inverter in the fifth simulation case does not represent either of the real 15 kW or 20 kW UPS inverters whose power semiconductors are presented in Table 3. However, in principle such configuration of the main circuit of the inverter could be designed and built.

In addition, other expenses which may result from adding IGBTs and diodes in parallel, such as heatsink enlargement, added gate drivers and added gate resistors, are estimated in sections 'heatsink' and 'other' in Table 13. The cost comparison is based on real prices which are achieved from a UPS manufacturer. However, costs are announced only as proportional prices. Cost comparison between simulation cases is implemented so that the cost of the fifth simulation case is compared to cost of the third simulation case which reference cost are determined to be 1,0 as presented in Table 13.

Table 13: *Cost comparison executed as proportional prices between cost of added components in the third and fifth simulation case. Configurations are applied for a three-phase three-level UPS inverter.*

COST OF ADDED COMPONENTS IN THE CONFIGURATION		
	Simulation case 3	Simulation case 5
IGBTs	1,00	1,86
Diodes	1,00	1,00
Heatsink	1,00	1,29
Other	1,00	2,00
Total	1,00	1,48

From the cost comparison presented in Table 13 can be seen that only the cost of diodes is equal with the two simulation cases. It is obvious since in both simulation cases diodes of 20 kW UPS inverter are added in parallel with original diodes of the main circuit. Otherwise, the configuration in the third simulation case will be cheaper to implement in all observed sections as shown in Table 13. The cost of IGBTs is 86 % higher in the fifth simulation case than in the third simulation case. It is caused by the two IGBTs of 15 kW UPS inverter which are required to be added in parallel with original IGBTs in the fifth simulation case. It raises the cost of IGBTs higher than in the third simulation case where single IGBTs of 20 kW UPS inverter are added in parallel with original IGBTs. Even though the cost of single IGBTs of 15 kW UPS inverter may be lower than IGBTs of 20 kW UPS inverter, the cost of IGBTs in the fifth simulation case remains higher due to the higher number of IGBTs required in the configuration.

The cost of all components in total which are required to be added in the configuration of the fifth simulation case are nearly 48 % higher compared to the cost of components required to be added in the third simulation case. Furthermore, the configuration of the fifth simulation case may include more expenses resulting from wirings and mechanics as it consists of higher number of IGBTs. However, costs resulting from changes in mechanics and wirings are not included in Table 13. The section 'other' in Table 13 includes, for instance, cost of gate drives and gate resistors which are related to number of added IGBTs. In addition, due to the higher number of IGBTs in the fifth simulation case, a larger heatsink may be required which increases the cost of a heatsink.

According to the cost comparison between configurations of third and fifth simulation cases it can be discovered that improving the fault clearing capability of a UPS device is more economical to be implemented according to the configuration of the third simulation case than with the configuration of the fifth simulation case. Therefore, a cost comparison between the cost of the configuration in the third simulation case and the cost of the fault clearing circuitry is executed next.

An estimated cost structure of the fault clearing circuitry is shown in Table 14 where costs of different electrical components of the fault clearing circuitry are separated. Costs in Table 14 are announced in proportion to total costs of electrical components in the fault clearing circuitry. Proportional costs are based on real and estimated prices of electrical components used in the fault clearing circuitry. The section 'other electrical components' in Table 14 includes, for instance, cost of resistors, gate drivers, wire terminals and printed circuit board which are required in implementing the fault clearing circuitry.

Table 14: *Estimated cost structure of the fault clearing circuitry. Costs are announced in proportion to total costs of electrical components in the fault clearing circuitry.*

Cost structure of the fault clearing circuitry	
Silicon controlled rectifiers	0,30
Capacitors	0,20
Inductors	0,22
Diodes	0,05
Other electrical components	0,23
Total	1,00

From the estimated cost structure of the fault clearing circuitry can be seen, that a majority of costs results from silicon controlled rectifiers, capacitors and inductors which cover in total approximately 72 % of total costs of electrical components in the fault clearing circuitry. It should be noticed that total costs presented in Table 14 do not include costs resulting from wirings and mechanics which obviously increase total costs of the fault clearing circuitry. It may be estimated that mechanics and wirings will increase total costs of the fault clearing circuitry with several dozens of percentages.

An estimated total cost of added components in the configuration of the third simulation case is compared to the estimated total cost of the electrical components required in the fault clearing circuitry. As a result, it was noticed that the total cost of components which are required to be added in the third simulation case may be approximately 14 % higher compared to the total cost of electrical components required in the fault clearing circuitry. However, the enlargement of the heatsink was included to the calculated total cost of the configuration in the third simulation case. If the enlargement of the heatsink is omitted from cost calculations in the third simulation case and thus only cost of electrical components of solutions are compared with each other, it was noticed that the cost

of electrical components in the configuration of the third simulation case is 9 % lower compared to the cost of electrical components in the fault clearing circuitry.
The cost of mechanics and wirings of solutions was not included in the above presented cost comparison. However, it can be estimated that the cost of wirings and mechanics may be higher in the fault clearing circuitry than in the configuration change of the inverter main circuit. The fault clearing circuitry would be a completely separate module which may be installed, for example, on top of the UPS device and therefore it may require installing more new mechanics and wirings than is required in the configuration change. In the configuration change where IGBTs and diodes are added in parallel with the original IGBTs and diodes, the existing mechanics and wirings could be better utilized which may lead to lower costs resulting from mechanics changes and new wirings.

If a coarse comparison between total costs of the two solutions is performed, when cost of wirings and mechanics is included in the comparison, it can be estimated that cost of the configuration change implemented according to the third simulation case may result in 10–20 % lower total costs compared to the cost of the fault clearing circuitry. However, it must be highlighted that especially estimations of costs of mechanics and wirings are very coarse since estimating them more precisely would require more prepared designs to exist. Nevertheless, according to results of the cost comparison performed in this thesis, it seems that it is somewhat more economical to improve the fault clearing capability of a UPS device by adding IGBTs and diodes of 20 kW UPS inverter in parallel with existing IGBTs and diodes of 20 kW UPS inverter than by using the fault clearing circuitry. However, technically the fault clearing circuitry may provide better reliability to clear C16 circuit breakers than configuration of the inverter main circuit where IGBTs and diodes of 20 kW UPS inverter are added two in parallel.

Practically, it can be deduced, that according to the simulation results of third and fifth simulation case, at least three IGBTs and two diodes of 20 kW UPS inverter should be added in parallel so that output current of the inverter could be increased close to 226 A and hence C16 circuit breakers could be cleared in a reliable way. However, in that case the configuration change in the main circuit may lead to 20–30 % higher costs in total compared to the cost of the fault clearing circuitry.

Therefore, it can be concluded that using the fault clearing circuitry is a more economical way to improve the fault clearing capability of a 20 kW UPS device to clear C16 breakers reliably than making the required configuration changes to the main circuit of the UPS inverter. However, it must be noticed that difference between cost estimations of the solutions is not substantial and therefore either of the solutions can not be considered as superior compared to another.

Nevertheless, other advantages which the fault clearing circuitry provides compared to the configuration change is that it may be installed only to UPS devices of customers who require higher fault clearing capability than which the UPS device may afford as standard. Thus, the fault clearing circuitry provides more flexibility since it is not required to be installed to those customer devices for which the improvement of the fault clearing capability is not necessary. Adding the fault clearing circuitry to existing UPS

designs afterwards may be also more feasible to implement than making the required configuration changes afterwards. New main circuit and mechanics designs must be probably developed to the existing UPS inverter so that configuration changes can be implemented as the physical space in the present main circuit board may not be large enough so that required number of new components can be added there.

In addition, it shall be considered that when the number of power semiconductors in the main circuit of the UPS inverter grows, the number of components which may fail during normal operation of a double conversion UPS also grows. Instead, components in the fault clearing circuitry are not continuously stressed by a load current when the double conversion UPS operates in normal mode. In the fault clearing circuitry components are conducting current only during charging and discharging of capacitors and at times when the fault clearing circuitry is triggered. Otherwise, capacitors are kept being charged and other components in the fault clearing circuitry experience voltage stress but they are not conducting current which may reduce their probability to fail accidentally during normal operation of the double conversion UPS.

6 SUMMARY AND CONCLUSIONS

The aim of this thesis was to find economical ways to improve the fault clearing capability of a UPS device. Characteristics of IGBTs and diodes in the main circuit of a UPS inverter determine the highest magnitude where the maximum current limit of the UPS inverter may be adjusted when the UPS is operating in stored-energy mode. Exceeding maximum operating currents, voltages or junction temperatures of IGBTs and diodes may lead to their break down and thus must be avoided. However, if a short circuit or a ground fault occurs in the load side of the UPS and the UPS is operating in stored-energy mode, the UPS must supply enough output current at its current limit to clear a respective circuit breaker on the load side before the UPS itself trips to overcurrent. By clearing the circuit breaker, the fault location may be isolated and the UPS can continue to supply power to remaining loads. Therefore, the current limit of the UPS shall be adjusted as high as possible so that a selective fault clearing may be executed with circuit breakers. However, it must be considered from not causing damage to power semiconductor devices in the main circuit of the UPS inverter when the UPS operates at current limit.

The problem is that at present UPS devices must be oversized in terms of rated current and rated power if circuit breakers protecting the load of the UPS and its wires are larger in terms of rated current and type of the circuit breaker than which is the fault clearing capability of a UPS device. Oversizing the whole UPS device only to achieve a higher fault clearing capability is dispensable during normal operation of the UPS.

In this thesis a simulation model was developed, which can be used to estimate how much output current of a UPS operating at current limit may be increased, or the fault clearing capability of a UPS device improved, by installing IGBTs and diodes in parallel to the main circuit of a UPS inverter. Thus, only the current-carrying capacity of the UPS inverter is consolidated but the whole UPS device including, for instance, the AC/DC rectifier is not oversized. The simulation model requires the user to input data which may be obtained from datasheets of IGBTs and diodes. It calculates average power losses of IGBTs and diodes and the switching frequency of IGBTs based on shape of the current waveform when the UPS operates at current limit. Number of IGBTs and diodes connected in parallel in the main circuit of the inverter can be entered as input to the simulation model. From average power losses, the simulation model derives average junction temperatures of IGBTs and diodes which may be used as references when adequate current limit values are adjusted for the inverter.

In simulations it was investigated that what kind of IGBT and diode configuration in the main circuit of the UPS inverter is required so that the UPS has a fault clearing capability to clear C16 miniature circuit breakers. The study was implemented by using IGBTs and diodes which are currently used as single components in 20 kW and 15 kW UPS inverters. Hence, the aim of simulations was to study if the fault clearing capability

of the existing 20 kW UPS device could be improved from C6 circuit breakers to C16 circuit breakers by adding IGBTs and diodes in parallel with existing power semiconductors in the main circuit of the UPS inverter. Furthermore, the cost of changes which are required to be done into the main circuit of the existing UPS inverter was estimated.

A fault clearing circuitry, which has been developed to improve the fault clearing capability of a UPS device was also introduced in this thesis. Inventors of the fault clearing circuitry have proven that it is able to supply enough current to clear C16 circuit breakers in short circuit situations. Consequently, the fault clearing capability of a UPS device may be improved without making changes to the main circuit of the UPS inverter if the presented fault clearing circuitry is installed at the UPS output. A cost analysis of the fault clearing circuitry was executed and the estimated cost of the fault clearing circuitry was compared to the cost of the configuration change in the main circuit of the UPS inverter which may enable achieving the desired fault clearing capability.

As a result of simulations, it was discovered that by using two IGBTs and two diodes of 20 kW UPS device in parallel or by using three IGBTs of 15 kW UPS device and two diodes of 20 kW UPS device in parallel the fault clearing capability of a UPS to clear C16 circuit breakers may be achieved. However, it was also noticed that magnitudes of output currents 173 A and 185,5 A achieved with above mentioned configurations in the simulation model may not be high enough to clear C16 breakers instantly in all cases. Even though the output currents lie in the magnetic tripping zone of C16 circuit breaker, they are clearly below the higher current threshold 226 A of the magnetic tripping zone. Hence, above presented configurations do not provide full certainty to clear C16 circuit breakers instantly in all cases. Nevertheless, during simulations it was observed that by lowering the switching frequency of the UPS inverter a certain amount from 18 kHz output currents of UPS devices operating at current limit could be increased 5–10 %. However, changing the switching frequency of the UPS inverter may not be easily realizable with the existing 20 kW UPS device as the control system of the UPS is adjusted to function at 18 kHz clock frequency and therefore it prevents changing the switching frequency dynamically.

Simulations were not performed with IGBT and diode configurations which could clear C16 circuit breaker reliably due to a lack of filter inductance data on higher current values. Nevertheless, it was deduced that practically at least three IGBTs and two diodes of 20 kW UPS device are required to be used in parallel in the main circuit of the UPS inverter so that the fault clearing capability of a UPS to clear C16 circuit breakers may be ensured. In that case, however, it was estimated that implementing the configuration change may result in 20–30 % higher costs compared to the cost of implementing the fault clearing circuitry. Thus, the result of cost comparison supports the fault clearing circuitry as a more economical solution to improve the fault clearing capability of a UPS device. However, the cost difference is not remarkable and thus the fault clearing circuitry can not be considered as superior solution in terms of arising costs compared to the configuration change. In addition, it must be highlighted that cost calculations included coarse estimations especially on cost of mechanics and wirings of the solutions which

were hard to estimate accurately due to a lack of proper and valid designs. Hence, the result of cost comparison shall be considered only as suggestive.
Technically the fault clearing circuitry may be a more feasible solution to be applied in existing UPS devices than the configuration change. The fault clearing circuitry can be installed, for example, on top of a UPS device without a need to make significant modifications to the framework of the UPS device. However, new main circuit and mechanics designs may be required to be implemented when IGBTs and diodes are added in parallel to the main circuit of the UPS inverter if added components do not physically fit to the existing main circuit board. Another advantage which the fault clearing circuitry provides is its flexibility since it can be installed only to UPS devices of such customers who require higher fault clearing capability for their UPS devices than is afforded as standard.

Furthermore, an inevitable risk that arises from adding more IGBTs and diodes in parallel to the main circuit of the inverter is that at the same time the number of components which may accidentally fail during normal operation of a double conversion UPS is increased as IGBTs and diodes conduct current when the inverter is operating normally. On the other hand, components in the fault clearing circuitry conduct current only during charging and discharging of capacitors and when the fault clearing circuitry is triggered. Hence, they do not conduct current continuously during normal operation of the double conversion UPS which may reduce their risk to fail accidentally in normal operation mode of the UPS.

Finally, it can be concluded that the fault clearing circuitry appears to be a more efficient solution to improve the fault clearing capability of a UPS device both economically and technically compared to the configuration change in the main circuit of a UPS inverter. However, more detailed mechanics and electrical designs should be implemented for the solutions so that a more precise cost comparison between the solutions may be performed. In the future, same kind of study as performed in this thesis could be performed to UPS inverters of higher rated powers and investigate what is the most economical way to improve the fault clearing capability in that case. Additionally, when the power semiconductor technology develops in the future and if, for example, the use of silicon carbide replaces the use of silicon in power semiconductor devices, further studies could be conducted on investigating how this development affects dynamic characteristics of power semiconductor devices used in UPS inverters.

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