DESIGN AND ANALYSIS OF A FAST TRANSIENT VOLTAGE REGULATOR WITH ALL CERAMIC OUTPUT CAPACITORS FOR MOBILE MICROPROCESSORS

By

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ABSTRAK

Keperluan untuk mereka bentuk pengatur voltan yang mempunyai tindak balas transien yang cepat didorong oleh kadar transien yang semakin meningkat daripada mikropemproses mudah alih. Oleh itu, mengoptimumkan frekuensi pensuisan pengatur voltan menjadi langkah penting untuk mencapai keseimbangan antara mengekalkan kecekapan pengatur voltan dan meningkatkan tindak balas transien. Kapasitor seramik berlapis telah menjadi lebih popular sebagai kapasitor output pengantara voltan disebabkan oleh saiznya yang kecil dan kos murah.

Walaupun topologi penukar buck kekal tidak berubah betahun-tahun, terdapat banyak inovasi dan kejayaan cemerlang dalam peringkat kuasa pengatur voltan dan teknologi kawalan. Selain itu, reka bentuk yang berorientasikan galangan keluaran dan AVP (Penempatan Voltan Automatik) telah diperkenalkan untuk menangani keperluan transien. Banyak kajian juga memberi tumpuan untuk meningkatkan kecekapan pegantara voltage terutama untuk system yang beroperasi dengan bateri.

Sebuah pengatur voltan bertindak balas laju yang mempunyai hanya kapasitor output seramik untuk mikropemproses mudah alih dicadangkan dalam kajian ini. Hasil kajian ini menunjukkan bahawa pengatur voltan yang direka adalah stabil dengan jenis dan bilangan kapasitor seramik berlapisan yang dicadangkan. Lebih penting lagi, keputusan transien juga adalah sehampir dengan keputusan simulasi di mana output pengantara voltan tidak mengalami kelanjakan dan kejatuhan voltan semasa dimuatkan dengan arus dinamik yang bermaknitud 10.5A dalam 1μs. Kesimpulannya, sebuah pengatur voltan dengan tindak balas laju yang mempunyai hanya kapasitor output seramik telah direka dan dianalisis and ia mempunyai tindak balas transien yang lebih baik berbanding dengan reka bentuk asal.

ABSTRACT

The need to have fast transient response of the voltage regulator is driven by the increasing current slew rate of the mobile microprocessor. Hence, optimizing the switching frequency of the voltage regulator becomes an important step to achieve a balance between preserving the efficiency of the voltage regulator and improving the transient response. Besides, output capacitor solution with multilayer ceramic capacitor has also become more popular due to its small size and cheap cost.

Over the years, even though the topology of the buck converter remains unchanged, there are plenty of innovations and breakthroughs in the power stage of the voltage regulator and controller technology. In addition, output impedance oriented design and adaptive voltage positioning (AVP) feature are also introduced to address the transient requirements. Apart from improving the dynamic response of the voltage regulator, many research works also focus on improving the efficiency of the voltage regulator, especially for battery-powered systems.

A fast transient voltage regulator with all ceramic output capacitors for mobile microprocessor is proposed in this study. The outcome of the study shows that the voltage regulator designed is stable with the proposed type and number of multilayer ceramic capacitors. More importantly, the actual transient results correlate well with the simulation results where minimal transient droop and overshoot are observed with a dynamic current load step with a slew rate of 10.5A per 1 µs. In conclusion, a fast transient voltage regulator with all ceramic output capacitors is designed and analyzed which proven to have better transient performance compared to the original design on the test board.

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LIST OF SYMBOLS

AC	Alternating current
A_{CS}	Gain of current sense amplifier
AVP	Adaptive voltage positioning
B_{max}	Maximum flux density
C_{boot}	Bootstrap capacitor
CCM	Continuous conduction mode
C_{droop}	Droop setting capacitor
C_{DS}	Drain-to-Source capacitance
C_{GD}	Gate-to-Drain capacitance
C_{GS}	Gate-to-Source capacitance
C_{in}	Input capacitance
C_{ISS}	Input parasitic capacitance of MOSFET
CMC	Current mode control
C_{OSS}	Output parasitic capacitance of MOSFET
C_{out}	Output capacitance
CPU	Central processing unit
C_{RSS}	Transfer parasitic capacitance
CSN	Negative current sense feedback terminal
CSP	Positive current sense feedback terminal
C_{VDD}	Input capacitance for supply voltage V_{DD}
dB	Decibel
DC	Direct current

DCM	Discontinuous conduction mode
DCR	Parasitic resistance of the inductor
DRVH	High-side MOSFET driver signal
DRVL	Low-side MOSFET driver signal
ESL	Equivalent series inductance of the capacitor
ESR	Equivalent series resistance of the capacitor
ET	Volt-second balance of the inductor
F_{CO}	Bandwidth of the voltage regulator
FET	Field effect transistor
FOM	Figure of merit
F_{SW}	Switching frequency
F_Z	Frequency of zero
GFB	Ground feedback terminal
G_L	Loop gain
G_M	Gain of error amplifier
GPU	Graphic Processing Unit
I_{DIODE}	Diode current
HS	Hide-side
I_{DRVH}	Driver signal current
I_{max}	Maximum load current
IMVP7	Intel mobile voltage positioning – 7
I_{out}	Output current
$I_{q5V\_controller}$	5V quiescent current of the controller
$I_{q3.3V\_controller}$	3.3V quiescent current of the controller
I_{q5V_driver}	5V quiescent current of the driver

$I_{q3.3V\_driver}$	3.3V quiescent current of the driver
I_{rr}	Reverse recovery current
I_{sat}	Saturation current of inductor
I_{step}	Dynamic current step of the load current
L_o	Ouput inductance
L_{out}	Output inductor
LS	Low-side
L_{VR}	Series inductor for voltage regulator model
MLCC	Multi-layer ceramic capacitor
MOSFET	Metal oxide field effect transistor
N-Ph	Number of phase
NVDC	Narrow direct current voltage
PCB	Printed circuit board
P_{core_PWM}	Core loss of inductor in PWM mode
PDN	Power delivery network
PFM	Pulse frequency modulation
PWM	Pulse width modulation
Q_G	Gate charge of MOSFET
Q_{GD}	Gate-to-Drain charge of MOSFET
Q_{GS}	Gate-to-Source charge of MOSFET
Q_{TH}	Gate charge of MOSFET at threshold point
Q_{OSS}	Output charge of MOSFET
Q_{rr}	Reverse recovery charger of MOSFET
Q_{SW}	Gate charge at switch point voltage
R_{cs}	Equivalent current sense resistance

R_{damp}	Damping resistor for MOSFET driver signal
R_{driver_sink}	Internal sinking resistance of driver
R_{driver_source}	Internal sourcing resistance of driver
R_{droop}	Droop setting resistor
$R_{ds(on)}$	Drain-to-source resistance of MOSFET
R_g	Internal gate resistance of MOSFET
R_{LL}	Load line
R_{load}	Output loading resistance
SMD	Surface mount device
SMT	Surface mount technology
SVID	Serial voltage identification
SW	Switch node
T_{DEAD}	Dead time
$T_{DLY(fall)}$	Delay time for falling edge
$T_{DLY(rise)}$	Delay time for rising edge
T_{off}	OFF time
T_{on}	ON time
T_{period}	Period
T_{rr}	Reverse recovery time
T_{slew}	Slew time
V_c	Control voltage
V_{DIODE_LS}	Forward voltage drop of body diode of low-side MOSFET
V_{DRIVE}	Driver voltage
V_{DS}	Drain-to-source voltage
VFB	Voltage feedback terminal

V_{GS}	Gate-to-Source voltage
$V_{GS(th)}$	Gate-to-Source threshold voltage
V_{in}	Input voltage
VMC	Voltage mode control
Vo	Output voltage
Vout	Output voltage
VR	Voltage regulator
V_{SP}	Switch point voltage
Z_c	Impedance of output capacitor
Z_{droop}	Impedance of droop setting RC components
Z_{out}	Output impedance
Z_{target}	Target impedance
Z_{vr}	Ouput impedance of voltage regulator

CHAPTER 1

INTRODUCTION

1.0 Chapter Overview

Chapter 1 is the introductory chapter of this study. First of all, Section 1.1 provides the background of the study and also listed down the five important criteria for a good voltage regulator in mobile segment. Section 1.2 explains the trend of switching frequency in the industry and the challenges to optimize the switching frequency to achieve a balance between good transient performance and good efficiency. Section 1.3 justifies the need to design a fast transient voltage regulator with optimized number of output capacitor in order to keep the solution size small and cheap. The problem statement and research objective are presented in Section 1.4 and Section 1.5 respectively. Last but not least, Section 1.6 provides the thesis outline.

1.1 Background

Non-isolated DC-DC voltage regulator is the key component of power delivery network in a modern computer system. It is used to step down the high DC input voltage to a well regulated lower output voltage which is consumed by platform devices. Out of all the platform devices, the design of the voltage regulator for the processor is most demanding and challenging because the quality of the power delivery network to the processor determines the overall performance of the system.

There are many key parameters which dictates the quality of a voltage regulator design. In fact, the importance of each parameters can be varied across different industry and segments. Figure 1.1 depicts the key parameters for a good voltage regulator design for mobile system such as laptop.

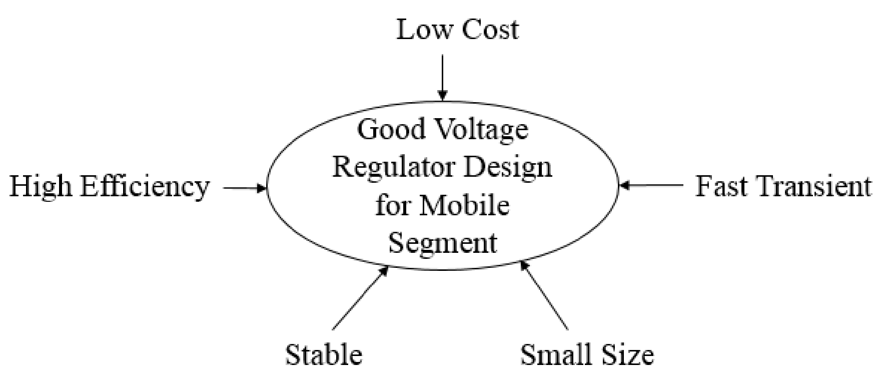

Figure 1.1: Key design requirements for power delivery circuits on mobile computer

First of all, the voltage regulator must be stable under all possible operating conditions, and this is the most important and fundamental requirement. Secondly, fast transient response of the voltage regulator has become more and more important as the mobile processor load current switches at a much higher slew rate nowadays. A fast reacting and stable voltage regulator is able to keep the output voltage under the specified regulation window even when high current transient event happens. A fast transient voltage regulator can also bring significant cost and area benefit to the voltage regulator solution. The reason is when the voltage regulator can react fast enough to high frequency transient, significant amount of output capacitors can be saved. This directly translates to less design cost and board area occupied.

Efficiency is another key metric to gauge the quality of the voltage regulator in a mobile computer system. A voltage regulator with good efficiency has low power loss which is translated to prolonged battery life for a battery-powered system. In addition, an efficient voltage regulator requires only simple thermal solution. In a greater extent, the whole system can be designed in a chassis with no fan at all. In fact, fan-less design is very much a requirement in thin and light-weight laptop design such as Intel's Ultrabooks.

1.2 Switching Frequency of Voltage Regulator

Typical design specifications for a switching regulator includes input voltage range, output voltage, maximum output current, and worst case magnitude of the dynamic output current. Switching frequency is the key design parameter that has direct impact to the transient performance and efficiency of the voltage regulator. Figure 1.3 below shows the typical switching frequency for different power converters in the market. For the case of voltage regulator residing in a mobile computer system, the switching frequency ranges from 200 kHz to 1 MHz. In fact, the trend for switching frequency of voltage regulator has been increasing steadily over the years.

Figure 1.2: Switching frequency of different voltage regulators [1]

High switching frequency is good for transient performance and reducing size of the passive components such as inductor and capacitors of the voltage regulator. However, too high of a switching frequency will degrade the efficiency of the voltage regulator and increase the risk of control loop instability. Hence, voltage regulator designer faces a great challenge to find the suitable switching frequency in order to meet both the efficiency and transient performance targets.

1.3 The Need for Fast Transient Voltage Regulator

Moore's law propelled the semiconductor industry to double the number of transistors integrated into the processor every 18 to 24 months as shown in Figure 1.4 below. In addition, advancement of semiconductor manufacturing process also helps to reduce the supply voltage to the processor to sub-1V in the most recent processors.

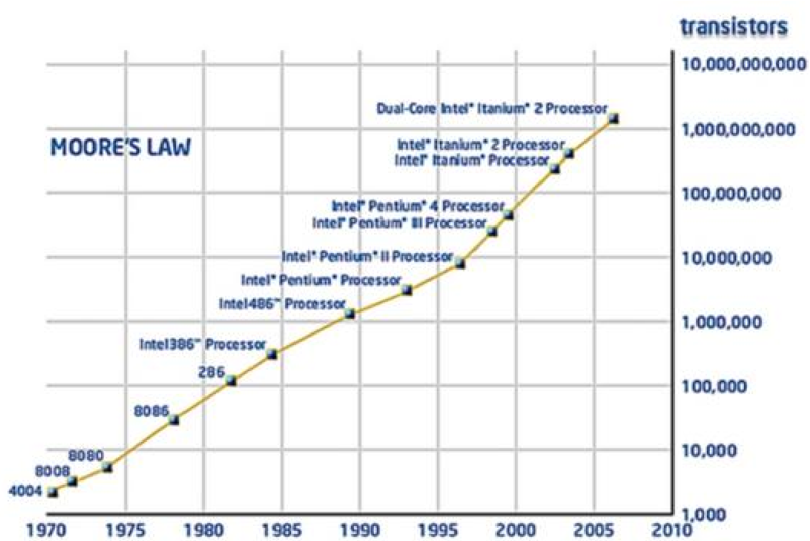

Figure 1.3: Increasing number of transistors integrated into the processor according to Moore's law [2]

However, current demand for processors is increasing year-over-year due to aggressive integration strategy and increasing complexity of circuit blocks inside the processor. Besides, computational frequency of the processor will always be pushed higher from one generation of processor to the next. Together with incremental power saving states being introduced to the processor C-states, the current profile of the processor becomes more dynamic in nature. Figure 1.5 below shows that the trend of the current slew rate of processor is increasing year-over-year when new generation of processors are released.

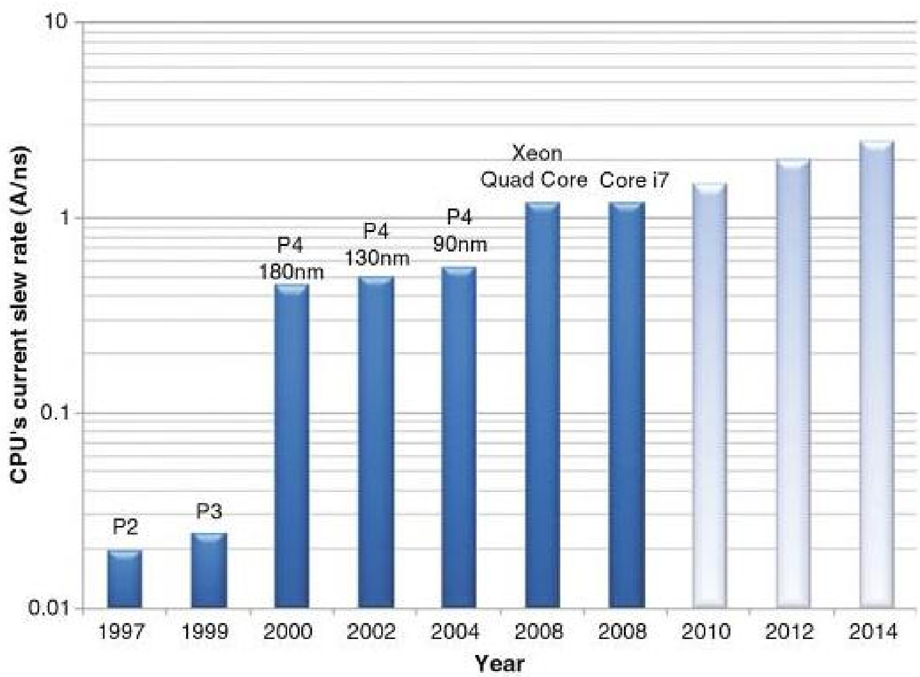

Figure 1.4: Trend of processor's current slew rate measured at the package pin [3]

The industry is trying to catch up with the high current slew rate of the processor current load by developing voltage regulator with high switching frequency. However, as mentioned in section 1.2, the switching frequency range for voltage regulator is limited in order to preserve the efficiency and stability. The other design solution to address the high current slew rate is to design with huge number of output capacitors. Unfortunately, design with too many output capacitors will increase the product cost and consume huge amount of board area. This is not a favorable solution for mobile segment. As a result, this situation poses a great challenge to the voltage regulator designer.

1.4 Problem Statement

Fast transient voltage regulator is very much needed to address droop and overshoot caused by the high current slew rate of the processor. Increasing the switching frequency of the voltage regulator is a way to improve the transient response. However, on-board voltage regulator has limited switching frequency range. Besides, too high of a switching frequency will result in poor efficiency. Hence, this situation challenges the voltage regulator design to optimize both the switching frequency and efficiency at the same time.

Secondly, size of the voltage regulator has always been too huge driven by increasing power demand of the mobile processor. This renders the overall mobile computing product to be heavy, bulky, costly, and unattractive. With AVP feature introduced, now the voltage regulator designer has the option to design with all ceramic output capacitors in order to present an area and cost effective solution. However, design with all ceramic output capacitors requires thorough analysis and engineering judgment so that the solution presented is stable and meets the design specifications.