A Development of Thin Films and Laser Processes for Patterning of Textured Silicon Solar Cells

by

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ABSTRACT

This work explores the application and optimization of laser patterning of dielectrics on textured crystalline silicon for improving the performance of industrial silicon solar cells. Current direct laser patterning processes introduce defects to the surface of the solar cell as a result of the film transparency and the intensity variation of the laser induced by the textured surface. As a means of overcoming these challenges, a co-deposited protective masking film was developed that is directly patterned with laser light at greatly depreciated light intensities that allows for selective chemical etching of the underlying dielectric films without incurring substantial defects to the surface of the device. Initial defects produced by the process are carefully evaluated with electron microscopy techniques and their mechanism for generation is identified and compensated. Further, an analysis of the opening fraction within the laser spot is evaluated –the area of removed film within the laser spot divided by the area of the laser spot– and residue produced by the laser process within the contact opening is studied. Once identified, this non-damaging laser process is a promising alternative to the standard screen print and fire process currently used by industry for metallization of silicon solar cells. Smaller contacts may be made with the laser process that are as of yet unattainable with screen printing, allowing for a decrease in shading losses. Additionally, the use of patterning allows for silver-free metallization and improved conductivity in the contacts, thereby decreasing parasitic losses in the device.

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CHAPTER 1

INTRODUCTION

a) Solar Power Production

A basic component for the improvement of the quality of life of an individual is a reliable and consistent source of energy. Pasten *et. al* link the quality of life to the available energy generated per capita[1]. While increasing the energy generation of a given region is important and worthwhile, it is also important to consider the accessibility of that energy to the general public. The World Health Organization (WHO) estimated in 2009 that 1.5 billion people do not have access to electricity, the vast majority of which live in developing countries[2]. Solar power has the potential to sustainably increase the accessibility of electricity for the general public in these regions. Most notably, regions like sub-Saharan Africa which have a high population of individuals without access to electricity (560 million), excellent solar insolation[3], and water scarcity[4] could benefit from photovoltaics, which requires little to no water consumption.

Solar energy is typically divided into two major categories, solar thermal and photovoltaics. Solar thermal uses light to generate heat, uses that heat to generate steam, and then uses that steam to turn turbines that generate electricity. A major disadvantage of this system is the need for a constant water supply, even though it does not have to be biologically compatible water.

Photovoltaics, once produced, require little to no water to support plant operation. The system directly converts photons (light) into a direct current (DC). It does so by using photons to stimulate electrons from the valence band, to the conduction band, across a band-gap. This requires that the material used for the photovoltaic effect –in this

case, silicon– to have a bandgap smaller than the photons being absorbed. Photons with an excess of energy above the bandgap of the material generate electrons, but also lose energy in the thermalization of those photons. Photons with energy less than the bandgap, simply pass through the material. The loss of energy in a photovoltaic system from thermalization can be reduced by using multiple materials, but requires the use of rare earth elements and more expensive fabrication equipment.

Typically the DC power supplied by this system is converted by an inverter to alternating current (AC) for grid compatibility, and transmitted along an infrastructure at high voltages to minimize power loss.

b) Motivation

For decades the integrated chip industry has developed the infrastructure and technology to mass produce high quality silicon. Analysis of the optimal bandgap for a solar cell using the Shockley-Queisser limit and assuming radiative emission from the front and rear of the cell, we find that the bandgap (E_G) of Si (1.1 eV) can reach a maximum efficiency of 32%. This compared to the optimal calculated bandgap of 1.4 eV with a maximum efficiency of 33% places Si in an ideal position for solar production[5,6]. Although technologies exist with bandgaps closer to the ideal –such as InP, GaAs, CdTe, Pervoskites, and die-sensitized solar cells– none are as readily available and cheaply manufactured as Si.

A major drawback of the current technology is the consumption of silver in the front-grid paste of the solar cell. In 2016 the price of silver varied between $0.50 and $0.73 per gram while the price of copper is $0.0057. The International Technology Roadmap for Photovoltaics (ITRPV) of 2016 specifies an average silver usage in 156 mm

x 156 mm solar cells to be 100 mg in 2016 and anticipates a reduction down to 40 mg by 2026[7–9].

Considering the volatility of the cost of silver and the fixed production of silver per year, it is desirable to find an alternate metallization that does not rely on precious metals for the growing solar industry. We explore a process that can be applied to very fine and precise metallization of contacts with Ni, Cu, and Sn. Feature sizes down to 10 μm can be produced with minimal to no damage to the surface of a textured substrate.

c) Passivated Emitter Aluminum Back Surface Field

Silicon solar cells with aluminum back surface field (Al-BSF) currently dominate solar cell production and the laser process in this thesis is initially applied to these types of cells. The process described here is a typical production process and also used to fabricate cells in this thesis. After an organic clean to remove packaging residue, as cut p-type wafers were put through saw damage removal. Saw damage removal is a process that is necessary to remove the lattice damage created by the dicing saw that is used to cut wafers from the boule; it typically consists of concentrated KOH at ~80 °C to etch roughly six microns on each side of the substrate. Once the surface has gone through some damage removal, texturing is used to roughen the surface of the substrate to reduce the surface reflection of light [10]. Pyramid sizes with this particular implementation are roughly 400 nm to 5 microns in size, but, depending on the optimization and processing conditions, pyramid sizes may vary up to and above 15 microns in size.

Figure 1.1 shows a typical uniform texturing result. There is a distribution of pyramid sizes that are pseudo-uniformly distributed across the entire surface of the

substrate, such that the reflection of the substrate remains roughly constant as a function of position.

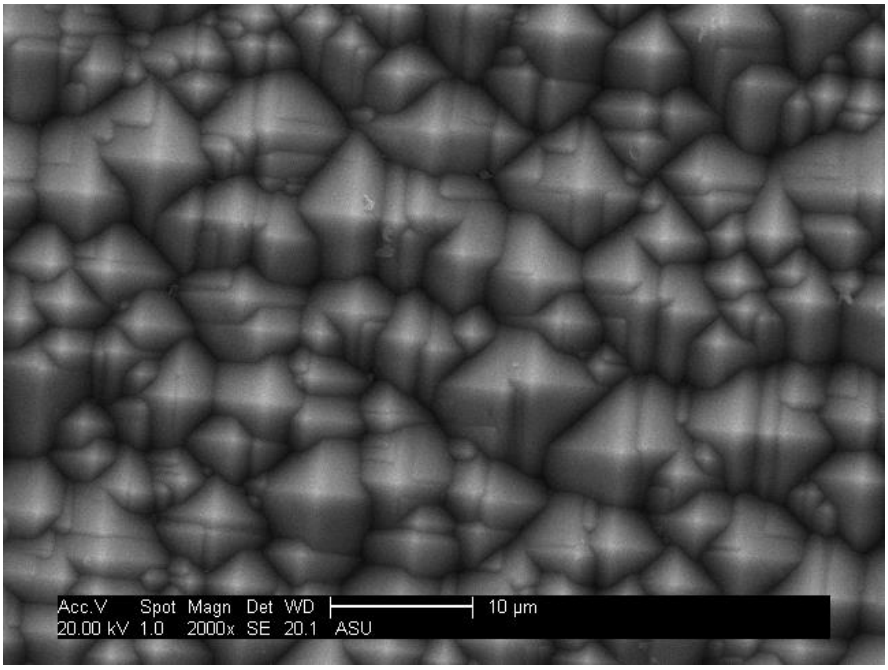

Figure 1.1: SEM Image of a Wafer after Saw Damage Removal and Texturing.

Non-uniform texturing can result depending on the temperature of the bath, duration of texturing, initial surface topography of the substrate, presence of organic contaminants on the substrate, and the chemistry of the bath. Evaporation of texturing agents during the etch process can lead to non-uniform texturing. For example, the density and shape of pyramidal structures is dependent on the concentration of isopropyl alcohol[11] for one such etch and would be grossly effected by a change in bath chemistry during processing. An important consideration during the process is the quality of the cassette used for acid processing as high temperature, concentrated KOH can degrade even chemical grade PVDF. Alternate, non-degrading plastics such as PFA or PTFE can avoid this issue. After texturing a standard metal ion clean with RCA-B (mixture of hydrochloric acid, hydrogen

peroxide, and water) is usually performed, and may or may not be followed by an organic clean to remove residual contaminants.

Once the wafer is textured and cleaned the approach for forming an emitter in the p-type substrate can vary depending on the manufacturer. Usually a CVD phosphosilicate glass (PSG) is formed in a tube furnace and used as a dopant source for phosphorous atoms, which behave as an n-type dopant in silicon[12–15]. If a backside oxide is deposited on one side of the wafer with a sufficient thickness then the subsequent diffusion process only occurs on the front-side of the wafer, resulting in a single sided diffusion as seen in figure 1.2 (a). Without a blocking oxide, diffusion occurs on both sides of the substrate, including the edges. The wrap-around diffusion necessitates either some form of edge isolation or etch back to remove the shunting diffusions. Edge isolation removes the shunt by removing a sufficiently large region of the wrap-around diffusion to restore a high shunt resistance (R_{SHUNT}), and this is performed chemically or with a laser as shown in figure 1.2 (b). Edge isolation can occur on the side, front, and/or the backside of the substrate, as long as the circuit connecting the front and backsides of the substrate is interrupted[16]. Etch back removes the entirety of the rear diffusion by using a single sided etch[17], alleviating the issue of shunting and allowing for a more desirable rear field.

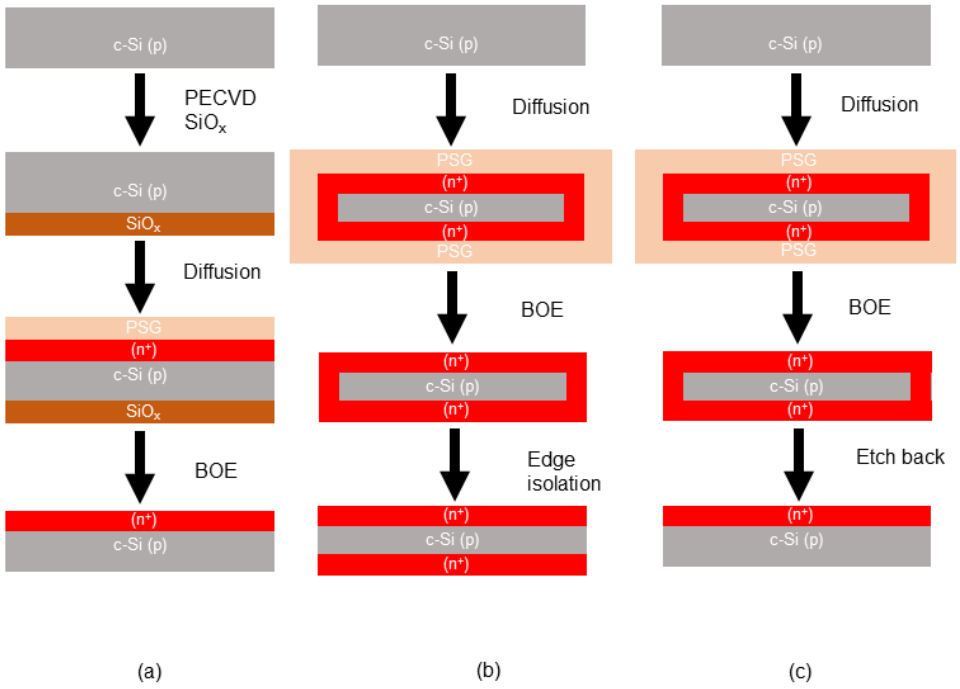

Figure 1.2: Varied Wafer Process Flows for Forming Pn-junctions (a) Use of a Blocking Oxide with PECVD, (B) Edge Isolation to Remove Edge Shunting, (C) Substrate Etch Back to Alleviate Shunting, Images Are Not to Scale.

While processes (a) and (c) in figure 1.2 result in a single sided junction, they do require a slightly more complex process than in (b). The PECVD SiO_x in (b) requires the use of PECVD which may be prohibitively expensive. The etch back process in (c) can be achieved through various processing schemes such as a single sided etching with a specialized tool and double sided etching with a protective front film[17]. The additional process steps involved with protective front films typically incur too much cost and the specialized single sided etching tool may also be expensive. While the process in (b) has the potential to be cheap compared to processes (a) and (c) it leaves a residual c-Si(n^+) field which will inevitably cause some small voltage drop across the junction when metallized, thereby reducing the performance of the solar cell.

Following the formation of the emitter and the removal of the phosphosilicate glass (PSG), films are either grown or deposited on the front of the substrate to electrically passivate the emitter and serve as an anti-reflection coating to enhance light trapping[12,18]. The state of the front surface has a large influence on the ability of silicon nitride (SiN_x), thermal silicon dioxide (SiO_2), and other passivating films' ability to tie dangling bonds and reduce surface recombination. The higher the surface concentration of phosphorous in the emitter, the higher the surface recombination velocity of the emitter and the poorer the general performance of the cell [12,14,15,18].

Once the front surface of the substrate is passivated, metallization is necessary to extract current from the device. The rear-side of the cell is metallized with screen printed aluminum that creates an aluminum silicide, thereby generating a back-surface field (BSF). Film thickness, firing temperature, and firing time are all important factors that need to be controlled to ensure proper BSF formation while avoiding bubbling or peeling[19,20]. The front-side of the solar cell is usually metallized with a silver-based paste with lead frit that allows the paste to fire through the non-conducting SiN_x. The temperature profile of the firing has a large impact on the formation of proper contact of the front grid. Too cold and short of a firing process and the paste will not completely burn through the SiN_x and fail to make ohmic contact with the emitter. Too hot and long of a firing process may cause the front paste to fire through the emitter and shunt the front and back sides of the solar cell.

While the rear Al paste can form a doped aluminum silicide region that allows for excellent ohmic contact, the Ag front grid paste does not. In order to achieve ohmic contact with the front contact metal the emitter must have a sufficiently high dopant concentration to prevent the establishment of Schottky diode behavior on the front surface. Modern pastes

incorporate a more complex chemistry that allows for the formation of an interfacial glass, enabling ohmic contact to much lower surface concentrations[14]. By using a depreciated surface concentration, assuming a properly designed grid, it is possible to improve the performance of the solar cell[12].

Once the solar cell is fully metalized, the architecture of the Al-BSF structure looks similar to figure 1.3.

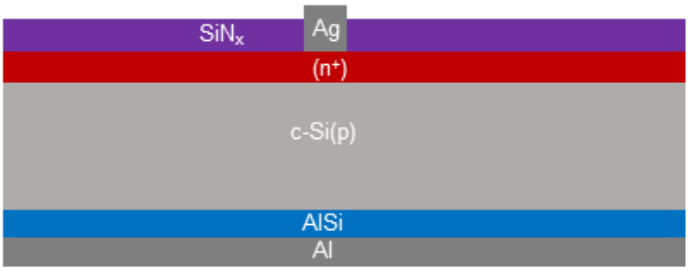

Figure 1.3: Typical Architecture for an Al-BSF Solar Cell, Image Is Not to Scale.

Presuming proper surface passivation of the front with SiN_x, ohmic contact with the front grid paste, proper Al-BSF formation, and bulk lifetime in excess of ~70 µs, solar cells with an efficiency over 19% have been achieved in industrial production[12,14].

Al-BSF solar cells produced in this work use the process defined in figure 1.2(a). Substrates are 156 x 156 mm^2, pseudo square, monocrystalline, boron doped, as-cut wafers with a bulk resistivity of 1-3 Ω·cm. Following PSG removal, samples are put through an oxidation process to grow ~12 nm of thermal oxide. The process reduces the surface concentration of phosphorous and improves passivation of the subsequent SiN_x deposition.

d) Passivated Emitter Rear-Contacted cells

Improvements beyond an efficiency of ~19.5% with a Si diffused junction cell requires a slightly more advanced structure. Once the emitter and its passivation have

been optimized, the bulk lifetime and rear surface of the solar cell must be considered. Even with optimization a fully metallized Al-BSF will have a higher surface recombination velocity than a properly passivated emitter and so limit the device performance.

One possible solution to improving the performance of the rear-side is to passivate the base with thin films and locally remove those films to subsequently permit formation of a local Al-BSF. This would allow for a complete Al rear-reflector, improved general surface quality, and local contact with an aluminum silicide. Figure 1.4 details a possible, albeit non-ideal structure for a passivated emitter rear-contacted (PERC) cell. The PERC structure is investigated to take advantage of the benefits provided by the laser processing developed in the course of this study.

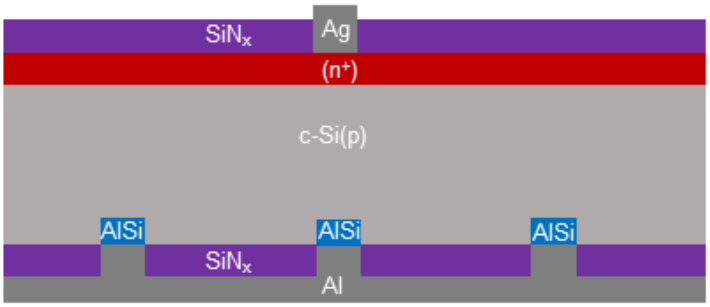

Figure 1.4: Representative Architecture for a PERC Solar Cell; Thin Films Are Used to Passivate the Rear Side and Locally Opened to Make Contact with Al Contact

The local contact opening in the SiN_x allows for the Al to make contact to the base; however the positive charges associated with SiN_x make it a less-than-ideal surface passivant for p-type regions. The positive charges attract negative charges in the substrate, and lead to a weak depletion of the surface thereby increasing the population of minority carriers and enhancing recombination. A strategy for mitigating this issue is to introduce a

thermal oxidation step before the SiN_x deposition and grow a passivating oxide on the front and rear side of the substrate. Thermal oxide has the potential to passivate both boron and phosphorous regions, without introducing deleterious depletion affects. Figure 1.5 details the new solar cell architecture.

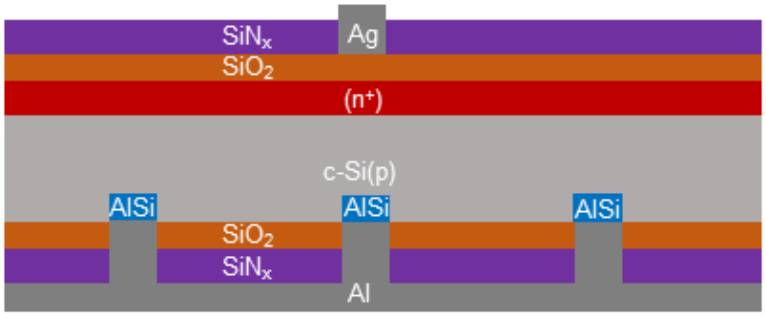

Figure 1.5: PERC Solar Cell with Thermal SiO_2 and Sinx Passivation; The SiO_2 Serves to Improve the Passivation of Both the Front and Backside of the Substrate

The SiO_2/SiN_x stack serves to passivate the front and back-sides of the substrate, but it isn't necessarily the best choice for passivating films. Atomic layer deposition (ALD) of Al_2O_3 has the potential to accumulate the base and have better passivation than SiO_2[21].

Of course, the front-side SiN_x will have to be adjusted in film thickness to account for the introduction of a thin SiO_2 layer in order to maintain good anti-reflective properties. The rear-side films should be thicker, on the scale of >100 nm to improve the rear-side reflection. Aluminum has parasitic absorption of infra-red light which negatively impacts the generation current in the substrate[22].

An important considerations to this structure involve the proper formation of the Al-BSF at the local contact openings. The width, pitch, Al thickness, and silicon content in the Al paste all have an impact on this optimization.

CHAPTER 2

EQUIPMENT AND EXPERIMENTAL METHODS

a) Plasma Enhanced Chemical Vapor Deposition

The thin dielectric film used in this thesis are deposited with the Plasma Enhanced Chemical Vapor Deposition (PECVD) system in the Solar Power Laboratory is a modified Precision 5000 (P-5000) tool from Applied Materials. The tool form factor was adjusted from eight inch round substrates to 156 mm square substrates. The P-5000 is equipped with an external cassette capacity of 26 substrates and an internal vacuum load-lock capacity of eight substrates. The three vacuum chambers are equipped with independent vacuum pumps, 13.56 MHz RF generators with a power capacity of 1.2 KW, and independent gas control. Chambers A, B, and C are all capable of depositing silicon nitride (SiN_x) and hydrogenated amorphous silicon (a-Si:H). Chambers B and C are also have the capacity to dope films with phosphorous or boron, respectively. Chamber A is the sole chamber capable of deposition silicon oxide (SiO_x).

Gas flows in the chambers are controlled by mass flow controllers and the tool pressure is monitored and controlled by a gas pressure sensor coupled with a butterfly valve. Typical operation regimes for film depositions are between 1.5 and 4 Torr. All residual gases are pumped through a Catalytic Decomposition and Oxidation burn-box (CDO). Substrate temperature is inferred from the susceptor temperature, which is monitored with a thermocouple beneath the susceptor. The susceptor is heated with a series of quartz lamps positioned beneath the susceptor. Substrate positioning and removal is handled with a robotic arm and ceramic substrate lift pins. Showerhead-to-

substrate distance is controlled by adjusting the susceptor gap to account for the substrate height.

Film thickness is inferred by measuring the deposition rate on a polished substrate for a given recipe with ellipsometry. Deposition rate variability is monitored by a weekly statistical process control with a series of standardized SiN_x recipes in all three chambers. On textured substrates, a decreased deposition rate with a dividing factor of 1.5 is assumed. This factor was experimentally determined with cross sectional Scanning Electron Microscopy (SEM) and approximates the effect of the increased surface area of an alkaline textured substrate.

Deposition occurs on substrates placed between the two capacitively coupled parallel plates, the gas showerhead and the substrate susceptor. The radio frequency plasma established between the showerhead and the dielectric coated susceptor ionizes gases flowing from the showerhead. Positive ions in the plasma are attracted to the grounded susceptor and arrive at the surface of the substrate on top of the susceptor, resulting in the formation of a network of ions that re-assemble themselves into the desired films, based on the precursor gases, deposition pressure, flow rates, power, substrate temperature, and power density of the deposition.

Deposited films are developed by depositing them on polished 6" crystalline silicon substrates and characterized with variable angle spectral ellipsometry as discussed below.

For this work PECVD is used to deposit the blocking oxide (SiO_x) on 156 x 156 mm^2 pseudo square p-type substrates to prevent backside diffusion (further detailed in the

diffusion furnace section), anti-reflection coating and passivating film SiN_x on the n-type emitter, and an a-Si:H etch mask.

b) Diffusion Furnace

Substrates are placed in a quartz boat and placed on a mobile paddle that travels horizontally into the MRL Furnace. Once the boat is fully placed in the tube a series of temperature ramps and stabilization steps are performed in an inert (N_2) atmosphere (pre-deposition) to reach the desired phosphosilicate glass (PSG) formation temperature (deposition/growth). Once the desired temperature has been reached, O_2 and $N_{2carrier}$ gasses are flowed into the tube. The $N_{2carrier}$ gas is bubbled through a vial containing phosphoric acid (H_3PO_4) at a controlled temperature of 30° C. The number of substrates, surface area of the exposed silicon, and location of the substrates on the paddle all have an effect on the diffusion process. An increase in the exposed Si surface area will decrease the amount of available phosphorous for each wafer and require an increase in either the bubbler temperature or the amount of $N_{2carrier}$ gas to maintain a similar diffusion profile and sheet resistance. A decrease in the exposed Si surface area has the opposite effect, requiring a complementary decrease in the bubbler temperature or the quantity of $N_{2carrier}$ gas. Additionally, the lattice orientation, surface morphology, and physical shape of the substrate have an impact on the diffusion process. Profiling of the diffusion requires polished substrates, which are distinctly different than the textured substrates we use to create solar cells. Additionally, readily available polished p-type substrates are cut along the <100> plane, while our textured substrates have exposed <111> planes from the alkaline texturing process. Given these differences the characterized profile of the

diffusions will vary slightly from the actual diffusion in our solar cells, but will exhibit the same trends seen in the characterized emitters.

Substrates used for solar cells have a PECVD deposited blocking oxide on the back to prevent side and rear-sided diffusions. Following the diffusion furnace pre-deposition and deposition steps, the substrate is removed and the thin films are removed with a buffered oxide etch (BOE). Following the etch-back the substrates are placed in an oxidation tube to grow a passivating oxide and drive in the existing dopant from the preceding diffusion process. Figure 2.1 depicts the diffusion process as described, below.

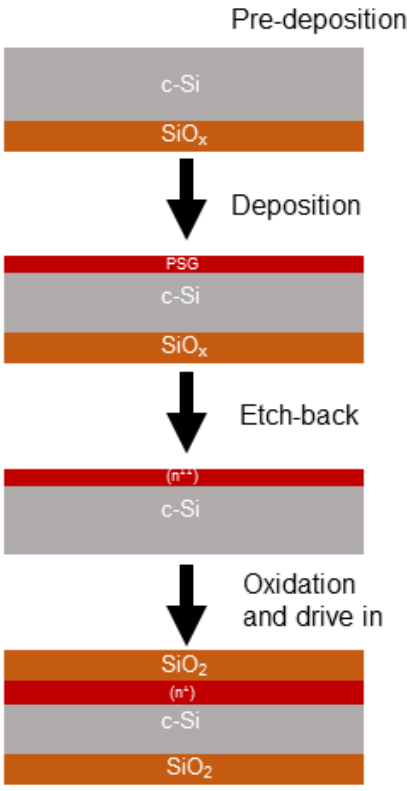

Figure 2.1: Diffusion and Oxidation of Substrates, the SiO_x Film Is Deposited with PECVD, the PSG Is Formed with High Temperature Chemical Vapor Deposition (CVD), and the SiO_2 Is Formed Thermally with the MRL Oxidation Furnace.

The oxidation process decreases the surface concentration and increases the junction depth. By using a two-step diffusion process we gain more control over the depth and surface concentration of phosphorous in the emitter.

The diffusion of phosphorous in silicon is a vacancy dominated process, with effects from field enhancement, inter-atomic strain, and interstitial diffusion. The diffusion profile has three distinct regions: a high concentration region where the magnitude of phosphorous exceeds the free carrier concentration, a precipitous drop known as the 'kink', and a tail region of enhanced diffusivity. In the high concentration region of the diffusion —where the phosphorous concentration exceeds the surface concentration of electrons n_s— a portion of the P^+ ions pair with $V^=$ vacancies to form $P^+V^=$ .The kink in the profile occurs when the dissociation of $P^+V^=$ pairs into P^+V^- pairs with a residual electron (e^-) when the fermi level sits 0.11 eV below the conduction band. Surface concentrations below 10^{19} cm^{-3} are believed to be primarily due to phosphorous atoms exchanging with neutral vacancies [23].

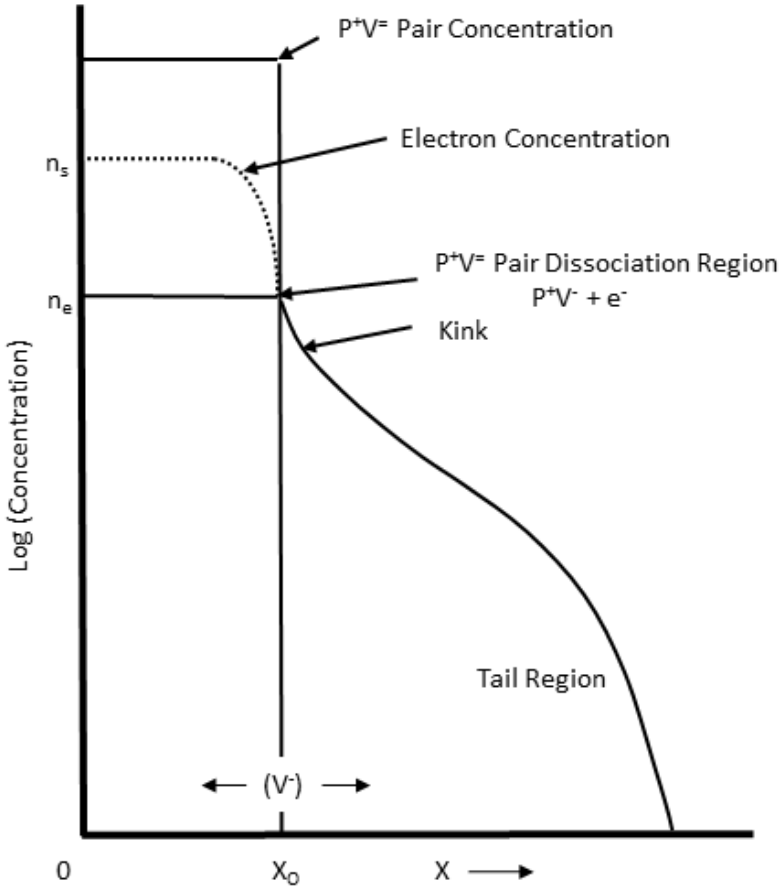

Figure 2.2: 7. Theoretical Phosphorous Diffusion Profile in Silicon. P+V= Pairs Dominate in the First Region of the Curve, P+V- Pairs Begin to Dominate Where the Electron Concentration (N) Meets the Second Acceptor Level of V= (N = Ne) . This Causes an Enhancement in the Diffusion Coefficient, Resulting in the Kink, Graph Adopted from Fair et al. [23].

Effects from the background doping level, strain from an excess of defect atoms, the quality of the crystal, and oxidation enhanced diffusion play a role in the shape of the diffusion profile, and are discussed in detail in [23].

c) Ellipsometry

In the present study, ellipsometry was employed for determining the properties of thin films on polished crystalline silicon. A collimated beam of polarized light is reflected off of the surface of the coated substrate at some incident angle, and the intensity, phase shift, and change in polarization are measured. The interaction of the film with the vertical and horizontal components of the light lead to an elliptic shift in the properties of the light, dependent on the extinction coefficient, index of refraction, and thickness of the films. By varying the wavelength of the incident light and the angle of incidence, a unique fit can be found for the film parameters yielding a reasonably accurate approximation of the film properties[24].

d) Femtosecond Laser

The Innolas 700-P is a femtosecond laser system that was used for patterning of the substrates. The system uses a set of flying optics that allows for rapid scanning in X and Y directions and slower scanning in the Z direction. The nature of a flying optics system lends itself well to the use of high numerical aperture optics that allow for small spot sizes while maintaining optical focus on the surface of the substrate, despite the decreased depth of field with increasing numerical aperture.

A machine vision alignment system with edge detection and fiducial recognition allows for micron level alignment in the patterning process, which would allow for multi-step patterning with the tool. The initial coarse alignment uses backlit edge detection of the substrates with overhead cameras and basic image processing to calculate 2-4 corner alignment. A more precise alignment may be done following the initial alignment with

the camera mounted on the laser head if alignment crosshairs have been patterned on the substrate.

The laser itself is an 800 nm 140 femtosecond pulsed laser with a pulse repetition rate up to 10 kHz. The system is comprised of a diode-pumped, frequency doubled YAG laser with a 532 nm 100-150 nanosecond pulse. The nanosecond pulses are guided into the femtosecond laser cavity and passive mode locked with an 800 nm seed using a Ti-sapphire crystal to facilitate lasing.

Sufficient absorption of the laser results in a plasma based ablation, with limited thermal effects. This particular ablation arises from the generation of energetic electron hole pairs with sufficient energy to cause impact ionization. The energetic electrons arise from multi-photonic absorption, a phenomena that is unique to lasers with very high intensities. The multi-photonic absorption that occurs with this type of laser allows for non-linear absorption in transparent materials and enables the use of the laser for ablation of wide-bandgap semiconductors well in excess of the 1.55 eV photons coming from the laser.

Initially this tool was used to directly ablate the passivating films on the front side of the solar cell, to expose the underlying emitter. However, investigation of the surface quality showed no direct-absorption of the laser in the SiN_x and a large amount of damage to the surface. Later work focused on using an absorbing etch mask of a-Si:H to absorb the laser, and allow for the development of an indirect patterning process. The details of absorption of this laser in both films is detailed in section 3.2(a).

e) Sinton Lifetime Tester

The Sinton Lifetime Flash Tester is used for determining the lifetime of electron-hole pairs in the substrate. The tester uses either a transient or a quasi-steady state photoconductance measurement. This measurement is enabled by using a circular inductor beneath the substrate that measures the change in conductance of the substrate as a result of the excess carriers generated during the flash. The change in conductance is proportional to the change in the excess carriers in the substrate, and as such gives an estimation of the lifetime of these excess carriers in the substrate as a function of the injection level. In this work, we estimate the effective minority carrier lifetime of our substrates at an injection level of 10^{15} cm^{-3}.

f) Light-Induced Plating

The plating equipment in the lab incorporates a single-sided immersion of our backside Al screen printed p-type diffused substrates. The Al contact is grounded with a power supply while the current flow is monitored. The solution is circulated and agitated at the front of the substrate to prevent depletion of the solutions additives and nickel content. Once illuminated by the 532 nm LEDs in below the solution, accumulation of the metal at the exposed c-Si sites begins. While the exact mechanisms of this complex chemical reaction are still under investigation, it is widely accepted that the potential difference between the semiconductor and the solution disassociates the nickel ions from the solution and causes their accumulation at the surface of the device. The rate at which this deposition occurs can be controlled via the illumination intensity and the power supply grounding the Al back contact.

Al-BSF samples that have a front-grid laser patterned with the indirect patterning process described in 3 b) are printed with a backside Al contact and fired. After a short HF dip the samples are then placed into the LIP system for front-side metallization stacks.

g) Illuminated Lock in Thermography

Illuminated lock in thermography uses thermal imaging of an illuminated solar cell to measure shunting in the device. Locations where the emitter is shunted cause local increases in current flow and subsequently generate hot spots in thermal imaging. Areas where screen printing has fired too deeply or where nickel silicide has migrated into the space-charge region of the PN junction exhibit these shunt-like characteristics, and are readily characterized by this device. The shunts that can form from the nickel silicide may be precipitated by the patterning process used to expose the c-Si surface beneath SiO_2 and SiN_x film stacks.

Steady state illumination and thermal imaging is limited to the detection of major shunts, while minor shunts are much more difficult to detect. This limitation is set by the overall sensitivity of the IR camera and the magnitude of background noise from the surroundings. By incorporating pulsed light, a lock-in amplifier allows the system to detect more subtle thermal variations that would otherwise be obscured by background noise. The increased sensitivity of this implementation improves the detection threshold of the system by a factor of 100-1000.

h) Scanning Electron Microscopy

Energetic electrons are generated and accelerated at the sample with an energy typically in the range of 1-20 keV. These electrons interact with the sample in a variety of

ways. Backscattered electrons are reflected from the sample with a sensitivity to the density of the material, Auger electrons are generated in the top ~1 nm of the sample, secondary electrons are emitted from the top 10 nm of the sample surface, and x-rays are generated with an energy spectra sensitive to the material (allowing for material characterization)[24,25]. For our purposes, we image the secondary electrons as they have a good sensitivity to the surface topography of the sample.

Due to the extremely short effective wavelength of energetic electrons compared to visible light, a high numerical aperture is not necessary for high magnification. As a result, high magnification and a good depth of field may be achieved simultaneously. This makes Scanning Electron Microscopy (SEM) a great tool for imaging features anywhere from tens of nanometers to tens of microns. When inspecting alkaline textured silicon, features ranged in size from hundreds of nanometers to approximately twenty microns.

A challenge associated with this technique is the need for a relatively conductive surface. Non-conducting surfaces will charge as they are hit with the electron beam necessary for generating an image. The charged surface then moves the electron beam away from the target area and causes image drift. There are multiple possible solutions including coating the surface with a thin conducting layer of metal, but an equilibrium of charging and discharging may be reached by decreasing the accelerating voltage of the SEM. By using an operation range of 1-4 keV it is possible to image non-conducting alkaline textured silicon surfaces with an SEM. We used a 3 keV beam to image laser ablated silicon nitride (SiN_x) and used the residual charging seen as a means to determine

the quantity of residual films while still being able to see any defects that might be introduced into the surface by the lasing process.

i) Transmission Electron Microscopy

Energetic electrons are generated with a field emission gun or other source and are accelerated towards a substrate. Electrons are typically accelerated to the 100-400 keV range, yielding an effective wavelength even smaller than what is achievable with an SEM. As a result, the transmission electron microscope (TEM) is capable of extremely high resolutions approaching 0.8 angstroms[26].

Bright and dark field images can be collected from the transmitted and diffracted electrons, respectively. Additionally, high resolution microscopy can be used to observe the columnar formation of atoms in the sample and observe transitions between materials, as well as any amorphization that might occur during processing. Sample prep is often the weak point of TEM as the sample needs to yield samples ~10 nm thick in order for electrons to successfully pass through the sample. An insufficiently thinned sample will still yield high resolution images, but columnar formations from lattice fringing will not be observable.

We use this technique to analyze the nature of the defects generated by the laser under certain conditions. The condition of the lattice at the defect sites gives an insight into the mechanisms of the defect generation and possibly how to prevent them. Before TEM, the samples must be prepared with a focused ion-beam to mill a sample out of the substrate.

j) Focused Ion-Beam

While this technology was initially developed for chip modification and repair, it has been adopted into the semiconductor industry for analyzing various material properties. The precise control afforded by focused ion-beam (FIB) milling allows for the selection of defect sites and analysis of the depth of the defects, as well as the nature of those defects in the material. In c-Si, a sufficiently thinned sample prepared with FIB can be placed into TEM for lattice fringe imaging. Threading dislocations and amorphization from thermal or mechanical strain.

In this work, samples are prepared with in-situ lift-out where the region with the desired defects are protected with an electro-deposited Pt layer, ion-milled, and removed with a glass needle (see figure 4.2).

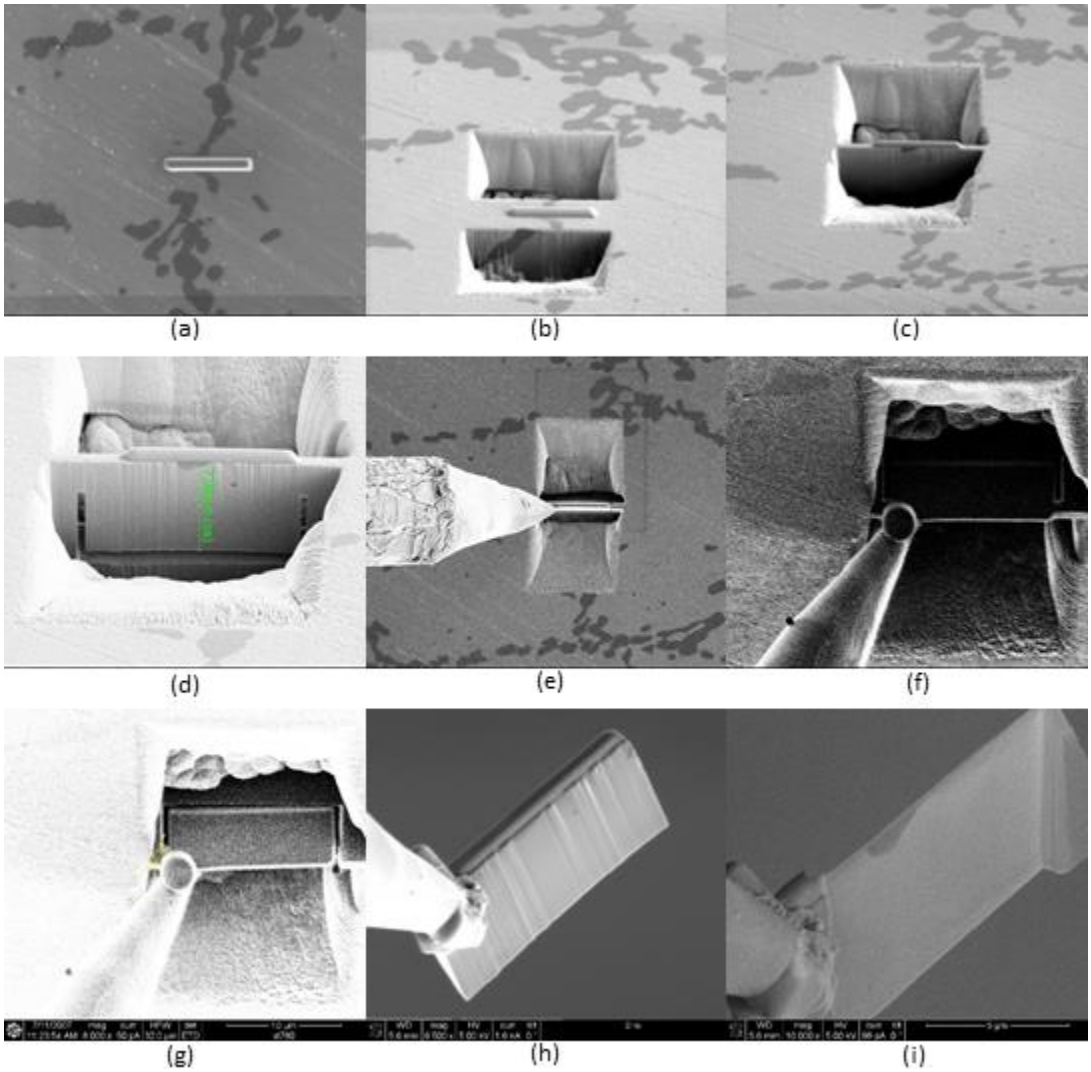

Figure 2.3: SEM Images of FIB Process Steps, (a) Pt Deposition from Vapor with an Electron Beam, (B) Coarse Ion Trench Milling Angled from the Substrate, (C) Sample Thinning with a Decreased Current, (D) Release Cuts Are Cut into the Sample at an Angle, (E) Probe Placed on the Sample, (F) Probe Welded to the Sample with Pt, (G) Final Cuts in the Sample Are Made, (H) Released Sample Is Re-positioned for Further Thinning, (I) Final Thinned Sample[27].

Once the voltage is reduced to 2 kV or lower, the sidewall damage induced in Si is low enough that sub-angstrom imaging is possible[28,29].

Even with careful preparation of the sample it is possible to induce defects in the sample of interest during the removal process. Effects of ion channeling can cause defects to propagate along a particular plane which can complicate the interpretation of TEM images aimed towards identifying pre-existing defects in a substrate.

Such an effect is observed in figure 4.4, region 5. Other considerations, such as the incorporation of Ga into the substrate, or the formation of intermetallic phases are also of concern. Work with this system will entail the analysis of Cu/Ni/Ni_xSi_y/Si stacks and eutectics, it is conceivable that such a layer will pose difficulties to the standard FIB process. Switching the predominant milling ion from Ga to Ar or other elements may be required to preserve the original structure. Further, the milling process has also shown a tendency to change grain sizes and intragrain boundaries of Cu which will certainly impact our film stack[28].

k) Spreading Resistance Analysis

Spreading Resistance Analysis (SRA) or Spreading Resistance Profiling (SRP) is a measurement technique initially used for lateral resistivity measurements to determine dopant concentration. The technique has excellent dynamic range allowing for characterization of ~10^{12} to 10^{21} cm^{-3}. When combined with a beveled surface as seen in figure 2.1, the technique can be used to generate a depth profile of active dopant.

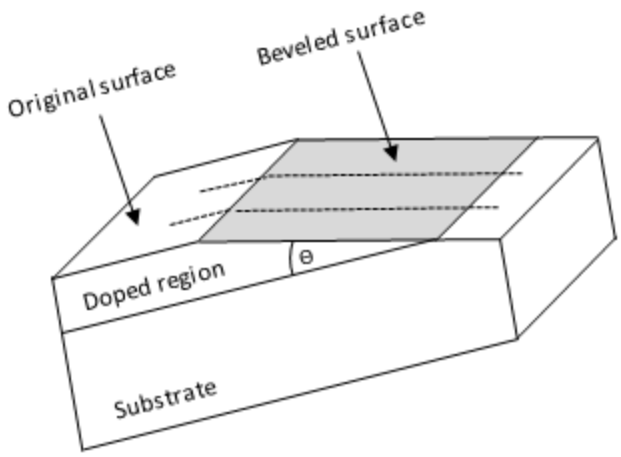

Figure 2.4: Example Beveled Sample Used for Spreading Resistance Analysis, the Dashed Lines Represent the Probe Paths Across the Surface [24].

Typically probes are kept 30-40 μm apart and 20-25 data points are taken per location. The measured resistance of this system is given by equation 2.1

$$R = 2 \cdot R_p + 2 \cdot R_c + 2 \cdot R_{sp} \quad (2.1)$$

where R_p is the probe resistance, R_c the contact resistance, and R_{sp} the spreading resistance [30]. The spreading resistance can be expressed as

$$R_{sp} = \frac{\rho}{2r} C \quad (2.2)$$

where ρ is the sample resistivity, *r* the spreading radius –which is not necessarily the physical radius of the probe–, and *C* is a correction factor that compensates for sample resistivity, probe radius, and current distribution [24].

A regularly calibrated and well compensated system that takes into account effects such as carrier spilling, depletion region width, and possible Schottky contact to the sample can achieve repeatability of ~10% [31]. It should be noted that this technique is sensitive to *active* dopant and insensitive to *inactive* dopant.

l) Four Point Probe

The Four-Point Probe (FPP) is an instrument used to measure semiconductor resistivities. This measurement technique allows for the de-coupling of the wire resistance (R_W) and contact resistance (R_C), allowing for a direct measurement of the resistance of the device-under-test (DUT). Figure 2.2 shows a circuit diagram of a two-point probe measurement in (a) and the FPP measurement in (b).

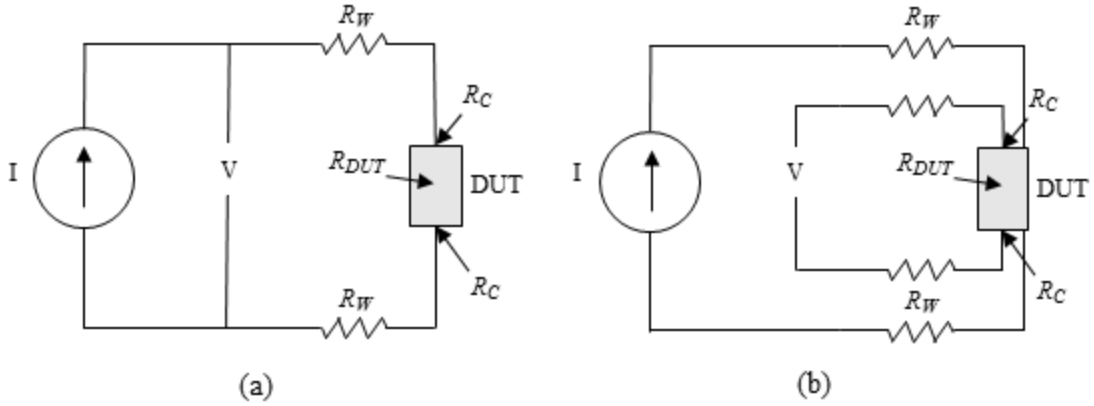

Figure 2.5: (a) Two Point Probe Measurement and (b) FPP Measurement [24].

By forcing a current on either side of the voltage probe measurement, we can simplify the expression for sheet resistance down to equation 2.3.

$$\rho = 2\pi s \frac{V}{I} \tag{2.3}$$

This equation assumes that the probe spacing is equal for all probes, a sample thinner than the probe spacing, and a probe area several times larger than the total probe width. Once the sample area becomes too small, edge effects being to dominate the measurement. If the sample is too thick, the vertical component of the spreading resistance begins to dominate and convolutes the lateral sheet resistance measurement. Correction factors can adjust for these effects, but may increase measurement error [24].

Coupled with SRA, this technique can give an approximation of the effect of varying parameters in the diffusion on the doping profile of the emitter. However, the probe measures the effect of the emitter as a whole, not the shape of the diffusion profile. Large changes to the diffusion process will require re-characterization of the process by SRA.

CHAPTER 3

DESIGN AND DEVELOPMENT OF LASER PATTERNING

a) Laser removal of thin films

Laser patterning of thin films such as hydrogenated amorphous silicon (a-Si:H), silicon nitride (SiN_x), and silicon oxide (SiO_x) is desirable for the production of silicon (Si) based solar cells. High fidelity patterning of these films is achievable with laser ablation and allows for improved metallization and selective doping [32–37].

Removing a wide-bandgap semiconductor (SiN_x) on top of a narrow-bandgap semiconductor (c-Si) is challenging. Wavelengths that are absorbed in the wide-bandgap material are more readily absorbed in the underlying narrow-bandgap material. This makes non-damaging removal of the SiN_x films on c-Si challenging. Short-wave lengths that are absorbed by SiN_x can be used to directly heat and ablate the film, but the high temperature may liquefy the underlying silicon. Long wavelengths not absorbed in the SiN_x may also be used to remove the film, but do so by delaminating it from the c-Si surface via c-Si damage. Both the directly absorbed short-wavelength laser and the long-wavelength laser can achieve surfaces with reasonable quality depending on the depth of diffusions and thermal profile of the laser.

Typically, silicon solar cells are not smooth or polished. Standard industrial solar cells are alkaline textured to reduce the reflectivity of their front surface; texturing while typically beneficial for the overall cell performance complicates the laser removal of thin films on top of it. The same lasers optimized for removing dielectrics on a smooth Si surface now have a propensity for inducing sub-surface defects that have deleterious effects on the device performance [38]. The large variation of laser intensity introduced

by the textured surface morphology introduces non-uniform ablation with defect rich regions. Knorz et al. demonstrated that laser intensity varied by as much as an order of magnitude for pyramidal structures between 5 and 10 μm [39]. Hernandez et al. correlated higher laser intensities to a decreased collection current and a decreased open circuit voltage (V_{OC}), suggesting that a wider variation of laser intensity will inherently cause increased degradation [32]. This degradation is attributable to non-uniform heating of the substrate and the generation of threading dislocations as deep as 1 μm[38].

The introduction of surface and threading defects negatively impacts the adhesion and pseudo-fill factor (*pFF*) of plated Ni/Cu contacts. The surface defects cause flaking of silicon –preventing good adhesion– and the threading dislocations enhance spike-through of nickel silicide through the emitter of the solar cell (thereby reducing the *pFF*) [35,40].

b) Direct Laser Ablation of Silicon Nitride with a femto-second laser

As-cut, p-type, mono-crystalline, boron-doped wafers with a bulk resistivity of 1-3 Ω·cm with an initial thickness of 200 $\pm$ 10 μm were cleaned and textured such that ~15 μm of material was removed from each side. This resulted in pyramidal formations ~0.4-6 μm in size. Film depositions were handled with an Applied Materials Precision 5000 PECVD tool. All film depositions were performed with the conditions listed in table 3.1.

Film (type)	Pressure (Torr)	Power Density (W/cm^2)	Temperature (°C)	SiH_4 /NH_4	SiH_4/ H_2
SiN_x	3.5	0.75	350	1	N/A
a-Si:H	3.2	0.15	300	N/A	0.2

Table 3.1: Deposition Conditions for Thin Films Deposited via PECVD [41]**.**

Film removal is accomplished with the femto-second laser previously described. The process flow for film removal is shown in figure 3.1.

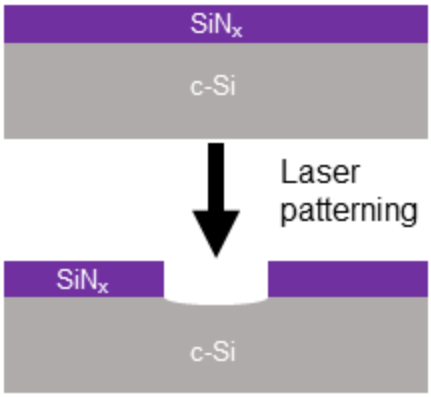

Figure 3.1: Direct Laser Ablation of SiNx on c-Si [41].

While this process flow is fairly typical for film removal, it is not standard to use a femto-second laser with an 800 nm wavelength. The wide bandgap SiN_x does not directly absorb the laser light as shown in figure 3.2.

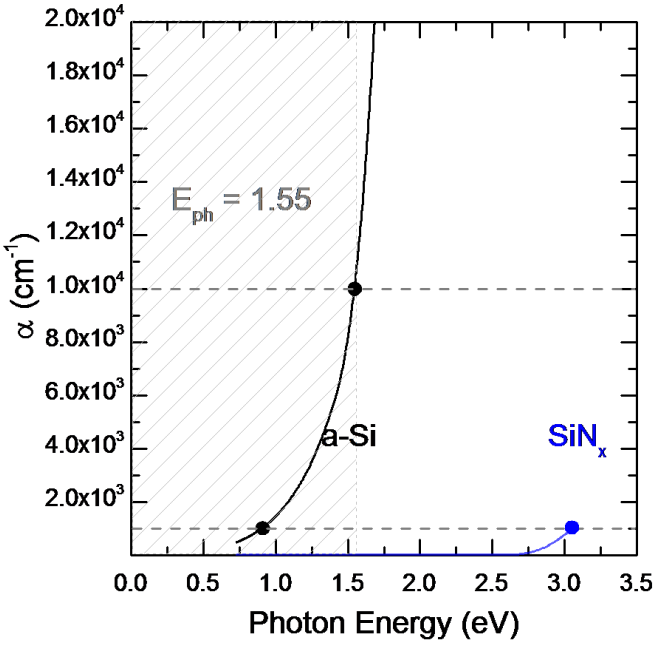

Figure 3.2: Absorption Coefficient as a Function of Photon Energy for a-Si:H and SiNx. The Grey Crosshatched Region Indicates the Bandgaps at Which the Laser Will

Be Directly Absorbed. The Horizontal Dashed Lines Show the Lower and Upper Limits (103 and 104 Respectively) for Empirical Determination of Bandgap as a Function of Absorption Coefficient [41], [42].

Given the transparency of the SiN_x and the absorbing nature of the underlying c-Si, the films here are removed via a lift-off process caused by the vaporization of the underlying c-Si substrate. On a smooth substrate this vaporization is shallow and uniform –making the process amicable towards solar cells with shallow emitters– but is non-uniform and damage intensive for textured surfaces. We empirically determined the bandgap of a-Si:H to be between 0.91 and 1.54 eV, whereas SiN_x has a bandgap equal to or greater than 3.06 eV. Figure 3.3 illustrates the effect of laser damage on smooth and textured surfaces. The number of shots listed in the image are indicative of the average number of pulses each location experiences; 5 shots corresponds to a laser overlap of 80%, 1.3 shots to 30%, and 1.2 shots to 20%.

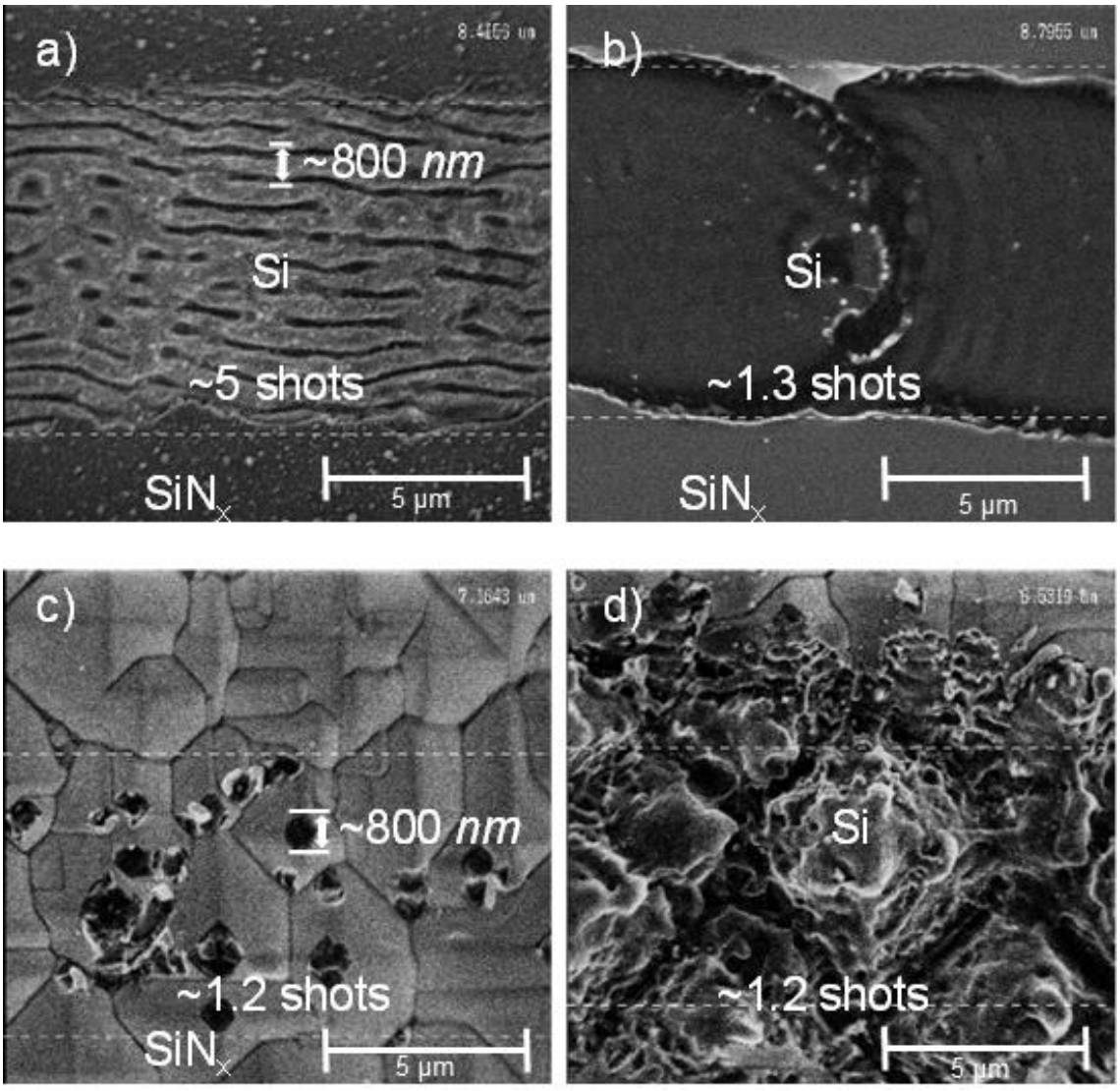

Figure 3.3: (a) SEM Image of Ablated SiNx on Smooth c-Si by the Femto-second Laser with an Average of ~5 Overlapping Pulses and Minimum Power for Ablation, (b) SEM of Ablated SiNx on Smooth c-Si with ~1.2 Overlapping Pulses and Minimum Power for Ablation, (c) SEM of Ablated SiNx on Textured c-Si with 1.2 Overlapping Pulses and Minimum Power for Partial Ablation, (d) SEM of Ablated SiNx on Textured c-Si with 1.2 Overlapping Pulses and Minimum Power for Full Ablation [41].

Due to the high intensity and short pulse duration of the femto-second laser, we calculated and report the instantaneous intensity of the pulses with Eq. (1). To do so, we assumed that the laser has a flat-top profile (thereby neglecting a 32% power variation within the full-width-half-max measured spot size).

$$P_d = \frac{P_{avg}}{(n * t_p * f)} \quad (1)$$

The laser intensity, P_d = 264 GW/cm^2 used for 3.3(a) was set for a minimum of power but required multiple pulses to achieve ablation and resulted in periodic trenching of the substrate at the photon wavelength. In 3.3(b) P_d was increased to 834 GW/cm^2 to improve the ablation while reducing the required number of pulses and resulted in far less trenching than seen in 3.3(a). The decreased damage from 3.3(b) compared to 3.3(a) is likely due to the increased explosive force with higher laser intensities; the increased vaporization of c-Si with a single pulse is more effective for promoting lift-off of SiN_x. Repeated small vaporizations in 3.3(a) will eventually lift off films, but require a larger volume of c-Si to be consumed, making the process undesirable. The introduction of texturing in 3.3(c) and 3.3(d) exacerbates the problem of damage; even partial ablation of the SiN_x with P_d = 834 GW/cm^2 in (c) shows significant pitting in the substrate's surface. The increased intensity of 1 TW/cm^2 required for the complete removal in (d) further increase the damage, indicating that sub-surface vaporization of c-Si for lift-off removal of transparent films on a textured surface is undesirable for any surface with a shallow diffusion or a need for a non-defective surface [41].

c) Indirect Laser Ablation of Dielectrics

Given the condition of the textured surface after the lift-off used in our direct ablation process, and the absorption properties of our thin films, we re-designed our process flow in figure 3.4.

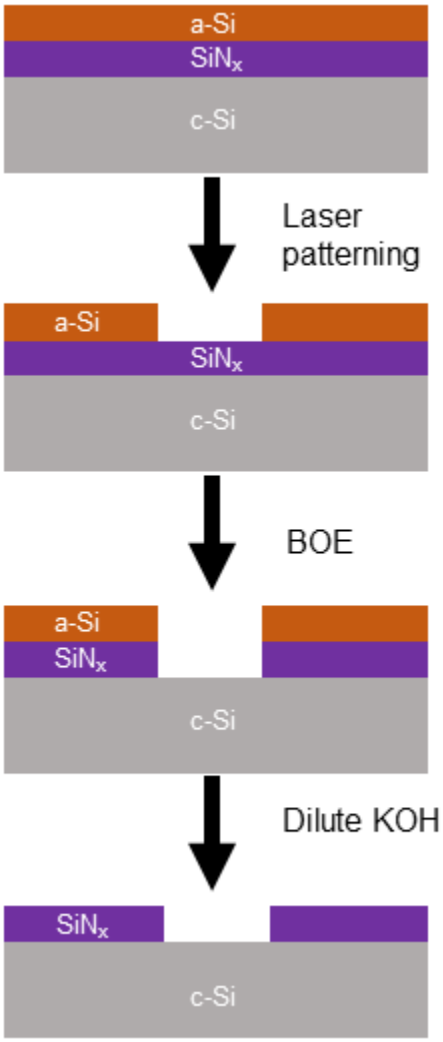

Figure 3.4: Indirect Laser Ablation of SiNx on c-Si Using an a-Si:H Mask, a Buffered Oxide Etch (BOE 10:1), and Dilute Room Temperature KOH (3%) [41].

From figure 3.2 we see that a-Si:H directly absorbs the 800 nm laser, so lift-off processes are not necessary for its removal. Vecchi *et al.* demonstrated that as the ratio of

NH_4/SiH_4 decreases, the etch rate in HF decreases and the etch rate in KOH increases [43]. This selectivity allows for the a-Si:H layer to absorb the laser and act as an easily-removable mask.

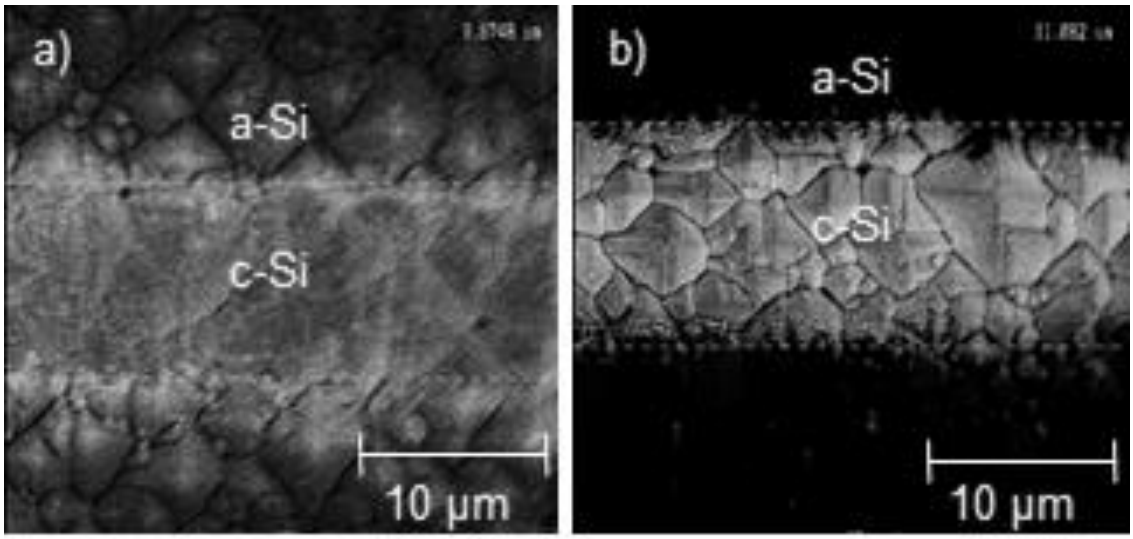

Figure 3.5: (a) SEM Image of Ablated a-Si:H on SiNx on a Textured Surface with Pd = 210 GW/cm^2, (b) SEM Image of Laser Ablated a-Si:H on Textured c-Si after 2 Minutes of BOE Etching [41].

The white distortion in 3.5(a) is due to the charging of SiN_x beneath the partially ablated layer of a-Si:H. After a 2 minute buffered oxide etch (BOE), the underlying non-conductive and amorphous SiN_x is removed, allowing for clearer imaging of the surface.

The a-Si:H mask in figure 3.5 was 5 nm thick, which proved insufficient to completely block etching pinholes into the SiN_x. When exposed to a light-induced plating process these pinholes resulted in ghost plating –deposition/growth of metal in non-contact areas– which reduces the contacts conductivity and increases shading [44–46].

d) Process Optimization

Al-BSF cells made in the fashion depicted in figure 1.2 (a) were made using 156 x 156 mm^2 pseudo square p-type substrates with a bulk resistivity of 1-3 Ω·cm and a front-side phosphorous doped emitter with a sheet resistance of 60 Ω/□. After emitter formation, the cell was coated with the SiN_x specified in table 3.1 followed by a subsequent deposition of a-Si:H with the conditions listed in the same table. After ablation, the sample was plated with nickel and copper in a light-induced-plating (LIP) system. The busbars of the cells are approximately 1 mm wide and the fingers are ~35 µm wide. The results with varied mask thicknesses are shown in figure 3.5.

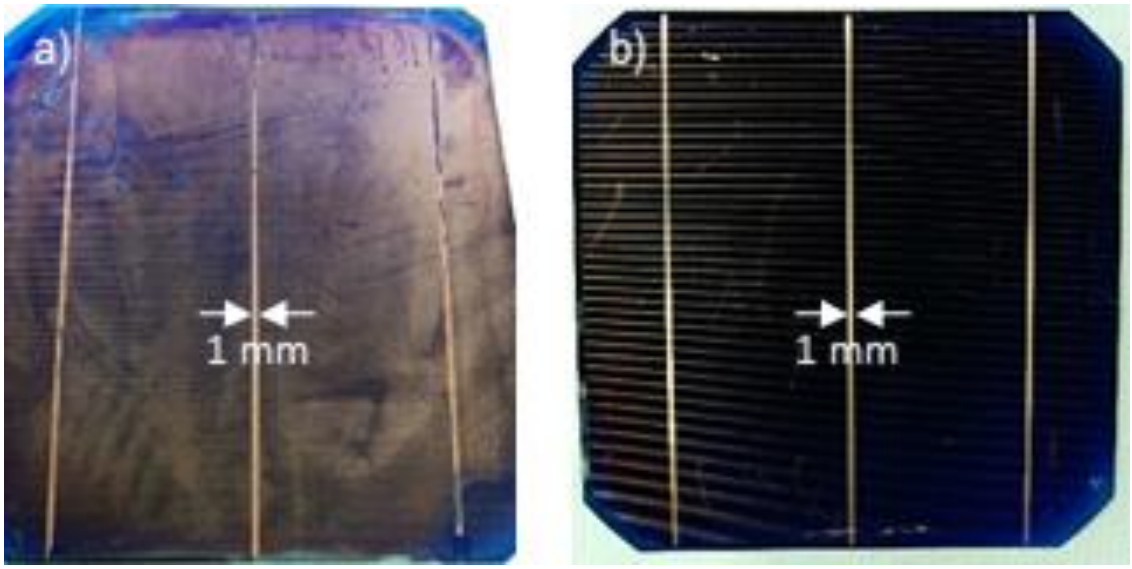

Figure 3.6: (a) Camera Image of Al-BSF Cell with Severe Ghost Plating (Background Haze) Using a 5 nm a-Si:H Etch Mask, (b) Camera Image of Plated Cell with Minimal Ghost Plating and a 20 nm a-Si:H Etch Mask [41].

A 5 nm a-Si:H etch mask was insufficient to prevent partial pinhole etching in the SiN_x passivating layer of the PERT cell, and this caused a substantial amount of ghost plating in 3.6(a). The ghost plating was so severe that fully opened locations at the top left and

bottom right of the cell did not plate. In 3.6(b) the laser intensity remained fixed at 210 GW/cm^2 and a 20 nm a-Si:H etch mask was sufficiently thick and prevented unintentional etching of the SiN_x. This also allowed for more complete plating in the contact areas that were deliberately opened with the ablation process. Both 3.6(a) and 3.6(b) were ablated with a laser intensity of 210 GW/cm^2 resulting in an increase in residual film at the ablation site.

SEM images of the solar cells shown in figure 3.6 (a) & (b) are shown in Figure 3.7. The 20 nm a-Si:H mask in 3.6(a) and 3.6(b) protects the SiN_x at non-ablation sites so that the Ni/Cu stack deposits in the laser openings without noticeable ghost plating. In 3.6(c) and 3.6(d) the 5 nm mask did not adequately protect the SiN_x at non-ablation sites, resulting in pinhole ghost-plating. Despite the reduction in the film removal for the 20 nm a-Si:H mask and the variation in the line-width introduced by the low overlap of pulses, the fingers and busbars in 3.6(a) and 3.6(b) maintain a reasonable uniformity. In the case of 3.6(c) and 3.6(d) the re-direction of the plating current causes a slight reduction of the finger and busbar thickness. The spacing of wires in 3.6(b) reduces the film stress in the busbar and improves adhesion of the contact. Samples without spacing would experience peeling with thermal anneals in excess of 300° C. Once annealed the solar cell shown in figure 3.5 (b) and SEM imaged in figures 3.6 (a) and (b) produced a cell with 16.9% efficiency.

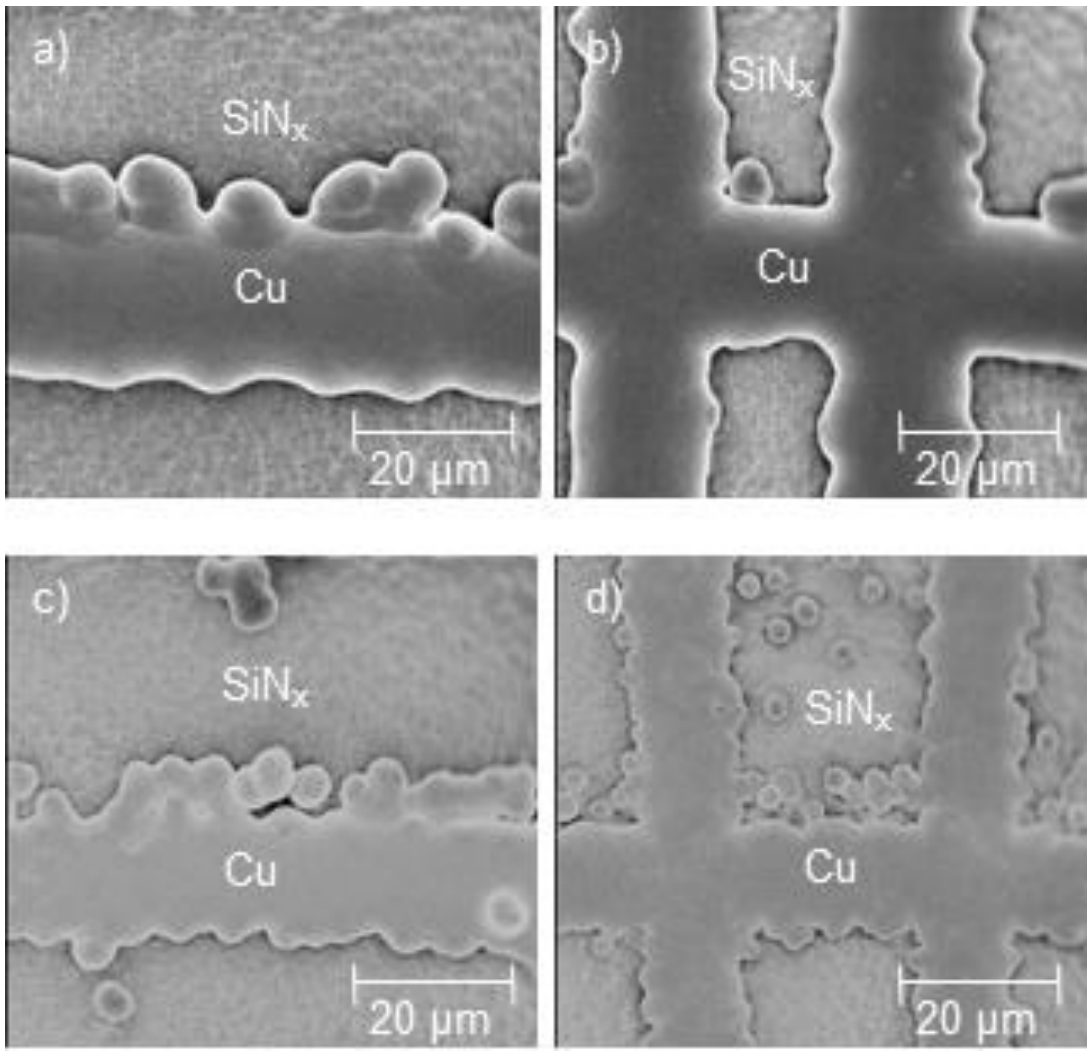

Figure 3.7 SEM Images of Ni/Cu Lip (a) Finger Location Using a 20 nm a-Si:H Mask, (b) Finger/Busbar Intersection Using a 20 nm a-Si:H Mask, (c) Finger Location with a 5 nm a-Si:H Mask, and (d) Finger/Busbar Intersection with a 5 nm a-Si:H Mask[41].

Figure 3.7 illustrates the effect of thickening the a-Si:H mask further while fixing the laser intensity at 210 GW/cm^2.

Figure 3.8 (a) shows an ~80% SiN_x film removal at the laser ablation site with the 20 nm layer of a-Si:H and less than 10% removal for a 40 nm a-Si:mask. The BOE etch step lifts-off a large portion of the non-ablated residual a-Si:H in 3.7(a), but in 3.7(b) the minor perforations that the laser causes in the thicker film are insufficient with a 5 minute etch time to cause lift-off. Further, as the mask thickness starts to approach the dielectric thickness, lift-off becomes less feasible. Further increase to the mask thickness would require an increase in the laser intensity, and will reduce the benefits of undercutting the residual a-Si:H mask that was not fully ablated.

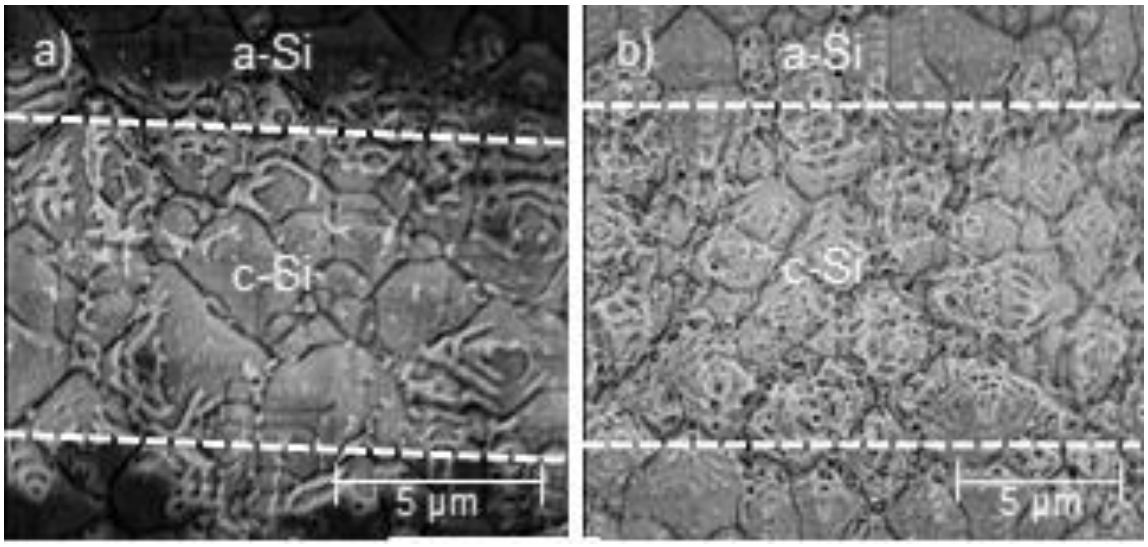

Figure 3.8: (a) SEM Image of a Laser Ablation Line with a 20 nm a-Si:H Etch Mask after BOE, (b) SEM Image of the Laser Ablation Line with a 40 nm a-Si:H Etch Mask after BOE. The Laser Line Widths Are Marked by the White Dashed Lines and Measure ~10 mm [41].

Figure 3.9 shows the performance of the 40 nm a-Si:H etch mask –after ablation and chemical processing– with increasing laser intensities. As the intensity in 3.9(a) of 210 GW/cm^2 is increased to 662 GW/cm^2 in 3.9(b) we see an emergence of laser-induced

defects (LID) highlighted in red in 3.9(b) and 3.9(c). Under the higher magnification in 3.8(c) the small black dots in 3.8(b) appear to be perforations in the c-Si surface ~200 nm in size and potentially penetrate through the shallow emitter.

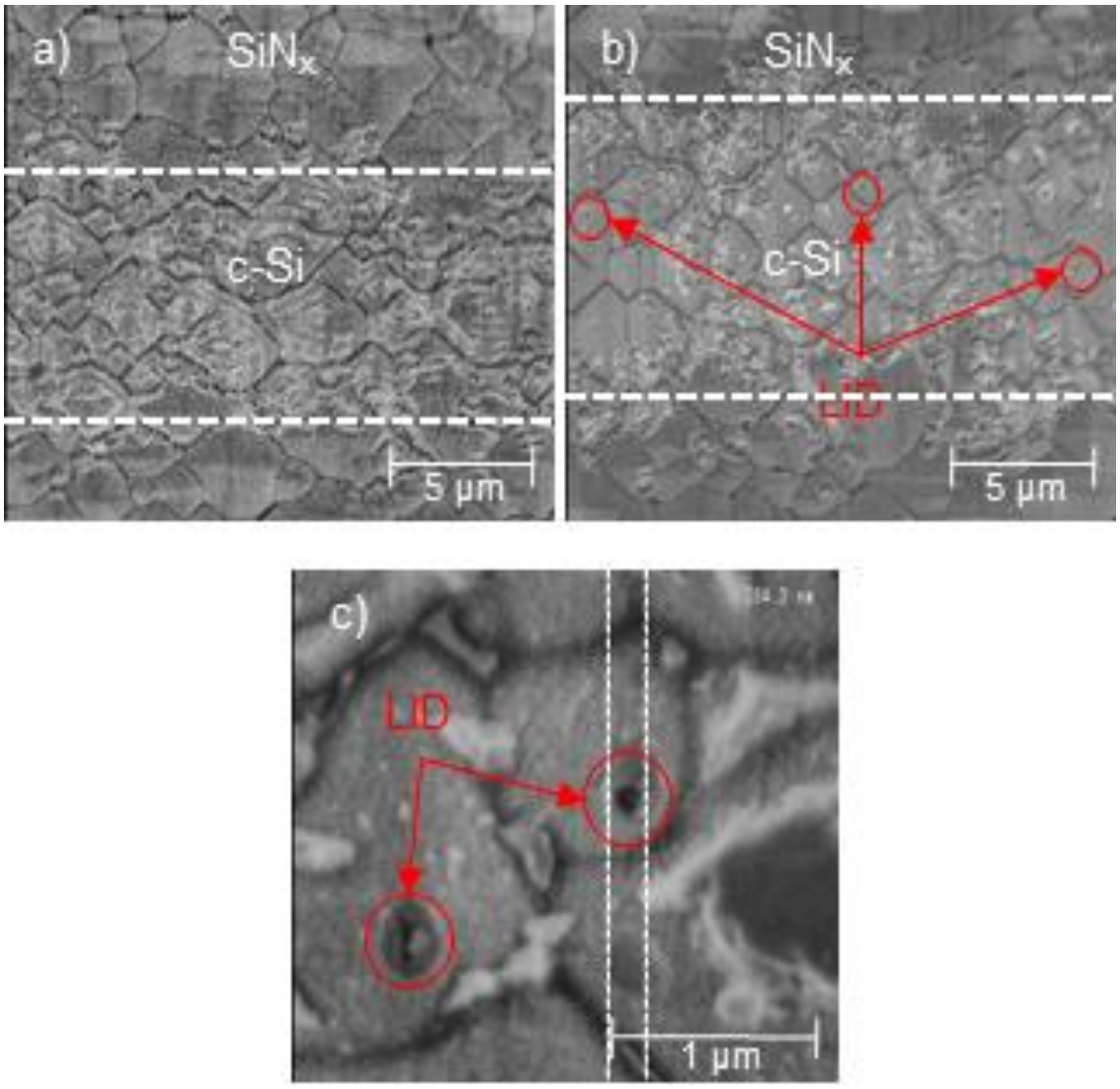

Figure 3.9: SEM Images of the Indirect Laser Ablation Process with a 40 nm a-Si:H Mask after BOE and KOH Processing with (a) Pd = 210 GW/cm^2, (b) Pd = 662 GW/cm^2, and (c) Pd = 662 GW/cm^2 with Higher Magnification [41].

Further investigation of the process shows more defects where laser lines overlap, i.e., at the busbar/finger intersections. Figure 3.10 shows this effect. Increasing the absorption of the laser in the mask would allow for a decrease in the laser intensity and potentially avoid the laser intersection defect generation. The approximate line width is denoted in 3.10(a) by the bounding white dashed lines ~10 μm apart and the defects are highlighted with red circles. The defect behavior here is similar to that observed in figure 3.3 (a); as the laser overlap is increased, defect generation is enhanced. A plausible explanation for the behavior in the indirect ablation process is that the a-Si:H mask partially shields the c-Si surface from the laser, thereby reducing its intensity. At the finger/busbar intersections the a-Si:H mask is first removed by the finger patterning, and then re-scanned by the busbar laser lines. This ~2.4 times exposure results in the c-Si surface being exposed to the full intensity of the laser. Under the higher magnification in 3.10(b) we see that the defects are ~200 nm in size, similar to the higher laser intensity case in figure 3.9 (b) and (c).

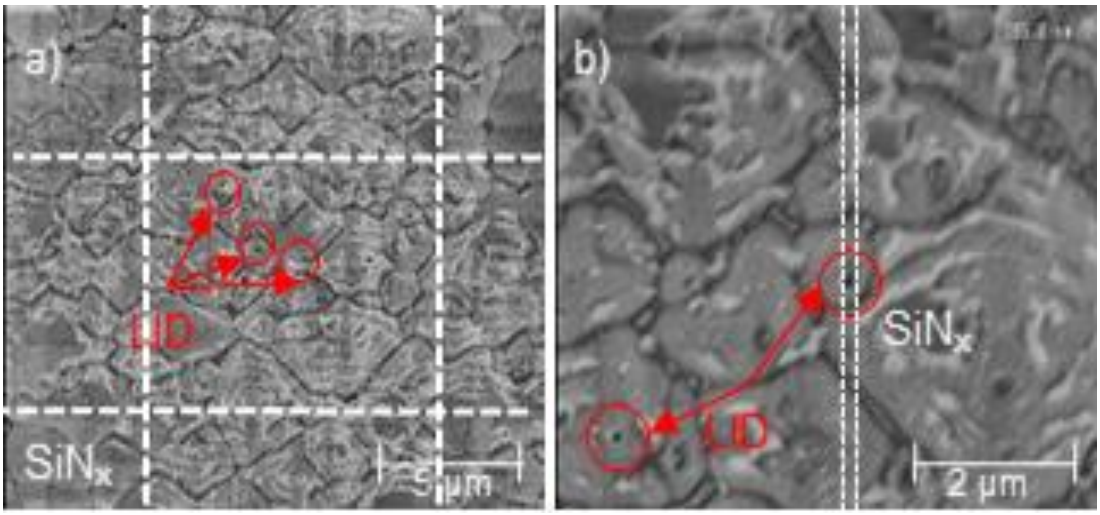

Figure 3.10: SEM Images of the Indirect Laser Ablation Process with a 40 nm a-Si:H Mask after BOE and KOH Processing with (a) Pd = 210 GW/ cm^2, (b) Pd = 662 GW/cm^2, and (c) Pd = 662 GW/cm^2 with Higher Magnification [41].

Given that we observe defects in all use cases of the laser, both with low intensities where we achieve ~80% film removal and higher intensities where we achieve ~95% removal, it can be concluded that line intersections should be avoided when possible.

CHAPTER 4

CHARACTERIZATION OF LASER-INDUCED DEFECTS

a) Effect of Defects on Surface Passivation and Shunting

Laser patterning is a low cost alternative to photolithography for patterning [32–37], but usually generates defects when used with textured surfaces. Methods for reducing the damage dealt have been devised, but there has been little success in completely eliminating defect generation [38,39,41,47]. Laser-induced defects (LIDs) have been correlated to the generation of nickel silicide (NiSi) induced shunts when combined with Ni/Cu plating and thermal annealing [40]. The thermal anneals are necessary to promote good ohmic contact to the solar cell necessitating that there be some form of defect compensation during processing.

Although some defects are present at the surface of the device, not all defects greatly depreciate the lifetime of the minority carriers. The effectiveness of the a-Si mask is evaluated and optimized in figure 4.1. In this case a symmetrical device with a double sided diffusion is used with a sheet resistance of 90 Ω/□. A Sinton WCT-120 photoconductivity tool is used to evaluate the minority carrier lifetime of the device after passivation, laser ablation, and firing (without contacts) for three different test cases. The initial case does not use an a-Si mask to protect the c-Si and relies on direct ablation of the SiN_x and SiO_2 films. The second and third cases use the process depicted in figure 3.4 for a non-optimized a-Si mask and an optimized a-Si mask. From the data collected on the photoconductivity tool, we can extrapolate an implied fill factor (iFF) for each step that includes all of the recombination present in the device, including shunting in the emitter.

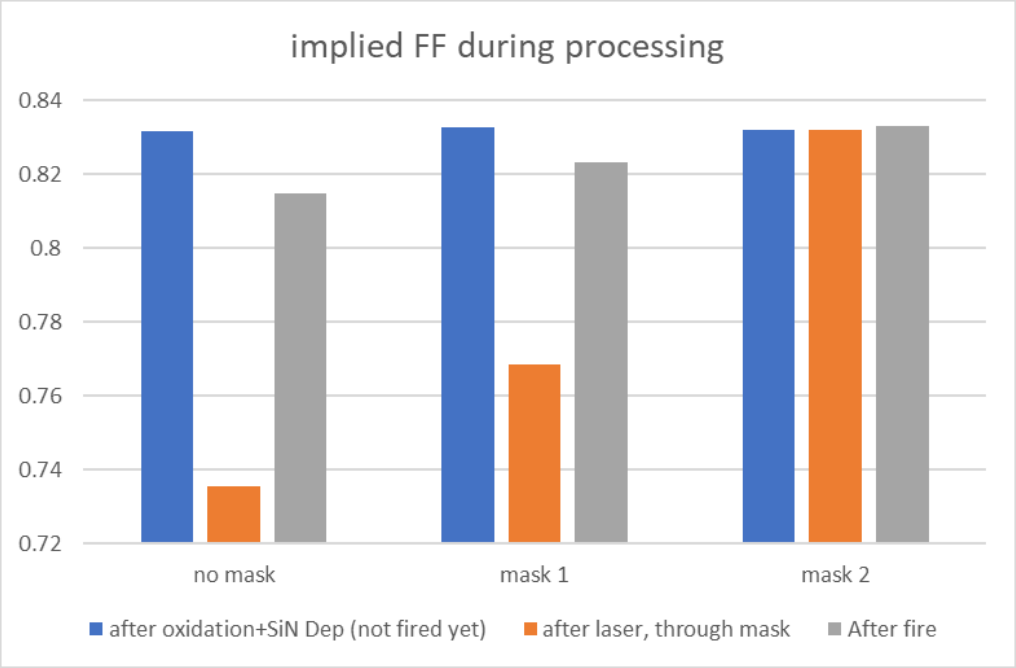

Figure 4.1: Effect of Laser Processing Optimization on iFF

From the optimization of the masking process shown in figure 4.1, we can see it is possible to eliminate the negative impact of the laser ablation process on the recombination present in the solar cell. The iFF over 0.83 throughout the process for the final process is consistent with an ideality factor of one and an implied open circuit voltage (iV_{OC}) of 640 mV. While the initial masking process showed a large improvement over the direct ablation process, it still depreciated the iFF and V_{OC} of the device, implying the presence of surface damage. While the last test case shows no evident damage, closer inspection is necessary.

Given the indirect laser patterning process, and the defects generated at the finger/busbar intersections, we expect there to be some loss of performance in the solar cell at the defect sites (if the defects are deep enough to allow for NiSi induced shunting). Figure 4.2 shows an illuminated lock in thermography (ILIT) image of the cell shown in Figure 3.5 (b), with the optimizations from figure 4.1.

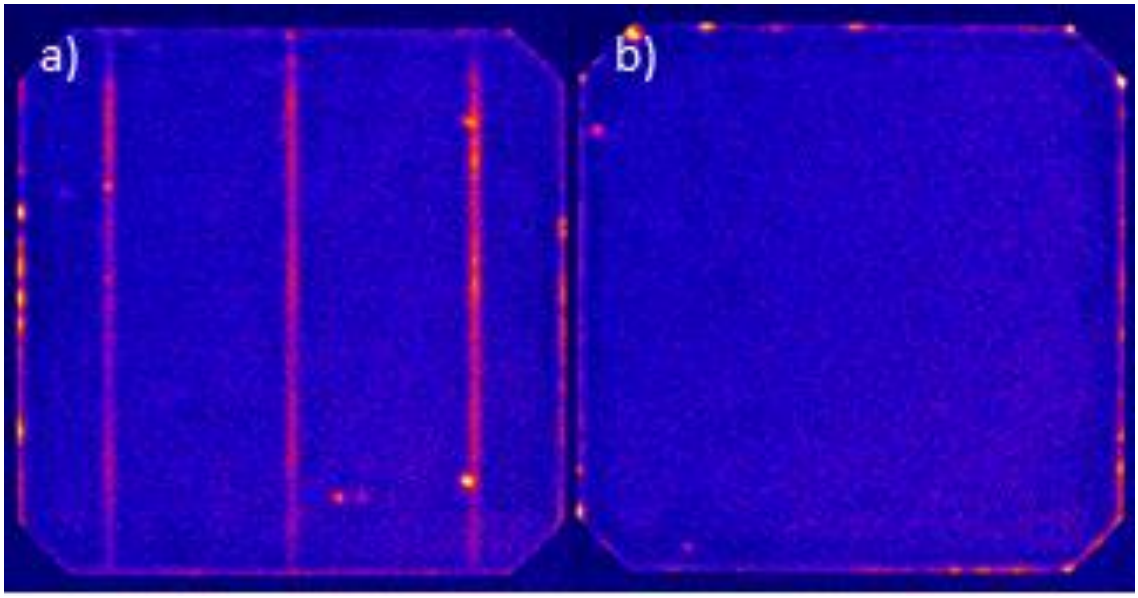

Figure 4.2: (a) ILIT of a Ni/Cu Metallized and Annealed Solar Cell Using the Indirect Laser Ablation Process with Finger/Busbar Intersections, (b) ILIT of a Ni/Cu Metallized and Annealed Solar Cell Using the Indirect Laser Ablation Process Without a Laser Patterned Busbar.

With ILIT, shunting in 4.2(a) at the busbar becomes evident. The defects introduced at the finger/busbar intersection are deep enough to reduce the shunt resistance of the solar cell with nickel silicidation. In 4.2(b) the laser patterned busbar is removed –thereby eliminating laser line intersections and the associated defects. Presumably this eliminated the defect-induced shunting as there is no observable correlation of bright spots in the ILIT to laser lines on the solar cell.

b) Identifying and Characterizing Defects

The shunt behavior observed in Figure 4.2 (a) suggests that the defects imaged in Figure 3.10 are deep enough to cause NiSi shunting with our metallization process and n-type emitter diffusion.

The periodic pattern appearing near and at the intersection of the laser lines is consistent with the behavior predicted by Hernandez *et al.* The red circle bounding the defects in 4.3(a) indicates the site of primary interest for transmission electron microscopy (TEM) [32]. The Pt deposition in 4.3(b) indicates some non-uniformity of the deposition (which may be due to the surface morphology of the sample); the increase in thickness at the site of interest causes some loss of lattice fringe imaging in TEM.

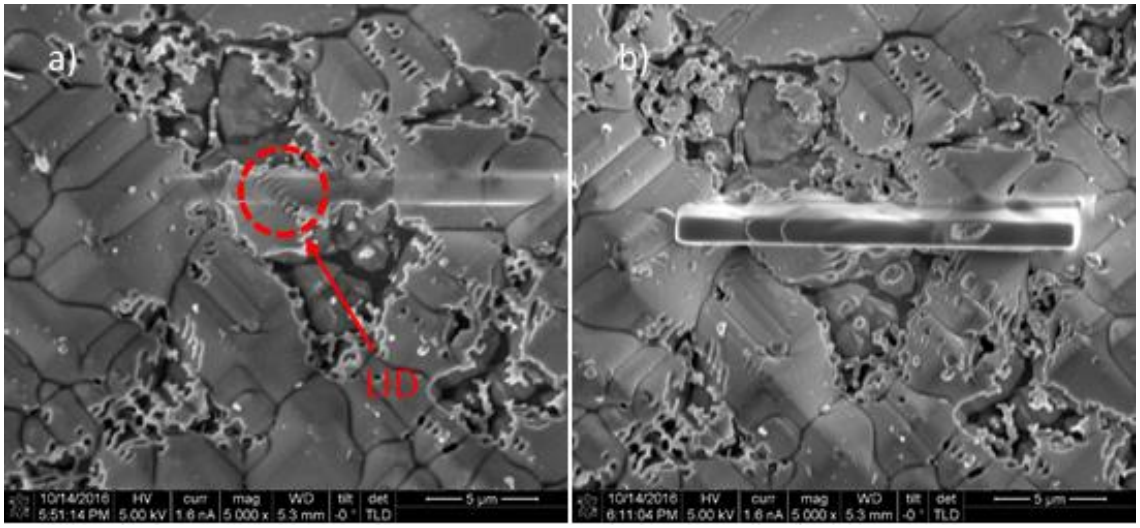

Figure 4.3: SEM of Samples Prepared for Focused Ion Beam Milling (FIB) with a 30 nm a-Si:H Mask and Pd = 210 GW/cm^2 (a) Image of the Sample at the Start of Platinum Deposition and (b) Image of Sample Once the Platinum Deposition Completed.

Figure 4.4 shows a low resolution TEM image of the sample cross section.

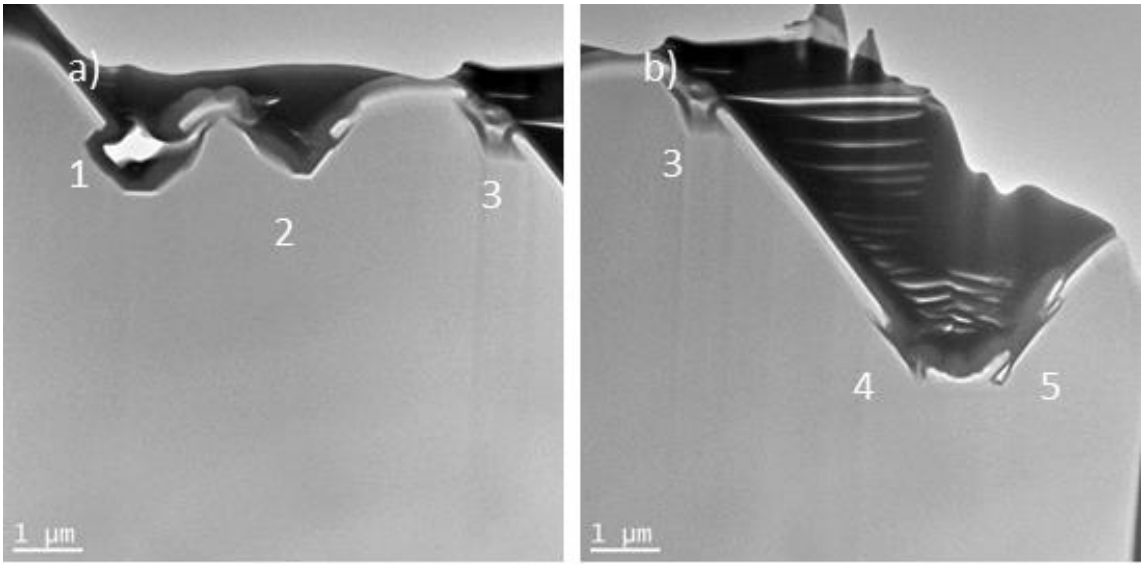

Figure 4.4: TEM of Samples Prepared via FIB (a) Left-most Region of the Sample, Numbered for Subsequent High Resolution Imaging (b) Right-most Region of the Sample, Numbered for High Resolution Imaging.

Defects 1-3 in 4.4(a) appear to be on a scale of ~100-400 nm in depth which is deep enough to cause issues with most industrial n-type emitters[12], especially with the formation of NiSi from annealing Ni. Defect 4 and 5 are ~50 nm deep which will not pose an issue for our emitter, presuming a lack of threading dislocations.

Under higher resolution we can see the lattice fringe images of the defects which will allow us to determine if there is amorphization of the lattice, threading defects, or other behavior. Figure 4.5 shows the lattice fringe images for defect regions 1, 3, and 5. The non-uniform deposition of Pt during the FIB process made the sample too thick in defect regions 2 and 4 from Figure 4.5 to get lattice fringing images of the sample so those images are not included.

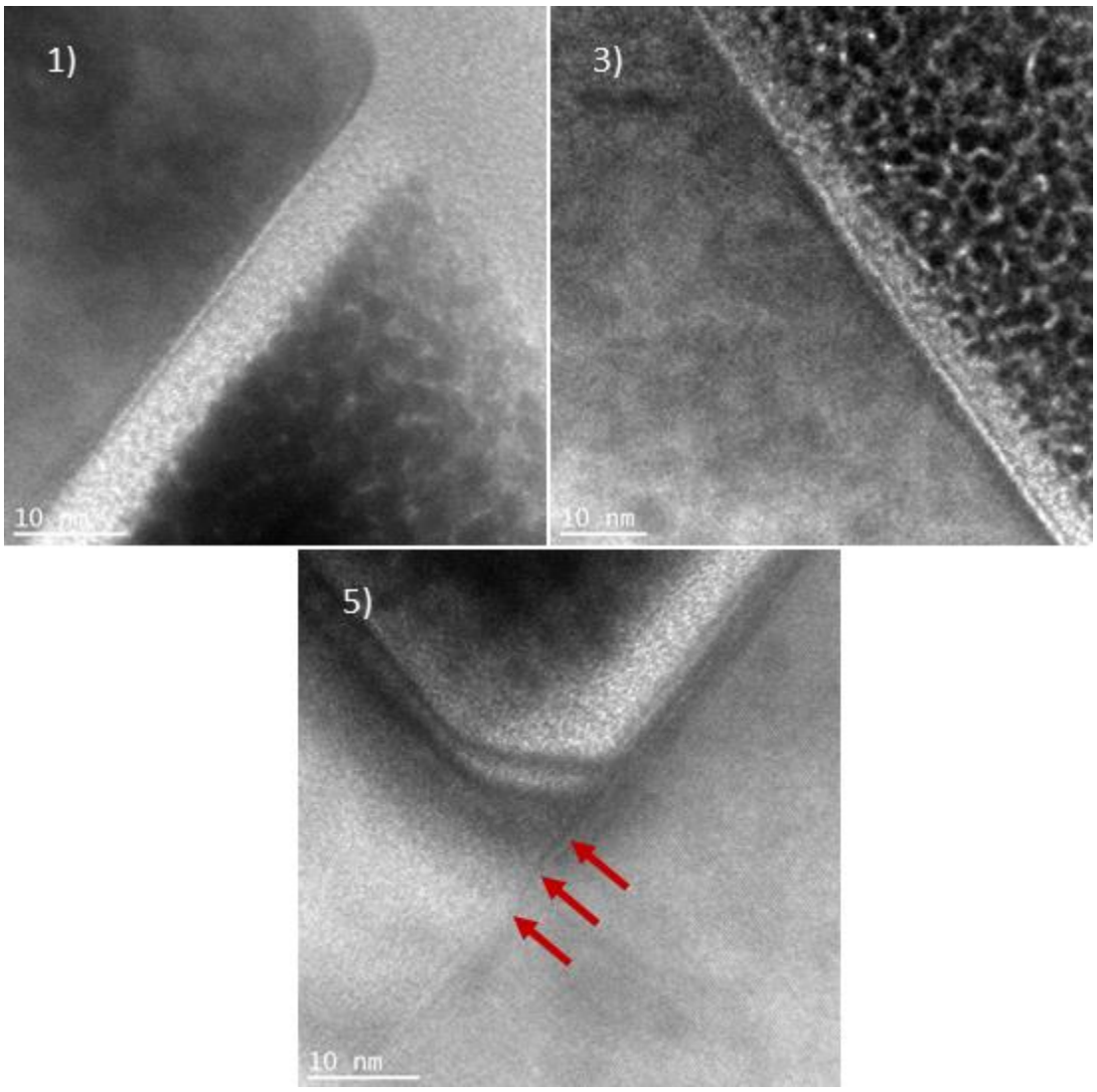

Figure 4.5: High Resolution TEM of Samples Prepared via FIB (1) Defect 1, (3) Defect 3, and (5) Defect 5, under Higher Magnification.

Defect region 1 is the top left corner of the region and shows no amorphization or threading defects; region 3 exhibits similar behavior. Region 5 also shows no amorphization or threading dislocations, but there is an observed defect denoted by the red arrows that propagates along a lattice plane. This defect is attributed to the channeling of ions across the crystal plane, leading to a partial amorphization of the lattice that was caused by the sample preparation, not the laser process.

Figure 4.5 supports the idea that the material removed by the laser process is removed via a plasma ablation process, not a thermal ablation process. The presence of lattice amorphization and dislocations is associated with the compressive strain introduced from non-uniform heating and liquefaction of the substrate at the lasing sites. The lack of these defects suggests that the multi-photonic absorption created with high intensities is generating impact ionization on a scale sufficient to cause the c-Si lattice to lose cohesion and vaporize at sites above the laser ablation threshold.

c) Nickel silicidation of defects

Investigation of Ni plated and annealed defect sites is more challenging than it is with non-plated samples. In the case without plating, defects can be seen from a top-view SEM during the FIB preparation process, allowing for the proper placement of the protective platinum bar and an understanding of where to start and stop the ion milling process. For plated samples, the relatively small surface defects are covered by plated metal, and milling has to be done in a 'guess and check' fashion to establish the presence of what appear to be defects. Figure 4.6 shows a concatenated TEM image (top right) of a laser line intersection along with a series of high resolution Scanning Transmission Electron Microscopy (STEM) images. Each one of the STEM images (categorized as A1-A5) is magnified region of the concatenated TEM image, and is indicated by a red dashed arrow. We consider A1 and A2 to be significant defect regions, A3 a shallow defect regiona, A4 a non-defective region, and A5 a SiN_x coated (non-ablated) region. No regions were found with threading dislocations.

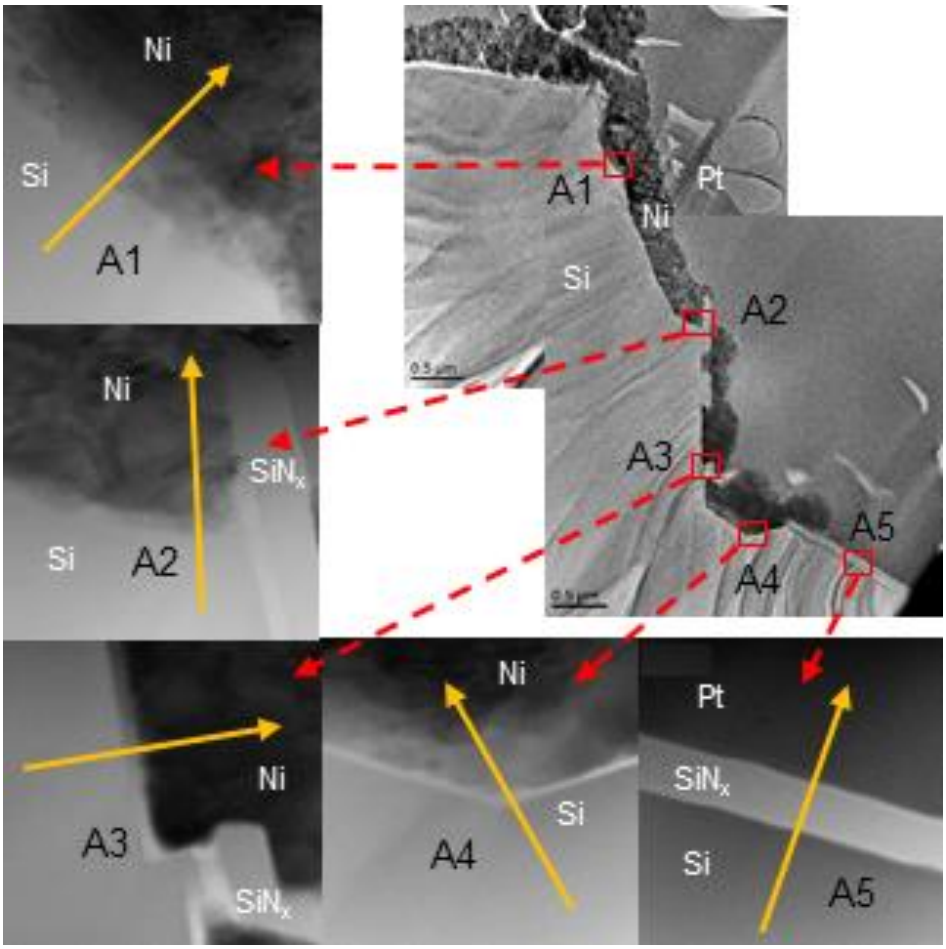

Figure 4.6: Cross Sectional TEM and STEM of a Laser Line Intersection with Annealed Ni, the Top Right Image Is a Concatenated Low Magnification TEM of the Sample, the Small Red Boxes Represent the Region of Interest and the Dashed Red Arrows Lead from the TEM Image to the Corresponding Stem Regions for Areas 1-5 (A1-A5). The Solid Orange Arrows Indicate the Direction of the EDS Line Scan for Material Composition Analysis of the Area of Interest.

Electron dispersive spectroscopy (EDS) scans were performed on each area, as indicated by the orange arrows in figure 4.6. Note that each scan starts in the bulk of the silicon and moves outwards into the plated nickel or protective platinum regions. For exposed silicon regions (regions without a SiN_x protective layer) the 2 minute 305 °C

rapid thermal anneal should have formed a 10-30 nm deep silicide. Figure 4.7 details the results of EDS for each area. A1-A5 all show a low Cu signal in all silicon regions with an increasing signal in Ni regions. The presence of Cu in the bulk of the silicon as well as in the Ni bulk indicates contamination in our Ni plating bath, or that the Ni layer is insufficient as a barrier layer but for our purposes this is of little concern. The defective regions A1-A3 were found to have no evidence of Ni spike through at the Si/Ni interface, suggesting that the laser process has introduced no bulk defects aside from the generation of surface voids. A3 shows the generation of a small void at the Ni/Si interface which we attribute to thermal strain from the annealing process, not to laser damage. A1, A2, and A4 show a NiSi silicidation depth of approximately 30 nm, as expected. The SiN_x coated area A5 shows no silicidation, indicating that the film is a barrier to Ni diffusion. The Cu seen in A5 is likely due to contamination from adjacent regions as Cu readily diffuses at room temperature in Si.

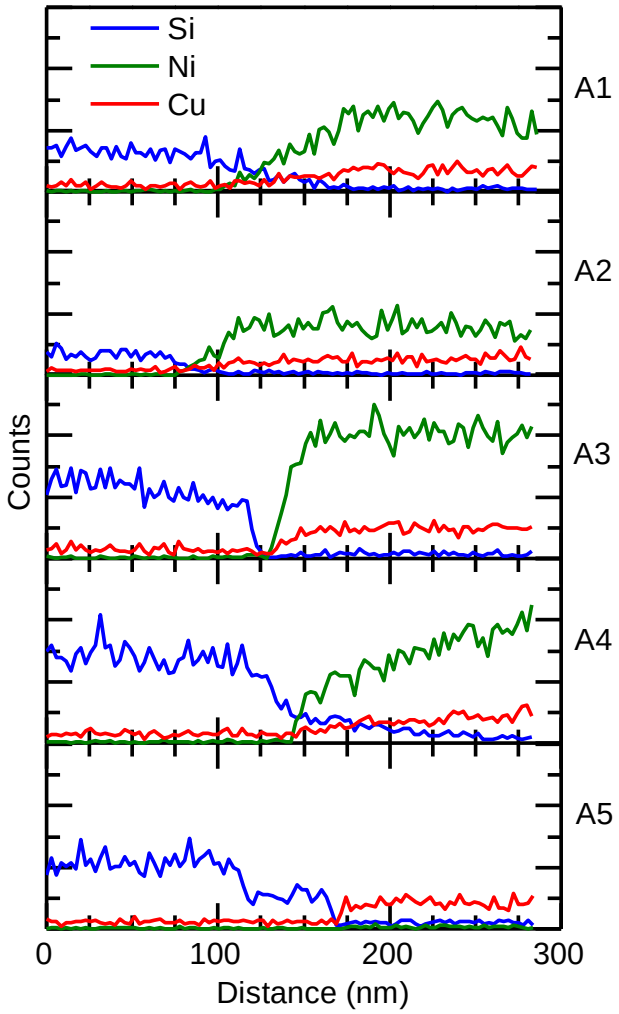

Figure 4.7: EDS Line Scan of Stem Regions, A1 a Deep Defect Area, A2 a Deep Defect Area, A3 a Shallow Defect Area, A4 a Normal Area, and A5 a SiN_x Coated Area.

Based on the lack of Ni spike through observed in A1-A5 we surmise that our laser ablation process does not generate threading dislocations into the bulk of the substrate, and that defects observed in SEM, TEM, STEM, and ILIT are the result of a conductive bridge that forms in voids that perforate the emitter of the solar cell. Appropriately compensating for these defects is then possible by reducing the size of the large voids, increasing the

diffusion depth of the emitter beyond the depth of the defects generated, or by preventing the metallization of voids.

d) Compensating for Defects

Defects introduced with laser processing can be compensated with selective emitter diffusions, annealing (presuming the c-Si material is still present), and sufficiently deep emitters[34,37,40]. As the depth of the emitter increases, the open circuit voltage (V_{OC}) and short circuit current density (J_{SC}) decrease, both of which are undesirable for high efficiency solar cells. This effect can largely be compensated for by reducing the surface concentration of the diffusion, and extending its depth.

Given that the laser line intersections have been demonstrated to generate defects on the scale of ~400 nm, and that extending diffusions into the bulk depreciates the performance of the solar cell, we simulated a series of diffusions using PC1D to guide our diffusion development. We assumed a front and rear texture depth of 3 µm, emitter contact resistance of 0.5 Ω, bulk resistivity of 2.5 Ω·cm, a rear reflectance of 68%, a substrate thickness of 170 µm, and surface recombination velocities of 300 cm/s. The dopant profile was established by varying the FrDopDpth parameter with an error function to get the desired junction depths. The surface concentration was varied from 5e18 cm^{-3} to 1e20 cm^{-3}. The results of the simulated V_{OC}, J_{SC}, and sheet resistance (R_{SHEET}) are shown below in figure 4.8.

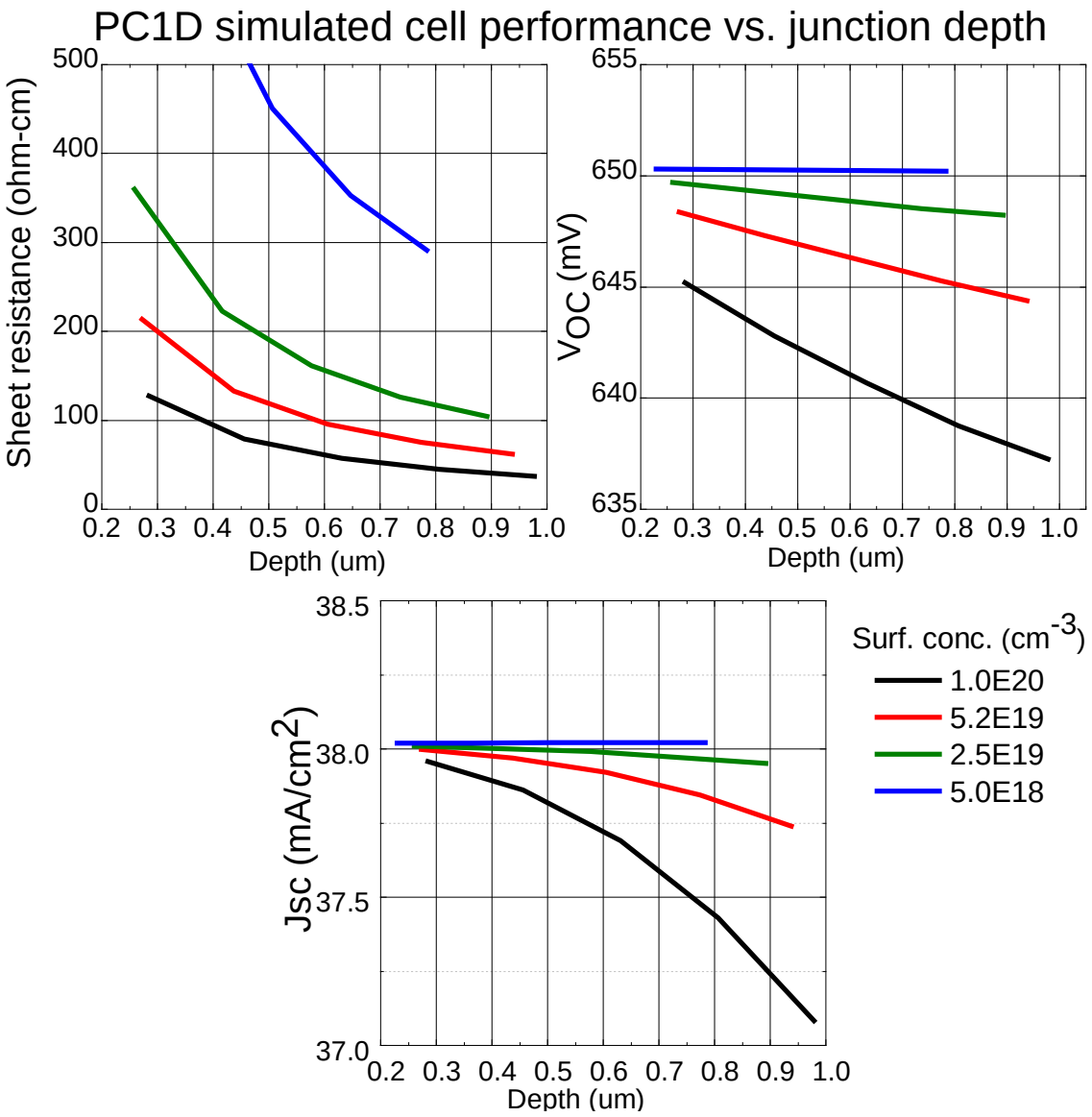

Figure 4.8: PC1D Simulation of R_{sheet}, V_{OC}, and J_{SC} as a Function of Varied Surface Concentrations and Junction Depths.

As expected, as the surface concentration of the diffusion decreases, the impact of deepening the junction on the solar cell's performance decreases. With FrDopDpths at and below 5.2E19 cm^{-3} the loss in V_{OC} drops to ~2-3 mV for depths up to 0.9 µm; similarly the loss in J_{SC} drops to 0.5 mA/cm^2. At concentrations as low as 5E18 cm^{-3} we see no appreciable loss in performance for this depth scale, but the sheet resistance of the emitter

becomes very high. While Stavitski *et. al* demonstrated m·Ω·cm contact resistance down to concentrations as low as 3E18 cm^{-3}, the ohmic losses from lateral transport of carriers for a typical front-grid contacted solar cell would be substantial[48]. As such, we limit our diffusion development to sheet resistances with ~100 Ω/□.

Emitter development was done with an MRL-FCE horizontal tube furnace. The $POCl_3$ bubbler temperature was fixed at 30° C and the temperature profile of all lots was fixed. Phosphosilicate glass (PSG) formation (pre-dep) and N_2 ambient drive in were both performed at 855° C for 10 and 20 minutes, respectively. Varied surface concentrations were achieved by adjusting the N_2 carrier gas flow to O_2 gas flow ratio. Samples were 156 x 156 mm^2 pseudo square substrates with a double-sided texture and a bulk resistivity of 1-3 Ω·cm. Table 4.1 details the effect of varying the gas flows on the sheet resistances of the emitters and the wafer-to-wafer standard deviation.

Table 4.1
Conditions for PSG Formation

O_2/N_2 carrier ratio	Sheet resistance (Ω/□)	Std. Dev (Ω/□)
2.5	27	0.7
9.5	66	3.3
13	89	7.7
20	147	7.4

The sheet resistance is useful for a first order approximation of the junction, but it does not provide detailed information on diffusion profile. A set of 6” round p-type boron doped wafers with a bulk resistivity of 1-10 Ω·cm was run through the varied diffusion processes with dummy wafers to approximate normal loading conditions and then sent to

Solecon Labs for spreading resistance analysis (SRA) [24]. The results are shown below in figure 4.9.

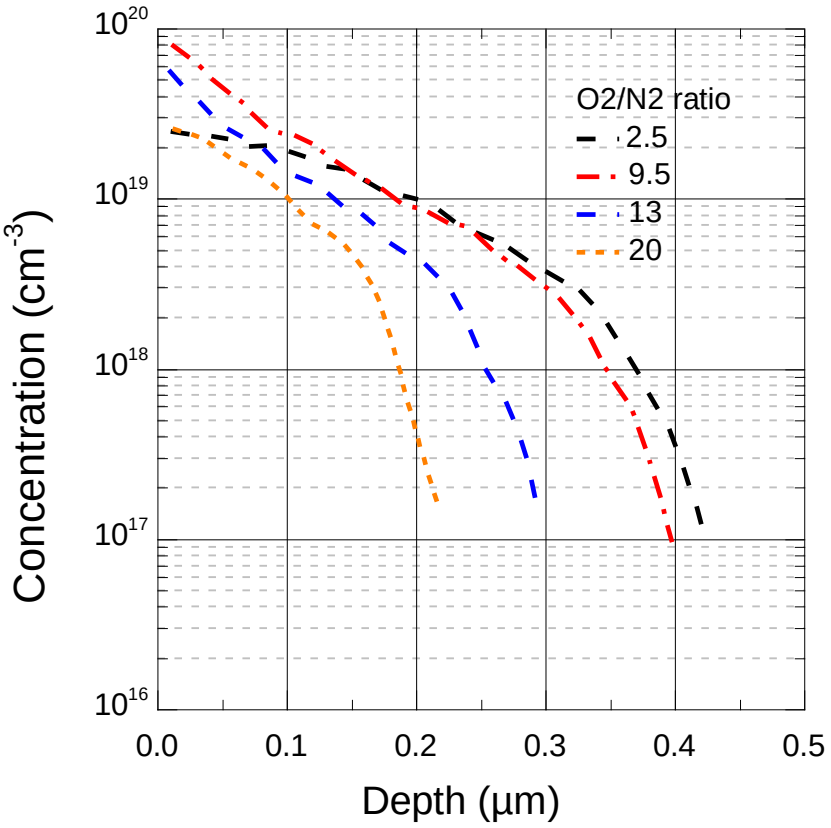

Figure 4.9: SRA of Polished P-type Boron Doped Wafers with Varied O_2/N_2 Carrier Gas Ratios

We see from figure 4.9 that lower ratios typically lead to a heavier doped emitter, but for some cases the active dopant concentration is seen to depreciate. The depreciation seen in the active dopant for the 2.5 ratio is attributed to the generation of a phosphosilicate dead layer, where the concentration of phosphorous is high enough that it forms non-active complexes with silicon. This dead layer has been demonstrated to inhibit proper surface passivation, as well as increase the resistance of metal contacts [14]. As the carrier gas for

the $POCl_3$ is reduced, the amount of phosphorous present in the PSG decreases. Very lightly doped emitters also experience a depreciation in depth –a result of a decrease in field enhanced diffusion and dopant atom availability– which will require longer drive in times to achieve similar junction depths [49].

Using a gas ratio of 9.5 and a lighter diffusion load (fewer dummy wafers), we maintained similar processing conditions used to generate figure 4.6 and varied the N_2 drive in time after PSG formation. The SRA analysis of this experiment for 45, 90, and 135 minute N_2 drive in times are shown below in figure 4.10.

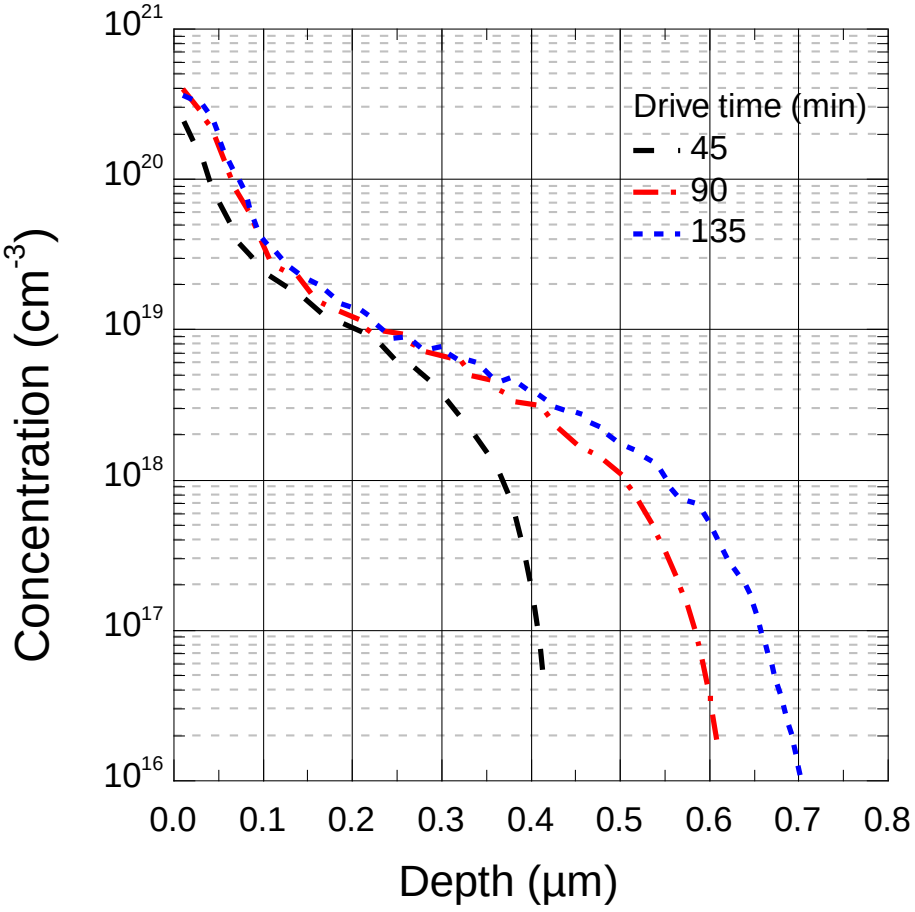

Figure 4.10: SRA of Polished P-type Boron Doped Wafers with N_2 Drive in Times

The decreased loading conditions increased the dopant concentration in the emitter, showing a large dependency on the area and number of wafers used for processing. The 45 minute sample was processed with a $POCl_3$ bubbler temperature of 20° C, whereas the 90 and 135 minute diffusions were processed with a bubbler temperature of 30° C. As is expected within normal diffusion operating regimes, a decrease in the bubbler temperature leads to a decreased concentration of phosphorous in the PSG and subsequently, a lighter doped emitter. Taking into consideration the cooler bubbler of the 45 minute diffusion process, the recipes with increased drive in times clearly show a deepening of the emitter while maintaining similar surface concentrations. This suggests that we can use this series of diffusion recipes to design emitters with surface concentrations ranging from 2.5E19 to 3E20 cm^{-3} and junction depths between 0.2 and 0.7 µm.

Considering the results of the PC1D simulation in figure 4.8, and the diffusion results in figures 4.9 and 4.10, we have a reasonable strategy to create a lightly doped deep emitter that can compensate for LIDs. Assuming a surface concentration between 2.5E19 and 5E19 cm^{-3}, a junction depth $\geq$ 0.5 µm (deeper than the LIDs shown in figures 4.3-4.6) we should be able to compensate for the NiSi shunting demonstrated in figure 4.2.

e) Cell results

Based on the development work done with Solecon Labs, what we see from PC1D modeling, and feedback from Ian Cooper, we opted for a gas ratio of 6.7 and a reduced bubbler temperature from 30 °C to 20 °C. These adjustments were made to improve the uniformity of the diffusion –as very high gas ratios provided very non-uniform emitters–

as well as maintain a lower concentration of phosphorous at the surface of the device (achieved by the decreased bubbler temperature). We target an average sheet resistance between 50 and 75 Ω/□ before thermal oxidation, and 65 to 90 Ω/□ after oxidation. Post-oxidation results are denoted with a * in table 4.2 along with the sheet resistance and standard deviation of each emitter for varied nitrogen anneal times. The varied nitrogen anneal times are used to achieve varied junction depths while maintaining the surface concentration of phosphorous, as was demonstrated in figure 4.7.

Table 4.2 Emitter Diffusion Parameters

Drive in time (min)	Average sheet resistance (Ω/□)	Standard deviation (Ω/□)	Estimated depth (nm)
45	72.5	3.7	400
45*	89.9	4.3	450
90	54.4	2	600
90*	65	2.6	650

Further work with Solecon labs (not shown here) demonstrated a junction depth increase of approximately 50 nm for standard diffusions, and is assumed in table 4.2. Given the relatively low standard of deviation for achieved for all diffusions, and the targeted resistance values for our cells, we perform the same indirect laser ablation process detailed in figure 3.4 to create openings in the dielectric for patterning. The most notable change in the process is the stabilization in the laser output power. The RMS instability in the time average power has been reduced from 5% to 1.2%, which allows for the same average intensity output, but depreciates the frequency of abnormally high intensity pulses. With the stabilization of the output, the overall time average power of the laser increased, necessitating an increase in the filtering to reduce the output to the same level.

Specifically, the neutral density filters were increased from a value of 3.0 to 3.1 in order to maintain the power density of 210 GW/cm^2 used previously. This coupled with a 30 nm a-Si mask, a 5 minute BOE, a 5 minute room temperature KOH etch (3%), and a metal ion clean with RCA-B proved to be the most effective set of conditions for patterning. Once the device is patterned we plate the cells in the same fashion as described in [50–52].

Following metallization and annealing the solar cells were flash tested to determine their performance, the results of which are detailed in table 4.3. The low short circuit current density (J_{SC}) is attributed to cell shading from ghost plating and is confirmed with external quantum efficiency (EQE) measurements. Integrating the EQE in non-ghost plated regions shows $J_{SC} \geq 39$ mA·cm^{-2} while the ghost plated regions only has a $J_{SC} \leq 37$ mA·cm^{-2}. If we consider the shading introduced by the busbars of the solar cell, and take the value for the ghost plated regions of the device, we would expect $J_{SC} \leq$ 36 mA·cm^{-2}. The high series resistance seen in all the devices (>1 Ω·cm^2) is attributed to the narrow contact width (~10 μm), narrow plated line width (< 40 μm), and finger breakages, ultimately resulting in a poor fill factor (FF). The low J_{SC} combined with the low FF of the device leads to a lower efficiency device, but for our purposes the primary parameter of concern is the shunt resistance, which indicates the presence of damage to the surface of the substrate. The high shunt resistance (R_{SH}) of ≥ 20 kΩ·cm^2 far exceeds the initial R_{SH} values of ≤ 1 kΩ·cm^2 we obtained for the device imaged with ILIT in figure 4.1 (a). The high R_{SH} of the devices yield a high pseudo fill factor (pFF) which suggests the surface quality is good and that if the plating issues can be resolved, a high efficiency device can be realized.

Table 4.3 Plated Cell Results

Cell #	Estimated depth (nm)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)	R_S ($\Omega \cdot cm^2$)	R_{SH} ($k\Omega \cdot cm^2$)	pFF (%)
1	450	630	34.3	66.3	14.3	2.6	20.4	81.1
2	650	632	35.7	72.6	16.4	1.6	30.7	81.7
3	650	623	34.7	70.4	15.2	1.9	23.6	81.2
4	650	628	33.2	67.8	14.1	2.4	24.5	81.6
5	650	628	32.3	72.2	14.6	1.8	23	80.4

Unlike the devices imaged with ILIT in figure 4.2, the devices imaged with ILIT in figure 4.11 from table 4.3 show minimal, if any shunting. The device in (a) corresponds to cell #1 in table 4.3 with an $R_{SH} = 20.4\ k\Omega \cdot cm^2$, with a slight shade variation in the image in the top of the middle busbar which may be due to some shunting. The device in (b) is cell #2 from table 4.3 and has a slightly deeper emitter, making it more robust to defects introduced by the laser process. While there is some shade variation in the image below, it is attributed to the effect of metal interacting with the backside illumination of the device. The $R_{SH} \geq 23\ k\Omega \cdot cm^2$ for the 650 nm deep junction may be due to the enhanced depth of the emitter, but with such a small sample size for the 450 nm deep junction, it is difficult to say so definitively, especially given $R_{SH} > 20\ k\Omega \cdot cm^2$ seen for the 450 nm deep device. While this device has the same depth emitter as the device in figure 4.2 (a), it was processed with a depreciated laser instability, which may have reduced the depth of the defects introduced.

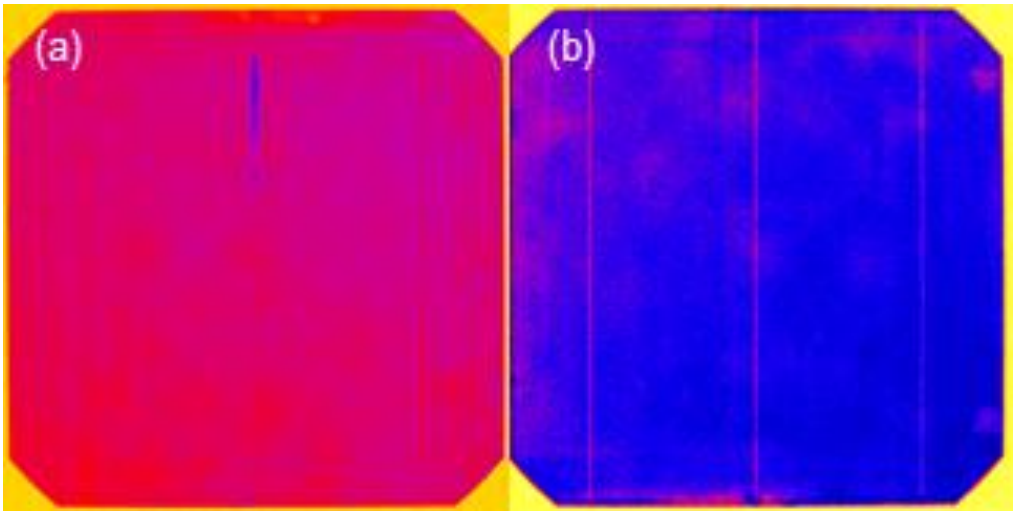

Figure 4.11: ILIT of Laser Patterned and Plated Solar Cells with (a) Laser Line Intersections and a Diffusion Depth of ~450 nm and (b) Laser Line Intersections and a Diffusion Depth of ~650 nm

CHAPTER 5

ANALYSIS OF LASER RESIDUE

a) Source of Residue Generation

Laser thin film removal on textured silicon solar cells generates debris on the surface of the cell, either within the laser spot, or immediately outside of the laser spot. In this section, we investigate the properties of the residue generated by femtosecond laser ablation of an amorphous silicon masking layer on both polished and textured substrates. We find that the presence of sharp edges introduced via alkaline texturing results in an increase in residue coverage due to the increase in the number of high arrival angle surfaces. Investigation of the residue with cross-sectional SEM shows that the residue is not the result of underlying film peeling. Ellipsometry, AFM, and SEM are used to establish an average surface roughness of the residue on a polished silicon surface. FTIR and EELS are used to determine the composition of the residue and demonstrate that there is no incorporation of nitrogen, carbon, or oxygen from the underlying films or surrounding materials. Finally, we use STEM along with electron diffraction to establish the micro-crystallinity of the residue, to which we attribute the chemical resilience of the residue to our etching processes. This behavior is consistent with findings that demonstrate ablation with sub-picosecond lasers is the result of plasma generation [53–55].

Figure 5.1 (a) illustrates the ideal performance of the indirect ablation process with a complete removal of all masking a-Si in the laser line. Figure 5.1 (b) details a more accurate model of the process where the a-Si was not completely removed, and the plasma from the ablation process has generated a residue that interferes with the removal

of the underlying dielectric films, SiN_x in this case. The decrease in the fractional opening of the a-Si mask leads to a similar depreciation in the opening in the SiN_x, reducing the opening of d_1 in (a) by the fraction of the residue in the laser ablation line to d_2 in (b). While this effect is mitigated by chemical undercutting that occurs from the isotropic etch behavior of wet etchants [56], it does not completely resolve the issue of depreciated openings in the dielectric within the laser spot.

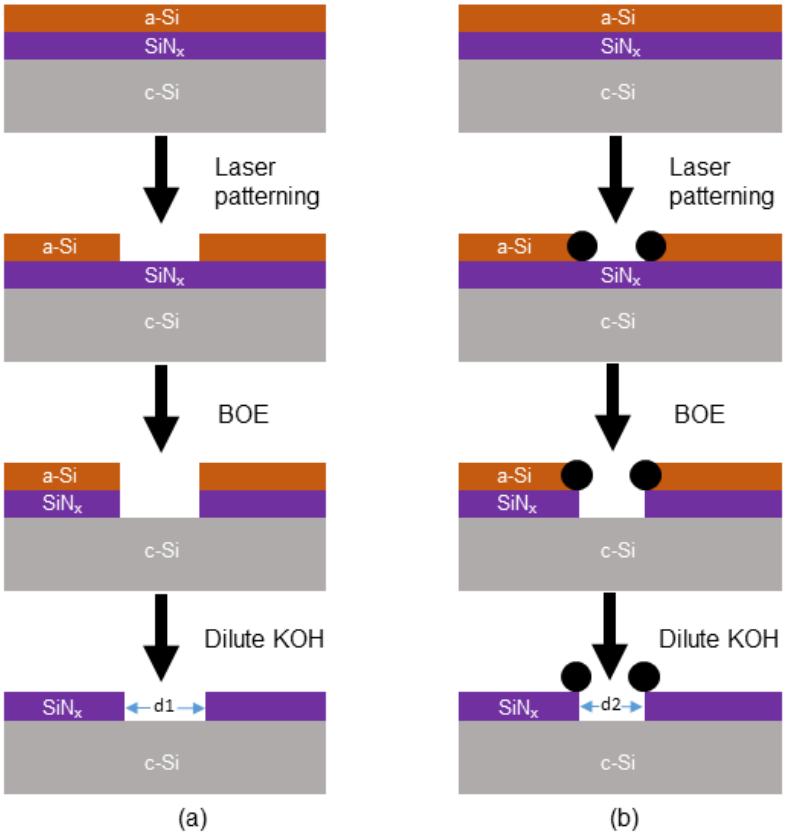

Figure 5.1: Processing Scheme for Indirect Removal of SiN_x (a) Ideal Removal of a-Si Mask and Underlying SiN_x Layer with an Opening Diameter D1 and (b) Theorized Removal Process of a-Si and SiN_x Layers with Incomplete a-Si Ablation, Laser Residue Formation, and Opening Diameter D2.

The removal of the mask layer occurs via the action of energetic electrons causing impact ionization on a large enough scale to generate bond breakage and facilitate the creation of a plasma [41]. Like other plasmas, such as those seen in reactive-ion etch (RIE) tools, the ions generated have some energy that may be sufficient to cause the generation of secondary ions. Ions can also be trapped on impact (presuming an inelastic collision) and cause the generation of sidewall veils at sharp interfaces, where the arrival angle of ions is high [57]. Figure 5.2 illustrates the generation of a step immediately adjacent to the ablation site, where the a-Si has not been removed. This step would serve to create an arrival angle (Θ°) of 270 degrees. Any ions impinging on this interface would impact a room temperature film at atmospheric pressure and cause the ion to become trapped, due to the poor ad-atom mobility. If a large enough volume of ions impact this interface then there would be an accumulation of material on the edge of the laser spot [41,57,58].

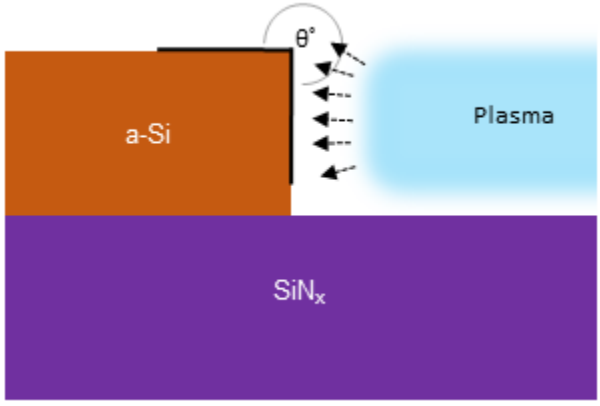

Figure 5.2: Diagram of Thin Films Interacting with the Femtosecond Laser Induced Plasma, the Arrows Denote the Direction of the Ions from the Vaporized a-Si Region, and θ° Represents the Arrival Angle of the Escaping Ions Impinging on the Non-vaporized a-Si Immediately Adjacent to the Laser Spot.

The resilience of these sidewall veils created during the ablation process suggests the generation of a hard residue. The resilience of this residue may be be the result of the incorporation of secondary ions generated in the laser plasma, or may be the result of a semi-crystalline residue.

b) Residue Identification

Patterned textured samples were prepared following the process illustrated in Figure 5.1, only without the buffered oxide etch step. Samples prepared in this fashion showed faint white lines where the laser had traveled (not shown due to poor contrast), similar to what was seen with the full process in figure 5.1. Initial attempts to characterize these lines with SEM were unsuccessful due to electron beam charging of the SiN_x film [59–63]. Fortunately, by using an in-lens detector in a ZEUSS Auriga CrossBeam© SEM allowed for appropriate stigmation and focusing corrections to image the surface. In Figure 5.3 (a) we see a collection of residue across the pyramid structures within the laser line.

The presence of many edges with high arrival angles (due to texturing) and the incomplete ablation of the a-Si during the ablation process on textured surfaces the probability of ions (and/or secondary ions) escaping from the area is reduced. The effect of ion trapping is exacerbated at the periphery of the laser spot, where there is the greatest amount of residual a-Si (due to the decreased laser intensity). To further characterize this a trench was milled in the sample shown in (a) using a focused ion beam (FIB) inside the laser line shown in (a) to create the cross-sectional SEM shown in (b). From the cross-sectional image we can see that the residue is not the product of SiNx film delamination, or the product of silicon emulsion from the surface, but rather some modified film from

the a-Si ablation process. This ‘sidewall veil’ deposited during the ablation process shows resilience to KOH etching, as it was not removed during the KOH mask strip step. This may indicate that the residue is resilient to the etch or thicker than the a-Si masking film.

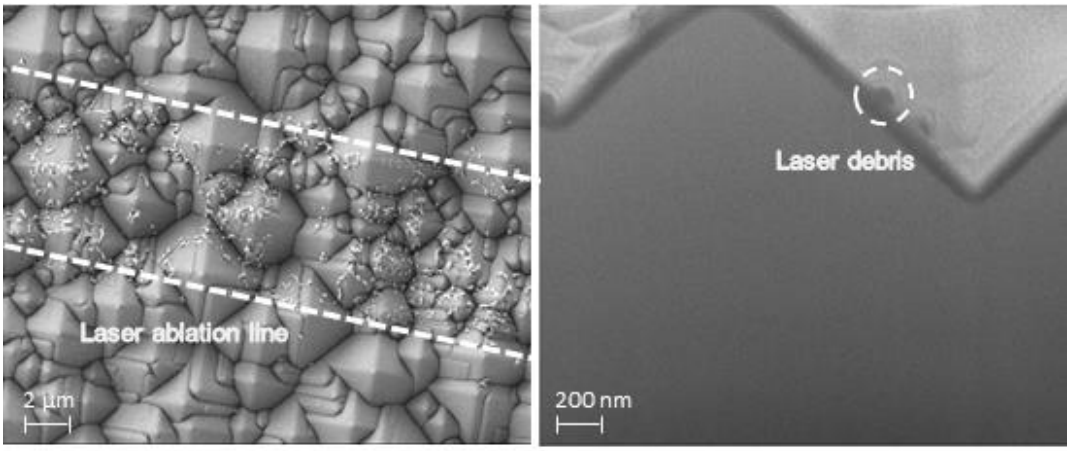

Figure 5.3: Scanning Electron Microscope (SEM) Images of a Laser Ablation Line on a Textured Surface Following Mask Removal. (a) Top View and (b) Ion-milled Cross Section of Residue

c) Residue Morphology and Optical Characterization

Optical characterization of the residue necessitates the use of a polished substrate. Two samples were prepared with SiN_x film thicknesses of 50 and 150 nm, respectively. Each sample was coated with 30 nm of a-Si, and then laser ablated and KOH etched.

Figure 5.4 illustrates the surface roughness of the laser process film with (a) atomic force microscopy (AFM) and (b) SEM. The AFM indicates an in-line root mean square (RMS) roughness of 11 nm, and a cross-line scan RMS surface roughness of 72 nm. SEM of the scanned regions show a similar surface roughness to what is seen in AFM, with a similarly increased cross-line surface roughness that we attribute to the scanning direction of the laser.

It appears from the AFM and SEM that the size and placement of the residue is dependent on the direction of laser travel, which suggests that the residue itself is ablated by the overlapping pulses. If the residue ablated in the plasma process, then it must be absorbing the laser readily, suggesting that the residue is comprised primarily of silicon.

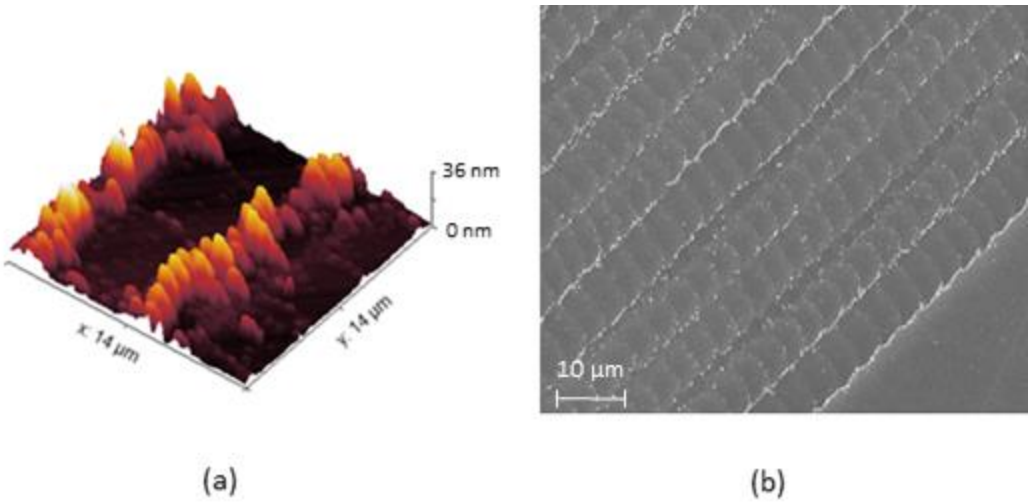

Figure 5.4: AFM and SEM of Overlapping Laser Ablation Lines with Surface Roughness from Residue Generated During the a-Si Ablation Process, Post a-Si Removal (a) AFM of Laser Ablation Lines with an In-line RMS Roughness of 11 nm and a Cross Line RMS Roughness of 72 nm (b) SEM of Ablation Region Showing Surface Roughness

Figure 5.5 shows the typical n and k values seen with our plasma enhanced chemical vapor deposition (PECVD) SiN_x without (solid lines) and with (dashed lines) laser ablation for the samples ablated in figure 5.4. Both conditions experienced KOH etching, but we have found no significant etching of our SiN_x films in the 4% room temperature KOH used for this process. Fitting was done with Complete Ease software made by Woolam for the 50 nm thick film and data was acquired with a variable angle spectral ellipsometer. For the non-laser patterned SiN_x film a model

with a thickness of 50 nm, a surface roughness of 0, and a mean square error (MSE) of 10.8 was produced. If we assume the residue is a part of the SiN_x film, fitting produces a model 50 nm thick, but with an average surface roughness of 16 nm, and an increase in the MSE to 12.1. The most notable change in the modeled film is the enhanced n and k values, implying an increase in the silicon content of the film. This increase could be due to a change in the SiN_x film itself or be the result of a silicon rich debris on the surface. The sparse coverage and ambiguous nature of the residue makes it challenging to fit it independently and accurately of the SiN_x film. Especially due to possible de-polarization effects induced by the rough surface and residue [24,64,65], necessitating further characterization.

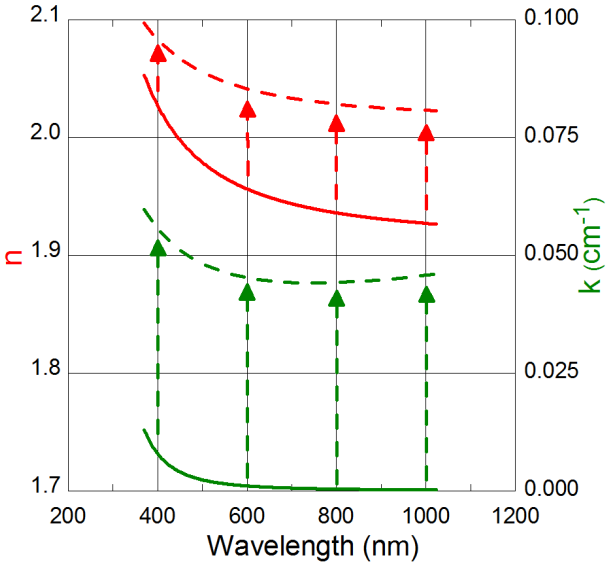

Figure 5.5: Index of Refraction (N) and Absorption Coefficient (K) Plot of a 50 Nm Thick SiN_x Film on a Polished Surface Before (Solid Line) and after (Dashed Line) Laser Processing. The Arrows in the Graph Denote the Change in N & K Post-laser Processing.

Changes to the underlying film structure (SiN_x) and the generation of a residue on the surface of the film should manifest itself as a change in the bond structure of the film(s), and manifest as a change in the absorbance signal in the Fourier Transform Infrared (FTIR) spectroscopy). Measuring this change will give information on any degradation in the SiN_x film and clarify the bond structure of the residue. Figure 5.6 depicts the signal profile for (a) Si-N stretching mode at 840 cm^{-1} and (b) Si-H stretching mode at 2160 cm^{-1} for before (solid black) and after laser processing. The complete signal overlap observed for the Si-N stretching mode in (a) suggests that the SiN_x film remains largely (if not entirely) unaffected by the laser plasma. The decrease in the signal seen for the Si-H stretching mode in (b) may not be due to Si-H bond breakage –as a Gaussian fit of the signal before and after laser processing shows an unchanged peak location and an unchanged full width half max– but rather is due to a change in the substrate from repeated pulse overlap, resulting in vaporization of a small volume of the substrate beneath the films. A change in bond structure of the substrate would alter the background signal of the substrate used for subtraction, causing a drift in the measurement. Otherwise, changes in the apparent signal in the 840 cm^{-1} stretching mode could indicate a loss of hydrogen and/or the creation of a microcrystalline film [66–69].

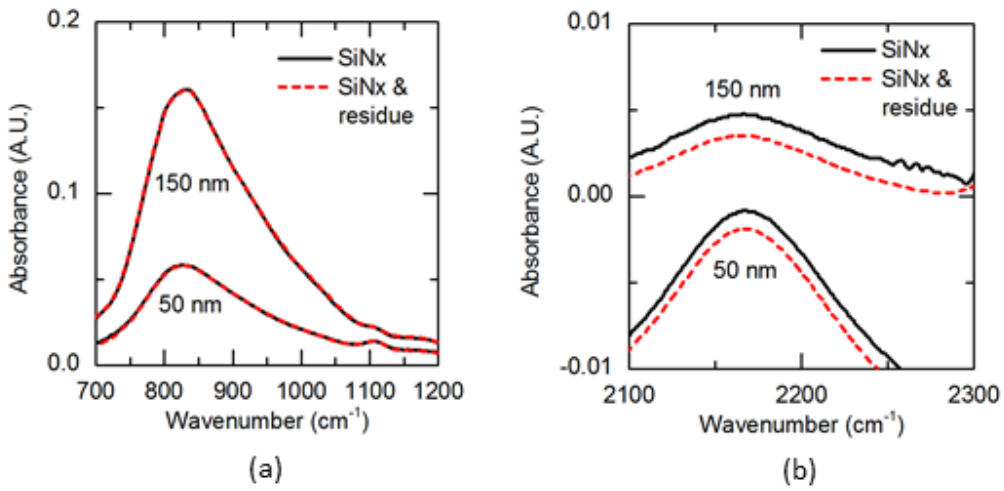

Figure 5.6: Fourier Transform Infrared (FTIR) Spectroscopy of SiN_x after Mask Removal, Before (Solid Black Lines) and after (Red Dashed Lines) Laser Scanning. (a) Si-N Stretching Mode (840 cm^{-1}) 50 nm and 150 nm Thick SiN_x Films and (b) Si-H Stretching Mode (2160 cm^{-1}) in 50 and 150 nm SiN_x Films

Inspection of the surface of the polished substrates with an SEM in figure 5.7 of the laser ablated regions shows the expected residue, but also shows a shade variation in the shape of the laser pulse throughout the wafer. In area 1 of (a) the periphery of the laser spot is visible as a dark-light intensity variation, where the center of the pulse is dark, and the periphery of the pulse is light. In area 2 of (b) there appears to be more dark variation than what was seen in area 1, and ripples are visible beneath the surface. This sub-surface shade rippling is the onset of sub-surface damage and a pre-cursor to the behavior seen in area 3 of (b). Film delamination and sub-surface c-Si vaporization skew the FTIR measurement by changing the bias introduced by the substrate during the measurement, causing downward shifts such as the one seen in 5.6 (b).

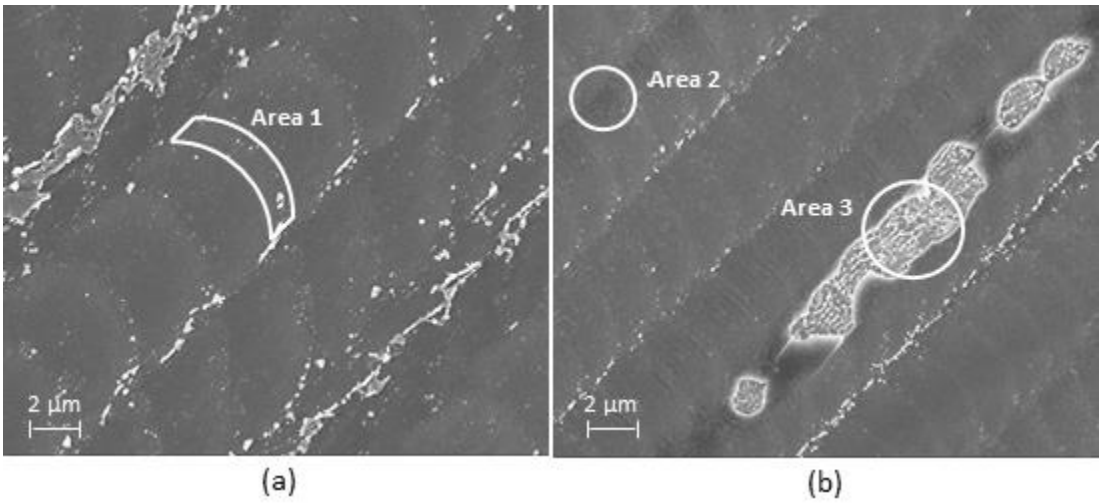

Figure 5.7: SEM Images of Laser Residue on 150 nm of SiN_x on a Polished Surface with 50% Pulse Overlap, Post-mask Removal (a) with Intensity Variation in Area 1 (b) with Large Intensity Variation in Area 2 and Definitive Defect Generation in Area 3

d) Scanning Transmission Electron Microscopy

Given the inconclusive results observed with ellipsometry and FTIR, we characterized a portion of the film stack in a cross-section using Scanning Transmission Electron Microscopy (STEM) and Electron Energy Loss Spectroscopy (EELS). We selected a region that did not show sub-surface rippling for characterization. The region of interest for EELS imaging is boxed in figure 5.8 (a) and shown in (b). The substrate and the residue circled and labeled 2 (illustrated in red) both showed strong silicon signals, while the SiN_x region showed a mix of silicon and nitrogen signals (colored in yellow). The SiN_x region was also the only region to show any nitrogen signal. The residue circled and labeled 1 showed a strong carbon signal, and the platinum region showed a moderate carbon signal from the deposition process. The lack of nitrogen and carbon signal in residue 2 affirms that there is no significant secondary ion generation

from the laser plasma, due to the lack of incorporation in the residue. The high carbon composition of residue 1 and the absence of oxygen in the bulk of the residue (which was also measured with EELS), indicates that the residue was not deposited via the laser plasma, but is rather a contaminate from atmosphere or handling [70–73].

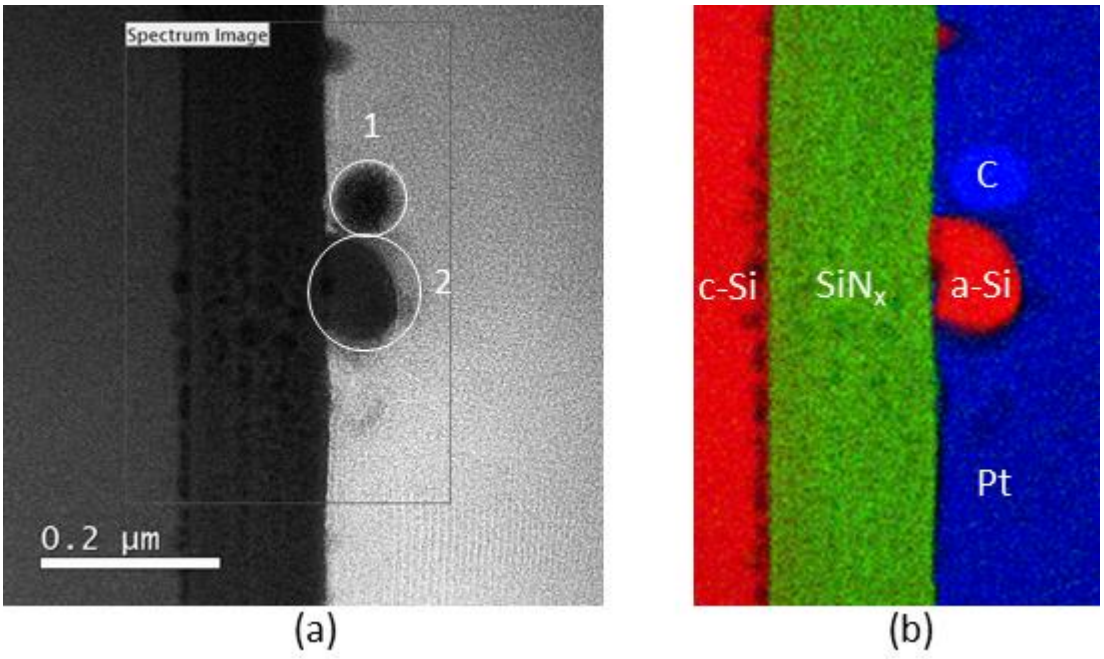

Figure 5.8: STEM and EELS of Laser Residue (a) STEM with Spectrum Imaging Shown, (b) Colorized Spectrum Map Generated from EELS Data

The composition of the residue does not explain the resilience of it to KOH etching however, if the material is thick compared to the mask then it would not etch in the same time as the mask. Additionally, if the residue is semi-crystalline in nature, it would etch at a slower rate than the a-Si mask. Figure 5.9 (a) shows a high resolution TEM of the targeted silicon residue and the selected-area electron diffraction of this region is shown in (b). The circular rings in (b) indicate an amorphous material and the series of bright spots indicate lattice fringing. The bright spots are electron diffraction peaks that correspond to polycrystalline material, and indicate the presence of

crystalline grains [73–76]. The rapid re-deposition of a-Si caused film stress and resulted in the nucleation of crystals with a stronger bond structure than that of the a-Si mask, causing a persistent residue that can withstand the dilute room temperature KOH etch.

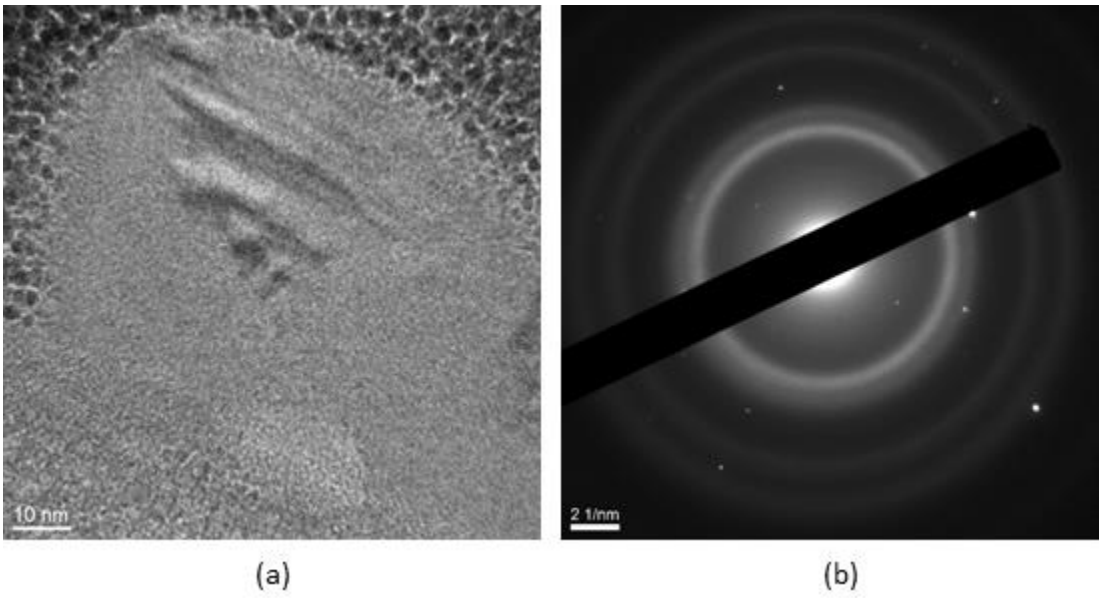

Figure 5.9: Laser Residue (a) TEM and (b) Selected-area Electron Diffraction Showing Amorphous Rings and Signal from Different Crystal Orientations

CHAPTER 6

CONCLUSION

The need for photovoltaics in generating renewable power is clear. Regions without power and with water shortages could take advantage of the minimal required infrastructure. To that point, the minimization of cost will certainly impact the availability and practicality of the technology. As a precious earth metal, silver will likely be expensive compared to cheaper alternatives. There is a need for a metallization scheme that produces high efficiency solar cells without the use of rare earth materials.

Laser processing combined with electroplating, or more specifically light-induced-plating, could provide a means for creating cost effective and practical metallization. A direct ablation process of the passivating thin films was explored, and found to produce an undesirable surface with the available lasers. An alternate approach that uses an a-Si mask and chemical etch selectivity to pattern the passivating thin films was developed to produce more desirable results.

The thickness, temperature, ablation energy, and robustness of the a-Si etch mask was explored and validated. A limitation of the process with pulse overlap and defect generation was identified, thoroughly characterized, and reduced via stabilization of the laser. Coupled with a series of varied depth diffusions that were developed, the issue of cell shunting was resolved for this patterning process.

Further, the fidelity of the opening created by the laser ablation process was evaluated and found to be partially obscured by a plasma generated residue. We identified the mechanism responsible for the residue generation as Si ion trapping. Detailed characterization identified that the material was comprised of silicon, with no

incorporation of secondary ions from the laser plasma. The short plasma process that occurs during the a-Si mask removal was found to produce a poly-crystalline material that is resilient to the mask etched used to strip the mask following dielectric patterning. The high arrival angles present in a textured substrate were identified as a site for ion accumulation due to their high arrival angle. While the residue does reduce contact opening width, it was not found to interfere with any metallization process so there is no need for its removal.

With the development of a damage free patterning process for the removal of dielectric layers on textured surfaces we have created a new means for industrial scale metallization of solar cells. For industry, this means there exists an industrially scalable patterning process that enables non-silver metallization of silicon solar cells. Once photovoltaic production reaches the point of enhancing the market volatility of silver beyond acceptable cost limits, it will be necessary to use this alternate metallization strategy. Further, the use of Ni/Cu metallization stacks will allow for further improvements in the passivation quality of devices due to the increased allowable doping range enabled via NiSi formation.

Further work to test the applicability of this process to textured multi-crystalline wafers is necessary to ensure its industrial relevance. Film conformity of the passivating layers, a-Si masking layers, and the enhancement to the process range over which the films may be removed via laser ablation all indicate that such an application is well within the scope of the developed patterning process.

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