

SMART DC/DC WALL PLUG DESIGN FOR THE DC HOUSE PROJECT

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Master of Science in Electrical Engineering

by  
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## ABSTRACT

### Smart DC/DC Wall Plug Design for the DC House Project

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The present day duplex wall receptacle in the United States provides 120Vrms AC at 60Hz, which comes from a standard set for AC loads by the National Electrical Manufacturers Association. With a DC system, such as what is used in the DC House project currently being developed at Cal Poly, providing DC power to DC loads presents a technical challenge due to the different required DC operating voltages of the loads. This thesis entails the design and construction of a Smart DC/DC Wall Plug, which can automatically adjust its output voltage to match any required DC load voltages. In the DC House implementation, renewable energy sources generate power to feed a 48V DC Bus. The Smart DC/DC Wall Plug converts power from the 48V bus to the appropriate voltage and power levels needed by the DC loads. The Smart DC/DC Wall Plug relies on load current detection, and uses a 10-bit digital potentiometer and a programmable current DAC to adjust the feedback network, thereby changing the output voltage. A dual channel 100W PCB prototype utilizing a STMF302R8 microcontroller is implemented for this design while confining to the NEMA wall outlet form factor. Results of hardware test verify the functionality of the Smart DC/DC Wall Plug in producing the required DC load voltages. Technical issues during the development of the Smart DC/DC Wall Plug will be described, along with suggestions to further improve from the current design.

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## Chapter 1

### INTRODUCTION

Wall plugs were established to enhance the convenience for people to access electricity to power lights, home appliances, electronics, computers and much more. The initial innovation of the wall plug began in the late 1800s as electricity became an emerging medium to provide power for the public. In efforts to help with the safety and convenience of accessing electricity, Harvey Hubbell designed the “separable attachment plug”. It was a two prong plug that can attach and detach to a socket plug to make accessing electricity power more convenient. Further advancements with the Harvey Hubbell separable plug design was done by Philip Labre, who added a third ground prong. An additional prong tied directly to ground reduces the hazard of electrical shock in case of an accidental short circuit. The Labre design was the model for the current wall receptacle [1]. In the North America, the National Electrical Manufacturers Association (NEMA) established the wall receptacle standard [2]. NEMA constitutes the dimensions and electrical specification of the wall receptacles that are in place in residential, commercial and industrial buildings. The design, shown in Figure 1-1, is the ubiquitous wall outlet marked with specific dimensions that all power plugs for devices conform to today.

PLUG AND RECEPTACLE  
 125 volts, 50 amperes, 2 pole, 3 wire, Grounding type

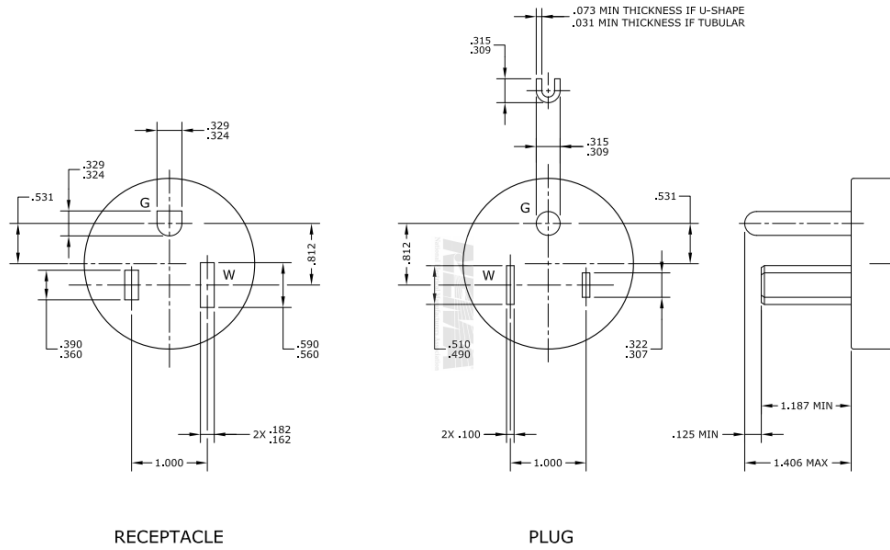


Figure 1-1: NEMA Dimension for the Common Wall Receptacle [2]

The common wall receptacle in North America is standardized to output 120 Voltage Alternating Current operating at 60 Hertz. The use of AC voltage has been adopted since Nikola Tesla developed the polyphase AC power distribution system and later demonstrated that it could deliver power to both lights and machines in the world fair at Chicago in 1893. Alternating Current was favored over Direct Current due to its long-distance power transmission capabilities and flexibility for voltage transformation [3]. The infrastructure today for power distribution have been established to use Tesla’s AC model and developed AC transmission lines to distribute power across great distances. This system brings power generated from utility companies hundreds of miles away to homes and buildings. The infrastructure is scalable to serve majority of the people today and allows people to receive AC electricity directly from wall outlets for energy.

AC, however, is not the form of power that is used internally in many of the devices and appliances today. The 120 AC voltage drawn from the wall outlet consequently has to be rectified and converted into a lower and usable DC voltage through the respective device's power supply. These specified power supplies, commonly seen as power blocks and wall attachments, specify the input AC voltage and output DC voltage that is rated to run the device. Among many of these loads include desktop computers, LED lights, and electronics that convert AC power to DC power. Almost all manufactured power supplies for devices use the 120V AC as the input source, but they do not output one common DC voltage level. Typical DC voltage levels are 5V for small handheld devices that are USB powered and 12V for larger electronics, but there is no set standard for DC voltages and devices can range to use lower DC voltages to much higher DC voltages. A survey was conducted from Amazon's website and the #1 best sellers were chosen from different categories. These devices' respective power supplies were evaluated to scope what output DC voltages these popular devices are using. The DC voltages for the selected items are listed in Table 1-1 [4]. These electronics require DC to operate due to the fact that these devices are constantly on and the power electronics incorporated in a lot of today's devices and electronics items are power efficient dealing with DC voltage conversions. Exchanging the AC infrastructure to entirely a DC system would be more appropriate for a more economical and energy efficient system.

Table 1-1: DC Voltages for Select Items

Load Type (Amazon Best Seller)	4.5V	5V (USB Power)	9V	12V	15V	19.5V
Night Light (Arova Motion Activated Toilet Nightlight)	X					
Cell Phone Wall Charger (Anker 2-Port 24W USB Wall Charger PowerPort 2)		X				
Home Security Camera (Nest)		X				
Digital Clocks (RCA Digital Alarm Clock)			X			
Computer (Acer Aspire ATC-780-AMZi5 Desktop 300W)				X		
Monitor (HP Pavilion 22cwa)				X		
Table LED Lamp (TaoTronics LED Desk Lamp)				X		
Door Bell Kit (Arova A1 Wireless Door Bell Kit)				X		
Home Automation Controller (Amazon Echo)					X	
Laptop (HP 15-f222wm)						X

The idea of DC House is geared towards creating a small independent power grid entirely on DC [5]. In the DC house project, electricity is generated locally and is used directly. Power generation from solar panels, DC hydro generators and DC wind powered generators produce DC energy which is then stored locally in batteries. This way, DC power would not have to be transmitted and become lost due to power loss from traveling through resistive wires. Figure 1-2 represents the concept of the DC house [5]. The DC system eliminates the

dependence of utility companies and caters to people in rural areas where accessing electricity from the grid is not available. DC will be the source of power for the wall outlets and would be the appropriate form of energy to supply the load.

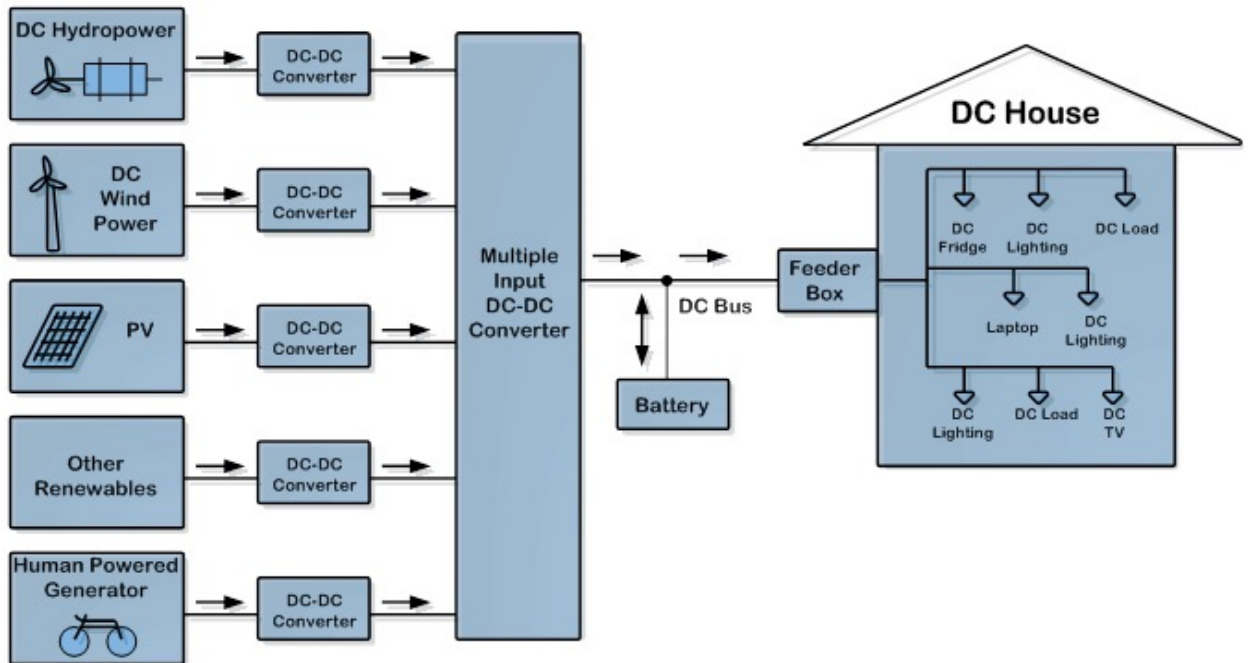


Figure 1-2: DC House Block Diagram [5]

## Chapter 2 BACKGROUND

### 2.1 Traditional DC Microgrid System

The Smart Wall Plug Project is a subsidiary to the DC House Project at Cal Poly State University. The DC house project is a residential scale “microgrid” system that is sourced from photovoltaics, wind power, hydro generators and other renewable sources. These sources generate DC power, which is stored and used to power the appliances and lighting in the house. Traditionally wall receptacles powered by renewable energy would obtain its power after a DC to AC inversion process that transforms the energy to conform with the standardized AC power at 120 Volts rms, or 170 Volts peak. On an external switching mode power supply, the voltage 120  $V_{rms}$  AC power is rectified and filtered to result a DC voltage at approximately 170V DC. The resulting 170V DC is then stepped down to meet the voltage specification of the device. This 3-stage process [3] requires multiple power converters and introduces power losses that leads to poor overall system efficiency. Additionally, multiple power converters add to more cost and complexity. Shown in Figure 2-1 is the energy transfer process from the energy sources to the load. Each power conversion stage is not 100 percent efficient due to power losses from non-ideal components, operational imperfections and other factors. These issues pose disadvantages towards conforming towards the conventional way of accessing power from the wall receptacle.

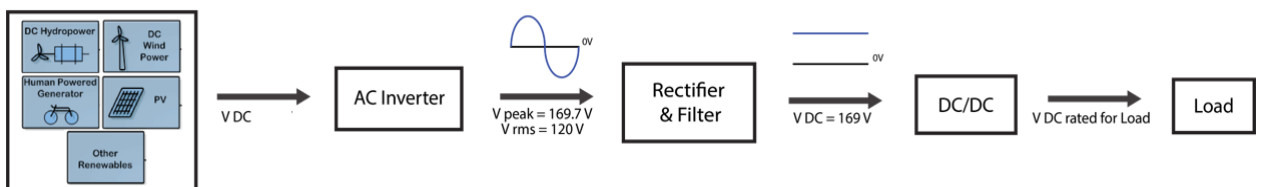


Figure 2-1: DC Sources to Load Flow Diagram

Ideally the power would stay in the same form and be accessed directly.

Eliminating the intermediate AC stage will help with reducing costs, complexity and power losses [3]. However, almost all home appliances and devices are designed to use 120 V<sub>rms</sub> AC as the power source. This is despite the fact the internal electronics of these appliances are mostly operating on DC circuits. With the recent increase in use of renewable energy sources especially solar panels, DC appliances, lighting and devices have gradually become commercially available. However, these DC loads vary in terms of their operating voltage. Therefore, the issue with eliminating the AC stage would be to meet the power requirements for any existing DC load. For residential DC electricity to work, its electrical distribution system must be able to accommodate for various DC voltage levels to run different types of DC loads. Of course, this is not a realistic solution as it would require several DC-DC converters with their corresponding wall plug to provide the different DC voltages. Thus, a better solution would be to have a universal wall plug that is capable of outputting the appropriate DC voltage as required by the connected load.



## 2.2. Smart Wall Plug Objective

The purpose of the Smart DC Wall Plug is to carry the same convenience as using the common AC outlets. The Smart DC Wall Plug powers a DC device by simply plugging the device through its power cable to the DC receptacle. To make the proposed wall plug easily adoptable, the wall plug will share the same standardized look from existing wall outlets that are known to provide 120VAC at 60Hz. The ubiquitous three prong receptacle will have different pinouts appropriate for DC power connection. In the AC outlet, shown in Figure 2-2, there is one GND and two AC power lines. DC uses only two power connection, the positive rail and negative rail (which is usually GND). For the DC Wall Outlet, the AC receptacle will be rewired to meet the DC specification. The DC wall plug is inherently polarized and is crucial that the power cable is connected at the proper orientation to the plug. Reverse voltage protection will be implemented and the DC wall plug should not operate unless the proper orientation of the power cable is inserted.

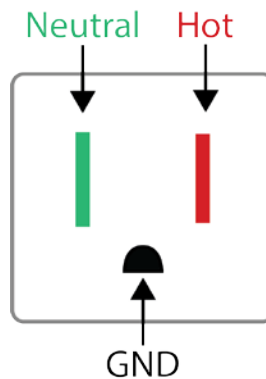


Figure 2-2: AC Receptacle Pin Out

For the DC House project, the DC bus operates at 48V and will need to be adjusted to mostly a lower voltage to power most of the DC loads. DC loads could range from cell phones, LED lights, speakers, cameras, computers, monitor displays and many

other electronic devices. Each of these devices requires different amounts of voltage to run properly. This consequently requires an implementation of a wide output DC-DC conversion range from 0V to 48V to meet load requirements. Additionally, a system which will detect and adjust the output voltage for different loads is required for the internal DC-DC converter of the proposed wall plug to supply the appropriate level. This further implies the implementation of a smart DC power supply, which will have the need for a microcontroller with the ability to detect and actuate the output power.

### 2.3. DC-DC Conversion Design Background

The method to transform one DC voltage to another DC voltage with the most flexibility and efficiency is through a switching mode power converter. The Buck Converter is an example of switching mode power converter that can transfer the power from the input to the output at a lower voltage level than the source. The power stage of the Buck circuit is shown in Figure 2-3.

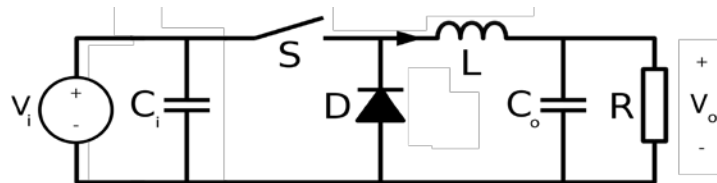


Figure 2-3: General Buck Converter Circuit Diagram

The operation of the buck converter is governed by the charge and discharge of the energy storage elements, mainly the inductor. The switch,  $S$ , is an electronic device that determines the charge and discharge cycles of the energy storage elements and is responsible for setting the nominal output voltage. The duty cycle,  $D$ , is the percentage of time the switch is turned on compared to the period of the switching cycle. At a duty cycle between 0 and 1, the average output voltage will be a fraction of the input voltage following the transfer function:

$$V_{out} = D * V_{in}$$

$V_{out}$  – Output Voltage

$D$  – Duty Cycle

$V_{in}$  – Input Voltage

The above equation indicates that changing the output voltage from the buck converter circuit requires an adjustment to the duty cycle of the switching network. To do this, the buck converter employs a feedback network whose output samples that of the output voltage and feeds into a buck controller that has an internal reference voltage. The duty cycle is then being adjusted based on the difference between the feedback network voltage and the internal reference voltage. For the proposed wall plug, the change of duty cycle has to be performed rapidly to prevent a long delay in power up a DC device. One way to do this is by using a microcontroller. For the proposed smart wall plug, a microcontroller with analog input would be able to detect a load by the voltage across a sense resistor on the output. The microcontroller will update to a higher output voltage setting until voltage on the sense resistor is detected. Then the microcontroller will make appropriate modifications to the feedback network to configure to the loads nominal output voltage. Along with a load detection system, all the components will need to be sized adequately for the maximum voltage and current operating conditions. To improve on efficiency, the diode can be replaced with a synchronous rectifier MOSFET to reduce the power loss due to the diode forward conduction. Also, multiple input and output filters are required to clear out AC characteristics and to form pure DC power produced by the wall plug.

#### 2.4. Previous Work

The Smart Wall Plug project is a variable DC voltage receptacle that detects and sets the appropriate nominal voltage for the load. This Smart Wall Plug thesis is a continuation of the project done by past Masters Students, Edward Sibal [6] and Kevin

Mendoza [7]. Improvements to the Smart Wall Plug will be targeted on the output load detection and actuation, wider output voltage range, and implementation to the DC house.

Edward Sibal started the design of the Smart Wall DC plug in 2012. His design was viable for select levels of output voltages, 3V to 12V in increments of 3V. The load detection relied heavily on multiple test cases to ramp up the voltage until it was enough to source a current. The shortcoming was that the output voltage does not reach the load's nominal value and would be at the minimum value. At the minimum voltage level, the receptacle will pose a risk to power the load. The overall project was in multiple parts and was not designed to fit the electrical box for implementation [6]. Kevin Mendoza, worked on improving the design from Edward Sibal and was able to create a single board that can fit in the electrical box enclosure [7].

For this thesis project, improvements to the previous smart DC wall plug designs will be made to enable a wider output range. The feedback network will be changed to control the adjustments through an injected current source to complement with the potentiometer control. Design of the proposed wall plug and computer simulation to verify the design will be conducted. Construction of the smart DC wall plug system will be performed and then tested whose results will be presented in this thesis report.

Chapter 3  
DESIGN REQUIREMENTS

The goal of the project is to design and construct a Smart Wall Plug which is a wall receptacle that provides a nominal output voltage for any load plugged into it. The Smart Wall Plug will detect the load plugged in from the outlet and output the appropriate voltage between 0V to 48V. Figure 3-1 shows the block diagram of the concept. The Smart Wall Plug simply is a single input and single output system that takes the 48 voltage DC bus line from the DC House battery as the input voltage source and outputs a voltage between 0V to its line voltage.

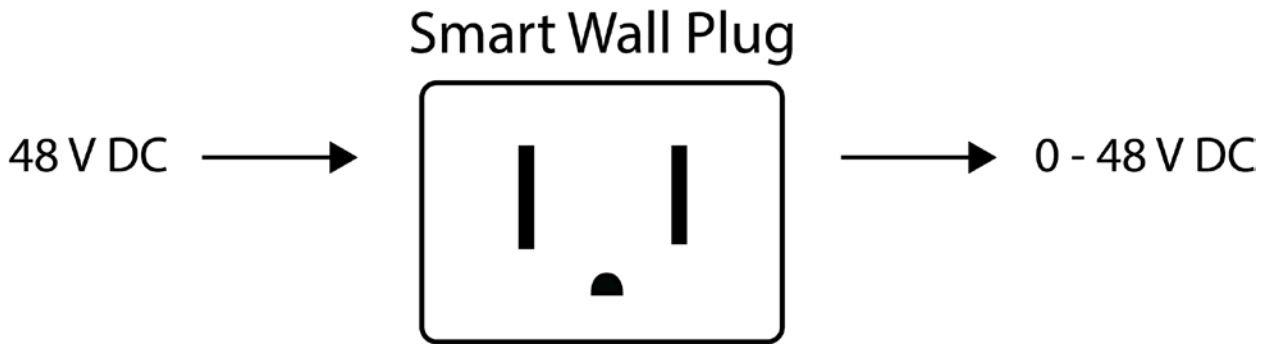


Figure 3-1: Level 0 Block Diagram

A more detailed diagram is shown in Figure 3-2 which describes the operation of the Smart DC Wall Plug. The 48V bus is the input and fuses are placed in between the line input and the DC/DC converters. The primary DC/DC converter is a step-down type switching mode power supply that converts the line voltage to any level between 0V to 48V while maintaining high efficiency. To aid with adjusting the output voltage of the DC/DC converter, a feedback loop is implemented with a microcontroller, a digital potentiometer and a variable current source circuit. The digital potentiometer and

variable current source are both methods to adjust the output voltage from the primary DC/DC converter. The digital potentiometer is a variable resistor that is set by the microcontroller and is a key component of the feedback network of the DC/DC controller. The digital potentiometer has the ability to change the resistance and affect the voltage seen at the feedback node of the DC/DC converter. The current source method adjusts the output voltage by injecting current to the feedback resistor. The injected current induces a voltage drop on the feedback resistor, thereby, manipulating the controller to adjust the output voltage. The microcontroller is responsible for detecting the load voltage and then determines the digital potentiometer and current source settings to adjust the DC/DC converter to the appropriate voltage.

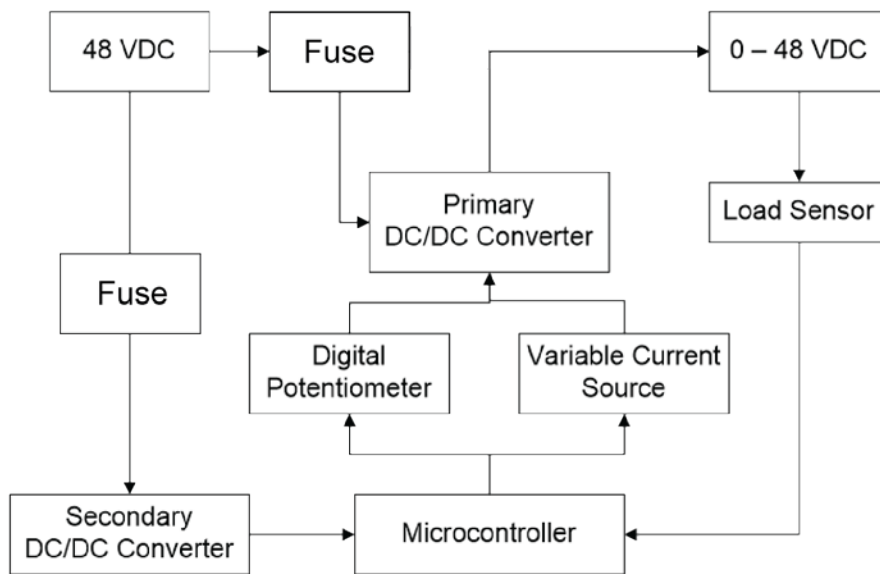


Figure 3-2: Level 1 Block Diagram

A secondary DC/DC converter is used to supply a fixed output voltage to power the microcontroller. The secondary DC/DC converter takes the 48V input and step-downs the voltage to the nominal required input voltage for the microcontroller. An additional feedback network involving a digital potentiometer and a variable current

source is not necessary for the secondary DC/DC converter because the output voltage does not need to be changed.

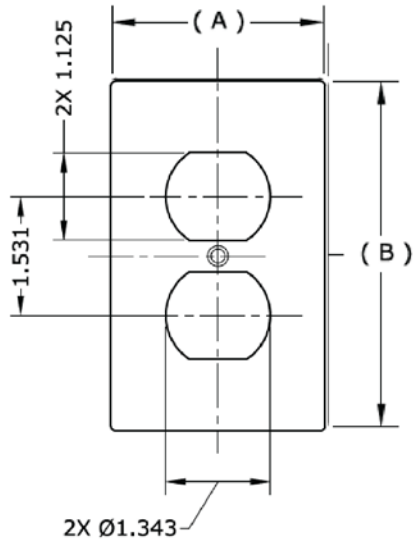
The electrical specification of the Smart DC Wall Plug is listed in Table 3-1. The input is specified at a fixed 48V supply and the output is a value in the range of 0V to the supply voltage. The output power is rated up to 100W, as the wall outlet should accommodate the maximum USB-C standard of 20V at 5A. The output current for the Smart DC Wall outlet ranges from .1A to 15A. The minimum output load should be about 0.1A to supply a sufficient load in order to acquire an adequate efficiency and proper functionality from the primary DC/DC converter. The peak load current is 15A due to the current limitation for existing wall receptacle products and the current ratings for common household circuit breakers. The target efficiency for the Smart DC Wall Plug is 85% at full load. Efficiency will vary depending on output current and how close to ideal the components used are. The targeted voltage accuracy error is 3% and the output voltage ripple is 5% to aim for an accurate and stable DC power supply characteristic.

Table 3-1: Target Design Specifications

Input Voltage	48V
Output Voltage	0 - Input Voltage
Output Voltage Ripple	< 5%
Output Current	.5A-15A
Output Power	Up to 100W
Steady State Voltage Percent Error	3%
Efficiency at Full Load	~85%

The physical design constraint will be based on the NEMA dimensions of a Duplex wall plate. The length and width of the wall receptacle is 4.87 inches by 3.12 inches as shown in Figure 3-3. The Smart DC Wall outlet will take the same physical dimension space from a wall set by NEMA. Since the vast majority of the wall receptacle used in residential homes and buildings adopt the duplex wall receptacle, the Smart DC Wall outlet will be implemented to have two systems to provide power to each wall plug. An electrical box enclosure, housing the two printed circuit boards, will be mounted behind the duplex wall faceplate. The depth of the electrical box must be enough to fit the two PCBs and the power components with some overhead room.





Duplex device

REFERENCE	MATERIAL	STANDARD DIMENSIONS	
		MIN	MAX
A	ALL	3.120	----
B	ALL	4.870	----

Figure 3-3: NEMA Specified Duplex Device Wall Receptacle [1]

Using the existing receptacle and plug configuration from the ordinary AC wall plug, the Smart DC Wall Plug will have same form factor but different pinouts. Shown in Figure 3.4 is a diagram that illustrates the wire connections between the printed circuit board and the front duplex faceplate. Wire gauge size of 12 and PCB trace width of 683 mil size will be used in order for the Smart DC Wall Plug to output up to 15A of current [8]. The “hot” wire will be noted as the positive polarity DC power line. The neutral wire and ground wire will be linked together and is grounded. The plug itself will be able to plug straight into the receptacle, although modification will be required to the device itself to bypass the AC to DC conversion stages.

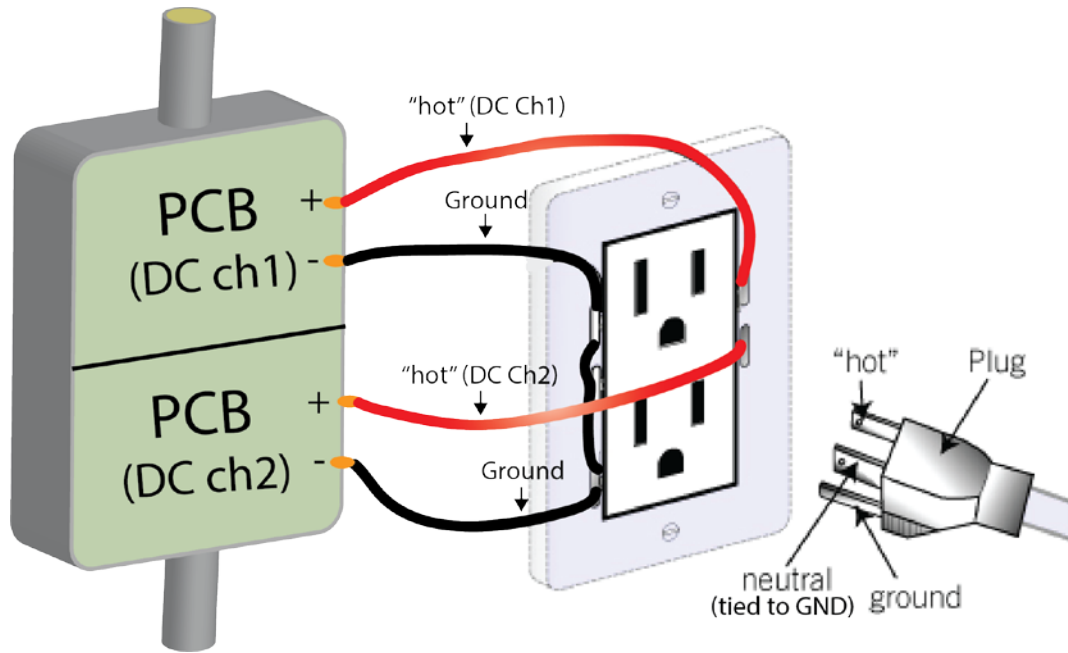


Figure 3-4: Smart DC/DC Wall Plug Connections

## Chapter 4

### DESIGN AND SIMULATION RESULTS

#### 4.1 Solution Statement

The objective for the 3<sup>rd</sup> iteration of the smart wall plug is to build upon and extend the past master thesis on the smart wall plug. The last thesis project of the smart wall plug produced a single channel outputting up to 15 V capable of 50 W of power. The feedback control involved a digital potentiometer to achieve a variable output voltage. The previous generation smart wall plug was able to detect the load voltage but would usually set to the load's minimum voltage requirement; thus, reducing system's efficiency due to the higher load current being pulled at the minimum input voltage operation. This iteration of the smart wall plug aims for a wider output voltage range, a higher power rating, two channels, an additional feedback adjustment control using a current source and a different algorithm to dynamically set the output voltage to the nominal load voltage.

#### 4.2 Controller Selection

The design of the Smart Wall Plug project begins with selecting the switching mode power supply controller. The controller must be capable of the target design specifications shown in Table 3-1. The controller must be rated above the voltage and power ratings to accommodate margin. When the output voltage levels are lower than 50% of the input voltage level, the low side switch will be conducting more than high side switch. A synchronous rectifier should be used instead of a diode to achieve more efficiency. For the compensation control scheme, current control mode controllers offer better transient responses and are easier to design for a compensator to achieve higher bandwidth and adequate phase margin than a voltage control mode controller.

The LTC3892 is a 60 Volt 2-Phase Synchronous Step-Down DC/DC Controller that offers high performance step down conversion capable up to 125 watts per phase without airflow [15]. Each channel can be independently configured and each can serve to be an output for the dual wall receptacle layout. The LTC3892 is also a current controlled mode controller which implies better load regulation and transient response than a voltage controlled mode controller. An advantage in selecting the Linear Technology part, LTC3892, is the ability to test the part with an accurate model in LTspice. LTspice serves as a simulation tool to develop the schematic for the project. The LTC3892 chip comes in two packages, a quad flat no lead (QFN) and the thin shrink small outline package (TSSOP). The LTC3892-1 in the TSSOP package was selected for ease of soldering, 4 fewer pins and a lower thermal resistance compared to the QFN package for the smart wall plug converter.

#### 4.3 Controller Design

Working with the LTC3892-1 controller, there are 28 pins to set the controller state of operation. The LTC3892-1 is not a fully integrated buck regulator, which means the controller requires discrete components and configuration to the control pins. Shown in Figure 4-1 is the LTC3892-1 package and pin out from the datasheet [9]. Fortunately, the controller is a two-phase controller, where the design for the power conversion pins from one phase can be repeated on the same pins in the second phase. The other pins are used for input connection and controller setup pins. View Table 4-1 to see the breakdown of pins. Each pin definition can be found in the LTC3892-1 datasheet.

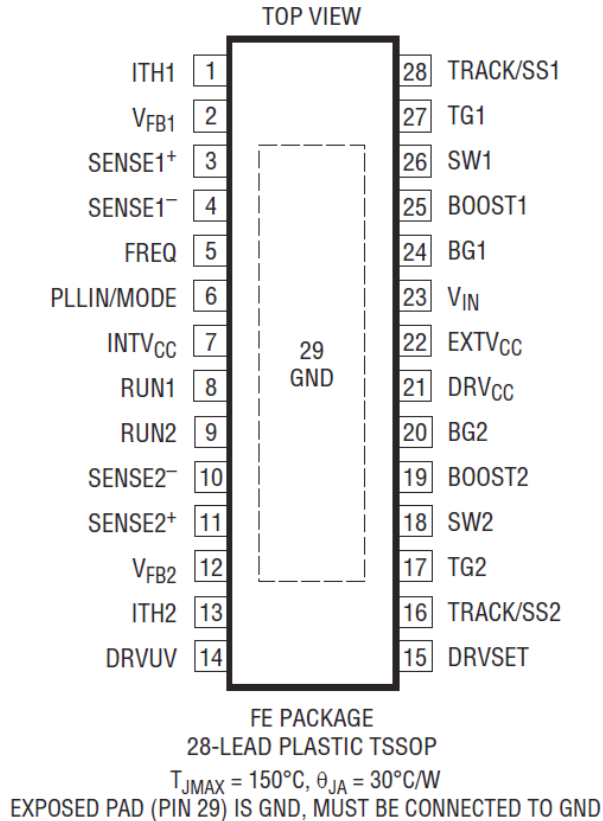


Figure 4-1: LTC3892-1 Pin Out [9]

Table 4-1: LTC3892-1 Pin Breakdown

<b>Power Pins (x1)</b>	<b>V<sub>IN</sub>, GND</b>
<b>Controller Set Pins (x1)</b>	FREQ, PLLIN/MODE, DRV <sub>CC</sub> , INTV <sub>CC</sub> , DRVSET, DRVUR, EXTV <sub>CC</sub>
<b>Symmetrical Phase Pins (x2)</b>	RUN, TG, BOOST, SW, BG, SENSE+, SENSE-, V <sub>FB</sub> , ITH, TRACK/SS

Selecting the frequency for the LTC3892-1 is a fundamental design consideration for the smart wall plug project. The frequency of the internal oscillator in the controller governs the switching frequency of the switching network for the power stage. The tradeoff between selecting a low frequency is the component sizing for the inductor and capacitor will increase and selecting a high frequency will introduce more switching losses in the synchronous switches. The smart wall plug is constrained on the

dimensions of a NEMA standard dual receptacle wall plug as shown in Figure 3-3. Operating at a higher frequency reduces the size requirement of the inductor and capacitor and smaller component values correlates to smaller physical dimensions of the components. The size of the project is more important than efficiency so a high frequency is more desirable.

The frequency of the controller is set through the FREQ pin in the LTC3892-1 either connecting the pin to an internal voltage regulator pin, INTV<sub>CC</sub>, to ground or to a resistor to ground. Tying the FREQ pin to INTV<sub>CC</sub> of the controller configures the frequency to 535 kHz, and connecting the FREQ pin straight to ground will configure the frequency to 350 kHz. The frequency can be set between 50 kHz to up to 900 kHz by connecting a resistor from the FREQ pin to ground. The resistor to frequency relationship is shown in Figure 4-2. The consideration of frequency variation due to temperature and tolerance distinguishes whether to use a resistor or the internal voltage source to set the frequency. Resistors are prone to thermal noise and would change resistance due to temperature. Typical thin film SMD resistor has a 100 ppm/C resistance variation to temperature and are tolerated to 1% nominal resistance. Looking at the datasheet shown in Table 4-2, using a resistor at 65 kΩ will have a maximum 130 kHz frequency variation whereas connecting the FREQ pin to the INTV<sub>CC</sub> will have a 100-kHz frequency variation. The FREQ pin to INTV<sub>CC</sub> is favored and the converter will run at a nominal 535 kHz. In the typical case, the oscillator frequency should exhibit the change of frequency due to temperature in Figure 4-3.

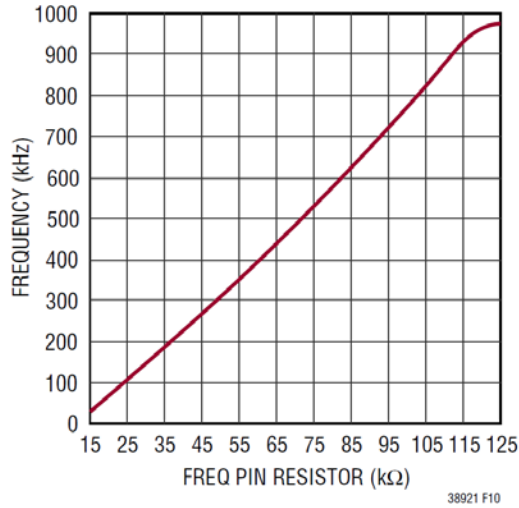


Figure 4-2: Resistor Selection for Switching Frequency [9]

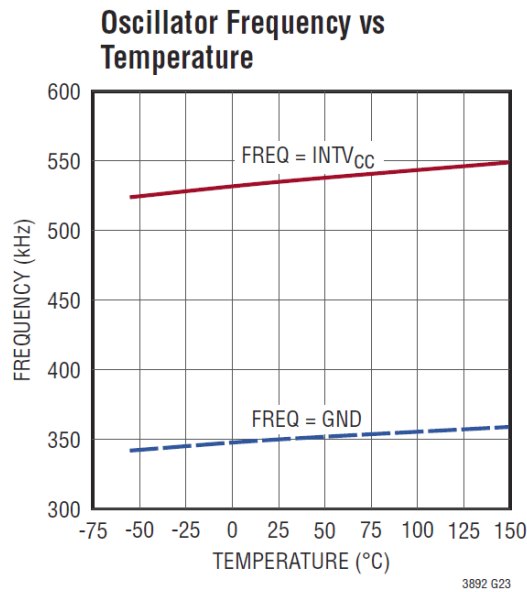


Figure 4-3: Frequency Variation due to Temperature at INTV<sub>CC</sub> and GND [9]

Table 4-2: Frequency Variation Comparison [9]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Oscillator and Phase-Locked Loop</b>						
f <sub>25kΩ</sub>	Programmable Frequency	R <sub>FREQ</sub> = 25kΩ, PLLIN/MODE = DC Voltage		105		kHz
f <sub>65kΩ</sub>	Programmable Frequency	R <sub>FREQ</sub> = 65kΩ, PLLIN/MODE = DC Voltage	375	440	505	kHz
f <sub>105kΩ</sub>	Programmable Frequency	R <sub>FREQ</sub> = 105kΩ, PLLIN/MODE = DC Voltage		835		kHz
f <sub>LOW</sub>	Low Fixed Frequency	V <sub>FREQ</sub> = 0V, PLLIN/MODE = DC Voltage	320	350	380	kHz
f <sub>HIGH</sub>	High Fixed Frequency	V <sub>FREQ</sub> = INTV <sub>CC</sub> , PLLIN/MODE = DC Voltage	485	535	585	kHz

#### 4.4 Component Sizing

The component sizing involves calculating the minimum values for the discrete components in the synchronous buck topology. The main components of the buck synchronous topology include an input capacitor, a high side switch, a low side switch, an inductor and an output capacitor. The principle of sizing the component is to have all the components rated appropriately to avoid blow outs of the components or shorts, and for performance to achieve low ripple and high filtering. Having a variable output voltage means different conditions of the converter with varying duty cycles and varying component values. Therefore, all conditions must be calculated to find the worst case rated values required to meet design specifications. Table 4-4 displays the component sizing specification across the different output voltage conditions. The worst-case values are highlighted in yellow and are used to select component values.

The high side and low side switches used for the LTC-3892-1 are N-Channel MOSFETs. Each transistor must be rated at least the input voltage, 48V. The current through each transistor will vary depending on the duty cycle of the PWM gate drive signal from the LTC3892-1 controller. Table 4-3 displays the current and voltage rating for the switching network. For an output voltage configuration below 50% input voltage, the low side switch will be conducting more and for an output voltage configuration greater than 50% of the input, the high side switch will be conducting more. Since the output voltage ranges from 3.3 V to 36 V, both the high side and low side transistors can be the same. For synchronous operation, a schottky diode is added in parallel to the low side switch to reduce conduction loss from the low side switch's internal body diode during dead time. Desirable characteristic when selecting a MOSFET is to look for low drain to source on resistance and low gate charge values for efficiency. Additionally, the switch should inhibit low thermal resistance and the appropriate threshold voltage for the controller to drive the switch into saturation.



Table 4-3: Current and Voltage Rating for the Switches

	Current Rating	Voltage Rating
<b>High Side Switch</b>	$I_{out} * D$	$V_{IN}$
<b>Low Side Switch and Schottky diode</b>	$I_{out} * (1 - D)$	$V_{IN}$

The inductor serves as the key component for the DC/DC step down conversion. The inductor stores current and maintains continuous current to the output. A design criteria to size the inductor is to identify the minimum load and calculate the critical inductance to maintain continuous conduction mode, where the current is always positive [10]. At minimum load condition, the inductor peak to peak current ripple must be smaller or equal to two times the average output current. The inductance can be solved from the  $V_L=L di_L/dt$  equation when substituting the on time of the high side switch, the voltage across the inductor when the high side switch is on and the targeted inductor peak to peak current ripple. The resulting critical inductance equation is shown in Equation 4.1. Beware of oversizing the inductor because higher inductance will cause a slower change in current and will increase the transient response time. The inductor selected for the project should also be shielded, low profile, low DCR and rated to handle the maximum load current. The inductance selected for the converter is a 75  $\mu$ H IHLP inductor from Vishay.

$$L_C = \frac{V_{IN} * (1 - D) * D}{2 * f * I_{outmin}} \quad (4.1)$$

$L_C$  – Critical Inductance  
 $V_{IN}$  – Input Voltage  
 $D$  – Duty Cycle  
 $I_{outmin}$  – Min Output Current  
 $f$  – Frequency

The input capacitor, also known as the bulk capacitor, is necessary to decouple the input's AC components and hold the input voltage from line disturbances. The capacitor must be sized to hold the charge during changes in input voltage. Stemming from the  $Q=C\Delta V$  equation, the capacitance can be solved from calculating the total charge from the current through the capacitor and the change in input voltage [10]. The equation of the input capacitor is shown below in Equation 4.2 [10]. The input capacitors were selected to be electrolytic and ceramic capacitors, placed in parallel to achieve a higher input capacitance and to reduce the equivalent series resistance. The input capacitors must also be rated with a voltage rating of at least the input voltage and have the appropriate  $I_{rms}$  current rating.

$$C_{in} = \frac{D * I_{outmax} * (1 - D)}{\Delta V_{in} * f} \quad (4.2)$$

$C_{IN}$  – Input Capacitance  
 $D$  – Duty Cycle  
 $I_{outmax}$  – Max Output Current  
 $\Delta V_{in}$  – Change in Input Voltage  
 $f$  – Frequency

The output capacitor functions as a decoupling cap to separate the AC components from the load. The output capacitance must be sized to the charge seen from the AC current decoupled from the inductor current. Equation 4.3 displays the equation for calculating the required output capacitance. The output capacitor selection should be electrolytic and ceramic based to achieve high capacitance and low ESR. Placing the capacitors in parallel will reduce the ESR and lower the output voltage ripple. The output capacitors require voltage ratings above 36V and a relatively high RMS current rating.

$$C_{out} = \frac{V_{out}(1 - D)}{8 * f^2 * L * \Delta V_{out}} \quad (4.3)$$

$V_{out}$  – Output Voltage  
 $D$  – Duty Cycle  
 $\Delta V_{out}$  – Change in Output Voltage  
 $L$  – Inductance  
 $f$  – Frequency

Table 4-4: Component Sizing due to Output Voltage

Vin(V)	Vout(V)	Duty Cycle	Vopp(V)	Iomax(A)	Iomin(A)	fsw(kHz)	Lmin(uH)	IswH(A)	IswL(A)	Cin min(uF)	Cout min(uF)
48	3.3	6.875%	0.00030	5	0.25	535	11.48832	0.34375	4.65625	124.656226	354.007363
48	5	10.417%	0.00050	5	0.25	535	16.74455	0.520833	4.479167	181.6899771	233.6448598
48	6	12.500%	0.00060	5	0.25	535	19.62617	0.625	4.375	212.9575545	194.7040498
48	9	18.750%	0.00090	11.11111	0.25	535	27.33645	2.083333	9.027778	659.1543354	129.8026999
48	12	25.000%	0.00120	8.333333	0.25	535	33.64486	2.083333	6.25	608.4501558	97.35202492
48	15	31.250%	0.00150	6.666667	0.25	535	38.5514	2.083333	4.583333	557.7459761	77.88161994
48	20	41.667%	0.00200	5	0.25	535	43.61371	2.083333	2.916667	473.23901	58.41121495
48	24	50.000%	0.00240	4.166667	0.25	535	44.85981	2.083333	2.083333	405.6334372	48.67601246
48	36	75.000%	0.00360	2.777778	0.25	535	33.64486	2.083333	0.694444	202.8167186	32.45067497

#### 4.5 Current Sense Resistor

A sense resistor voltage, placed in series with the inductor, is measured through the differential inputs of the converter, SENSE+ and SENSE– pins. The LTC3892-1 controller has a 75-mV maximum threshold to read the differential voltage across the sense resistor. The sense resistor must be sized to the appropriate value for the converter to read the maximum peak load current, shown in Equation 4.4. A sense resistor sized to 5 mΩ gives adequate margin to sense the load current up to 15 amps. The sense resistor should have very low resistance variation due to temperature and be rated appropriately with a power rating to handle maximum load currents.

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}} \quad (4.4)$$

*R<sub>SENSE</sub> – Sense Resistance*  
*V<sub>SENSE(MAX)</sub> – Max Voltage Sense*  
*I<sub>MAX</sub> – Max Output Current*  
*ΔI<sub>L</sub> – Change in Inductor Current*

The sense resistor also serves as a current sense input to the microcontroller for output or load voltage detection. The output current passes through the resistor and is translated to an analog voltage across the resistor. The analog voltage will vary in the mV range and must be amplified before being processed by the analog to digital converter in the microcontroller. The output voltage range should be within the ADC's full scale range. When designing the differential operational amplifier such as setting the gain, equation 4.5 is used while ensuring that the output swing of the op amp is accommodated. The op amp used for the smart DC/DC wall plug is the AD8422 and the swing is shown as 120 mV from the rails at 4.6 V between supply in Table 4-5 [11].

$$0 \leq Gain * (V_{IN+} - V_{IN-}) + V_{REF} \leq V_{FullScaleRange} \quad (4.5)$$

Table 4-5: Output Voltage Swing of AD8422 [11]

Parameter	Test Conditions/ Comments	AD8422ARMZ		
		Min	Typ	Max
INPUT				
Input Impedance			200  2	
Differential			200  2	
Common Mode			200  2	
Input Operating Voltage Range <sup>4</sup>	$V_S = \pm 2.3 \text{ V to } \pm 18 \text{ V}$	$-V_S + 1.2$		$+V_S - 1.2$
Over Temperature	$T = -40^\circ\text{C to } +85^\circ\text{C}$	$-V_S + 1.2$		$+V_S - 1.3$
OUTPUT				
Output Swing, $R_L = 10 \text{ k}\Omega$	$V_S = \pm 15 \text{ V}$	$-V_S + 0.2$		$+V_S - 0.2$
Over Temperature	$T = -40^\circ\text{C to } +85^\circ\text{C}$	$-V_S + 0.25$		$+V_S - 0.25$
Output Swing, $R_L = 10 \text{ k}\Omega$	$V_S = \pm 2.3 \text{ V}$	$-V_S + 0.12$		$+V_S - 0.12$
Over Temperature	$T = -40^\circ\text{C to } +85^\circ\text{C}$	$-V_S + 0.13$		$+V_S - 0.13$

#### 4.6 Control Loop Compensation

The LTC3892-1 is a current control mode controller and it requires a type II loop gain compensator design. The LTC3892-1 controller has a ITH pin which is the error amplifier output and the switching regulator's compensation points. The compensation network comprises of a resistor and capacitor network shown in Figure 4-4. The compensator introduce a zero and two poles to offset the poles introduced by the converter power stage to achieve a higher crossover frequency and more phase margin. The goal of the compensator is to improve the converter's stability and transient response due to load step changes. The current control mode system uses the feedback from the sense resistor to generate the voltage waveform into the PWM comparator and reduces the second order system into a single pole system. A guideline for the closed loop system is to aim for a bandwidth of 20% of the switching frequency. A wide bandwidth allows the system to quickly respond to sudden line and load changes. Another aspect is to achieve a phase margin greater than 45 degrees. Sufficient phase margin dampens undesired oscillations and shortens the transient settling time. Lastly the closed loop gain plot should exhibit high gain until gain crossover point and low gain after gain crossover point. These rules of thumb will ensure good line and load regulation for the system and minimal stability issues [12].

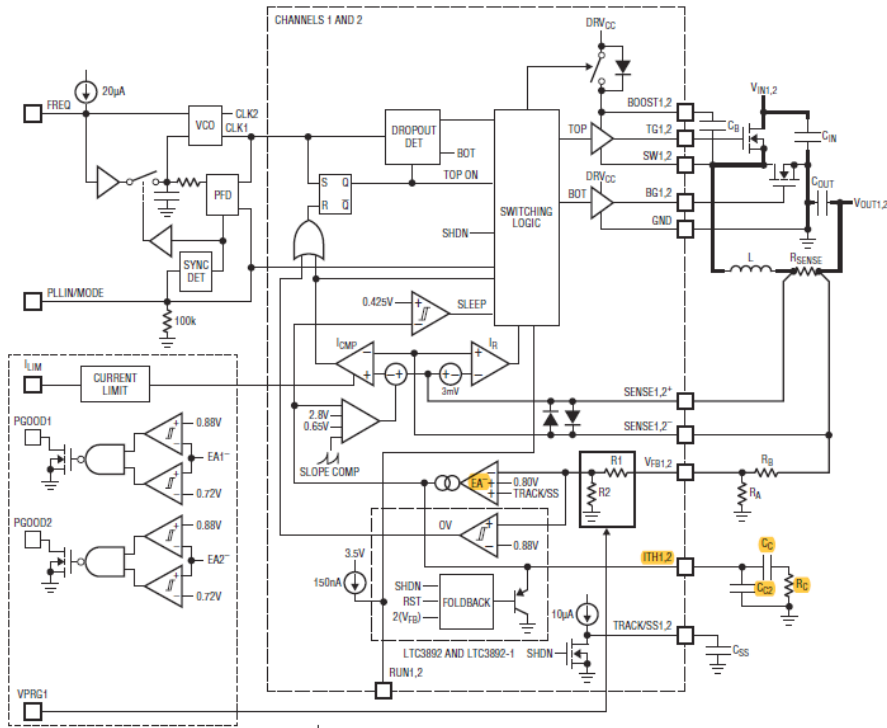


Figure 4-4: LTC3892-1 Functional Diagram, Highlighting Compensation Network [9]

To calculate the resistor and capacitor values, the procedure is followed by the K method [12]. Knowing the desired cross over frequency and phase margin, the compensator can be designed to provide additional gain and introduce a phase shift to bring up the gain and phase margin. The open loop of the power converter is simulated and is shown in Figure 4-5. At the desired bandwidth of 100 kHz, the magnitude plot shows -72 dB and the phase plot shows -111 degrees. Additionally, the PWM circuit of the LTC3892-1 introduces a -8.943 dB attenuation. The total gain of the filter and the PWM is then -81.783 dB, so the compensator must provide an 81.783 dB gain. 81.783 dB gain can be achieved by a ratio of 12278:1 between the feedback resistor and input resistor of the network. To accommodate 45 degrees of phase margin, select the appropriate value of K shown in Table 4-6. Verify that selected K and the phase of the open loop subtracted from 360 degrees is above 45 degrees. The K value selected for the compensator was chosen to be 5. The resistor and capacitor values can be solved

from using equations 4.6, 4.7 and 4.8. The calculated values for the resistor and capacitor in the compensation network is listed in Table 4-7.

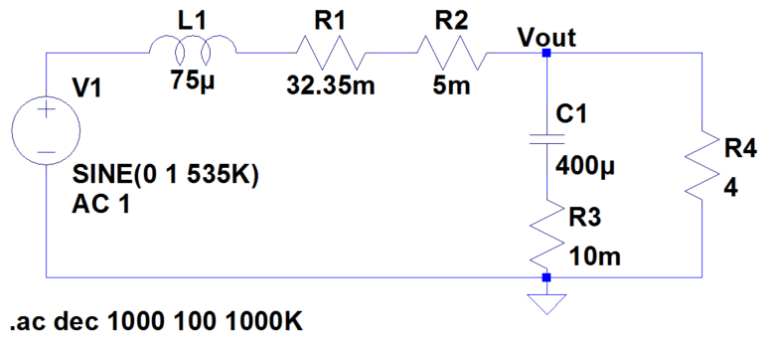
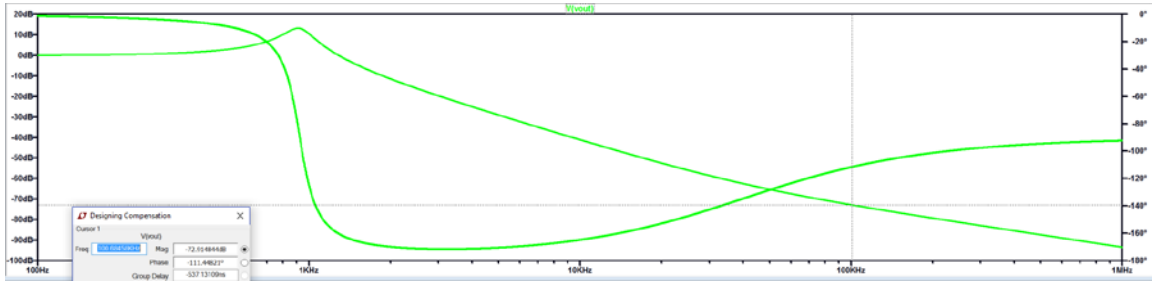


Figure 4-5: Schematic and simulation results for Open Loop Power Converter

Table 4-6: K Factor and Phase [12]

K	$\Theta_c$
2	-233
2.5	-224
3	-217
4	-208
5	-203
6	-199

$$K = \frac{\omega_{co}}{\omega_z} = \frac{\omega_p}{\omega_{co}} \quad K - K \text{ Factor} \quad (4.6)$$

$\omega_{co}$  – Crossover Frequency

$$\omega_z = \frac{\omega_{co}}{K} = \frac{1}{R_C C_C} \quad \omega_p - \text{Pole Frequency} \quad (4.7)$$

$R_C$  – Series Compensation Resistor

$$\omega_p = K \omega_{co} = \frac{1}{R_C C_{C2}} \quad C_C - \text{Series Compensation Capacitor} \quad (4.8)$$

$C_{C2}$  – Parallel Compensation Capacitor

Table 4-7: Compensation Resistor and Capacitor Values

$R_{in}$	100 $\Omega$
$R_C$	1.227 M $\Omega$
$C_C$	6.48 pF
$C_{C2}$	.259 pF

#### 4.7 Feedback Network Design

The feedback of the buck controller is a critical design implementation for the smart wall plug to adjust the output voltage. A voltage divider from the output voltage is connected back to the controller to be compared by the internal voltage reference to adjust the duty cycle of the gate drive to the switching network. Varying the feedback network can adjust the feedback voltage and achieve the different output voltages. The adjustable feedback network of the smart wall plug comprises of resistors, a digital potentiometer and a current source VID voltage programmer. A voltage divider is formed as shown in Figure 4-6, and will exhibit the output voltage relationship shown in Equation 4.7.

$$V_{out} = V_{FB\_REF} \left( 1 + \frac{R_{FB\_Top}}{R_{DigPot} + R_{FB\_Bot}} \right) - I_{VID} R_{FB\_Top} \quad (4.8)$$

$V_{out}$  – Output Voltage  
 $R_{FB\_Top}$  – Top Resistor  
 $R_{DigPot}$  – Digital Potentiometer  
 $I_{VID}$  – Programmable Current  
 $R_{FB\_Bot}$  – Bottom Resistor



#### 4.7.1 Digital Potentiometer Design

The digital potentiometer acts as the primary feedback adjustment for the buck regulator. When selecting the digital potentiometer, qualities to consider are end to end resistance, resolution, digital interface, internal memory, and performance [13].

Selecting the end to end resistance is directed related to the top fixed resistor. Fixing the top resistor to 49.9 k $\Omega$ , the digital potentiometer must range up to 15.5 k $\Omega$  to achieve the desired output voltages. Resolution should be high to offer small incremental steps to adjust to nominal voltage and reduce the percent error. The interface relates to how the digital potentiometer is configured like I2C, SPI or push button interface. In the smart wall plug application, the digital potentiometer needs to be quickly configured. SPI is favored among the three because SPI offers speeds up to 50 MHz and will allow for dynamic performance of adjusting the output voltage to the load's nominal requirement. The internal memory type matters whether the potentiometer can be reprogrammable or not. Lastly, the performance pertains to the tolerance error level and accuracy. The smart wall plug uses the AD5270BRMZ-20 as the digital potentiometer. The AD5270BRMZ is a 20 k $\Omega$  10bit SPI interfaced reprogrammable digital potentiometer with 1% maximum resistor tolerance error [14]. A 470  $\Omega$  was tied in series to help protect the feedback node from shorts in case the digital potentiometer malfunctions.

#### 4.7.2 Current Source VID Voltage Programmer

A current source VID voltage programmer serves as a secondary adjustment to the feedback voltage. The digital potentiometer will set to the closest digital resistance value, then the current source will inject a current to the feedback network and would adjust the feedback voltage to change the output voltage. The injected current drives the feedback resistor and lowers the necessary current supplied through the top feedback resistor, thereby lowering the output voltage [15]. The current source VID voltage

programmer used for the smart wall plug project is the LM10010. The LM10010 is a 6-bit current DAC that takes a VID interface to decode an output current. The LM10010 has the ability to adjust from the output voltage up to 3 V in increments of 46.9 mV.

Implementing the current source improves the output voltage accuracy for 12 V, 15 V and 20 V output voltage setting shown in Table 4-8.

Table 4-8: Digital Potentiometer and VID Current Source Configuration for Output Voltage

Vin (V)	Vout (V)	Duty Cycle	Top Resistor ( $\Omega$ )	Digital Pot Bits	Digital Pot ( $\Omega$ )	VID bits	Actual Vout (V)	Percent Error
48	3.3	6.875%	49900	793	15488.28125	0	3.301522525	0.046%
48	5	10.417%	49900	462	9023.4375	0	5.00501004	0.100%
48	6	12.500%	49900	368	7187.5	0	6.013189683	0.220%
48	9	18.750%	49900	225	4394.53125	0	9.006340539	0.070%
48	12	25.000%	49900	158	3085.9375	1	11.97938805	0.172%
48	15	31.250%	49900	119	2324.21875	2	14.99282894	0.048%
48	20	41.667%	49900	82	1601.5625	1	20.0235722	0.118%
48	24	50.000%	49900	64	1250	0	24.00930233	0.039%
48	36	75.000%	49900	34	664.0625	0	36.00088179	0.002%

#### 4.8 Power Converter Simulation

The LTC3892-1 controller simulation model was used to test out the converter design in LTSpice, shown in Figure 4-6. Parameters were set for the digital potentiometer and the VID current DAC for the appropriate output voltage listed in Table 4-6. The component values used for the power stage, frequency and compensation network were implemented. The simulation is configured to a single-phase operation to analyze the behavior of the converter.

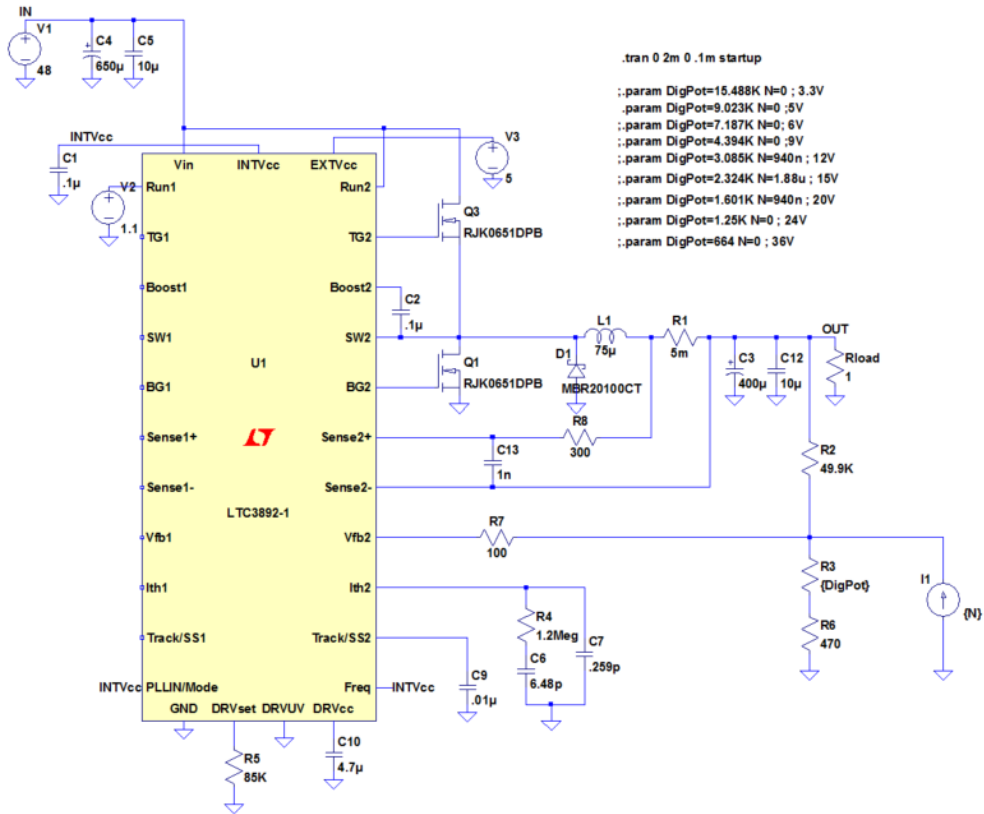


Figure 4-6: LTC3892-1 Controller Simulation Schematic

The converter was simulated to output 3.3 V, 5 V, 6 V, 9 V, 12 V, 15 V, 20 V, 24 V, and 36V at minimum and maximum load conditions. The simulations exhibited positive results on each output voltage setting. Simulation waveforms from two extremes of the output voltages, 3V and 36V, are shown in the following four figures. Shown in Figures 4-7 and 4-8 are the start up to steady state waveforms when the converter is configured to output at 3.3 V and supplying .25 and 5 A load current. Figures 4-9 and 4.10 show the startup for the 36 V output voltage condition, supplying .25 amps and 2.778 amps.

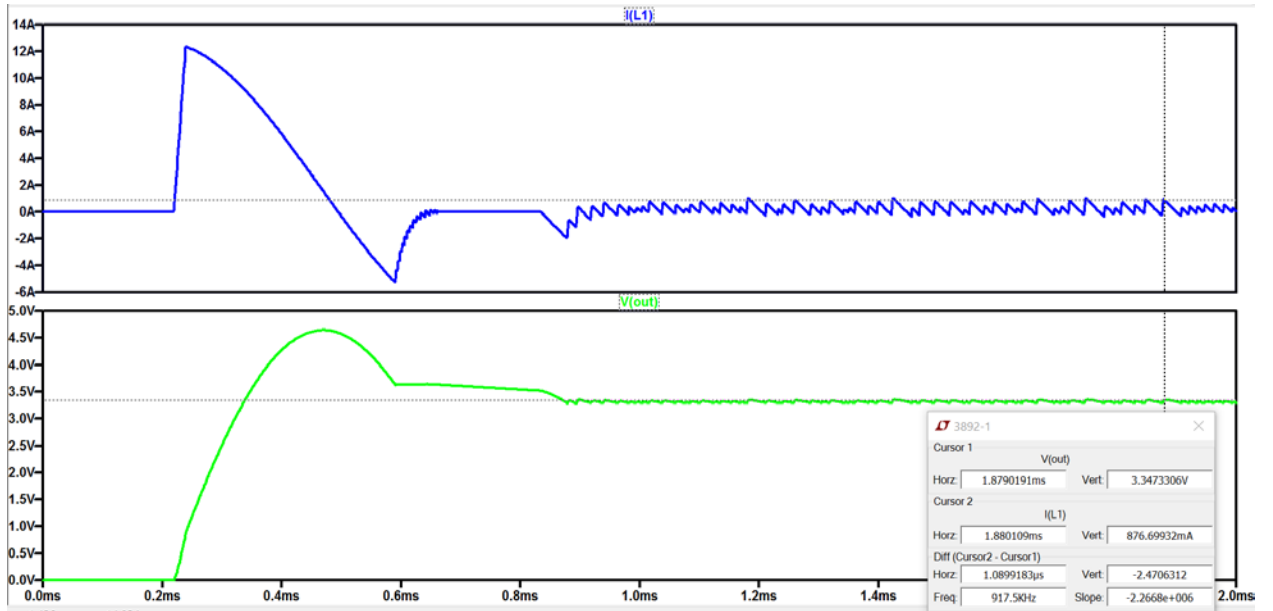


Figure 4-7: Output Voltage at 3.3 V and Load Current at .25 A

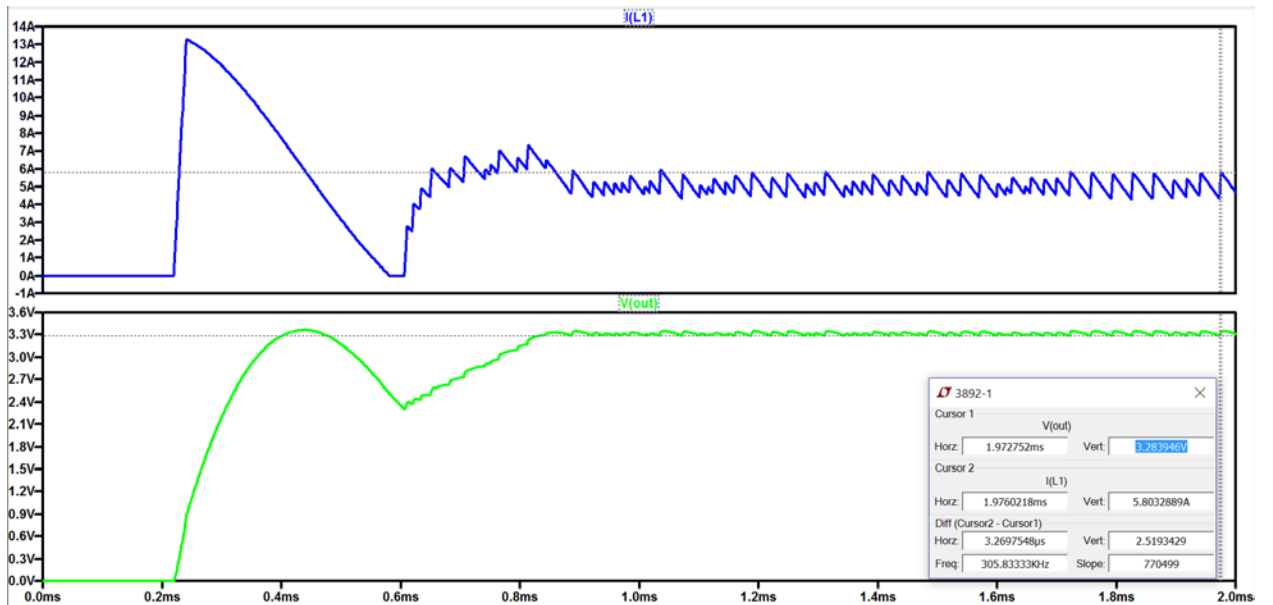


Figure 4-8: Output Voltage at 3.3 V and Load Current at 5 A

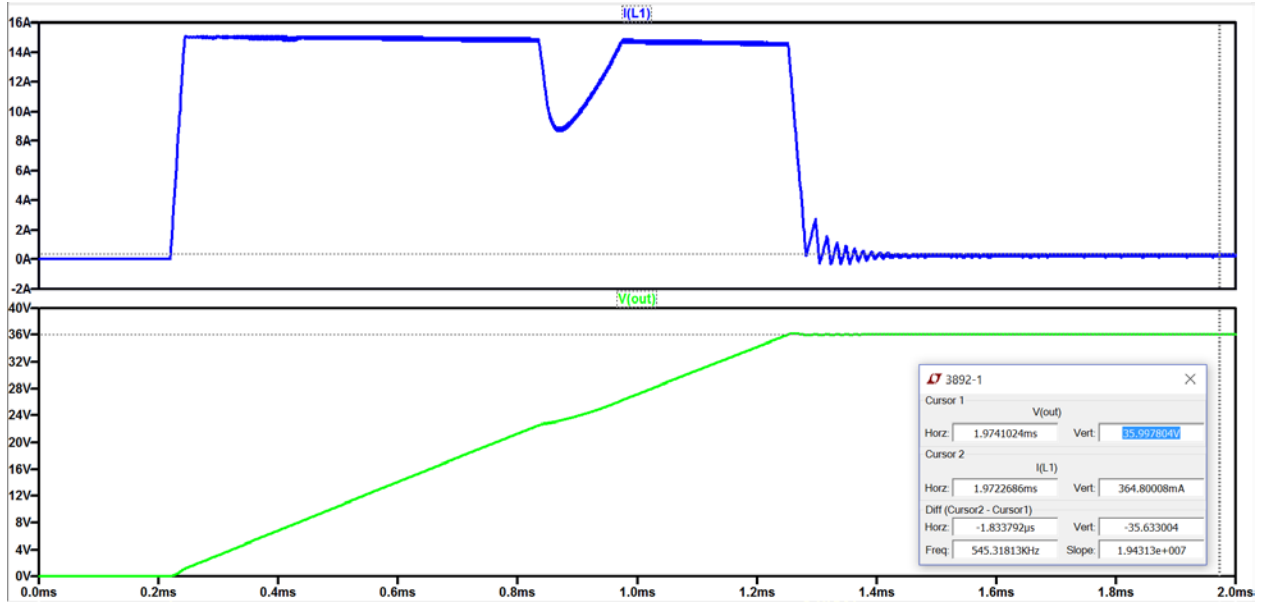


Figure 4-9: Output Voltage at 36 V and Load Current at .25 A

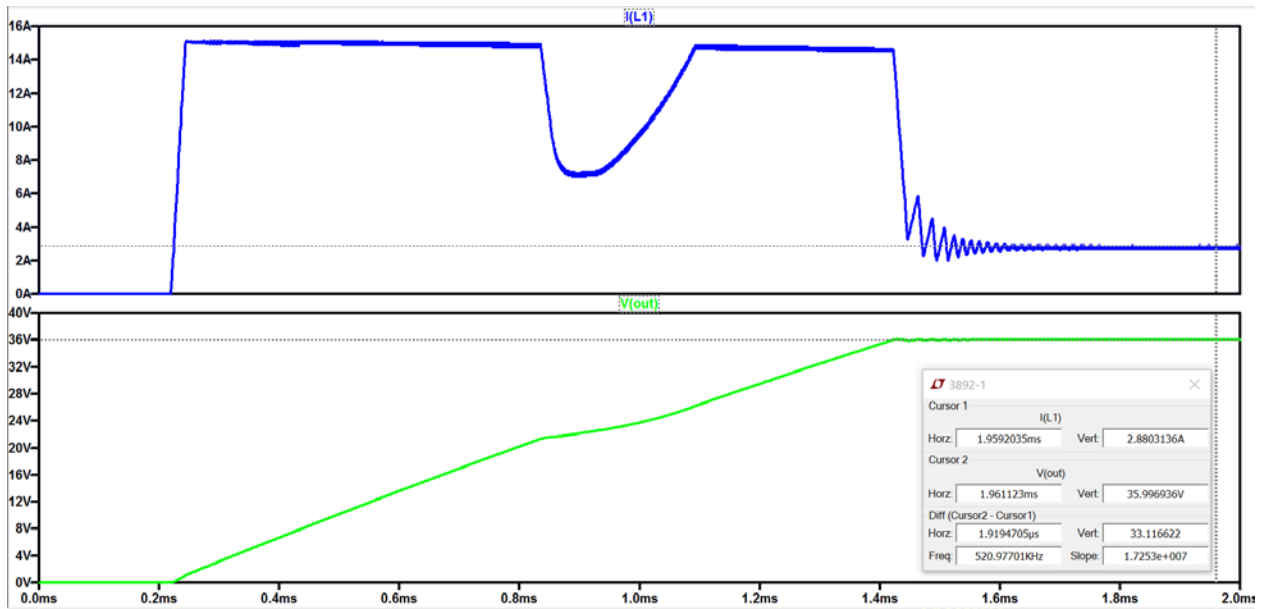


Figure 4-10: Output Voltage at 36 V and Load Current at 2.778 A

#### 4.9 Microcontroller Selection

With the required ICs to operate the smart wall plug, such as the differential operation amplifier for the current sense resistor, the digital potentiometer, and the VID current source across two channels, the smart wall plug project requires 17 digital connections and 2 analog connections. The microcontroller should offer at least the required number of digital and analog connections needed. The microcontroller is also the component that acts as the transceiver for the SPI and VID interface to control the feedback network. The microcontroller must also run at a high frequency to dynamically detect the output load voltage and control the digital Potienometer, and VID current source.

The STM32F302 on the Nucleo-64 board was chosen to be the microcontroller of the smart wall plug. The STM32F302 board offers more pins than the Arduino board used in the past thesis project, as well as a higher operating frequency and more memory. The STM32F302 microcontroller runs on the embedded ST-Link programmer platform[16] and can configure its pins for analog connections for the load current sensing and digital connections for the SPI and VID interfaces in the feedback network.

#### 4.10 Schematic and Bill of Materials

The full schematic of the smart wall plug is shown in Figure 4-11. The schematic illustrates the LTC3892-1 controller configured to provide two identical channels. At the input of both channels, there is a fuse for over current protection. At the output of the converter, reverse polarity voltage protection is implemented using bridge rectifiers. The smart wall plug project also include a secondary buck regulator and a LDO to provide auxiliary power to the ICs. Additionally, LED driver circuits were implemented to turn on LEDs when the controller is providing power to the output. The schematic tool used to

generate the schematic was Altium Designer. The list of materials used in the smart wall plug project are listed in Table 4-9.

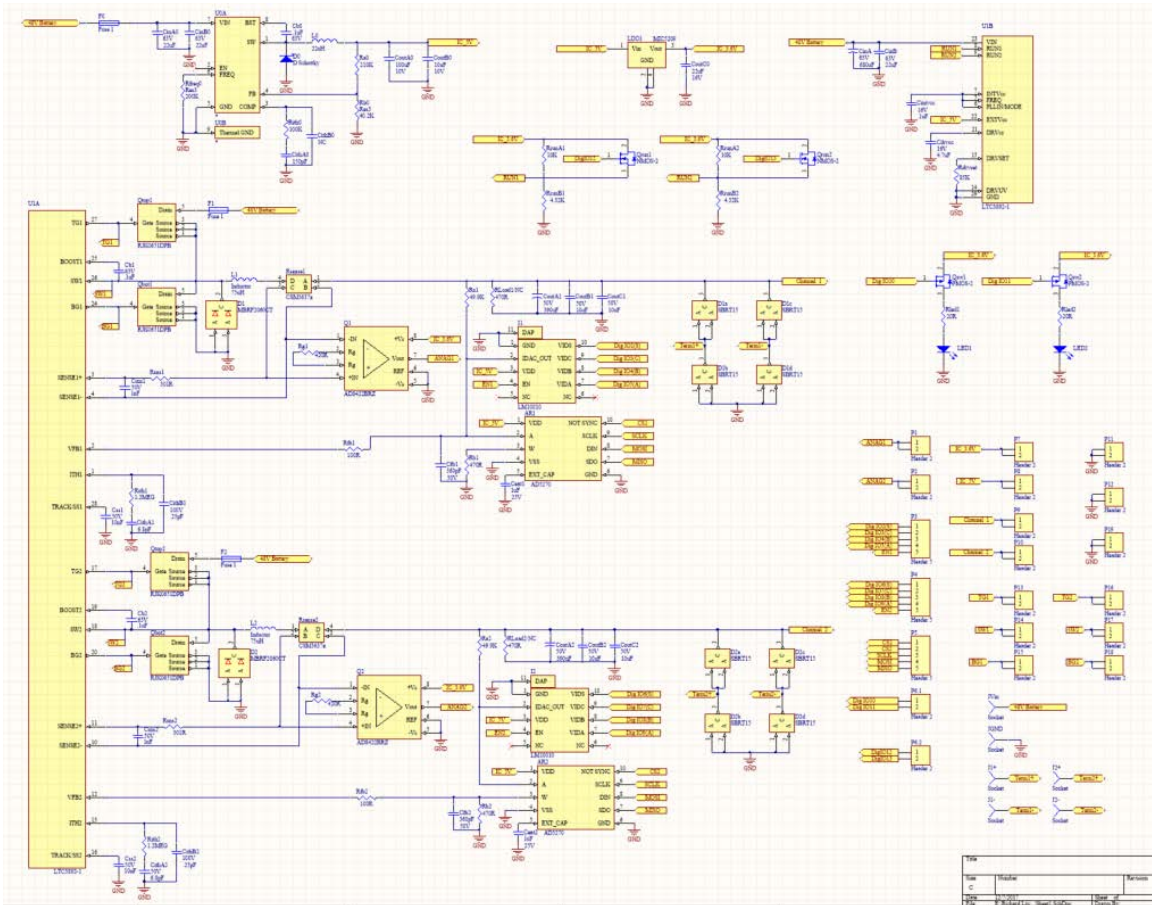


Figure 4-11: Smart DC/DC Wall Plug Schematic

Table 4-9: Schematic Bill of materials

Comment	Description	Designator	Footprint	LibRef	Quantity
AD5270	AD5270	AR1, AR2	AD5270	AD5270	2
	Capacitor (Semiconductor SIM Model)	Cb0, Cb1, Cb2, Cdrvcc, Cext1, Cext?, Cfb1, Cfb2, CinB, CinB0, CinC, Cintvcc, CithA0, CithA1, CithA2, CithB0, CithB1, CithB2, CoutB0, CoutB1, CoutB2, CoutC1, CoutC2, Csns1, Csns2, Css1, Ccss2	C1206	Cap Semi	27
Cap2	Capacitor	CinA, CinA0, CoutA0, CoutA1, CoutA2	CAPR5-4X5	Cap2	5
D Schottky	Schottky Diode	D0, D1a, D1b, D1c, D1d, D2a, D2b, D2c, D2d	SMB	D Schottky	9
MBRF2060CT		D1, D2	DIP6	MBRF2060CT Schottkey Diodes	2
Fuse 1	Fuse	F0, F1, F2	PIN-W2/E2.8	Fuse 1	3
LM10010		I1, I2	LM10010	LM10010	2
Inductor	Inductor	L0	INDC4532	Inductor	1
Inductor	Inductor	L1, L2	IHLP-8787MZ Inductor	Inductor	2
3.6V	Voltage Regulator	LDO1	D2PAK_N	Volt Reg	1
LED0	Typical INFRARED GaAs LED	LED1, LED2	LED-0	LED0	2
AD8422		Q1, Q2	SOIC127P600 X175-8N	AD8422 OP AMP	2
RJK0651DPB	RJK0651DPB	Qbot1, Qbot2, Qtop1, Qtop2	RJK0651DPB	RJK0651DPB	4
PMOS-2	P-Channel Power MOSFET	Qsw1, Qsw2	TO-220AB	PMOS-2	2
Res3	Resistor	Ra0, Ra1, Ra2, Rb0, Rb1, Rb2, Rdrvset, Rfb1, Rfb2, Rfreq0, Rg1, Rg2, Rith0, Rith1, Rith2, Rled1, Rled2, Rload1/NC, Rload2/NC, Rsns1, Rsns2	J1-0603	Res3	21
CSM3637z		Rsense1, Rsense2	SOT190P914X 120-4N	CSM3637z	2
MP2565		U0	SOIC127P600 X175_HS-9N	MP2565	1
LTC3892-1		U1	LTC3892	LTC3892	1



## Chapter 5

### HARDWARE CONSTRUCTION, TEST AND RESULTS

#### 5.1 Component Selection

To begin with the hardware construction of the Smart DC/DC Wall Plug, each component on the schematic must be selected and obtained. The task of selecting each component for the project involves navigating thousands of products offered by dozens of IC manufacturers on electronic distributor sites like Digikey and Mouser. Some of the project constraints that help guide the process are size and cost. All of the components from the schematic must fit in the size constrained by the wall plug dimensions shown previously in Figure 3-3. The components such as capacitors, inductors, and MOSFETs with high voltage and current requirements can be very large and selecting large components may jeopardize all the components to fit on the board. In contrast, selecting small components can be less effective with thermal abilities and power ratings, and leave unused space. It is critical to understand the physical size of the board and optimize the components selection based on physical size to fit on the wall plug dimension. Other physical traits to consider with selecting components are the package type, the number of pins, and the type of pins. These physical traits pertain to the feasibility of soldering the components on to the board. Components may come in inconvenient packages and will be tough to solder, given the tools and skill level of assembling components by hand. The second main constraint during the component selection process is cost based on a provided budget. This budget criteria pertains to selecting the cheapest component that can suffice for the project. When choosing components from a selection, attempt will be made not to over compensate on tolerance, temperature coefficients, voltage ratings, or current ratings. These two guidelines, physicality and cost, can help with the component selection process.

Once a component is identified to use for the project, they are listed into a bill of materials table. The bill of materials table helps account for each item required for the proposed Smart DC/DC Wall Plug and keeps a record of the project cost. The bill of materials for one Smart DC/DC Wall Plug is shown in Table 5-1. When ordering the components from the list of materials, at least 3 to 5 times the quantity for each line item should be ordered to account for chip malfunctions, possibility of losing chips or shorting, etc. When an event of which an extra part is needed, spare inventory for each component is available for use and will save on project time from reordering. Reordering parts will add on shipping charges and delay towards project progress. Also, free samples can be ordered directly from the IC manufacturers. This can be a method to save on costs and to have additional parts to use just in case for the project.



## 5.2 PCB Layout

The next step in hardware design is to create a printed circuit board of the Smart DC/DC Wall Plug Design from the schematic in Figure 4-11. Construction of the printed circuit board involves specifying the board dimension, placing of the components, and routing of the nets together properly in a PCB layout program. Altium Designer 17 is used to create the PCB layout of the design. The dimension of the PCB is constrained to the physical dimension of the wall outlet shown in Figure 3-3. The physical board is set to 2.8 inches by 3.8 inches so that the project can fit into a wall outlet enclosure. The component placement begins with importing the components from the schematic design and the proper footprints. The footprint of each component must be either created or imported from the manufacturers or PCB library. When creating the component footprint manually, the datasheet will be used for margin and tolerances. All of the components from the Smart DC/DC Wall Plug project were created manually. The bulk of the PCB layout process involves the optimal placement of the components and the appropriate routing design to connect the components together properly. The guidelines to aid this process involve identifying the AC and DC power paths. The datasheets of the various components in the bill of materials may provide tips on how to place and route on a PCB such as symmetrical routing for differential pair signals and for layout guidelines on thermal relief.

When considering the AC power path of the converter, inductance is the most critical parameter to be optimized. Abrupt changes of current in inductors are not desirable and can induce sharp voltage spikes. PCB traces are representatives as wires and wires inherently introduce finite inductance, therefore traces must be minimized. The AC power path of the buck converter relates to the path along with the input capacitors and switches. At the connection from the input capacitor and the two switches, the switches turn on and off and induce the largest change in current of the buck converter.

The component placement and routing of the input capacitors and switches were prioritized because the traces will have the most influence at these areas. Figure 5-1 shows the buck converter AC waveforms of the LTC3892 at its 2-channel arrangement.

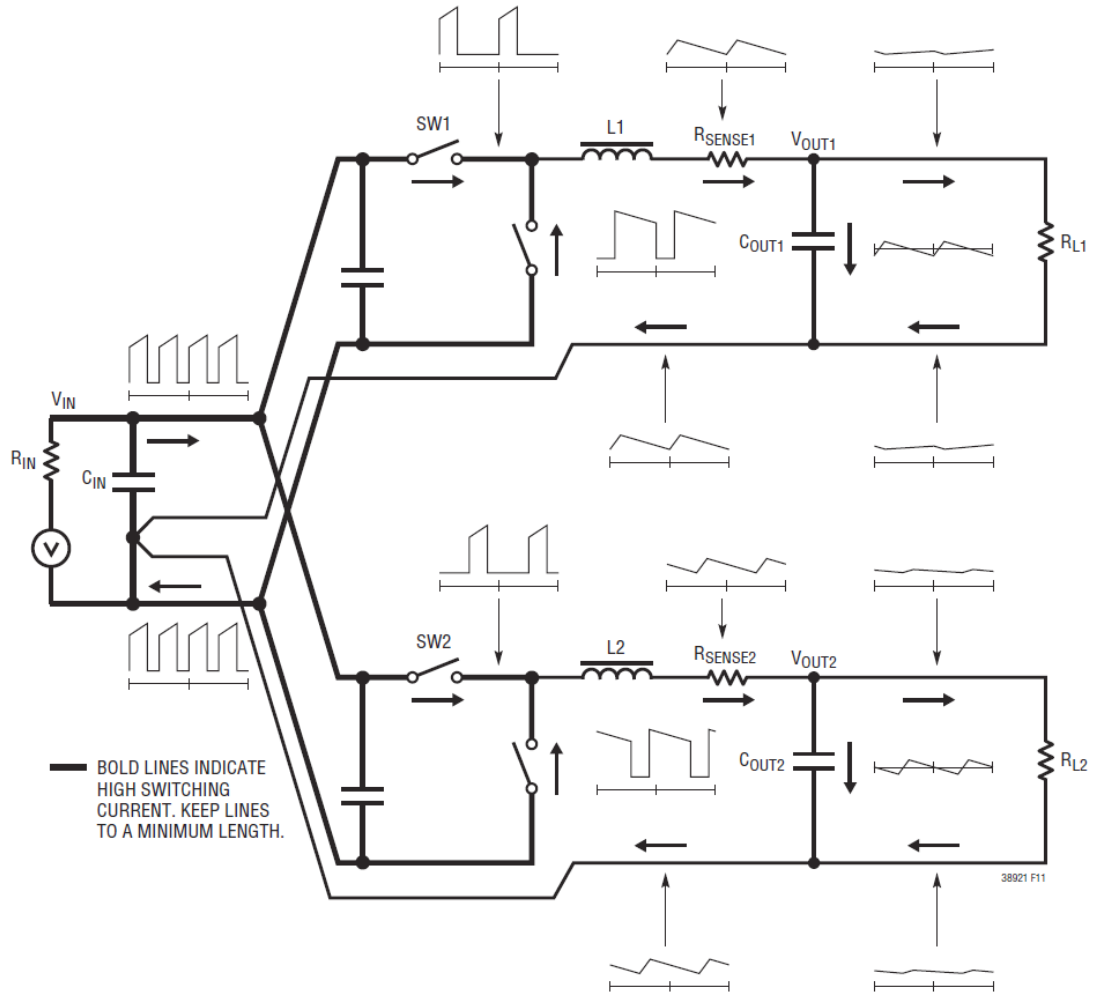


Figure 5-1: Branch Current Waveforms of LTC3892 [15]

The second consideration is the DC power path of the converter. This criterion aims to minimize the power path and to place components as close together as possible. The goal of placing components and routing is to minimize DC resistance and voltage drops. PCBs are typically fabricated using copper as the material for traces. A square area of two-ounce copper is approximately .25 milliohms of resistance [8]. For the Smart

DC/DC Wall Plug project, the maximum possible current per channel is 12A and so each square area of copper can have up to 3mV of potential difference. The severity of the potential difference issue increases as the amounts of copper squares used for traces increases. An example to put this issue in to perspective is the case of a 10mm by 1000mm trace width of 2 ounces of copper. A 10mm by 1000mm trace equates to 100 10mm by 10mm squares and totals 25 mohms of resistance. The maximum load current of 12A through a 25mohms trace results in a 300mV of potential difference from end to end, which is quite significant. This metric of the DC power path such as the input, output, and ground paths must be minimized to reduce the resistance from traces and the DC voltage drops.

The Smart DC/DC Wall Plug acts as a high current power supply with up to 12A load capabilities on each channel. Sizing the trace width appropriately is important in order to reach the current rating of 12-amp maximum current. Implementing 12A load trace for each of the two channels will be very difficult to maintain the appropriate thickness of PCB trace width on the same layer without exceeding the size constraint shown in Figure 3-3. A layout trick to overcome this issue involves having multilayer PCB traces and using vias to stitch them together, effectively having twice the amount of trace width. Another design parameter to aid with more current while maintaining the same area is to increase the amount of copper weight the board will be fabricated with, in ounce per square foot. The more copper each layer has, the less width size the traces can be sized. Using the PCB trace width calculator [8], the appropriate minimum sized trace width can be determined based on current requirements.

Once the board has all the components laid out and routed for the design, headers and test pins were added in the layout. The headers serve to interface the input and output from the Smart DC/DC Wall Plug PCB with the microcontroller. The connections to the microcontroller are branched out to the side of the board as female or

male headers. The microcontroller connection includes the SPI interfaced digital potentiometer and the VID programmable current DACs, LEDs drive signals and enable signals. Placing test pins along the board is important especially during the bring up of the board to serve as probe points for debugging purposes. Each critical part of the circuit such as the transitory' gate trace, the analog out from the gain amplifier, the output of each converter should have test pins. Since majority of the components used in the PCB layout are surface mount devices, branching out the pins to test pins helps with the convenience of probing the signals on an oscilloscope or other test instrumentations.

The completed two-sided PCB layout in the 3D view is shown in Figure 5-2 and Figure 5-3. The completed 3D layout in Altium Designer gives a visual reference on how the board will look like. Visually inspect the layout to see how close components are placed together. Adjust the spacing between components if they are too close to each other, especially small components where they can be easily blocked from large components and would pose an issue to solder and assemble. Review every component if they are placed in the proper orientation, because while designing a two-sided board, the orientation of viewing from back to front view is flipped and so the components should be consistent with the orientation. Next, inspect the placement of the exposed pads and vias. Exposed pads and vias are outlets for possible shorts when soldering so there must be clearance between other components. Especially, careful attention was given to where the ground plane is at and that the ground vias are not placed too close to other pad traces. Lastly, reference designators labels on each component location were added where they are visible.

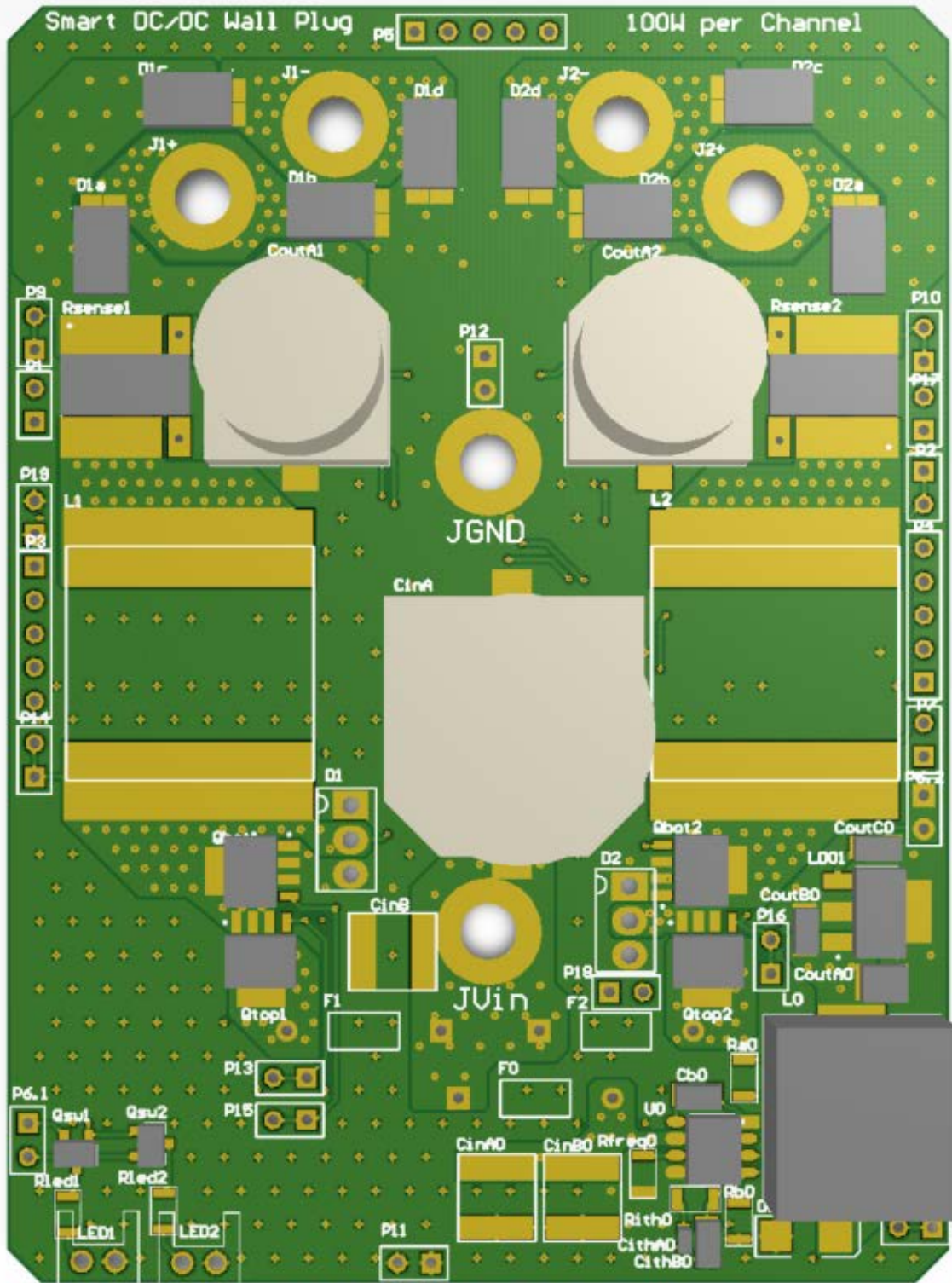


Figure 5-2: Front Side 3D View of PCB



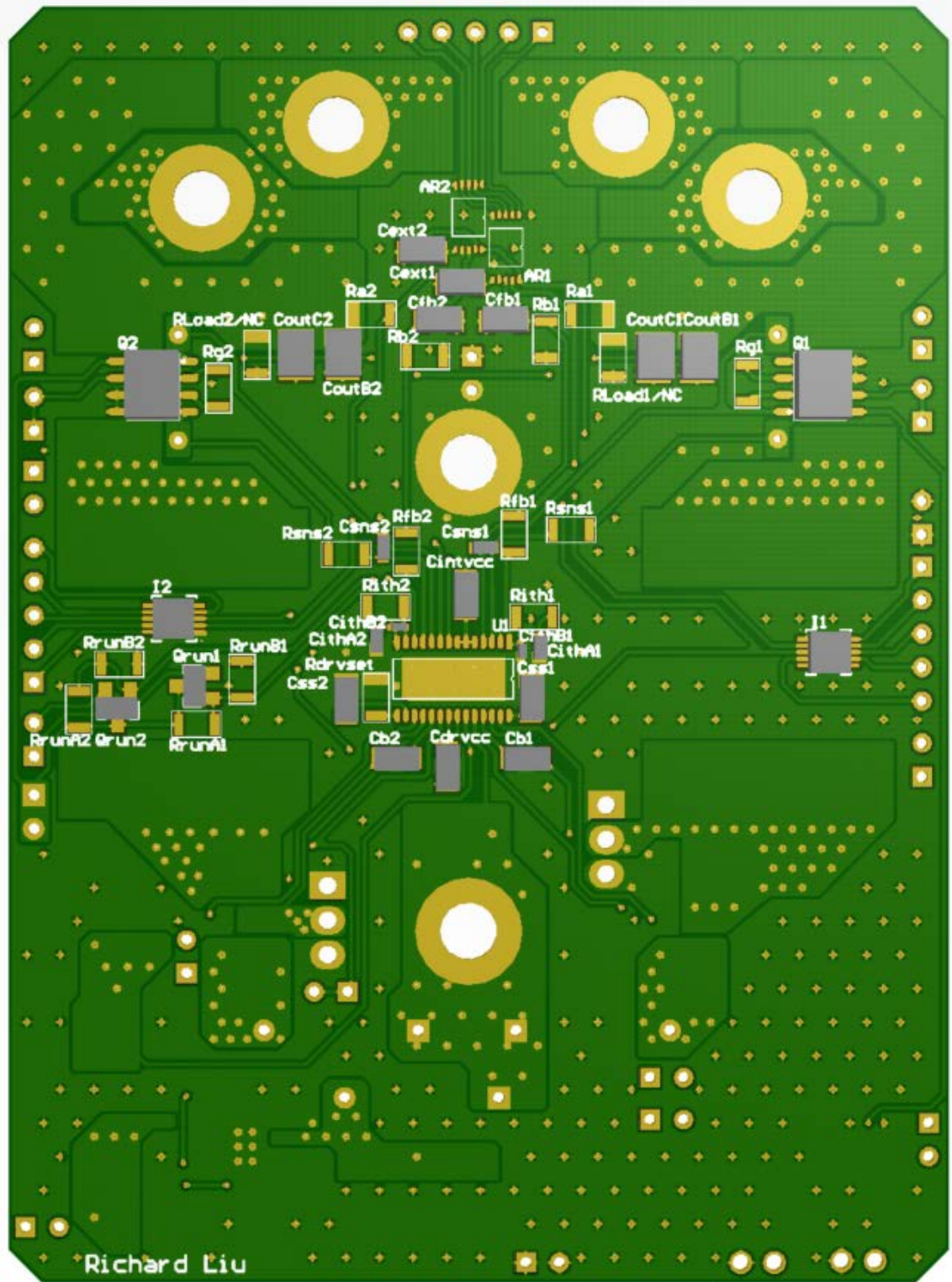


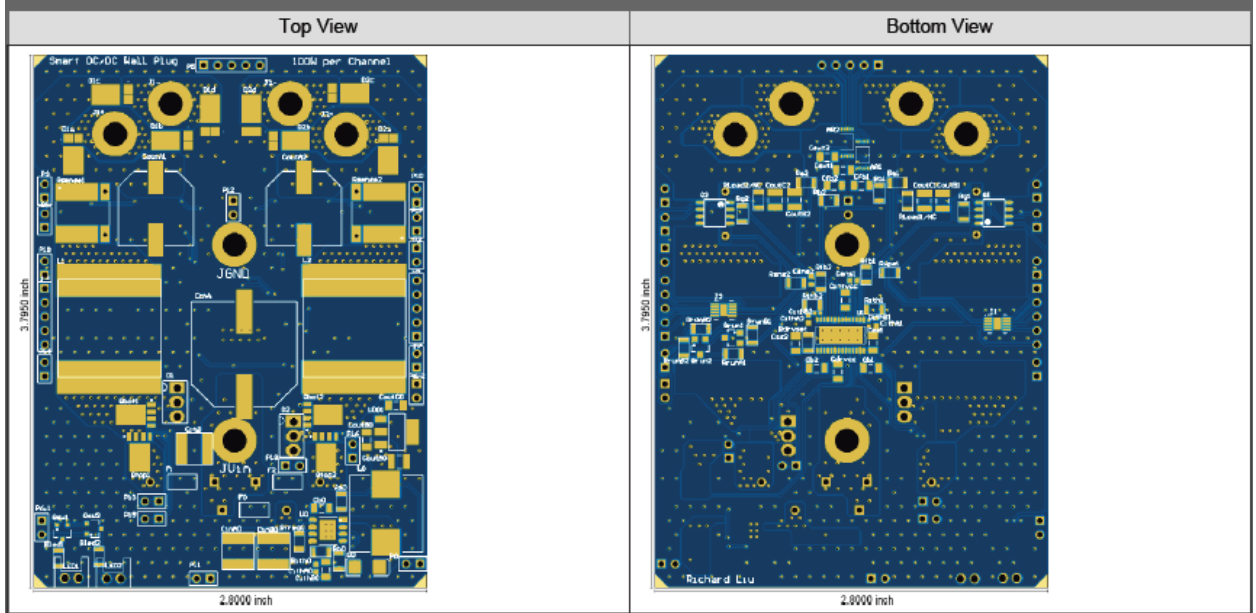
Figure 5-3: Backside of 3D view of PCB

### 5.3 Fabrication

Once the PCB layout is complete, the design rule check needs to be verified on the layout software. Once the design passes the DRC, the design is ready to be exported and can be sent out to a fabrication vendor. There are many fabrication services available. Popular ones include PCB express, Oshpark and Bay Area Circuits. For the Smart DC/DC Wall Plug project, Bay Area Circuits was selected based on price, lead time, board size, copper weight and hole density. Bay Area Circuits offered a student special fabrication service that compromised on lead time for the cost.

Bay Area Circuits has a useful online tool where we can upload our layout files to check if board design is viable for fabrication called DFM, design for manufacturing. The DFM site accepts Gerber X2 formats, which are layout files of the design, and generates a report detailing on the minimum constraints of the layout. The minimum constraints on the layout must comply with the specifications listed on the fabrication service site for trace spacing, edge clearances and ring clearances. The DFM identified the board design needed adjustments to the copper to edge margins. Originally, the original board layout was edge to edge on copper, but the design was changed to meet the minimum edge requirement of 10 mils off the edges. Shown in Figure 5-4 and Figure 5-5 are the DFM generated report [17] after the DFM is completed and passes on the fabrication services' PCB guidelines. The board files are then submitted and the order for the board was placed.

Single PCB View - Original



Summary - General - Original

PCB Size	2.8000 inch x 3.7950 inch	Copper Layers	2
PCB Thickness	62.00 mil	Solder Mask	Both
Customer Panel Size		Solder Mask Color	Blue
SMD Pads Top	111	Legend	Both
SMD Pads Bottom	171	Legend Color	White
SMD Density Top	11 SMD/inch <sup>2</sup>	Peeloff Mask	None
SMD Density Bottom	16 SMD/inch <sup>2</sup>	Carbon Mask	None
Number of Nets	88	Drill Hole Density	65 Holes/inch <sup>2</sup>
Electrical Test	Double Sided	Holes in SMD Pads	Yes
Max. Aspect Ratio on PTH	7.9	Edge Connectors	No
		Surface Finish	

Summary - Copper Layers - Original

Layer Type	Min. Line Width	Min. Copper Width	Min. Ring	Min. Clr. to Copper	Min. Clr. to Plated Hole	Min. Clr. to NPTH	Min. Clr. to Outline
	mil	mil	mil	mil	mil	mil	mil
Outer	<sup>1</sup> 5.52	<sup>2</sup> 5.02	<sup>3</sup> 6.00	<sup>4</sup> 5.90	<sup>5</sup> 15.99		<sup>6</sup> 10.00

Figure 5-4: PCB Layout Summary from DFM Report [17]

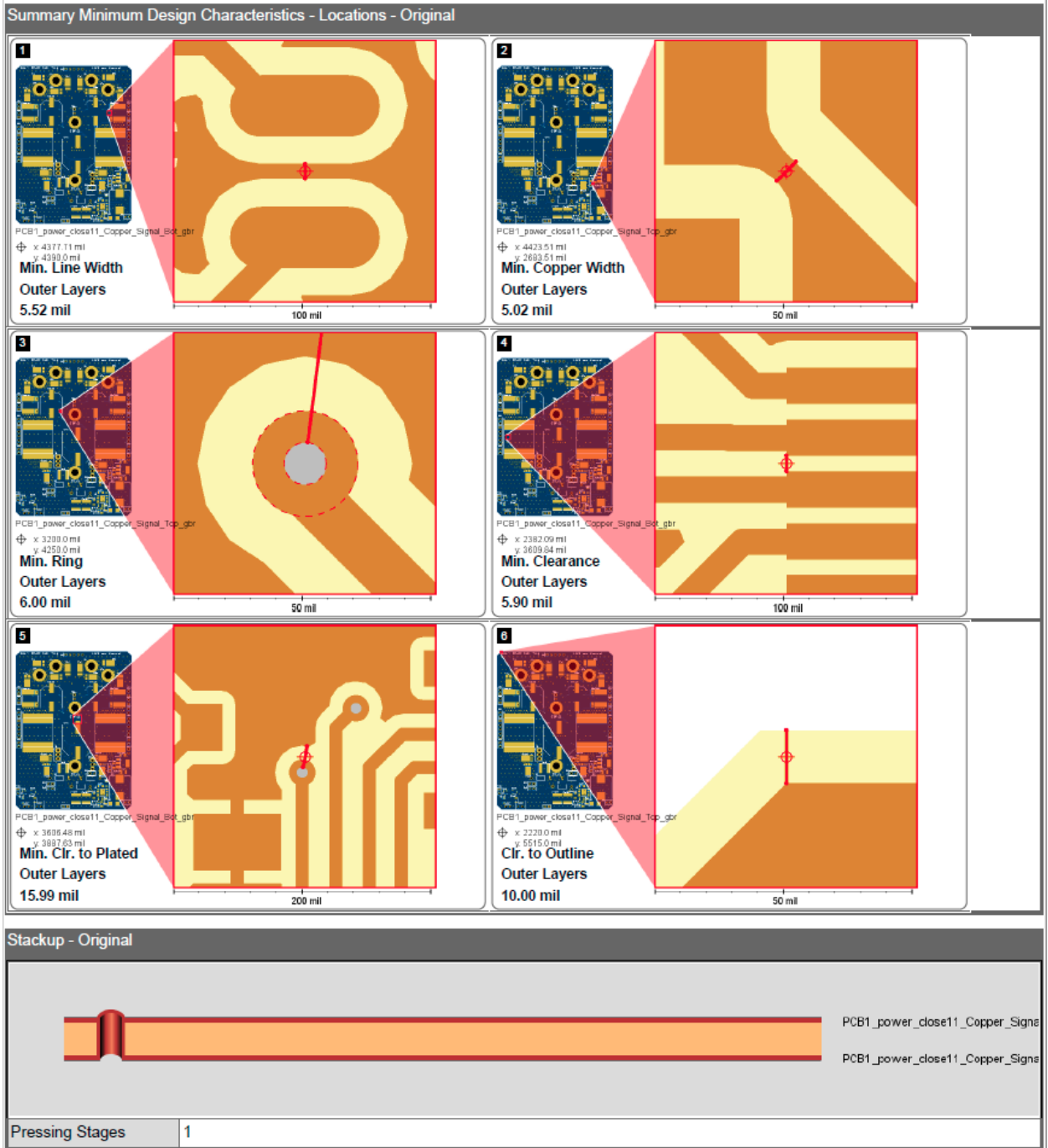


Figure 5-5: Minimum Design Characteristics and Board Stackup from DFM report [17]

## 5.4 Microcontroller Programming

Next, a test board of the feedback network was constructed to begin the development of the algorithm for the Smart DC/DC Wall Plug. The feedback network consists of the digital potentiometer, a current DAC and two resistors in series. The digital potentiometer interfaces with the microcontroller through SPI, which requires four digital connections: chip select, clock, MOSI, and MISO. The current DAC requires five digital pins for data and a digital enable. Headers are placed along the board which serve to connect the test board to the microcontroller and provide test points to verify the response of the feedback. The schematic of the feedback network is shown in Figure 5-6. The feedback test board layout is shown in Figure 5-7. The board was constructed as a single layer board so that it can be developed quickly to test with the microcontroller.

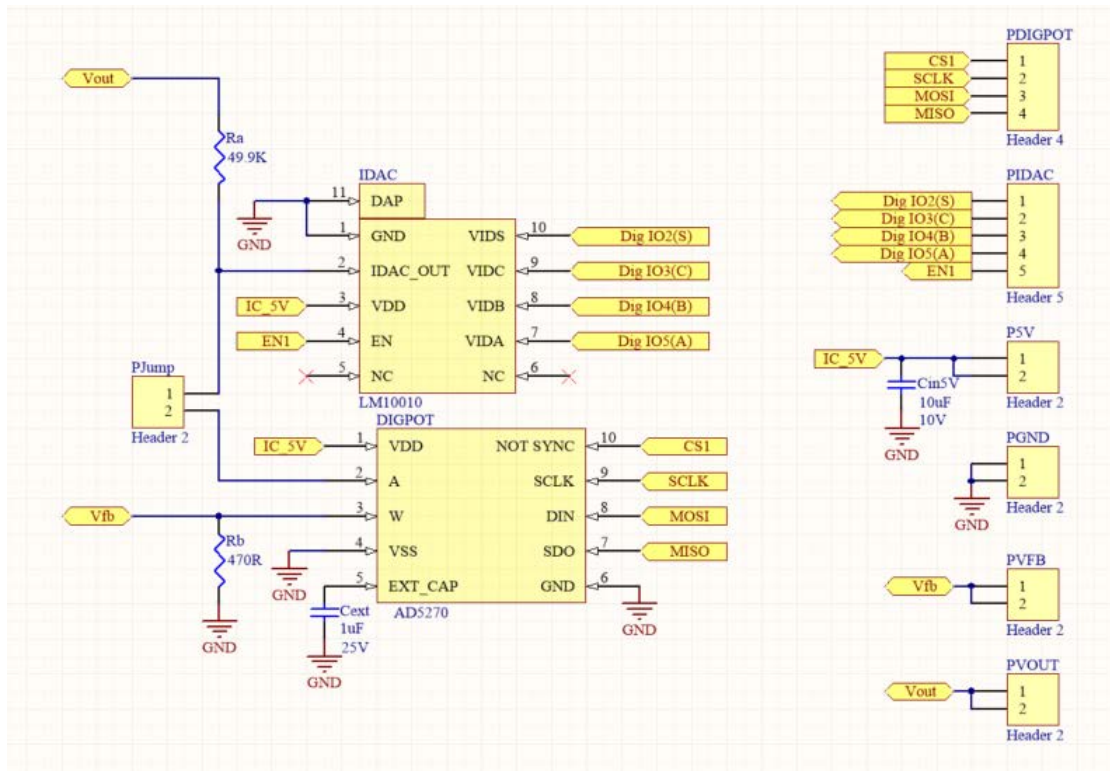


Figure 5-6: Feedback Test Board Schematic

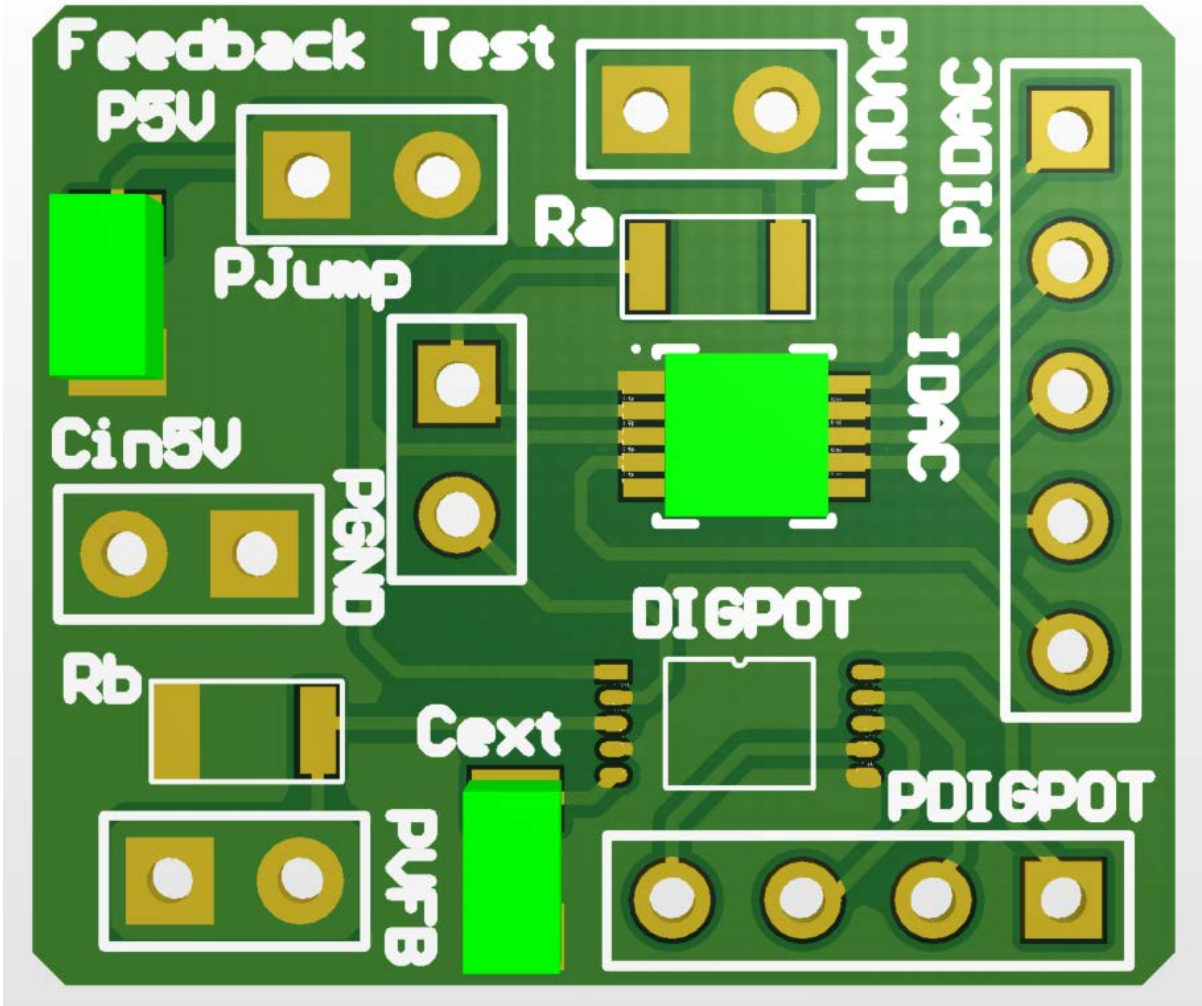


Figure 5-7: Feedback Test Board 3D Layout View

To begin with the microcontroller programming on the STM32F302R8 Nucleo board, the required pins for the Smart DC/DC Wall Plug were identified. The STM32F302R8 Nucleo board offers a 64-pin ARM Cortex M4 microcontroller. Of the 64 pins, 19 pins are preset for the board operation and 45 pins can be configured. To setup the pins of the microcontroller, STCUBEMX is the tool to configure the pins from the STM32F302R8 Nucleo board to digital GPIOs, SPI bus, or ADC analog input pins. The STCUBEMX tool displays a visual pinout of the microcontroller and can configure each pin individually to its desired function as shown in Figure 5-8.

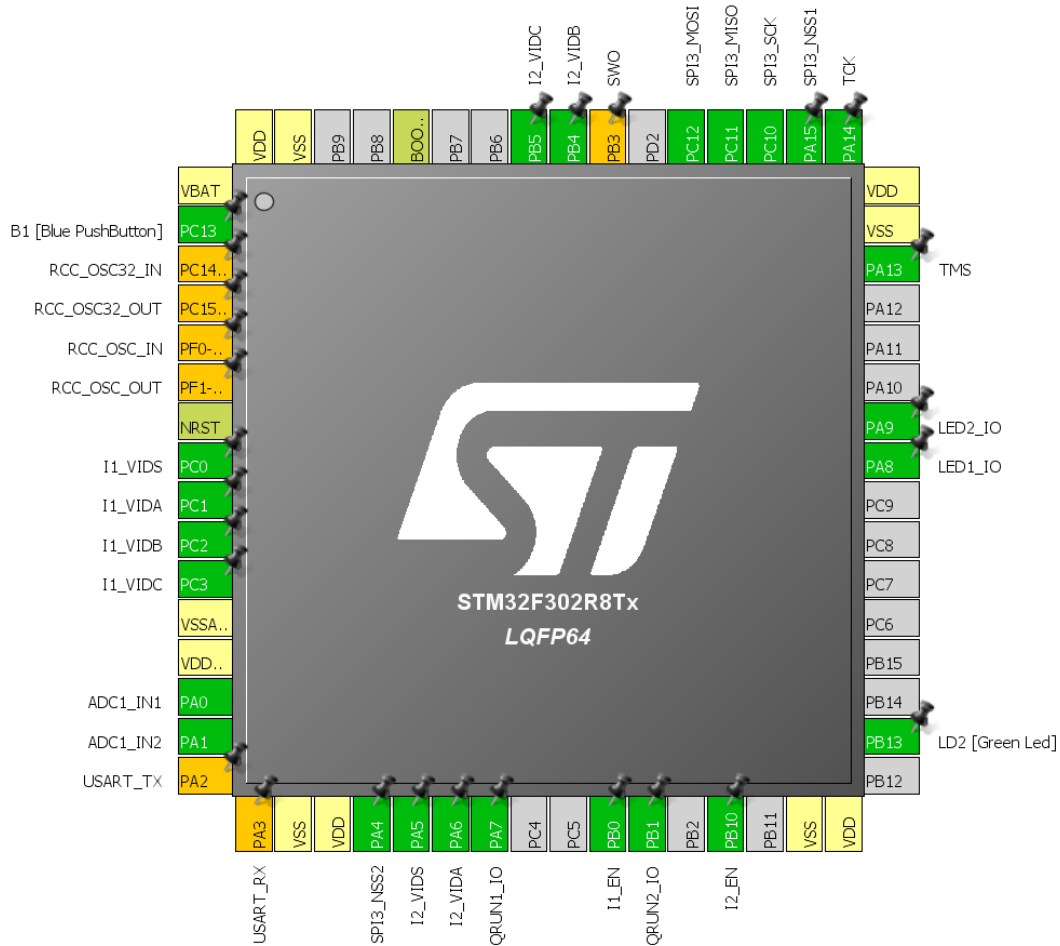


Figure 5-8: ST32F302R8Tx Pinout Configurations

The GPIOs can be configured with the starting output levels, the GPIO mode and output speed. Set the GPIO to the appropriate initial output level so that at the microcontroller boot up sequence, the microcontroller would not set the wrong peripherals on or off. The GPIO mode can be adjusted from push-pull to open drain if the output drive topology requires a pull up resistor. The speed should be adjusted if higher speeds are needed to suit the GPIO functionality. Lastly, an appropriate label was provided for each GPIO pin used.

Table 5-2: GPIO Pin Setting Configurations

Pin Name	Signal on Pin	GPIO output level	GPIO mode	GPIO Pull-up/Pull-down	Maximum output speed	Fast Mode	User Label
PC13	n/a	n/a	External Interrupt Mode wi...	No pull up pull down	n/a	n/a	B1 [Blue PushButton]
PB0	n/a	Low	Output Push Pull	No pull up pull down	Low	n/a	I1_EN
PC1	n/a	High	Output Push Pull	No pull up pull down	Medium	n/a	I1_VIDA
PC2	n/a	High	Output Push Pull	No pull up pull down	Medium	n/a	I1_VIDB
PC3	n/a	High	Output Push Pull	No pull up pull down	Medium	n/a	I1_VIDC
PC0	n/a	Low	Output Push Pull	No pull up pull down	Medium	n/a	I1_VIDS
PB10	n/a	Low	Output Push Pull	No pull up pull down	Low	n/a	I2_EN
PA6	n/a	High	Output Push Pull	No pull up pull down	Medium	n/a	I2_VIDA
PB4	n/a	High	Output Push Pull	No pull up pull down	Medium	n/a	I2_VIDB
PB5	n/a	High	Output Push Pull	No pull up pull down	Medium	n/a	I2_VIDC
PA5	n/a	Low	Output Push Pull	No pull up pull down	Medium	n/a	I2_VIDS
PB13	n/a	Low	Output Push Pull	No pull up pull down	Low	n/a	LD2 [Green Led]
PA8	n/a	High	Output Push Pull	No pull up pull down	Low	n/a	LED1_IO
PA9	n/a	High	Output Push Pull	No pull up pull down	Low	n/a	LED2_IO
PA7	n/a	Low	Output Push Pull	No pull up pull down	Low	n/a	QRUN1_IO
PB1	n/a	Low	Output Push Pull	No pull up pull down	Low	n/a	QRUN2_IO
PA15	n/a	High	Output Push Pull	No pull up pull down	Low	n/a	SPI3_NSS1
PA4	n/a	High	Output Push Pull	No pull up pull down	Low	n/a	SPI3_NSS2

To properly configure the SPI bus, STCUBEMX was navigated to the SPI bus configuration tab. From the drop down settings, the proper configuration for the SPI bus was selected, which includes clock polarity, clock edge triggering and the number of bits needed per transactions. The SPI component used for the Smart DC/DC Wall Plug is the Analog Devices AD5270 digital potentiometer. The AD5270 requires data to be triggered on the falling edge, and it has a phase of 1 edge, and 16 bits of data per transaction, with MSB first [14]. Shown in Figure 5-9 is the shift register and timing diagram sequence of the AD5270. Once the microcontroller is configured, STCUBEMX generates the source code with all the preset configuration built in. The project is then brought into ARM MDK for editing the source code for the Smart DC/DC Wall Plug project and compiled to the microcontroller.



**Shift Register and Timing Diagrams**

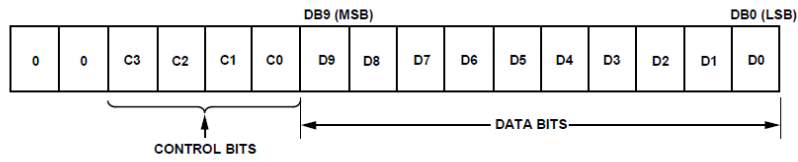


Figure 2. Shift Register Content

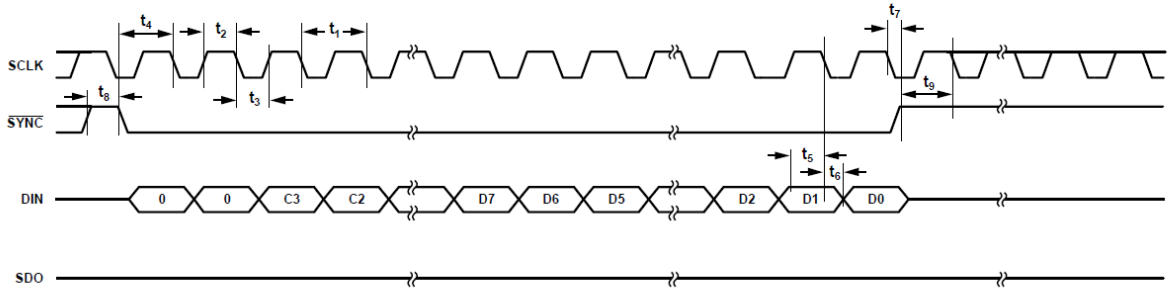


Figure 3. Write Timing Diagram (CPOL = 0, CPHA = 1)

Figure 5-9: SPI Shift Register and Transmit Timing Diagram for the AD5270 [14]

The algorithm of the Smart DC/DC Wall plug relies on the digital potentiometer, which acts as the main adjustment for the feedback network of the DC/DC converter. The startup of the converter will begin at the lowest output voltage setting, 3V. This occurs when the digital potentiometer is set at 43.5KΩ for the AD5270BRMZ-50. To write 43.5KΩ to the digital potentiometer, the SPI transmit must follow the format shown in Figure 5-9; the format starts with two don't care bits, followed by four bits for control and ten bits for data. The data sent to the digital potentiometer total to be two bytes. To write in this format, the digital potentiometer resistor setting is first converted into a 10-bit word, and is concatenated with the control bits then is split into two 8 bit words written in HEX. The HEX message for each output setting has been decoded and can be viewed in Table 5-3.

Table 5-3: HEX Codes for the AD5270BRMZ-50 Digital Potentiometer

Voltage Settings(V)	Target Resistance( $\Omega$ )	Bits	10-bit Binary Data	Control bits	HEX
3	43530	891	1101111011	0001	0x077B
3.3	38250	783	1100001111	0001	0x070F
5	22577.61905	462	0111001110	0001	0x05CE
6	18145.38462	371	0101110011	0001	0x0573
9	11334.87805	232	0011101000	0001	0x04E8
12	8172.857143	167	0010100111	0001	0x04A7
15	6346.901408	129	0010000001	0001	0x0481
20	4571.666667	93	0001011101	0001	0x045D
24	3702.413793	75	0001001011	0001	0x044B
36	2280	46	0000101110	0001	0x042E

To provide additional output voltage adjustment, the secondary feedback adjustment is the Texas Instruments VID programmed current DAC, LM10010. The LM10010 requires an enable pin to be inserted to operate and four digital data lines to change the amount of current to output. To enable this second feedback control, the enable pin must be set higher than 1.34V to turn on the device [15]. To program the LM10010, the sequence of the digital outputs required to set the device is as shown in Figure 5-10. The data sent the LM10010 is a 6-bit word worth inversely proportional to its decimal weight. View Table 5-4 to correlate the data word needed to program the LM10010 Current DAC based on the targeted output voltage setting.

### Timing Diagram

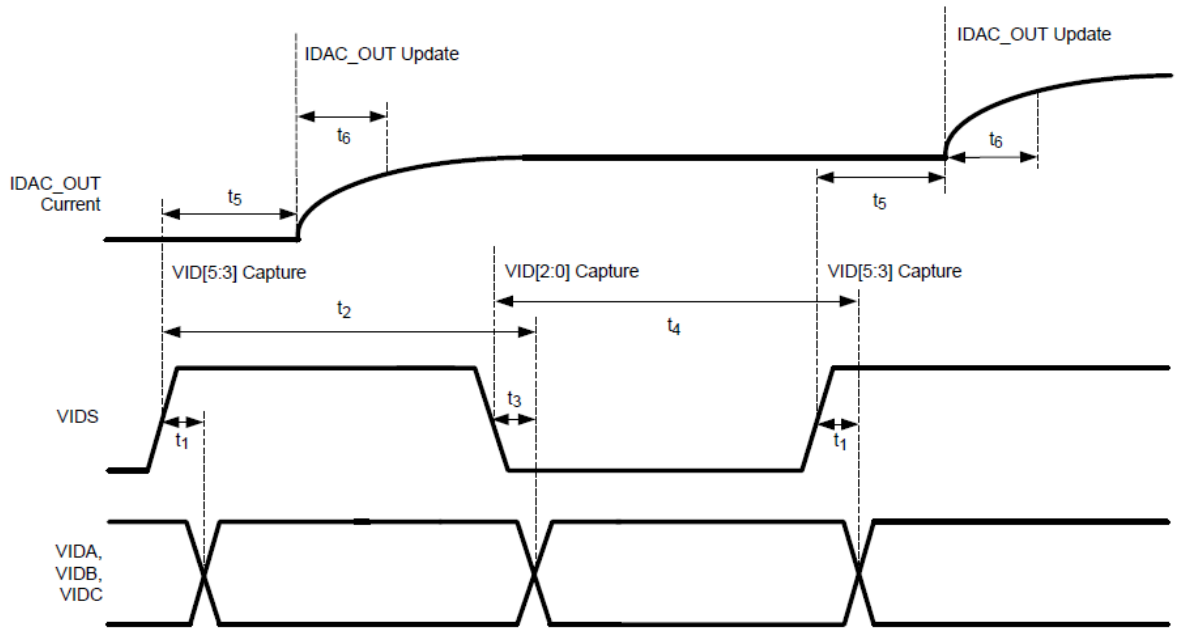


Figure 5-10: Timing diagram for LM10010 Communications [15]

Table 5-4: VID Binary Data for LM10010 Current DAC

Voltage Settings(V)	Decimal Bits	VID Binary Data
3	0	0x111111
3.3	0	0x111111
5	0	0x111111
6	0	0x111111
9	0	0x111111
12	0	0x111111
15	1	0x111110
20	1	0x111110
24	2	0x111101
36	4	0x111011

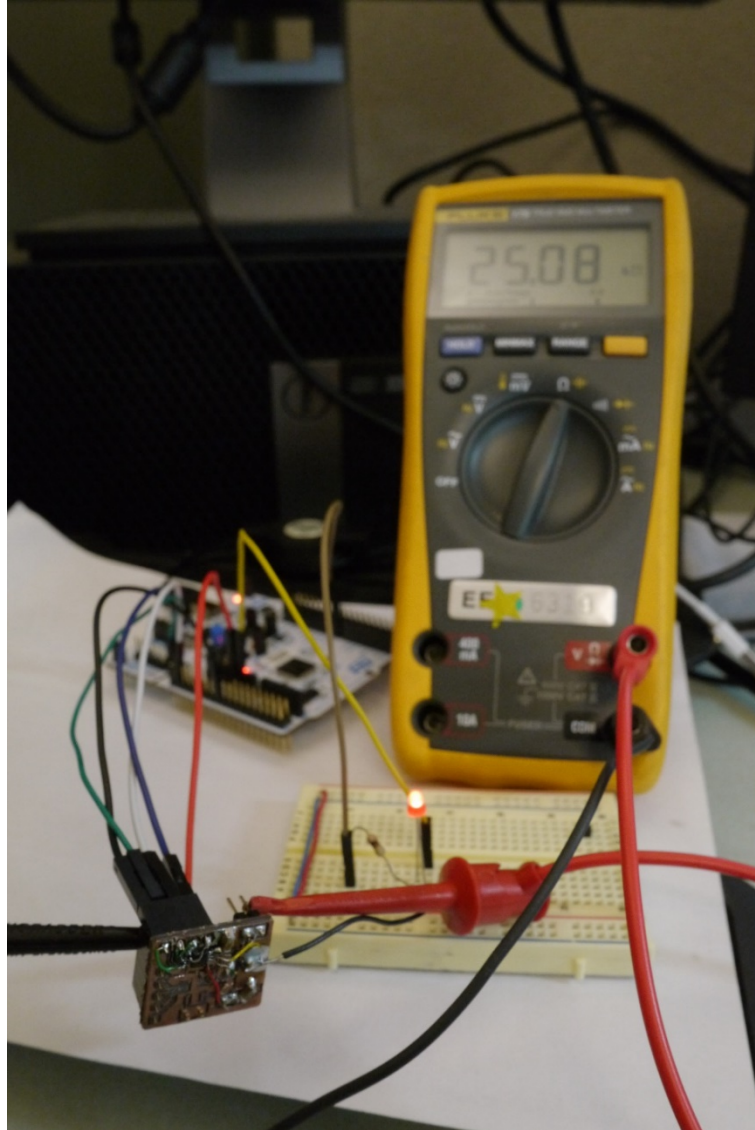


Figure 5-11: Microcontroller Interfacing with the Milled Test Board

The feedback test board is evaluated as depicted in Figure 5-11, using a Fluke multimeter to measure the feedback resistance set by the digital potentiometer. The current DAC was omitted at this initial milled test board setup because the milling machine was unable to properly trace out the LM10010 foot print. The initial test validates that the digital potentiometer is able to adjust its feedback resistance through

the microcontrollers SPI commands. An LED was used to visually indicate the microcontroller running SPI commands.

## 5.5 Soldering and Assembling

When the board and components arrive, they were inspected for any possible defects. The pads on the board should be tinned and have a coat of solder mask applied. To start assembling the printed circuit board, the small ICs were placed using a heat gun. Small components should be placed before large components, starting from the left side then towards the right side for right hand dominant soldering. For components, such as the current DAC and the buck controller which have a thermal ground pad and/or pins underneath the package, solder paste was carefully applied on the pads of the PCB to minimize the chances of shorting connections. Throughout soldering, a continuity check was performed with a digital multimeter to verify the pins has been properly soldered and are not shorted to nearby pins, ground vias, or pads. Large surface mount components such as the inductor require the pads to be tinned and need a large solder tip to heat the leads hot enough to melt the solder. Lastly, the test headers were soldered, and the input/output terminals to connect the input and output of the Smart DC/DC Wall Plug. The complete assembled PCB is shown in Figure 5-12 and Figure 5-13. Figure 5-14 and Table 5-5 show the list of GPIOs configured to pin mapping between the PCB Smart wall plug with the STM32F302R8 microcontroller.

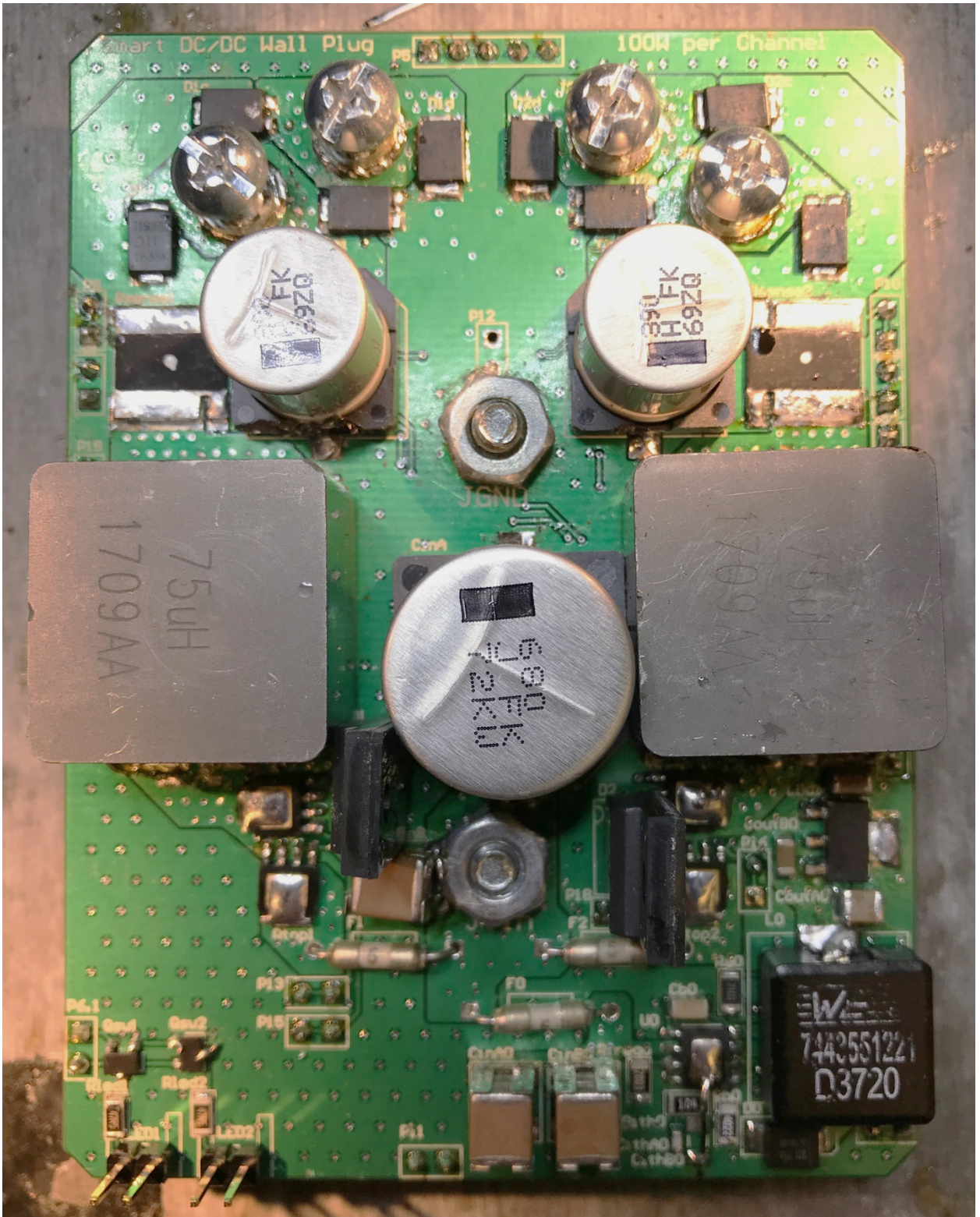


Figure 5-12: Assembled PCB (Front Side)

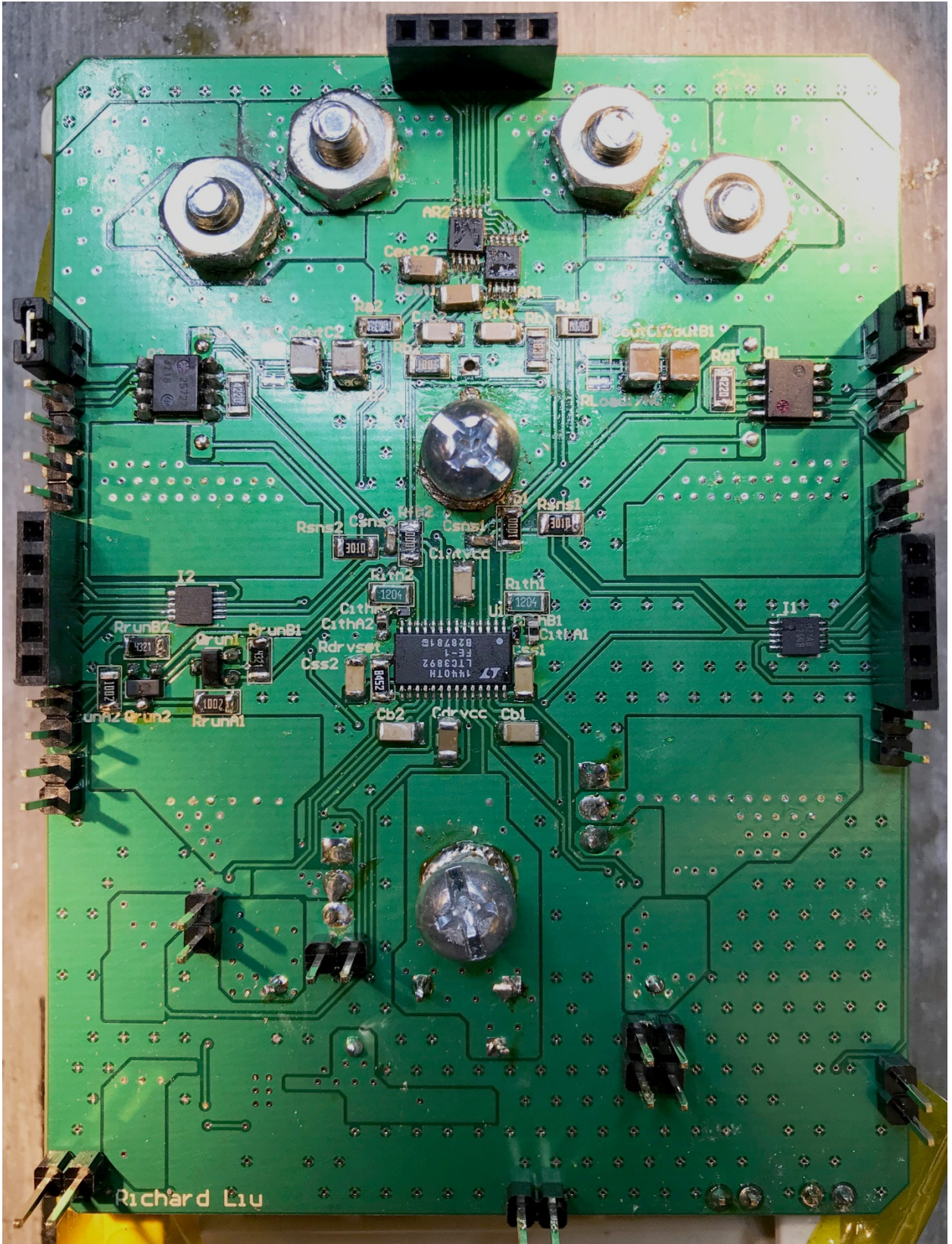


Figure 5-13: Assembled PCB (Back Side)

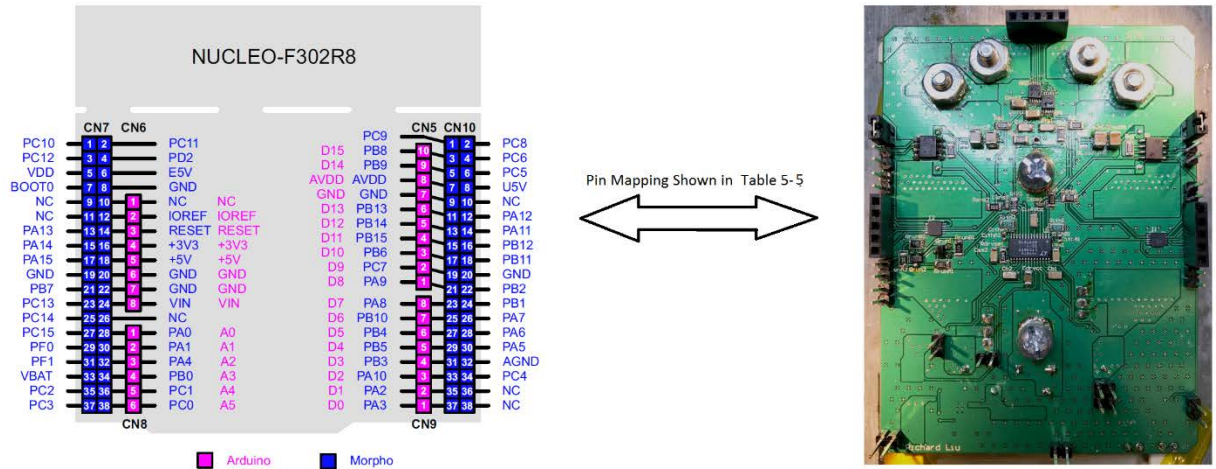


Figure 5-14: Nucleo F302R8 to PCB High Level Mapping

Table 5-5: Pinout Mapping between PCB and Nucleo F302R8 Microcontroller

Jumper	Category	uC Pinout	Pin Label
P1	ADC 1	PA0	ADC1_IN1
P2	ADC 2	PA1	ADC1_IN2
P3	VID I1	PC0	I1_VIDS
		PC1	I1_VIDA
		PC2	I1_VIDB
		PC3	I1_VIDC
		PB0	I1_EN
P4	VID I2	PA5	I2_VIDS
		PA6	I2_VIDA
		PB4	I2_VIDB
		PB5	I2_VIDC
		PB10	I2_EN
P5	SPI	PC12	SPI3_MOSI
		PC11	SPI3_MISO
		PC10	SPI3_SCK
		PA15	SPI3_NSS1
		PA4	SPI3_NSS2
P6.1	LED1	PA8	LED1_IO
	LED2	PA9	LED2_IO
P6.2	Run1	PA7	QRUN1_IO
	Run2	PB1	QRUN2_IO



## 5.6 Testing and Results

The Smart DC/DC Wall Plug testing involves a test equipment bench setup to power the PCB and to evaluate the MOSFET switching and output voltage waveforms. The test equipment bench setup is shown in Figure 5-15. Using the RIGOL DP832 programmable power supply, two channels are each set at 24V and are placed in series to provide a 48V input supply for the PCB. A RIGOL DM3058E multimeter is used to probe at the output voltage of the converter, while in parallel configuration, and to read the output load current, while in series configuration. A Keysight InfiniVision MSOX2002A oscilloscope is used to evaluate the switching waveforms and the output voltage waveform. With this test bench setup, the Smart DC/DC Wall Plug can be tested against various loads and can be evaluated based on the target design specifications such as output voltage ripple, voltage accuracy error and efficiency listed in Table 3-1.

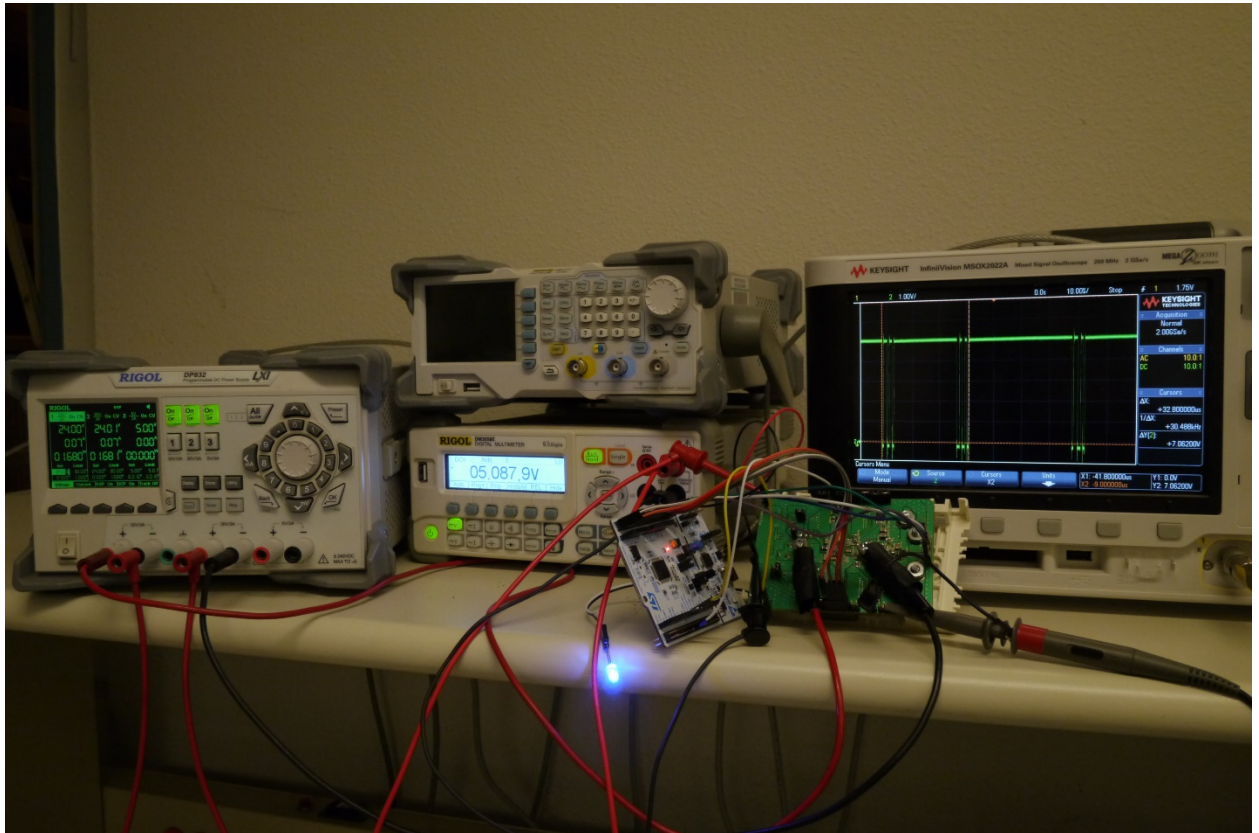


Figure 5-15: Test Setup of Smart DC/DC Wall Plug

The Smart DC/DC Wall Plug project is first tested with a Kaide handheld radio, which acts as a passive 3V load. The Smart DC/DC Wall Plug project begins with the 3V voltage setting and is able to continuously power the Kaide radio device as shown in Figure 5-16. The RIGOL DC input supply provides 48V and 70mA while the output of the power converter reads 2.758V and .915A from the RIGOL DM3058E multimeter, at this 3V load test. The efficiency relationship, output power over input power, is calculated to be 75.11%. The output voltage difference, from the expected value and the experimental value, is .242V which equates to a percent error at 8.067%. The efficiency and the output voltage percent error data are noted in Table 5-6 and Table 5-7 respectively. The Keysight oscilloscope captures the top MOSFET switching waveform and the output voltage waveform as shown in Figure 5-17. The video demonstration of the 3V test can be seen in the link provided in Figure 5-16.

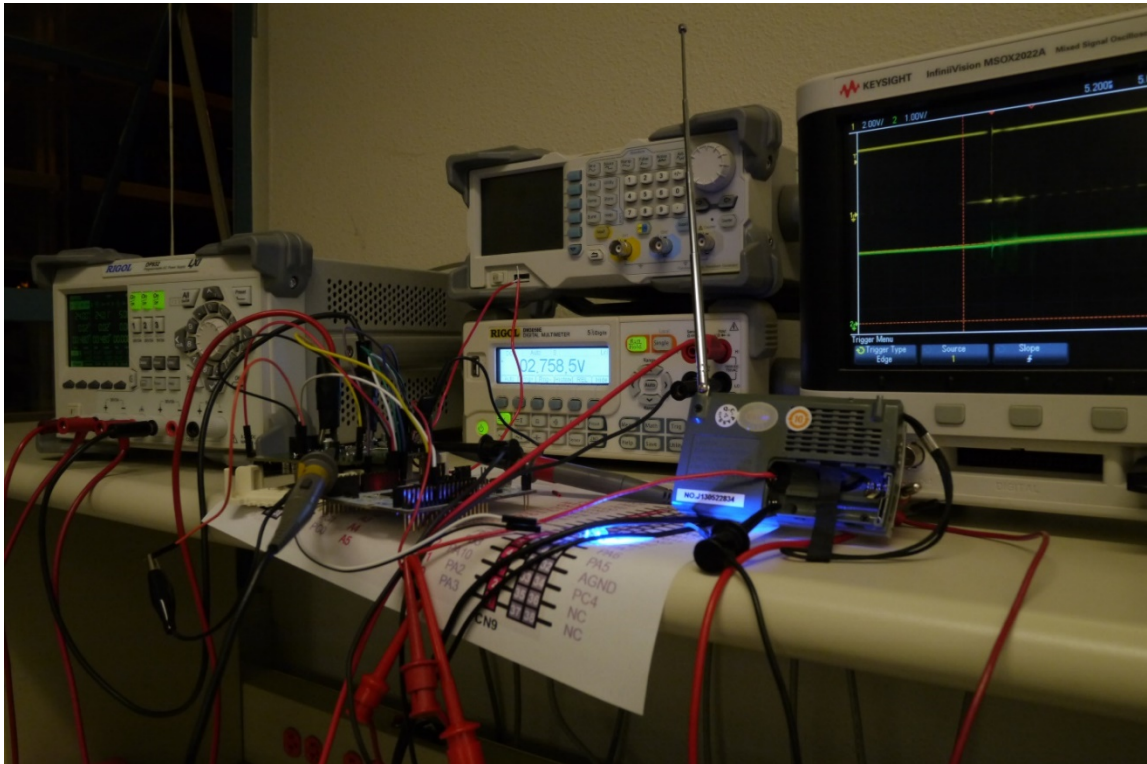


Figure 5-16: Smart DC/DC Wall Plug Kaide 3V Radio Load Test

(Link to view 3V FM radio test: <https://youtu.be/VSoT0GWhQoY>)

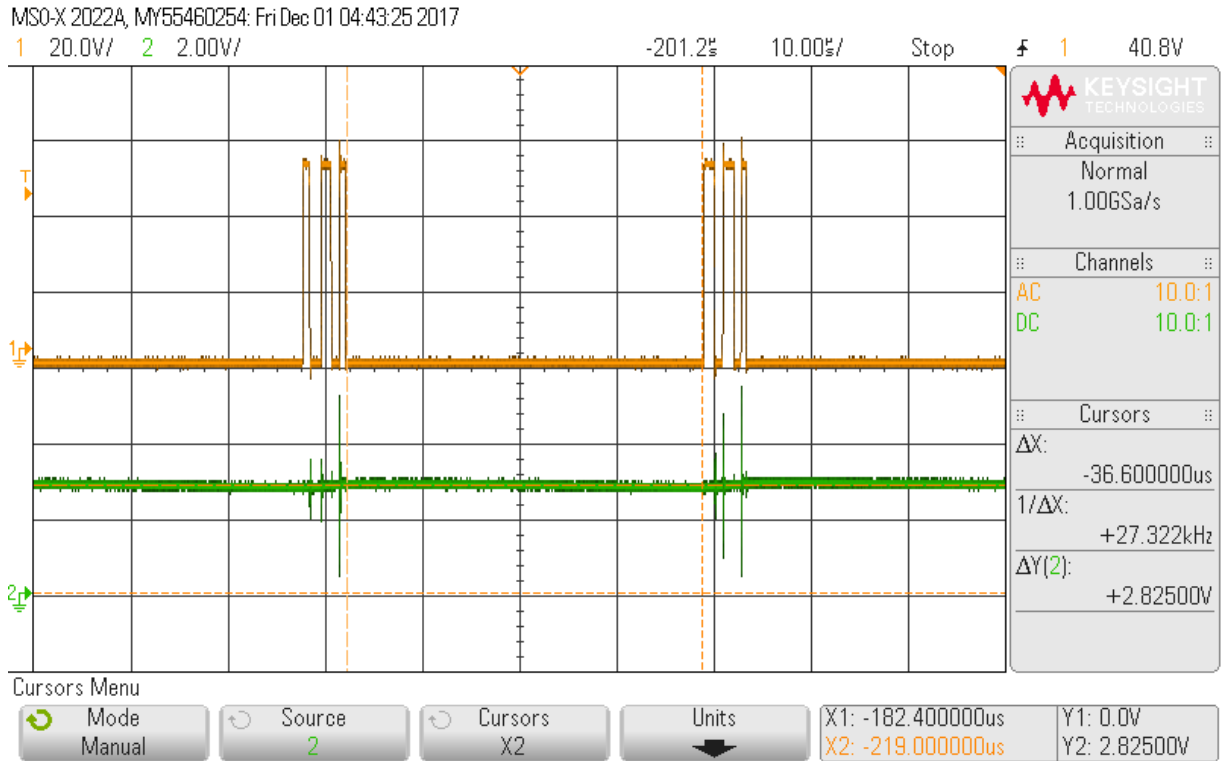


Figure 5-17: Top MOSFET Gate Drive (CH1) and 3V Output Voltage (CH2)

The output voltage ripple of the Smart DC/DC Wall Plug under the 3V Kaide radio load test is shown in Figure 5-18. The waveform is AC coupled and the cursors, measuring the wave like ripple, reads 90mV peak to peak. Along the rising curve of the voltage ripple, noise and voltage spikes are visible and reaches 747mV peak to peak. The noise and voltage spikes are caused by abrupt changes of current from the synchronous rectifiers. The abrupt changes of current are translated into voltage through the ESR of the capacitor and are viewed as voltage spikes. Excluding the noise and voltage spikes, the Smart DC/DC Wall Plug performs well against the design specification in Table 3-1 under the output voltage ripple criteria. The output voltage ripple performance of the Smart DC/DC Wall Plug under the 3V Kaide radio test is tabulated in Table 5-6.

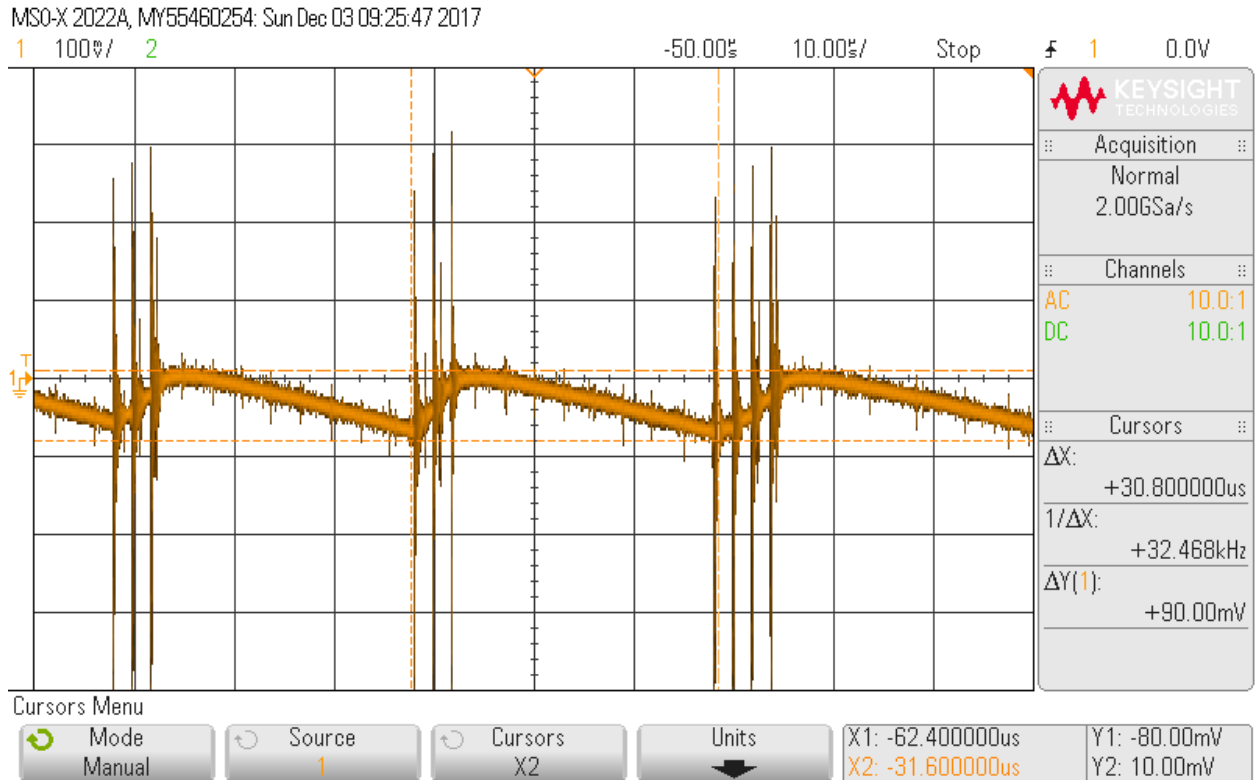


Figure 5-18: Output Voltage Ripple under 3V Load Test

The next load test conducted was the 5V load test conducted through a Samsung cell phone. For this load test, the Smart DC/DC Wall Plug connects to a USB female port to power the 5V cell phone through USB as shown in Figure 5-19. The converter produces 5.11V at the 5V configuration setting and was able to charge the Samsung cell phone. The output voltage percent error falls within the design specification of 3% as shown in Table 5-7. During this test, 80mA is being drawn from the input power supply and .548A is being drawn from the DC/DC power converter, yielding 72.92% efficiency as shown in Table 5-6. A video recording can be found in the link provided under Figure 5-19. The switching gate signal for the top MOSFET and the output voltage waveform is shown at Figure 5-20. In Figure 5-21, the output voltage ripple is AC coupled and is measured to be 147.5mV peak to peak. The voltage ripple

percentage evaluation is shown in Table 5-8. The voltage ripple has increased from the 3V load test voltage ripple due to increase in load current and load voltage. Noise and voltage spikes are still present and the total peak to peak AC voltage is 1.0125V.

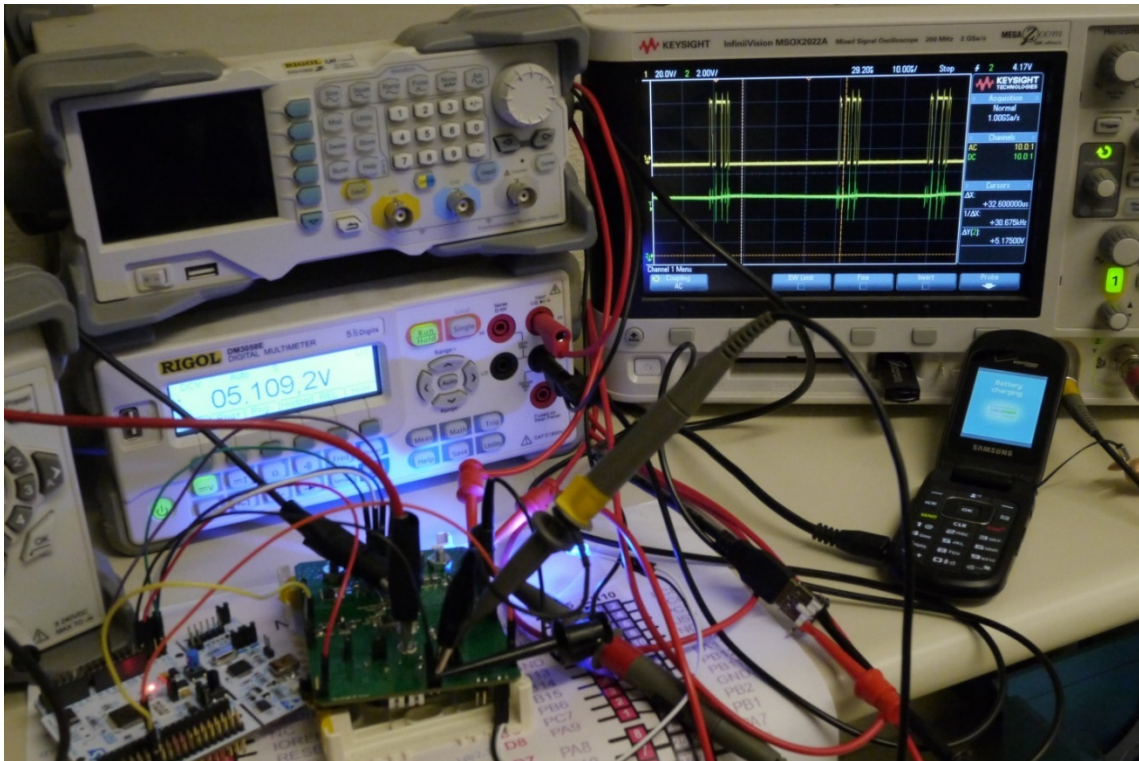


Figure 5-19: Smart DC/DC Wall Plug Samsung 5V Cell Phone Load Test

(Link to view 5V cell phone test: <https://youtu.be/WzTcCdmESbE>)

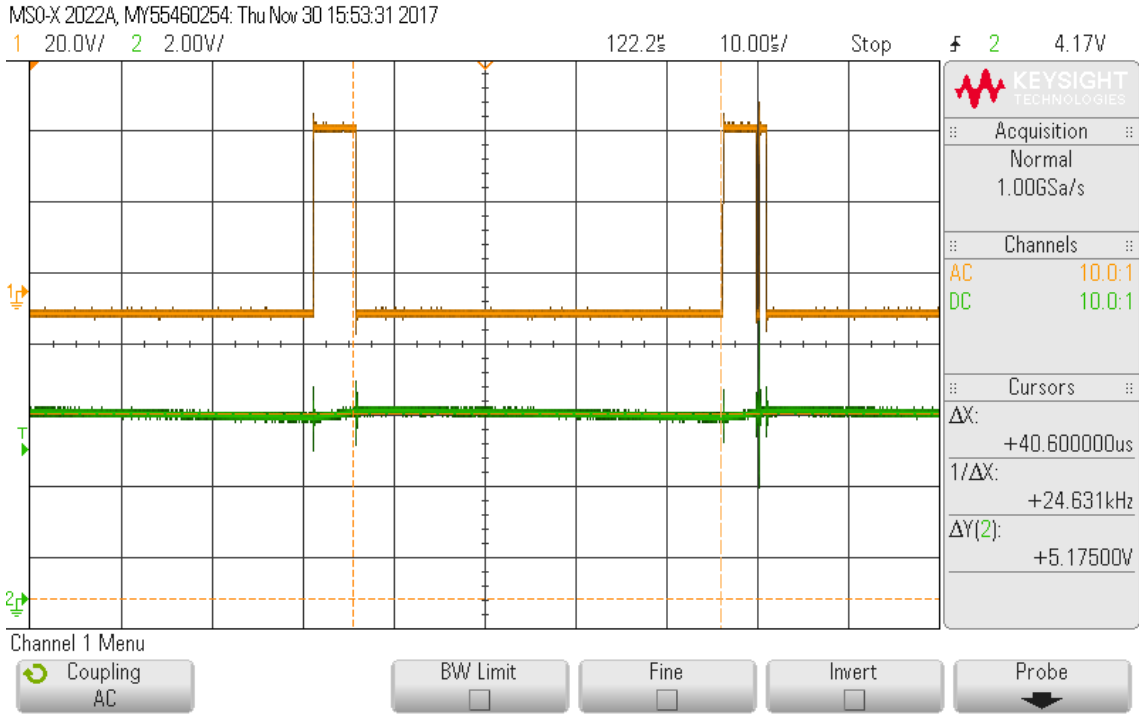


Figure 5-20: Top MOSFET Gate Drive (CH1) and 5V Output Voltage (CH2)

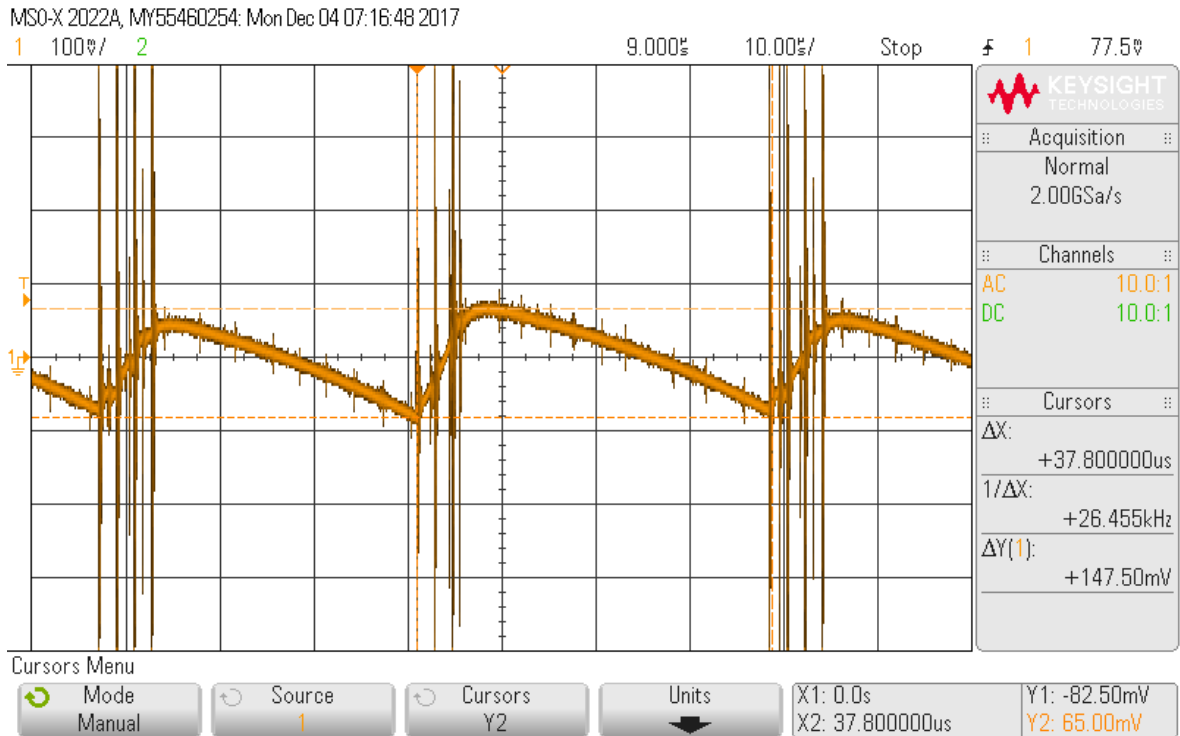


Figure 5-21: Output Voltage Ripple Waveform under 5V Load Test

The third load test on the Smart DC/DC Wall Plug was to power the Panaflow 12V DC brushless fan. At this test, the PCB output terminals are directly connected to the power lines of the 12V DC fan as shown in Figure 5-22. The input power supply of the Smart DC/DC Wall Plug reads 60mA at 48V. The power converter at its 12V setting outputs 12.1V and provides 70mA of load current. The efficiency during this test yields 29.56% and is listed in Table 5-6. The output voltage percent error of the converter at the 12V load test results 1.33%, as shown in Table 5-7. The Smart DC/DC Wall Plug continuously powers the fan and can be viewed in the link provided under Figure 5-22. The switching MOSFET waveform and the 12V output voltage waveform from the Keysight oscilloscope is shown in Figure 5-23. In Figure 5-25, the output voltage ripple shows a 177mV peak to peak voltage fluctuation and voltage spikes up to 1.027V peak to peak. Although, the 12V condition yields the largest voltage ripple, the percentage against the output voltage is the smallest as shown in Table 5-8.

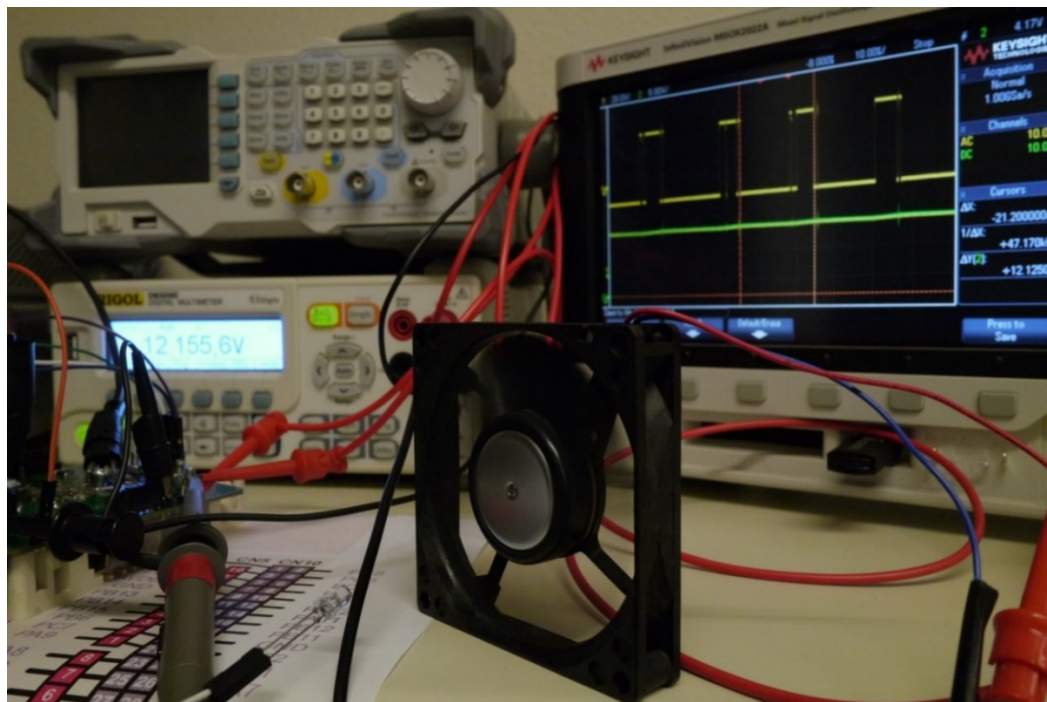


Figure 5-22: Smart DC/DC Wall Plug 12V DC Fan Load Test

(Link to view 12V fan load test: <https://youtu.be/do7pcB07D2I>)



Figure 5-23: Top MOSFET Gate Drive (CH1) and 12V Output Voltage (CH2)

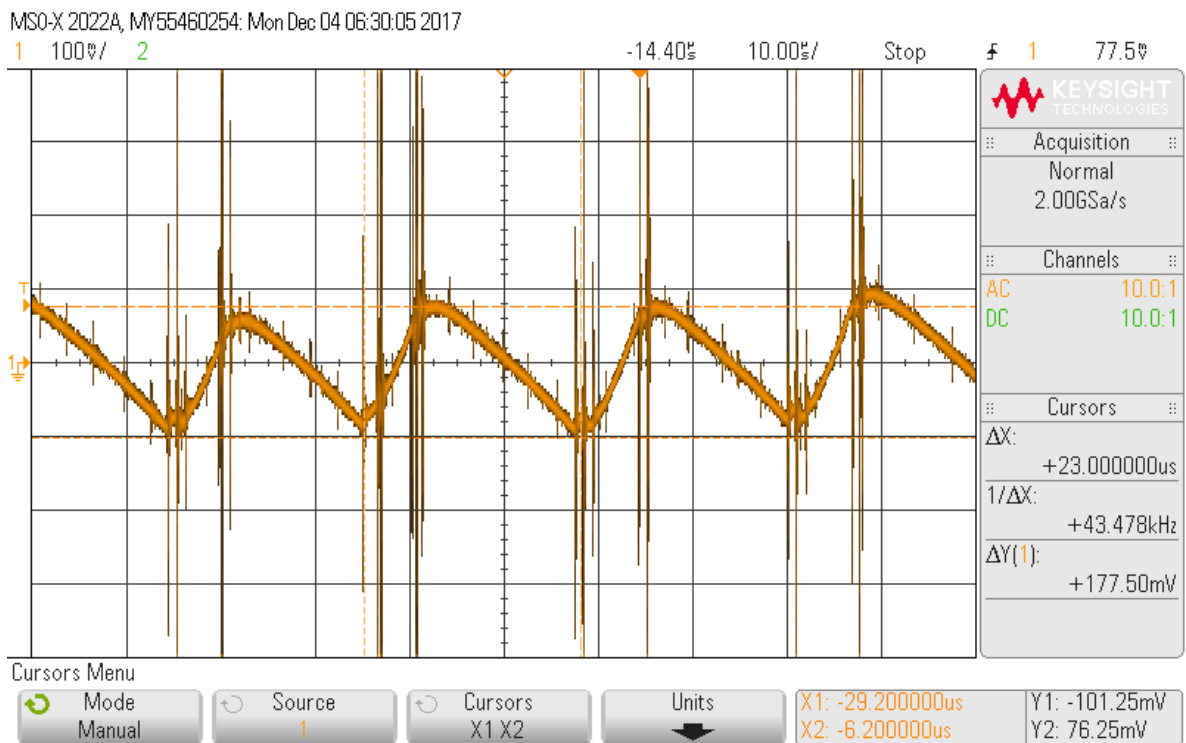


Figure 5-24: Output Voltage Ripple Waveform under 12V DC Fan Load Test



From the 3V, 5V, and 12V load tests, the efficiency, output voltage percent error and output voltage ripple of the Smart DC/DC Wall Plug can be evaluated with respect to the target design specifications, Table 3-1. The power efficiency evaluation of the Smart DC/DC Wall Plug falls below the targeted 85% efficiency, especially at the 12V DC Fan test. The 12V DC load test demonstrates that under low load current conditions, the efficiency of the power converter is fairly poor. Referring to the “Efficiency versus Output Current” plot in Figure 5-25 from the LTC3892 datasheet, the efficiency of the Smart DC/DC Wall Plug converter should follow most closely to the black dotted line, stated as  $V_{in}=50V$ . The discrepancies can be explained by difference in circuit schematics and slight differences in the input and output voltage conditions. The target 85% efficiency can theoretically be reached at loads greater than 2 amps. For the output voltage accuracy, shown in Table 5-7, the Smart DC/DC Wall Plug achieved the 5V and 12V output voltage within 3% tolerance. At the 3V load test, the feedback setting at initial startup is defaulted at certain potentiometer settings and would need to be further calibrated reduce the percent error down from 8% to 3%. Lastly, for the output voltage ripple, the targeted design specification was to have a ripple less than 5% of the set output voltage. If not considering the voltage spikes and noise, the steady state voltage ripple from the three load tests falls within specification.

Table 5-6: Power Efficiency Evaluation

Test	Input Voltage (V)	Input Current (A)	Output Voltage(V)	Output Current (A)	Efficiency (%)	Target Design Spec (%)
3V Radio	48	0.07	2.758	0.915	75.11%	~85%
5V Cell Phone	48	0.08	5.11	0.548	72.92%	~85%
12V DC Fan	48	0.06	12.16	0.07	29.56%	~85%

Table 5-7: Output Voltage Percent Error Evaluation

Test	Output Voltage (V)	Target Output Voltage (V)	Output Voltage Percent Error (%)	Target Design Spec
3V Radio	2.758	3	8.067%	3%
5V Cell Phone	5.11	5	2.200%	3%
12V DC Fan	12.16	12	1.333%	3%

Table 5-8: Output Voltage Ripple Design Spec Evaluation

Test	Output Voltage (V)	Output Voltage Ripple (V)	Output Voltage Ripple (%)	Design Spec
3V Radio	2.758	0.09	3.263%	<5%
5V Cell Phone	5.11	0.1475	2.886%	<5%
12V DC Fan	12.16	0.1775	1.460%	<5%

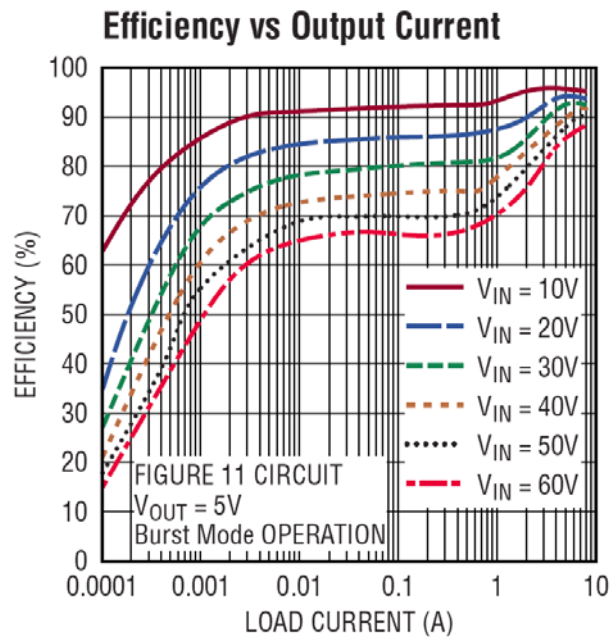


Figure 5-25: Efficiency versus Load Current of LTC3892 [9]

## 5.7 Smart DC/DC Wall Plug Assembly

One of the goals of the project was to confine the Smart DC/DC Wall Plug electrical design to the NEMA duplex device wall form factor, shown in Figure 3-3. The enclosure and wall receptacle hardware can be obtained from a hardware store like Home Depot or ACE. The present electrical hardware requires wiring and modifications to connect from the PCB output terminals to the terminals from the wall receptacles. Originally the “hot” terminals from the two channels on the NEMA wall receptacle are shorted together. The modification was made to separate the “hot” connection from the two receptacles so that the two channels can output different voltages. The deepest available depth of the enclosure box was chosen for this project to house the project. However, the microcontroller was not able to fit inside the box and is placed outside of the enclosure. Two holes were drilled to allow LEDs to surface the front side as visual indicators of the Smart DC/DC Wall Plug. Figure 5-26 and Figure 5-27 displays the front and back look for the Smart DC/DC Wall Plug. To distinguish this outlet from typical AC wall outlets, black tape is placed around the enclosure as parallel lines to indicate DC current. The assembled PCB is wired and placed inside the enclosure. The red and black wires on the sides are the input power supply connections.



Figure 5-26: Smart DC/DC Wall Plug Enclosure Front Side

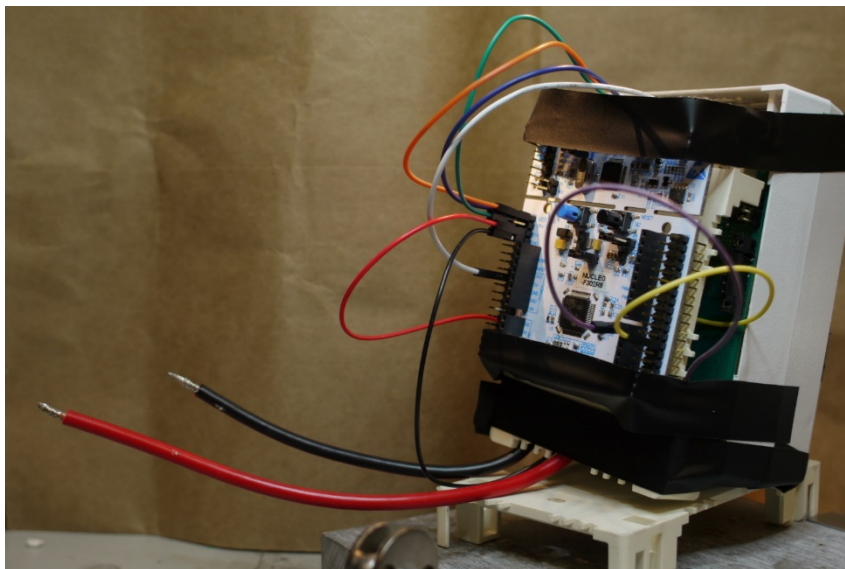


Figure 5-27: Smart DC/DC Wall Plug Back Side

## Chapter 6

### CONCLUSION

The Smart DC/DC Wall Plug project presented in this thesis serves as a proof of concept to implement the one wall-outlet solution to extract power from the 48V DC bus in the DC House system, and to provide automatic DC output voltage adjustment for DC loads. The Smart DC/DC Wall Plug sets to improve on energy savings by eliminating the AC conversation losses while maintaining the convenience of using the ubiquitous wall plug form factor. In this iteration of the Smart DC/DC Wall Plug design, the objective is to provide two channels of 100W rated power from 3V-36V. Additionally, a current DAC was introduced as a second feedback adjustment to set the output voltage of the Smart DC/DC Wall Plug.

The project served as a great opportunity to gain firsthand experience going from a conceptual design of the Smart DC/DC Wall Plug to creating the project and successfully powering loads such as the 3V Kaide handheld radio, the 5V Samsung phone and the 12V Panaflo DC fan. The Smart DC/DC Wall Plug project also delve into embedded system work which enabled the power supply to dynamically change its output voltage based on the load requirements. The proposed algorithm for the Smart DC/DC Wall Plug begins with its 3V setting and checks if load current is being drawn. The Smart DC/DC Wall Plug steps its output voltage until load current is detected and sets to the appropriate nominal voltage setting.

In terms of meeting the design specifications, results from the hardware implementation and test show that the proposed design was able to achieve its targeted output voltage within 3% except for the case of the 3V load. The percent output voltage ripple requirement of <5% was achieved in all three load tests. The efficiency measurement, however, was a tricky one to use a performance criterion due to the fact

that the efficiency of a converter depends so much on load condition. Typically, the efficiency profile starts from a very low value at low load and increases to its peak value at higher load conditions. The 12VDC load test demonstrated this point, where the fan load was drawing a small 0.07A, which consequently yielded a low 29.56% efficiency.

There were some shortcomings and areas of improvements in future iterations of the Smart DC/DC Wall Plug project. Some areas to improve are the Smart DC/DC Wall Plug's algorithm implementation, voltage range, thermal considerations, and space integration. The algorithm implementation to coordinate the feedback control could be further refined. The Smart DC/DC Wall Plug relies on current sensing to determine the settings on the feedback elements and becomes somewhat problematic to coordinate with the load if the load voltage changes. To dynamically set an output voltage that is appropriate to the load at any case, it would be beneficial to investigate on a communication bus to communicate with the load electronically to determine the output voltage, similar to how USB-C issues a power contract. This implementation may offer more control stability and versatility with the Smart DC/DC Wall Plug appliance as more technologies are developing devices powered through USB-C. The next item is to improve on the voltage range. Future Smart DC/DC Wall plugs should strive to provide more voltage levels from 0V up to its line voltage. Another area of improvement can be geared towards the mechanical side of the smart wall plug such as thermal and space integration. Heat dissipation due to power loss was not accounted for and heat sinks were not considered due to space constraints. The space integration in a new and optimally designed enclosure may be better suited than the traditional NEMA wall outlet designs. It will be a challenge to implement two 100W power supplies with high performance, efficiency, accuracy, while having the dynamic ability to change between 0V to 48V in a constrained 2.8 inch by 4-inch enclosure space where typical two outlet receptacles are sized.

## BIBLIOGRAPHY

- [1] Hartman, Robin. "A Powerful History: The Modern Electrical Outlet." *Illumin.usc.edu*, University of Southern California, 19 June 2008, [illumin.usc.edu/122/a-powerful-history-the-modern-electrical-outlet/](http://illumin.usc.edu/122/a-powerful-history-the-modern-electrical-outlet/).
- [2] N. E. M. Association, "Wiring Devices - Dimensional Specifications," 2016.
- [3] C. D. Xu and K. W. E. Cheng, "A survey of distributed power system AC versus DC distributed power system," in *2011 4th International Conference on Power Electronics Systems and Applications, PESA 2011*, 2011.
- [4] AMAZON, [www.amazon.com](http://www.amazon.com).
- [5] Taufik. "The DC House Project." The DC House Project. N.p., n.d. Web. Apr. 2014. <http://www.calpoly.edu/~taufik/dchouse/>
- [6] Sibal, Edward, "Smart Wall Plug Design for the DC House Project." Master's Thesis, California Polytechnic State University San Luis Obispo, 2012 DigitalCommons@Calpoly. Web. Apr. 2014.
- [7] K. R. Mendoza, "SMART WALL OUTLET DESIGN AND IMPLEMENTATION FOR THE DC HOUSE PROJECT," no. June, 2014.
- [8] "Advanced Circuits." *PCB Printed Circuit Board File Creation Calculator | Advanced Circuits*, [www.4pcb.com/trace-width-calculator.html](http://www.4pcb.com/trace-width-calculator.html).
- [9] N. External, B. Diodes, O. O. Reduces, R. Input, P. Supply, I. Noise, S. Continuous, B. Mode, I. P. Systems, H. Voltage, and B. Operated, "LTC3892/LTC3892-1/LTC3892-2 60V Low I," pp. 1–38.
- [10] Taufik. *Power Electronics*. Vol. 12, Cal Poly State University, San Luis Obispo, 2015.
- [11] "High Performance , Low Power , Rail-to-Rail Precision Instrumentation Amplifier AD8422 \* PRODUCT PAGE QUICK LINKS," 2015.
- [12] Taufik. *Power Supply Design: Components and Control*. Vol. 4, Cal Poly State University, San Luis Obispo, 2016.
- [13] A. Devices, B. The, and W. Voltage, "Choosing the Correct digiPOT for Your Application," *Options*, pp. 1–4.
- [14] A. Devices, "SPI Interface and 50-TP Memory Digital Rheostat AD5270/AD5271," *Current*, p. 24, 2010.
- [15] Texas Instruments, "LM10010 VID Voltage Programmer for Point of Load Regulator", LM10010 datasheet, July 2011 [Revised March 2013].
- [16] M. Autolab, "User Manual," no. November 2016, 2017.
- [17] M. Ring, "QED REPORT," *QED Rep.*, pp. 1–6, 2017.