Modular Multilevel Converter Grid-Interface for Klystron Modulators: an Augmented Modulation Scheme for Arm Balancing

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***Abstract*—This paper discusses the control of a Modular Multilevel Converter (MMC) used as a grid-interface for the klystron modulators in the Compact Linear Collider (CLIC). The converter has a DC side load which takes short-duration power pulses, causing high DC side power fluctuations that are not tolerable if seen by the AC grid. The DC-AC power decoupling capability of the MMC enables mitigation of the power ripple on the AC side, guaranteeing compliance with power quality requirements. However, the pulse repetition rate of the CLIC modulators is synchronised the the 50 Hz AC grid and this induces permanent power imbalance in the arms of the MMC, causing voltage deviation and over-modulation unless appropriate balancing strategies are implemented. Unlike existing arm balancing methods that control 50 Hz circulating currents to balance the arm powers, the method proposed in this paper introduces an augmented modulation strategy where modulation signals are redistributed among arms based on the demand from a balancing controller. The resulting controller has lower complexity and its simple structure enables an easier design of the balancing loop, which guarantees predictable dynamics in operation. The effectiveness of the method has been demonstrated in simulation for the full scale CLIC converter ratings and experimentally on a 7 kW MMC prototype operating with a 3.3 kA pulsed DC load.**

***Index Terms*—Arm balancing control, Grid-connected converter, Pulsed Power, Modular Multilevel Converter, Modulation strategy, Klystron Modulator**

I. Introduction

Future high-luminosity colliders, such as the Compact Linear Collider (CLIC), require input power supplied to the accelerating cavities via high voltage, high power pulses. Klystron modulators, in the case of CLIC, draw short duration high current pulses with a repetition frequency of 50 Hz from a medium voltage DC source, to produce high voltage pulses at the klystrons [1]. The power electronic grid-interface for the klystron modulators has to be highly efficient and reliable, capable of processing high powers and must be able to prevent propagation of the pulsed power effects from the DC side to the AC grid [1], [2]. The Modular Multilevel Converter (MMC) shown in Figure 1 has been selected as a suitable topology [3] due to its modularity, efficiency and high quality AC waveforms [4]. Additionally, the independent control of AC and DC side currents [5] enables cancellation of the DC side power pulsation from the AC grid.

Unlike typical HVDC/MVDC applications, where the MMC operates without a bulk DC capacitor, in the application of interest the MMC operates with a DC link comprising the capacitor banks of the klystron modulators, as shown in Figure 2. These are periodically discharged by the high current

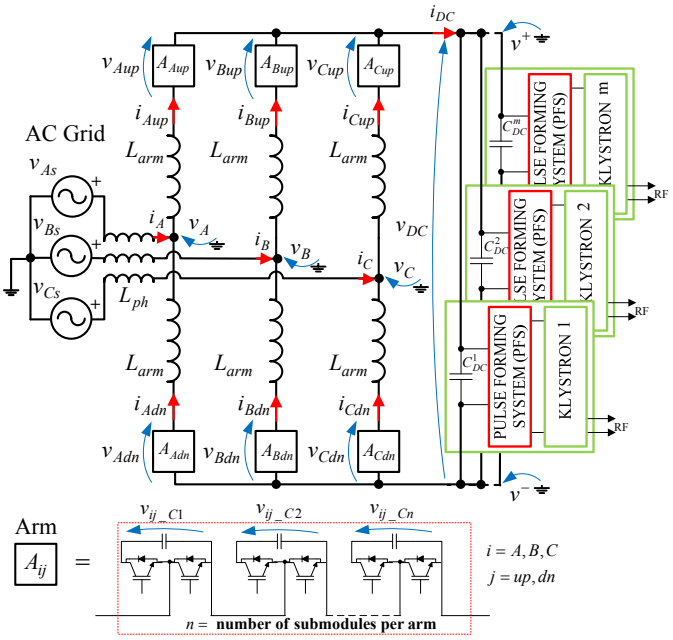

Fig. 1. Three phase Modular Multilevel Converter grid-interface for klystron modulators.

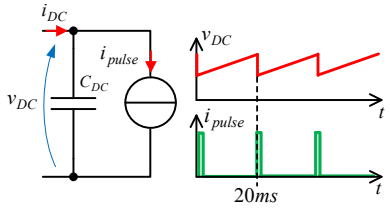

Fig. 2. Lumped equivalent circuit of the klystron modulators.

pulses, with a duration of approximately 140 μs, drawn by the modulators. In between pulses, the grid-interface converter draws power from the AC grid to restore the voltage on the capacitor bank. For CLIC, the capacitors are designed to limit the droop to 10 % of the nominal DC voltage. The main challenge for the grid-side converter and its control is to ensure an AC power fluctuation below 2 % [1], [2]. The nominal converter and klystron modulator ratings, obtained by system optimisation studies [3], are summarised in Table I. The MMC parameter design is based on [6].

Early solutions investigated to suppress the DC power fluctuation were based on the insertion of a fast series voltage compensator in each modulator [7], requiring a high bandwidth to respond to the pulse without affecting the DC voltage. In [1], an intermediate DC/DC conversion stage with high

bandwidth current control is used in each modulator to minimise the voltage ripple seen by the grid-interface. However, taking advantage of the internal energy storage, an MMC can generate the required AC currents despite large DC power fluctuations, thus minimising the AC power fluctuation with a single converter stage that does not affect cost and complexity of the modulators and does not require time critical controllers [8].

Unfortunately however, the DC current pulse repetition rate in this application matches the AC grid frequency and as a result it introduces a constant source of imbalance between the cell capacitor voltages of the upper and lower MMC arms [9], [10]. This leads to overmodulation and distortion of the AC power [11] unless adequate balancing controllers are implemented. Various different arm balancing methods have been reported so far in the literature, and they can be classified as those acting on the specific cell modulation signal to guarantee correct cell capacitor voltage [12]–[14] and others manipulating the circulating current reference [15], [16]. These methods are aimed at compensating for small converter asymmetries due to non-idealities of the converter and transient imbalances. As a result, the dynamics of the small correction terms are not significant for the overall converter operation, provided that stability is ensured. For this reason, balancing controller design is not typically studied in detail in the literature.

A preliminary arm balancing method for the CLIC grid-interface MMC was proposed by the authors in [10]. The method was based on the addition of a 50 Hz component to the circulating current in quadrature with the 50 Hz component of the DC voltage ripple. The main drawback of the solution was its sensitivity to the position of each pulse within the AC voltage period, with some critical positions were arm balancing was not possible, resulting in high AC power fluctuation. Therefore, the method would require the klystron modulators to be phase-locked with the grid, to guarantee that the pulses does not occur in the non-controllable regions. The solution in [10] belongs to the arm balancing methods manipulating the circulating current reference, and like other similar methods it requires the generation of an AC circulating current reference and the implementation of suitable controllers, for example Proportional-Integral (PI) or Proportional-Resonant (PR) [17], to track it.

A preliminary analysis of the new method proposed in this paper was first presented in [9]. However, only the basic concept was discussed and validated in steady state operation. No in-depth analysis of the balancing control design and of the interactions with the other controllers of the MMC was provided. The aim of this paper is to fill that gap, providing a comprehensive analysis and design of the proposed balancing controller, validated by a set of experimental results on a 7 kW MMC lab demonstrator with a 3.3 kA, 150 μs pulsed load emulator.

The paper is organised as follows. In Section II, MMC operation is briefly reviewed. Section III provides an analysis of the arm power imbalance caused by the pulsed DC load. Sections IV and V discuss the new arm balancing control algorithm based on the augmented modulation scheme, providing a detailed analysis of the controller design and of its interaction with the existing circulating current controller. Section VI presents results from a simulation study in PLECS to validate the proposed arm balancing method and its performance on the full-scale grid-interface MMC for the CLIC (Table I). Finally, in Section VII the proposed method is experimentally validated on a laboratory-scale prototype (Table I) and Section VIII gives the conclusions of the work.

Remark: throughout the paper, equations are given only for phase A of the converter for brevity.

TABLE I. Converter and load parameters.

Description	Full-scale rating	Experimental rig rating
Rated power	16.6 MW	7 kW
DC voltage	20 kV	400 V
AC voltage	10.5 kV	225 V
Number of cells per arm	20	4
Nominal cell voltage	1 kV	100 V
Phase inductance	3.6 mH	3 mH
Arm inductance	1.8 mH	1.5 mH
Cell capacitance	13 mF	3.3 mF
DC link capacitance	8 mF	8.5 mF
DC voltage droop	2 kV	48 V
Pulse frequency	50 Hz	50 Hz
Peak pulse current	118 kA	3.3 kA
Pulse duration	140 μs	150 μs

II. MMC GRID-INTERFACE BASIC OPERATION AND CONTROL ARCHITECTURE

The arrangement of an MMC grid-interface feeding a set of m klystron modulators is shown in Figure 1. Table I gives the total average powers and the peak pulsed current drawn by the Pulse Forming Systems (PFSs) in the full power CLIC converter and in the laboratory scale demonstrator. From the different possible arrangements for the real application [18], the arrangement and ratings considered here are $m = 82$ synchronised klystrons per MMC, each rated for $29MW$ pulsed power, for a total of $2.37GW$. The pulse duration is $140\,\mu$s, giving an average power of $16.6MW$ if the pulse repetition frequency is $50Hz$. As a result, each power pulse corresponds to a current pulse of $118kA$ drawn from the total equivalent DC link capacitor C_{DC}. For the purpose of the analysis in this section and the following one, the lumped circuit in Figure 2 will be assumed where all the klystrons and the PFSs are modelled as a DC link capacitance C_{DC} in parallel with a current source drawing current pulses. The same lumped representation has been adopted in the design of the experimental rig.

In the following paragraphs, a review of the MMC [4] operating principle and control is briefly presented. As shown in Figure 1, each phase has two sets of controllable chains of half bridge submodules with floating capacitors (upper and lower arm) and two arm inductors. The AC side equation for phase A can be written as:

$$v_{As} - L_{eq}\frac{di_A}{dt} + \frac{v_{Aup} - v_{Adn}}{2} = \frac{v^+ + v^-}{2}, \qquad (1)$$

where $L_{eq} = L_{ph} + \frac{L_{arm}}{2}$ is the equivalent AC circuit inductance. According to Eq. (1), a dq AC grid current controller can be implemented that generates the AC voltage demand v_{AC_A} and the AC modulation signals for the upper

(v_{Aup}) and the lower (v_{Adn}) arms in each phase as shown in Figure 3. The AC current references are driven by the total energy controller, which guarantees that the sum of all the submodule capacitor voltages v_{TOT} is maintained at the nominal value by adjusting the power absorbed from the AC grid. The relationship between the AC voltage demand and the upper and lower arm modulation signals can be written for phase A as:

$$v_{AC\_A} = -\frac{v_{Aup} - v_{Adn}}{2}, \tag{2}$$

where the converter arms are assumed to be ideal controlled voltage sources, imposing the voltage demand of the current controller, i.e. the NLC-PWM and cell sorting blocks [20], [21] in Figure 3 are neglected for simplicity. A second equation can be written for the DC side of the converter:

$$v_{Aup} + v_{Adn} - 2L_{arm}\frac{di_{Acirc}}{dt} = v^+ - v^- = v_{DC}, \tag{3}$$

where i_{Acirc} is the circulating current of phase A, defined as:

$$i_{Acirc} = \frac{i_{Aup} + i_{Adn}}{2}. \tag{4}$$

From the DC side equation, it can be seen that the circulating current can be controlled by acting on the control variable:

$$v_{DC\_A} = v_{Aup} + v_{Adn}. \tag{5}$$

In the CLIC, the MMC must control the voltage across C_{DC}, recharging it after each load pulse, as indicated in the overall control scheme shown in Figure 3. An average DC voltage controller can be implemented by generating a reference for i_{DC} which is then divided into three identical circulating current references for the three phases. The low frequency circulating currents are controlled by Proportional-Integral (PI) controllers. The circulating current references are then corrected with a small DC component generated by a phase balancing controller, that ensures equal energy redistribution among phases [10]. It should be noted that this simplified analysis is true under the assumption that the arms can be treated as ideal voltage sources, and neglecting the impact of the second harmonic circulating currents [11], [19]. The modulation demands for the upper and lower arms of phase A can be described by equation Eq. (6) by combining the demands from the AC and DC side controllers:

$$v_{Aup} = \frac{v_{DC\_A}}{2} - v_{AC\_A}, \quad v_{Adn} = \frac{v_{DC\_A}}{2} + v_{AC\_A}. \tag{6}$$

III. Pulsed Load Effects

With a non-pulsed load, the AC and DC controllers discussed in the previous section will enable correct operation of the converter. However, in the application under study the DC voltage has a 50 Hz ripple due to the klystron pulse repetition frequency. In the controller in Figure 3, the DC voltage ripple will be transferred to the upper and lower arm voltages Eq. (6) by the action of the circulating current controller, and will interact with the 50 Hz components of the arm currents:

$$i_{Aup} = i_{Acirc} + \frac{i_A}{2}, \quad i_{Adn} = i_{Acirc} - \frac{i_A}{2} \tag{7}$$

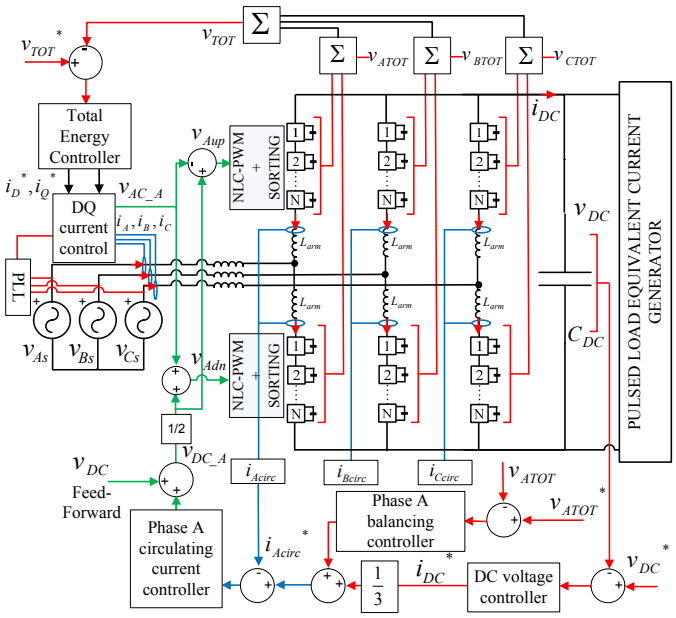

Fig. 3. Architecture of the DC side and AC side controls of the MMC grid-interface for klystron modulators - all controllers are Proportional-Integral (PI).

to produce a non-zero average power with opposite signs in the arms of each phase. This causes divergence of the cell capacitor voltages, even if capacitor voltages are perfectly balanced within each arm and the converter operates in global power balance. As a consequence, overmodulation will ultimately occur, leading to AC power distortion [10].

If the modulation strategy follows the conventional one given by (6), arm balancing can be achieved by acting on the circulating current reference in each phase through an additional AC component coming from an arm balancing controller. Such an arm balancing controller would generate an AC circulating current reference according to existing balancing techniques [10], [16]. Alternatively, as proposed here, arm balancing can be achieved by redistributing the arm voltage references among the arms, without an explicit generation of a balancing circulating current component, thus simplifying the control structure.

IV. Proposed Augmented Modulation Scheme

The method proposed in this paper achieves arm balancing by tailoring the distribution of the AC modulation signals between the arms within each phase according to balancing requirements. Based on Eq. (2), the modulation signals can be redistributed among the arms without affecting the AC component of the voltage reference or the AC grid current [9]. The distribution of the DC voltage reference should remain unchanged, to avoid DC components in the converter AC voltages. This can be achieved by using equations Eq. (8) instead of equation Eq. (6) in the repartition of the modulation signals, i.e.:

$$v_{Aup} = \frac{v_{DC\_A}}{2} - (1 + x_A)v_{AC\_A},$$
$$\text{and} \tag{8}$$
$$v_{Adn} = \frac{v_{DC\_A}}{2} + (1 - x_A)v_{AC\_A},$$

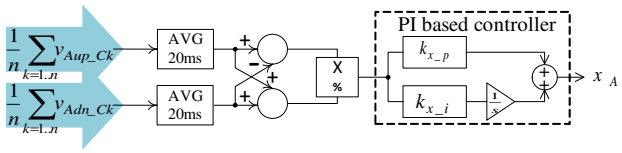

Fig. 4. Parameter x_A generation on the basis of the normalised cell capacitor voltages imbalance on the example of phase A.

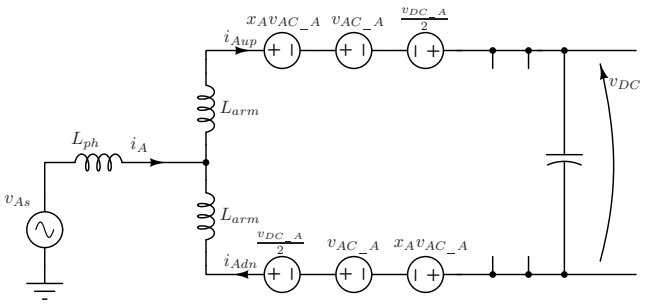

Fig. 5. Simplified schematics of the phase A of an MMC with uneven distribution of AC voltage reference.

where x_A controls the distribution of the AC modulation signal. The basic principle is that the redistribution of the AC modulation signals between the upper and lower arms induces another source of arm imbalance, independent from the pulsed DC load effect. This can be controlled by x_i, $i = A, B, C$, in each phase to counteract the effect of the pulses and re-establish arm balancing. In steady state, the x_i have constant values defined by the Proportional-Integral (PI) controllers that regulate the arm imbalance to zero in each phase as shown in Figure 4 for phase A.

The simplified converter diagram for phase A is given in Figure 5, where it can be seen that $x_A v_{AC\_A}$ only affects the DC side equivalent circuit and not the AC side equivalent circuit [22]. This confirms that the proposed method will not cause uneven distribution of the AC current between arms. A non-zero x_A generates a 50 Hz voltage in the differential circuit that drives a 50 Hz component in the circulating current. The interaction of this current with the AC components of the arm voltages gives a power contribution that can be used to counteract the effect of the pulsed load, as discussed in detail in the following section. The 50 Hz current is seen as a disturbance by the circulating current controller whose effect on the arm balancing controller must be carefully taken into account in the analysis and design of the proposed balancing method.

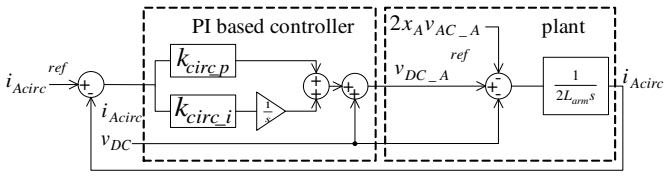

Fig. 6. Closed loop circulating current controller with arm balancing control acting as a disturbance.

V. Augmented Modulation Scheme and Arm Balancing Control Design

Remark: In this section, design of the Proportional-Integral controllers will be based on the Bode design approach [17], where target Phase Margin (PM) and Bandwidth are defined and the proportional and integral gain derived analytically using the model of the control plant. It is important to note that the choice of target Phase Margin and Bandwidth is not unique. Both Bandwidth and Phase Margin are typically maximised within the constraints imposed by the modelling method used to derive the control plant and by the restrictions imposed by nested control structures. Referring to Phase Margin, PM$>60^\circ$ is usually desirable to guarantee damped response and robustness to changes in the system parameters.

The closed loop circulating current controller diagram is illustrated for phase A in Figure 6. The plant model is based on the DC side equation and the arm balancing controller acts as a disturbance through the component $2x_A v_{AC\_A}$. Since the circulating current now has a 50 Hz component, the circulating current controller will have non-zero error under steady state conditions, with the mean value following the reference. Thus, the output of the DC side controller including DC voltage feed-forward and the Proportional-Integral (PI) controller output, is a function of the circulating current 50 Hz component and can be approximated as:

$$v_{DC\_A} = v_{DC} + {v_{DC\_A}}^0 - k_{circ\_p} \cdot i_{Acirc50} - k_{circ\_i} \int_0^t i_{Acirc50}(\tau) d\tau, \quad (9)$$

where ${v_{DC\_A}}^0$ is a DC offset ensuring that the mean circulating current follows its constant reference. From Eq. (9) and the equivalent circuit in Figure 5, the differential circuit can be represented as a series connection of a resistor k_{circ_p} and a capacitor $1/k_{circ\_i}$ at 50 Hz, as shown in Figure 7.

The relationship between the circulating current 50 Hz component and the converter AC voltage can be written as:

$$I_{Acirc50} = -\frac{2x_A V_m}{Z_{arm}} \qquad \phi_{Acirc50} = \phi_{vA} - \Delta\phi_{circ50}, \quad (10)$$

where $I_{Acirc50}$ and $\phi_{Acirc50}$ are the amplitude and phase of the 50 Hz component of the circulating current, V_m and ϕ_{vA} are the amplitude and phase of the phase A AC voltage reference and Z_{arm} and $\Delta\phi_{circ50}$ are the magnitude and phase of the equivalent RLC impedance in Figure 7 at 50 Hz (assumed to be the same in all the three phases).

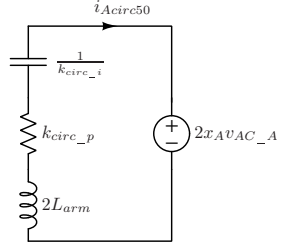

Fig. 7. Differential circuit for the 50 Hz components in phase A, valid with uneven AC reference distribution and assuming a Proportional-Integral (PI) based circulating current controller.

Combining Eqs. (9) and (10), neglecting all the DC components and defining v_{DC50} as the 50 Hz fundamental of the DC voltage ripple caused by the pulsed load and v_{DC_A50} as the 50 Hz component in Eq. (9), the 50 Hz upper arm voltage and current can be derived as:

$$\begin{aligned} v_{Aup50} &= \frac{v_{DC\_A50}}{2} - x_A v_{AC\_A} - v_{AC\_A} \\ &= \frac{v_{DC50}}{2} + L_{arm}\frac{di_{Acirc50}}{dt} - v_{AC\_A}, \end{aligned} \tag{11}$$

and

$$i_{Aup50} = i_{Acirc50} + \frac{i_A}{2}. \tag{12}$$

The lower arm voltage and current can be derived in a similar manner. The average power of the upper and lower arms can be derived and their difference ΔP_{Aarm} can be written as:

$$\begin{aligned} \Delta P_{Aarm} = &-\frac{V_{DC50} I_m \cos(\phi_{DC50} - \phi_{Ai})}{4} \\ &+ \frac{x_A L_{arm} \omega V_m I_m \cos(\phi_{vA} - \Delta\phi_{circ50} + \frac{\pi}{2} - \phi_{iA})}{Z_{arm}} \\ &- \frac{2 x_A {V_m}^2 \cos(\Delta\phi_{circ50})}{Z_{arm}} = -NUM_A + x_A DEN, \end{aligned} \tag{13}$$

where V_{DC50} and ϕ_{DC50} are the amplitude and phase of v_{DC50} and I_m and ϕ_{Ai} are the phase A AC current amplitude and angle. An analytical estimation of the steady-state value of x_A required to balance the arms of an MMC feeding the pulsed DC load can be derived setting Eq. (13) to zero:

$$x_A = \frac{NUM_A}{DEN}. \tag{14}$$

The value NUM_A depends on the pulsed DC load and on the AC current while DEN depends on the AC current and voltage and on the circulating current controller parameters through Z_{arm} and $\Delta\phi_{circ50}$. Assuming balanced grid conditions, DEN is the same for all the three phases. The relation between the power difference ΔP_{Aarm} and the difference of the sums of cell capacitor voltages Δv_{Aarm} in the upper and lower arms is given by:

$$\Delta P_{Aarm} = \frac{C_{cell} \cdot V_{DC}}{n} \frac{d\Delta v_{Aarm}(t)}{dt}. \tag{15}$$

Therefore, the Proportional-Integral (PI) arm balancing controller in Figure 4 can be represented in more detail in Figure 8, where the term $1/(2V_{DC})$ represents a normalisation by the sum of all the nominal cell voltages and the measured voltages Δv_{Aarm} are averaged over (20 ms) to filter the ripple.

The pulsed DC load, which is the source of imbalance, acts as a disturbance to the arm balancing controller through NUM_A and therefore the balancing control design will be independent from the specific value of imbalance. This is a

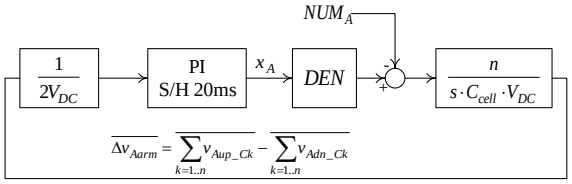

Fig. 8. Closed loop representation of the arm balancing controller for phase A.

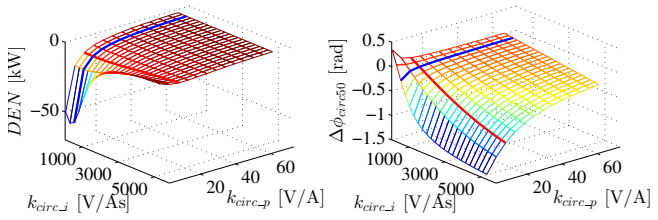

Fig. 9. DEN and the phase shift $\Delta\phi_{circ50}$ vs. the circulating current Proportional-Integral (PI) controller gains.

desirable feature since load pulses can occur with different phase with respect to the grid voltages, leading to different imbalances in the different phases as shown in Eq. (13). Referring to the full-scale CLIC converter in Table I, the circulating current controller in Figure 6 has been initially designed for a nominal bandwidth of 3750 rad/s and phase margin (PM) of 89 °, which corresponds to $k^{nom}_{circ\_p} = 13.3\,\mathrm{V/A}$ and $k^{nom}_{circ\_i} = 532\,\mathrm{V/A/s}$.

To evaluate the impact of the circulating current controller design on the proposed arm balancing method, DEN and the phase shift $\Delta\phi_{circ50}$ Eq. (10) (both functions of the circulating current controller) are computed for different current controller parameters as shown in Figure 9. The proportional gain is in a range of ($\frac{k^{nom}_{circ\_p}}{5}$, $5k^{nom}_{circ\_p}$) and the integral gain is in a range of ($\frac{k^{nom}_{circ\_i}}{10}$, $10k^{nom}_{circ\_i}$). For both DEN and $\Delta\phi_{circ50}$, the lines of $k^{nom}_{circ\_p}$ and $k^{nom}_{circ\_i}$ are shown in red and blue, respectively. The red line corresponds to nearly constant bandwidth while the PM is varied. The blue line corresponds to change of both bandwidth and PM. When the circulating current controllers have high bandwidth and high PM, the proposed balancing scheme produces a circulating current almost aligned with the AC voltage vector, showing the affinity between this method and the methods introduced in [15] and [16]. However, the value of DEN approaches zero, requiring a larger x_A to achieve balancing. Conversely, low bandwidth circulating current controllers lead to a larger phase shift between the AC voltage and circulating current and a larger absolute value of DEN. Therefore, a trade-off between circulating current control bandwidth and balancing is needed.

For the CLIC parameters in Table I, the nominal design for the circulating current controller is considered acceptable given the relatively high bandwidth and the value of DEN in Figure 9. Therefore, the arm balancing controller in Figure 8 assumes $k^{nom}_{circ\_p}$ and $k^{nom}_{circ\_i}$ and has been designed to achieve a bandwidth of 7 rad/s and a PM of 65 °, yielding $k_{x\_p} = 0.3$ and $k_{x\_i} = 1\,\mathrm{s}^{-1}$.

VI. Simulation Results

The MMC grid-interface for the CLIC with the proposed arm balancing controller has been simulated in PLECS initially according to the full-power ratings in Table I. The sampling frequency and equivalent switching frequency is 10 kHz. The control gains used in the simulation are given in Table II and refer to the continuous-time control schemes shown in Figs. 3-8.

The denominator of Eq. (14) does not depend on the pulse position, and arm balancing is expected for all pulse positions.

TABLE II. Control gains - Full-scale CLIC Simulation

Controller	Proportional		Integral		Bandwidth
Phase Current	k_{dq_p}	9	k_{dq_i}	900	2000 [rad/s]
Circ. Current	k_{circ_p}	13.3	k_{circ_i}	532	3750 [rad/s]
Energy	k_{en_p}	140	k_{en_i}	70	10 [rad/s]
DC voltage	k_{dc_p}	0.083	k_{dc_i}	0.83	12.5 [rad/s]
Ph. balancing	k_{pb_p}	0.014	k_{dc_i}	0.007	20 [rad/s]
Arm balancing	k_{x_p}	0.3	k_{x_i}	1	7 [rad/s]

Without loss of generality, results are shown for a pulse position of 0.534 rad with respect to the phase A positive zero crossing. Figure 10 presents the converter waveforms in steady state. From top to bottom, the converter phase currents and voltages and the DC current and voltage are presented (v_{Xs} and i_X with $X = A, B, C$, v_{DC} and i_{DC} in Figure 1). The 50 Hz component is present in the DC current, as a consequence of the 50 Hz components in the three circulating currents, caused by the arm balancing controllers. A variation of the pulse position affects the amount of disturbance in each phase, i.e. $NUM_{A,B,C}$ is different, leading to different $x_{A,B,C}$ values and different amplitudes of the 50 Hz component in the circulating current.

Figure 11 shows the converter AC and DC side instantaneous powers where it can be seen that the AC power ripple is very low, below 0.3 % despite the large DC power fluctuation caused by the pulsed load.

Finally, to validate the dependence of the steady state values of $x_{A,B,C}$ and $I_{A,B,Ccirc50}$ on the design of the circulating current control, simulations have been run for five pairs of circulating controller gains: (k_{circ_p}, k_{circ_i}), (k_{circ_p}, $10k_{circ\_i}$), (k_{circ_p}, $\frac{k_{circ\_i}}{10}$), ($5k_{circ\_p}$, k_{circ_i}) and ($\frac{k_{circ\_p}}{10}$, k_{circ_i}). The values obtained for $x_{A,B,C}$ and $I_{A,B,Ccirc50}$ are shown in Figure 12. In accordance with the analysis in Section V, the circulating current amplitudes are comparable for all the cases except the second, that corresponds to a larger absolute $\Delta\phi_{circ50}$ value in Figure 9. Moreover, $x_{A,B,C}$ increase when the bandwidth of the circulating current controller increases causing a smaller absolute value of the DEN in Figure 9.

The full-scale simulation results confirm the feasibility of the arm balancing method and demonstrate the impact of the circulating current control design for the operation of an MMC as a grid-interface for klystron modulators. For the sake of brevity, the validation of the balancing controller design is presented only in the experimental results section.

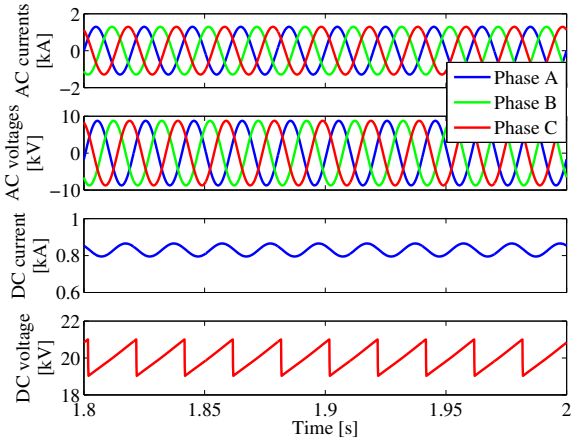

Fig. 10. Simulation of the 16.6 MW converter in steady state: Phase currents, AC grid voltages, DC current and DC voltage.

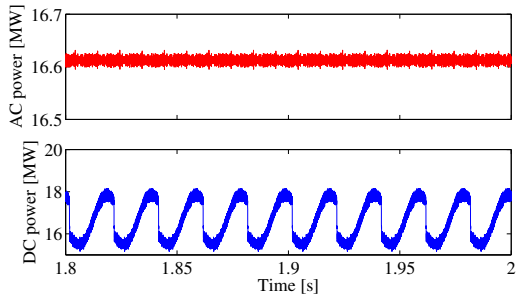

Fig. 11. Simulation of the 16.6 MW converter AC and DC side power in steady-state.

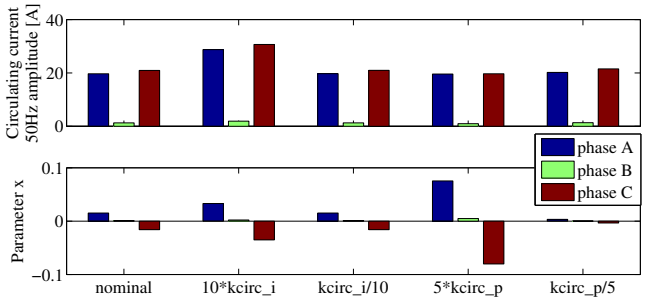

Fig. 12. Simulation of the 16.6 MW converter: phase A, B and C 50 Hz circulating current amplitude and x parameter vs. the circulating current Proportional-Integral (PI) controller parameters.

VII. Experimental Results

A laboratory scale prototype has been built for the purpose of validating the behaviour of the grid connected MMC under pulsed DC load conditions. The 4 cell per arm, 7 kW MMC has been designed by scaling both the converter voltages and currents with the same scaling factor. Scaling to low average power has been necessary to limit the cost of the prototype. However, as shown in Table I, the pulsed load emulator draws about 3.3 kA, corresponding to an instantaneous power approximately equal to 900 kW. Considering that scalability is one of the main advantages of the MMC and that control is the main focus of the paper, the laboratory scale tests are meant to provide an initial indication of the practical viability of the proposed solution. A photograph of the experimental converter is presented in Figure 13. A resonant thyristor based L-C circuit has been designed to emulate the pulsed DC load as discussed in [9] and [10]. Table I lists the parameters of the experimental prototype.

The load parameters are designed to provide the same average current (16.5 A) as the scaled flat top pulse in the real

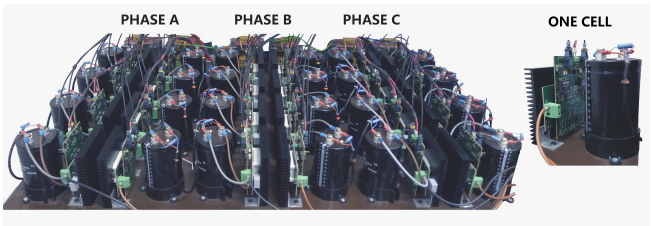

Fig. 13. Experimental MMC with 4 cells per arm.

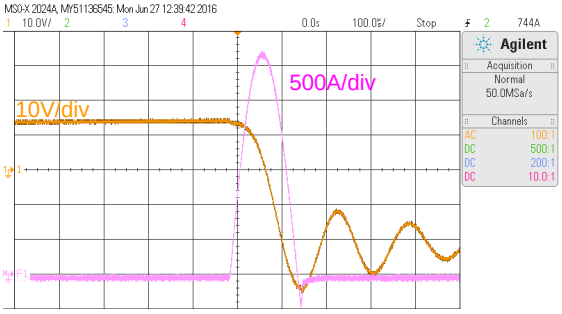

Fig. 14. Experimental pulsed load emulator characteristics captured by the oscilloscope: DC voltage and load current.

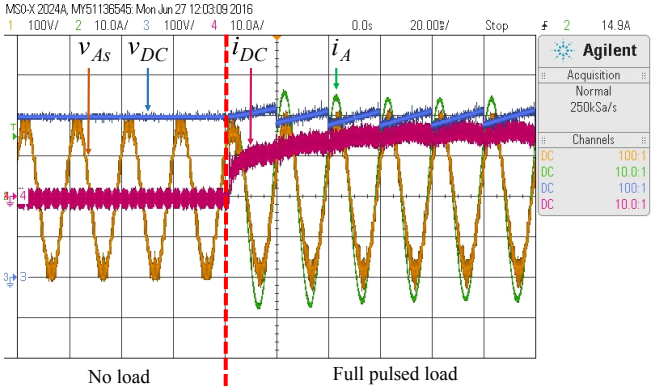

Fig. 15. Experimental converter waveforms captured by the oscilloscope: Phase A current, phase A voltage, DC current and DC voltage.

application, with the same pulse area and duration. The pulse is in the shape of positive half of a sinusoid, which results in $\approx \frac{\pi}{2}$ times higher peak pulse current. Table III presents the controller gains used in the control implementation for the experimental converter, designed according to the models developed in Section V and referred to the continuous-time implementation of the controllers as shown in Figures 3 to 8.

TABLE III. Control gains - Laboratory-scale experimental setup

Controller	Proportional		Integral		Bandwidth
Phase Current	k_{dq_p}	10	k_{dq_i}	2000	2670 [rad/s]
Circ. Current	k_{circ_p}	10	k_{circ_i}	500	3333 [rad/s]
Energy	k_{en_p}	2.8	k_{en_i}	8.3	8.8 [rad/s]
DC voltage	k_{dc_p}	0.12	k_{dc_i}	0.12	14.2 [rad/s]
Ph. balancing	k_{pb_p}	0.1	k_{dc_i}	0.02	120 [rad/s]
Arm balancing	k_{x_p}	0.3	k_{x_i}	1	7.3 [rad/s]

The control algorithm is implemented in a DSP-FPGA platform, including a Texas instruments 225 MHz TMS320C6713 DSP and FPGA cards used for data acquisition and PWM signal generation. The DSP board is equipped with a daughter card for online data logging through a Matlab Host Port Interface (HPI). DSP sampling and control frequency and HPI frequency are set to 10 kHz. Some of the results are based on the HPI data while other waveforms are captured with a 200 MHz oscilloscope.

An initial set of experimental waveforms is shown to confirm the effectiveness of the balancing controller with nominal design parameters. Figure 14 presents the load waveforms, including the current pulse and the droop of the DC voltage. The current pulse has a repetition of 50 Hz with the peak current of nearly 3.3 kA. The pulse causes a voltage droop of 48 V (12 %) and the nominal DC voltage is 400 V.

Figs. 15, 16 and 18 are captured for the nominal controller gains (Table III) and a pulse occurring 1.7 ms after the phase A grid voltage positive zero crossing. Figure 15 presents the phase A grid voltage and current together with the DC voltage and current (v_{As}, i_A, v_{DC} and i_{DC} in Figure 1) before and after activation of the pulsed load. Figure 16 presents the grid power and the DC power under steady-state conditions with the pulsed DC load, measured with the HPI. The AC power shows little variation in the presence of the pulsed load while the DC power has a significant droop at the pulse instant. The AC power fluctuation is about 1.65 %. The steady-state waveforms obtained correspond to $x_{A,B,C}$ values of 0.0098, 0.0007 and -0.0156. The peak values of the corresponding 50 Hz components in the circulating currents are 0.39 A, 0.07 A and 0.42 A.

A second set of experimental results is presented in order to validate the dependence of the steady-state values of the balancing controller on the design of the circulating current controller and to confirm the design of the balancing controller and its dynamic performance as discussed in Section V.

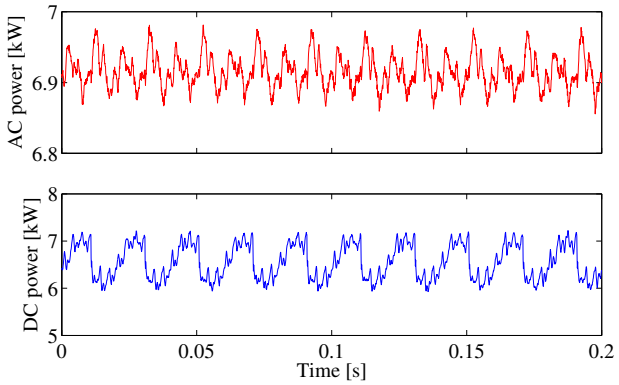

Fig. 16. Experimental converter AC and DC side power captured using the HPI, under steady-state operation with pulsed load.

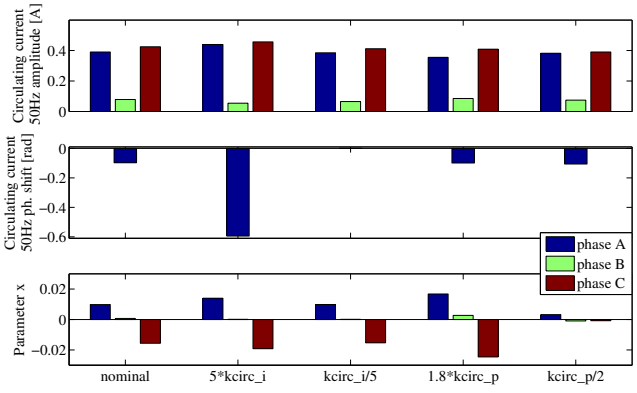

Fig. 17. The phase A, B and C circulating current 50 Hz component amplitudes and phase shift (computed for the phase A) and x parameters vs. the circulating current Proportional-Integral (PI) controller parameters obtained experimentally.

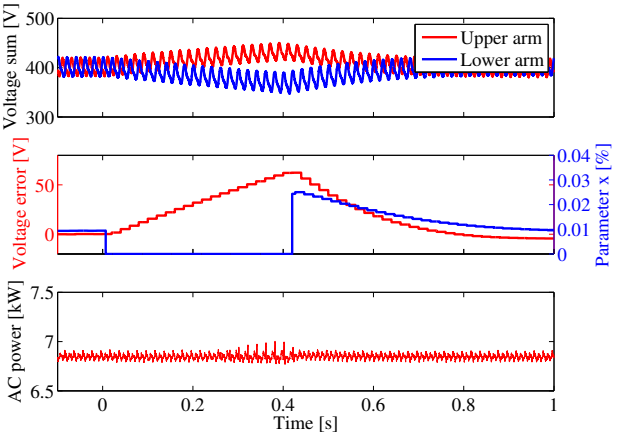

Fig. 18. Experimental validation of Phase A arm balancing control dynamics (HPI waveforms): sum of the cell capacitor voltages in the upper and lower arm (top plot), difference between the sum of the upper and lower arm cell capacitor voltages averaged at 20 ms and x parameter (middle plots) and AC power fluctuation (bottom plot).

A. Effect of circulating current control parameters

The circulating current controller gains are varied within the controller stability region, to obtain the dependence of the steady state $x_{A,B,C}$ values and the circulating current 50 Hz component as presented in Figure 17. The values obtained show trends that are similar to those predicted analytically and found by simulation in Figure 12, having the highest circulating current amplitude for the highest phase shift angle and the highest-parameter x values for the highest bandwidth of the circulating current controller.

B. Arm balancing controller dynamics

To complete the validation of the proposed arm balancing controller design, a further experimental test has been performed yielding the results given in the HPI acquisition shown in Figure 18 where the MMC operates under pulsed DC load with nominal control gains from Table III and the arm balancing control is temporarily disabled. The purpose of the test is twofold: first, by disabling the balancing controller the rapid deviation of the upper and lower arm voltages from their nominal value can be appreciated, highlighting the need for balancing to avoid overmodulation; second, once the balancing controller is re-enabled, its transient response can be evaluated and compared with the design target. In Figure 18, the arm balancing is disabled from $t = 0\,\mathrm{s}$ to $t = 0.4\,\mathrm{s}$ and then re-enabled. The convergence of the voltage error, after re-enabling the arm balancing controller, is in agreement with the expected bandwidth of $7.3[rad/s]$ given in Table III, since the fall time of the error can be estimated as $t_f \approx 0.39\,\mathrm{s}$.

VIII. Conclusion

This paper presents a new arm balancing method suitable for the operation of an MMC grid-interface for the klystron modulators used in the Compact Liner Collider (CLIC). The modulators represent a pulsed DC load for the converter, with a pulse repetition frequency of 50 Hz. The correspondence between pulse repetition frequency and AC grid frequency necessitates the use of arm balancing controllers in the MMC that have to be incorporated into a suitable control algorithm. A decoupled AC and DC side control has been adapted for the specific conditions and requirements of the application, while the modulation strategy is augmented in order to cope with the imbalances caused by the pulsed load. By employing the presented strategy, low AC power fluctuation can be achieved under pulsed DC load conditions.

The proposed control algorithm is effective and achieves its objectives with very low control complexity, since there is no need for generating and tracking sinusoidal circulating current references. The proposed method has been discussed in detail, including the modelling and design of the balancing controller. Moreover, the effects of the circulating current control design on the steady state operation of the balancing control have been discussed.

The proposed strategy has been initially validated in simulation for the full ratings of the CLIC application, achieving capacitor voltage balancing and AC power fluctuation below 0.3 %. A 7 kW small scale prototype has been developed to experimentally prove the effectiveness of the proposed approach. Experimentally, the measured AC power fluctuation is still below 2 % despite the reduced number of voltage levels available in the experimental converter. The dynamic response observed in the experimental converter is in agreement with the theoretical expectation, confirming the analysis and procedures used in the design.

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