EOCB-Platform for Integrated Photonic Chips Direct-on-Board Assembly within Tb/s Applications

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***Abstract*—Efficient packaging of integrated photonic chips (PIC) on host substrates is essential to fully deploy their potential and to co-integrate electronic chips (EIC). A high-performance electro-optical printed circuit board (EOCB), which exhibits a combined electrical and optical interface, is proposed to serve as integration platform for PICs. This enables an assembly approach which combines two assembly steps, the optical and the electrical one, into one single step. Whereby, the two processes usually operate in quite different accuracy regimes.**

EOCB (Electro-Optical Circuit Board); Optical interconnections; Photonic integrated circuit packaging; Optical coupling;

I. INTRODUCTION

ICT-STREAMS [1] is a European research and innovation project aiming for high-data throughput between multiple computing nodes on a server-board. Any-to-any optical connections between processors will be achieved by using WDM (wavelength division multiplexing) signals routed over a cyclic AWGR (arrayed waveguide grating router). The main target of this configuration is to enable high data bandwidth (12.8 Tb/s) for a 16 socket server-board with reduced latency and reduced power consumption for communication [1].

This work deals with the realization of a printed circuit board with integrated polymer waveguides (EOCB) to enable the proposed integration density and novel functionality portfolio on architecture level [1]. A key feature is to enable the direct attachment of photonic chips (PIC) onto the board. Adiabatic coupling of PICs to polymer waveguides provides a solution for assembling photonic chips onto a substrate with electrical and optical interfaces in a straightforward manner [2].

Population of semiconductor devices directly on large boards requires conventional interposer, by maintaining large formats and at lower cost. This implies an efficiently manufacturable substrate as assembly platform, which provides exposed polymer waveguide cores for adiabatic optical coupling and small electrical interconnection pads (125 µm pitch) very close to the waveguides.

II. REQUIREMENTS FOR ON-BOARD OPTICAL COMMUNICATION

A. System Aspects

For large systems with multiple computing nodes, the direct connection between these nodes is critical in terms of bandwidth, latency and power consumption. Optical interconnects provide a solution to these challenges, and with integrated photonic chips aiming for cost-efficiency in the near term, they eventually will become commercially viable [1], [3]. Placing the electro-optical conversion device, e.g. the optical transceiver, close to the computing node and therefore to minimize the length of the electrical trace, will therefore help to overcome electrical limitations [4]. The combination of wavelength multiplexing and parallel waveguides, leads to the desired high integration density.

B. Photonic Integration

One of the main drivers for high level photonic integration is the optical link budget. The pursued approach helps to minimize the number of interfaces and increases the efficiency of the optical coupling.

Adiabatic coupling between tapered silicon waveguides on the photonic integrated chip and the polymer waveguides on the EOCB enables efficient coupling with a wide optical bandwidth and relaxed lateral alignment tolerances. The chip is thereby mounted face-down onto the board with a remaining gap well below 0.5 µm between the silicon waveguide and polymer core surfaces. A transparent underfill is applied to attach the chip and acts as cladding [5]–[7]. This approach allows a vertical coupling between two optical planes.

The main advantage of the system is the very wide wavelength range of more than 100 nm without significant excess loss. This enables very broadband WDM applications.

The alignment tolerance of approximately ±1.5 µm in the lateral direction simplifies assembly process significantly. An advanced flip-chip bonder can be used to achieve the lateral alignment, while mechanical reference plane can be used as vertical position reference [5].

C. Board Requirements

The key requirement for EOCB is to provide the optical and electrical interface to host PIC. Exposed polymer core waveguides, which are part of the adiabatic coupling interface, are placed close to electrical pads, see Figure 1.

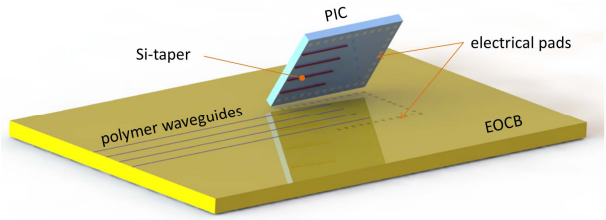


Figure 1. Illustration of EOCB and PIC with the respective adiabatic optical coupling interface and the electrical pad arrays before assembly.

Adiabatic interfaces require an area of a few square millimeters with an excellent flatness. The surfaces of all polymer core waveguides in the coupling area are required to be coplanar within about 1 µm, to ensure a minimal gap between polymer and silicon. The mechanically compliant lower cladding allows the polymer core surface height variation to adapt to the flat silicon surface. Hence, the coplanarity tolerance (approx. 1 µm) can be slightly larger than the required final gap (< 0.5 µm).

Fabricating polymer waveguides with precise vertical control in terms of core thickness and position in order to reach a high optical performance requires the substrate, in this case the electrical circuit board, to have a low thickness variation and low topography.

The positioning tolerance in all three dimensions between electrical pads on the chip and the board are in the range of ±5 µm (lateral and vertical) due to the pad size of only 65 µm. Thus, also the polymer waveguides are required to be aligned within in ±5 µm to the copper layer L1.

Chips with a length of up to ten millimeters will draw ones attention to the difference in thermal expansion. Common printed circuit board materials exhibit usually a coefficient of thermal expansion (CTE) in the range of 17 ppm/K, which is close to copper. But the PICs exhibit a coefficient of only 3 ppm/K. Thus, lowering the CTE of the EOCB would be beneficial for the reliability of the electrical interface.

The goal is to transmit electrical signals at a data rate of 56 Gbps, using non-return to zero (NRZ) coding scheme over the electrical transmission lines to the PIC. The bond pads should provide good adhesion for wire and solder bonds.

III. Design, Manufacturing and Methods

A. Layer Build-Up

The aforementioned aspects regarding flatness, topography, lateral thermal expansion, and high-speed signals have been taken into account for the EOCB build-up.

The laminates, prepregs, and bond plies used as dielectric materials in this work are listed in TABLE I, and are selected to meet the requirements.

TABLE I Dielectric Materials Types

Dielectric material type and properties				
ID	***Description***	***Dk*** *(dielectric constant)*	***Df*** *(dissipation factor)*	***CTE*** *[ppm/°C]*
L	LCP based layers	2.8 - 3.2	0.002-0.003	n.a.
H	High-frequency layers	2.8 -3.2	0.0015 – 0.003	n.a.
C	Low-CTE layers	4.1 – 4.5	0.01 0.02	4-6

Electrical waveguides embedded in the dielectric, with the copper surface just a few micrometers below the dielectric surface, provide the required low topography, see Figure 2b).

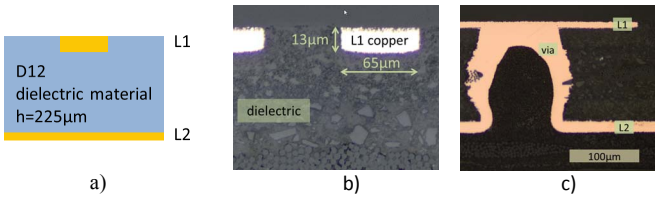


Figure 2. a) Illustration of cross-section for simulation and micrograph of b) layer L1 cross-section and c) via L1-L2 cross-section.

Having the electrical traces countersunk into the dielectric material maximizes the propagated electrical energy in the high frequency dielectric D12. Hence, the impact on the signal propagation of the optical layer, which acts as dielectric material which placed on top of the transmission lines (Figure 3), minimizes the signal propagation. This is important, since the dielectric properties (Df, Dk) of the optical material cannot be altered.

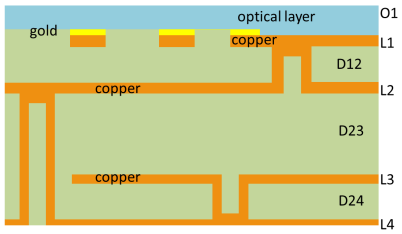


Figure 3. Illustration of layer build-up for four layer boards (L1-L4) and two layer boards (L1-L2).

The dielectric D23 (Figure 3), which represents the core laminate of the electrical board is made of dielectric type “C” (TABLE I), with a thickness of approximately 350 µm, to reduce the thermal expansion of the board. The layer D24 is

made out of the same dielectric type as D12 and 250µm thick to obtain a symmetrical layer build up.

B. Board Design

Three different types of boards, summarized in TABLE II have been investigated in the course of this work.

TABLE II Description of the used circuit boards

Board Concept			
ID	***Purpose***	***Layer count***	***Dielectric D12***
EL1	Characterize Dk_{eff} using ring resonators	4	type H
EL2	Test impact of optical polymer on high-frequency performance	2	type L
EOCB2	Platform for PIC assembly	4	type H

Firstly, the correspondent dielectric constant, $Dk_{eff,}$ is verified through comparison of simulated and measured ring resonators on the board EL1. The ring resonators are designed as microstrip lines. In comparison to coplanar waveguides, microstrip lines are strongly coupling to the bottom ground plane (L2) through the dielectric layer (D12). Therefore,the dielectric constant Dk_{eff} is increased and the contribution of the dielectric material under the test structure to the resulting Dk_{eff}. Small Dk_{eff}-differences of the neighboring material are directly converted into measurable frequency differences. One of the ring resonators is shown in Figure 5a.

To verify the impact of the optical polymer layer on the performance of the electrical coplanar waveguides, a test board EL2 has been designed and identical layouts are manufactured with and without optical cladding.

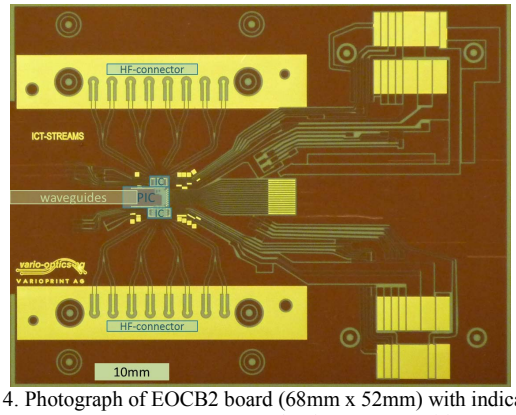


Figure 4. Photograph of EOCB2 board (68mm x 52mm) with indication of PIC, IC, HF-connector, and polymer waveguides.

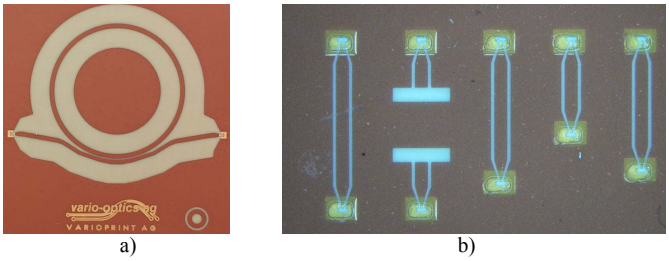
The EOCB2 board will act as host for the PIC. It provides an adiabatic coupling area below the PIC with polymer waveguides running eastbound towards the board edge, see Figure 4. Landing areas for high-frequency connectors are located at the north and south side of the EOCB2.

C. Simulation

The transmission lines and test structures have been designed with the Keysight ADS software, and simulated with the Momentum Microwave EM tool, according to cross-section in Figure 2a. Coplanar waveguides are chosen to minimize radiation losses and increase isolation in between test lines.

D. Manufacturing

The fabrication process starts with patterning and lamination of L1 and L2, with subsequent via (L1-L2) formation, see Figure 2c. The layers L3 and L4 are patterned and the vias formed prior to the lamination of the complete stack using type C dielectric as core, see Figure 3. Then, vias are processed from the backside to layers L2 and L3. Finally, the bond pads and connector areas are coated with bondable, electrolytic gold. The electrical substrate undergoes an electrical probe testing as a final step.



a) b)

Figure 5. Photograph of a) ring resonator on board EL1 to verify effective permittivity Dk_{eff} and b) part of transmission lines placed on the EL2 board for propagation loss measurements.

The singlemode polymer waveguides are based on a silicon material compound with excellent reliability and good optical performance. The optical material has been obtained from Dow Chemical. They are fabricated using layer deposition processes and UV-laser direct imaging [8]–[10].

E. Electrical Test Setup

The electrical test board contains multiple sets of test lines with a variation of line/space patterns, where each set is designed to be matched to 50 Ω impedance. To limit space, all lines are probed instead of connectorized. To calibrate out the probe launch and the probes itself, through-reflect-line (TRL) calibration kits are added; one for each type of line. The lines are measured with 40 GHz and 67 GHz RF probes and a 67 GHz PNA-X network analyzer. TRL calibration is done both offline and with the calibration software of the PNA-X, producing very similar results.

Several transmission line profiles have been compared, each with their own TRL calibration kit. The line standards used for the TRL calibration are reused as device-under-test (DUT). Increasing trace width improves loss by reducing skin effect penalty, maintaining matching conditions. Effective length of the test lines after removal of the probe launches via TRL is reduced from 1.8 cm to 1.53 cm. After this step, the line standards used for the multi-line TRL calibration can be reused as device-under-test. Increasing trace width improves loss by reducing skin effect penalty, while still resulting in good matching.

1) Effective permittivity and loss

Extraction of the effective permittivity is done both by differential length method, on S-parameters obtained after TRL calibration; and as a direct result of offline TRL calibration itself. As Ln1 is the widest line with the largest gap; it couples most to the bottom ground plane; Dk_{eff} is highest and the increase in Dk_{eff} due to the optical cladding is limited. Ln2 and Ln3 are narrower and with a smaller gap; they therefore couple more to the top ground layer; resulting in more field lines through air and a lower Dk_{eff}. When the cladding is applied, the increase in Dk_{eff} is therefore larger; and the overall Dk_{eff} is even larger than Ln1.

2) Time domain

To visualize the performance of the EOCB technology; a comparative time domain measurement has been done. The differential output of a 92 GSa/s arbitrary waveform generator (AWG) is split in two branches with identical cables and connectors. In one branch, the device-under-test, consisting of two 67 GHz GSG-150 probes and 1.8 cm long transmission line with cladding, is inserted. The probes have a typical insertion loss of -0.95 dB and -0.75 dB at 67 GHz and at 50 GHz, respectively (Picoprobe® Model 67A). The output eyes are compared with a 70 GHz sampling scope. The 67 GHz RF probes and their launch section are not calibrated out in this measurement. Even in this case, the measurement does not indicate significant eye closure; confirming the HF performance of the EOCB lines.

IV. Results and Discussion

A. Manufacturing process

Initial fabrication runs showed limited scalability of the described manufacturing procedure for the dielectric type L (LCP material family) for four layer configuration due to process related issues. The material was then successfully replaced with type H dielectric, except for the two layer board EL2. The similar Dk values allowed keeping the same transmission line dimensions for the new dielectric. The applied process yields electrical traces with nearly vertical sidewalls in the L1 (high-frequency) layer, see Figure 2b. The copper surface has a surface treatment to improve the adhesion of the cladding layer.

B. Dk Characterization using ring resonators

When comparing the simulated and measured S_21 for both rings, situated on opposite sides of the test board; we observe that, for both rings, Dk_{eff} is 3% larger than the values obtained by simulation. We conclude that the small deviation in the effective permittivity is not a local or random fluctuation; but nonetheless, this error is very small and has little impact on the other test features, see Figure 6.

C. Dk and Df for transmission lines and impact of optical layer

Extracted S-parameters after TRL on the network analyzer, including renormalization to 50 Ω impedance, indicate a very limited loss penalty due to the addition of optical cladding, without adapting the design.

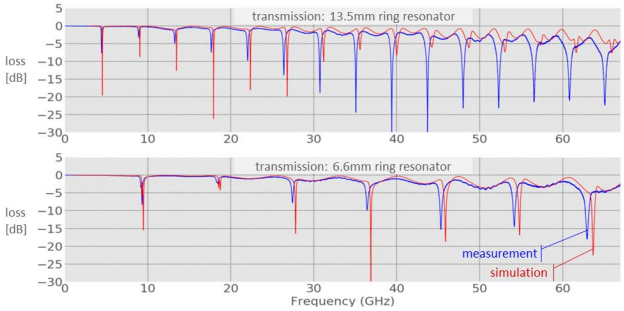


Figure 6. Transmission in the 13,5 mm (top) and 6,6 mm (bottom) diameter ring resonators; simulation (red) vs. Measurements (blue).

Best loss values for 50 GHz signals are -0.37 dB/cm and -0.44 dB/cm for uncovered and cladding covered transmission lines, respectively. The insertion loss is in-line with high-end high-frequency laminates such as Rogers RO4350BLoPro (-0.4 dB/cm at 50 GHz) [11] with similar dielectric thickness.

TABLE III Transmission and permittivity for transmission lines

IL and Dk extracted from S-parameters (50GHz)			
Width [µm]	430	300	200
Gap [µm]	60	60	125
IL_{air} [dB/cm]	-0.37	-0.49	-0.52
IL_{clad} [dB/cm]	-0.44	-0.55	-0.65
Dk_{eff_air} [1]	2.345	2.26	2.26
Dk_{eff_clad} [1]	2.55	2.58	2.615

D. Time domain signal integrity

The longest transmission lines on EL2 show good signal integrity for 60 Gbps NRZ signals (Figure 7), and acceptable eye opening even for 112 Gbps PAM-4 signals (Figure 8).

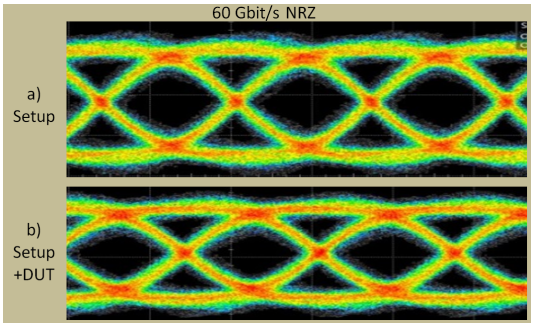


Figure 7. Comparison of 60 Gbit/s NRZ transmission through a) the reference setup and b) the DUT.

Neglecting reflection in the probe or at the probe launch, the S-parameters indicates that at least the same eyes can be

obtained for approx. 4 cm of EOCB line with cladding, without the probes.

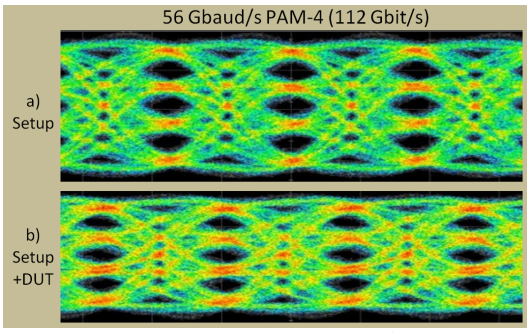


Figure 8. Comparison and 56 GBaud (112 Gbit/s) PRBS9 PAM-4 transmission through a) the reference setup and b) the DUT.

E. Topography

The coplanarity of the bond pad surfaces, for the pads which are used to assemble the PIC (Figure 9), is below 5 µm over an area of 13mm^2. The measurements were performed with a scanning confocal microscope (Keyence VK-X) with applied planar tilt correction.

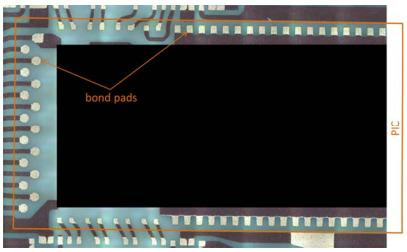


Figure 9. Micrograph of PIC assembly area on the EOCB2

The gold pads are coplanar with the dielectric surface, while the copper surface is 4 µm recessed with respect to the dielectric layer. First cladding coating test exhibit, that this minor topography has no severe impact onto the surface topography of the lower cladding. The trench based layout approach minimizes the amount of the dielectric area and ensures therewith the cladding layer quality.

V. Conclusion

Herein presented is an electro-optical circuit board as mounting platform for adiabatically coupled, flip-chipped photonics integrated chips. The electrical performance exceeds the targeted 56 Gbps NRZ signal transmission. The smooth topography enables the critical layer deposition for singlemode polymer waveguide fabrication, and eventually enables the flip-chip bonding of large photonic chips. The demonstrated assembly platform can be applied for integrating photonics on boards for various applications, including transceiver modules and multi-socket boards.

Acknowledgment

The strong support of S. Beyer, N. Crameri, M. Halter, and D. Meier (all vario-optics) towards the successful fabrication of the electro-optical circuit boards is kindly appreciated. We would also like to acknowledge the support from ICT-STREAMS consortium members, M. Fickry, R. Zhang (FCI Deutschland), and R. Dangel (IBM Research Zurich).

This project has received partial funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 688172 and this work was partially supported by the Swiss State Secretariat for Education, Research and Innovation (SERI) under contract number 15.0339-1. The opinions expressed and arguments employed herein do not necessarily reflect the official views of the Swiss Government or the European Commission.

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