Vertical nanowire TFETs with channel diameter down to 10 nm and point S MIN of 35 mV/decade

Memisevic, Elvedin; Svensson, Johannes; Lind, Erik; Wernersson, Lars Erik

Published in:
IEEE Electron Device Letters

DOI:
10.1109/LED.2018.2836862

2018

Document Version:
Peer reviewed version (aka post-print)

Vertical nanowire TFETs with channel diameter down to 10 nm and point S_{MIN} of 35 mV/decade

Elvedin Memisevic,[a] Johannes Svensson, Erik Lind, and Lars-Erik Wernersson
Department of Electrical and Information Technology, Lund University, 221 00 Lund, Sweden

[a]Electronic mail: elvedin.memisevic@eit.lth.se

We present experimental data from vertical InAs/InGaAsSb/GaSb nanowire tunnel field-effect transistors with channel diameter scaled down to 10 nm and ability to reach a point subthreshold swing of 35 mV/decade at V_{DS} = 0.05 V. Furthermore, the impact of drain, channel and source diameter scaling on the subthreshold swing and currents are studied. Impact of gate-overlap is more evident for devices with highly scaled source due to strong reduction of the current. Furthermore, small channel diameter makes these devices more susceptible to Random Telegraph Signal noise.

I. INTRODUCTION

The Tunnel Field-Effect Transistor (TFET) is considered to be one of the most promising steep slope transistors for low power applications (V_{DD} < 0.3 V) [1]. Based on improved understanding of these devices, a number of research groups have been able to demonstrate TFETs that operate below the thermal limit [2-4]. A number of different

semiconductors (Si as well as III-V) and geometries have been utilized to fabricate TFETs [5,6]. Vertical InAs/InGaAsSb/GaSb nanowires with 20-nm-thick channel have demonstrated the ability to operate well below the thermal limit reaching subthreshold swings down to 43 mV/dec at V_{DS} of 0.1 V and to combine the steep slope with high current levels due to the staggered bandgap alignment [7,8]. Further device improvement and integration density require scaling of the drain, channel, and source diameters. In this work, we are scaling the diameter of the InAs segment (drain/channel) to a diameter of 10 nm and InGaAsSb source (from 30 to 18 nm) and demonstrate improved subthreshold swing. Also, the impact of source-gate overlap is studied.

II. Fabrication

The fabrication follows a previously reported process [7,8]. Prior to growth, Au-seed particles were defined in arrays with 1-8 nanowires using Electron Beam Lithography (EBL) and PMMA based lift-off on an n^+-InAs layer (260 nm) integrated on a highly resistive Si (111) substrate (ρ>12 kΩ-cm) [9]. The diameter of the Au-seed particles was set to either 40 or 44 nm with a spacing of 1.5 μm. The growth of the nanowires was subsequently performed using metal-organic-vapor-phase epitaxy (MOVPE) utilizing the vapor-liquid-solid growth method. The growth of the InAs and GaSb segments were the same as described in [8]. However, the InGaAsSb segment was grown using trimethylgallium, arsine, and trimethylantimony with gas phase molar fraction of $4.9 \cdot 10^{-5}$, $5.1 \cdot 10^{-6}$, and $1.3 \cdot 10^{-4}$, respectively. Thus, compared to the growth used in [7,8], the growth rate was lower due to lower arsine flow. The final composition at the source side is $In_{0.29}Ga_{0.71}As_{0.66}Sb_{0.34}$ determined using energy dispersive X-ray spectroscopy [8]. The

bottom part of the InAs was n-doped with an estimated doping of 10^{19} cm^{-3} using triethyltin and the InGaAsSb/GaSb-segments where p-doped with an estimated doping of 10^{19} cm^{-3} using diethylzinc. Using this recipe, four samples (A, B, C, D) with similar nanowires where grown. The next step after the growth was digital etching to reduce the diameter of the InAs to either 20, 15 or 10 nm. During this process, the InGaAsSb diameter was also reduced although with a slower rate. The diameter of the GaSb segment was unaffected. Nanowires with 10-nm-thick diameter, see Fig 1a, are included on sample D that was most extensively etched. Subsequent processing of these samples was performed using the same steps as described in [7,8]. A schematic image of a finished device can be viewed in Fig 1b. The gate dielectric is a bilayer of 1 nm Al_2O_3 and 4 nm HfO_2, with estimated EOT of 1.4 nm. The bottom spacer that separates the drain and gate-metal is a 15-nm-thick SiO_x-layer. The effective gate-length is ~ 100 nm. More details on the devices can be found in Table 1.

III. DISCUSSION

Figure 1c and d show data from a device from Sample B, with three nanowires and an InAs diameter of 20 nm. The device exhibits good electrostatic control, confirmed by low drain-induced-barrier-lowering (DIBL) of 30 mV/V and a point subthreshold swing of 49 mV/decade at 0.1 V. The output data show a superlinear behavior and a Negative Differential Resistance (NDR) peak is shown with a Peak-to-Valley Current Ratio (PVCR) of 6. The device on-state current level is lowered by the gate-overlap, which is evident in Fig 2a, where devices without any overlap and with overlap are

compared [10], possible due to gating of the p-type source leading to a higher access resistance and lower junction electric field, decreasing the tunneling current. Figures 2b and c, show transfer and subthreshold characteristics for devices from samples B, C, and D. A thinner InAs channel will allow for better electrostatics, which helps to reduce the subthreshold swing. The reduction in diameter reduces the point subthreshold swing from 49 to 45 mV/decade as well as the on-current level. Furthermore, the device with the thinnest diameter exhibits stronger Random Telegraph Signal (RTS) noise in the on-state [8]. As Fig 2c shows, a device with 10-nm-thick channel (7 nanowires) demonstrate a minimum slope of 45 mV/decade although only over a restricted current range with a lower I_{60}. Also, at these diameters, a reduction in the number of nanowires improves the subthreshold swing [7], Fig 2d. A device with one 10-nm-diameter nanowire exhibits a lower point subthreshold swing of 35 mV/decade at V_{DS} = 0.05 V, where the minimum off-current of these devices is one order of magnitude lower than the devices with larger diameters (18-20 nm) presented in [7,8].

To further understand why the drive current decreases in thinner diameters we evaluate R_{ON} and NDR. Fig. 3a shows how R_{ON} changes with a reduction of the InAs diameter and as it is reduced below 15 nm, a larger increase in R_{ON} is observed. Comparison of the NDR region in the output data for devices with 20, 15, and 10 nm shows that the peak and valley currents of the device with thinnest diameter is noticeably lower (Fig. 3 b,c). Devices with larger diameters show similar I_{peak} even if they have different R_{ON}, suggesting a similar transmission across the heterojunction with a slightly different access resistance. For the thinnest nanowire, the current density is lower and the peak voltage higher, suggesting a reduced transmission across the heterojunction as well as a

higher series resistance. We attribute the current reduction for the 10-nm-diameter devices to both carrier depletion at the surfaces and decreased tunneling probability, for instance due to quantum confinement, as calculated previously [11] and both effects need to be considered in the device design. However, source depletion certainly plays a role for these thin heterojunctions as well. Similar scaling trends with increasing R_{ON} and reducing I_{peak} has been observed for broken gap InAs/GaSb as well (not shown). Those devices operate with 100x lower R_{ON} due to the broken gap heterostructure, and the data shows the ability of the device structure to operate at higher current levels after optimization of the heterojunction.

To confirm the influence of the series resistance, a NDR region of a device with 15 nm diameter is shown in Fig 3d. As the V_{GD} is increased, the I_{peak} moves to higher V_{SD} due to series resistance supporting the high R_{ON} values.

IV. CONCLUSIONS

We have demonstrated vertical InAs/InGaAsSb/GaSb nanowire TFETs with channel diameters of 20, 15, and 10 nm with the ability to operate well below 60 mV/decade. Devices with a single 10-nm-thick nanowire have demonstrated ability to reach 35 mV/decade at V_{DS} = 0.05 V. However, at this diameter, the impact of RTS noise is stronger. We also find that the gate-alignment is critical for the on-state as the source is depleted. Fabrication of highly scaled TFETs requires a careful consideration of used heterostructure to limit possible impacts of quantization with adequate gate alignment to avoid source depletion. Furthermore, a highly scaled channel will require a high-k/semiconductor interface of higher quality to reduce the impact of RTS. Identified

challenges needs to be addressed to fully harvest the potential of highly scaled TFETs, however, there is a path forward to explore these exciting devices.

ACKNOWLEDGMENTS

This work was supported in part by the Swedish Foundation for Strategic Research, in part by the Swedish Research Council, and in part by the European Union Seventh Framework Program E2SWITCH under Grant 619509. The authors are with the Department of Electrical and Information Technology, Lund University, Lund 221 00, Sweden (elvedin.memisevic@eit.lth.se)

[1] A. C. Seabaugh and Q. Zhang, “Low-Voltage Tunnel Transistors for Beyond CMOS Logic,” *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010. doi: 10.1109/JPROC.2010.2070470

[2] D. H. Ahn, S. M. Ji, M. Takenaka, and S. Takagi, "Performance Improvement of $In_xGa_{1-x}As$ Tunnel FETs with Quantum Well and EOT Scaling," in *2016 IEEE Symp. on VLSI Tech.*, 2016, pp. 1-2, doi: 10.1109/VLSIT.2016.7573443

[3] X. Zhao, A. Vardi, and J. A. d. Alamo, "Sub-Thermal Subthreshold Characteristics in Top-Down InGaAs/InAs Heterojunction Vertical Nanowire Tunnel FETs," *IEEE Electron Device Lett.,* vol. 38, no. 7, pp. 855-858, 2017, doi: 10.1109/LED.2017.2702612.

[4] A. Alian, Y. Mols, C. C. M. Bordallo, D. Verreck, A. Verhulst, A. Vandooren, R. Rooyackers, P. G. D. Agopian, J. A. Martino, A. Thean, D. Lin, D. Mocuta, and N. Collaert, "InGaAs Tunnel FET with Sub-Nanometer EOT and Sub-60 mV/dec Sub-Threshold Swing at Room Temperature," *Appl. Phys. Lett.,* vol. 109, no. 24, p. 243502, 2016, doi: 10.1063/1.4971830.

[5] L. Knoll, Q.-T. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schäfer, D. Esseni, L. Selmi, K. K. Bourdelle, and S. Mantl, "Inverters with Strained Si Nanowire Complementary Tunnel Field-Effect Transistors," *IEEE Electron Device Lett.*, vol. 34, no. 6, pp. 813–815, Jun. 2013. doi: 10.1109/TED.2017.2689746

[6] K. E. Moselund, D. Cutaia, H. Schmid, M. Borg, S. Sant, A. Schenk, and H. Riel, "Lateral InAs/Si p-Type Tunnel FETs Integrated on Si-Part 1: Experimental Devices", *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4233 - 4239, Nov. 2016 DOI: 10.1109/TED.2016.2606762

[7] E. Memisevic, J. Svensson, E. Lind, and L. -E. Wernersson, "InAs/InGaAsSb/GaSb Nanowire Tunnel Field-Effect Transistors," *IEEE Trans. Electron Devices,* vol. 64, no. 11, pp. 4746-4751, 2017, doi: 10.1109/TED.2017.2750763.

[8] E. Memisevic, M. Hellenbrand, E. Lind, A. R. Persson, S. Sant, A. Schenk, J. Svensson, R. Wallenberg, and L.-E. Wernersson, "Individual Defects in InAs/InGaAsSb/GaSb Nanowire Tunnel Field-Effect Transistors Operating Below 60 mV/decade," *Nano Lett.,* vol. 17, no. 7, pp. 4373-4380, 2017/07/12 2017, doi: 10.1021/acs.nanolett.7b01455.

[9] S. G. Ghalamestani, M. Berg, K. A. Dick, and L.- E. Wernersson, "High Quality InAs and GaSb Thin Layers Grown on Si (111)," *Jour. of Crystal Growth*, vol. 332, no. 1, pp. 12-16, July 2011. DOI: 10.1016/j.jcrysgro.2011.03.062

[10] H. Carrillo-Nuñez, M. Luisier, A. Schenk, "Analysis of InAs-Si Heterojunction Nanowire Tunnel FETs: Extreme Confinement vs. Bulk," *Solid-State Elect.*, vol. 113, no. -, pp. 61-67, Jun. 2015, doi: 10.1016/j.sse.2015.05.019

[11] E. Lind, E. Memisevic, A. W. Dey, and L.-E. Wernersson, “III-V Heterostructire Nanowire Tunnel FETs” *IEEE Jour. Electron Devices Soc.*, vol. 3, no. 3, pp. 96-102, May 2015. doi: 10.1109/JEDS.2015.2388811

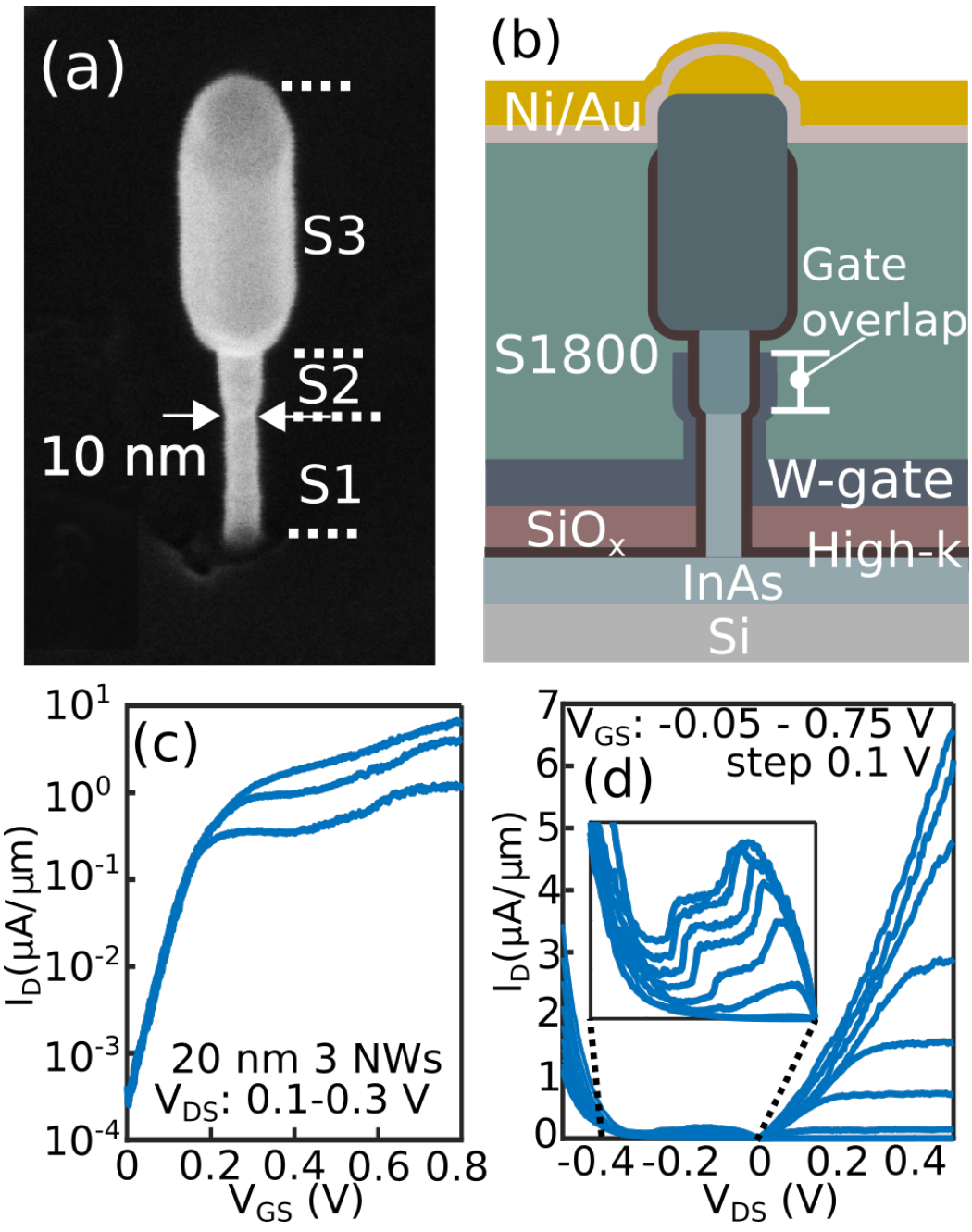
Figure Captions

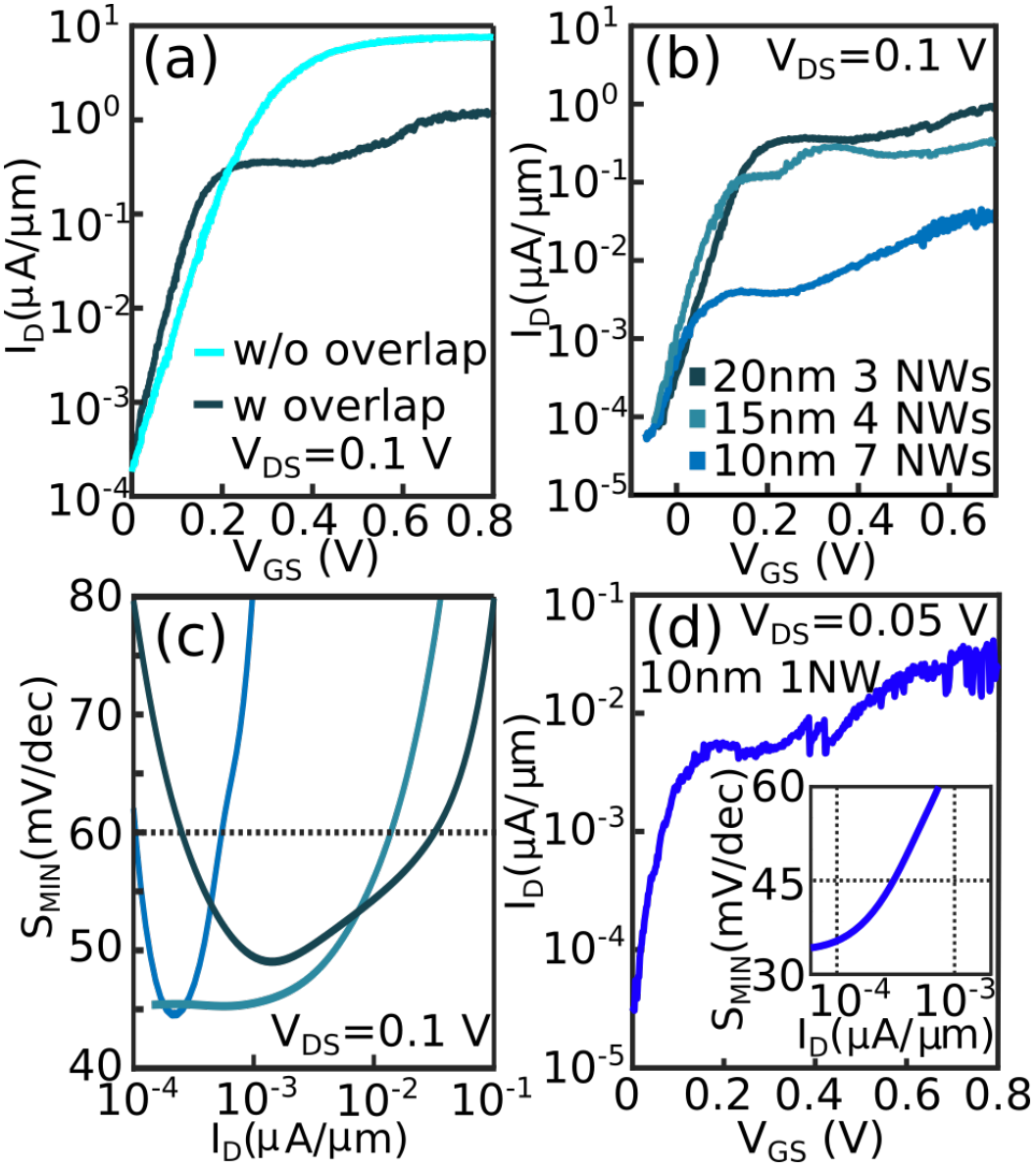
Figure 1. (a) Scanning electron microscope image of a nanowire with a diameter of 10 nm. S1 = InAs, S2 = InGaAsSb, S3 = GaSb (b) Schematic image of a device used in this work. (c) Transfer data from a device from group B with diameter of 20 nm. (d) Output data from same device as in fig (c). Insert shows NDR region. The current is normalized to the circumference and the number of nanowires.

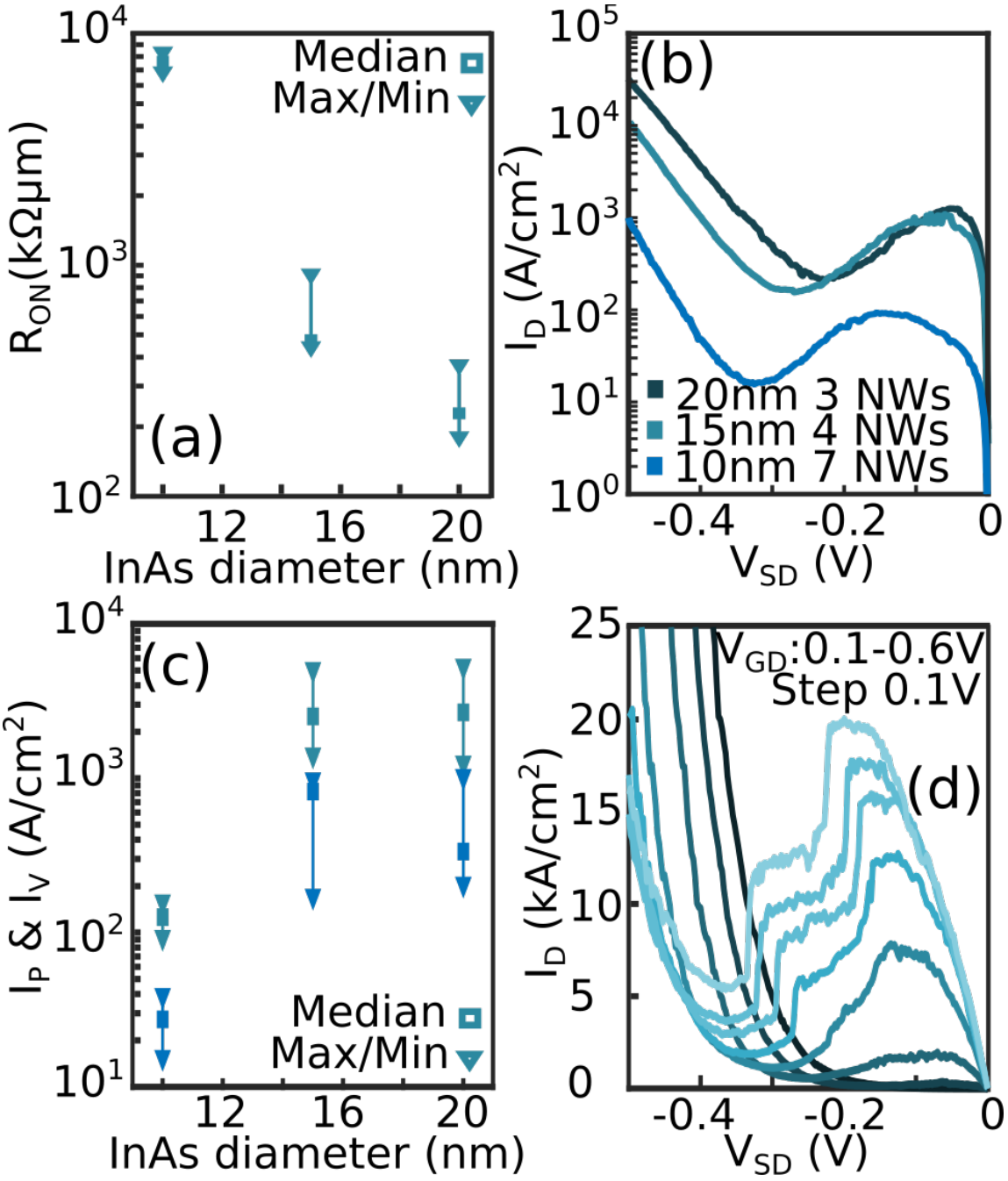
Figure. 2. (a) Transfer data from device from sample A (w/o overlap) and B (with overlap). Both devices comprise 3 nanowires. (b) Effects of diameter scaling for devices from the samples B, C, and D. (c) Point subthreshold swing of the same devices as in Fig 2c. (d) Transfer curve of a devices with 1 nanowire and 10-nm-thick InAs at the heterojunction. The device exhibits source depletion and RTS noise in the on-state. The insert shows point subthreshold swing of the device which reaches down to 35 mV/decade for V_{DS} = 0.05 V. The current is normalized to the circumference and the number of nanowires.

Figure 3. (a) Effects of diameter scaling on R_{ON}. (b) NDR region in the output data for V_{GS} (~0.22 V) which results in highest PVCR. Devices are from group B, C, and D. (c) I_{peak} and I_{valley} vs InAs diameter for devices in group B, C, and D. (d) NDR region for a device with diameter of 15 nm. The position of I_{peak} and I_{valley} moves to higher V_{SD} with increasing V_{GD}. The current in figure b-c is normalized using cross-sectional area at the heterojunction and number of nanowires.

Table I: Dimensions of nanowires and gate were measured with SEM during the processing of the transistors. (S1 = InAs segment, S2=InGaAsSb segment)


(a)
S3
S2
10 nm
S1
(b)
Ni/Au
Gate
overlap
S1800
W-gate
SiOx
High-k
InAs
Si
(c)
20 nm 3 NWs
VDS: 0.1-0.3 V
ID(μA/μm)
VGS (V)
(d)
VGS: -0.05 - 0.75 V
step 0.1 V
ID(μA/μm)
VDS (V)


(a)
w/o overlap
w overlap
V_{DS}=0.1 V
I_D(μA/μm)
V_{GS} (V)
(b) V_{DS}=0.1 V
20nm 3 NWs
15nm 4 NWs
10nm 7 NWs
I_D(μA/μm)
V_{GS} (V)
(c)
V_{DS}=0.1 V
S_{MIN}(mV/dec)
I_D(μA/μm)
(d) V_{DS}=0.05 V
10nm 1NW
I_D(μA/μm)
S_{MIN}(mV/dec)
I_D(μA/μm)
V_{GS} (V)


(a)
Median
Max/Min
R_{ON}(kΩμm)
InAs diameter (nm)
(b)
I_D (A/cm^2)
20nm 3 NWs
15nm 4 NWs
10nm 7 NWs
V_{SD} (V)
(c)
I_P & I_V (A/cm^2)
Median
Max/Min
InAs diameter (nm)
(d)
V_{GD}:0.1-0.6V
Step 0.1V
I_D (kA/cm^2)
V_{SD} (V)

Sample	Diameter of S1 & S2 (nm)	Length of S1 & S2 (nm)	Gate length (nm)	Gate overlap (nm)
A	20 / 30	145 / 90	130 – 135	-5 – -15
B	20 / 30	150 / 90	165	20 – 30
C	15 / 25	160 / 90	165 –175	20 – 30
D	10 / 18	160 / 90	185	35 – 40