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Monolithic integration of patterned BaTiO₃ thin films on Ge wafers

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Titanates exhibit electronic properties highly desirable for field effect transistors such as very high permittivity and ferroelectricity. However, the difficulty of chemically etching titanates hinders their commercial use in device manufacturing. Here, the authors report the selective area *in finestra* growth of highly crystalline BaTiO₃ (BTO) within photolithographically defined openings of a sacrificial SiO₂ layer on a Ge (001) wafer by molecular beam epitaxy. After the BaTiO₃ deposition, the sacrificial SiO₂ can be etched away, revealing isolated nanoscale gate stacks circumventing the need to etch the titanate thin film. Reflection high-energy electron diffraction in conjunction with scanning electron microscopy is carried out to confirm the crystallinity of the samples. X-ray diffraction is performed to determine the out-of-plane lattice constant and crystal quality of the BTO film. Electrical measurements are performed on electrically isolated Pt/BaTiO₃/SrTiO₃/Ge capacitor devices. *Published by the AVS.* https://doi.org/10.1116/1.5026109

I. INTRODUCTION

Titanates are an important class of materials that possess many interesting functional properties, i.e., ferroelectricity [BaTiO₃ (BTO), PbZr$_x$Ti$_{1-x}$O₃],[1,2] large dielectric constant [CaTiO₃, BaTiO₃, SrTiO₃ (STO), and Ba$_x$Sr$_{1-x}$TiO₃],[3–8] and high Pockels coefficient.[9–13] A wide variety of applications exist for them, such as nonvolatile memory,[14,15] microwave device applications (Ba$_x$Sr$_{1-x}$TiO₃),[16–18] and waveguides.[10,19–22] Due to their very high dielectric constants and added functional behavior such as ferroelectricity and piezoelectricity,[23–25] titanates could replace SiO₂ and even high-k dielectrics like HfO₂ in the future as gate dielectrics in MOSFET devices.[26–28] Ferroelectrics have also been explored to achieve a steep subthreshold swing of <60 mV/dec.[29,30] However, practically all microelectronic device manufacturing is based on the ability to pattern such materials using some form of etching. The main problem in fabricating titanate-based devices on a submicron level is the lack of an easy way to etch and pattern this class of materials. Selective wet chemical etching of titanates is not available and even nonselective reactive ion etching is not suitable because it is extremely slow and degrades not only the quality of the titanate layer, but more importantly, the quality of the surrounding device areas as well. This resistance to chemical and reactive ion etching of titanates hinders their commercial use in device manufacturing. If one could find a way to pattern and integrate them into existing semiconductor processes, they could lead to great improvements in existing electronic devices such as microprocessors or new kinds of integrated architecture combining optical or sensor functionality and logic/memory on a single chip.

These problems can be circumvented by growing titanates as a gate-last process into the openings of predeposited sacrificial layers of SiO₂ that then can be easily and selectively etched away. By depositing the titanate last on a prepatterned sacrificial layer, and then by etching away this sacrificial SiO₂ layer, the need to selectively etch the titanate layer to fabricate devices is no longer necessary. Here, we report the growth of out of-plane polarized BTO on germanium by molecular beam epitaxy (MBE) within microscopically patterned openings (*in finestra*) of a sacrificial SiO₂ layer on a Ge(001) substrate. A thin template layer of STO is grown on the Ge substrate to impose compressive strain on BTO which leads to an out of-plane polarization of BTO,[31,32] followed by Pt metal deposition as a top electrode. Isolated Pt/BTO/STO/Ge capacitor structures are then formed by removing the SiO₂ pattern using buffered oxide etch (BOE). In order to evaluate the electrical performance of the stack, capacitance versus voltage (C-V) and current versus voltage (I-V) measurements are performed. The technique describes a method by which titanium oxides and titanates can be readily patterned into desired shapes by using a combination of existing processing techniques without the need to etch the titanate itself. This proof of principal will allow titanates to be used in nanoscale devices, such as a super high-k gate dielectric material in capacitors and MOSFET devices.

II. EXPERIMENTAL DETAILS

Ge(001) wafers (p-type, 0.059–0.088 Ω cm) are first degreased with acetone and isopropyl alcohol and then wet chemical cleaned with hydrofluoric acid (HF) (49%)/de-ionized H₂O (DI-H₂O) (1:1150) and NH₄OH (27%)/DI-H₂O (1:2000) in an automated spray acid tool at elevated temperatures (60–90 °C). For a typical lift off experiment, a patterned bilevel photoresist profile is generally used, however,

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due to the higher growth temperature of MBE grown films, this is not an option for this work. In this case the lift off profile is achieved by the deposition of a two layer system (1) a plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide layer (200 or 500 nm) followed by (2) an undoped polycrystalline layer of silicon (100 nm) at 570 °C. Openings in these layers are patterned using standard optical photoresist and ultraviolet lithography. The patterned openings are transferred through the polysilicon layer using a Trikon Omega 201 MORI dry-etch tool with a $Cl_2/HBr/O_2$ plasma which has high selectivity to the under-lying oxide. The lift off profile is realized by using a buffered oxide etchant (5:1) at room temperature to etch the underlying oxide layer to both expose the germanium in the openings and also to etch laterally under the defined polysilicon edge to create an overhang which is the desired profile for lift off. A schematic image of the final SiO_2 pattern on the germanium wafer is shown in Fig. 1.

Prior to BTO growth, the patterned Ge wafer is diced into $10 \times 10 \, mm^2$ pieces. For the BTO thin film deposition, a customized DCA Instruments M600 MBE chamber with a base pressure of $3.0 \times 10^{-10} \, Torr$ is used. Ba, Sr, and Ti are evaporated using Knudsen effusion cells while an electron beam evaporation source is used for Pt. A quartz crystal monitor is used to calibrate the metal deposition rate. A Staib Instruments electron gun operating at 21 keV for reflection

high-energy electron diffraction (RHEED) under a grazing angle of 3° is used to monitor the crystal growth and surface quality. X-ray photoelectron spectroscopy (XPS) of the samples is carried out in a VG Scienta custom analysis chamber with an R3000 electron energy analyzer and monochromated Al Kα radiation to fine tune the exact stoichiometry of the BTO and STO films. The MBE chamber is connected to the XPS through a vacuum buffer line to allow *in situ* sample transfer without breaking the vacuum. X-ray diffraction measurements are performed using a Rigaku Ultima IV diffractometer with a Cu Kα radiation source. The microstructure of the fabricated samples is analyzed by top–down scanning electron microscopy (SEM), which was performed on an FEI 650 FEG SEM. Cross-sectional transmission electron microscopy (XTEM) was carried out using the JEOL 2100 HRTEM operated at 200 kV. Cross-section samples were prepared by focused ion beam etching using a FEI's Dual Beam Helios Nanolab system. For I-V and C-V measurements the KEITHLEY 37100 and KEITHLEY 2602 are used.

Before loading the samples into the UHV system, the Ge substrates are degreased in acetone, isopropanol and deionized water for 10 min each using a sonicator. The samples are then transferred into the MBE where they are exposed to oxygen plasma for 30 min at 100 °C, completely removing carbon contamination from the Ge surface. The plasma exposure also forms a thin oxide layer on the Ge surface, which has to be removed through a final vacuum anneal for 1 h at 750 °C to obtain an atomically clean, 2×1 reconstructed Ge surface. The sharp and intense half ordered spots of the cleaned Ge surface can be clearly seen in Fig. 2(a). The details of the Ge cleaning procedure used can be found elsewhere.[33] It should be noted that unlike the Ge cleaning procedure described by Ponath *et al.*,[33] it is found, in this case, that a wet-etching step prior to the oxygen plasma cleaning is not critical in obtaining the same Ge surface quality.[34]

After the final annealing step at 750 °C, $1/2$ monolayer of Ba is deposited at 200 °C to form a Zintl template.[35–39] This template prevents Ge from forming germanium oxides during the growth of the STO buffer layer. STO of 2 nm are then grown by codeposition of Sr and Ti on this Zintl template at 200 °C using $5 \times 10^{-7} \, Torr$ molecular oxygen. This thin STO layer is needed to impose compressive strain on BTO to achieve an out of-plane polarization.[31] Increasing the substrate temperature to 750 °C with a ramp rate of 30 °C/min crystallizes the STO film, as can be seen in Fig. 2(b). The narrow streaks are typical for epitaxial and smooth crystalline STO films.[31] The molecular oxygen pressure is then increased to $5 \times 10^{-6} \, Torr$ and 16 nm of BTO is deposited on the STO/Ge template at 750 °C, by shuttering the Ba and Ti effusions cells. At this temperature BTO crystallizes as deposited, as observed by RHEED [see Fig. 2(c)]. When the desired film thickness is reached, the sample is cooled down to 200 °C with a ramp rate of 30 °C/min in an oxygen environment of $5 \times 10^{-6} \, Torr$. Immediately after growth, the sample is transferred in vacuum into the XPS to verify the correct stoichiometry of the grown films. The samples are then transferred back into the MBE chamber where at least
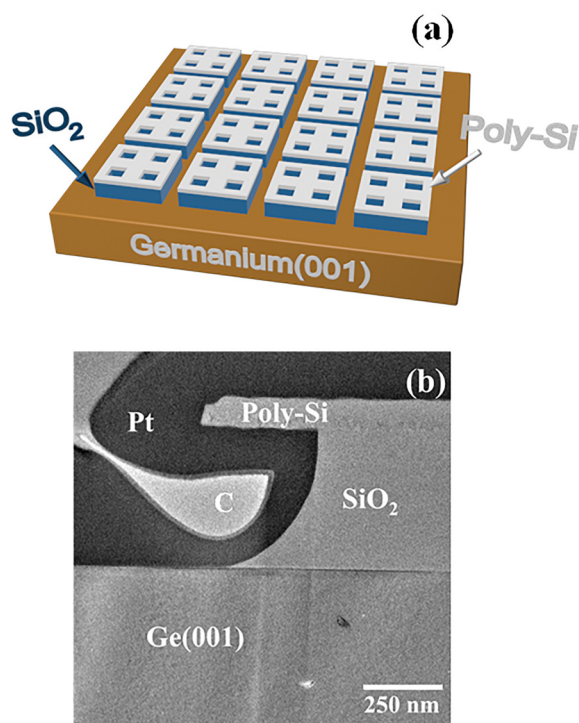

FIG. 1. (Color online) (a) Schematic of the lithographically defined polycrystalline Si overhang (white, 100 nm) and SiO_2 pattern (blue, 500 nm) on the p-type Ge wafer (brown). The square SiO_2 patterns are $400 \times 400 \, \mu m^2$ in size and $100 \, \mu m$ apart from each other. The openings inside the SiO_2 pattern have a dimension of $80 \times 80 \, \mu m^2$. (b) Cross-sectional TEM image of the poly-Si/SiO_2/Ge structure prior to deposition. The visible Pt layer is part of the TEM sample preparation process. After the thin film and top gate deposition, the sacrificial SiO_2 can be lifted off by chemical etching, revealing micron scale gate capacitor devices of $80 \times 80 \, \mu m^2$.
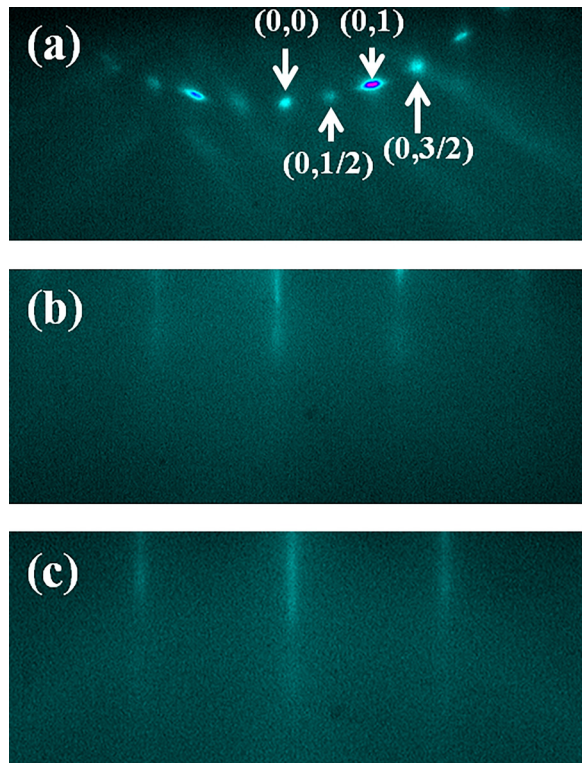
FIG. 2. (Color online) (a) 2×1 reconstructed Ge surface after oxygen plasma exposure followed by a thermal anneal at $750\,^\circ C$. (b) STO of 2 nm thick on Ge(001) viewed along the [110] direction. (c) Crystalline BTO of 16 nm grown on top of the STO/Ge viewed along the [110] direction.

10 nm of Pt is deposited at a substrate temperature of $100\,^\circ C$ with a growth rate of around 1 Å/min using electron beam evaporation. After a sufficiently thick layer of Pt is deposited *in situ*, the sample is taken out of the vacuum system and additional 100 nm thick Pt is sputtered on top *ex situ* at a rate of 60 Å/min using e-beam evaporation, to make a top contact thick enough so it can be probed by the needles during electrical characterization without punching though to the substrate.

III. MATERIALS CHARACTERIZATION

A. Reflection high-energy electron diffraction

A major MBE-growth-problem that arises when a substrate is almost completely covered with a sacrificial layer with only a few small openings to allow crystalline growth, is the very weak RHEED signal. The ratio between the amorphous SiO_2 layer covering most of the Ge substrate and the small areas of crystalline film is too small to obtain even qualitative RHEED information about the crystal quality. Due to the grazing angle of incidence of about 3° in RHEED, the aspect ratio of the SiO_2 openings (wall height and width) must also be considered, if one uses the RHEED signal coming from the crystalline films within the openings. To work around this issue, the sacrificial SiO_2 is lithographically patterned in such a way that it forms islands of SiO_2 on the Ge surface with four openings inside them (see Fig. 1). This results in the presence of relatively large areas of exposed Ge. By having a large area of the Ge substrate not covered by SiO_2, BTO not only crystallizes in the small openings inside the SiO_2 window, but also on the exposed areas between the SiO_2 islands. With this setup, a high coverage of crystalline BTO on Ge is obtained leading to a strong RHEED signal allowing one to control and monitor the crystal quality of the deposited BTO film.

B. X-ray diffraction

To determine the out of-plane lattice constant and overall crystal quality, x-ray diffraction measurements are performed. A symmetric 2θ-θ scan of a 16 nm thick BTO film on the STO/Ge template is shown in Fig. 3 plotted on a log scale. Only peaks from single orientations of BTO, STO and the Ge substrate are observed. Typical high resolution scans around the BTO (002) peak indicate an out of-plane lattice constant between 4.03 and 4.05 Å, corresponding to the longer c-axis being out of plane and the shorter a-axis to be in-plane. Due to the direction of the long axis being out of plane, this implies that the BTO ferroelectric polarization points normal to the Ge surface.[31] Rocking curve scans around the BTO (002) Bragg peak reveal FWHM values lying in the range of 0.5°–1.0° (see Fig. 3 inset).

C. TEM and SEM

Figure 4(a) shows a cross sectional transmission electron microscope (TEM) image of the deposited BTO film on the sacrificial poly-Si/SiO_2 structure on Ge. The polycrystalline Si overhang layer, preventing thin film deposition on the SiO_2 layer, can be removed using BOE. The crystal quality of the BTO and STO layer grown in an opening is confirmed using cross-sectional TEM [Fig. 4(b)]. The absence of an amorphous GeO_2 layer between the STO and Ge substrate is confirmed and expected due to the use of a Zintl template. Both STO and BTO layers are highly crystalline with sharp interfaces between the different layers. Both oxide layers show highly uniform growth in conjunction with a very low surface roughness. To form electrically isolated Pt/BTO/STO/Ge metal oxide semiconductor capacitor (MOSCAP) structures, the sacrificial SiO_2 layer is removed using BOE which also leads to the removal of the SiO_2 and the
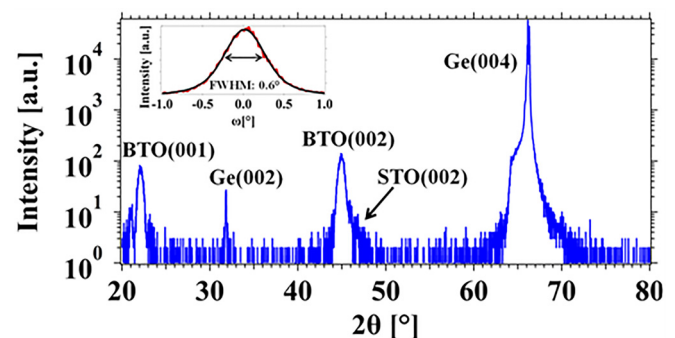

FIG. 3. (Color online) 2θ-θ scan of a 16 nm thick BTO film grown epitaxially on 2 nm STO on Ge(001). Only peaks from Ge, STO and BTO are observed. The c lattice parameter of BTO is between 4.03 and 4.05 Å and is directed out of plane. The inset shows the rocking curve around the BTO (002) peak for the same film with a FWHM value of 0.6°.

overlaying polycrystalline-Si layer. As can be seen in Fig. 4(c), isolated square patterned Pt/BTO/STO/Ge MOSCAPs are revealed in areas where the SiO_2 layer is removed. Current versus voltage (Agilent B 1500) and capacitance–voltage (E4980A Precision LCR Meter) measurements were performed in a Cascade probe station in a dry air environment at 22 °C. The current–voltage analysis of the Pt/BTO/STO/Ge gate stack revealed high leakage values of 1.9×10^{-1} and 2.9×10^{-1} A/cm^2 at -0.1 and $+0.1$ V on the Pt gate, respectively. From inspection of the cross sectional TEM image in Fig. 4(a), the presence of the void at the periphery of the defined STO/BTO gate stack results in the possibility of direct contact of the Pt gate to the Ge substrate, which is a probable source of the high leakage current. Furthermore, the conduction band offset between BTO/STO and Ge is nearly zero further adding to the leakage.[40]

The capacitance and conductance of the Pt/BTO/STO/Ge gate stack were measured with a 25 mV ac signal level in parallel mode. The leakage currents preclude meaningful
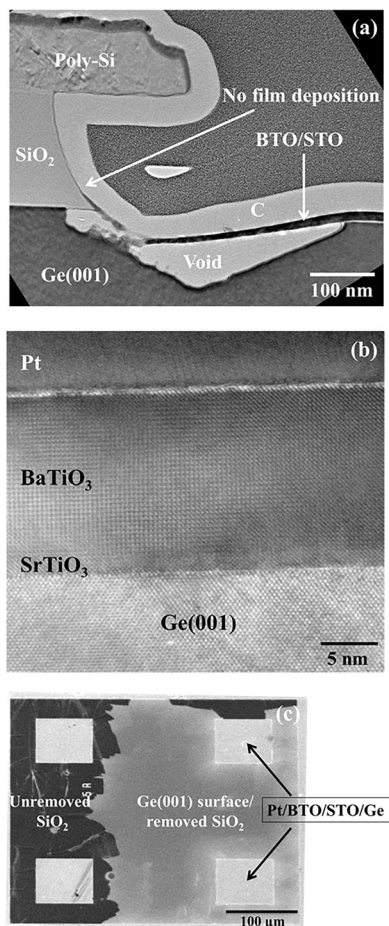

FIG. 4. (a) Representative XTEM image of the structure shown schematically in Fig. 1. The polycrystalline-Si overhang prevents film deposition on the sacrificial SiO_2 layer, allowing its removal with BOE. (b) XTEM confirming the crystal quality of the BTO and STO layer grown on the exposed Ge areas. Both STO and BTO layers are highly crystalline with sharp interfaces between the different layers. Both oxide layers show highly uniform growth in conjunction with a very low surface roughness, (c) top-view SEM image showing the test structure after the BOE etch, revealing patterned Pt/BTO/STO/Ge capacitor devices.

capacitance measurements over an extended bias range, however, at 0 V the measured impedance (3.25×10^3 Ω) and phase angle ($-58.2°$) at 100 kHz yield a capacitance of around 0.063 F/m^2, compared to an expected value of around 0.11 F/m^2 based on relative dielectric constant values of 50 and 400 for the thin film STO and BTO films, respectively.[41,42] This demonstrated the expected high capacitance per unit area of the Pt/BTO/STO/Ge gate stack. Further studies are ongoing to substantially reduce this leakage current including, further analysis of the peripheral Ge void, growth in oxygen plasma,[43] wet oxygen postdeposition annealing, Al doping, and N doping.

The SEM and TEM image confirm that the method of using a sacrificial oxide with openings can indeed be used to grow crystalline titanate films in small openings, and that the capacitor stacks can be revealed by means of a subsequent lift-off process.

IV. SUMMARY AND CONCLUSIONS

In summary, we report the growth of highly crystalline *c*-axis oriented BTO in the photolithographically patterned openings of sacrificial SiO_2 (*in finestra*) on a germanium (001) wafer by molecular beam epitaxy. RHEED, x-ray diffraction, SEM, and TEM are performed to confirm the high crystal quality of the BTO film within the openings. Buffered oxide etch is then used to electrically isolate a given device from the rest of the film to perform electrical measurements. Current versus voltage measurements reveal a relatively high leakage current through the BTO/STO/Ge gate precluding meaningful capacitance measurements over an extended bias range This selective area deposition in conjunction with a general lift off process can be used to create nanoscale titanate capacitor structures in the future, circumventing the problem of having to etch titanate materials. Such a process can ultimately be refined for the fabrication of titanate-based three-terminal devices.

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