Millimetre Wave Series Connected Doherty PA Using 45nm SOI Process

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

With the high demand for high data rate communication systems, it is expected that wireless networks will migrate into the unexploited millimeter-wave frequencies. This migration and the utilization of wideband digitally modulated signal possessing of high Peak-to-Average-Power-Ratio (PAPR) brings difficult challenges in attaining a satisfactory trade-off between linearity and efficiency when designing mm-wave power amplifiers (PAs).

There are various methods of maximizing the output power and peak efficiency of mm-wave PAs that use deep-sub-micron technologies. Of these methods, little attention has been given to the efficiency enhancement of PAs in back-off region. The use of the Doherty technique in the mm-wave frequencies has attracted little attention. This is mainly due to complexity in realizing the $\lambda/4$ impedance inverter and the low-gain of the class-C operating peaking transistor using deep-sub-micron technologies.

In this thesis, a series-connected-load (SCL) Doherty topology is proposed to enhance the efficiency of a millimeter-wave power amplifier realized on a deep-sub-micron semiconductor technology. The output combiner is determined by the $ABCD$ matrices of the ideal combiner network in the SCL Doherty PA to ensure proper load modulation. Then, it describes the methodology applied to realize the transformer-based combiner networks while absorbing the parasitic capacitances of the transistors to maximize efficiency in the back-off region. This methodology is then applied to realize a two-stage SCL Doherty PA in 45 nm Silicon-on-Insulator CMOS technology to operate at 60 GHz.

Acknowledgements

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I am truly indebted to my beloved parents Mohammed and Hessa for their unconditional love, constant prayers, and endless support. May Allah reward them in this world and in the hereafter. I also extend my deepest appreciation to my siblings Fahad and Alhanouf for their friendship and encouragements.

Dedication

This is dedicated to my parents and my grandparents

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List of Acronyms

AC	Alternating Current
AM-AM	Amplitude-Amplitude
AM-PM	Amplitude-Phase
BEOL	Band-End of the Line
CMOS	Complementary Metal-Oxide-Semiconductor
CW	Continuous-Wave
DAT	Distributed Active Transformer
DC	Direct Current
DPA	Doherty Power Amplifier
DSM	Deep Sub Micron
DUT	Device Under Test
EER	Envelope Elimination Restoration
ET	Envelope Tracking
GSG	Ground-Signal-Ground
HP	High Power
LP	Low Power

MM-Wave	Millimeter-Wave
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PA	Power Amplifier
PAE	Powed-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCT	Parallel Combining Transformer
PDF	Probability Density Function
RF	Radio-Frequency
SCL	Series-Connected Load
SCT	Series Combining Transformer
SiGe	Silicon Germanium
SOI	Silicon-on-Insulator
SOLT	Short-Open-Line-Thru
OFDM	Orthogonal Frequency-Division Multiplexing
VNcap	Vertical-Nature Capacitor

Chapter 1

Introduction

1.1 Motivation

Wireless technologies have become an integral part of our everyday life and a key element in improving the productivity of various economic sectors. Its application is rapidly expanding from personal voice and data centric communication services to machine-to-machine centric communications. The number of wirelessly connected devices is expected to reach an average of 25 Billion by 2021 [1]. Given the limited spectrum resources in the sub-6 GHz portion, wireless communication systems are expected to expand into the untouched millimeter-wave (mm-wave) frequencies (30 GHz - 300 GHz) where the wavelength of the signal is in the millimeter range. Mm-wave frequency allow for larger bandwidth utilization enabling high data rates to mobile broadband applications, reliable short range communications, and automotive radar [2]; however, this frequency band is unlicensed. About 23 GHz of bandwidth is assigned to mm-wave cellular in the 30-100 GHz band. For short range communications, the 57-64 GHz frequency band is utilized due to the high atmospheric attenuation due to oxygen absorption at that frequency range [2]. This frequency shift comes with the cost of significantly complicating

the radio front-end hardware, especially when the communication signals are digitally modulated using spectrally efficient techniques (modulation bandwidth in the hundred of MHz and GHz range) and consequently exhibit high peak-to-average-power ratio (PAPR). An example of a signal with high PAPR is Orthogonal Frequency-Division Multiplexing (OFDM) as shown in Fig.1.1(a). The probability density function (PDF) of these complex digitally modulated signal follows Rayleigh PDF as shown in Fig. 1.1(b). This acts as an obstacle to obtain an adequate linearity vs. efficiency trade-off when designing mm-wave power amplifiers (PAs). As a result, the PA is forced to operate below peak power, hence, reducing the efficiency of the PA. To efficiently amplify signals with high PAPR the radio frontend requires PA that is efficient at peak power and at back-off power levels. Motivating the need for efficiency enhanced PAs.

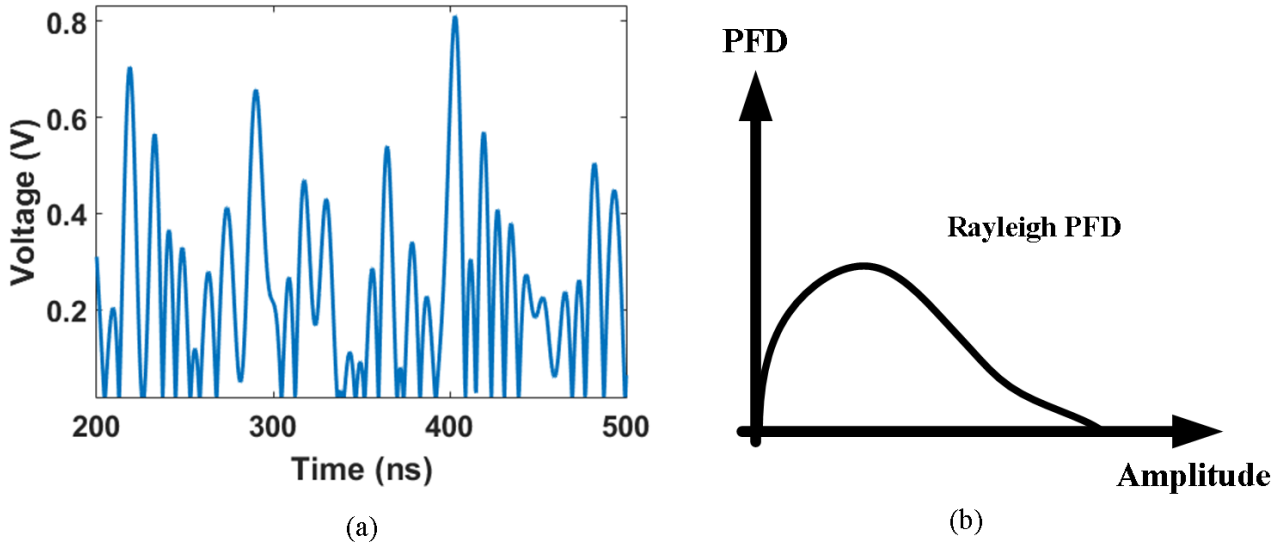

Fig. 1.1: (a)Amplitude of OFDM signal (b) Rayleigh PDF

This frequency migiration will complicate the design of the key blocks in the transmitters path and the PA is considered to be the most critical block. Implementing PAs at mm-wave is a difficult. First, although the advanced deep-sub-micron (DSM) silicon technologies offer higher transistor transition frequency (f_T) they suffer from a low breakdown voltage. For instance, the gate oxide breakdown voltage of a Metal-Oxide-semiconductor field-effect transistor (MOSFET)

is below 1.8 V since the thickness of the silicon oxide layer is below 2 nm or less [3]. As a result, the RF output power of the PA is limited by the supply voltage of the technology. Silicon germanium (SiGe) technology is preferred when operating at mm-wave frequencies due to its high output resistance and lower substrate losses. However, complementary metal-oxide semiconductor (CMOS) has attracted more attention since it provides lower-cost thean SiGe when the volume of production is in the millions per year. A second limitation is that, as the operating frequency increases the maximum stable gain of the transistor is reduced resulting in a significant negative effect on the efficiency of the PA. Adding more stages to the PA can achieve higher gain but it comes at the cost of increasing the direct-current (DC) consumption of the overall PA; hence, lowering the overall efficiency of the transmitter.

1.2 Thesis Objectives

Several RF device and circuit levels techniques were utilized to increase the achievable output power and the efficiency of mm-wave PAs using DSM silicon technologies. At the device level, various voltage combining (transistors stacking [4]) and current combining (digital PAs [5]) methods have been adopted to increase the maximum achievable voltage or current and consequently maximizing the output power. However, the non-negligible parasitics of the devices impose practical bounds on the achievable power for each technology. At the circuit level, while significant efforts were made to increase the PAs peak efficiency using harmonically tuned modes of operations (Class F, F^{-1}, D) [6], however very little attention was given to the enhancement of the efficiency in back-off region, especially as the frequency increases. This is critical to the efficient amplification of digitally modulated signals with high PAPR. For example, while being a very popular technique at the sub-6 GHz frequencies, the Doherty technique attracted very limited attention at mm-wave.

The realization of mm-wave Doherty PAs using DSM technologies faces several challenges. First, the low gain of the class-C operating peaking transistor often imposes either the utilization of an oversized transistor compared to the main transistor or an uneven power splitting ratio at the input resulting in a larger output capacitance or lower overall Doherty PA gain. While utilized at low frequencies, both approaches are not suitable for at the mm-wave frequencies. Adaptive gate biasing of the peaking transistor has been utilized in [7]-[8] to overcome the low gain of the peaking transistor but would require an additional high speed DC/DC converter circuitry due to the large modulation bandwidths at the mm-wave frequencies. Secondly, the $\lambda/4$ impedance inverter in Doherty PA and its inherent losses and frequency dispersive behavior present a major source of efficiency deterioration in the back-off region and bandwidth limitation. To minimize these drawbacks, authors in [9] opted for SiGe Bi-CMOS process with a high resistivity substrate.

To overcome the afore mentioned challenges, this thesis proposes a Series-Connected-Load (SCL) Doherty PA (DPA) as an alternative solution to the conventional parallel-connected DPA scheme. The SCL places the $\lambda/4$ impedance inverter line at the output of the peaking amplifier rather then having it at the output of the main amplifier. This is to ensure that the losses of the $\lambda/4$ impedance inverter line do not contribute to the efficiency in the back-off region of the DPA and the leakage in the back-off region is minimized. Furthermore this thesis proposes a series output combiner that is derived from $ABCD$ matrices to achieve proper load modulation in the SCL DPA.

1.3 Organization of the Thesis

The organization of the thesis is as follows. Chapter two starts with an overview of the classes of operation of PAs. Then, it discuses the output power maximization techniques for PAs at mm-wave frequencies at device and circuit levels. Furthermore, it continues with a brief

overview of the conventional parallel-connected DPA. Finally, a literature review on the latest mm-wave DPA is presented.

Chapter three introduces the theory behind the SCL DPA and proposes an output combiner which is derived to absorb the parasitics of the main and peaking transistors. Lastly, ideal simulations are presented to verify the proposed theory.

Chapter four presents a 60 GHz mm-wave SCL DPA designed using the proposed output combiner and fabricated using a 45 nm CMOS Silicon-on-Insulator (SOI) technology. Simulation and measurement results of the design are presented in Chapter four. Finally, Chapter five presents concluding remarks and suggests some future work.

Chapter 2

Literature Review on mm-Wave DPA

Designing PAs using DSM silicon technologies such as CMOS and SiGe poses many challenges at mm-wave. Many specifications increase the design complexity such as output power, linearity, efficiency, reliability, and bandwidth. The PA designer must balance performance trade-offs among the design complexity factors to achieve good performances in the majority of the factors. Furthermore, it is difficult to realize a fully integrated PA using DSM technologies due to the intrinsic drawbacks of these technologies, that are, low-quality factor of lossy substrate of passive structures and low breakdown voltages of active devices [10]. Thus, it is essential to have an additional block to the PA, i.e. power combiner, to combine output power from various unit power cells to generate an acceptable overall output power at mm-wave [10]. In addition, while transmitting broadband complex modulated signals that exhibits high PAPR, the PA is forced to operate at a lower input power level; hence, yielding poor efficiency. This motivates the need of efficiency enhancement of PAs at mm-wave frequencies. This chapter discusses the basics of PAs and the classes of operation. Furthermore, it briefly describes the popular power combining techniques used at mm-wave to maximize the output power of the PA. The remainder of this chapter explores the possible PA efficiency enhancement techniques used at mm-wave. Special attention will be given to the Doherty technique and its feasibility

at mm-wave frequencies since it's the focus of this thesis. Moreover, it presents the analysis of the conventional DPA to show a better understanding of load modulation and the limitation of the conventional DPA. Lastly, a literature survey will be presented on recent DPA works at mm-wave frequencies.

2.1 Overview of PAs

The PA can be described as a DC to RF power converter. The PA amplifies the RF input power, P_{in}, and delivers the output power, P_{out}, to the load. At low input power, the RF input power is amplified by a certain constant gain, G. The linear power gain of the PA is defined as the radio of the output power delivered to the load to the input of the PA,

$$G = \frac{P_{out}}{P_{in}} \tag{2.1}$$

In order to deliver the output power to the load, the PA must consume DC power, P_{DC}, from the DC source. One metric of determining the efficiency of the PA is the drain efficiency,

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.2}$$

The Power-Added Efficiency (PAE) is another figure of merit that provides more insight on the effectiveness of the DC to RF power conversion. The PAE includes the RF input power and this is important especially when the PA exhibits low gain; for example, at mm-wave where the transistor's stable gain is limited especially at mm-wave frequencies. The PAE is defined in the following equation,

$$PAE = \frac{(P_{out} - P_{in})}{P_{DC}} = \eta(1 - \frac{1}{G}) \tag{2.3}$$

It is evident that as the gain of the PA increases the PAE converges to η. In order for the PA to deliver the maximum power to the load the PA is usually matched to a certain impedance so called the optimum impedance, R_{opt}. It is defined as the ratio of the fundamental voltage amplitude (approximately V_{DC}) to the fundamental current amplitude (approximately I_{max}) as shown in (2.4). This is to ensure that the transistor delivers the maximum power without over stressing the transistor. In addition, the input of the PA is conjugated matched to the impedance of the previous stage to achieve an acceptable gain.

$$R_{opt} = \frac{V_{DC}}{I_{max}/2} \tag{2.4}$$

Another performance metric that is important for PA design is the 1 dB compression point of the PA. It is the power at which the 1 dB gain drop from the linear gain of the PA.

The class of operation for the PA is defined by the biasing point and load terminations (at fundamental and harmonics) of the transistor. Fig. 2.1 shows the I-V characteristic of an ideal transistor model that is primarily a voltage controlled current source.

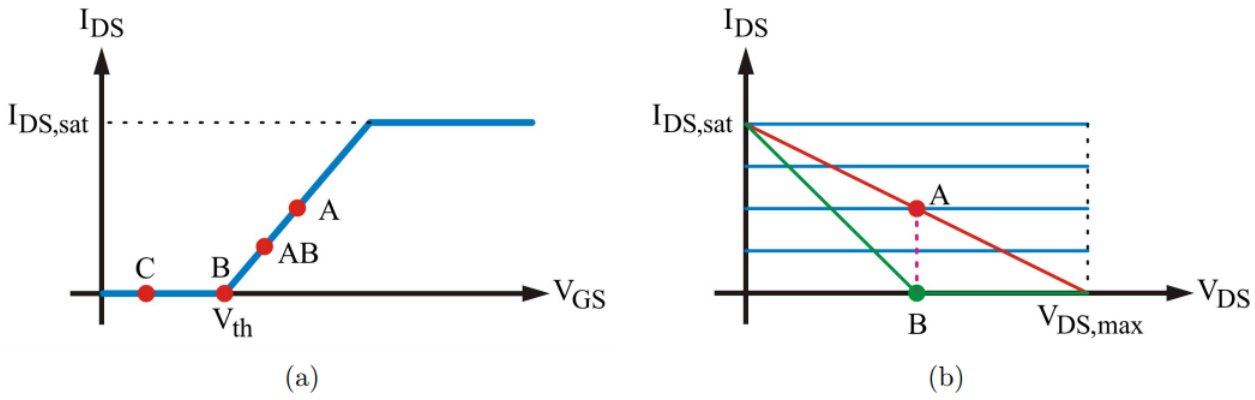

Fig. 2.1: (a) Current versus gate bias (b) I-V Characteristics of ideal transistor [11]

For class-A PA, the transistor is biased at the mid-point of the I-V characteristic of the transistor i.e. $I_{max}/2$ and $V_{DSmax}/2$. This is to ensure that both output voltage and current waveforms are perfectly sinusoidal, thus, indicating that class-A is a linear operation. In addition, the DC power of the class-A PA consumes $I_{max}/2$ and $V_{DSmax}/2$ even when the RF input power is not present. The DC power of a class-A PA is,

$$P_{DC,A} = \frac{I_{max}V_{max}}{4} \tag{2.5}$$

The RF peak power of the class-A PA,

$$P_{out,A} = \frac{I_{max}V_{max}}{8} \tag{2.6}$$

Therefore, the peak efficiency of class-A PA,

$$\eta_A = \frac{P_{out,A}}{P_{DC,A}} = 50\% \tag{2.7}$$

Hence, the downside of a class-A PA is that half of the power is dissipated as heat and lowering the peak efficiency. However, the class-A PA achieves the highest gain among all classes of operation.

There are two ways of increasing the peak efficiency of the PA, one is to reduce the DC power consumption and the other is to increase the RF output power. The class-B PA increases the peak efficiency by reducing the DC power consumption. This is done by biasing the gate of the transistor at threshold level so when the RF input power is not present at the input of the transistor there is no DC power consumption. Since the transistor is biased at threshold level, the PA is only conducting current half the cycle and the conduction angle is π. As shown in Fig. 2.2 the current waveform for a class-B PA is half sinusoidal. Thus, the peak efficiency of

a class-B PA is calculated though the following,

$$P_{DC,B} = \frac{I_{max} V_{max}/2}{\pi} \tag{2.8}$$

$$P_{out,B} = \frac{I_{max} V_{max}}{8} \tag{2.9}$$

$$\eta_B = \frac{P_{out,B}}{P_{DC,B}} = \frac{\pi}{4} = 78.5\% \tag{2.10}$$

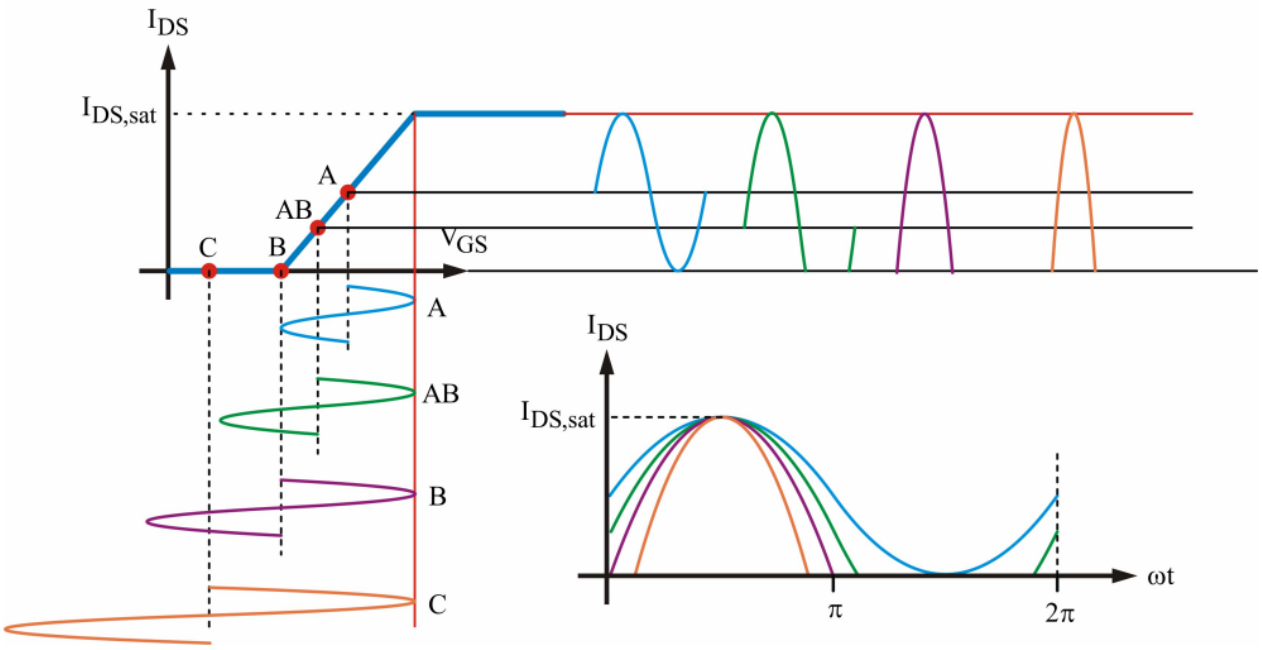

Fig. 2.2: Current waveforms and conduction angles for classes of operation [11]

Hence, the advantage of the class-B PA is the reduction of the DC power consumption when there is no RF power at input. However, this is in the cost of reducing the PAs gain by 6 dB since a class-B PA needs to be driven twice as hard as a class-A PA to achieve the same output power. Furthermore, when the conduction angle is less than 2π the harmonics start to distort the voltage and current waveforms. For a class-B PA all harmonics must be terminated with a short circuit. When conduction angle is between 2π and π, the PA is classified as class-

AB. It exhibits a higher peak efficiency than class A and higher gain than class-B. When the conduction angle is lower than π the PA is classified as class-C PA and the peak efficiency is ideally 100%. However, this sacrifices the gain. Lastly, class-AB and C are classified as nonlinear PAs since the conduction angle varies with input power; whereas, the class-A and B do not and are classified as linear modes of operation. Table 2.1 summaries the characteristics of the classes of operation of PAs.

Table 2.1: Comparison of PA classes

Class	**Conduction Angle (α)**	**Efficiency (%)**	**Gain**	**Linearity**
A	2π	50	Excellent	Excellent
AB	$2\pi < \alpha < \pi$	$50 < \eta < 78.5$	Good	Good
B	π	78.5	Fair	Fair
C	$\alpha < \pi$	100	Poor	Poor

Until now, all the mentioned classes of operation must terminate all harmonics with short circuit. However, there are other classes of operation that tune the harmonics to achieve high peak efficiency. For instance, Class-F/F^{-1} is biased as class-B and terminate the even harmonics with short/open impedance and the odd harmonics are terminated with open/short impedances to engineer the waveform of the output current and voltage.

2.2 Power Maximization of mm-wave PAs

Implementing the classes of operation of PAs is difficult and more complex using DSM silicon technologies at mm-wave frequencies. The DSM silicon technologies provide low output power and this is primarily due to the low breakdown voltage of the active device which reduces the maximum operating voltage and output voltage swing of the PA. However, DSM silicon technologies are capable of integrating complex circuit techniques to increase output power, peak efficiency, and linearity while keeping the cost of fabrication at minimum. This section

provides an insight on the power combining techniques that are utilized at mm-wave frequencies at the device and circuit level

2.2.1 Device level

There are several ways of increasing the output power of mm-wave PAs at the device level. Stacking transistors is considered a power combining effective approach at the device level. It is essentially combining transistors in series to increase the effective breakdown voltage of the transistors by sharing the supply voltage among the transistors [4]. As a result, all the voltages combine at the top-most transistor and the output power increases and Z_{opt} increases which lowers the impedance transformation ratio. Ideally, stacking more transistors increases the output power; however, there is a significant practical limit on how many transistors can be stacked. As more transistors are added, the device parasitics make the alignment of the phase of the voltages of the transistors more challenging [4]. Fig. 2.3 shows a three stacked-FET PA implemented in 45 nm CMOS-SOI. The top-most gate transistor contains a capacitor to adjust the impedance presented at the drain of each of the transistors; this process can be assisted by adding a shunt or series inductor at the source of the top-most transistors to align the drain voltages in-phase and sum at the PA output [4]. Furthermore, work in [4] implemented two, three, and four stacked-FET PAs to determine the limitation of stacking-FET and the affect on the performance in terms of output power and efficiency. Fig. 2.4(a) shows an increase of P_{-1dB} by 5 dBm for a four stacked-FET PA compared to a two stacked-FET PA. However, Fig. 2.4(b) shows a significant trade-off between peak efficiency and output power. The two stacked-FET achieved the highest peak PAE with difference ranging from 5 % to 10% compared to the three stacked-FET and four stacked-FET PA cases.

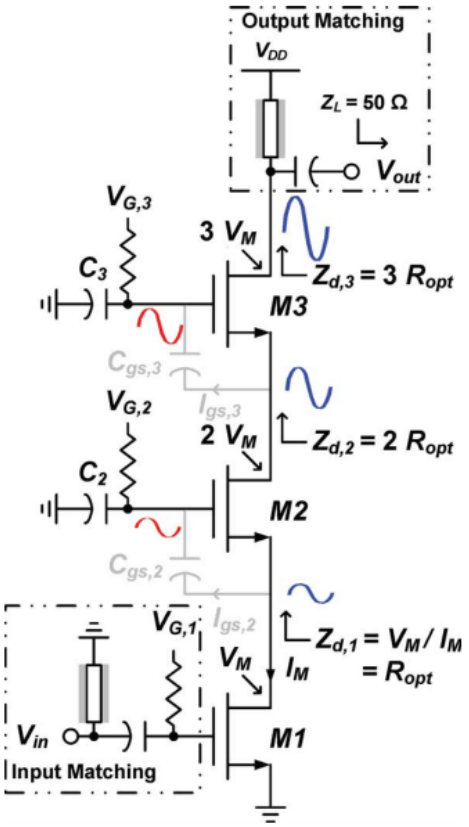

Fig. 2.3: Schematic of three-stacked-FET PA [4]

Alternatively, there is current combining method where multiple unit power cells are connected in parallel and the current from each cell is combined at the output to increase the output power of the PA [5]. Fig. 2.5 shows a two-stage two-way digital PA that is dual-band where the unit power cells are controlled digitally by 7-bit binary weighted code to dynamically suppress Amplitude-to-Amplitude (AM-AM) distortion and improve the dynamic range. Moreover, the driver stage contains two-stage varactors to adjust the RF signal phase to compensate for the Amplitude-to-Phase (AM-PM) distortion. The unit power amplifier cell is designed to operate in the class-D^{-1} mode of operation. The output combiner is designed to reject even harmonics and combine the active unit power amplifier cells. Fig. 2.6 illustrated how the RF current at odd harmonics are added in the output combiner and how the even harmonics are rejected in the output combiner.

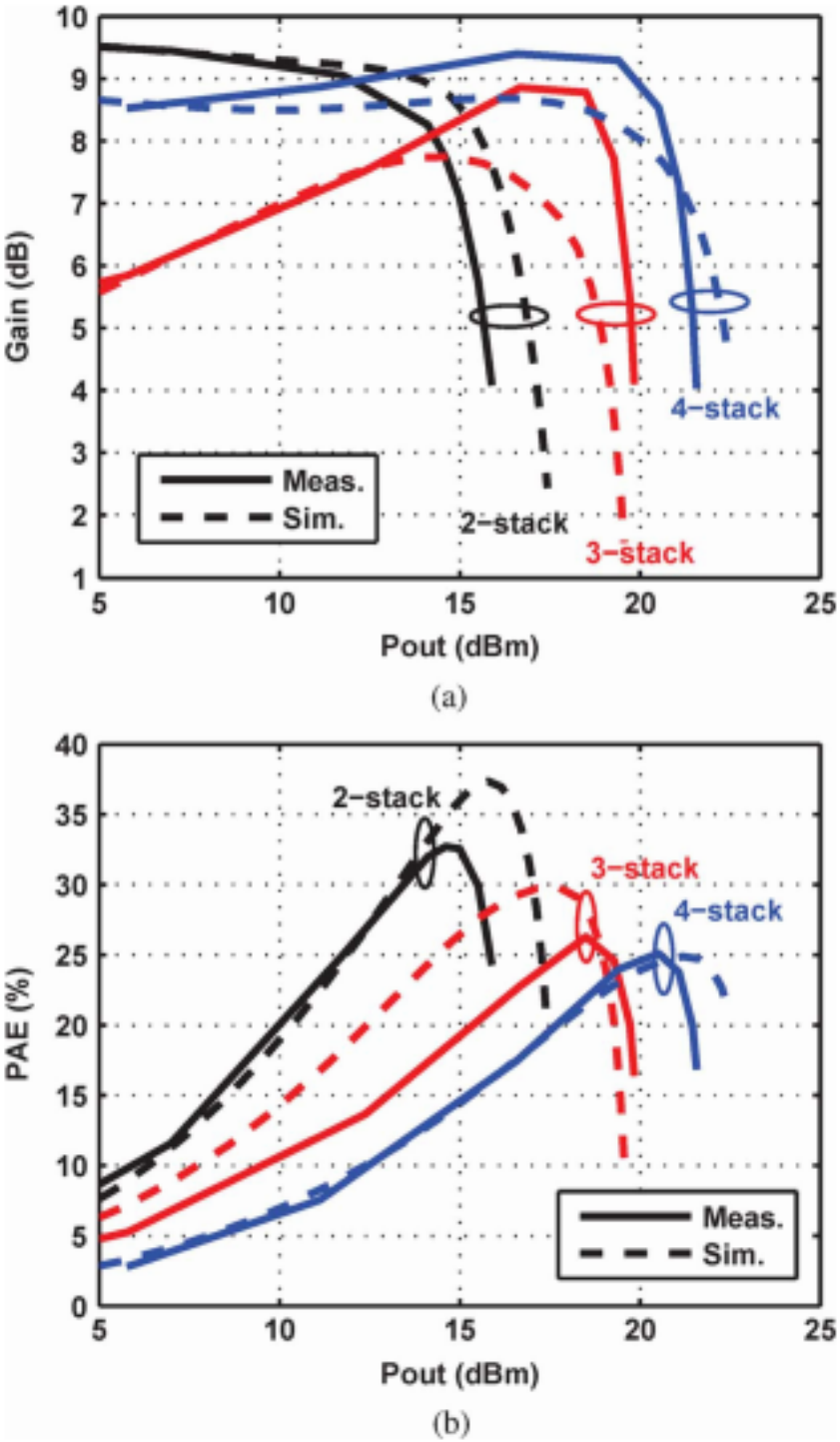

Fig. 2.4: (a) Gain versus output power for two, three, and four stacked-FET (b) PAE of two, three, and four stacked-FET [4]

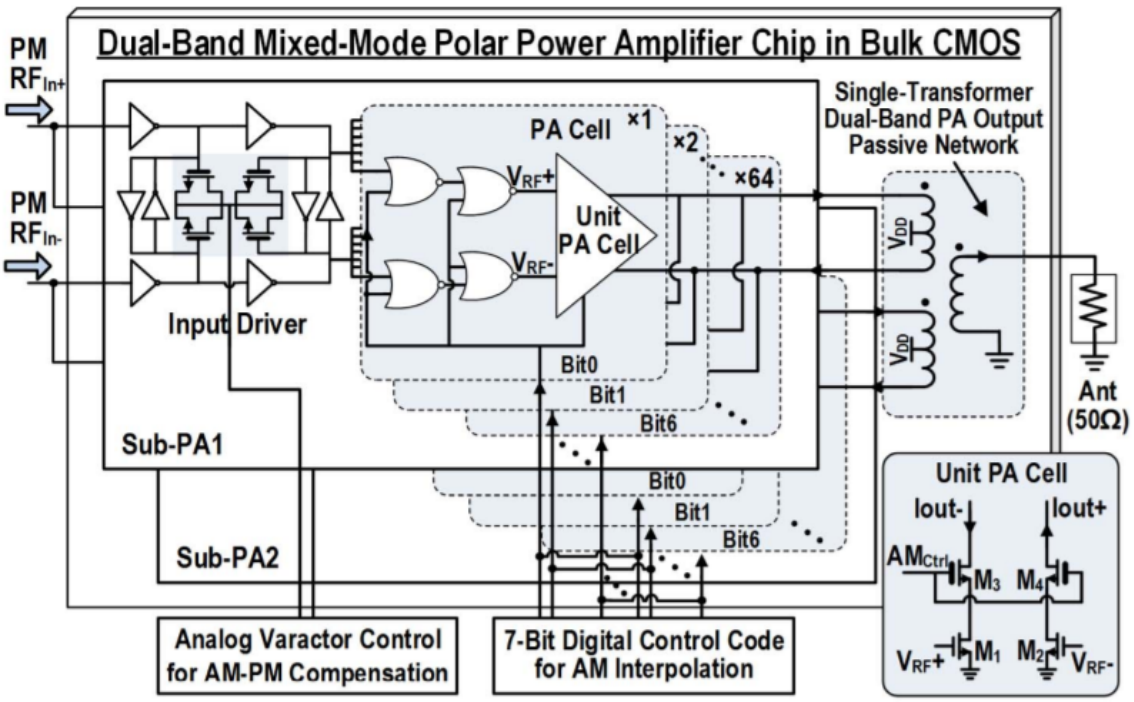

Fig. 2.5: Schematic of the digital PA [5]

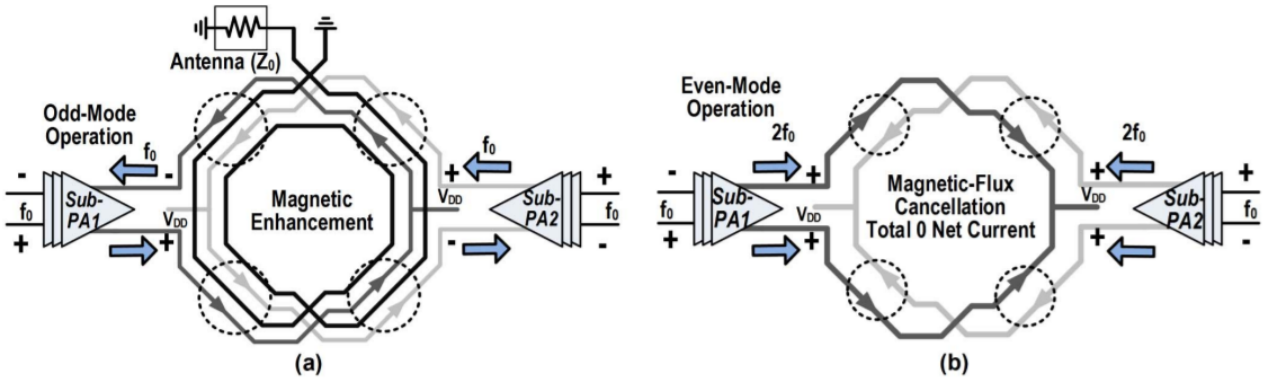

Fig. 2.6: layout of the output combiner with odd and even mode operation [5]

2.2.2 Circuit level

On-chip passive combiners are usually implemented using monolithic transformers due to their compactness, bandwidth capabilities, and offering high coupling between the two windings. Fig. 2.7 shows a simplified transformer model with N:1 turns ratio and k is the coupling factor between the two windings. The transformer model includes the primary and secondary winding

inductance, L_p and L_s, respectively. In addition, losses in the coils are represented by series resistance at the primary and secondary windings and the coupling between the primary and secondary is represented by the $C_{interwiding}$. Lastly, the parasitic capacitances and dissipation in the substrate are modelled by the shunt element C_{OX}, C_{si}, and r_{si} in each coil.

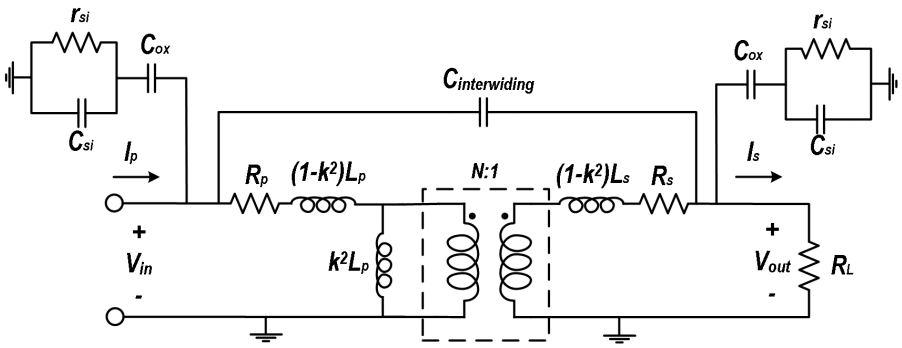

Fig. 2.7: Schematic of non-ideal transformer model [12]

In order to combine amplifier paths multiple transformers are used to combine either the voltages or currents to increase the output power of the PA. Work in [12] proposed a series combining transformer (SCT) that combines voltages at the load. Fig. 2.8 shows the equivalent circuit of SCT that contains N transformers and each transformer having a winding ratio of m. The secondary winding of each transformer carries the same current, V_{out}/R_L. When all PAs present the same output impedance, thus, the impedance seen by each transformer are determined by N and m.

$$R_m = \frac{R_{load}}{Nm^2} \tag{2.11}$$

In the literature of SCT, the distributed active transformer (DAT) and figure-8 combiner are examples of SCT combiner. Work in [13] proposed a DAT topology for the output combiner by combining the output voltages in series at the primary windings. It consists of N number of independent 1:1 transformers each with a primary winding driven by an independent PA cell while the secondary windings are connected in series. Fig. 2.9 shows how the PAs are distributed in the DAT layout. It is laid out in a circular geometry to create a low-loss low-

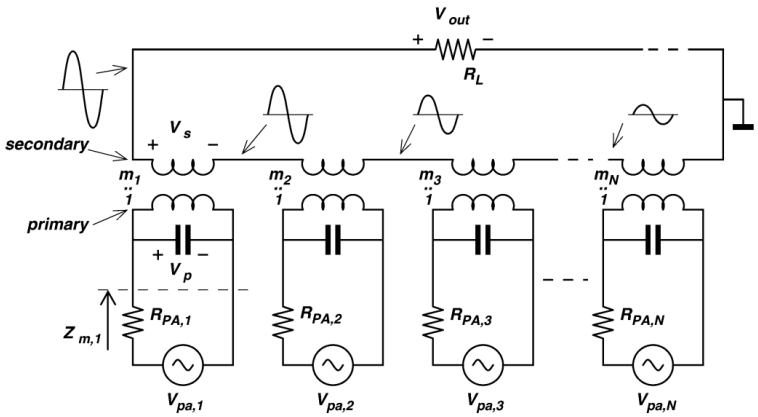

Fig. 2.8: Schematic of series-combining [12]

impedance virtual alternating-current (AC) ground. In addition, capacitors are connected to each adjacent drain of the transistors for harmonic suppression; however, this is only valid when the voltage at the drain of all transistors are identical and the transistors are driven with the proper phases. Furthermore, the input matching for each transistor uses a slab inductor to resonate out the gate capacitance. Fig. 2.9 also shows the input power distribution to the gate of the transistors at center of the DAT. A major disadvantage of this topology is that all PAs must be turned on; thus, it requires switches for the idle PAs to improve the back-off efficiency of the combining efficiency. Lastly, the supply and ground inductance can affect the DAT combiner if some PAs are idle because those PAs are not located at the virtual ground of the combiner [13]. Thus, the DAT is not suitable for DPA operation.

Figure-8 combiner consists of independent primary windings and the power combining happens at the secondary winding [14]. This enables the PAs to drive the combiner with different levels of current without the shift or loss of virtual ground. Another advantage of the figure-8 combiner is that it does not require an RF choke for the supply feed. Furthermore, the figure-8 combiner can be used to control the power dynamically or discretely. Fig. 2.10(a) shows the figure-8 combiner controlled discretely using switches and Fig.2.10(b) shows the figure-8 combiner controlled dynamically. In the discrete power control, the idle PAs are short-circuited and the associated transformer inductance at the secondary winding acts as a parasitic that

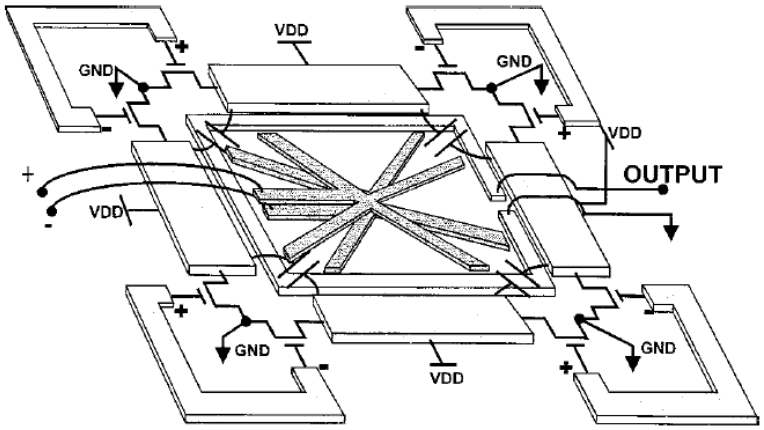

Fig. 2.9: Layout of DAT combiner [13]

can degrade the combining efficiency at back-off power levels. In addition, the resistance of the switches adds unnecessary losses to the combiner. In dynamic power control, the idle PA sees an output impedance that can be represented by an output capacitance. The output capacitance of the non-working PA can degrade the combining efficiency and should by minimized.

Work in [14] proposed a hybrid transformer that combines two DATs in a figure-8 manner. The hybrid transformer is a compromise between the high combining efficiency of DAT and the flexibility of the figure-8 combiner. The hybrid transformer contains both dynamic and discrete power control. The hybrid transformer demonstrated back-off efficiency enhancement in the combining efficiency because most of the current from the working PAs at back-off level are in the larger portion of the transformer that are being used. Furthermore, the idle PAs are located at the virtual ground and the parasitic capacitance associated with them has no affect on the combining efficiency. Hence, the only source of degradation at back-off levels is due to the switches that are located at the output of the idle PAs and the supply inductances that are not located at the virtual ground in the back-off levels. Furthermore, the DAT and figure-8 combiner suffers from impedance imbalances and affects the impedance matching within the push-pull PAs and can generate a common-mode current which can degrade the linearity and efficiency. This is primarily due to inter-winding capacitance and the capacitances to the substrate within

the push-pull PAs encounter different voltages. In contrast, the hybrid transformer does not suffer from impedance imbalances because the PAs are laid out across the symmetry plane and the symmetry is maintained even at back-off level as shown in Fig. 2.11; as a result, all of the parasitic capacitances encounter the same voltage.

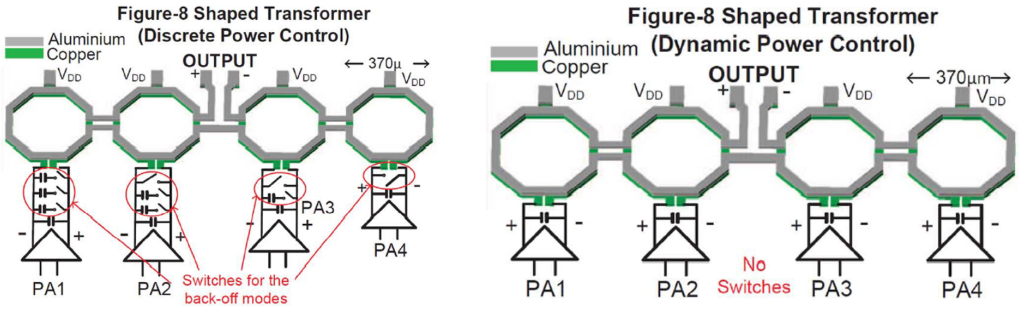

Fig. 2.10: Layout of figure 8 combiner for discrete and dynamic power control [14]

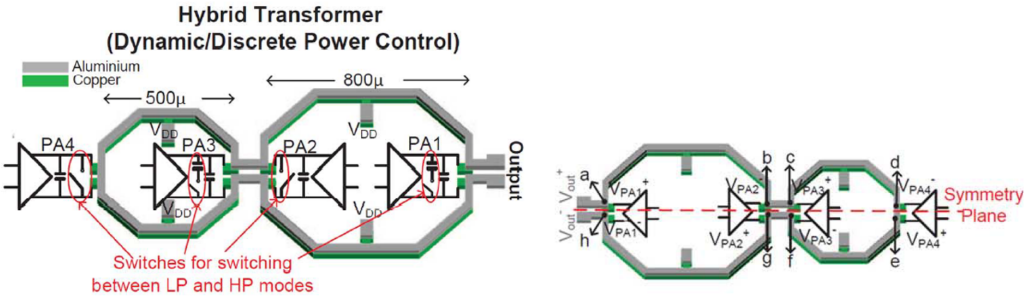

Fig. 2.11: Layout of hybrid transformer combiner using dynamic and discrete power control [14]

Another way of amplifying more than one PA path is using parallel combining transformer (PCT) where each primary winding is coupled to the secondary winding. In other words, the PCT is a form of current combining from all primary windings and induces a current at the secondary winding. The impedance transformation ratio ($n = Nm^2$) increases with the number of transformers combined [12]. Hence, it requires the secondary winding to have more than one turns ratio to match to the optimum impedance of the PAs, which is difficult to realize at mm-wave frequencies. Fig. 2.12 shows the equivalent circuit for the PCT combiner.

Zhao [15] proposed a PCT combiner where it combines four PAs at the primary winding and induces a current in the secondary winding as shown in Fig. 2.13. Moreover, the secondary

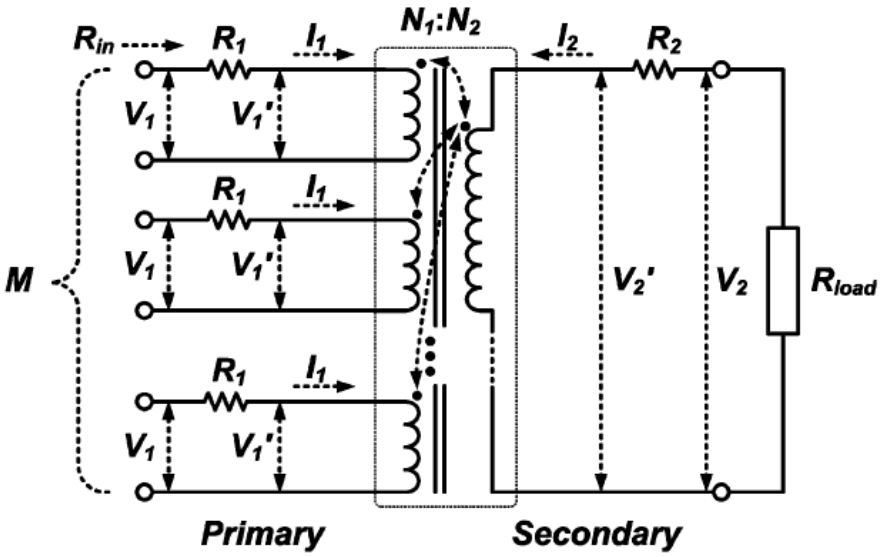

Fig. 2.12: Schematic of parallel-combining [12]

incorporates a lateral compensation that is a dummy turn metal to reduce the effect of the inter-winding capacitance, which causes impedance imbalances to each PA. It replicates the voltage swing seen at the RF output; thus, equalizing the electric coupling across the interwinding capacitance.

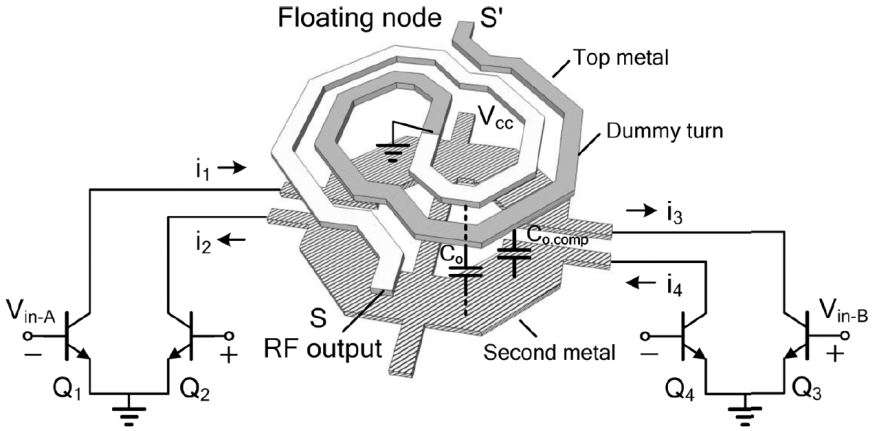

Fig. 2.13: Layout of the proposed parallel-combining with lateral compensation [15]

2.3 Efficiency Enhancement Techniques of PA

When linear PA is driven with complex modulated signals that exhibit a high PAPR, it forces the PA to operate below peak output power; hence, the efficiency of the PA is degraded. The are two techniques of enhancing the efficiency of the PA at back-off power levels namely supply and load modulation. The supply modulation technique adjusts the supply voltage of the PA as a function of the input power to reduce the DC power consumption at back-off power levels. Envelope tracking (ET) technique utilizes a linear PA where the supply voltage is modulated based on the envelope of the RF input signal to maintain a high efficiency at back-off power levels [16]. Furthermore, envelope elimination and restoration (EER) uses a high efficiency non-linear PAs with a linear envelope amplifier to achieve linear amplification with high efficiency at back-off levels [17]. On the other hand, load modulation involves modulating the load of active device based on the input power to enhance the back-off efficiency. The Doherty technique is based on the load modulation technique.

The previous section focused on increasing the output power and peak efficiency of mm-wave PAs. However, little attention has been given to enhancing the efficiency at back-off levels. Despite its popularity for use at sub-6 GHz frequencies, the Doherty technique has attracted limited attention for use at mm-wave frequencies. This section will provide an overview on the Doherty technique and a conducted literature review on mm-wave DPA.

2.3.1 Doherty Amplifier Technique

Fig. 2.14 shows the schematic of the conventional DPA. The Doherty technique is an active load-pull technique that is used to enhance the efficiency of the PA at back-off power levels when the PA is amplifying a signal that exhibits high PAPR as shown in Fig. 2.15. It maintains the peak efficiency of the PA from a back-off power level (i.e. 6, 9, 12 dB back-off) to the peak

power. The introduction of another transistor is considered as the active load-pulling, so called peaking transistor, to modulate the impedance seen by the main transistor. The main and peaking PAs are biased as class-B and class-C, respectively.

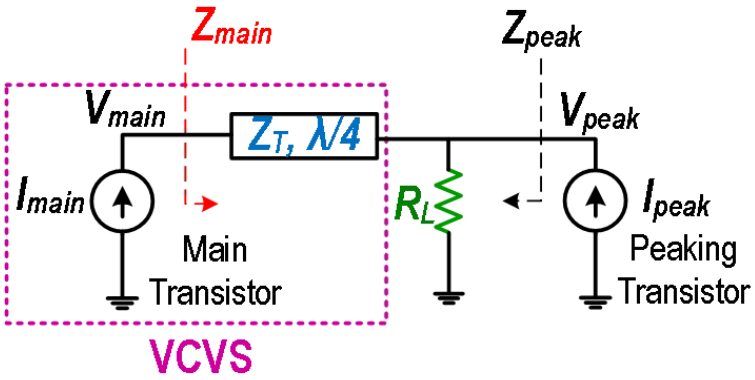

Fig. 2.14: Schematic of conventional DPA

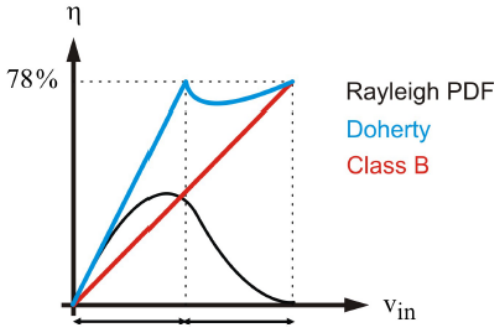

Fig. 2.15: Efficiency and Probability Density Function versus input voltage [11]

The impedance seen by the main transistor and the peaking transistor are the following,

$$Z_m = \frac{V_m}{I_m} = Z_T\{\frac{Z_T}{R_L} - \frac{I_p}{I_m}\} \tag{2.12}$$

$$Z_p = \frac{V_p}{I_p} = Z_T\{\frac{I_m}{I_p}\} \tag{2.13}$$

Where Z_T and R_L are,

$$Z_T = R_{opt} \tag{2.14}$$

$$R_L = \frac{R_{opt}}{2} \tag{2.15}$$

Thus, Z_m when I_p=0 is,

$$Z_m = 2R_{opt} \tag{2.16}$$

$$R_L = \frac{R_{opt}}{2} \tag{2.17}$$

When I_p=I_m,

$$Z_m = R_{opt} \tag{2.18}$$

$$Z_p = R_{opt} \tag{2.19}$$

The drain voltage and current profiles of the main and peaking transistors are shown in Fig. 2.16 (a) and (b). The peaking current starts to turn on at half the maximum input voltage and that is when the voltage of the main transistor saturates. At 6 dB back-off, the main transistor is operating with maximum efficiency. When the peaking is injecting current into the load, the impedance seen by the main transistor starts to reduce. When $I_p = I_m$, the impedance of the main transistor reduces from $2R_{opt}$ to R_{opt} and the impedance seen by the peaking transistor reduces from open-circuit to R_{opt}. Fig. 2.17 shows the load modulation of the main and peaking transistor.

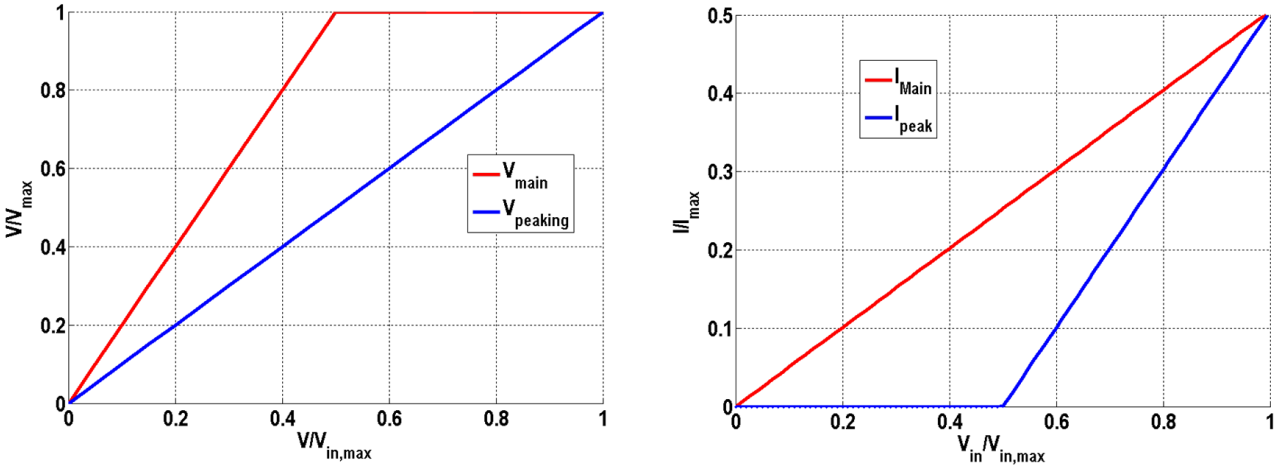

Fig. 2.16: Voltage and current profiles for Doherty Technique

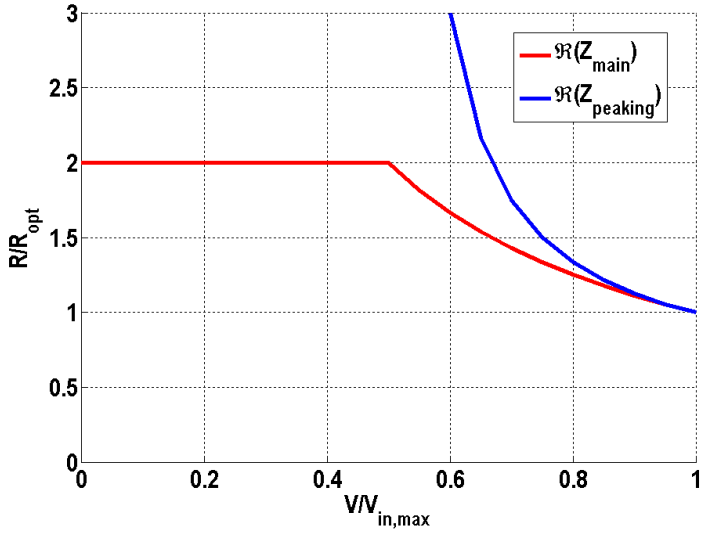

Fig. 2.17: Load modulation of the main and peaking impedance

2.3.2 Literature Review of mm-Wave DPA

There are two major challenges in the implementation of DPA at mm-wave frequencies. First, the implementation of the $\lambda/4$ impedance inverter using a conventional transmission line-based introduces significant losses to the output combiner due to the low-quality factor of passives on lossy silicon substrates [18]. Secondly, the low gain of the class-C biased peaking transistor imposes constraints on mm-wave DPAs using silicon technologies. There are several common

solutions applied in sub-6 GHz designs, such as oversizing the peaking transistor so the current of the peaking transistor reaches the main transistor's current at peak power or using an uneven power splitting ratios at the input of the DPA to provide more gain to the peaking PA. These solutions result in excessive parasitic capacitance, unsatisfactorily low overall gain of the DPA, or lower bandwidth.

One way to implement the Doherty output power combiner output combiner with compactness and lower the losses on silicon substrates is transformer-based combiner methods. In [18], a 72 GHz Doherty PA combiner was implemented using a parallel-series combiner transformer-based on a 40 nm CMOS technology as shown in Fig. 2.18. In addition, transistor stacking was used to increase the output power of the main and peaking PAs. The combiner showed an average combining efficiency of 74 %; however, sub-optimum load modulation was achieved as illustrated in Fig. 2.19.

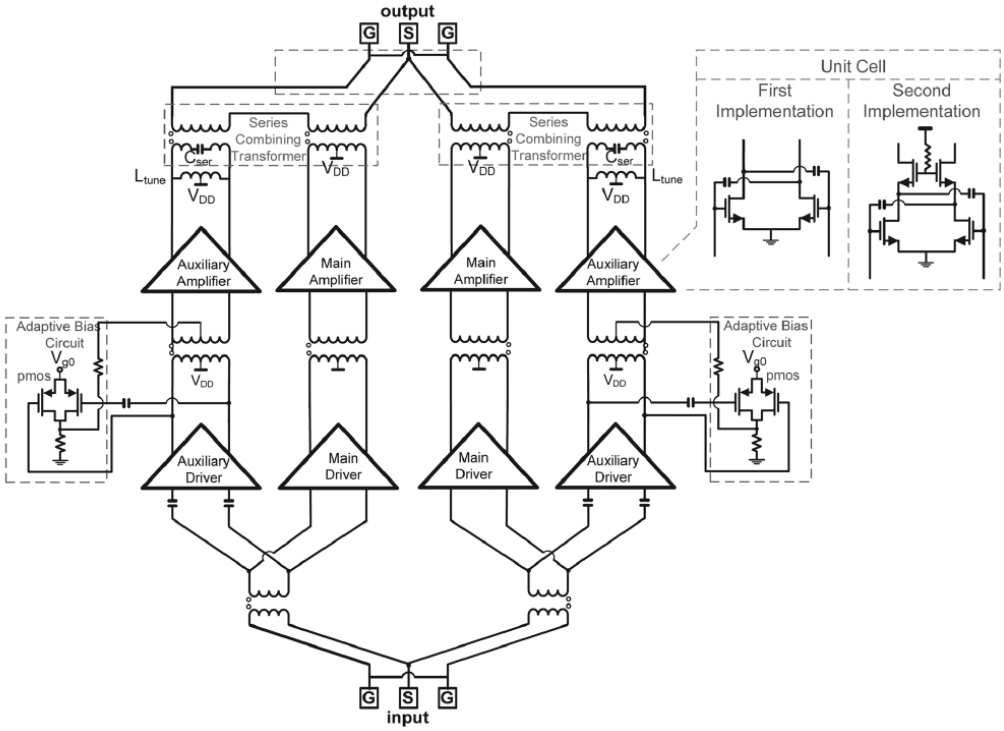

Fig. 2.18: Schematic of the series-parallel transformer-based Doherty PA with adaptive biasing at E-band [18]

In [19], implemented a multi-band 28/37/39 GHz DPA using a 130 nm SiGe process. The

output combiner is a transformer-based parallel combiner that carefully absorbs the transistor parasitics. In addition, the output combiner consists of an additional capacitve-based matching network to achieve the required operation of the DPA. However, the load modulation was only demonstrated at 39 GHz. In [20], a 32 GHz DPA transformer-based combiner was implemented using 28 nm CMOS as shown in Fig.2.21. The output combiner combines two DPA in parallel where each of the DPA contains two main and peaking PAs that are combined in parallel and then combined in series to achieve a high output power ($>$ 20 dBm) and this method reduces the impedance transformation ratio from the load to the unit power cells. However, the DPA achieved a peak PAE at more than 5 dB compression compromising the linearity and adding two more stages to the output combiner can potentially reduce the combining efficiency.

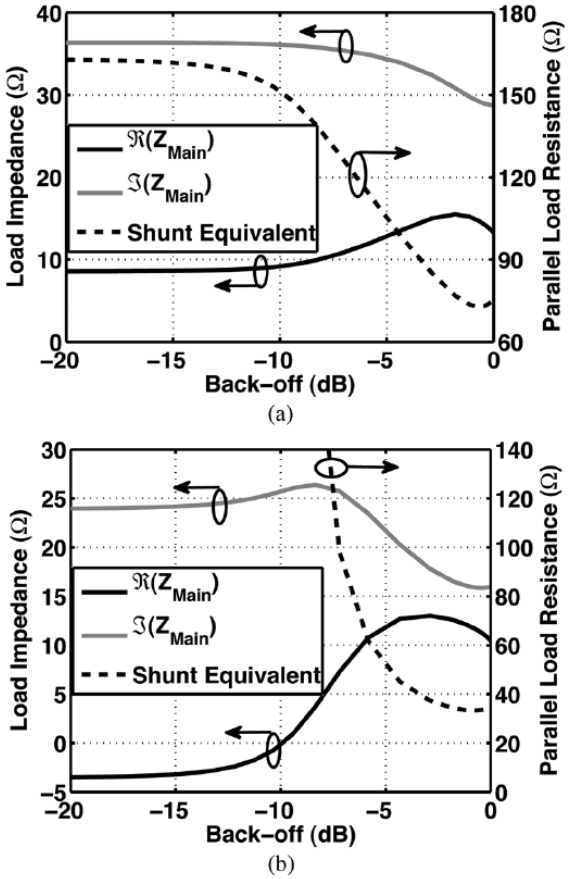

Fig. 2.19: Load modulation of the (a) main and (b) peaking impedances for Doherty PA at E-band [18]

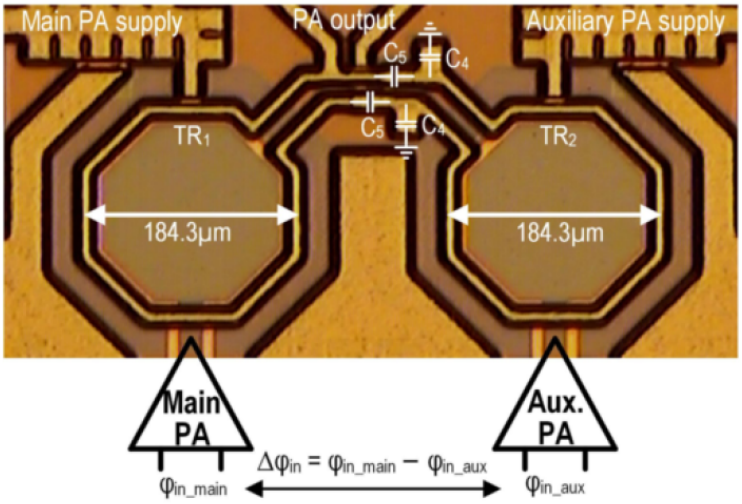

Fig. 2.20: Layout of Parallel Doherty PA at 28/37/39 GHz with the additional capacitive network [19]

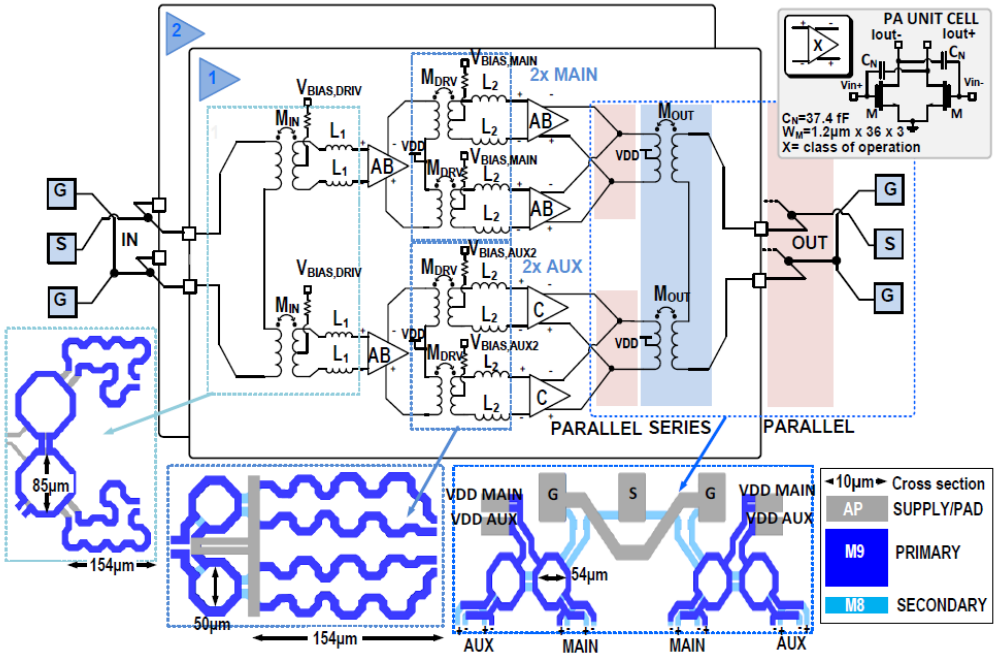

Fig. 2.21: Schematic of the parallel-series-parallel Doherty PA at 32 GHz [20]

Adaptive gate biasing of the peaking transistor has been utilized to mitigate the issue regarding the class-C biased peaking transistor. Authors in [7]-[8], applied adaptive gate biasing on the peaking transistor to adjust the biasing based on the input power to minimize the DC consumption at low input power and operate the peaking transistor as a class-AB at peak

power. Fig. 2.22 shows the adaptive biased DPA schematic of [7]. However, the additional broadband supply modulator creates a major overhead. To minimize this drawback, authors in [9] added dual-vector rotators to maintain the amplitude and phase balance between the two RF input signals to the DPA versus frequency and to maximize the back-off efficiency as shown in Fig. 2.23. Authors in [20], proposed an AM-PM compensation method to linearize the DPA that is based on the vector addition of the main and peaking current. This is accomplished by biasing the main and peaking transistor at a point where the main transistor's gain compression is counteracted by the peaking transistor's gain expansion. Table 2.2 compares the state-of-the-art mm-wave DPAs.

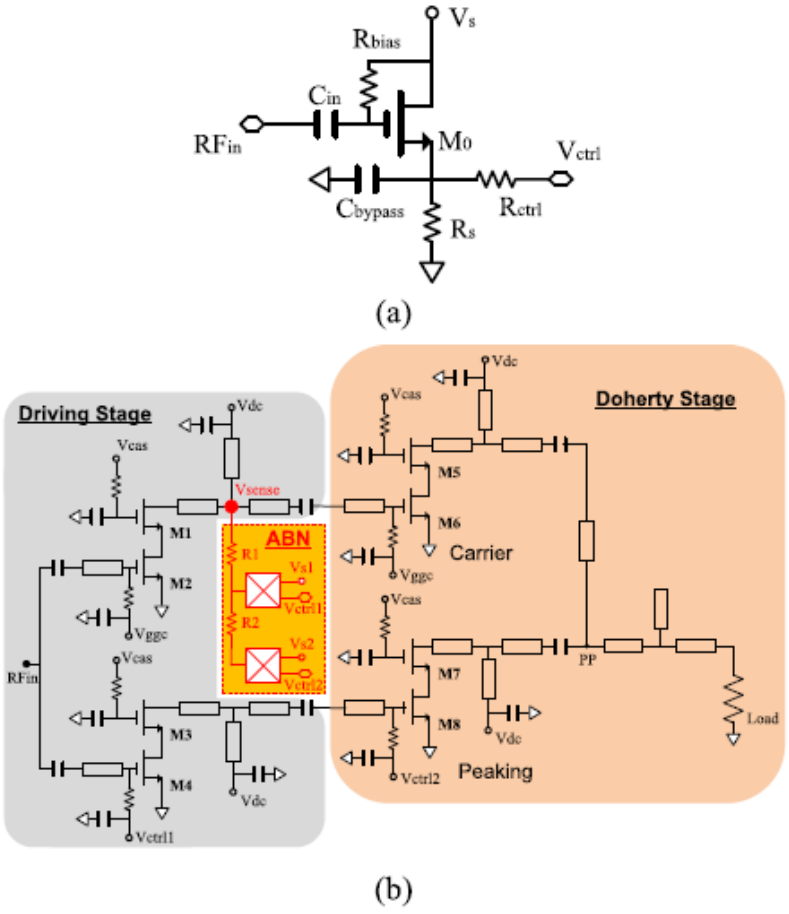

Fig. 2.22: (a) Adaptive biasing circuit used at 60 GHz (b)Schematic of the Doherty PA at 60 GHz [7]

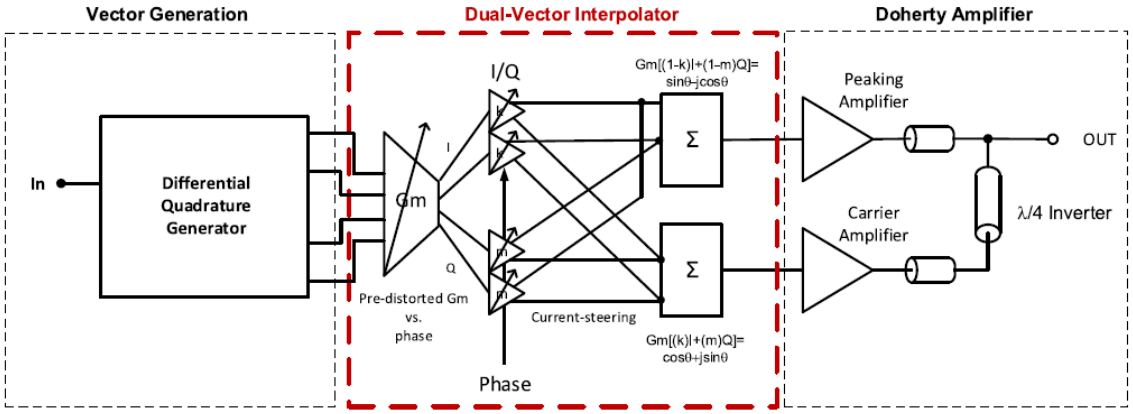

Fig. 2.23: Schematic of Dual-vector Doherty beamformer [9]

Table 2.2: Comparison of mm-Wave DPAs

FoM	[8]	[18]	[19]	[20]	[7]	[9]
Technology	45 nm CMOS SOI	40 nm CMOS	130 nm SiGe	28 nm CMOS	65 nm CMOS	130 nm SiGe
Output Combiner Topology	Transmission-Line	Transformer-Based Parallel-Series	Transformer-Based Parallel	Transformer-Based Parallel-Series-Parallel	Transmission-Line	Transmission-Line
Frequency(GHz)	42	72	28/37/39	32	60	62
Gain(dB)	8	18.5	17	22*	−−	19
BW_{-3dB}(GHz)	−−	10	16.4	4*	−−	10*
OP_{1dB}(dBm)	17*	19.2	15.4	16	−−	17.1
P_{sat}(dBm)	19	21	17	19.8	−−	17.1
PAE_{P1dB} (%)	19	12.4	20.7	12.8	17**	23.7
PAE_{6dBBO} (%)	19	7	12.6	5*	8**	13
Adaptive Gate Biasing	Yes	Yes	No	No	Yes	No

In conclusion, this chapter introduced background information regarding PAs and the classes of operation and the importance of efficiency enhancement of PA at back-off power levels.

Moreover, a literature review is conducted on the power combining techniques that are used at mm-wave frequencies at the device and circuit levels. At the device and circuit level, voltage or current combining can be utilized to increase output power of the PA. The pros and cons of each type of power combining technique are discussed. Moreover, this chapter discusses the Doherty technique as an efficiency enhancement technique. The limitations that are encountered at mm-wave frequencies are discussed and the solutions that are used to counteract those limitations. A literature review is conducted on the existing work of the DPA at mm-wave frequencies.

Chapter 3

Theory of Series-Connected Load DPA

In this chapter, the theory of the SCL DPA will be presented. The load and the $\lambda/4$ impedance inverter in Fig. 3.1b are replaced by two transformers in series connection. The $ABCD$ parameters of the output combiner will derived to achieve the SCL DPA operation. In addition, a design methodology will be proposed for designing the output combiner of the SCL using the $ABCD$ parameters and the transistors characteristics. Lastly, the formulated equations of the output combiner will be used to validate the SCL DPA theory by using ideal lumped components.

3.1 Series-Connected Load DPA

The placment of the $\lambda/4$ impedance inverter in the peaking path, in Fig. 3.1b, pinpoints several advantages to the silicon-based mm-wave DPA as opposed to the conventioal topology shown in Fig. 3.1a. First, as the efficiency in back-off region and bandwidth of the DPA are mainly dictated by the main amplifier. Therefore, eliminating the lossy $\lambda/4$ impedance inverter from that path is very beneficial due to the following. First, the $\lambda/4$ impedance inverter in

the peaking path can be utilized to absorb its transistor's large parasitics compared to the main's transistor and to mitigate the current leakage in the back-off region without deploying an explicit matching network [18]. Secondly, the load impedance, R_L is four times higher in the SCL DPA topology than in the conventional topology, which eases its transformation to 50 Ω.

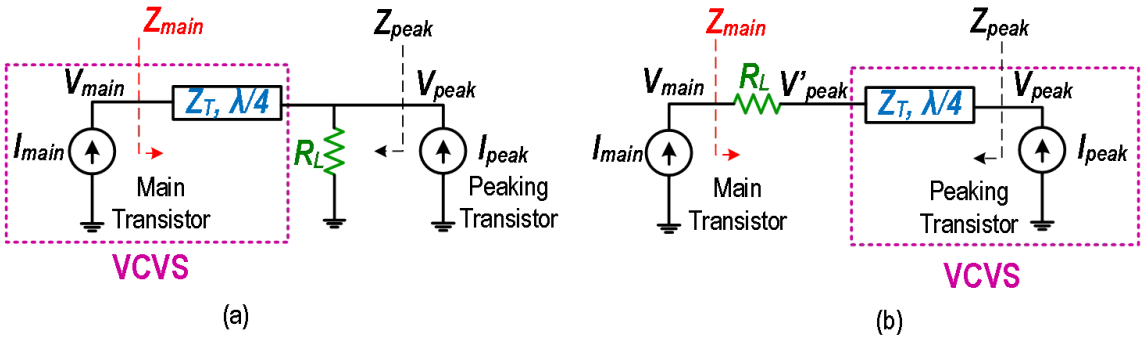

Fig. 3.1: (a) Conventional and (b) Series-Connected Load Doherty PAs

At low-power (LP) levels, the peaking transistor is off and the voltage at the output of $\lambda/4$ impedance inverter, V_p', is zero, assuming infinite output impedance for peaking transistor. Thus, the voltage of the main transistor,

$$V_m = R_L \cdot I_m \tag{3.1}$$

Hence, to maximize the efficiency in back-off R_L must be set to be equal to

$$R_L = \alpha R_{opt} \tag{3.2}$$

where α represent the back-off level at which the second efficiency peak will occur. For instance, $\alpha = 2$ indicates 6-dB back-off DPA. At high-power levels, as the peaking transistor embarks, V_p' starts to increase and lowers the impedance Z_{main} seen by the main transistor which is govern by the following equation

$$Z_{main} = \frac{V_m}{I_m} = R_L - Z_T \frac{I_p}{I_m} \tag{3.3}$$

Where Z_T is the characteristic impedance of the $\lambda/4$ impedance inverter and I_m, I_p are the output current swing at main and peaking transistors, respectively. In addition, the peaking transistor sees an impedance Z_{peak},

$$Z_{peak} = Z_T \frac{I_m}{I_p} \tag{3.4}$$

Thus, assuming ideal current profiles of the main and peaking transistors shown in Fig. 3.2a to achieve proper load modulation profile shown in Fig. 3.2b, the characteristic impedance of the $\lambda/4$ impedance inverter, Z_T , must be,

$$Z_T = R_{opt} \tag{3.5}$$

Fig. 3.2c depicts the voltages profiles V_m and V_p' using (3.2) and (3.5) and Fig. 3.2d confirms efficiency enhancement similar to the one achieved using conventional DPA.

In addition, asymmetrical supply voltages can be added into the SCL DPA theory. Incorporating asymmetrical supply voltages into PAs that use low power silicon technologies such as CMOS is beneficial because biasing the transistor in Class-C operation exhibits low gain at mm-wave frequencies. This relaxes the requirement on the current profile and the output current of the peaking transistor can be lower than the current of the main transistor at peak power. The difference in magnitude between the currents at peak power is the ratio of the drain voltage of the peaking to the drain voltage of the main. This increases the impedance seen by the peaking transistor and changes the required characteristic impedance of the $\lambda/4$ impedance inverter as shown in the following,

$$\frac{I_m}{I_p} = \frac{V_{DDp}}{V_{DDm}} = \sigma \tag{3.6}$$

$$Z_{peak} = \sigma^2 R_{opt} \tag{3.7}$$

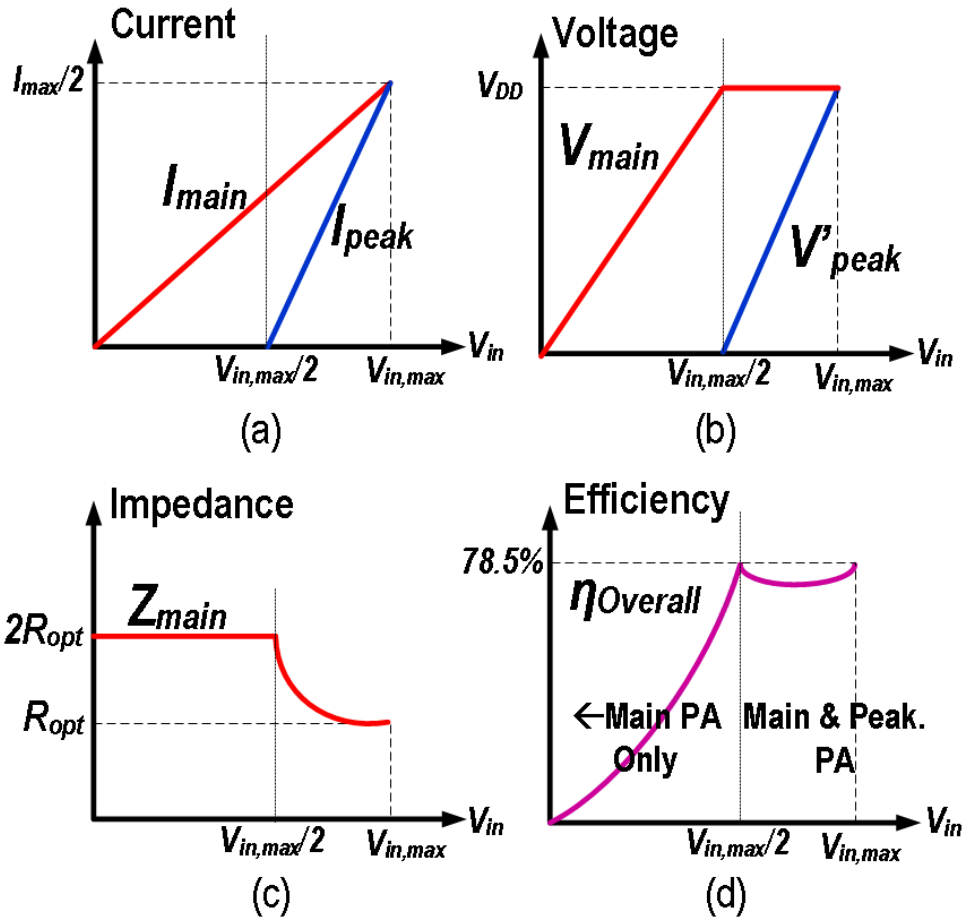

Fig. 3.2: Ideal (a) current (b) impedance (c) voltage and (d) efficiency profiles of the DPA

$$Z_T = \sigma R_{opt} \tag{3.8}$$

Fig. 3.3a depicts an SCL Doherty circuit where the series-connected load R_L is replaced by an ideal transformer with a turn ratio, n, and a load, R_o, in the transformers secondary winding. In addition, the impedance transformation ratio is m, which is R_L to R_o. The equivalent $ABCD$ matrices corresponding to the main and peaking combiner are given

$$\begin{pmatrix} A_m & B_m \\ C_m & D_m \end{pmatrix} = \begin{pmatrix} m & 0 \\ 0 & 1/m \end{pmatrix} \tag{3.9}$$

$$\begin{pmatrix} A_p & B_p \\ C_p & D_p \end{pmatrix} = \begin{pmatrix} 0 & jZ_T \\ j/Z_T & 0 \end{pmatrix} \tag{3.10}$$

Also, Fig. 3.3b shows the proposed SCL Doherty PA combiner network where the ideal transformer and $\lambda/4$ impedance inverter of Fig. 3.3a are replaced with non-ideal transformer models that includes the leakage and magnetization inductances. Furthermore, it incorporates the parasitic drain-to-source capacitances of the two transistors, C_m and C_p. To avoid the performance degradation associated with C_m and C_p, two additional capacitors, C'_m and C'_p, were added to the secondary windings of the two transformers. C'_m resonates with inductances of the main's transformer to provide a real-to-real impedance transformation and the addition of C'_p to the peaking transformer provides the 90° phase shift. Implementing the output combiner as a two transformer combiner is more area efficient than a single transformer with $\lambda/4$ transmission line based because when transformers are driven differentially it can provide higher effective inductances due to the mutual coupling of the coils.

3.2 Formulation of the ABCD parameters

Fig. 3.4 shows the main and peaking non-ideal transformer models that consists of leakage inductance and magnetization inductances, L_a and L_b, respectively. The leakage inductance is modeled as $(1 - k^2)L$ and the magnetization inductance is modeled as k^2L. In addition, the series and shunt capacitor that are added at port 2 are to resonate out C_m and C_p to provide real-to-real impedance transformation for both transformers. Also, the shunt capacitor along with the peaking transformer will provide the 90° phase shift that is required from the $\lambda/4$ impedance inverter. The values of C'_m and C'_p can be obtained by formulating the $ABCD$ parameters of the main and peaking transformers separately.

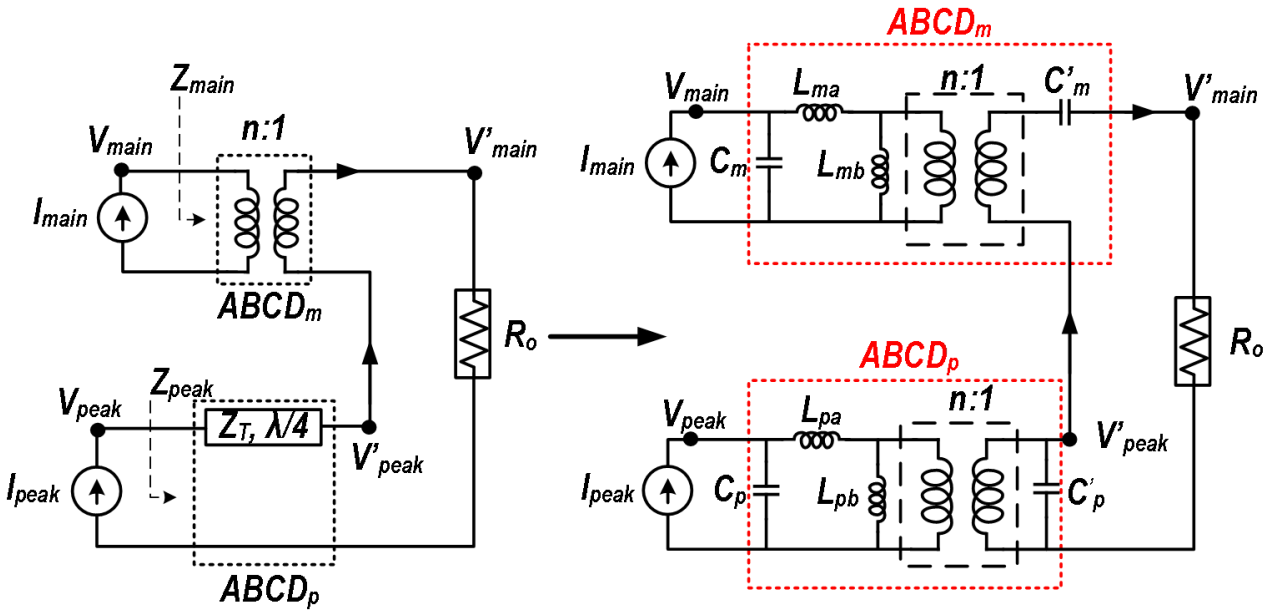

Fig. 3.3: (a) SCL Doherty PA and (b) the proposed transformer-based realization of output combiner for SCL Doherty PA

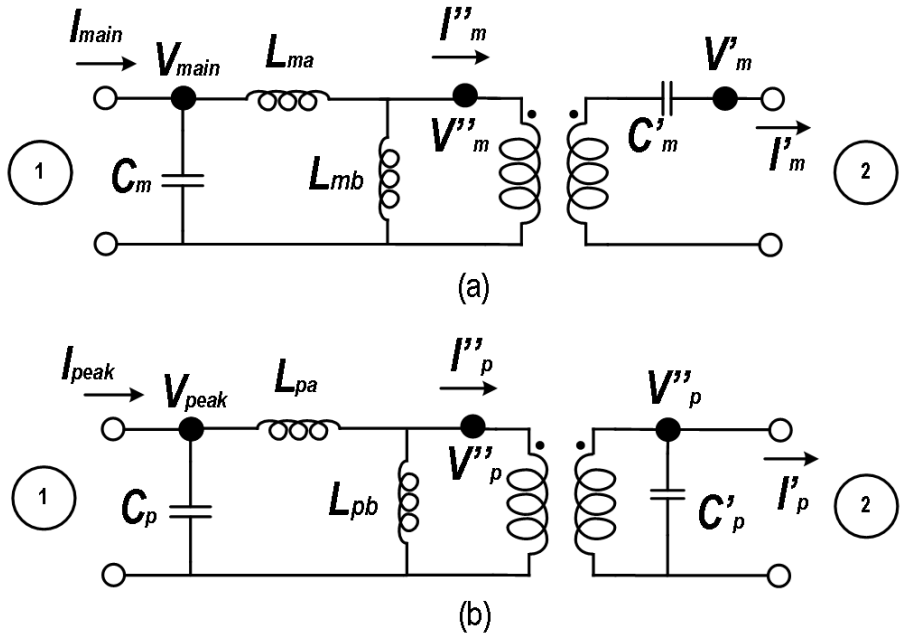

Fig. 3.4: (a) Transformer of the main PA with series capacitor and (b) transformer of the peaking PA with shunt capacitor

Fig. 3.4a shows the main transformer with the series capacitor at port 2. The parameter A^m of the $ABCD$ matrix of the main transformer is defined as the voltage ratio V_m/V'_m when

the port 2 is open circuit (I'_m =0). As shown in (3.11) and (3.12), the voltage ratio is simply the impedance transformation ratio, m.

$$V''_m = V_m \frac{j\omega_o L_{mb}}{j\omega_o (L_{mb} + L_{ma})} \tag{3.11}$$

$$A^m = \frac{V_m}{V'_m} = \frac{n'(L_{mb} + L_{ma})}{L_{mb}} = \frac{n'(k^2 L_m + (1-k^2)L_m)}{k^2 L_m} = \frac{n'}{k^2} = \frac{n}{k} = \frac{1}{k}\sqrt{\frac{L_m}{L_2}} = m \tag{3.12}$$

The parameter C^m is defined as the I_m/V'_m when port 2 is open circuit. L_m can be determined to resonate with C_m at a certain frequency as shown in (3.14). Lastly, the parameter B^m is defined as the ratio V_m/I'_m when port 2 is short circuit (V'_m= 0) and C'_m can be reflected back to primary side of the main transformer as C'_m/n'^2 to resonate with the magnetization inductances as shown in (3.16).

$$C^m = \frac{I_m}{V'_m} = \frac{n'}{j\omega_o L_{mb}}(1 - \omega_o^2 L_m C_m) = 0 \tag{3.13}$$

$$L_m = \frac{1}{\omega_o^2 C_m} \tag{3.14}$$

$$B^m = \frac{V_m}{I'_m} = n'\{\frac{1}{j\omega_o C'_m} + \frac{L_{ma}}{C'_m[j\omega_o L_{mb} \| \frac{n'^2}{j\omega_o C'_m}]}\} \tag{3.15}$$

$$C'_m = \frac{n'^2}{\omega_o^2 L_m k^2 (1-k^2)} \tag{3.16}$$

Fig. 3.4b shows the peaking transformer with the shunt capacitor at port 2. The parameter

D^p of the $ABCD$ matrix of peaking transformer is defined as the ratio of I_p/I'_p when port 2 is short circuit. Thus, the inductor size, L_p, needed to resonate out parasitic capacitance of the peaking transistor can be determined as illustrated in (3.18). Furthermore, the parameter A_p is defined as the voltage ratio V_p/V'_p when port 2 is open circuit and that helps in finding the required shunt capacitor, C'_p, to with L_p. (3.22) shows how to determine the required shunt capacitor at port 2.

$$\frac{I''_p}{I_p} = \frac{1}{n'^2} \frac{\frac{1}{j\omega_o C_p}}{\frac{1}{j\omega_o C_p} + j\omega_o L_{pa}} \tag{3.17}$$

$$D^p = 1 - \omega_o^2 C_p L_{pa} = 0 \tag{3.18}$$

$$L_p = \frac{1}{\omega_o^2 C_p (1 - k^2)} \tag{3.19}$$

$$A^p = \frac{V_p}{V'_p} = \frac{Z + j\omega_o L_{pa}}{Z} = 0 \tag{3.20}$$

where,

$$Z = \frac{j\omega_o L_{pb}}{1 - \omega_o^2 L_{pb} \frac{C'_p}{n'^2}} \tag{3.21}$$

$$C'_p = \frac{n'^2}{\omega_o^2 L_p k^2 (1 - k^2)} \tag{3.22}$$

Lastly, the parameter B^P is defined as the ratio of V_p/I'_p when V'_p =0 and is also defined as the characteristic impedance of the $\lambda/4$ impedance inverter. (3.23) Shows the derivation of the characteristic impedance of the $\lambda/4$ impedance inverter.

$$B^p = \frac{V_p}{I'_p} = \frac{j\omega_o L_{pa}}{n'} = \frac{j\omega_o(1-k^2)L_p}{n'} = jZ_T \tag{3.23}$$

3.3 Design Methodology

The proposed design methodology aims to improve back-off efficiency of the main amplifier by reducing the current leakage that is in the peaking path and improving the combining efficiency of the output combiner at back-off region. At high power levels, the output combiner efficiency must also be efficient to maximize the efficiency at peak power. There are four unknowns in the output combiner namely L_m, C'_m, L_p, and C'_p. The proposed design methodology of determining the unknowns of the output combiner is summarized in the following steps:

Step 1: Select the transistor size such that the R_{opt} of the transistor is close to R_o.

Step 2: Determine the R_{opt} of the main and peaking amplifiers through load-pull simulation.

Step 3: Determine the output capacitance of the main and peaking amplifiers.

Step 4: Determine the required inductor, L_m, in order to resonate out C_m at the center frequency through (3.14).

Step 5: The required impedance seen by the main amplifier at back-off region is $2R_{opt,m}$. The impedance transformation ratio, m, can be calculated through the following

$$m = \sqrt{\frac{2R_{opt,m}}{R_o}} = \frac{1}{k}\sqrt{\frac{L_m}{L_2}} \tag{3.24}$$

Step 6: Estimate a reasonable coupling factor given the back-end of the technology kit and determine the inductance of the secondary winding of the output combiner.

Step 7: Select the desired turn ratio of the main transformer, n', and determine the series capacitor, C'_m through (3.16).

Step 8: At peak power, the desired impedance seen by the peaking amplifier is $R_{opt,p}$. The characteristic impedance of the $\lambda/4$ impedance inverter can be calculated using the following

$$Z_T = \sqrt{R_{opt,p} R_L} \tag{3.25}$$

Step 9: Using (3.22), select a turn ratio for the peaking transformer and estimate a reasonable coupling factor to determine L_p that provide the calculated Z_T.

Step 10: Determine the required capacitor seen by the peaking transistor by using (3.17).

Step 11: Using (3.21), determine C'_p to resonate with the peaking transformer at center frequency.

To conclude, this section proposes a DPA topology to improve the back-off region efficiency by placing the lossy $\lambda/4$ impedance inverter in the peaking path rather than the conventional topology. In addition, the $\lambda/4$ impedance inverter can be utilized to absorb the parasitics of the peaking transistor and minimize the current leakage that is drawn by the peaking transistor in the back-off region. Furthermore, the circuit in Fig. 3.2 is replaced with an output combiner that is transformer-based and it consists of additional matching network, namely, C'_m and C'_p, in order to fulfil the required $ABCD$ matrix for each transformer. Deriving the $ABCD$ parameters for each transformer can determine C'_m, C'_p, L_m, and L_p. Lastly, a design methodology is proposed on how to design the output combiner of the SCL DPA given the transistor's optimum impedance and output capacitance. The design methodology gives a good starting point for optimization at the schematic level.

3.4 Simulation with Ideal Lumped Components

This section applies the formulated equations in the previous section and simulates the main and peaking transformers with ideal lumped components to prove that the *ABCD* matrices satisfies (3.9) and (3.10). In addition, the ideal main and peaking transformers is combined in the same configuration as Fig. 3.4 in order to validate that the output combiner for SCL DPA meets the required DPA profiles namely the voltage, current, and impedance profiles. First, the two transformers are simulated separately using S-parameter simulation and the *ABCD* parameters are extracted. Secondly, once the *ABCD* parameters for each transformer satisfies (3.9) and (3.10) the two transformers are placed in the same configuration as Fig 3.3 with ideal current sources (infinite output impedance) at the input of the output combiner and determine the impedance seen by the main and peaking current sources. The following example illustrates how lumped components are determined and how the DPA operation is achieved. Given that this example uses ideal current sources it is reasonable to assume the following parameters:

- $f_0 = 60$ GHz
- $\mathrm{R}_{opt,m} = \mathrm{R}_{opt,p} = \mathrm{R}_L = 50\Omega$
- $k_m = k_p = 0.7$
- $\mathrm{C}_m = 50$ fF

Hence, the following parameters are calculated,

- $m = \sqrt{\frac{2*50}{50}} = \sqrt{2}$
- $L_m = \frac{1}{(2\pi*60GHz)^2(50fF)} = 140.7$ pH
- $C'_m = \frac{0.98^2}{(2\pi*60GHz)^2(140.7pH)(0.7)^2(1-0.7^2)} = 192.1$ fF

- $Z_T = \sqrt{50\Omega * 50\Omega} = 50\Omega$
- $L_p = \frac{(50\Omega)(0.98)}{(2\pi * 60GHz)(1-0.7^2)} = 254.9$ pH
- $C_p = \frac{1}{(2\pi * 60GHz)^2(254.9pH)(1-0.7^2)} = 54.1$ fF
- $C'_p = \frac{0.98^2}{(2\pi * 60GHz)^2(254.9pH)(0.7^2)(1-0.7^2)} = 106.1$ fF

3.4.1 ABCD parameter extraction

Fig. 3.5 and 3.6 show the main and peaking transformers configuration, respectively. The transformers contains the calculated L_m, C_p, L_p, C'_m, and C'_p. Table 3.1 shows the simulated $ABCD$ parameters for the main and peaking transformers. At 60 GHz, the $ABCD$ parameters achieves Z_T and m of 50 Ω and $\sqrt{2}$, respectively; hence, satisfying (3.9) and (3.10). Fig. 3.7 shows the real and imaginary impedance seen by port 1 verses frequency for each transformer. It is evident that at 60 GHz the impedance is completely real and no imaginary component is present. As the frequency deviates from f_o the $ABCD$ parameters start to deviate from the ideal parameters. The impedance seen by the main port slightly varies and can be optimized to achieve less variation across bandwidth. However, the impedance seen by the peaking transistor exhibits less variation across bandwidth. This is beneficial because it can maintain the 90° phase shift across the targeted bandwidth.

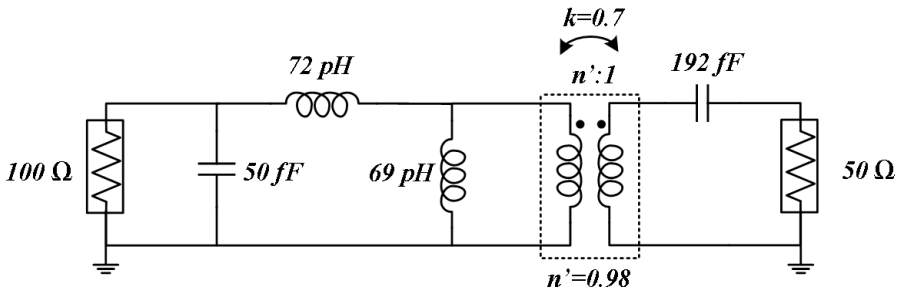

Fig. 3.5: Ideal simulation of the main transformer for $ABCD$ extraction

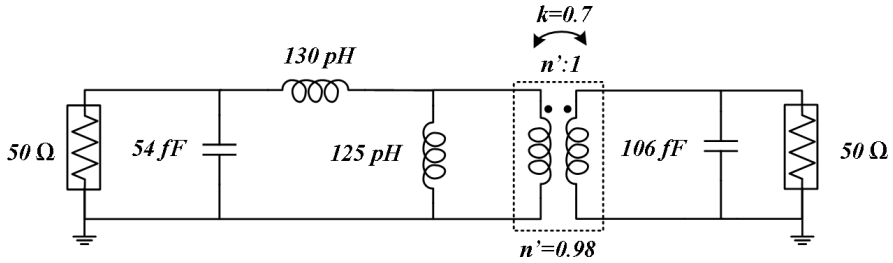

Fig. 3.6: Ideal simulation of the peaking transformer for $ABCD$ extraction

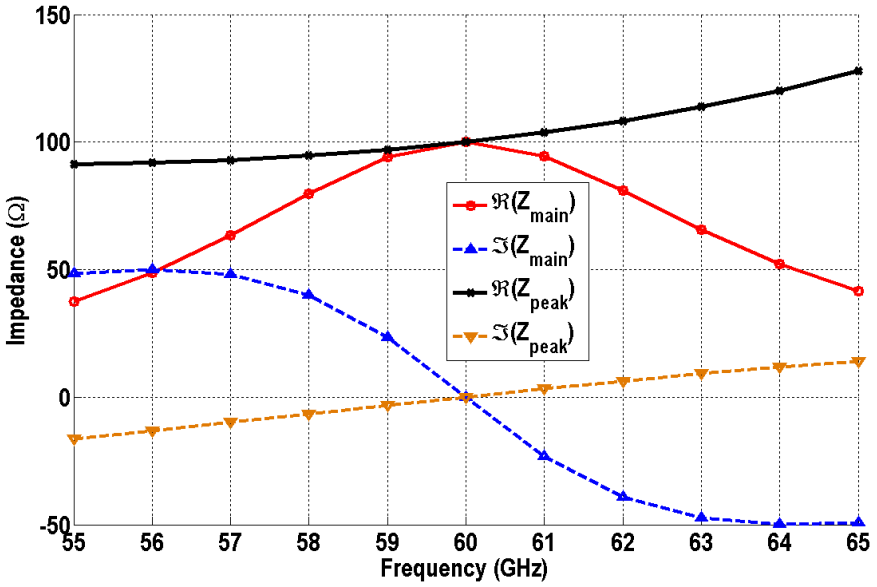

Fig. 3.7: Impedance presented by each transformer across frequency

Table 3.1: $ABCD$ extraction of each transformer across frequency

Frequency (GHz)	A^m	B^m	C^m	D^m	A^p	B^p	C^p	D^p
58	1.414/0	1.324/-90	0.004/-90	0.704/0	0.131/0	48.33/90	0.021/90	0.067/ 0
59	1.414/0	0.656/-90	0.002/-90	0.706/0	0.066/0	49.17/90	0.020/90	0.034/0
60	1.414/0	0/-90	0/-90	0.707/0	0/0	50/90	0.020/90	0/90
61	1.414/0	0.645/90	0.002/90	0.706/0	0.067/180	50.83/90	0.706/90	0.034/180
62	1.414/0	1.280/90	0.004/90	0.704/0	0.136/180	51.67/90	0.704/90	0.069/180

3.4.2 SCL DPA Configuration

This section places the main and peaking transformers that were developed in the previous section in the SCL DPA configuration and applies two ideal AC currents at the input of the output combiner. Fig. 3.8 shows the test bench for the SCL DPA configuration. Furthermore, the trans-conductance of peaking current source is twice as large of the main current source. This is to ensure that the peaking current reaches the main current at peak power. Fig. 3.9a shows the current profiles of the main and peaking current sources. Fig. 3.10 shows the impedance seen by each current source. As the peaking currents starts to increase the impedance seen by the main current source is lowered from $2R_{opt}$ to R_{opt} and the impedance seen by the peaking current sources is lowered to R_{opt}; hence, the load modulation is achieved. Fig. 3.9b shows the voltage profile of the SCL DPA and it is evident that the voltage at the main saturates when the impedance seen by the main current is lowered.

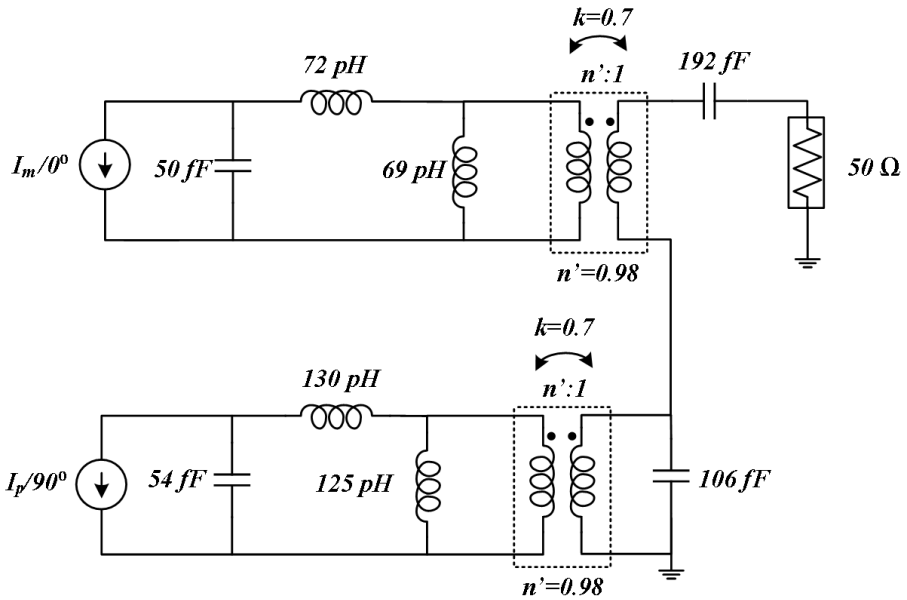

Fig. 3.8: Ideal simulation of SCL Doherty PA

In conclusion, this chapter presented the theory of SCL DPA and the formulation of the output combiner using the optimum impedance and output capacitance of the transistors.

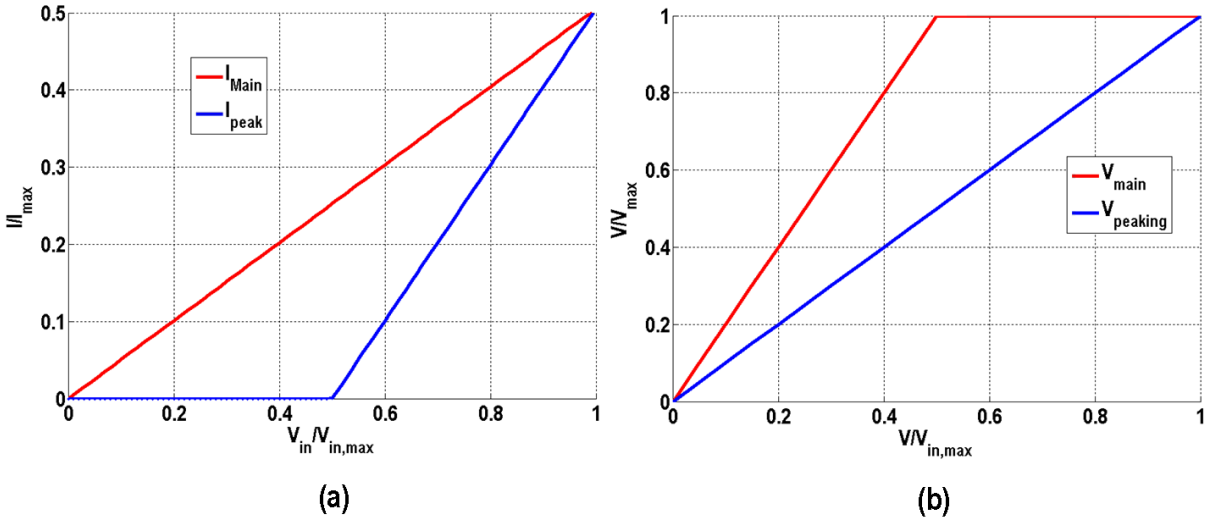

Fig. 3.9: Voltage and current profiles for SCL Doherty PA

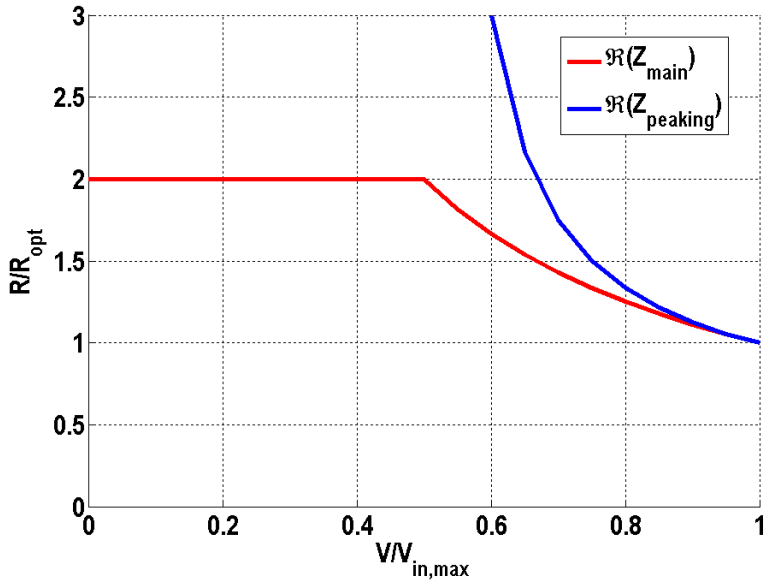

Fig. 3.10: Load modulation of main and peaking impedances for SCL Doherty PA

Furthermore, a design methodology is presented on how to approach the output combiner design. An example at 60 GHz is shown on how to extract the capacitors and inductors for each transformer. The *ABCD* parameter for each transformer is simulated and proven that the criteria in (3.9) and (3.10) are met. The two transformers are configured in an SCL DPA to prove that the profiles in terms of voltage, current, and impedance satisfies the DPA operation.

Chapter 4

mm-Wave DPA Design and Fabrication

This chapter presents the design of a two-stage SCL DPA at 60 GHz as an efficiency enhancement technique to improve back-off efficiency. The design is implemented using 45 nm CMOS SOI. The output combiner is the key building block of the design. In addition, a discussion on the design of the inter-stacked matching for the two stacked-FET and the inter-stage matching between the driver and the power stage. Also, this chapter discusses the optimal layout for the transistor to reduce parasitics and distribute the thermal effect evenly. Lastly, this chapter continues the design details of the implementations and presents simulation and measurement results.

4.1 60 GHz SCL DPA Design

Fig. 4.1 shows the schematic of the proposed transformer-based SCL DPA with dual RF inputs for the main and peaking paths where each path contains a driver and power amplifier. The driver stages use a common-source topology to provide a high gain for the power stages. The power stages utilize a two-stacked FET topology to achieve a higher output power.

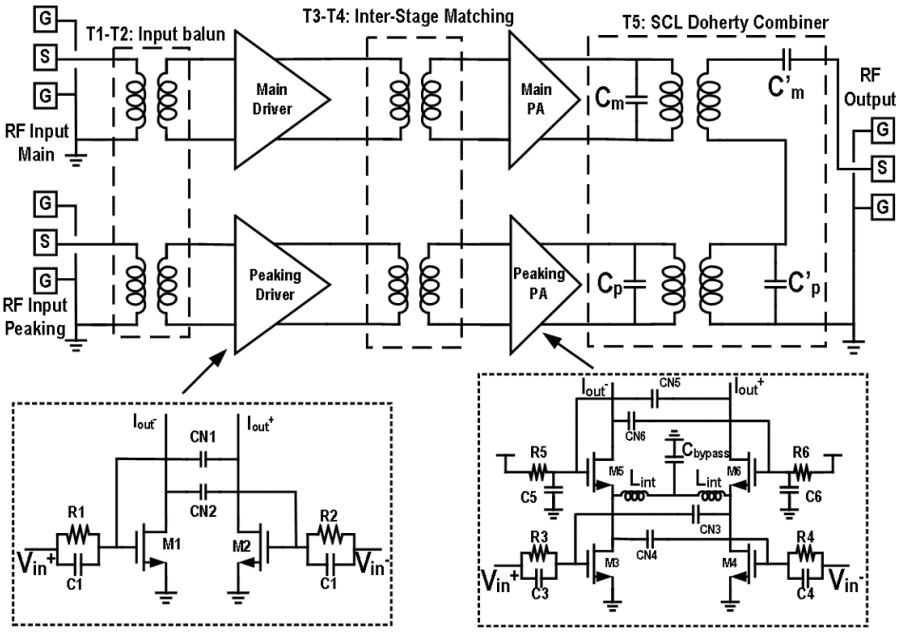

Fig. 4.1: Schematic of the proposed transformer-based SCL Doherty PA

4.1.1 Power Transistors

In this design, the transistors are laid out in a manifold manner to reduce the output capacitance and distribute the thermal effect evenly among the unit transistors. The unit transistor cell is sized to be 30 μm in width and 45 nm in length as shown in Fig. 4.2. Fig. 4.3 shows the drain and gate are laid out to form a global connection to each drain and gate terminals of the unit transistor cells. This allows the current from each cell combine at the global connections. Each source of the unit transistor cells are connected through ground ring to provide a stronger connection to ground.

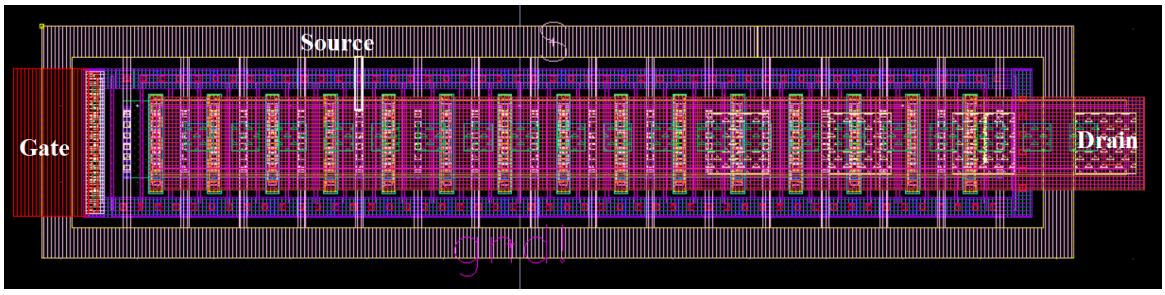

Fig. 4.2: Layout of the differential pair two-stacked FET

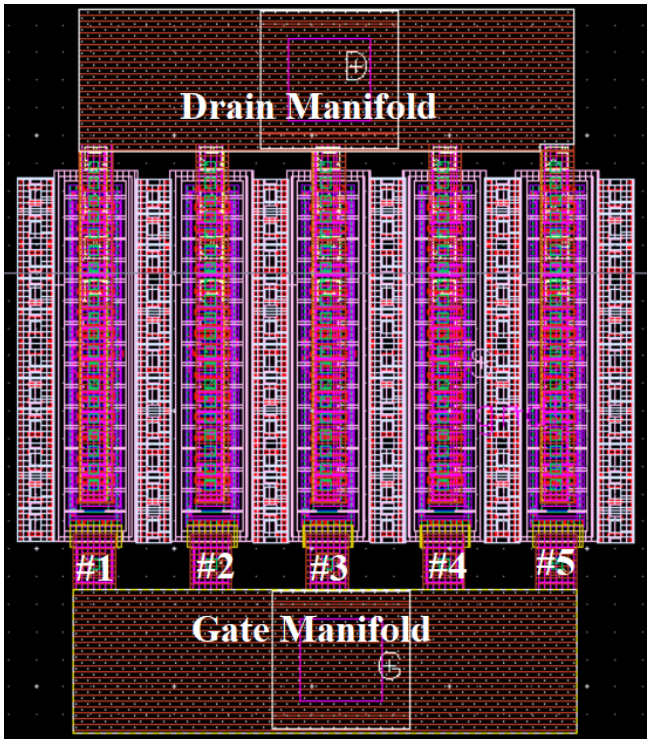

Fig. 4.3: Layout of the differential pair two-stacked FET

The power stage is designed as a two-stacked transistor as shown in Fig. 4.1. The width of each of the transistor is 150 μm and an inductive inter-stacked matching of 80 pH is added to maximize the output power by adjusting the drain voltage at M3 and M4 to combine in-phase at the output combiner. Parasitic capacitances at inter-stacked nodes causes current leakage through C_{GS}. With the use of inter-stacked stubs and the addition of stacked capacitors at the gate of M5 and M6, this helps in presenting the optimum impedance to each FET. The added stacked capacitors are 200 fF.

The transistor sizing is based on how close the optimum impedance to 50 Ω to simplify the matching while maximizing the output power and efficiency. The optimum impedance of the 150 μm is around 30 Ω. The output capacitance of the differential two stacked transistor is 65 fF. In addition, the drain-to-gate neutralization capacitors of 45 fF are added to top and bottom transistors to improve the reverse isolation and differential-mode stability of the transistors. The stability issue in the cascode topology arises from the fact that the top FET

is degenerated by capacitive load and the real part of the input impedance seen from the gate is negative. Adding a drain-to-gate neutralization capacitor cancels the capacitance seen by the top FET. Furthermore, a series RC stabilizing network is added to improve common-mode stability at low frequencies. Fig. 4.4 shows the layout of the 150 μm power transistor differential pair of the power stage containing the neutralizing capacitors.

The driver amplifiers are designed as a common-source transistor that are 120 μm wide. Also, the driver stage use a drain-to-gate neutralization technique (34 fF) and RC series stabilizer to improve reverse isolation and stability. The driver amplifiers were used in the main and peaking path. To address the low gain of the class-C operating peaking transistor, different gate bias voltages were applied to the main and peaking driver stages to ensure a gain difference of 2 dB needed to achieve the proper current profile of DPA operation.

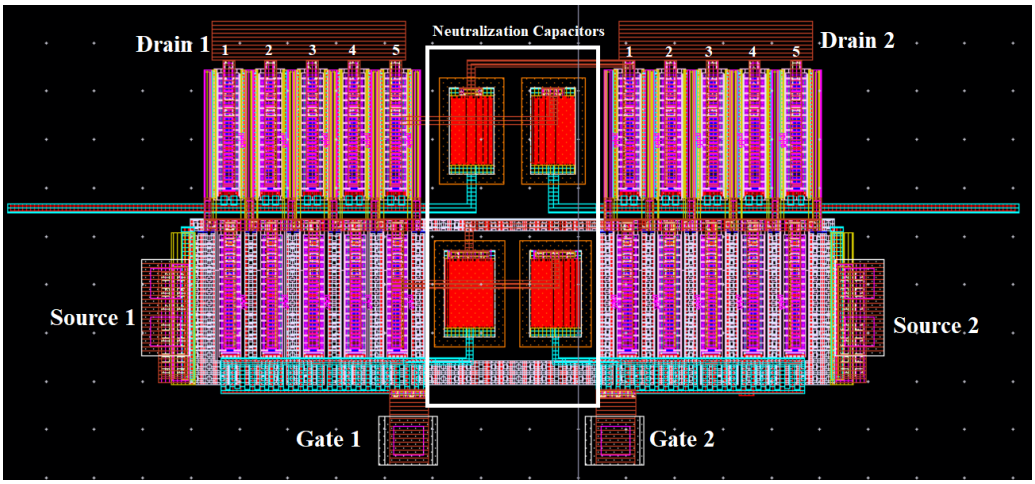

Fig. 4.4: Layout of the differential pair two-stacked FET

4.1.1.1 Load pull Simulation

The interconnects of the transistors are electromagnetic simulated to accurately determine the optimum impedance of the overall two-stacked differential pairs with the active layer of

the transistors are RC extracted. Fig. 4.5 shows the load pull simulation at 60 GHz of the differential pair two-stacked main PA biased as deep class AB (V_G=0.3 V and V_{DD} = 2.4) under 3 dB compression with input power of 2 dBm. The optimum impedance of the main ($Z_{opt,m}$) at low input power is, (10.3 + j39.5) Ω, and at 3 dB compression the $Z_{opt,m}$ is, (8.9 + j36.6) Ω. The expected output power of the main is 16.4 dBm with a peak PAE of 39 %.

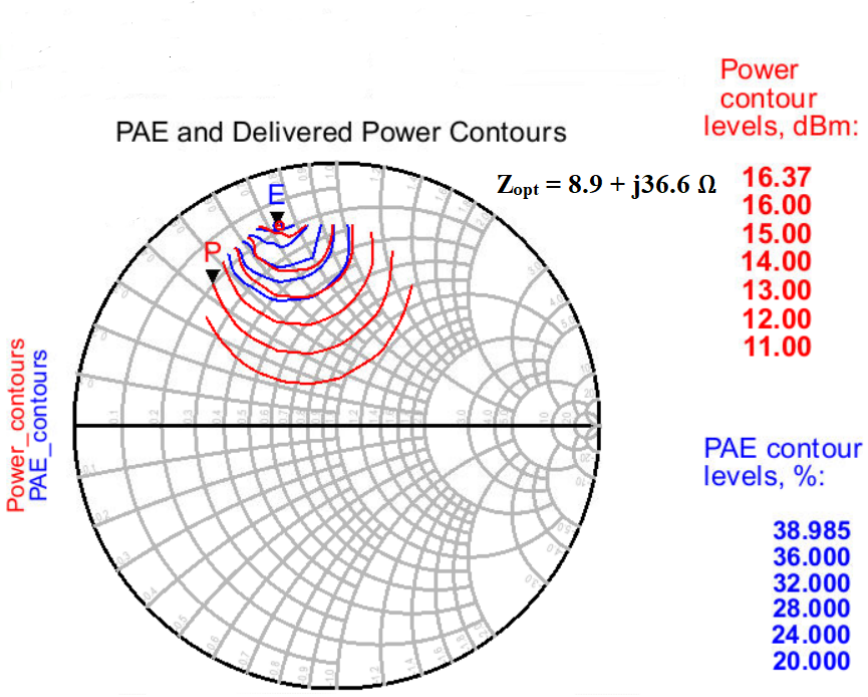

Fig. 4.5: load pull simulation for main transistor with input power of 2 dBm and gain compression of 3 dB

When the peaking PA starts to turn on, the main PA should start to saturated, thus, the peaking PA should peak at 3 dBm input power after the compression of the main PA. Fig. 4.6 shows the load pull simulation at 60 GHz of the differential pair two-stacked peaking PA biased as class C with input power of 3 dBm. The $Z_{opt,p}$ is (8.9 + j36.6) Ω. Lastly, the top gate-to-drain neutralization showed an increase of output power by 0.6 dBm and PAE of 2 % for the main and peaking PAs.

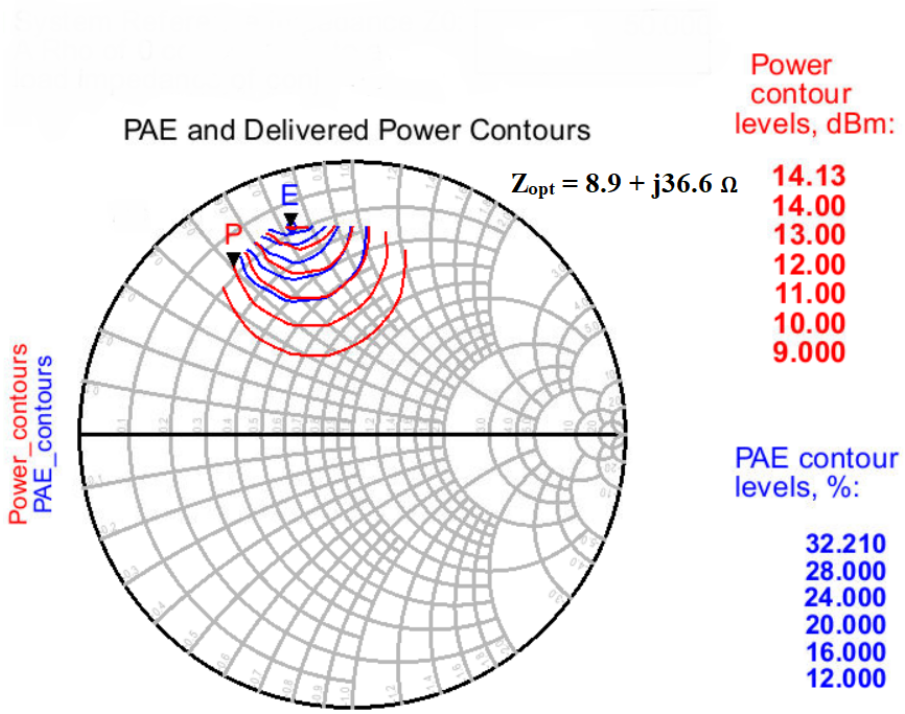

Fig. 4.6: Load pull simulation of the peaking transistor with input power of 5 dBm

4.1.2 Output Combiner, Inter-stage and Input matching

The design of the output combiner network, T5, is initiated by individually designing the main and peaking transformers, which were implemented using vertically coupled coils using the two topmost copper layers (UA and UB) of thickness 1.2 μm on a low-resistivity silicon substrate. The BEOL of the 45 nm CMOS SOI is shown in Fig. 4.7. The vertical coupling octagon topology for the transformer showed a higher coupling factor than lateral coupling using the BEOL of the 45 nm CMOS SOI. However, this could introduce impedance imbalances between the branches since both coil experience different parasitics. The electromagnetic simulation results of the transformers and the power transistor interconnects (from the lowest metal, M1, to the highest metal layer, UB) aids in accurately determining the optimum impedance and the output capacitance of the power transistors in order to determine the values of C'$_m$ and C'$_p$, so that (3.9) and (3.10) are satisfied at 60 GHz. However, the effective inductance for the peaking transformer is less than the inductance of the main transformer. This is to reduce the

loading effect on the main at 6 dB back-off since the peaking acts as a parasitic loading. The output capacitance of the peaking transistor must increase to shift back the design frequency to 60 GHz, thus, a Vertical-Nature capacitor (VNcap) of 12 fF is placed at the output of the peaking transistor. In this design, the diameters of the main and peaking transformers were set to 43 and 38 μm, respectively. The width for both transformers is 4 μm. The values of C'$_m$ and C'$_p$ were found to be 160 and 95 fF, respectively. In addition, the output combiner is co-designed with the bondpads and the capacitance associated with the bondpads are absorbed into the combiner.

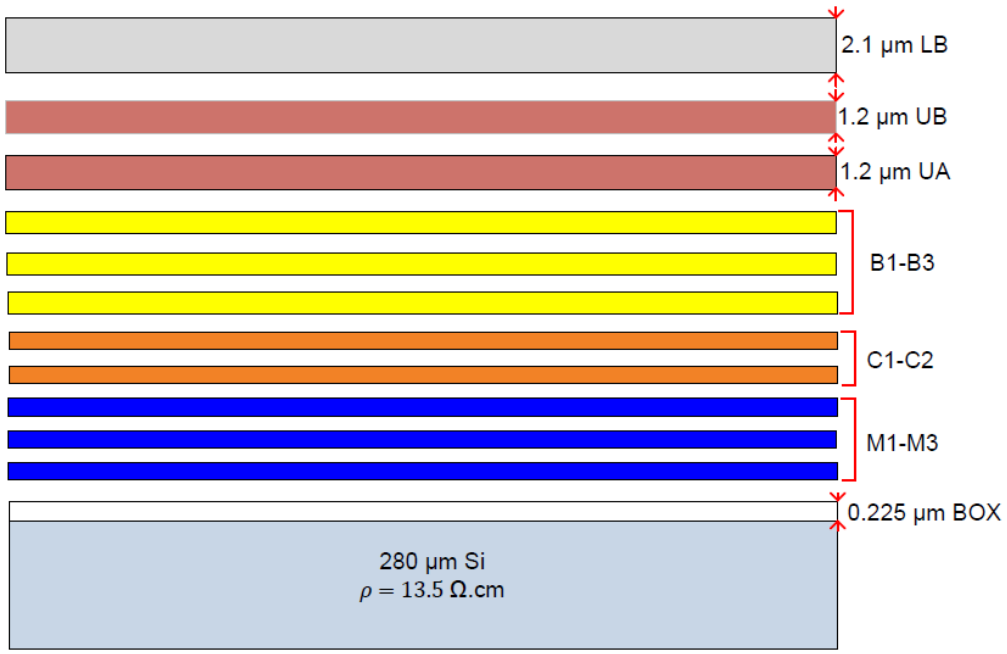

Fig. 4.7: IBM 45 nm CMOS SOI Back-end of the line stack [21]

Fig. 4.8 shows the layout of the output combiner containing the series and shunt capacitors. The capacitors are implemented using VNcaps in the 45 nm CMOS SOI process. These capacitors exhibit low quality factor (20-30) at 60 GHz. Furthermore, the connection between the two secondary coils is minimized by bring the two transformers as close as possible to the point where the coupling between them is at the lowest. The two transformers exhibits capacitive coupling between the primary and secondary coil in each transformer and this causes

impedance imbalances within in the transformers. Fig. 4.9 shows the electromagnetic simulation of the impedance imbalance between each branch of the main and peaking transistors. The output combiner exhibits low impedance imbalances between the branches of the main and peaking transformers. From 55 GHz to 65 GHz, the impedance of main path shows a variation of (1.2+j2) Ω and the impedance of the peaking path shows a variation of (0.4+j1) Ω at peak power. Furthermore, Fig. 4.10 shows the voltage across C'$_p$ and it evident that at low output power the peaking transformer is acting as a $\lambda/4$ impedance inverter since the voltage is close to zero. As the input power increases the peaking transistor starts to turn on around 12 dBm output power. Furthermore, the combining efficiency achieves an efficiency of 63 % in back-off region and increases as the peaking PA starts to turn on shown in Fig. 4.11. Lastly, Fig. 4.12 shows the output Ground-Signal-Ground (GSG) pad that is connected to the output combiner. The GSG pad contains grounded shield to minimize the loss from the output port of the output combiner to the output pad.

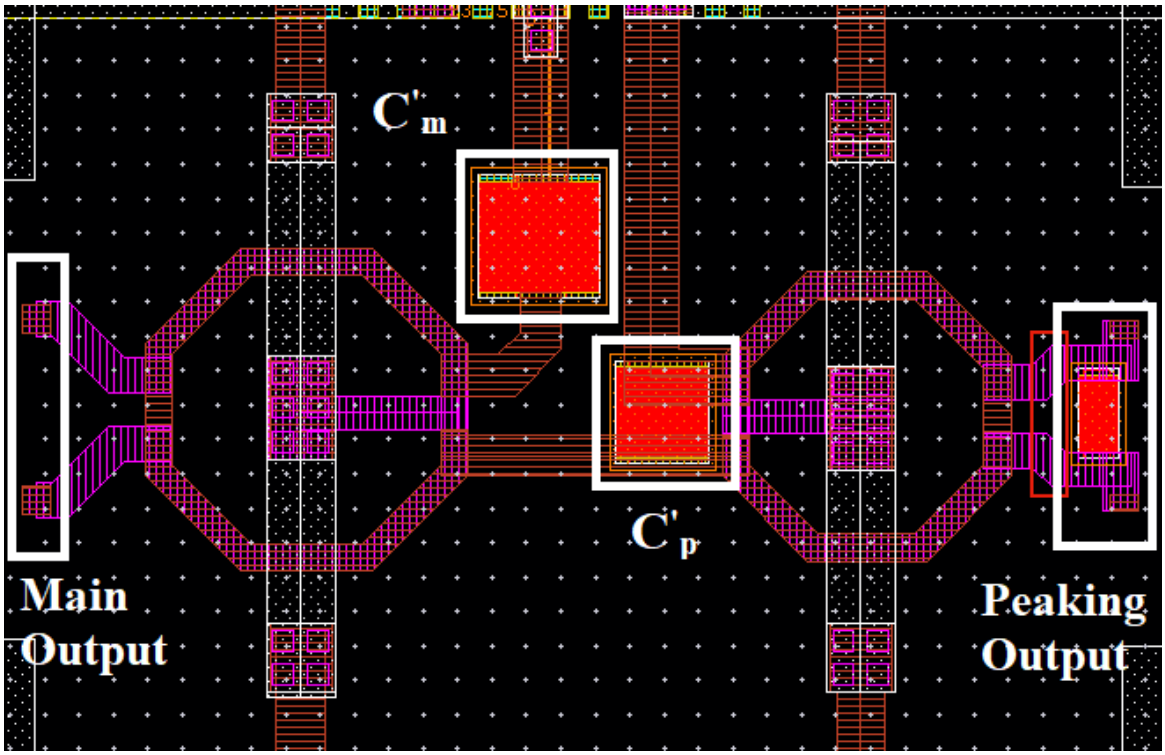

Fig. 4.8: Layout of the output combiner for SCL Doherty PA

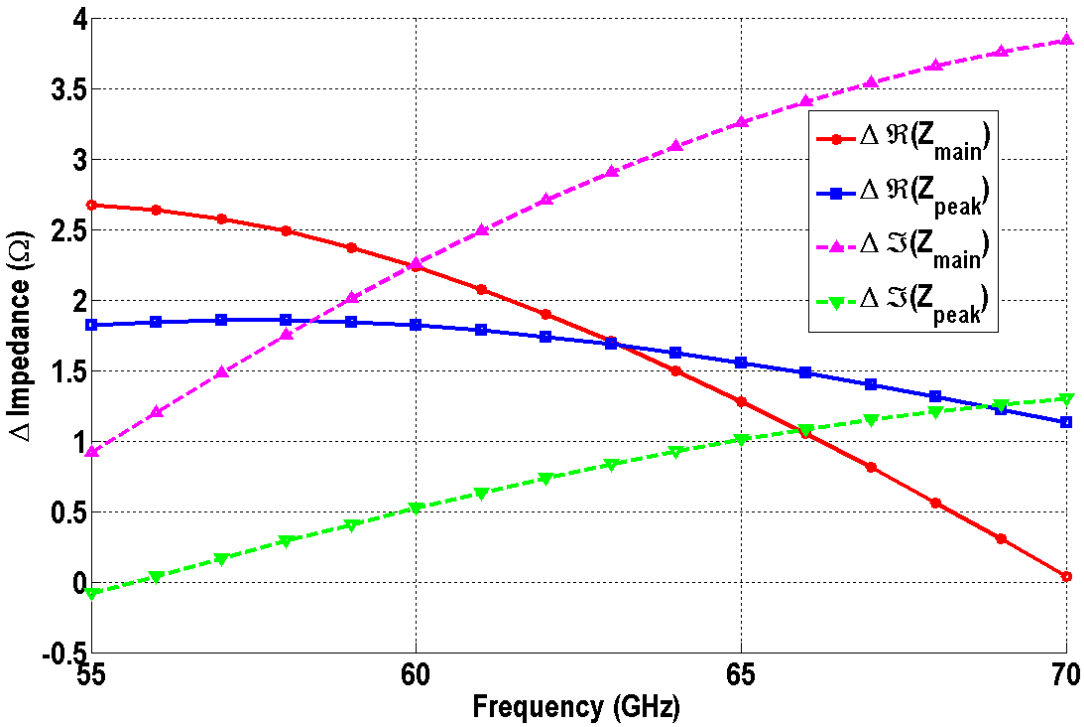

Fig. 4.9: Output combiner impedance imbalances between branches across frequency

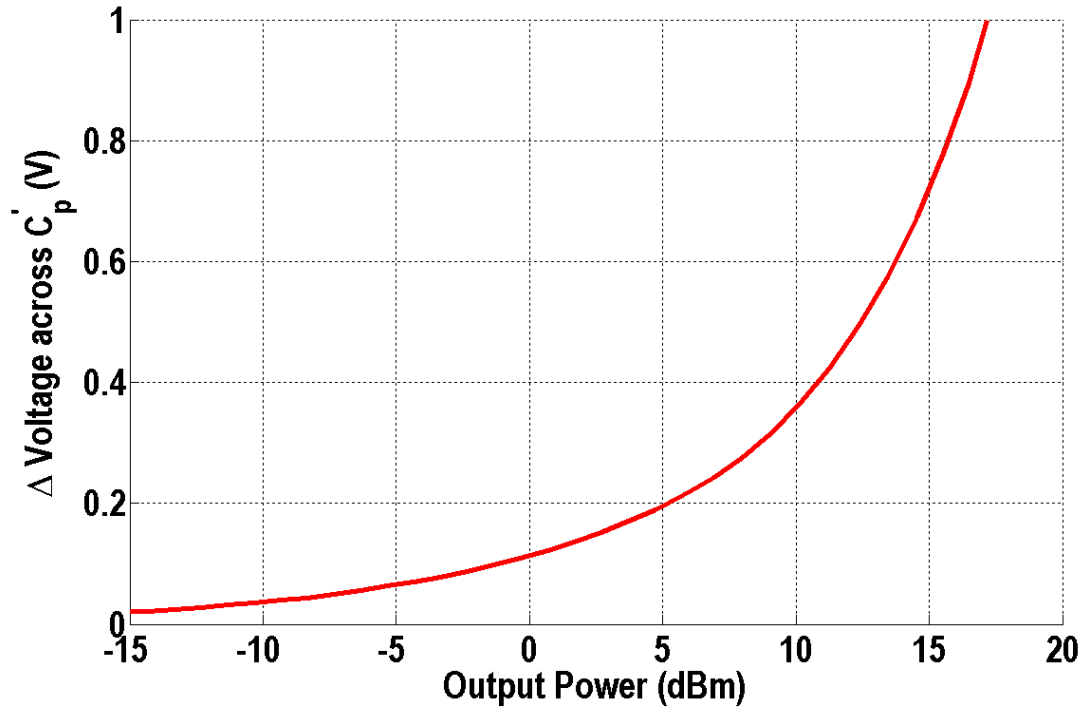

Fig. 4.10: Post-layout simulation - Voltage across C'$_p$

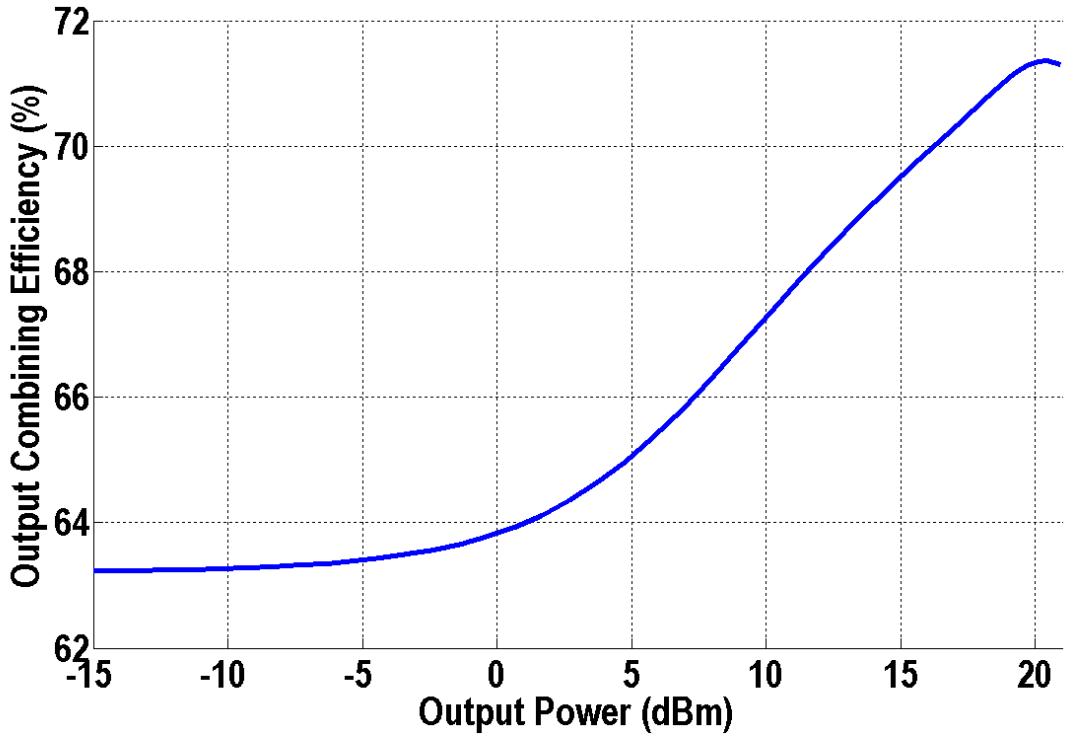

Fig. 4.11: Simulated combining efficiency of the output combiner for SCL Doherty PA

As shown in Fig. 4.1, the proposed SCL DPA uses transformer-based input and inter-stage matching to maximize the power gain at 60 GHz. The input matching of the main and peaking paths does the conversion from single-ended to differential. The diameters and widths of the input and inter-stage matching were designed to be 50 and 6 μm, respectively. Fig. 4.13 and 4.14 shows the layout of inter-stage and input balun matching. Both of the matching use the three topmost layers where LB and UB are shunted together and magnetically coupled to UA.

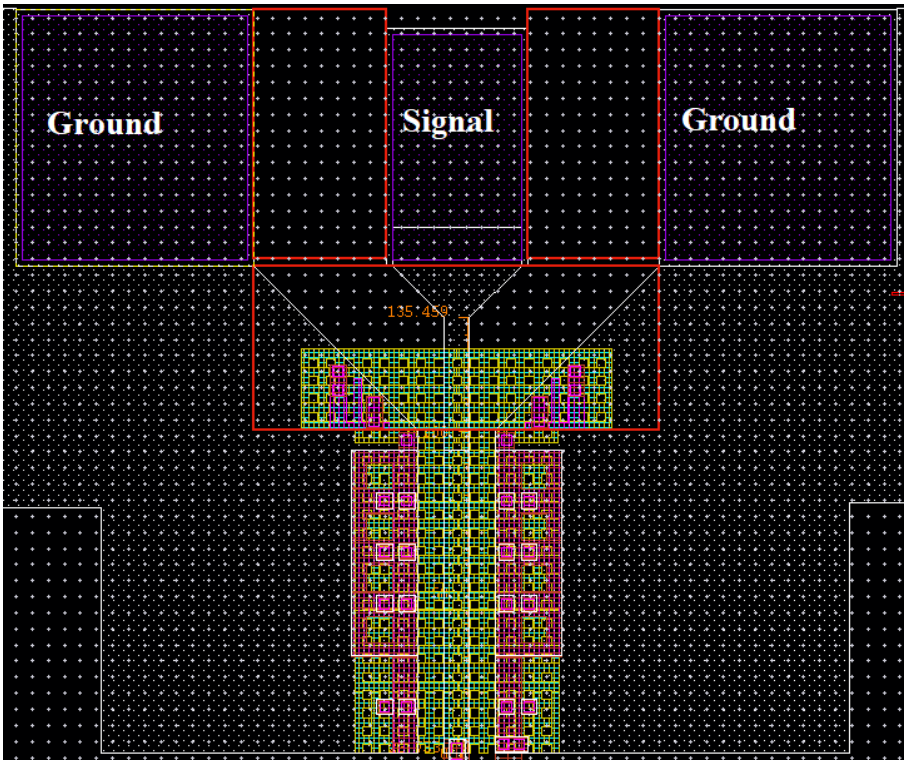

Fig. 4.12: Layout of the output GSG pad

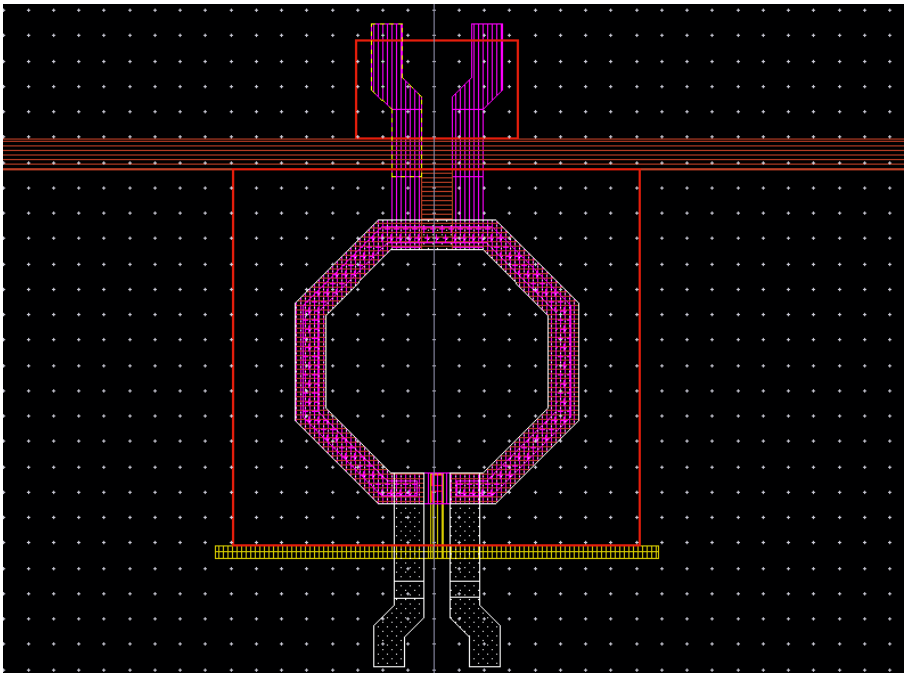
Fig. 4.13: Layout of the inter-stage matching

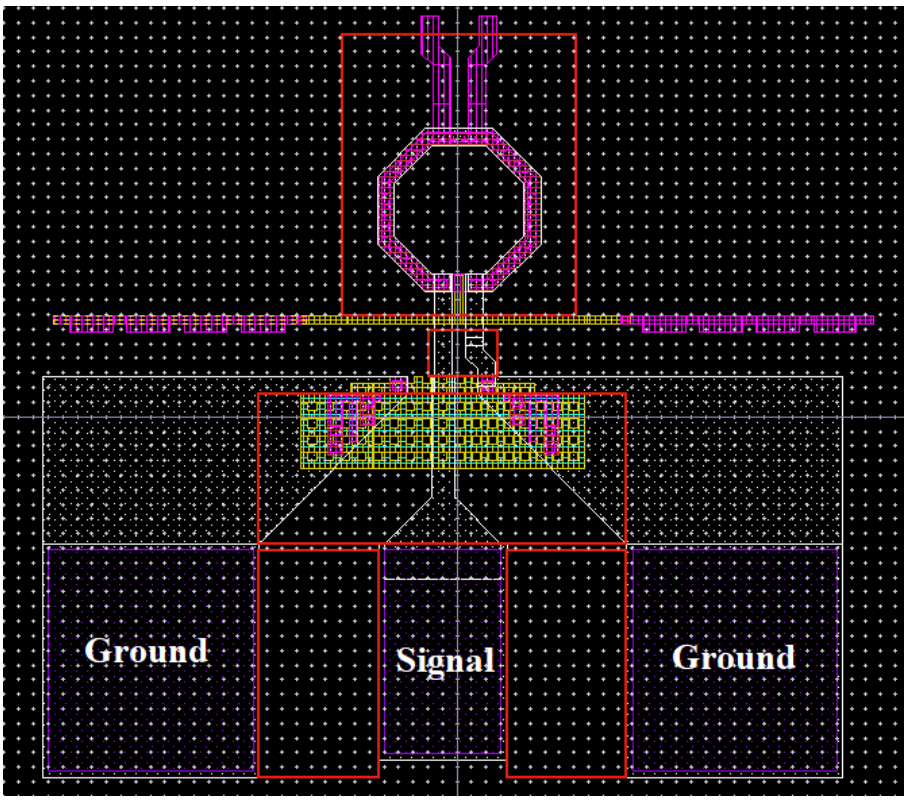

Fig. 4.14: Layout of the input balun with GSG pad

4.1.3 Simulation and Measurement Results

Fig. 4.15 shows the micro-photograph of the fabricated SCL DPA chip in 45 nm CMOS SOI technology (from Global Foundry) with a core area of 0.83 by 0.15 mm^2. Fig. 4.16 (a) and (b) shows the measurement setup for small-signal and continuous-wave (CW) large-signal, respectively. The following small-signal and large signal measurements are obtained using a vector network analyzer (PNA-X N5247A) with the source phase control option to provide the 90° phase shift between the peaking and main inputs. Furthermore, conducting measurements at mm-wave frequencies is difficult due to the errors introduced in the RF paths by the components (i.e. phase stable cables, RF probes, adapters), thus, calibration for small-signal and large-signal measurements are necessary. The calibration for conducting small-signal measurement is performed on a impedance standard substrate using Short-Open-Load-Thru

(SOLT) to shift the reference plane up to the Device Under Test (DUT). Furthermore, the calibration for the large-signal measurement required source power calibration for both RF inputs and receiver calibration from the two RF inputs to the RF output. External drivers are added in the main and peaking paths to compensate for the losses in the RF paths and have enough power to drive the main and peaking paths to saturation. During the power calibration the external drivers are included in the RF paths.

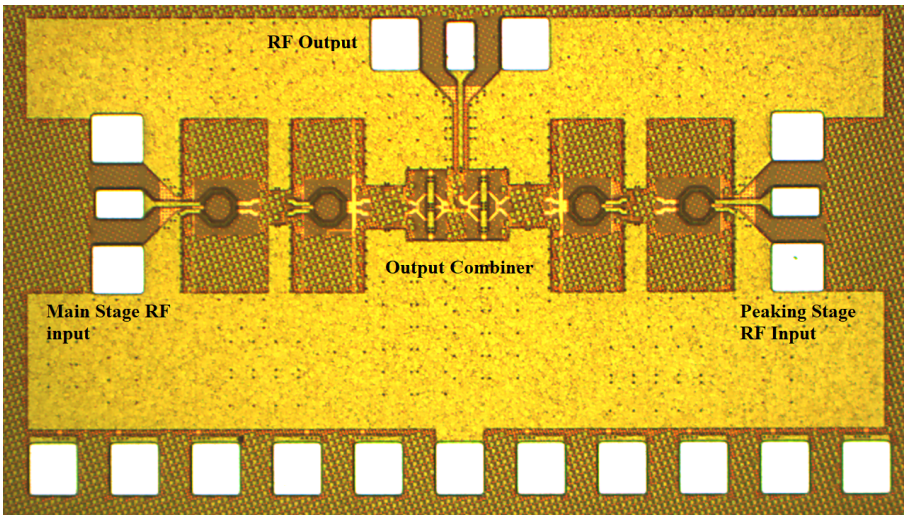

Fig. 4.15: Die micro-photograph of SCL Doherty PA

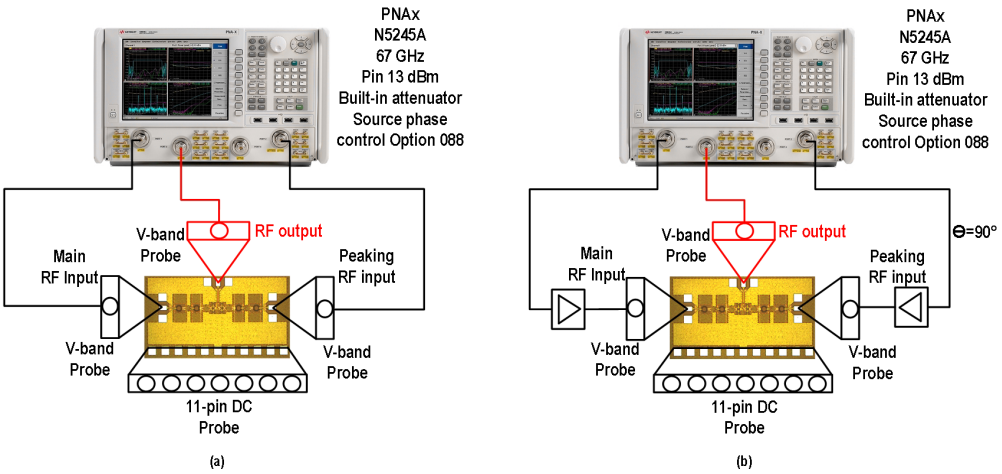

Fig. 4.16: Measurement setup for (a) Small-Signal (b) 60 GHz continuous-wave large-signal

During the small-signal measurement the peaking path is off and the gate biasing of the driver and power stage of the main path are both 0.30 V. Fig. 4.17 shows the measured and simulated S-parameters which reveal a gain close to 15 dB with - 3 dB bandwidth of 7 GHz. The center frequency shift is caused by the inaccurate electromagnetic modelling of the transistors. However, the effect is minimal since the center frequency is shifted by 1.6 GHz. Fig. 4.18 shows the input and output reflection coefficients that are maintained below -10 dB within the frequency band of 57 to 64 GHz. The output reflection coefficient experiences a resonance around the center frequency. It is speculated that this is due to the output combiner since it is a resonance structure.

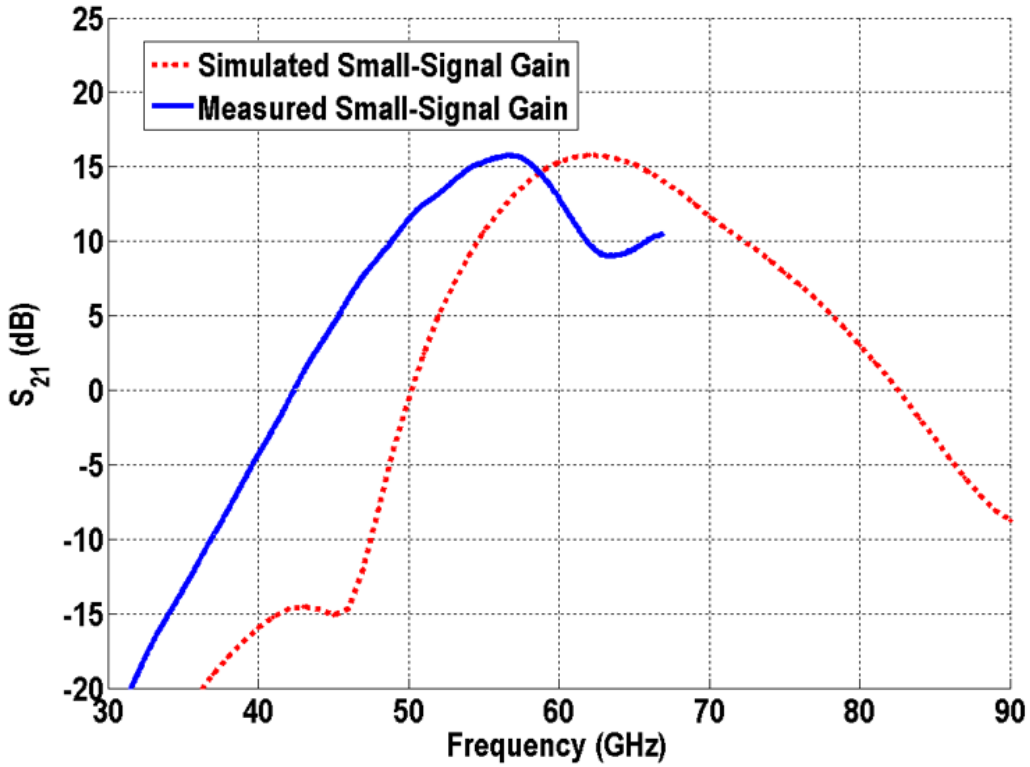

Fig. 4.17: Small-signal gain of the SCL Doherty PA

The post-layout simulation of the current profile of the main and peaking transistor are shown in Fig. 4.19. The peaking transistor is biased to turn on around 12 dBm of output power. Since both transistors are sized the same, unequal power split at the input of the SCL

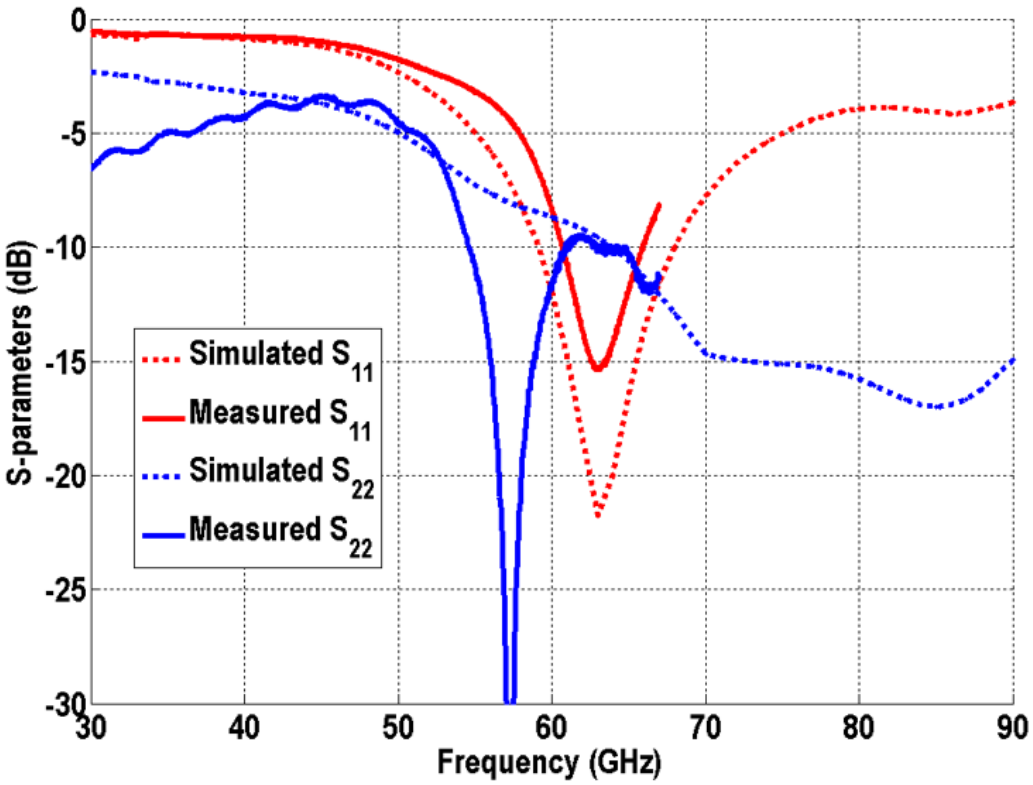

Fig. 4.18: Input and output reflection coefficient of the SCL Doherty PA

DPA must be used to achieve the proper current profile. In this design, unequal power split of 2 dB to peaking path is used by adjusting the biasing of the drivers. Fig. 4.20 shows the drain voltage of main transistor is saturating when peaking transistor (12 dBm) starts to modulate the load seen by the main transistor. Fig. 4.21 shows the load modulation across output power. The real impedance presented to the main is lowered from 62 Ω to 34 Ω, which is roughly from $2R_{opt}$ to R_{opt} and the impedance presented to the peaking transistor at peak power is the same as the main transistor since both transistors are the same size.

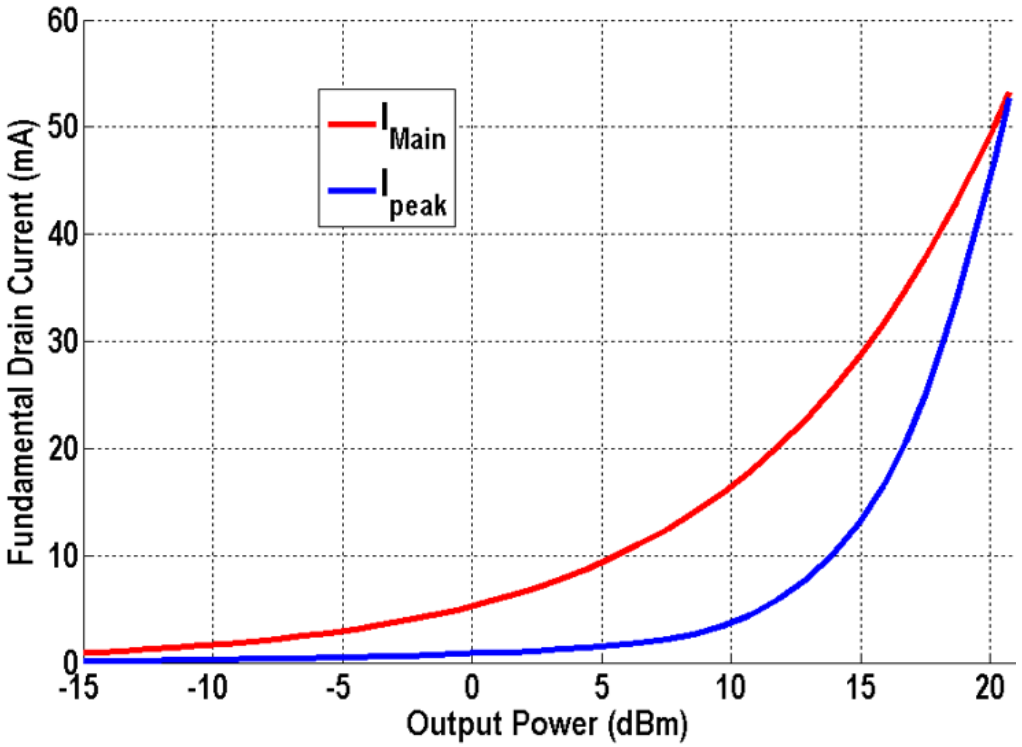

Fig. 4.19: Fundamental current of main and peaking transistors

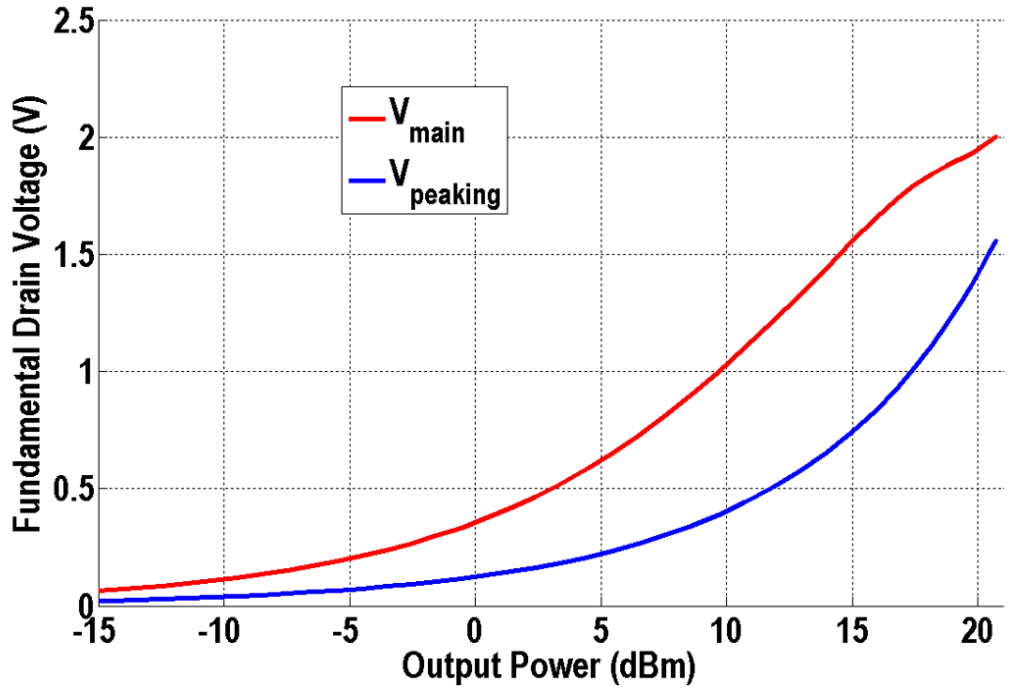

Fig. 4.20: Fundamental drain voltage of main and peaking transistors

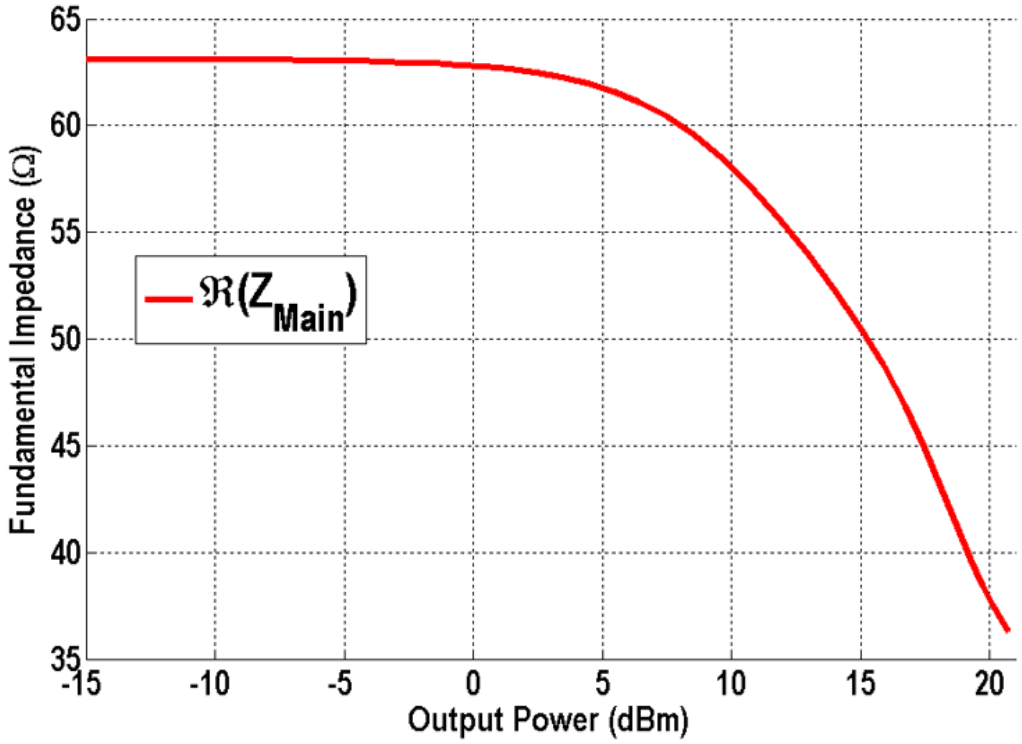

Fig. 4.21: Fundamental impedance seen by the main and peaking transistors

The large-signal measurement results under a 60 GHz continuous-wave stimuli, as shown in Fig. 4.22, showed a saturated output power (P_{SAT}) of 19.3 dBm and a PAE of 18.9 % and 8.5 % at P_{SAT} and 6 dB back-off, respectively. Based on Fig. 4.23 the SCL DPA demonstrated good large signal performance from 57 to 64 GHz. In fact, the P_{SAT} varied by only 1 dB over that band and the PAE at P_{SAT} and 6dB back-off power levels were equal to 18 % and 8 % or higher respectively. Furthermore, the measured DC currents of the main and peaking PAs fulfil the Doherty current profile as shown in Fig. 4.24. The measured AM-PM distortion at the output of the SCL DPA showed a phase variation up to 7° at P_{SAT} as shown in Fig. 4.25.

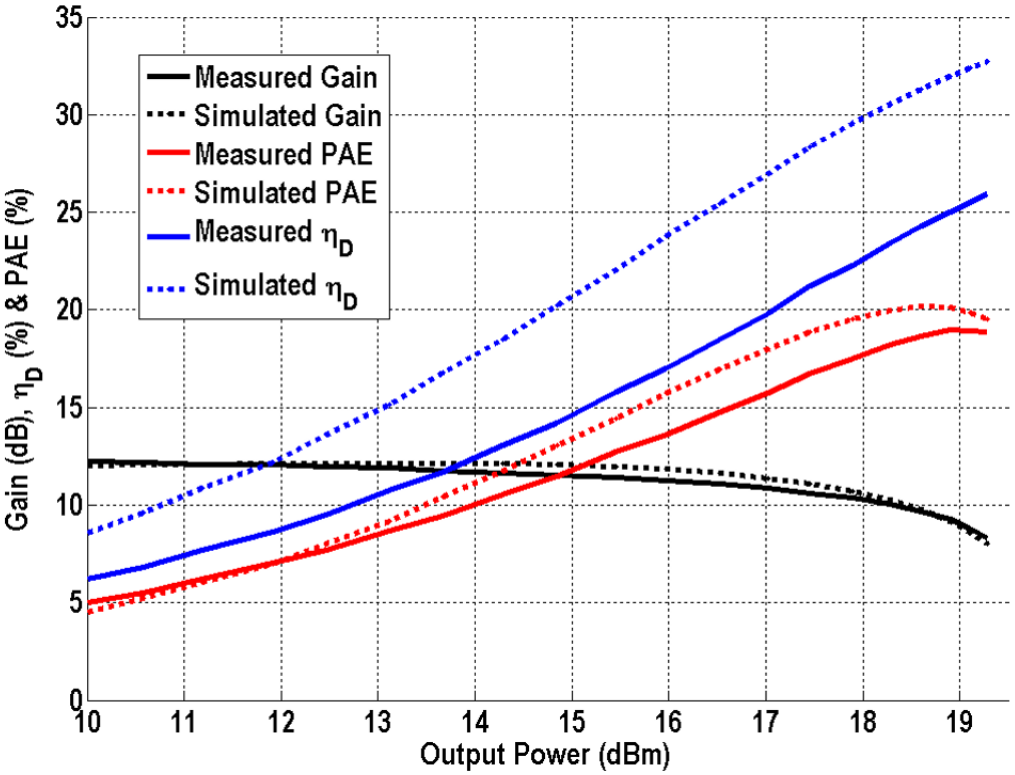

Fig. 4.22: Measured and simulated AM-AM, drain efficincy and PAE at 60 GHz

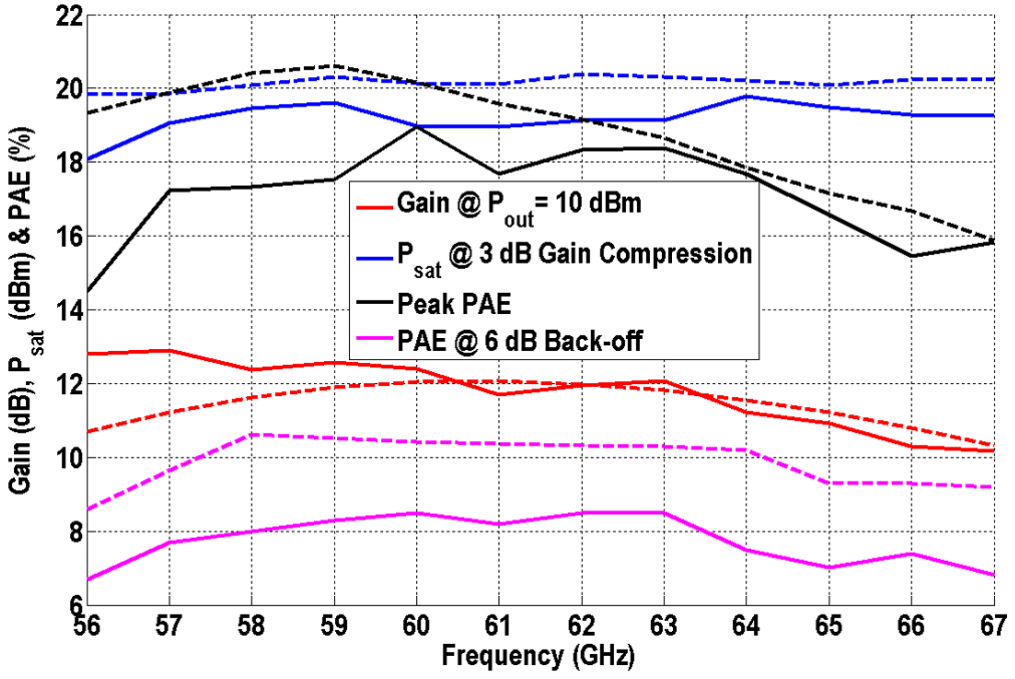

Fig. 4.23: Measured (solid) and simulated (dashed) performance of SCL DPA across 18 % fractional bandwidth

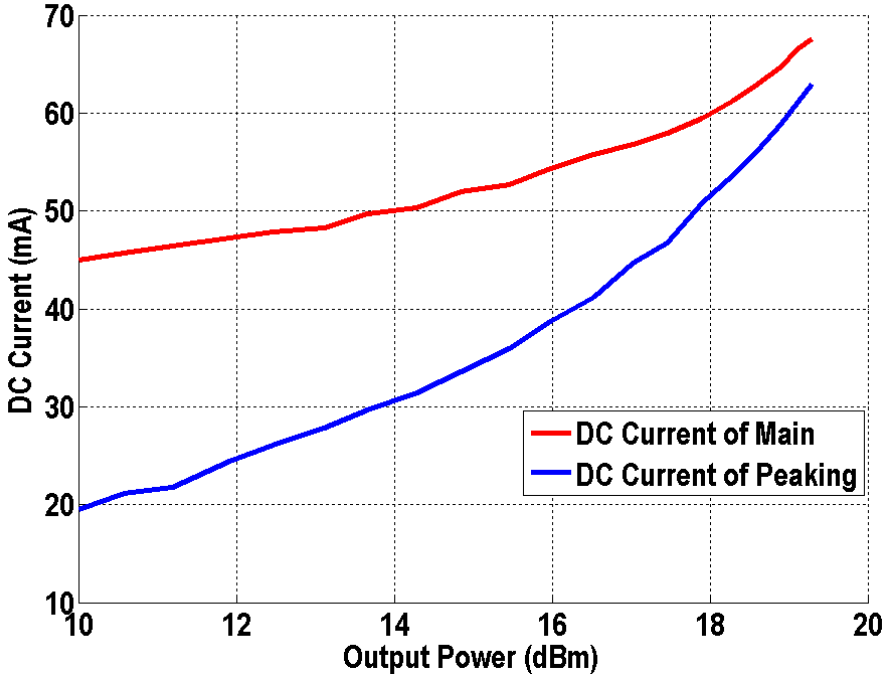

Fig. 4.24: Measured DC current of the main and peaking PAs at 60 GHz

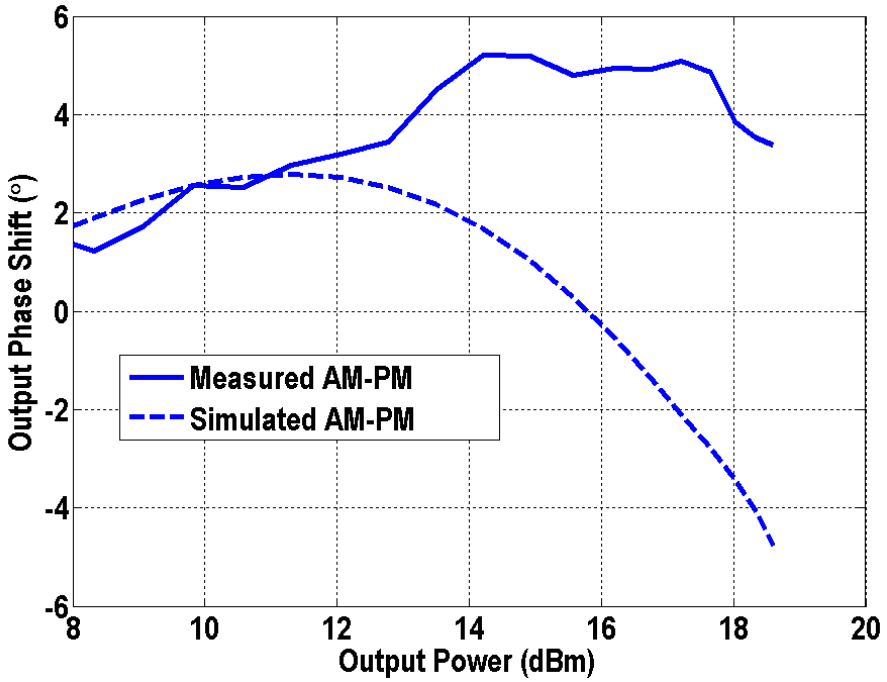

Fig. 4.25: Measured (solid) and simulated (dashed) AM-PM distortion of SCL DPA at 60 GHz

Chapter 5

Conclusions and Future Work

5.1 Conclusions

The primary drive for moving towards the unexploited mm-wave frequencies is to meet the demand of the high data rate communication systems. However, this increases the complexity in the radio front-end hardware design, especially when digitally modulated signal with spectrum efficient technique is being utilized. These signals exhibit high PAPR and acts as an impediment in attaining an adequate linearity vs. efficiency trade-off when designing mm-wave PAs. The need for PAs that are efficient at peak power and back-off region is crucial to efficiently amplify signals with high PAPR. One technique of efficiently enhancing PAs in back-off region is the Doherty technique. However, the realization of DPAs at mm-wave frequencies faces several challenges namely the $\lambda/4$ impedance inverter design and the low gain of the biased class C peaking PA. This motivated the need to explore other DPA topologies to reduce the affects of the mentioned challenges. This thesis has opted for SCL DPA instead of the conventional DPA topology to reduce the effect of the lossy $\lambda/4$ impedance inverter from the main path to improve efficiency in the back-off region. The objective was to determine an output combiner

for the SCL DPA that achieves the Doherty profile and minimize the losses in the main path. This thesis opted for a transformer-based output combiner that is derived from the ideal $ABCD$ matrices of the $\lambda/4$ impedance inverter and the impedance matching of the main transformer.

Chapter two provided an overview of the classes of operation of PAs and their feasibility at mm-wave frequencies. Furthermore, a literature survey was presented on how to maximize output power of PAs at mm-wave frequencies through power combining techniques at device and circuit levels. Lastly, a comparison of the state-of-art mm-wave DPAs is conducted. Chapter three, presented the theory of SCL DPA and derivation of the output combiner based on the $ABCD$ matrix. In addition, to illustrate the validity of the proposed output combiner ideal simulations are shown. Chapter four, presented the fabricated design of the two-stage SCL DPA at 60 GHz using the 45 nm CMOS-SOI technology. The SCL DPA topology was proposed in this thesis in an effort to improve the efficiency of PAs in the back-off region. The 60 GHz SCL DPA design achieved a gain of 12.3 dB, P_{SAT} of 19.3 dBm, and PAE of 18.9% and 8.5% at 0 dB and 6 dB back-off power levels.

5.2 Future Work

As the frequency deviates from the design frequency, due to the dispersive behaviour of the $\lambda/4$ impedance inverter, the load modulation profile is not guaranteed across frequency hence the linearity and efficiency enhancement is not maintained. Therefore, in a wideband SCL DPA one needs to maintain the same load modulation profile. As future work, one can expand the output combiner analysis to extend the bandwidth of the SCL DPA. One technique of practically extending the SCL DPA bandwidth is by adding varactor-loaded transmission lines after the 90° quadrature hybrid as implemented in [19]. The relative phase of main and peaking paths can be adjusted to further extend the DPA bandwidth.

Another potential area for future investigation could be to reduce the AM-PM distortion at the output of the SCL DPA. Assuming the driver stage is linear, the input voltage to the power stage before amplification gets distorted by the non-linearity of the input capacitance (C_{IN} =C_{IN}) when C_{GD} is perfectly cancelled. However, if this is not the case then C_{GD} gets reflected back to the input through the miller effect with a factor of (1-A_v), where A_v is the voltage gain and depends on the trans-conductance, G_m, of the power stage. Hence, the miller input capacitance show a non-linear behaviour with respect to the input voltage since G_m is strongly non-linear under large-signal operation [22]. One way of alleviating the AM-PM distortion is by adding PMOS varactors to compensate the non-linear behaviour of the input capacitance of an NMOS transistor [22]. Another way of reducing the AM-PM distortion is by implementing the driver stage as PMOS drivers. When properly sized, the technique can effectively cancel the non-linear capacitance and the non-linear G_m [23].

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