EVALUATION OF THE PRACTICALITY OF SYSTEM EFFICIENT ESD DESIGN

BY

COLLIN MICHAEL REIMAN

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2017

Urbana, Illinois

Adviser:

Professor Elyse Rosenbaum

ABSTRACT

A custom test board facilitates transmission line pulse (TLP) characterization of the external pins of an integrated circuit. Models extracted from the data are used to simulate the pin-level response of the integrated circuit (IC) to an IEC 61000-4-2 discharge. Electrostatic discharge (ESD) gun zaps are applied to the test board; simulated and measured waveforms are compared.

ACKNOWLEDGMENTS

I would like to thank my advisor, Professor Rosenbaum, for her guidance and teaching. Her mentoring has helped me grow as a scientist and an experimentalist. I would like to thank my family and friends for their continued support. I would also like to thank the students who helped me with this work: Robert Mertens, Nicholas Thomson, and Yang Xiu.

TABLE OF CONTENTS

CHAPTER 1: INTRODUCTION 1

1.1 Motivation 1
1.2 Thesis Overview 2

CHAPTER 2: PRIOR WORK 3

2.1 Transmission-Line Pulse Measurements 3
2.2 IEC 61000-4-2 Standard 3
2.3 System-Efficient ESD Design 5

CHAPTER 3: OVERVIEW OF TEST SYSTEM 7

3.1 Test Board 7
3.2 Test Chip Protection Circuitry 10

CHAPTER 4: TLP MEASUREMENTS 13

4.1 Power-On vs. Power-Off Response 13
4.2 Effect of Reference Bus 15
4.3 Effect of Decoupling Capacitance 15
4.4 Effect of Pin Bias 16
4.5 Die-Level vs. Board-Level TLP 18

CHAPTER 5: I-V SIMULATION RESULTS 20
CHAPTER 6: SYSTEM TRANSIENT RESPONSE 23

6.1 Effect of Package and Board Inductances 23
6.2 Limitations of Static I-V Models 25

CHAPTER 7: IEC 61000-4-2 ESD Testing 29
CHAPTER 8: CONCLUSION 34

8.1 Future Work 34

REFERENCES 36

CHAPTER 1: INTRODUCTION

1.1 Motivation

Electrostatic Discharge (ESD) occurs when a charged object discharges into another object. If the two objects are a person and an electronic device, a large current may flow through the device during the ESD event. The current happens for a brief period of time but tends to be quite large. If the current finds its way into a small integrated circuit (IC), it may damage or break the device [1].

Product manufacturers test the reliability of their devices before releasing them to consumers in order to ensure that the device can withstand the ESD that may occur. A common reliability test is the IEC 61000-4-2 standard. With this standard, system designers can test the reliability of their final products. However, if the final product does not pass the standard, the system designer must determine why the product failed and how to fix it. Due to the lack of information from IC manufacturers about their IC's ESD protection circuitry, system designers do not have an accurate way to simulate their product's response to ESD stress. Therefore, a system designer may take several iterations of testing and redesigning before a product passes the IEC 61000-4-2 standard.

System-Efficient ESD Design (SEED) [2, 3] is intended to increase the likelihood that an electronic product will pass system-level ESD qualification. The SEED methodology stipulates that transmission line pulse (TLP) measurements can be used to develop models of a microelectronic component's external pins (i.e., pins directly subjected to ESD stress). However, TLP was originally developed as a die-level measurement technique [4]. In contrast, microelectronics at the system-level are packaged and are required to have power applied for complete ESD characterization. When performing board-level TLP measurements, the parasitics associated with the package and board will alter the results relative to a die-level measurement. This thesis builds on previous efforts to extract SEED models of components using TLP measurements, e.g. [5, 6, 7, 8, 9], by developing a practical procedure to perform the required I-V measurements and ascertaining the limitations of TLP-based modeling.

1.2 Thesis Overview

In this work, the proper procedure and practicality of SEED will be evaluated. In Chapter 2, TLP, IEC 61000-4-2, and the fundamentals of SEED will be briefly discussed. In Chapter 3, an overview of the test board designed for this work will be discussed as well as the type of IO protection circuitry placed on the test chip. Chapter 4 will present TLP measurement results using the test chip and test board. In Chapter 5, I-V simulation results are given using the models derived from the TLP measurements in Chapter 4. Chapter 6 will move into transient simulation results using the same models. Finally, in Chapter 7, IEC 61000-4-2 simulation and measurement results will be present using the SEED models.

CHAPTER 2: PRIOR WORK

2.1 Transmission-Line Pulse Measurements

In order to understand the SEED methodology, it is important to first understand standard measurement techniques for ESD testing. One very common technique is called transmission-line pulsing (TLP) [4, 10]. A TLP tester creates a square current pulse by charging up a 50 Ω transmission line and releasing its stored charge into a device under test (DUT). A sample waveform measurement is shown in Figure 1. The width of the current pulse is equal to twice the propagation delay of the transmission line, which is proportional to the length of the line. A typical TLP is 100 ns wide; however, shorter pulses less than 10 ns are used in a technique referred to as very-fast TLP (VFTLP). The rise-time of the current pulse is usually adjusted with a rise-time filter. A typical rise-time for TLP is 10 ns and for VFTLP less than 1 ns is used. A quasi-static I-V curve can be constructed by pulsing the DUT with increasingly larger current pulses and then averaging over the quasi-static portion (i.e. the flat portion in Figure 1) of the measured current and voltage waveforms. In this work, the averaging window was between 60 ns and 80 ns after the rising edge for TLP measurements. TLP is a popular reliability measurement because it stresses the DUT for only a short period of time, thus preventing the DUT from overheating. This allows designers to test devices at very high current levels (i.e. current levels that may be seen during an ESD event) without prematurely damaging the device. TLP measurements will be the basis for the SEED models used in this study.

2.2 IEC 61000-4-2 Standard

Another important reliability test for system designers is the IEC 61000-4-2 testing standard [11]. The need for this standard stems from the fact that every time a consumer handles a product, charges are exchanged between them. Depending on where the consumer contacts the product, the current can damage or destroy the device. The IEC standard is a measure of how well a piece of equipment under test (EUT) can survive ESD stress during normal consumer operation. The IEC standard guides designers to discharge into points on the EUT where consumers may come into contact with their product. Example test points might be the touchscreen on a smart phone, the keyboard on a laptop computer, or a USB port.

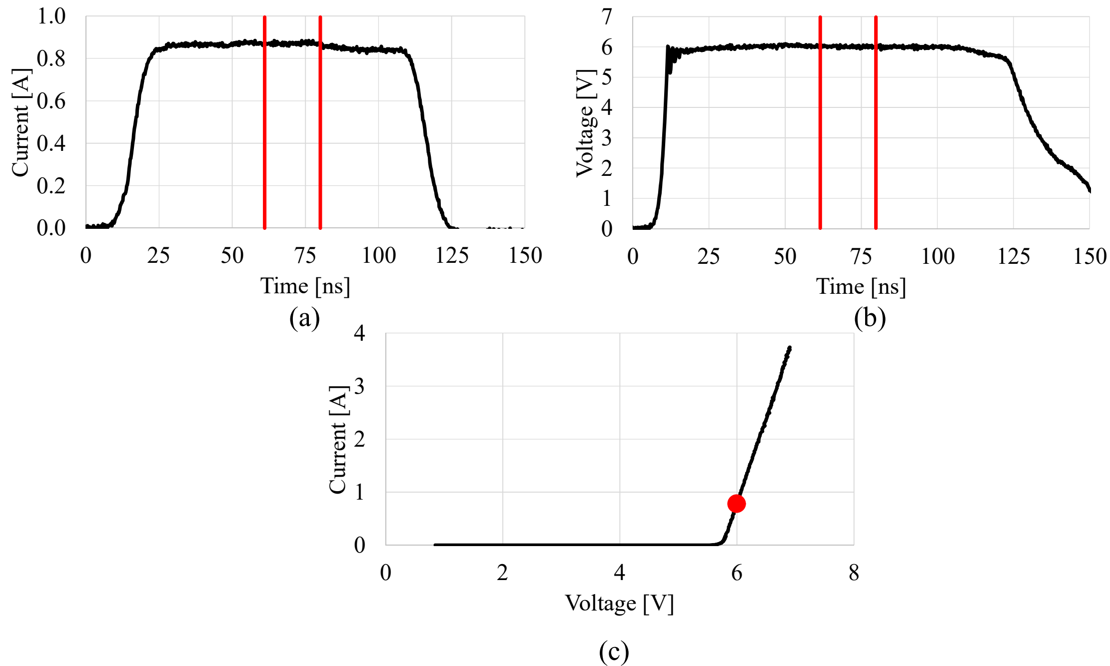

Figure 1: Sample TLP waveforms with 100 ns pulse-width and 10 ns rise-time for semiconductor DUT. Averaging windows are marked with red lines, and corresponding placement on I-V is marked as a red dot. (a) Typical current pulse from transmission line measured into the DUT. (b) Measured voltage across DUT. (c) Constructed quasi-static I-V from averaging TLP waveforms between 60 ns and 80 ns.

In this study, only IEC 61000-4-2 contact discharge was used. The test setup for contact discharge, shown in Figure 2, is comprised of a horizontal coupling plane (HCP), a sheet of insulator on which to place the EUT, and a charge source referred to as an "ESD gun." For contact discharge, the ESD gun can be pre-charged up to 8 kV. It is then brought into contact with the EUT and discharged. Although not necessary for the standard, current waveforms were measured for this study with a current probe around the ESD gun tip. The current waveform out of the gun tip has an initial fast-transient large amplitude peak followed by a slower, smaller second peak. An IEC 61000-4-2 waveform is shown in Figure 3.

If the EUT can survive ESD zaps of up to 8 kV, it may pass the standard. However, if the EUT fails, the system designer has to figure out why it failed and redesign a portion of the system to improve its reliability. This may take many iterations of testing and redesigning before a final product passes the IEC 61000-4-2 standard, costing both time and money. The goal of SEED is to bypass this cycle of testing and redesigning and instead provide designers with a quicker method of estimating how well a product will perform under test.

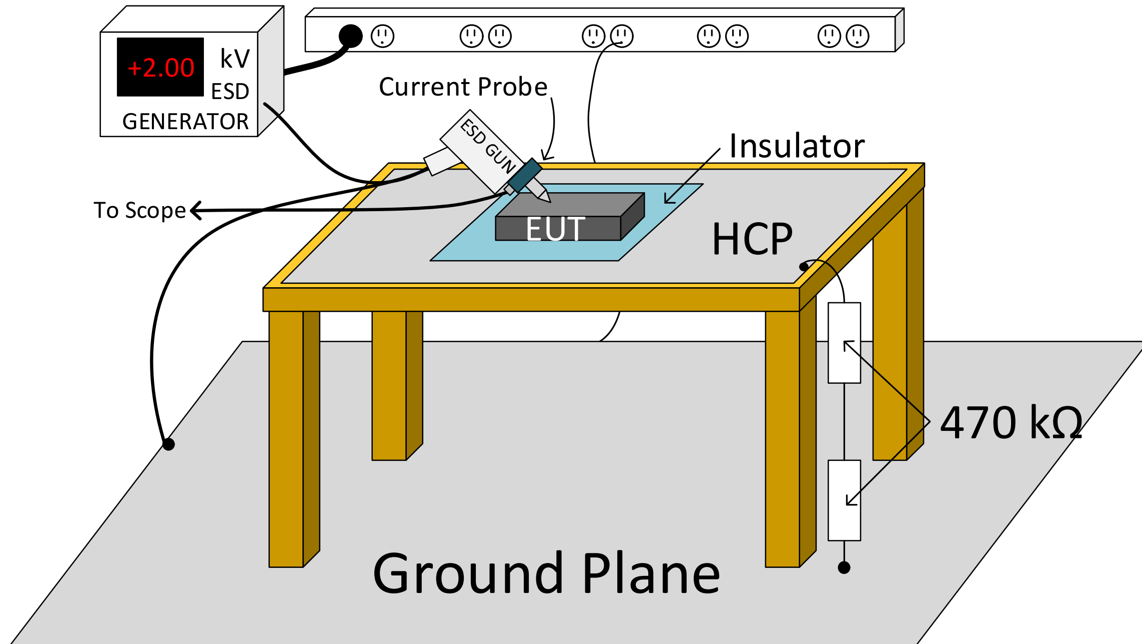

Figure 2: Test setup for the IEC 61000-4-2 standard. Standard includes an HCP connected to the ground plane through two 470 Ω series resistors to allow the HCP to slowly discharge in between zaps. An insulator separates the EUT from the HCP. An ESD generator supplies the charge to a test point on the EUT. Optionally, current can be measured via a current probe around the tip of the ESD gun. Figure courtesy of N. Thomson.

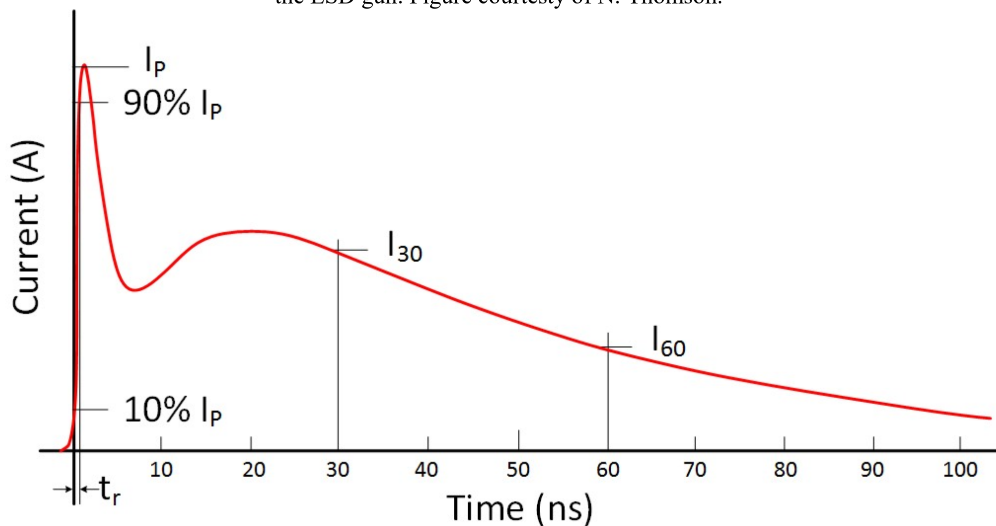

Figure 3: Discharge current waveform from the ESD gun into a 2 Ω target. Important values that are specified in the IEC 61000-4-2 standard are marked. I_P is the specified maximum current and t_r is the specified rise-time of the first peak. I_{30} and I_{60} are specified current values of the second peak at 30 ns and 60 ns, respectively. Figure courtesy of N. Thomson.

2.3 System-Efficient ESD Design

System-Efficient ESD Design (SEED) [2, 3] suggests that quasi-static TLP I-V measurements can be used to develop ESD models of chip IO pins to simulate a system's behavior during an IEC 61000-4-2 zap. The SEED methodology is intended to predict only hard failure in products rather than soft failures or data corruption. Not much detail is given about the proper methodology for extracting SEED models nor much about what beyond the SEED models is

important for system-level simulations. Previous work has been done comparing models from the SEED methodology to models based on datasheet information [12]. Additional efforts have explored the practicality of using quasi-static models in simulations involving the transient behavior of an IEC zap. SEED has been tested on a wide range of applications such as a CMOS inverter IC [5], an automotive voltage regulator [6], an automotive local interconnect network driver [7], a cell phone LED [8], and a USB interface [9]. These works use board-level TLP I-V measurements to create piecewise-linear (PWL) models for SEED with varying results. Mismatch between transient IEC 61000-4-2 simulation and measurement is often observed, undermining the benefit a system designer could get from using SEED. Improved accuracy has been found with the SEED methodology by adding high current and 3 GHz broadband models [13]. This work also stresses the importance of correctly modeling the complex return path that IEC current may take.

Work applying the SEED methodology to a different standard, the human metal model (HMM) test, has also found better results [14, 15]. These works attribute this largely to a strong correlation between HMM and TLP failure levels. They also go beyond the original SEED methodology by substituting wafer-level measurements of chip pins in SEED for board-level measurements of on-chip protection circuitry.

SEED focuses on modeling ESD protection devices and using those models in simulation. SEED does not explain whether or not models for the rest of the system (i.e. PCB traces, discrete components, and chip parasitics) are necessary. Using only quasi-static TLP measurements may lead to inaccuracies in transient simulations for both TLP and IEC waveforms. Additionally, SEED does not address how TLP measurements should be taken for a specific system component (i.e. a chip pin). TLP is traditionally a die-level measurement and it may not scale up to the system level. This work will focus providing a proper approach to using the SEED methodology and evaluating its practical use for system designers.

CHAPTER 3: OVERVIEW OF TEST SYSTEM

3.1 Test Board

A test board was developed for TLP characterization of the IO pins of the 130-nm CMOS test chip described in [16]. The test board had ports for connecting the TLP generator and an oscilloscope; it also had a means to supply power to the DUT (i.e. an IC or other microelectronic component). A socket fitted to 80-pin QFN packages was placed on the board to hold the DUT. This facilitated the testing of multiple DUTs, which was necessary if the DUT was accidentally damaged during testing or for monitoring part-to-part variability. SMA connectors were used to connect the TLP generator and oscilloscope to the board, as shown in Figure 4. On-board voltage regulators supplied power to the DUT; decoupling capacitors (decaps) were placed around the chip and at the voltage regulators to help maintain power integrity. To stabilize the voltage regulator's output, 10 µF was placed on board. In addition to the 10 µF for the voltage regulator, four sets of 100 pF (0402 packaging), 10 nF (0603 packaging), and 1 µF (0805 packaging) capacitors were placed around the chip. Decap around the chip may increase the chip's immunity to ESD stress as decap can provide a low impedance path to ground during an IEC 61000-4-2 zap. Various sized capacitors in various packages have different equivalent series resistance (ESR) and inductance (ESL). The ESR and ESL of a capacitor are dependent on its capacitance and its packaging. Larger capacitances and larger packages generally have larger ESR and ESL. Because of the ESL, each capacitor will have a resonant frequency. For frequencies below resonance, the impedance of the capacitor will decrease with frequency toward its ESR, as expected for a capacitor. Above resonance the impedance of the capacitor will increase with frequency as though it were an inductor. Having multiple capacitors connected in parallel, each with a different resonant frequency, allows the decap to maintain a low impedance across a broad range of frequencies. This is important for ESD immunity because ESD stress may have a wide range of frequency components. Decap is not solely used for reliability purposes. For the same reasons given above, decap is used to reduce ringing on supplies due to circuit switching in the IC. Therefore, it is common for decap to be found near an IC. The IO circuits were operated from a 3.3 V supply named VDDIO. Ideally, when developing SEED models, the amount of decoupling capacitance on the test board should be comparable to that used in the end-product, as it will be shown in Chapter 4 that this can affect the pin I-V characteristic.

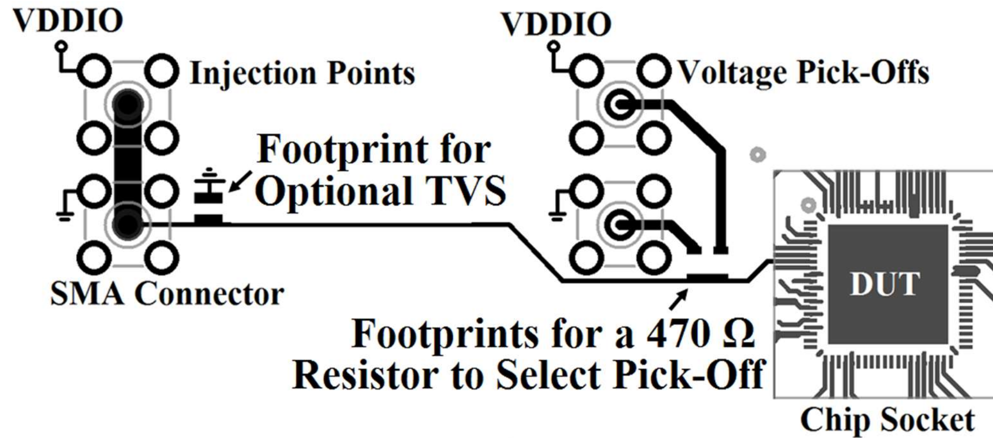

Figure 4: Trace used for delivering TLP pulses to a single IO pin. Figure is to scale.

For comprehensive characterization of a pin's I-V characteristic, the pulses could be applied with respect to board ground or to VDDIO, as indicated by the SMA connector's references. Figure 4 shows the configuration of an on-board pulse injection point. For measurements taken with respect to VDDIO, the board's VDDIO net became the test setup ground, and the board's "ground" plane was at a negative potential. Pins that are not intended to be characterized could be either left floating or tied to the board ground during testing. Control pins were used to set the IO-under-test to either input or output mode; when the pin was in output mode, a separate control pin was used to set it to either logic high or logic low. These control pins were tied to either VDDIO or ground on the test board.

The injected current was measured between the TLP generator and the SMA injection point by a current probe with sufficient bandwidth. The passband of the current probe covered the fundamental frequencies of the pulse-width and rise-time. Ideally, the lower (upper) 3-dB frequency of the passband should be an order of magnitude below (above) the relevant fundamental frequency. For example, for TLP with a pulse-width of 100 ns (10 MHz) and rise-time of 10 ns (100 MHz), the selected current probe should have a passband that extends from 1 MHz to 1 GHz. The CT-1 current probe was suitable for this study; its passband extends from 25 kHz up to 1 GHz.

A pick-off was used to measure the voltage at the DUT. An oscilloscope with a 50 Ω input was connected to the IO trace via the 470 Ω pick-off resistor; this gave a net resistance of 520 Ω in parallel with the DUT, which was deembedded from the measurement results. The voltage pick-offs were placed as close as possible to the test chip to minimize the delay between the incident and reflected pulses, as reflections can cause ringing which makes it difficult to accurately sample the quasi-static voltage. However, the footprint of the SMA connector places a lower-bound on

the spacing. To calibrate the voltage and current measurements, the on-board structures shown in Figure 5. Calibration structures were included on the test board. An open was used to find the shunt resistance, a Zener diode was used to calibrate the voltage measurements, and a resistive load was used to calibrate the current measurements. The calibration procedure used in this study is similar to the procedure presented in [17] and is summarized below.

Measured TLP voltage has the form:

$$V_{meas} = V_{DUT} \frac{R_{osc}}{R_{po} + R_{osc}} = \alpha_k V_{DUT}$$

where V_{meas} is the uncalibrated measured potential, V_{DUT} is the actual potential across the DUT (the desired measurement value), R_{osc} is the resistance of the oscilloscope channel, and R_{po} is the pick-off resistance (in this study 470 Ω was used). The coefficient α_k represents the voltage divider from R_{po} and R_{osc}. Since the Zener diode has a very precise holding-voltage that does not vary much with current, a TLP voltage measurement will have the form:

$$V_{meas} = \alpha_k V_Z$$

where V_Z is the Zener's holding-voltage. Since both V_{meas} and V_Z are known, α_k can be extracted. The DUT voltage can therefore be found:

$$V_{DUT} = \alpha_k^{-1} V_{meas}$$

Measured TLP current has the form:

$$I_{meas} = K_{CT}\left(I_{DUT} + \frac{V_{DUT}}{R_{shunt}}\right)$$

where I_{meas} is the uncalibrated measured current, I_{DUT} is the actual current into the DUT, V_{DUT} is the potential across the DUT, R_{shunt} is all resistance that may be in parallel with the DUT (in this study R_{shunt} is the series combination of R_{po} and R_{osc}), and K_{CT} is the scaling factor from the CT-1 current probe. During an open measurement, there is no DUT current. The measured current has the form:

$$I_{meas} = \frac{\mathrm{K_{CT}} V_{open}}{R_{shun}}$$

where V_{open} is the measured open potential. Both I_{meas} and V_{open} are known and K_{CT}/R_{shunt} can be extracted:

$$K_{CT} I_{DUT} = I_{meas} - \frac{K_{CT} V_{DUT}}{R_{shunt}}$$

To find the value of I_{DUT}, a third measurement using a resistive load is needed. A resistive load measurement has the form:

$$V_{DUT} = \frac{R_{DUT}}{K_{CT}}\left(I_{meas} - \frac{K_{CT}V_{DUT}}{R_{shu}}\right)$$

Since V_{DUT}, I_{meas}, R_{DUT}, and R_{shun} are all known, K_{CT} can be extracted. The DUT current can be found:

$$I_{DUT} = K_{CT}^{-1}\left(I_{meas} - \frac{K_{CT}V_{DUT}}{R_{shunt}}\right)$$

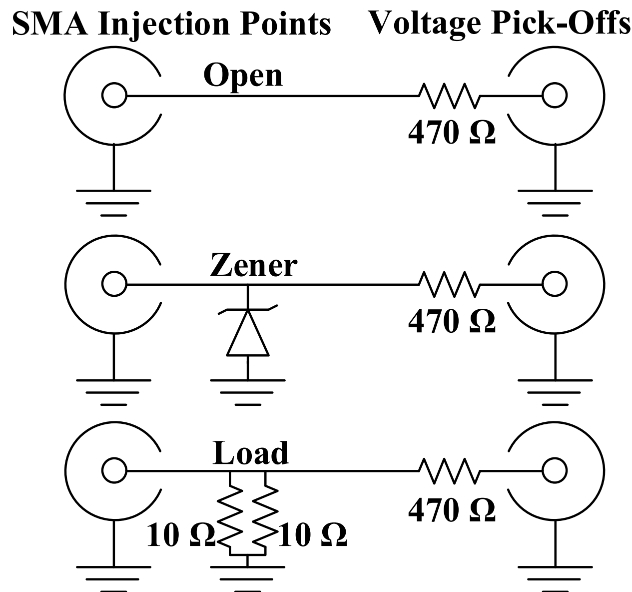

Figure 5: Open, Zener, and Load calibration structures. Note that a 5 Ω resistive calibration load was used in this study because it was on the order of expected resistances in test structure.

3.2 Test Chip Protection Circuitry

System designers often buy off-the-shelf components with protected IP for their products. Therefore, modeling a system during ESD can be difficult for designers because they do not often know what ESD protection a chip may have. However, two very common protection circuits used on chips are dual-diode pairs and silicon controlled rectifiers (SCR). The test chip used for this study contains pins with dual-diode protection and pins with SCR protection [16].

Dual-diode protection consists of an “up diode” and a “down diode.” These diodes connect an IO to the on-chip power buses. The up diode connects the IO to the on-chip VDDIO while the down diode connects it to the on-chip VSSIO, as shown in Figure 6. During an ESD event,

excessive current may enter or leave an IO, forward-biasing one of the diodes. The diode will shunt the ESD stress away from the core circuitry to the on-chip supply busses. The excess current, shown in Figure 6, can return to board ground safely through the chip pins, on-chip rail clamp, and decoupling capacitance placed around the chip.

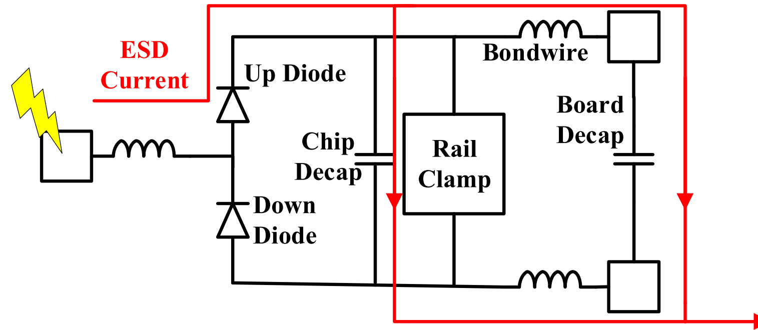

Figure 6: Circuit layout showing only ESD protection and chip bond wires for a dual-diode protected pin. Current shown is for positive ESD current into a chip pin's IO.

An SCR is a semiconductor device with a PNPN structure. It is often modeled as a pair of cross-coupled bipolar junction transistors, a PNP and an NPN. For the test chip used in this study, IO pins were protected by a diode-triggered SCR (DTSCR), shown in Figure 7, placed between the IO pin and the on-chip VSSIO. While the voltage from the anode to the cathode of the DTSCR is below four diode drops, the PNP and NPN will remain in cutoff. In other words, the DTSCR will have a large impedance and should not affect the normal operation of the IO pin. If the anode to cathode voltage further increases, the PNP will become forward active and begin to conduct collector current. Once the PNP's collector current is large enough to produce a voltage across the internal semiconductor resistance, R_P, large enough to forward bias the base-emitter junction of the NPN, the NPN will become forward active. When both transistors are forward active, their cross-coupled configuration will cause them to push each other toward saturation, given large enough current gain. At this point, the DTSCR will conduct more current at a lower voltage. This transition is referred to as "snapback," and the DTSCR will have a negative differential resistance region in its I-V curve, which can be seen in Figure 8, as it moves from its triggering current and voltage to its holding current and voltage. Once the SCR has snapped back, it will behave like a conductor with resistance, R_{on}. The DTSCR should be designed to only trigger during an ESD event at which point it will shunt the excess current to the on-chip ground bus to protect IO circuitry. Again, the shunted current can safely return to board ground through chip pins, the on-chip rail clamp, and decap around the chip. The SCR will remain in a low impedance state while

its current and voltage are above their holding points. Once enough charge is shunted the voltage and current will fall below the holding points and the SCR will return to its initial high impedance state.

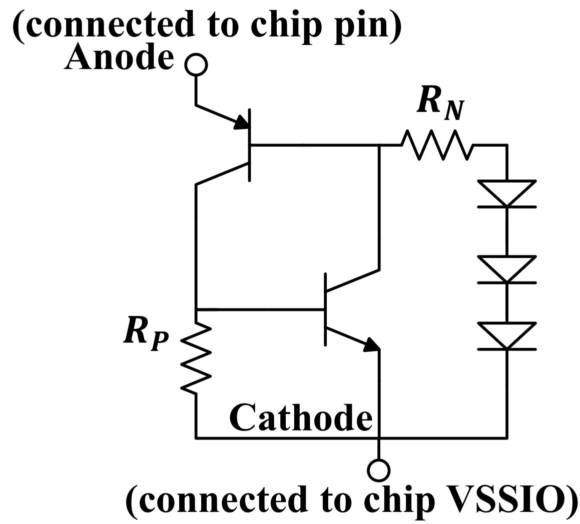

Figure 7: Circuit representation of a DTSCR. The values R_N and R_P come from the intrinsic resistances of the NWELL and PWELL of the SCR, respectively.

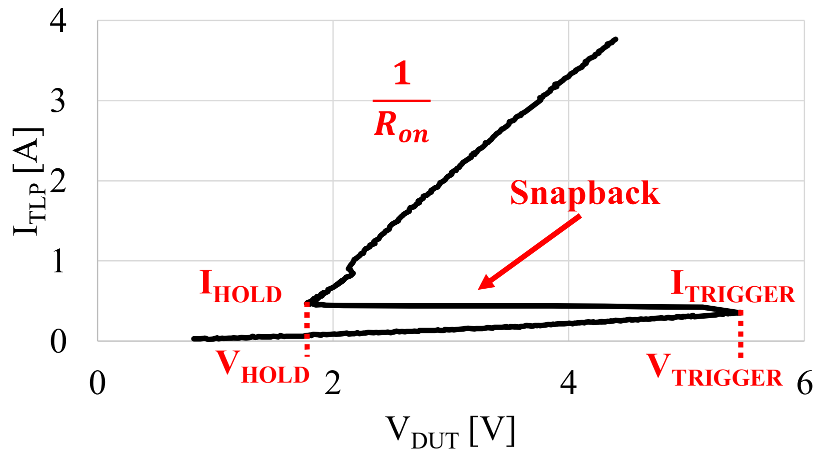

Figure 8: Sample TLP I-V of DTSCR device in 130-nm. Trigger and holding values are shown. Once the SCR is triggered, it snaps back to its holding voltage and has a resistance, R_{on}.

CHAPTER 4: TLP MEASUREMENTS

System-level TLP measurements were performed using pulses with a 100 ns duration and 10 ns rise-time. The initial measurements were performed without the experimenter's knowledge of the details of the test-chip. Only such working information that would be found in a datasheet was shared. This was to ensure that prior knowledge did not bias the experimenter's findings.

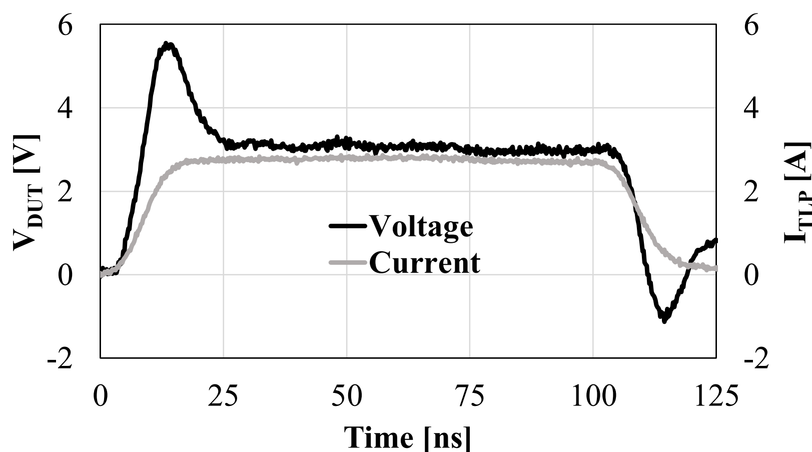

Figure 9: Transient response for a 3 A TLP pulse. Voltage measured at pick-off near the IO pin.

Sample current and voltage waveforms are shown in Figure 9. To generate an I-V point, the average values of current and voltage over the interval between 60 ns and 80 ns after the rising edge are used. The duration of the voltage overshoot in Figure 9 is too long and its amplitude too high to be caused by the on-chip protection's turn-on dynamics; as evidence, a 3 A die-level TLP measurement, with a shorter pulse rise-time of 1 ns, causes only a 250 mV overshoot. Instead, the overshoot is attributed to the package bond wire and board trace inductances. Rough calculations support this assertion: given a 10% to 90% rise-time di/dt of (0.8*3 A)/(10 ns), a package inductance of 6 nH, and a board trace inductance of 4 nH, the associated voltage overshoot is expected to be about 2.4 V. In Figure 9, the measured overshoot is about 2.5 V, close to the estimated value.

4.1 Power-On vs. Power-Off Response

System-level ESD testing is generally performed in both power-off and power-on conditions, perhaps requiring the pin model to be extracted in both the power-off and power-on states. References [2, 3] do not provide definitive instructions on this point. In this work, TLP measurements were taken with the chip powered-on and powered-off. The two resulting I-V

characteristics for test chip IO pin #3 ("IO3") are compared in Figure 10; these measurements were performed with respect to the board ground. When the chip is powered on, the I-V curve is offset by 3.3 V relative to the power-off case, the value of VDDIO. This finding suggests that the protection circuit shunts the current to VDDIO. The on-resistance values for the two curves are virtually the same. Similar results were found in [18].

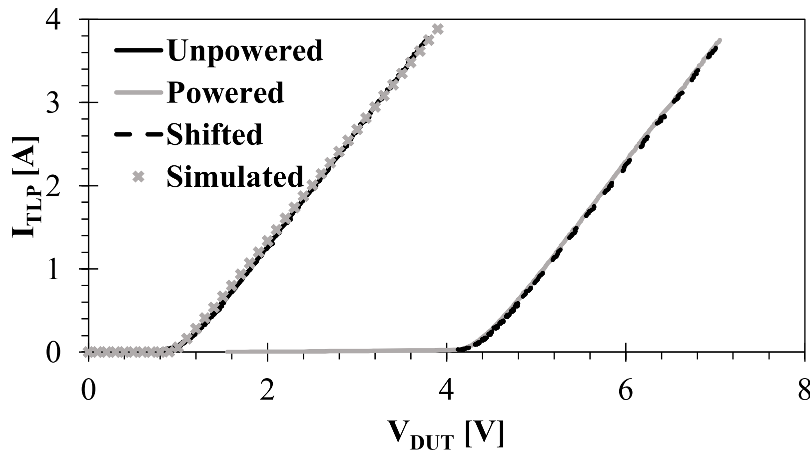

Figure 10: TLP I-V for IO3 measured w.r.t. board ground. The curve labeled "Shifted" is the off-state I-V curve shifted right by 3.3 V.

A markedly different result is obtained for IO pin #4 ("IO4"), as seen in Figure 11. Here, the I-V characteristic is similar in both the powered and unpowered states. As this measurement was performed with respect to board ground, it can be surmised that IO4 is protected by a local clamp referenced to the on-chip VSSIO bus. It is observed that at pin voltages less than the clamp's trigger voltage, more current is sunk in the power-off state than in the power-on state. After gaining access to the design schematic, it was found that the drain-body diode of the PMOS output driver provides a secondary path for the ESD current. However, when the power is on, VDDIO elevates the diode cathode (body of the PMOS) voltage to 3.3 V, keeping the diode off until well after the local clamp triggers on.

For this chip, a simpler behavioral model may be used to describe IO3 than IO4, as the latter shows snapback. IO3 may be represented by a very simple (two branch) piecewise-linear (PWL) model; in this work, it is modeled as a voltage source and a diode with an empirical value for its on-resistance.

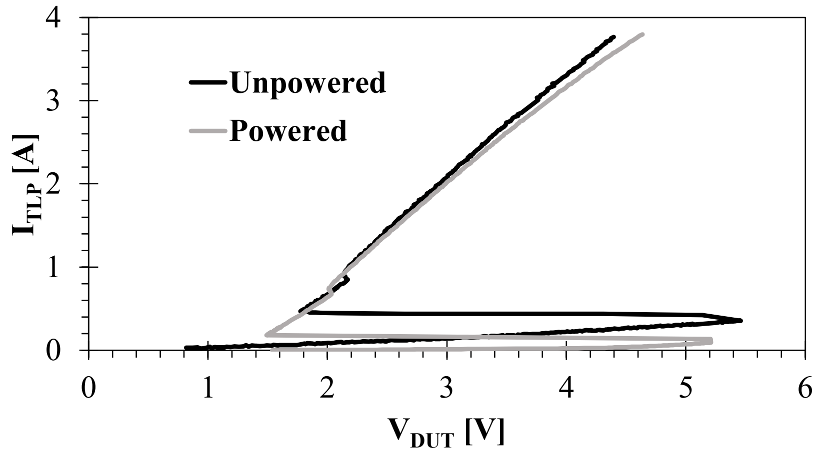

Figure 11: TLP I-V for IO4 pin measured w.r.t. board ground.

4.2 Effect of Reference Bus

The pin model should describe conduction from the pin to ground and from the pin to the supply (VDDIO in this case). Therefore, complete TLP characterization will involve injecting pulses with respect to both board ground and VDDIO. For this test chip, the two sets of I-V curves are nearly identical; sample results, obtained in the power-off state, are shown in Figure 12. The similar appearance of the two I-V curves indicates that the injected TLP current bypasses the on-chip rail clamp, with the on-board decoupling capacitors providing the dominant current path on the TLP time scale; a similar finding was presented in [19].

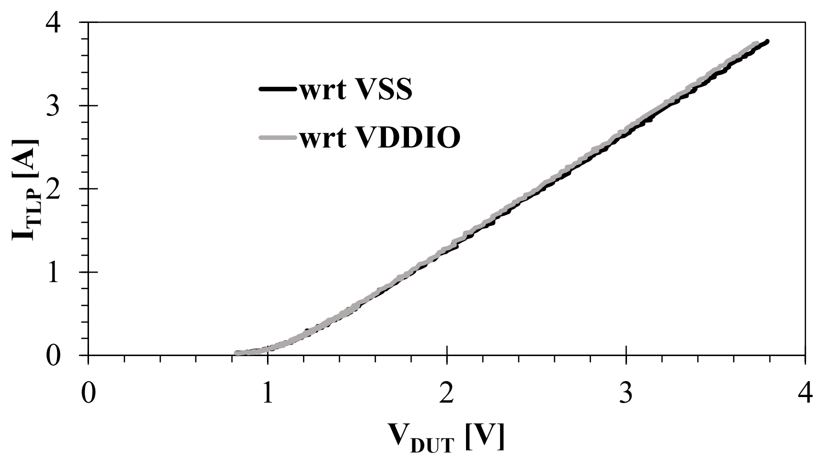

Figure 12: TLP measurement is performed between IO pin and board ground, and between IO pin and VDDIO.

4.3 Effect of Decoupling Capacitance

Product circuit boards may contain significant decoupling capacitance near each IC component. However, it is not guaranteed that all ESD test boards will have as much decoupling

capacitance as the one used in this work, it is important to investigate whether the measurement results are sensitive to the amount of on-board decoupling capacitance. The TLP measurements were repeated but without having decoupling capacitors placed around the chip. The required 10 μF of decoupling capacitance for the on-board voltage-regulator to operate properly was also removed; however, only power-off measurements were taken, so the stability of the voltage-regulator was not a concern. The results are shown in Figure 13. As noted previously, when decoupling capacitors are placed near the chip, they short the TLP current from VDDIO to board ground. However, when the capacitors are removed, the injected current must travel through the on-chip rail clamp to get from VDDIO to ground. The voltage offset between the two I-V curves in Figure 13, approximately 0.5 V, is a measure of the trigger voltage for the on-chip rail-clamp [20]. Clearly, the amount of decoupling capacitance affects the TLP I-V measurement, and the information needed to characterize the chip's pins in a low capacitance environment is obscured when the I-V is measured on a test board with enough decoupling capacitance.

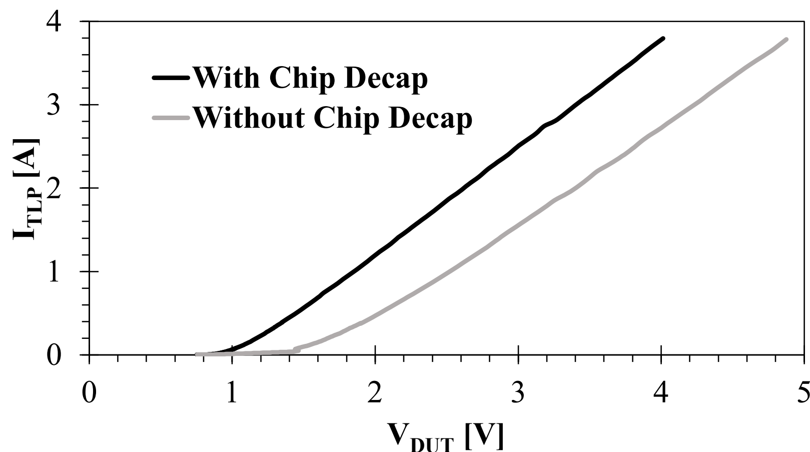

Figure 13: TLP I-V for IO3 pin w.r.t. board ground with and without on-board decoupling capacitors near the chip. Board is unpowered.

4.4 Effect of Pin Bias

Plausibly, a pin's TLP I-V may change based on how the IO is configured [3]. For example, an IO might have different behavior if it is configured as a high output, a low output, or an input. Furthermore, many of the chip pins will not need to be accessed during the TLP testing, i.e., only the external pins and their control pins and the supply pins will be utilized; the other "internal" signal pins might be left floating, or might be tied low or tied high. The SEED methodology, as

outlined in [3], does not specify how the chip should be configured on board or in software; such decisions are left to the person applying the methodology.

To gain insight as to whether the I-V is sensitive to the IO and chip configuration during test, TLP measurements were performed with the chip in a variety of different configurations. The signal pins undergoing characterization are referred to as the target pins; pins other than supply or control pins are called the untargeted pins. The chip's control pins could be tied low, tied high or left floating at the board level; note that if the control pins are left floating, the IO at the target pin is in an undefined state. The untargeted pins could be tied low or left floating. TLP measurements were performed for the following four cases.

i. The control pins and untargeted pins are floating.
ii. Target pin is in receive mode; untargeted pins are tied to board ground.
iii. Target pin is in transmit mode, with its output set low; untargeted pins are tied to board ground.
iv. Target pin is in transmit mode, with its output set high; untargeted pins are tied to board ground.

The measurement results will address two questions. First, does the state of the driver at the target pin significantly affect the TLP I-V? Second, do the additional current paths provided by grounded untargeted pins noticeably affect the TLP results?

The obtained I-V curves are shown in Figure 14 and Figure 15, with the former showing only the low-current I-V. The effects of the pin bias are most noticeable at low current levels (Figure 14); for example, when the pin is transmitting a low, the NMOS driver can carry some of the ESD current. In the "Transmit High" case, it is expected that at 3.3 V (VDDIO), the measured current entering the pin should be zero, but this is not seen in Figure 8. The current probe has a limited bandwidth and cannot measure DC current. Thus, the measured current is missing the DC component, and the associated error is noticeable at low current levels. At higher current levels, the I-V characteristic (Figure 15) has a negligible dependence on the target pin's configuration. Furthermore, a comparison of the I-V curve for case (i) with those obtained in the other cases, shows that the untargeted pins do not provide significant paths for the ESD current. These findings might be particular to the test chip used in this study.

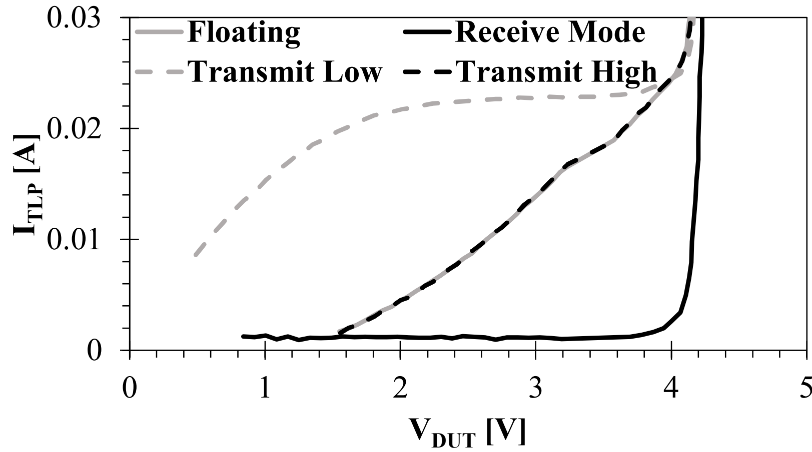

Figure 14: Pulse I-V characteristics of IO3 pin w.r.t. board ground. Floating corresponds to case (i). Receive Mode corresponds to case (ii). Transmit Low corresponds to case (iii). Transmit High corresponds to case (iv). Board is powered.

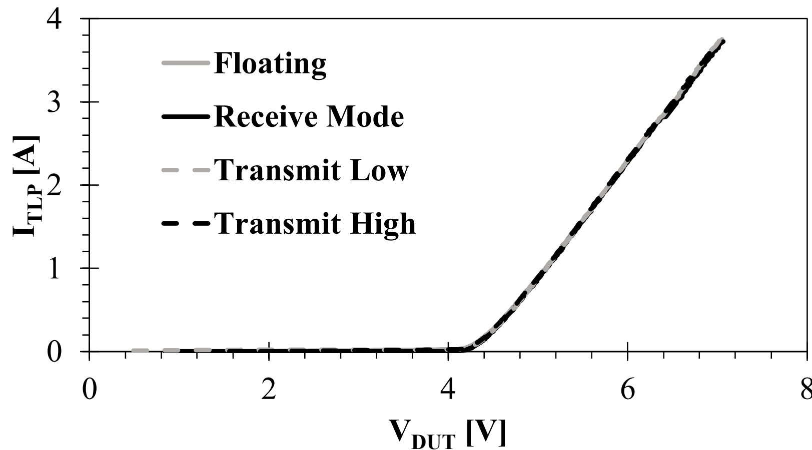

Figure 15: Same as previous figure, but with the curves extended to high current levels.

4.5 Die-Level vs. Board-Level TLP

If provided, a system designer could use the pin model generated by the IC designer. Presumably, models provided by the IC designer would be based on die-level measurement data or layout circuit simulations. To quantify the difference between die-level and board-level measurements, the I-V for IO3 is used as an example. This pin is known to have dual-diode protection. Figure 16 compares the I-V curve obtained using board-level TLP with that obtained from die-level measurement of a dual-diode test structure. For the board-level measurements, the chip was unpowered and configured with all of its pins floating. The I-V curve obtained from the board-level measurement exhibits much greater on-resistance; this is attributed to the package resistances as well as additional resistance from the on-chip supply nets and on-board traces. The IC manufacturer would need to extract the supply net resistance and incorporate it into the model

to provide a more reasonable representation of the pin's I-V. This may prove to be challenging as the results shown in Section 4.3 indicate that external components may change the current path through the supply net, which will affect the pin's single-port I-V model. A multi-port I-V model may need to be adopted in order to capture the external components' effect on the current path through the supply net.

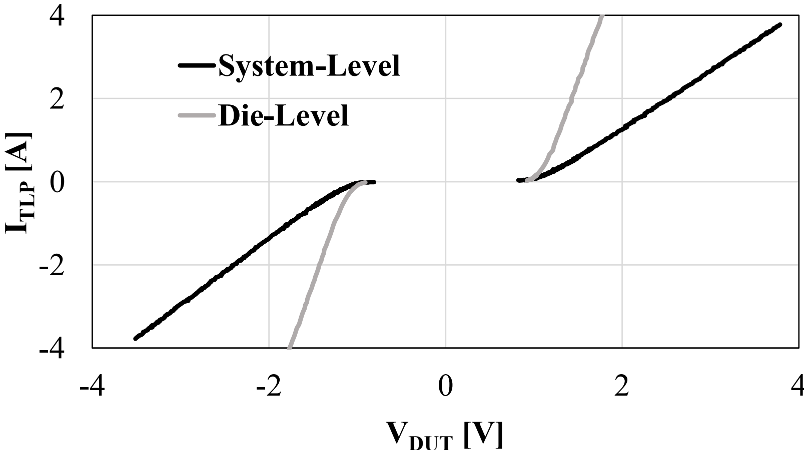

Figure 16: Pulsed I-V from die-level and board-level TLP measurements.

CHAPTER 5: I-V SIMULATION RESULTS

SEED is intended to allow a system designer to design the ESD protection for a product by using simulation, rather than having to build and test multiple prototypes. In this chapter, it is investigated whether component models extracted from TLP I-V data can be used and combined to accurately simulate I-V curves measured on a test board. Toward this end, the trace leading to IO3 is simulated both with and without an 80 pF transient voltage suppressor (TVS). The schematic for these simulations is shown in Figure 17. As noted earlier, the I-V characteristic for IO3 is represented by a pair of diodes, whose parameters are extracted from the data shown in Figure 10. The package model in Figure 17 is provided by the package manufacturer. The board signal traces are modeled as transmission lines with characteristic impedances calculated from the physical trace dimensions. Since TLP I-V data includes resistance between the active device and pick-off, this resistance must be de-embedded from the transmission line model. The TLP tester is represented by a pulse source with 50 Ω output impedance that is followed by a rise-time filter [21]. Simulations are performed using the Advanced Design System (ADS) software [22]. However, to generate the I-V characteristic, a DC simulation may be used in lieu of an actual (transient) TLP simulation, since the TLP I-V is measured well after the transients have died down, i.e., when the system has entered a quasi-static state. The simulated I-V of IO3 is plotted in Figure 10 and there is a close match between the measured TLP I-V and the simulated DC I-V.

Prior to placing a TVS on the signal line to IO3, TLP testing was used to obtain the I-V characteristic of the TVS. To perform the I-V measurement, a TVS was mounted on a separate trace that is similar to the middle structure shown in Figure 5. The pulsed I-V measurement data as well as the simulated I-V are shown in Figure 18. Next, simulation was used to predict how the I-V measured at IO3 would change if a TVS was mounted on the IO3 trace. Figure 17 shows that the TVS is added to the simulation model in a manner that emulates its physical placement near the TLP injection point on the IO3 trace (Figure 4).

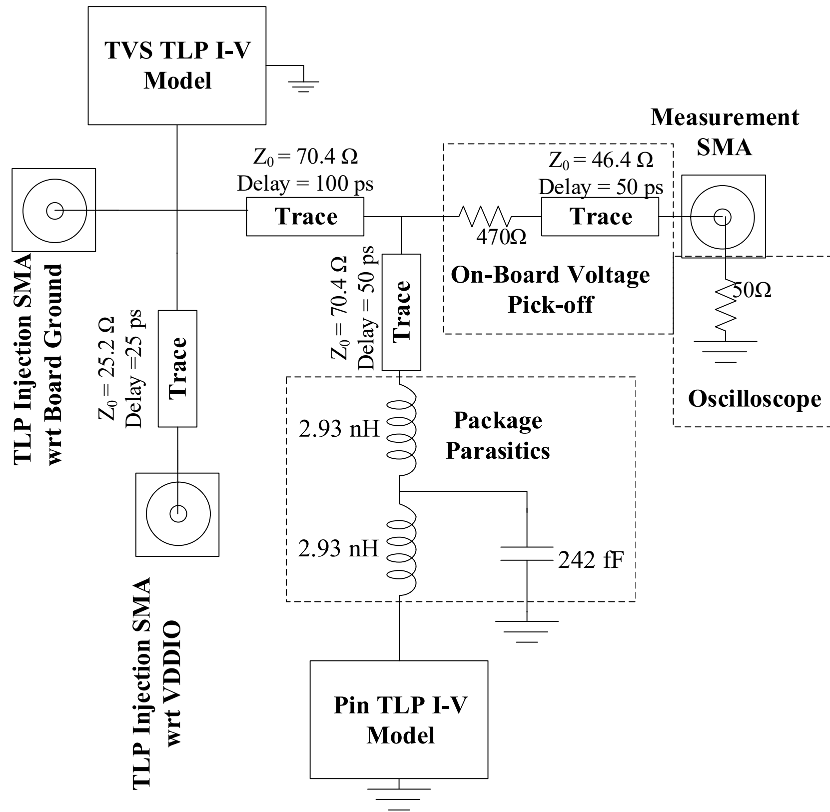

Figure 17: SEED-type model of test board and IO pin. This model was simulated in ADS.

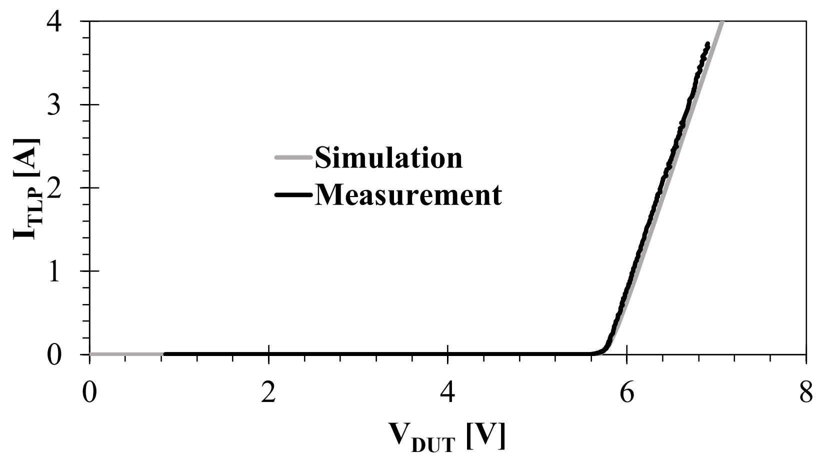

Figure 18: Measured pulse I-V characteristic and DC simulation of the TVS.

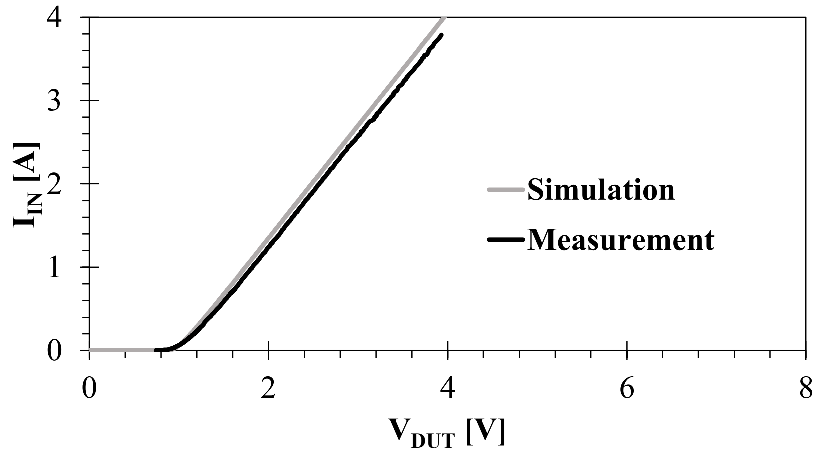

Figure 19: Measured TLP I-V and DC simulated I-V for IO3 trace with TVS. Board power is off.

Simulations of the TVS-protected trace are performed for both the unpowered and powered-on cases; the results are shown in Figure 13 and Figure 14, respectively. In both cases, the simulated (DC) I-V curve well represents the I-V obtained from TLP measurement. A comparison of Figure 19 with Figure 10 shows that, in the unpowered state, the on-chip protection carries all of the ESD current, apparently because it clamps the voltage on the signal line below the trigger voltage of the TVS. However, the TVS does turn on if the chip is powered, as shown in Figure 20, because the on-chip protection's I-V is shifted to higher voltages, as was seen in Figure 10. For this design, the on-chip protection is required to safely handle a larger ESD current in the power-off state than in the power-on.

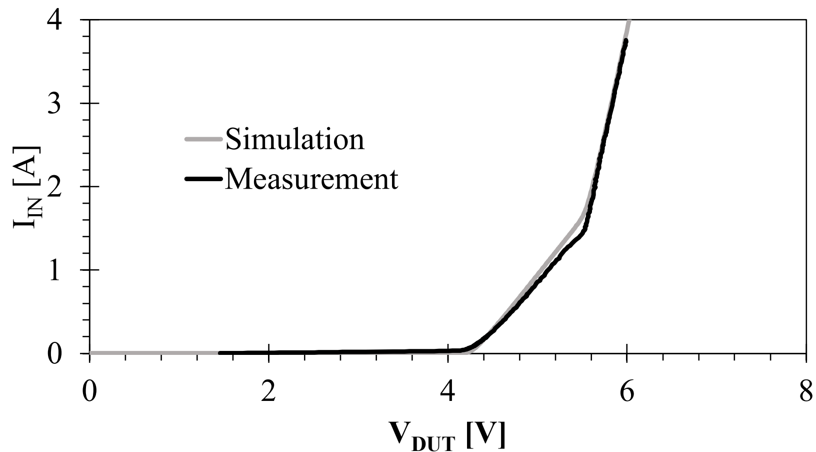

Figure 20: Measured TLP I-V and DC simulated I-V for IO3 trace with TVS. Board power in on.

CHAPTER 6: SYSTEM TRANSIENT RESPONSE

In [2, 3] it is suggested that TLP I-V models be developed for the IC pins and TVS devices; Chapter 5 verified that this approach results in accurate quasi-static simulations. This chapter explores to what extent these "SEED models" can reproduce measured transients. The results will highlight some limitations of board-level TLP characterization.

6.1 Effect of Package and Board Inductances

Transient simulation of a 1 A TLP pulse at IO3 was performed using the schematic shown in Figure 17. The results are shown in Figure 21 and Figure 22, for the case that the chip is unpowered and not protected by a TVS. Figure 15 shows the current pulse and Figure 16 shows the voltage waveform measured at the pick-off near the IO3 pin. The large initial overshoot seen in Figure 22 is caused by the chip's package parasitics and reflections at discontinuities on the board trace. The overshoot is replicated in simulation with some degree of accuracy, due to the schematic having included the package inductances and transmission line models for the board traces.

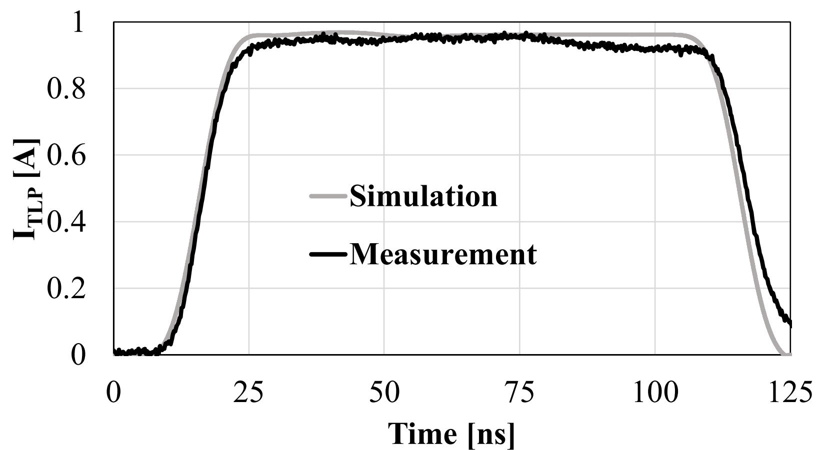

Figure 21: Simulated and measured current of 1 A TLP to IO3.

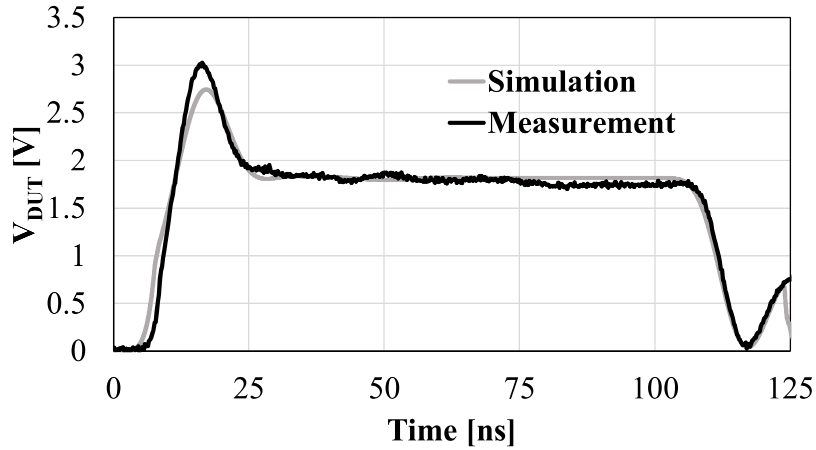

Figure 22: Simulated and measured voltage for a 1 A TLP to IO3.

It has been suggested that very fast TLP (VFTLP) measurements may be additionally useful for SEED [3]. However, transient effects caused by the traces and package parasitics can prevent the system from achieving a quasi-static state during a few-nanosecond long VFTLP measurement, eliminating it as a useful I-V measurement technique; these transients are exacerbated by the short rise-times used for VFTLP. The VFTLP measurement result shown in Figure 23 supports these assertions. A VFTLP pulse with 600 ps rise-time and 5 ns duration was applied to the IO3 trace with a setup otherwise identical to that for Figure 16. Clearly, the voltage pulse shown in Figure 17 does not reach a quasi-static state. The observed ringing is caused by reflected waves along the board trace between the voltage pick-off and the chip pin. It is further noted that the system parasitics place a lower limit on the pulse width that may be used for a safe operating area characterization [23].

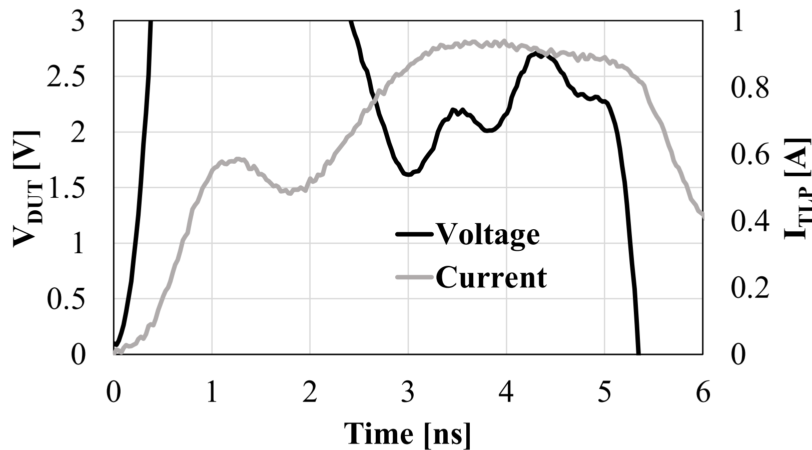

Figure 23: Measured response of IO3 to a VFTLP injection. The pulse has a 5 ns width and a 600 ps rise-time filter is used.

6.2 Limitations of Static I-V Models

In Section 6.1, it was found that the transient response of an IO pin to a TLP current pulse can be simulated with reasonably good accuracy. However, this does not guarantee that an accurate transient simulation will be obtained for more complicated systems. To assess the extent to which SEED models can reliably reproduce measured transients, TLP simulations will be performed for the case that a TVS is included on the trace shown in Figure 4.

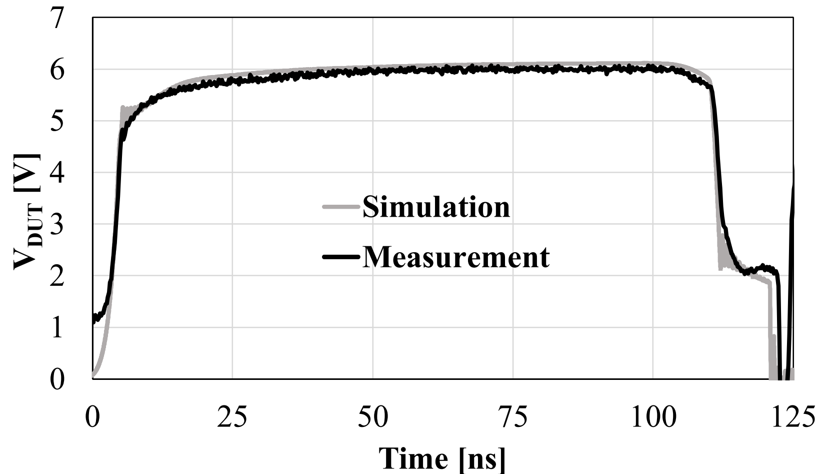

Figure 24: Simulated and measured voltage of 4 A TLP to TVS and chip pin with board powered.

As before, the schematic being simulated is the one shown in Figure 17. In the first simulation, a 4 A TLP current pulse was injected into the IO3 trace with the board powered-on; from Figure 20, it is known that the TVS will turn on at 5.6 V. Figure 24 provides a comparison of the simulated voltage response at IO3 with the measured response. No voltage overshoot is observed, so it is concluded that the TVS suppresses this transient. Simulation and measurement agree well, indicating that simulations which use TLP-based I-V models can reproduce most of the features of the measured waveforms. However, initially there is a 1 V offset between the measured and simulated waveforms. During the measurement, the chip pin was configured to output logic high. The output driver is not accounted for in simulation, so the logic high output does not appear in simulation. Interestingly, when I_{TLP} = 0 A (at Time = 0 s) in measurement, the driver does not raise the pin voltage all the way to 3.3 V (VDDIO) because the chip's driver is too small to drive the 50 Ω load presented by the TLP system all the way to VDDIO. As shown in the measured waveform, the pin voltage only reaches about 1 V.

Next, a 3 A TLP pulse is simulated; in this case, the board is not powered-on and a 1 ns rise time filter is substituted for the usual 10 ns filter. The measured and simulated voltage

waveforms are shown in Figure 25. In both measurement and simulation, the voltage is observed to drop at about 30 ns. This finding can be explained using the equivalent schematic shown in Figure 26. The TVS turns on initially, since the transient voltage overshoot at the chip, shown in Figure 3, is large enough to trigger on the TVS. Both the TVS and the on-chip protection clamp to different on-voltages; so, the inductance associated with the trace and bond wire has a fixed voltage drop across it due to the on-voltage for the TVS being greater than that for the on-chip protection. Because of this fixed voltage drop, the current to the chip will increase linearly with time until the TVS turns off. During the time that the current into the chip is increasing, the resistive voltage drop across the on-chip ESD diode increases, an effect that is seen in both measurement and simulation from about 5 to 30 ns. When the TVS turns off, the current to the chip becomes constant, so the voltage drop across the trace inductance drops from its previous fixed value to zero. This causes the voltage drop at 30 ns. The simulated current into the chip and the TVS, shown in Figure 27, confirms the explanation of the voltage waveform; the current is observed to transition linearly from the TVS to the chip, and the voltage drop occurs in simulation at the same time as the current in the TVS reaches zero. After this occurrence, reflections in the traces cause the small ripples in the voltage waveform.

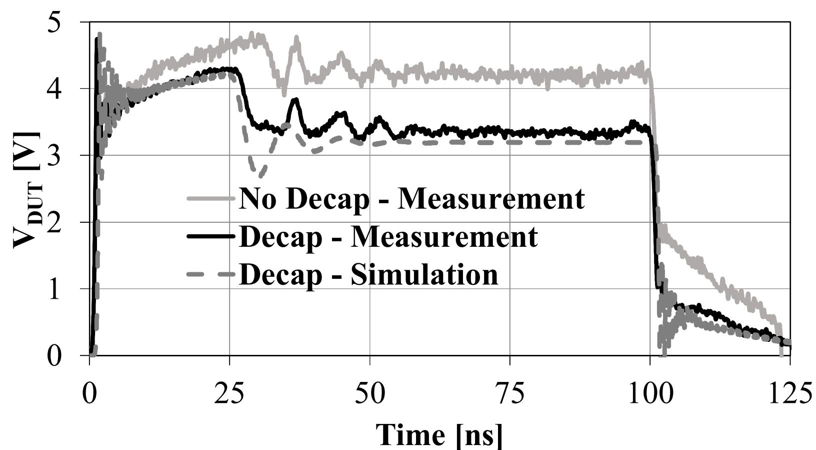

Figure 25: Simulated and measured voltage waveforms at IO3 during a 3 A, 1 ns rise-time TLP pulse when the chip is unpowered. Also plotted is the measured voltage waveform obtained when the board-level ceramic decoupling capacitors are removed.

The same 3 A TLP measurement was repeated, but with the on-board ceramic decoupling capacitors that are normally located at the chip removed; however, the large electrolytic decoupling capacitor near the voltage regulator remained. This result, labeled “No Decap,” is also plotted in Figure 19. The voltage measured at the pin is increased relative to when the board is

populated with all of its decoupling capacitors; also, the voltage step occurs at a slightly later time point. The schematic shown in Figure 26 provides an explanation for these results. Without the local decoupling capacitance, the current into the IO pin returns to ground through the rail clamp and L_{SS}. With the local decoupling capacitance, the current returns through L_{DD}, which is not identical to L_{SS}. Because L_{DD} and L_{SS} are unequal, the rate at which the current transitions between the TVS and the chip is different in these two cases and the voltage step occurs at different times. After the step, the voltage across the chip is higher in the "No Decap" case; this is due to the extra voltage drop across the rail clamp.

The measured results presented in Figure 19 highlight two shortcomings of the model in Figure 11. First, lumping all of the package parasitics at the IO only works if the on-board decoupling capacitance has a fixed value in all applications. Second, the TLP I-V model of the IC pin does not include the rail clamp, yet this element may play a role depending on the board design. In short, a naïve representation of the IC supply net may lead to erroneous simulation results.

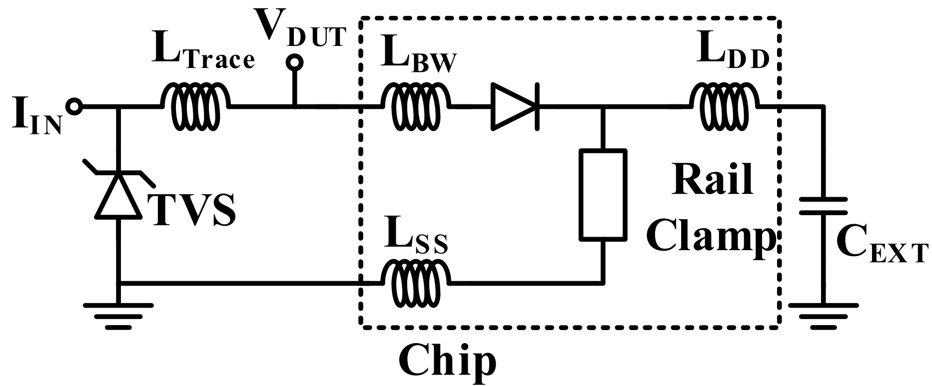

Figure 26: Simplified schematic of the discharge path; there is a TVS on the signal line and an off-chip decoupling capacitance.

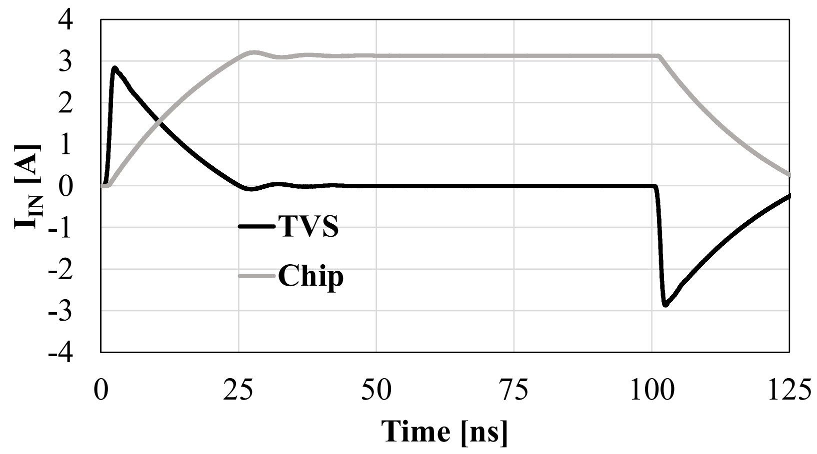

Figure 27: Simulated current waveforms into the TVS and chip during a 3 A, 1 ns rise-time TLP pulse; the chip is unpowered. The current into the TVS decreases linearly until it turns off.

CHAPTER 7: IEC 61000-4-2 ESD Testing

System designers ultimately need to qualify their design using an IEC 61000-4-2 or other system-level ESD test. As noted earlier, SEED is intended to allow a system designer to design the ESD protection for a product by using simulation, rather than having to build and test multiple prototypes. It is therefore necessary to evaluate whether “SEED models” can be used to accurately simulate a system’s response to IEC 61000-4-2 discharges rather than just TLP. The schematic of Figure 11 is again used to represent the system-under-test but the TLP tester model is replaced by the ESD gun model described in [24].

The first case to be considered is an ESD gun zap to the IO3 trace without a TVS and with the power off. A comparison of the measured and simulated waveforms can be seen in Figure 28 and Figure 29. While the simulated current in Figure 28 matches the measured current reasonably well, the simulated and measured voltage waveforms show significant mismatch in Figure 29. This may be due, in part, to having not modeled the oscilloscope input capacitance which, in series with the pick-off, forms a low pass filter that removes some high frequency components from the waveform.

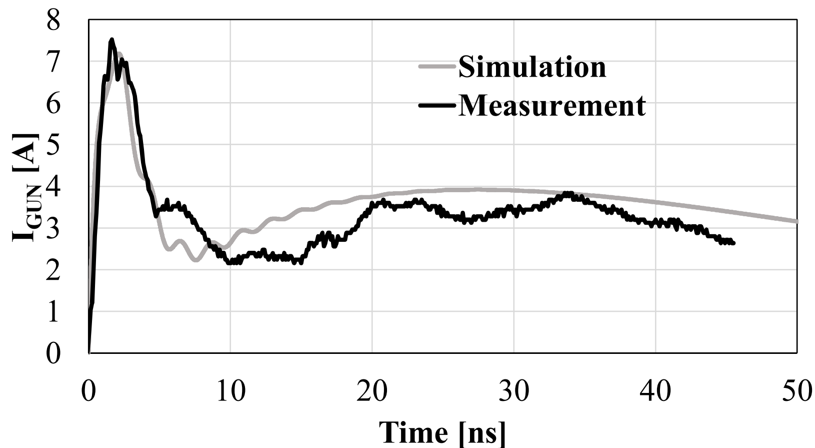

Figure 28: Simulated and measured current from 2 kV IEC gun zap to chip on board (trace leading to IO pin #3).

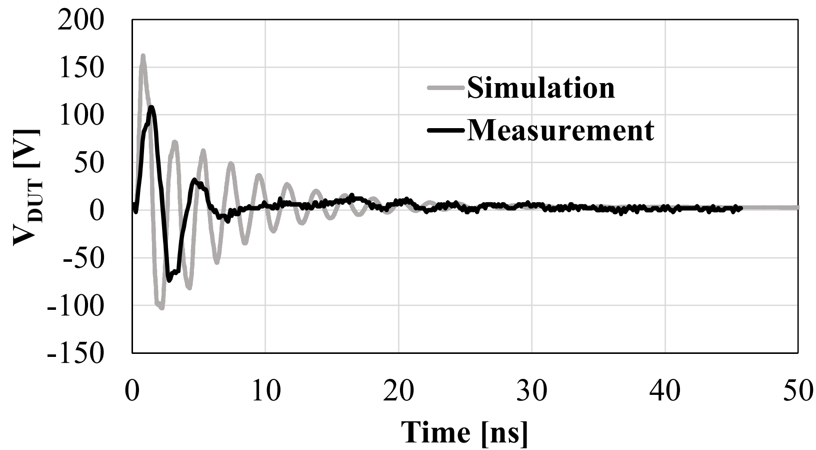

Figure 29: Same setup as for Figure 22; simulated and measured voltage.

Next, the response of a stand-alone TVS to a gun zap was both simulated and measured. This TVS was mounted on a separate 5 cm trace rather than on a signal trace to an IO pin. For the simulation, the actual trace used for the measurement was modeled.

The measured and simulated waveforms are shown in Figure 30 and Figure 31. In Figure 30, simulation is seen to provide an overly optimistic prediction of the voltage clamping provided by the TVS; i.e., the simulated voltage is lower. However, in Figure 30, as the time progresses past 20 ns, the measured voltage waveform begins to approach the simulated waveform, and by 40 ns, the two waveforms are nearly identical. From Figure 31, it is noted that the current varies quite significantly prior to 40 ns, and more so in measurement than in simulation. That observation suggests that there may be transient effects which are not properly replicated in simulation; this could be the result of inadequate models. There are a couple possible sources of error. First, the board trace models are extracted by ADS for the case that the board ground plane is the system ground; this is not the case during ESD gun testing. Second, the TVS and IC models are derived from quasi-static TLP I-V data, whereas the IEC current waveform does not have a constant (static-like) region.

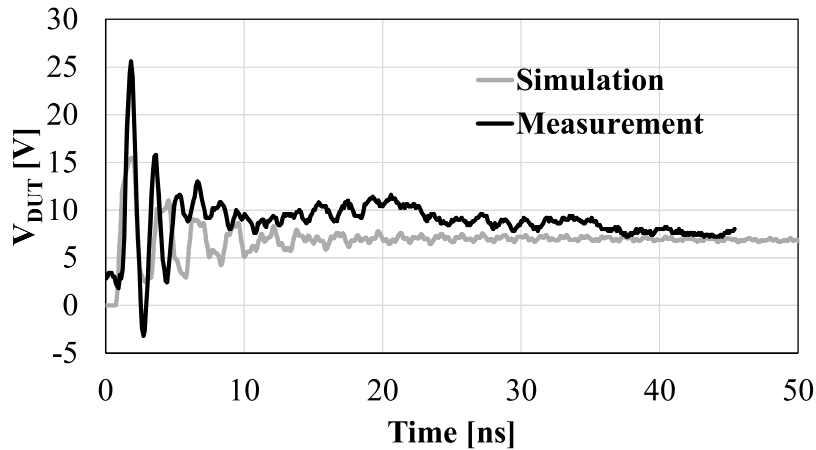

Figure 30: Voltage resulting from a 2 kV IEC gun zap to a stand-alone TVS; measurement and simulation.

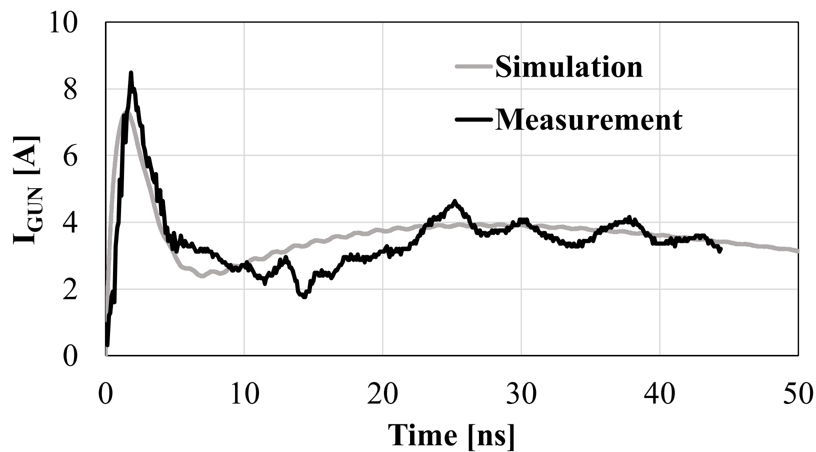

Figure 31: Current resulting from a 2 kV IEC gun zap to a stand-alone TVS; measurement and simulation.

The final case investigated is a gun zap to the board trace for IO3, with a TVS mounted on the board trace. The board is unpowered. Figure 26 shows both the measured and simulated voltage waveforms at the pick-off; simulation again predicts a lower clamping voltage than is found in measurement. Simulation was also used to look at the various branch currents in the system; it was seen that during the first current peak, the TVS is triggered on and conducts current away from the chip pin. The high impedance presented by the IC package inductance during the quick rise-time of the initial peak allows the voltage on the trace to reach a high enough value to trigger on the TVS. During the second current peak after 20 ns, most of the ESD current is conducted through the on-chip protection. The sudden drop in voltage at 35 ns is due to the same process described in V.B. The TVS has a larger on-voltage (clamping voltage) than does the on-chip protection; this induces a potential difference across the trace and bond wire inductances. The sustained potential difference induces a positive di/dt and progressively more current is shunted to the chip pin until

finally no more current flows through the TVS. When the current through the TVS reaches 0 A, it will turn off, and the fixed voltage drop across the inductance is eliminated, resulting in the voltage drop at 35 ns in Figure 32.

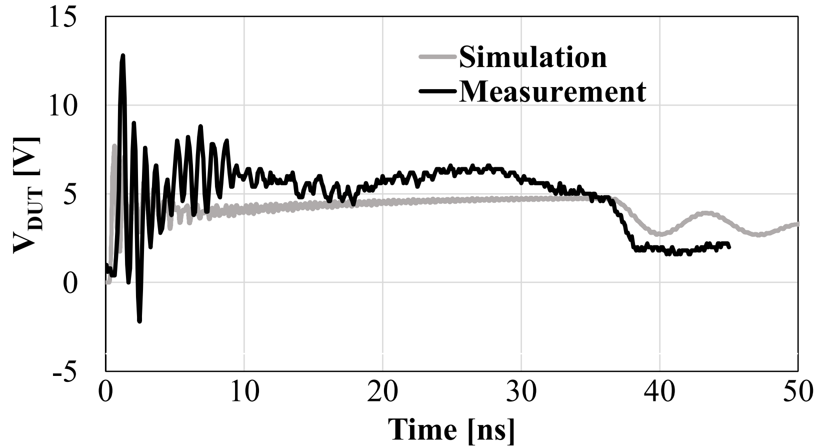

Figure 32: Simulated and measured voltage of 2 kV IEC gun zap to TVS and chip.

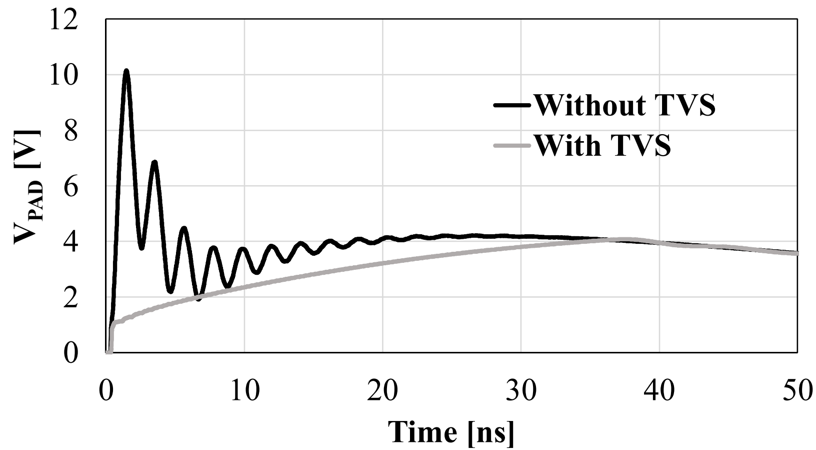

Figure 33: Simulated 2 kV IEC gun zap to chip with and without TVS. Simulated voltage from on-chip pad to on-chip VSSIO bus.

In all the IEC gun zap case studies presented here, the measured waveform has a noisier appearance than the simulated one. This is attributed to noise generated in the system by the gun, which is not captured by the gun model, as well as inaccuracies in the models of the board traces. Therefore, the simulation results for IEC gun zaps are not very precise. Nevertheless, there is some value to running the simulations. For example, simulation correctly predicted that the TVS protects the IC against the high current associated with the first discharge peak. The importance of this observation is highlighted by the simulation results shown in Figure 33. Figure 27 contains a plot of the voltage difference between the on-chip IO pad and the on-chip VSSIO bus; if this voltage

is too high, the on-chip devices will be damaged. Simulation shows that the TVS significantly reduces the maximum voltage stress on-chip, despite the TVS not being on during most of the ESD event.

CHAPTER 8: CONCLUSION

SEED calls for deriving component ESD models from TLP I-V data, and thus the TLP testing methodology will impact the model one derives. Pulse I-V characteristics can be different in the powered-on and powered-off states, thereby requiring separate models. A TVS may protect the chip more when it is powered-on than when it is powered-off due to the chip's varying I-V. The I-V characteristic measured with respect to board ground is a function of the amount and placement of the on-board decoupling capacitors. Board-level TLP characterization obscures the characteristics of the on-chip rail clamp and the detailed partitioning of the supply net impedances. This can result in inaccurate simulations when the board decoupling capacitance is changed.

If an IO pin receives the discharge, the pin's configuration (e.g., output high or output low) primarily affects the I-V at low current levels. For the test chip used in this study, the connection of the untargeted pins, i.e., chip pins that are neither external pins nor control pins, had no effect on the measurement results, i.e., it did not matter whether these pins were tied to the board ground or left floating. However, it is not known whether this is a general result. Board-level very-fast TLP cannot be used to obtain the pin I-V characteristic because the voltage does not settle to a constant value within its pulse width.

TLP I-V characteristics are accurately reproduced in simulation. By including models of the package parasitics and board traces, TLP waveforms could also be simulated accurately. Simulations of IEC 61000-4-2 discharges are less accurate, perhaps due to using quasi-static models of the components and insufficiency of the board trace models. However, simulation correctly predicted that the TVS protects the test chip against the large first current peak of an IEC discharge, even though the TVS was off during the balance of the ESD event as a result of the on-chip protection's smaller on-voltage.

8.1 Future Work

The current SEED methodology focuses on modeling the behavior of a single chip pin. That is to say, SEED models all IEC 61000-4-2 current entering a single pin and exiting aggregated VSSIO and VDDIO pins. This may not be realistic. In reality, the current entering into a chip may exit through multiple VSSIO and VDDIO pins. Additionally, the current of one pin may induce currents in other pins. Moving from modeling a single pin to a multi-port model of an IC may improve the accuracy of IEC 61000-4-2 simulations. Having a more complete model of the board

may also benefit the SEED methodology. In this work, the board was modeled as though board traces were isolated from each other. However, realistic products may have PCBs with dense traces that couple to each other. During an IEC zap, the current in the zapped trace will induce currents other traces. These currents may lead to a separate pin of the targeted IC or to a separate IC before returning to ground. Having more complete models of the IC and the board is important for capturing all paths the IEC current can take to return to ground, which may improve the accuracy of the simulation.

REFERENCES

[1] K. Kaschani and R. Gaertner, "The impact of electrical overstress on the design, handling, and applicaiton of integrated circuits," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2011.

[2] *System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches,* JEDEC, 2011.

[3] *System Level ESD Part II: Implementation of Effective ESD Robust Designs,* JEDEC, 2013.

[4] T. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Electrical Overstress / Electrostatic Discharge Symposium*, 1985.

[5] N. Monnereau et al., "A system-level electrostatic-discharge-protection modeling methodology for time-domain analysis," *IEEE Transactions on Electromagnetic Compatibility,* 2013.

[6] R. Bèges et al., "Practical transient system-level ESD modeling - environment contribution," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2014.

[7] F. Escudié et al., "From quasi-static to transient system level ESD simulation: extraction of turn-on elements," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2016.

[8] T. Li et al., "An application of utilizing the system-efficient-ESD-design (SEED) concept to analyze an LED protection circuit of a cell phone," in *IEEE Electromagnetic Compatibility Symposium*, 2012.

[9] S. Bertonnaud et al., "IEC system level ESD challenges and effective protection strategy for USB2 interfaces," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2012.

[10] N. Thomson, "High current pulse characterization of semiconductor devices," M.S. thesis, University of Illinois at Urbana-Champaign, Urbana, IL, 2015.

[11] *Electromagnetic Compatibility (EMC) - Part 4-2: Testing and Measurement Techniques - Electrostatic Discharge Immunity Test,* IEC, 2008.

[12] M. Scholz et al., "Comparison of system-level ESD design methodologies - towards the efficient ESD robust design of systems," *IEEE Transactions on Device and Materials Reliability,* vol. 13, no. 1, pp. 213-222, 2013.

[13] T. Li et al., "System-level modeling for transient electrostatic discharge simulation," *IEEE Transactions of Electromagnetic Compatibility,* vol. 57, no. 6, pp. 1298-130, 2015.

[14] G. Notermans et al., "HMM-TLP correlation for system-efficient ESD design," *Microelectronics Reliability,* vol. 52, no. 6, pp. 1012-1019, 2012.

[15] M. Scholz et al., "System-level ESD protection design using on-wafer characterization and transient simulations," *IEEE Transactions on Device and Materials Reliability,* vol. 14, no. 1, pp. 104-111, 2014.

[16] N. Thomson et al., "Custom test chip for system-level ESD investigations," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2014.

[17] J. Barth et al., "TLP calibration, correlation, standards, and new techniques," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2000.

[18] D. Johnsson and H. Gossner, "Study of system ESD codesign of a realistic mobile board," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2011.

[19] N. Monnereau et al., "Building-up of system level ESD modeling: impact of a decoupling capacitance on ESD propagation," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2010.

[20] R. Mertens et al., "Theory of active clamp response to power-on ESD and implications for power supply integrity," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2014.

[21] R. Mertens et al., "Separating SCR and trigger circuit related overshoot in SCR-based ESD protection circuits," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2013.

[22] Advanced Design System (ADS), Computer Software, Keysight (Agilent), www.keysight.com.

[23] V. Dwyer, J. Franklin and D. Campbell, "Thermal failure in semiconductor devices," *Solid-State Electronics,* vol. 33, no. 5, pp. 553-560, 1990.

[24] Y. Xiu et al., "S-parameter based modeling of system-level ESD test bed," in *Electrical Overstress / Electrostatic Discharge Symposium*, 2015.