TOWARD HIGH-EFFICIENCY HIGH POWER DENSITY SINGLE-PHASE DC-AC AND AC-DC POWER CONVERSION — ARCHITECTURE, TOPOLOGY AND CONTROL

BY

SHIBIN QIN

DISSERTATION

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Doctoral Committee:

Assistant Professor Robert C. N. Pilawa-Podgurski, Chair
Professor Philip T. Krein
Associate Professor Kiruba Sivasubramaniam Haran
Associate Professor Pavan Kumar Hanumolu

ABSTRACT

Power conversion between the single-phase AC grid and DC sources or loads plays an indispensable role in modern electrical energy system for both generation and consumption. The renewable resources and electrical energy storage are integrated to the grid through inverters. Telecoms, data centers and the rest of the digital world is powered by the grid through rectifiers. Existing and emerging applications all demand the DC-AC and AC-DC systems to be not only more efficient to reduce energy consumption, but also more compact to reduce cost and improve portability. Therefore, new AC-DC and DC-AC converter designs that improve the efficiency and power density of the system is a critical area of research and is the focus of this dissertation.

The recent development of wide band-gap devices stimulates a new round of improvement on efficiency and power density of AC-DC converters. However, despite the new transistors used, the fundamental system architecture and topology remain relatively unchanged, which is becoming the bottleneck for further improvement.

This dissertation explores new architecture, topology and control to overcome this bottleneck, targeting an order-of-magnitude improvement on power density and comparable efficiency to the conventional design. The proposed solutions build on two key innovations: the series-stacked buffer architecture for twice-line-frequency power pulsation decoupling in single-phase AC-DC and DC-AC conversion, and the flying capacitor multilevel topology for power transfer and waveform conversion between AC and DC. This work provides complete solutions for these ideas, including the theoretical development, design procedure, control method, hardware implementation and experimental characterization.

To Mengyao

ACKNOWLEDGMENTS

It has been five amazing years since I came to Illinois (how time flies). When I reflect back on my time here, what I appreciate the most are the people that I have the privilege of knowing.

I would like to thank my advisor, Professor Robert Pilawa-Podgurski, who brought me to Illinois and helped me thrive here. He is the coolest boss a graduate student could wish for. He is nice and caring to his students, while he has the ability to really encourage and inspire us to work hard and achieve our full potential. Five year ago, I was a complete novice in power electronics; now I feel like a really engineer ready to solve challenging problems. My research work in the past five years is not possible without his vision and support, and I am grateful for all the things he taught me — power electronics and much more.

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I would like to thank my parents, who taught me the most important lessons in my life. They always trust me and support me in all my decisions. They are always there to listen.

Living so far away from home has not been easy for either them or me. I wish I could have gone home more often; now I certain will.

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LIST OF ABBREVIATIONS

EMI	ElectroMagnetic Interference
EUR	Energy Utilization Ratio
FCML	Flying Capacitor MultiLevel
IVI	Inductor Volume Index
PFC	Power Factor Correction
RVR	Ripple Voltage Ratio
THD	Total Harmonic Distortion
TSS	Total Switch Stress

CHAPTER 1

INTRODUCTION

1.1 Single-phase AC-DC and DC-AC power conversion

Power conversion between DC and single-phase AC (inversion or rectification) finds a wide range of applications in both energy generation and consumption, spanning some of the most important areas of power electronics research and applications, such as transportation electrification and grid integration of storage and renewable resources. To name a few examples, on the energy generation side, residential or commercial scale PV installations typically have a string inverter or many micro-inverters to feed the DC power from PV modules into the single-phase electric grid; on the energy consumption side, most of the electrical systems power from the grid require rectifiers with power factor correction (PFC) capability; many battery storage systems require an AC-DC converter with bidirectional power transfer capability.

A modern distributed power architecture utilized in many industrial applications including telecoms and data centers is shown in Fig. 1.1 [1,2]. A PFC front end converter, typically non-isolated, interfaces the grid and transfers the power to a high voltage DC bus (e.g., 400 V). Then a front end DC/DC converter (e.g., an LLC converter) provides the isolation and steps down the voltage to an intermediate voltage DC bus (e.g., 48 V), which further distributes the power among downstream point-of-load (POL) regulators. The POL regulators eventually provide well-regulated voltages to the load. Similar architecture with power flowing in reverse can be found in distributed PV generation systems [3–5], etc. While such a distributed power architecture involves a variety of different power converters at different points of the system, the focus of this research is on the AC-DC converters between the AC grid and the high voltage DC bus, i.e., PFC front end rectifiers or grid-connected inverters. Beside the power supply architecture given in Fig. 1.1, such AC-DC converters are also indispensable in a wide range of other applications such as electric vehicle charging, LED drivers, battery storage systems and many more. Therefore, it is an important building block worth in-depth study.

A high-level conceptual schematic of a single-phase AC-DC converter is shown in Fig. 1.2a.

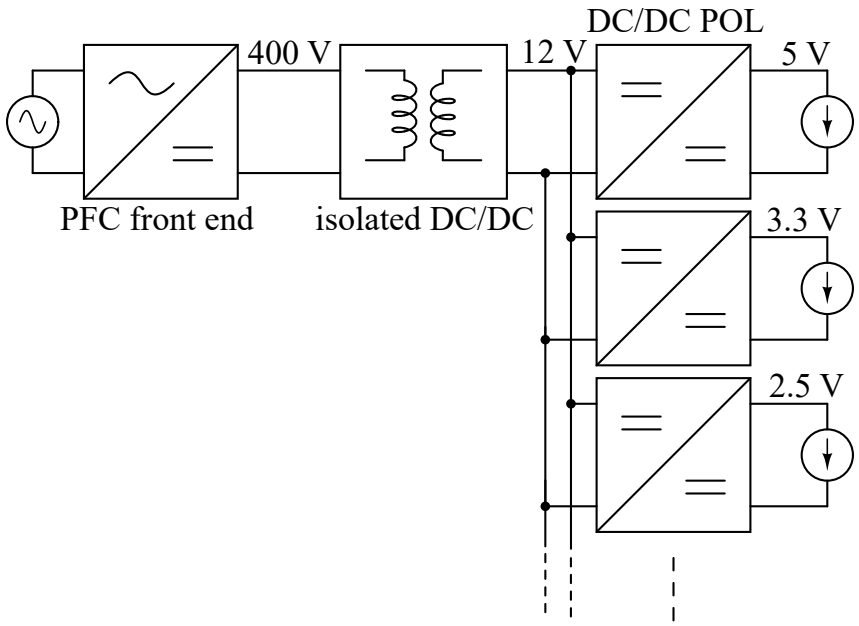


Figure 1.1: A typical distributed power architecture.

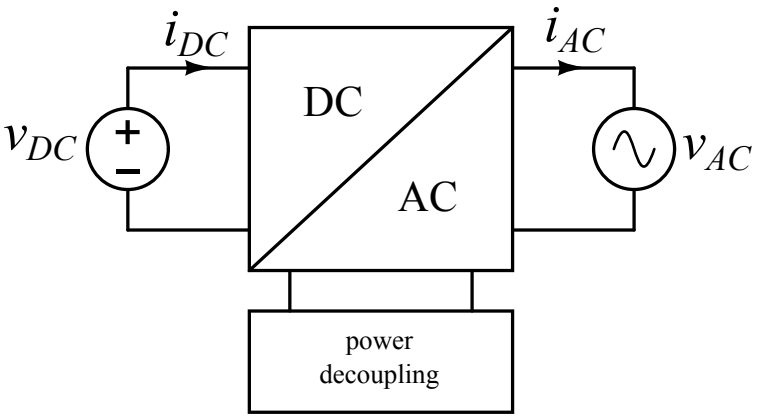
The power on the AC side is given as

$$\begin{aligned} P_{ac} = v_{ac} i_{ac} &= V_{AC} sin(\omega t) \times I_{AC} sin(\omega t + \phi) \\ &= \underbrace{\frac{1}{2} V_{AC} I_{AC} cos\phi}_{\text{constant}} - \underbrace{\frac{1}{2} V_{AC} I_{AC} cos(2\omega t + \phi)}_{\text{pulsation}}, \end{aligned} \tag{1.1}$$

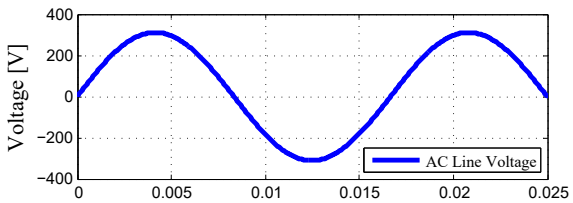
where ω is the line angular frequency, ϕ is the power factor angle and V_{AC} and I_{AC} are the AC output voltage and current amplitude, respectively. Obviously, the AC side power consists of a constant part and a pulsating part at twice line frequency. With a unity power factor, $\phi = 0$ represents the inverter operation and $\phi = \pi$ represents the rectifier operation. The power on the DC side is supposed to be constant and equals the constant part of the AC side power, i.e.,

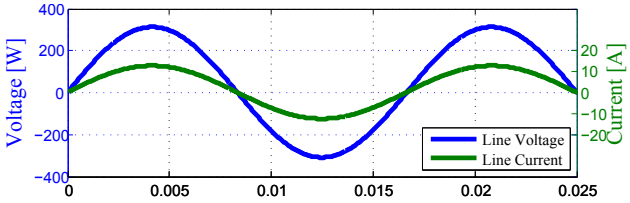
$$P_{dc} = v_{dc} i_{dc} = \frac{1}{2} V_{AC} I_{AC} cos\phi. \tag{1.2}$$

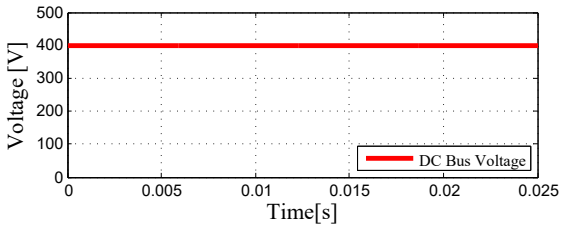
While the constant power should transfer between the AC and DC sides, the pulsation power on the AC side is supposed to be buffered completely by the AC-DC converter. Otherwise, the pulsation power would propagate to the DC side and introduce current and voltage ripples on the DC bus. Such ripples are usually very undesirable and strictly restricted. For example, ripples in a PV system reduce the tracking efficiency of maximum power point tracking operations [6]; ripples in an LED driver cause flicker in the light, which imposes



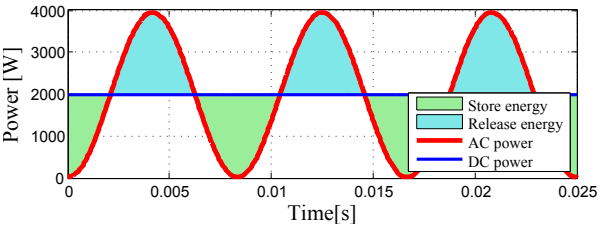
(a) Schematic.







(b) Voltage conversion.



(c) Power pulsation decoupling.

Figure 1.2: The main functionalities of a DC-AC converter.

potential health concerns [7]. Therefore, the basic task of a single-phase AC-DC converter is twofold: it needs to convert the voltage and current to the right level and transfer the power between input and output, as illustrated in Fig. 1.2a; it also needs to buffer the twice line frequency power pulsation from the AC side to maintain a ripple-free DC side, as illustrated by Fig. 1.2c. The entire research is built around fulfilling these two tasks in the most effective and efficiency way.

1.2 Research scope and goal

When designing a system to fulfill these two tasks, a few performance metrics should be first determined. As the case for most power converters, the conversion efficiency is often the most important metric, as it affects not only the amount of energy consumption but also

Table 1.1: Google/IEEE little box challenge design specifications [8]

Specifications	Value
Input	450 Vdc with 10 Ω source resistance
Output	240 Vac, 60 Hz
Power Level	0 to 2 kVA
Power Factor	0.7 - 1, leading and lagging
Input Ripple	current < 20 %, voltage $< 3\%$
Efficiency	$> 95\%$ (CEC weighted)
Power Density	> 50 W/inch^3
Thermal Limit	< 60 °C on all enclosure surface
Output Current THD	$< 5\%$ for 25% to 100% load, < 60 mA for below 25% load
Output Voltage THD	$< 5\%$
EMC	FCC Part 15 B

other factors in the system such as thermal management and component lifetime. Besides efficiency, power density (i.e., the hardware volume to deliver certain power) is often an equally important metric. A large portion of AC-DC converter applications are volume or weight constrained, so a high power density converter is very desirable. Usually high efficiency and high power density are closely related. It is difficult to achieve high power density with poor efficiency since more power loss will likely increase the heatsink volume. However, high efficiency and high power density are also contradicting to each other. It is relatively easy to build a highly efficient converter with unlimited volume, while to build a very efficient converter with as small as possible volume is difficult, but of high interests in both research and applications.

One such example is the Google/IEEE little box challenge [8], an open competition to build the world's most power dense inverter with high efficiency. The competition requires the design and implementation of a 2 kW single-phase inverter with a 240 V RMS AC output; the DC source is 450 V with a 10 Ohm source resistor (presumably to emulate the characteristics of a PV string), implying a DC bus voltage of 400 V at full 2 kW load; the efficiency has to be higher than 95%; the DC side voltage ripple has to be smaller than 3% and the DC side current ripple smaller than 20% of the average. There are also other requirements on the EMI, etc. The main requirements listed in [8] are summarized in Table 1.1. The competition is to achieve the highest power density while meeting all these specifications. In order to establish a common baseline for analysis and comparison, the aforementioned specifications will be used as a design example target throughout Chapter 2 to Chapter 6.

Table 1.2: 1.5 kW PFC front end design specifications

Specifications	Value
Input voltage	90 Vac – 260 Vac (RMS)
Output power	1500 W
Output voltage	400 Vdc
Output voltage ripple	< 5 V
Power factor	> 0.98
Input current THD	$< 5\%$ above 25% load

The Google/IEEE little box challenge design requirements represent most of the important aspects of single-phase AC-DC power conversion, but an important part that is missing is the grid-connected operation. The little box challenge only requires the inverter driving a standalone passive load, while most of the practical applications requires connection with the AC grid. Therefore, this work also study grid-connected operation of single-phase AC-DC converter. This part is studied through a 1.5 kW PFC rectifier design with requirements listed in Table 1.2. This design example is considered throughout Chapter 7 to Chapter 9.

To summarize, the goal of this research is to develop new techniques for AC-DC and DC-AC power conversion achieving high efficiency and high power density simultaneously, while improving other commonly cited performance for grid connected converters such as power factor and total harmonic distortion (THD). With other performance comparable or better than conventional approaches, this research targets power density improvement by an order of magnitude compared to conventional approaches. The fundamental methodology to achieve this goal is to leverage new system architecture, unconventional circuit topology and advanced digital control. Two design examples that embody the new ideas developed are considered throughout this work: the 2 kW inverter per the little box challenge requirement and the 1.5 kW universal input PFC front end.

1.3 Research contribution

The contribution of this work builds upon two major innovations to address the challenge of designing high-efficiency, high power density AC-DC system. The first one is a series-stacked buffer architecture for the task of twice-line-frequency power pulsation decoupling. The second one is the practical realization of a compact, high frequency flying capacitor multilevel (FCML) topology for the task of AC-DC power converter. The theoretical development of the idea as well as its design procedure, control method, hardware implementation and

experimental characterization are presented in this dissertation.

In the Google/IEEE little box challenge, while the originally set power density challenge is 50 W/inch^3, our team from University of Illinois at Urbana-Champaign developed a 216 W/inch^3 inverter which makes the highest power density entry from academia [9]. The multilevel topology and active power pulsation decoupling techniques to be discussed in this dissertation are the key enablers of such high power density.

1.4 Organization of this dissertation

The rest of this document can be divided into two major parts.

The first part consists of Chapter 2 to Chapter 6. This part prepares the necessary background on circuit element property, topology, control characteristics to derive and analyze active energy buffers, and then presents a new active power pulsation decoupling technique with tenfold power density improvement compared to other solutions in the literature.

Chapter 2 introduces the property of inductors and capacitors as energy storage elements in the circuit, which greatly affect the design considerations throughout this research. The conventional passive decoupling solution is introduced and its shortcomings are discussed, which motivates the use of active power pulsation decoupling techniques.

Chapter 3 reviews previous work on active power pulsation decoupling in the literature. To facilitate comparison, the concept of active buffer cell is established and a few performance metrics are highlighted. The main drawbacks of the existing solutions are the high component voltage stress and severe efficiency penalty of the active decoupling circuit, which motivates the development of the series-stacked buffer that solves these problems.

Chapter 4 explains the operation of the series-stacked buffer architecture and its advantages compared to other solutions reviewed in Chapter 3. The design constraints and optimization procedures are also derived.

Chapter 5 reveals the control challenges associated with this architecture and presents the solution. Due to the series-connected nature of this architecture, current matching and capacitor voltage balancing are difficult. A compensation scheme utilizing the small ripple on the DC bus is developed to solve this problem.

Chapter 6 presents the hardware prototype implemented for this architecture per the little box challenge requirements and the experimental results that verify the performance of the prototype, including power density, efficiency, DC side ripple, transient performance and various other waveforms illustrating of the operation. The experimental performance is also compared with various works in previous literature and other little box challenge entries.

The second part consists of Chapter 7 to Chapter 9. This part introduces the FCML topology and explores its control for grid connected operations.

Chapter 7 reviews the problems of conventional two-level based topologies and introduces the basics of the FCML topology. Its advantages is highlighted to motivate its application in single-phase AC-DC converters.

Chapter 8 presents a seven-level FCML converter design for a 1.5 kW PFC front end. The PFC control challenges when applying the FCML topology is analyzed in details and a feed-forward control scheme is developed to achieve excellent power factor and THD performance.

Chapter 9 presents the hardware prototype of the seven-level FCML based PFC front end. Various practical implementation issues are addressed. The high efficiency, high power density and high waveform quality are experimentally verified. Again, the experimental performance is compared with others reported in the literature.

Lastly, Chapter 10 summarizes the underlying reason why such high power density can be achieved with the proposed idea. Future work of this research is also suggested.

CHAPTER 2

ENERGY BUFFER BACKGROUND

2.1 Energy storage in single-phase AC-DC converter

As illustrated in (1.1), a twice line frequency power pulsation is present in the AC side power. Within each line cycle, this power pulsation needs to be absorbed and the associated energy stored in certain circuit elements when the pulsating power is positive; this energy is then released when the pulsating power is negative. Based on (1.1) and (1.2), the power of the energy storage element is given as

$$\begin{aligned} P_{buf} = P_{dc} - P_{ac} &= \frac{1}{2} V_{AC} I_{AC} cos(2\omega t + \phi) \\ &= \frac{P_{dc}}{cos\phi} cos(2\omega t + \phi). \end{aligned} \tag{2.1}$$

The energy needs to be stored in each line cycle is given as

$$E_{buf} = \int P_{buf} dt = \frac{P_{dc}}{2\omega cos\phi} [sin(2\omega t + \phi) + \sigma], \tag{2.2}$$

where σ is a constant and $\sigma \geqslant 1$, since the energy stored by a circuit element needs to be positive. The condition $\sigma = 1$ is often selected to minimize the energy storage, but in certain situations there would be reasons to choose $\sigma > 1$, as will be discussed in Chapter 3. Therefore, the storage elements have to be designed to be *at least* capable of storing

$$E_{buf,peak} = \frac{P_{dc}}{\omega cos\phi}. \tag{2.3}$$

Note that in power converter designs, it is common to leverage a high switching frequency to reduce the energy storage requirement (and thus the energy storage element volume). However, in this scenario, ω in (2.3) is fixed by the slow AC line frequency. Therefore, the single-phase AC-DC converter has to store a relatively large amount of energy and the volume of the energy storage element typically dominates the volume of the entire system.

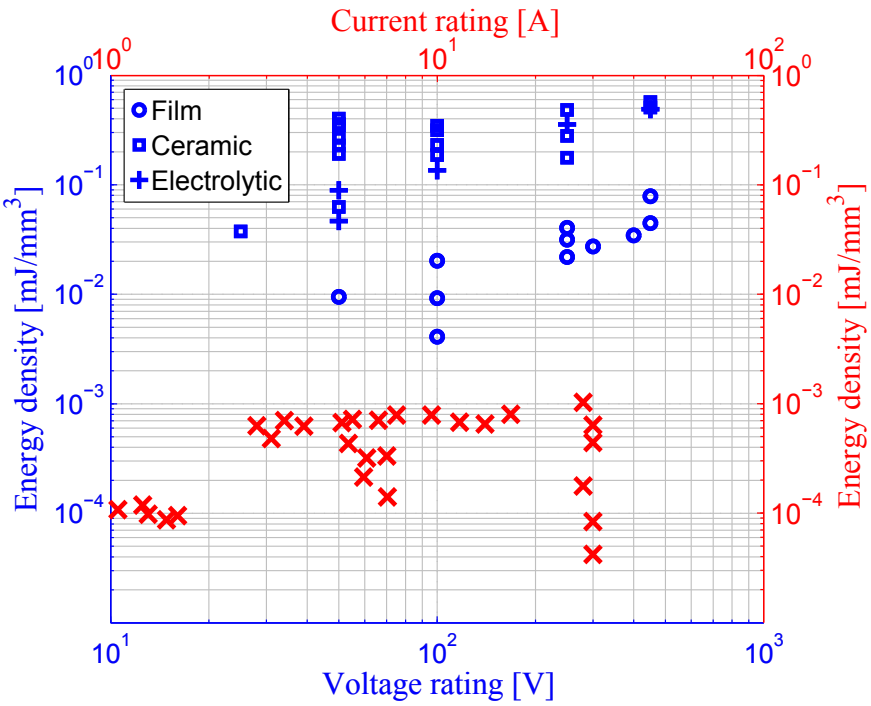


Figure 2.1: The energy density of selected capacitors measured in [10] and selected Coilcraft inductors calculated from the datasheet.

2.2 Energy density of storage elements

In twice-line frequency buffering, the most commonly considered storage elements are capacitors ($E = \frac{1}{2}CV^2$) and inductors ($E = \frac{1}{2}LI^2$). For high power density AC-DC converter design, it is important to consider the energy density of these components.

The power density of selected capacitors and inductor are plotted in Fig. 2.1. This voltage and current rating range is consider as it is applicable to the little box challenge design requirement considered as a baseline throughout this document. The inductors are selected from Coilcraft and their power density values are calculated from the datasheet with nominal inductance and saturation current rating. The capacitors are selected mostly from TDK and their power density values are all measured experimentally as presented in [10]. It is clear from Fig. 2.1 that in terms of power density, the best commercially available capacitors are about 500 to 1000 times better than the best commercially available inductors. Therefore, capacitors are often chosen as the energy storage component in single-phase AC-DC converters.

There are three major types of capacitors: electrolytic, ceramic and film. Electrolytic capacitors offer large capacitance at low cost, but they have relatively large equivalent series resistance (ESR), and thus high power loss and poor ripple current capability. Electrolytic

capacitors are unipolar, so they cannot withstand AC voltage. The reliability of electrolytic capacitors is relatively low and it is a bottleneck of the system reliability in many applications [11]. In comparison, film capacitors have low ESR, good ripple current capability and reliability, but the energy density is at least an order of magnitude lower. Ceramic capacitors have both good power density and low loss compared to the other two types. In fact, the best power density measured in Fig. 2.1 is achieved by an X6S ceramic capacitor rated at 450 V. Ceramic capacitors are also more reliable compared to electrolytic capacitors. For all these merits, ceramic capacitors are used extensively in all the prototypes in this work.

It is important to note some of the unique characteristics of ceramic capacitors as an energy storage element. The capacitance of ceramic capacitors is nonlinear and highly dependent on the voltage applied on the capacitor. This is often referred to as voltage de-rating. Typically, the capacitance of class II ceramic capacitors can decrease more than 70% from their nominal values when the applied voltage increases from zero to the rated voltage. Therefore, it is important to consider the large signal behavior of the ceramic capacitors when used as storage elements, and that is why experimental measurement in [10] are important to determine the actual energy density of the capacitor. The measured result in Fig. 2.1 indicates that the X6S ceramic capacitor, even after voltage de-rating, still offers the best power density.

It should also be noted from Fig. 2.1 that ceramic capacitors at different voltage ratings have approximately the same energy density. Although higher voltage leads to more energy stored, a capacitor rated at higher voltage typically has lower capacitance density, so the end result on energy density cancels out. At different voltage ratings, there might be small irregularities of power density due to practical issues like packaging footprint, but to the first order, they have approximately the same power density at different voltage rating, at least on the same order of magnitude. This means that for ceramic capacitors, there is limited or perhaps even no advantage to use high voltage rating capacitors. As long as the capacitors are charged fully to the rated voltage, it should make little difference which voltage rating is chosen. Note that the above argument is only valid for ceramics. For electrolytic and thin film capacitors, higher voltage rating does imply high energy density. This point can also be observed from Fig. 2.1. This work focuses on the use of ceramic capacitors, though, given its high energy density and high current ripple capability.

2.3 Capacitor passive decoupling

In single-phase AC-DC converters in practice, the simplest and most widely used power pulsation buffer nowadays is a large DC link capacitor, as shown in Fig. 2.2. This approach

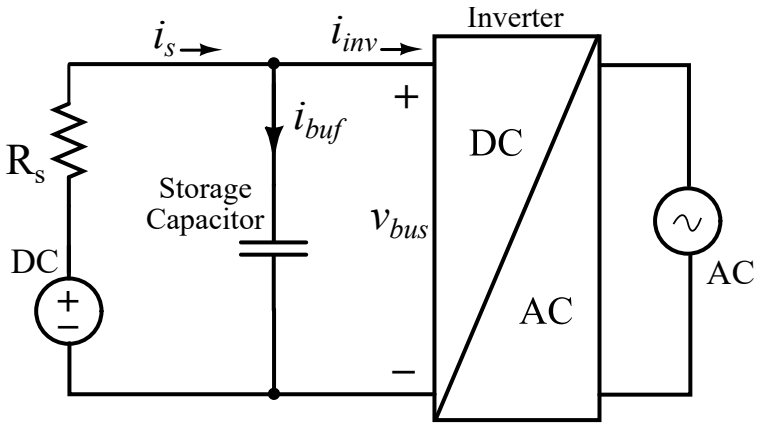


Figure 2.2: Capacitor passive decoupling.

is often referred to as capacitor passive decoupling. Based on (2.3), in one cycle, the energy storage of the capacitor bank can be expressed as

$$\begin{aligned} E_{buf,max} - E_{buf,min} &= \frac{P_{dc}}{2\pi f cos\phi} \\ &= E_c(V_{max}) - E_c(V_{min}) \qquad (2.4) \\ &\approx \frac{1}{2}CV_{max}^2 - \frac{1}{2}CV_{min}^2 \\ &\approx \underbrace{\frac{1}{2}(V_{max} + V_{min})}_{\text{average}}\underbrace{(V_{max} - V_{min})}_{\text{ripple}}C \ , \qquad (2.5) \end{aligned}$$

where P_{dc} is the average power (i.e., the DC power) of the DC-AC converter, f is the line frequency and V_{max}, V_{min} are the two extremes of the voltage across the capacitor bank. The energy storage requirement in one cycle is determined by the average load power (i.e., $\frac{P_{dc}}{2\pi f cos\phi}$), and is fulfilled by charging and discharging the capacitors (i.e., $E_c(V_{max}) - E_c(V_{max})$). We may ignore the fact that C might be nonlinear and depends on the voltage, as it is especially the case for ceramic capacitors. Assume a constant C, then we arrive at (2.5). This assumption is made for the simplicity of analysis and the general conclusions of the following analysis is valid regardless of the nonlinearity of C.

According to (2.5), the capacitor bank needs to have enough capacitance C and voltage ripple (i.e., $V_{max} - V_{min}$) to provide the required power pulsation buffering capability. Note that as discussed in Section 1.1, voltage ripple on the DC bus is very undesirable. Most applications impose strict constraints (a few percentage of the average DC bus voltage) on the magnitude of the allowed voltage ripple on the DC bus. Therefore, to meet certain energy storage requirement, the capacitance C typically has to be very large. Such large capacitance

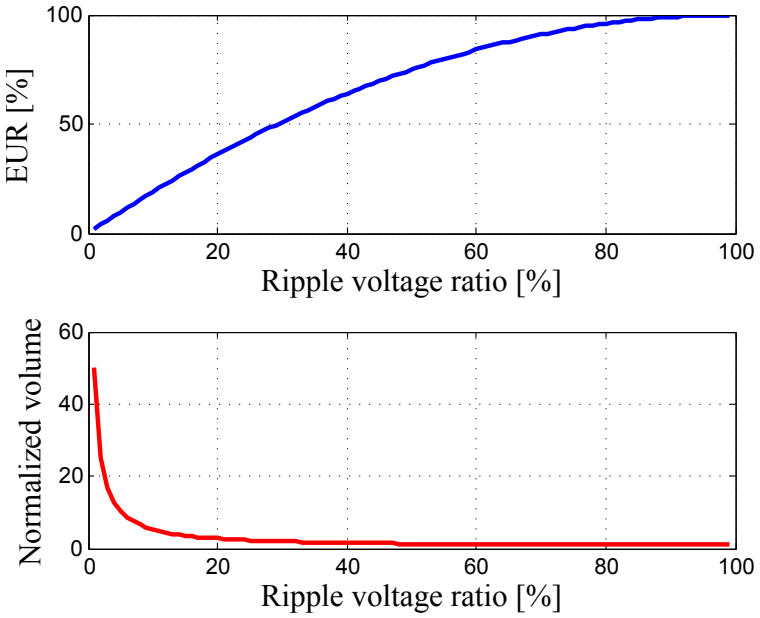


Figure 2.3: The energy utilization ratio (EUR) and passive decoupling capacitor volume (normalized over the volume at 100% EUR) as a function of the ripple voltage ratio on the DC bus.

is usually provided by a bulky electrolytic capacitor bank, as electrolytic capacitors offer large capacitance at low cost, and it is often the only economically viable solution given the large C needed. However, as mentioned in Section 2.2, electrolytic capacitors are known for their high power loss, low reliability and limited current ripple capability [11]. In fact, in practice the volume of the electrolytic DC bus capacitor bank is often limited by the ripple current capability [12], rather than the capacitance requirement of (2.5). Therefore, due to efficiency and reliability considerations, ceramic or metal film capacitors are often preferred, but the large volume and high cost becomes the major limitations. With either type of capacitor, the volume of the DC link capacitor bank typically dominates the volume of the overall AC-DC converter.

2.4 Energy utilization ratio

To better understand the problem of capacitor passive decoupling, let us define two important metrics. The first one is the ripple voltage ratio (RVR), which is simply the voltage ripple over the maximum voltage on the DC bus, i.e.,

$$\Gamma_{\text{RVR}} = \frac{V_{max} - V_{min}}{V_{max}}. \tag{2.6}$$

The second one is the energy utilization ratio (EUR) [13]. EUR of *a single capacitor* is defined as the peak energy exchanged in one line cycle over the full energy storage at the maximum rated voltage, i.e.,

$$\Gamma_{\text{EUR}} = \frac{E_{buf,peak}}{E_c(V_{max})} = \frac{E_c(V_{max}) - E_c(V_{min})}{E_c(V_{max})}, \tag{2.7}$$

where $E_{buf,peak}$ is defined in (2.3). The total volume of the energy storage element is determined by $E_c(V_{max})$, while the energy storage requirement is fulfilled by $E_c(V_{max}) - E_c(V_{max})$. EUR = 100% would be highly desirable as it implies that a certain energy storage requirement is fulfilled with the smallest capacitor volume possible.

For an active buffer structure with more than one energy storage capacitor, such as the series stacked buffer to be presented in this dissertation, EUR is typically calculated for all the capacitors in the structure, i.e.,

$$\Gamma_{\text{EUR}} = \frac{E_{buf,peak}}{\sum E_c(V_{max})}, \tag{2.8}$$

where the sum is over all energy storage capacitors in the circuit. It is very important to note that, in general,

$$E_{buf,peak} \neq \sum E_c(V_{max}) - \sum E_c(V_{min}), \tag{2.9}$$

since not all the capacitors reach their maximum or minimum voltage at the same time.

Fundamentally, the problem of the capacitor passive decoupling is that the DC link capacitor bank needs to perform both energy storage and DC bus voltage regulation, but these two functionalities are contradicting to each other. Effective energy storage requires a large EUR while DC bus voltage regulation restricts the EUR to only a few percentage. To see this point, Fig. 2.3 plots the EUR of the capacitor bank as a function of the allowed RVR on the DC bus. For an application that allows 3% ripple on the DC bus, the EUR is only approximately 6%, resulting in a capacitor volume 17 times larger than the volume under 100% EUR.

The key to overcoming this limitation is to separate the energy storage and voltage regulation functionalities from the capacitors. The capacitors should be allowed to ripple more to improve EUR while being interfaced to the DC bus through an active converter to maintain a constant bus voltage. This approach is often referred to as active power pulsation decoupling, or active decoupling for short. Various embodiments of such schemes have been presented in the literature [14–16], which will be review in Chapter 3. Active decoupling,

however, usually introduces efficiency penalty, additional circuit elements and considerable complexity into the system, which designers should strive to minimize.

Consider the Google/IEEE lttle box challenge design example in Table 1.1. For this 2 kW inverter generating 60 Hz output, only 3% voltage ripple is permitted on the 400 V DC bus. If a conventional passive decoupling solution is used, it can be calculated that at least 1.1 mF is required for the DC link capacitor bank according to (2.5) . Moreover, if practical ripple current limitations of electrolytic capacitors are taken into consideration, even more capacitors are typically needed. On the opposite extreme, if a 100% EUR is somehow achieved, then only 64 μF of buffer capacitor is required. Practical active decoupling solutions will result in capacitance somewhere between these two extremes.

CHAPTER 3

REVIEW OF ACTIVE ENERGY BUFFER

3.1 Overview

As reviewed in Section 2.1, the twice-line-frequency power ripple decoupling is a fundamental challenge in all single-phase AC-DC or DC-AC converters since the beginning. While some previous works focus on improving the passive DC link capacitors through component level optimizations [17] or system level tradeoffs [18–22], many works study active decoupling circuits. Many of the active decoupling circuit topologies to be reviewed in this chapter can be traced back to the earlier works in [23–34]. For example, Wang et al. [23] and Hsu et al. [24] represent the early work on the full-bridge active buffer with capacitor energy storage while Bose et al. [25] and Shimizu et al. [26] have a similar active circuit topology but with inductor energy storage. Martins et al. [27–29] propose a two-stage structure containing a high voltage intermediate bus with larger voltage ripples to reduce the required storage capacitor, while the first stage DC-DC converter keeps the DC side ripple-free; this structure is still widely used in various current works [35]. Moreover, Shimizu et al. [30, 31] and Kjaer et al. [32] propose an active buffer circuit integrated to the operation of a flyback converter. Kyritsis et al. [33,34] present some of the original ideas of the half-bridge active buffer with capacitor energy storage. These works form the basis of a rapid development of this area in the past decade [13–16,36–48]. Nowadays there are well over 50 variations of active decoupling buffers in the literature with different combinations of system architecture, converter topology and control method. While this dissertation will only review closely related works leading to the development of the series-stacked buffer architecture, comprehensive reviews on twice-line-frequency power decoupling can be found in [14–16, 49].

In this dissertation, they are classified as "independent decoupling" and "dependent decoupling" buffers, as it would be the best way to understand the logic flow. "Independent decoupling" means that the operation of the active buffer is independent of the rest of the AC-DC converter; that is, the active buffer is intended to be a plug-and-play replacement of the bulky DC bus capacitors in the capacitor passive decoupling solution. It should not

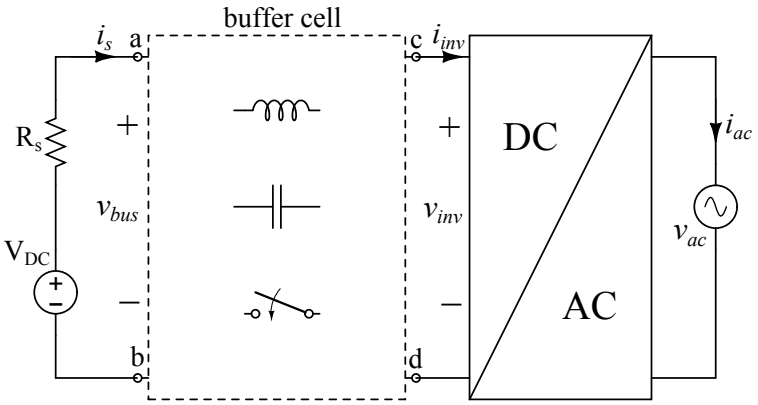


Figure 3.1: The concept of "independent decoupling". The active buffer cell and the inversion/rectification stage are two distinct parts in the system and operates independently.

change the operating point or the control method of the inversion/rectification stage. "Dependent decoupling", on the other hand, means that active buffer shares part of the circuit elements with the inversion/rectification stage and the control and operation of both parts are integrated together. These two approaches are closely related. One can often derive a "dependent decoupling" solution from a corresponding "independent decoupling" solution, or vice versa. This chapter mostly discusses "independent decoupling", as it is the necessary preparation to understand the series-stacked buffer architecture; "dependent decoupling" will only be discussed briefly.

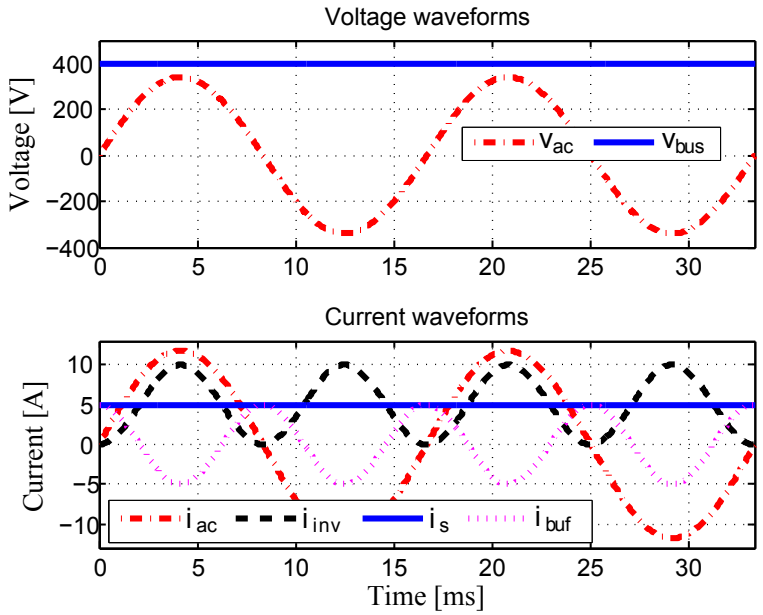


Figure 3.2: Waveforms of key voltage and current variables marked in Fig. 3.1 in two line cycles.

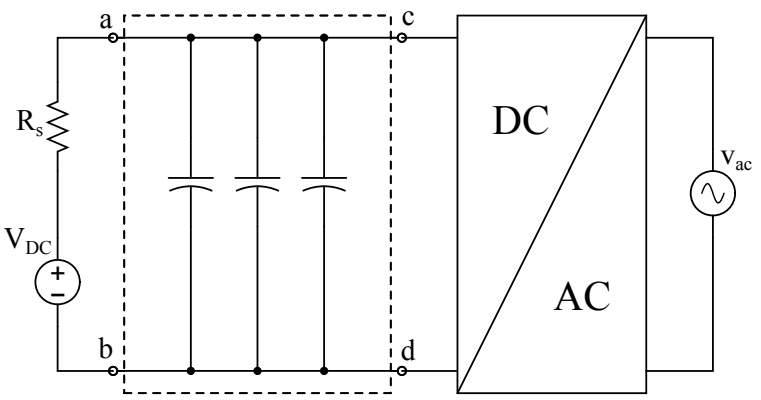


Figure 3.3: Capacitor passive decoupling solution fitting into the concept of buffer cell.

3.2 Buffer cell concept

A high-level schematic of the "independent decoupling" buffer in an AC-DC system is shown in Fig. 3.1. Note that the analysis throughout this document applies equally to inverters and rectifiers in almost all cases unless otherwise stated, so the following analysis will assume an inverter system for simplicity of description.

The active decoupling circuit can be abstracted as a two-port element (i.e., a buffer cell) inserted between the DC source and inversion stage. Some key voltage and current variables are marked in Fig. 3.1 and their ideal waveforms are plotted in Fig. 3.2. The voltage and current on the AC side are 60 Hz sine wave. Ideally, we would like the DC bus voltage and the DC side input current, i_s, to be constant. Under this condition, the power of the buffer cell is given in (2.1) and the energy it stores is given in (2.2). If the DC bus voltage is held constant, the current flowing into the active buffer cell, i_{buf}, follows a 120 Hz sine wave, i.e.,

$$i_{buf} = \frac{P_{buf}}{V_{bus}} = \frac{P_{dc}}{V_{bus} cos\phi} cos(2\omega t + \phi), \tag{3.1}$$

as shown in Fig. 3.2.

The capacitor passive decoupling discussed in Section 2.3 can fit into the buffer cell concept as shown in Fig. 3.3, and the current through the capacitor would be i_{buf}. Depending on the voltage ripple, the EUR of such a passive buffer cell is calculated in Fig. 2.3 and is expected be very low as discussed. Active buffer cells are therefore developed to improve the EUR so capacitor volume can be small, while preserving the same functionality of absorbing current and power mismatch. One example of such an active cell structure is shown in Fig. 3.4, where a magnetic-based converter interfaces the energy storage capacitor and the DC bus. The converter is controlled to shape its waveform, as shown in Fig. 3.2, such that power

pulsation is absorbed. Details of various types of buffer cells will be reviewed in this section.

3.2.1 Buffer cell performance metrics

Before introducing any specific buffer cell structure, it would be of high interest to highlight a few performance metrics that allow quantitative comparison of their performance.

The first metric is EUR, which has been defined in Section 2.4. This parameter reflects the volume of the capacitor and improving EUR is the most important motivation of active decoupling.

The second metric is the total switch stress (TSS) of the converter, defined as

$$S = \sum_{i=0}^{n} (V_{max} I_{max}), \tag{3.2}$$

where the sum is over all switches in the converter, V_{max} is the maximum voltage blocked by the switch and I_{max} is the maximum current conducted by the switch. Typically, switch utilization ratio, defined as the power delivered over the switch stress, is considered for a converter. However, once the system power level is given, the power processed by the energy buffer is the same for all buffer cells (i.e., the power delivered is the same), so it is enough to consider only the TSS. Note that since TSS is obtained by summing over all switches, the effect of the switch count is also reflected in TSS. This metric is often a good indicator of the switch size, switching frequency and power loss. A good topology should minimize TSS.

The third metric is the power loss. A complete and precise calculation of all power losses in the converter is very difficult; therefore, we consider only a few major components in their approximate forms. The conduction loss, including both inductor DCR and transistor on-resistance, is given as

$$P_{cond} = (I_{ave}^2 + \frac{1}{12}\Delta I^2)[R_{on} + R_{DCR}], \tag{3.3}$$

where R_{DCR} is the DCR of the inductor and R_{on} is the on-resistance of all the transistors. The inductor core loss is given as [50]

$$P_{core} = k(\Delta I)^{\beta} f_s, \tag{3.4}$$

where k and β are empirical parameters, ΔI is the inductor current ripple and f_s is the

switching frequency. The transistor output capacitor loss is given as

$$P_{Coss} = \frac{1}{2} C_{oss} V^2 f_s, \tag{3.5}$$

where C_{oss} is the parasitic capacitance across the transistor drain-source. Lastly, the current-voltage overlap loss is given as

$$P_{op} = \frac{VI}{2} t_{tr} f_s, \tag{3.6}$$

where t_{tr} is the sum of transistor turn-on and turn-off time. Note that purpose of studying these loss equations here is not to calculate the specific value of loss, but rather to understand how the power loss scales with other circuit parameters such as voltage and current stress.

The fourth metric to consider is the voltage stress on the circuit components, especially the inductor. For certain current ripple and switching frequency, the value of inductance is directly determined by the voltage applied, i.e., $L \propto V$. Moreover, the voltage stress usually affects the switching frequency and power loss of the converter as well, which might in turn increase the required inductance. High inductance limits the dynamic performance of the buffer cell and increase the inductor volume. Voltage stress should be minimized.

The fifth metric to consider is the inductor volume. Since one of the major purposes of active decoupling is to improve power density, care must be taken that the volume reduction due to higher EUR is not offset by the volume of the added components. The volume of the added component is often dominated by the inductor volume. As discussed in Section 2.2, we can assume a constant power density for all inductors regardless of the current rating level. Then the volume of the inductor is determined simply by its peak energy storage, i.e., $\frac{1}{2} L I_{max}^2$. The inductance L is affected by voltage stress and frequency. For different converter designs with the same current but different voltage stress levels, a fair comparison can be made by making the entire converter have the same efficiency and inductor current ripple. Since all buffer cells process the same pulsation power, this means the same power loss for different designs. To maintain the same conduction loss, consider (3.3); when the voltage stress increases, to the first order, the transistor length increases proportionally for higher voltage rating, i.e., $l_{sw} \propto V$; to make the on-resistance the same, the width of the transistor will increase proportionally with voltage stress as well, i.e., $w_{sw} \propto V$. This suggest that the gate capacitance of the transistor increases quadratically with the voltage stress. To maintain the same switching loss, we examine (3.6), (3.5) and (3.4). In (3.6), the transition time t_{tr} is dependent on many factors, but here suppose we want to keep the same $\frac{dv}{dt}$ for the transition, so $t_{tr} \propto V$ and thus $P_{op} \propto V^2 f_s$. In (3.5), the output capacitance C_{oss} is

assumed a linear function of voltage rating, i.e., $P_{op} \propto V^3 f_s$. In (3.4), since we try to keep the inductor current ripple the same, $P_{core} \propto f_s$. For simplicity, we average all the dependency and approximate all the switching loss as $P_{sw} = P_{op} + P_{Coss} + P_{core} \propto V^2 f_s$. This suggest that $f_s \propto \frac{1}{V^2}$ to keep the switching loss the same. Moreover, note that $\Delta I \propto \frac{V}{L f_s}$. To keep the inductor current ripple the same, $L \propto V^3$. Therefore, we can make the approximation that the inductor volume $V_{ind} \propto \frac{1}{2} L I_{max}^2 \propto V^3 I^2$. Therefore, $V^3 I^2$ can be used as a performance metric to compare the inductor volume between different buffer cells. Therefore, we define the inductor volume index (IVI) as $\frac{V^3 I^2}{V_{bus}^3 I_{DC}^2}$, where $V^3 I^2$ is normalized by bus voltage and average DC current.

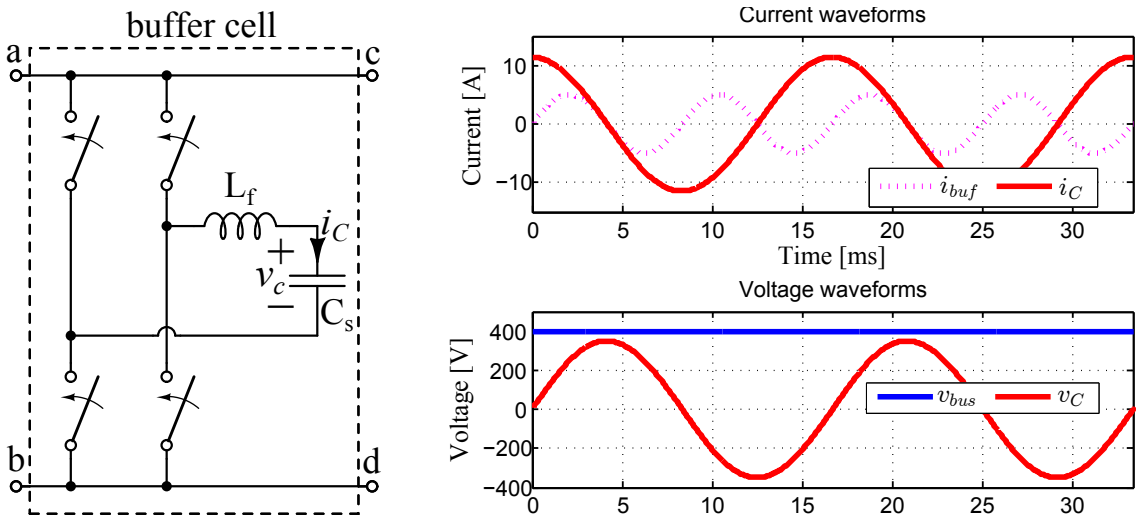
The last metric to consider is the harmonic content in the voltages and currents of the buffer cell. A well-designed buffer cell has smooth 120 Hz or 60 Hz voltage and current waveforms, which makes the design of the local controller easy. The controller only needs to track a single frequency reference at 60 Hz or 120 Hz. Otherwise, certain buffer cells operate with spiky voltage and current waveform, which contains large harmonic contents. These high frequency contents need to be tracked by the controller as well, requiring very high control bandwidth, otherwise the power pulsation is not fully absorbed and there would be ripple on the DC bus. THD is a good indicator of the high frequency contents and the ripple if the buffer failed to track this high frequency content. As will be shown later in this chapter, for converters under high voltage stress and with large filter inductors, obtaining high bandwidth can be very difficult.

3.3 Parallel-connected cell

A magnetic-based bi-directional power converter can be inserted between the DC bus and the energy storage capacitor such that one can control the conversion ratio to discharge the buffer capacitor more deeply while still maintaining a constant bus voltage. Since the energy storage capacitor is still connected across the DC bus but through a buffer converter, this structure is referred to as parallel-connected cell.

3.3.1 Full-bridge buck cell

One example of such a structure is shown in Fig. 3.4, where a full-bridge converter interfaces the energy storage capacitor and the DC bus [40, 51]. Note that this full-bridge converter is referred to as buck cell since it operates in buck mode when charging the capacitor, according to the convention in the literature [16], although it is bi-directional and operates in boost



(a) Schematic. (b) Waveforms.

Figure 3.4: Schematic and operating waveforms of the full-bridge buck cell; $C_s = 87\ \mu F$ used to plot the waveform.

mode when discharging the capacitor.

With proper control, the full-bridge buck cell can absorb the instantaneous difference between i_s and i_{inv} to charge or discharge the energy storage capacitor C_s. The expression of the real-time energy stored by the capacitor is given in (2.2), so the capacitor voltage can be derived as follows,

$$\frac{1}{2}C_s v_c^2 = \frac{P_{dc}}{2\omega cos\phi}[sin(2\omega t + \phi) + \sigma],$$
$$\Rightarrow v_c = \pm\sqrt{\frac{2P_{dc}}{2\omega C_s cos\phi}[sin(2\omega t + \phi) + \sigma]}\ . \tag{3.7}$$

Note that this equation, along with all the equations in this section, is intended not for control purposes but only for analytical purposes. In other words, here it is assumed that a perfect control has been implemented and these equations describe the system behavior under perfect control. In this way, we can evaluate the theoretical performance limit of each buffer cell structure without considering the details of control implementations.

Considering (3.7), for the smallest capacitor volume, $\sigma = 1$ can be chosen. Since it is a full-bridge converter, v_c can be bipolar, so the plus and minus sign in (3.7) can be selected

properly such that v_c is a smooth sine wave, i.e.,

$$\begin{aligned} v_c &= \pm\sqrt{\frac{2P_{dc}}{2\omega C_s cos\phi}[sin(2\omega t+\phi)+1]} \\ &= \pm\sqrt{\frac{2P_{dc}}{2\omega C_s cos\phi}[2cos^2(\omega t+\frac{\phi}{2}+\frac{3\pi}{4})]} \\ &= \sqrt{\frac{2P_{dc}}{\omega C_s cos\phi}}[cos(\omega t+\frac{\phi}{2}+\frac{3\pi}{4})] \ . \end{aligned} \tag{3.8}$$

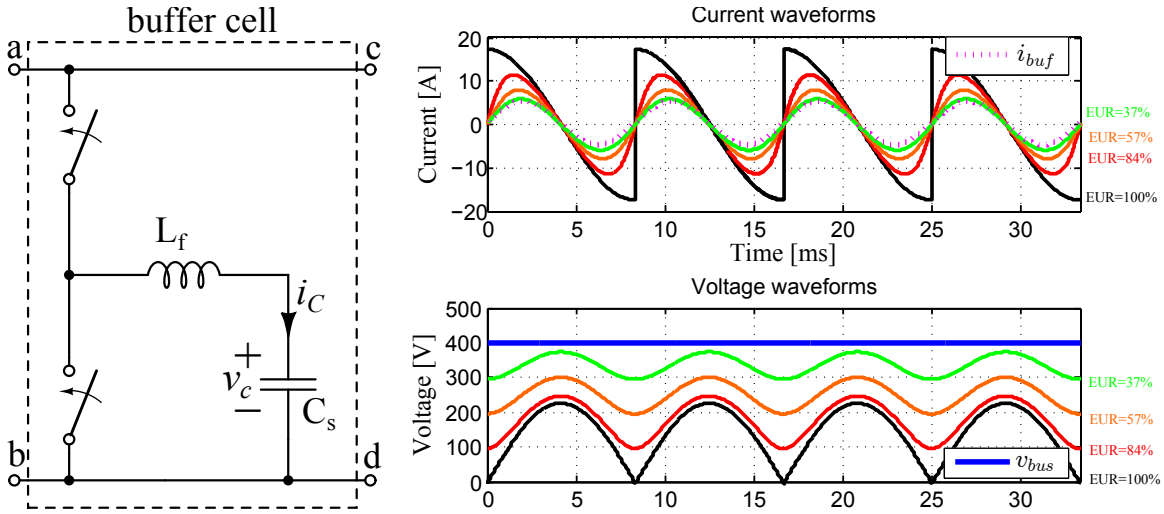
The reason to select a smooth sine wave over other possible waveforms is that such a waveform contains only 60 Hz content and zero THD. This makes the controller design very easy, as it only needs to track 60 Hz reference signals. A PI controller with low bandwidth or a proportional resonant controller with a single resonant frequency at 60 Hz can easily fulfill this task. As shown in Fig. 3.4b, the capacitor can be discharged from the rated voltage down to 0, indicating that the EUR is 100%. The capacitor current i_c is given as

$$i_c = C_s\frac{dv_c}{dt} = \sqrt{\frac{2\omega C_s P_{dc}}{cos\phi}}[sin(\omega t+\frac{\phi}{2}-\frac{\pi}{4})] \ . \tag{3.9}$$

The magnitude of the capacitor voltage can be adjusted by different value of C_s. The lower limit of C_s is that the capacitor voltage magnitude cannot exceed the DC bus voltage, i.e.,

$$\sqrt{\frac{2P_{dc}}{\omega C_s cos\phi}} \leqslant V_{bus}, \tag{3.10}$$

otherwise it will cause over-modulation of the full-bridge converter. Therefore, for the little box challenge design example, C_s in this topology can be as small as 66 μF rated at 400 V. Note that as discussed in Section 2.2, capacitors rated at different voltages have approximately the same power density; this means that the capacitor volume is minimized as long as EUR = 100%, regardless of the capacitor voltage rating. However, a high capacitor voltage magnitude leads to low capacitor current, which does offer benefits in terms of the minimization of TSS and inductor volume. In this structure, both TSS and inductor volume is minimized when (3.10) takes the equal sign. Since the capacitor voltage is bipolar, electrolytic capacitor cannot be used in this structure.



(a) Schematic. (b) Waveforms.

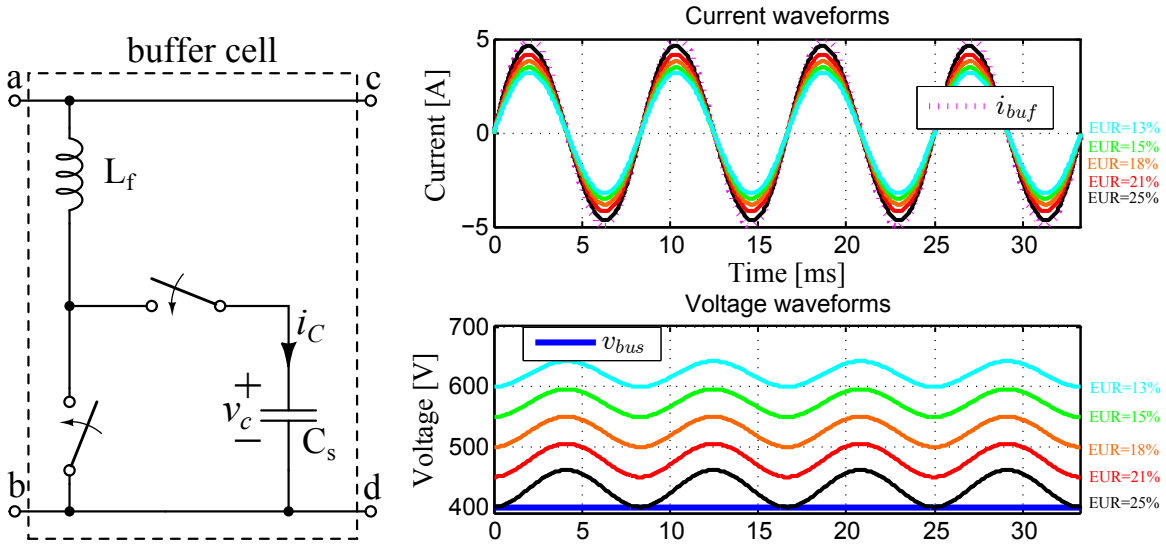
Figure 3.5: Schematic and operating waveforms of the half-bridge buck cell; $C_s = 200\ \mu F$ used to plot the waveform.

3.3.2 Half-bridge buck cell

The switch count of a full-bridge buck cell can be reduced by half to form a half-bridge buck cell, as shown in Fig. 3.5a. In this structure, since one side of the capacitor is permanently connected to the ground, the capacitor voltage has to be unipolar. The analysis for full-bridge buck cell in (3.7) and (3.8) still holds, except that v_c is always positive, i.e,

$$v_c = \sqrt{\frac{2P_{dc}}{\omega C_s cos\phi}} |cos(\omega t + \frac{\phi}{2} + \frac{3\pi}{4})| \ . \tag{3.11}$$

The capacitor current i_c has the same magnitude as given in (3.9), but is now a piecewise function with a discontinuous jump as shown in Fig. 3.5b. For this capacitor voltage waveform, EUR = 100%. However, with EUR = 100%, the capacitor is a rectifier sine wave, which contains not only 120 Hz components but large harmonics. The high harmonic contains in current and voltage impose challenges for controller design. In practice, a voltage bias is often added, i.e., $\sigma > 1$ in (3.7). As illustrated by Fig. 3.5b, this voltage bias decreases EUR but smooths out the spiky capacitor current and voltage, which is helpful for improving switch utilization and reducing inductor size.



(a) Schematic. (b) Waveforms.

Figure 3.6: Schematic and operating waveforms of the half-bridge boost cell; $C_s = 200\ \mu F$ used to plot the waveform.

3.3.3 Half-bridge boost cell

The half-bridge buck cell can be reconfigured to form a half-bridge boost cell [52, 53], as shown in Fig. 3.6a. Since (3.7) is derived from conservation of energy and not specific to buck topology, it is still applicable to half-bridge boost cell except that now

$$v_c > V_{bus}, \tag{3.12}$$

due to the boost configuration. The condition described in (3.12) is achieved by a large value of σ in (3.7), which further decreases the EUR. The voltage stress on the buffer converter components is also higher. A half-bridge buck-boost cell [54] can be derived as well, which imposes no limitation on the capacitor voltage so the EUR can be high, but the voltage stress on the buffer converter is the highest. Both the half-bridge boost cell [55] and half-bridge buck-boost cell suffer higher voltage stress while offering no obvious advantage over the half-bridge boost cell, unless the DC bus voltage on the original system is very low and the rating of the practical switch component is significantly under-utilized. Similarly, the full-bridge boost cell [56] and full-bridge buck-boost cell can be derived, but offer no obvious advantage over the aforementioned topologies.

3.3.4 Half-bridge split-capacitor cell

The capacitor voltage and current for half-bridge buck cell, even after certain voltage bias is added ($\sigma > 1$ in (3.7)), contains large harmonic contents, which imposes challenges to controller design. One topology to eliminate the harmonic content while still having the low switch count of the half-bridge buck cell is the split-capacitor structure [38, 57] as shown in Fig. 3.7a. The energy storage capacitor is split into two equal halves, i.e., $C_1 = C_2 = C_s$. The half-bridge is connected to the mid-point of the split capacitors and control the voltage of that point. Again the energy stored in the capacitors is given in (2.2), therefore

$$\frac{1}{2}C_s v_1^2 + \frac{1}{2}C_s v_2^2 = \frac{P_{dc}}{2\omega cos\phi}[sin(2\omega t + \phi) + \sigma], \tag{3.13}$$

$$v_1 + v_2 = V_{bus}. \tag{3.14}$$

Note that given the constraint (3.14),

$$\frac{1}{2}C_s v_1^2 + \frac{1}{2}C_s v_2^2 \geqslant \frac{C_s V_{bus}^2}{4}, \tag{3.15}$$

where the equal sign is taken when $v_1 = v_2 = V_{bus}$. Therefore,

$$\begin{aligned} \frac{P_{dc}}{2\omega cos\phi}[sin(2\omega t + \phi) + \sigma] &\geqslant \frac{C_s V_{bus}^2}{4} \\ \Rightarrow \sigma &\geqslant 1 + \frac{C_s V_{bus}^2}{4\frac{P_{dc}}{\omega C_s cos\phi}}. \end{aligned} \tag{3.16}$$

Here for the highest EUR, σ should be minimized so we take the equal sign of (3.16). Then (3.13) and (3.14) can be solved as

$$\begin{aligned}
v_1 &= \frac{1}{2}V_{bus} \pm \sqrt{\frac{P_{dc}}{2\omega C_s cos\phi}[sin(2\omega t+\phi)+\sigma] - \frac{1}{4}V_{bus}^2} \\
&= \frac{1}{2}V_{bus} \pm \sqrt{\frac{P_{dc}}{2\omega C_s cos\phi}[sin(2\omega t+\phi)+1+\frac{CV_{bus}^2}{4\frac{P_{dc}}{\omega C_s cos\phi}}] - \frac{1}{4}V_{bus}^2} \\
&= \frac{1}{2}V_{bus} \pm \sqrt{\frac{P_{dc}}{2\omega C_s cos\phi}[sin(2\omega t+\phi)+1]} \\
&= \frac{1}{2}V_{bus} + \sqrt{\frac{P_{dc}}{\omega C_s cos\phi}}[cos(\omega t+\frac{\phi}{2}+\frac{3\pi}{4})], \qquad (3.17) \\
v_2 &= V_{bus} - v_1 \\
&= \frac{1}{2}V_{bus} - \sqrt{\frac{P_{dc}}{\omega C_s cos\phi}}[cos(\omega t+\frac{\phi}{2}+\frac{3\pi}{4})]. \qquad (3.18)
\end{aligned}$$

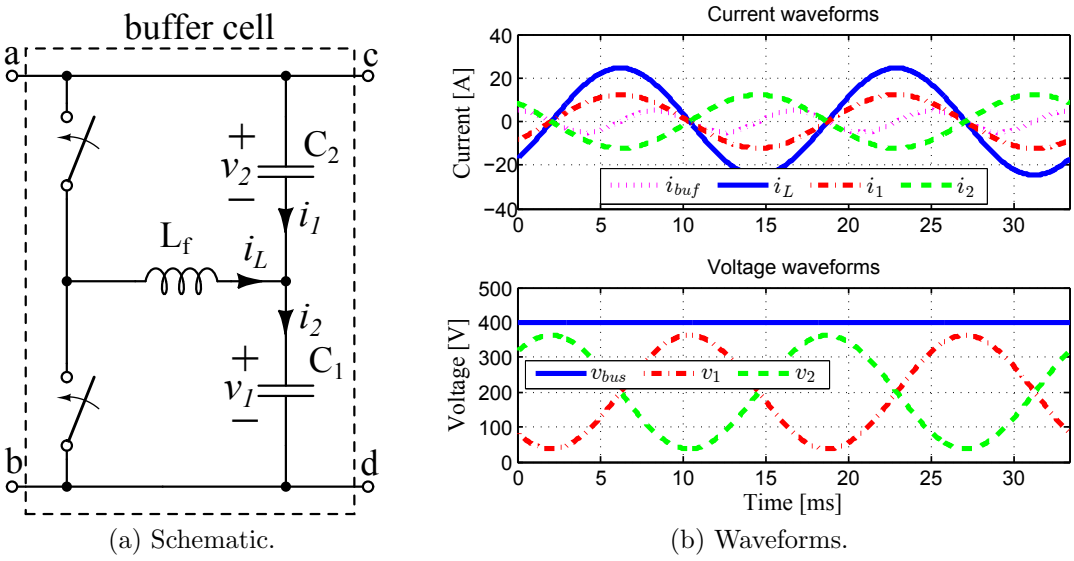
The current through the filter inductor, i_L, is given as

$$\begin{aligned}
i_L = i_2 - i_1 &= C_s\frac{dv_2}{dt} - C_s\frac{dv_1}{dt} \\
&= \sqrt{\frac{4\omega C_s P_{dc}}{cos\phi}}[sin(\omega t+\frac{\phi}{2}-\frac{\pi}{4})] \ . \qquad (3.19)
\end{aligned}$$

The waveforms of v_1, v_2 and i_L are shown in Fig. 3.7b. The magnitude of the capacitor voltage is adjusted through the choice of C_s. Due to the buck topology, v_1 and v_2 must be lower than V_{bus}, i.e.,

$$\sqrt{\frac{P_{dc}}{\omega C_s cos\phi}} \leqslant \frac{1}{2}V_{bus}. \qquad (3.20)$$

When the equal sign in (3.20) is taken, the highest EUR of 25% for this buffer cell structure is achieved. The minimum value of C_s is 132 μF (rated at 400 V) considering the little box challenge design example. As shown in Fig. 3.7b, both the current and voltage of the capacitors are smooth 60 Hz waveforms with no harmonics. However, the current flowing through the filter inductor is very large, resulting in high TSS and IVI.



(a) Schematic. (b) Waveforms.

Figure 3.7: Schematic and operating waveforms of the half-bridge split-capacitor cell; $C_1 = C_2 = C_s = 200\ \mu F$ used to plot the waveform.

3.3.5 Analysis and comparison

The performance metrics of all the aforementioned buffer cells are summarized in Table 3.1. For half-bridge buck converter and half-bridge boost converter, these metrics are dependent on the DC bias voltage on the energy storage capacitor as well as the capacitance. The performance metrics as a function of DC bias voltage is plotted in Figs. 3.8 to 3.10 for the difference values of C_s. As the DC bias voltage increase, the EUR decreases, and the THD in the signal decreases as well as the voltage and current becomes smoother and smoother as shown in Fig. 3.5b and Fig. 3.6b. The TSS and IVI first decrease with DC bias voltage for the buck cell as the current stress in the converter decreases, and increase with DC bias voltage for the boost cell as the voltage stress increases. Note that a certain range of bias voltage DC bias voltage (marked by colored area in Fig. 3.8 to Fig. 3.10) is not viable with either buck or boost converter because it results in capacitor voltage both above and below bus voltage. The minimum point of TSS and IVI on the curve is at the left boundary point, which corresponds to the point where in buck configuration the highest voltage on the energy storage capacitor within a cycle is exactly the bus voltage.

The results in Table 3.1 and Figs. 3.8 to 3.10 reveal the tradeoff between EUR and other performance metrics. While EUR is the motivation to study active decoupling, the buffer structure with 100% EUR will not give the smallest overall size due to the large volume of inductors and power loss of the converter. The full-bridge buck cell has the best EUR but relatively large TSS and IVI. The half-bridge split-capacitor cell aims at reducing the

Table 3.1: Performance metrics of various buffer cells calculated with the little box challenge design example

Buffer cell	max EUR	min current stress	min voltage stress	min TSS	IVI	THD	capacitor polarity
full-bridge buck	100%	10 A	400 V	4×4000 VA	4	0	bipolar
half-bridge buck	about 100% to 15%, , see Fig. 3.8	$\leqslant$10 A	400 V	see Fig. 3.8	see Fig. 3.8	see Fig. 3.8	unipolar
half-bridge boost	about 15% to 0%, see Fig. 3.8	10 A	$\geqslant$400 V	see Fig. 3.8	see Fig. 3.8	see Fig. 3.8	unipolar
half-bridge split-capacitor	25%	20 A	400 V	2×8000 VA	16	0	unipolar
Stacked switched-capacitor cell	about 10% to 50%, see Fig. 3.12	5 A	$\ll$400 V	high	NA	NA	bipolar
Series-connected (for parameters in Fig. 3.15, not optimized)	33.6%	5 A	100 V	4×500 VA	0.0156	0	unipolar
Series-stacked (for parameters in Sec. 4.2, not optimized)	42%	5 A	90 V	4×450 VA	0.0114	0	unipolar

switch count of the full-bridge buck cell but actually has worse performance metrics. The half-bridge buck cell and half-bridge boost cell allow for flexibility in adjusting the balance between EUR and other parameters and the right tradeoff will result in the smallest volume among all parallel connected cells. However, harmonics in the voltage and current signal remains a control challenge for these structures.

Certain variations of the parallel-connected cells might offer small advantages over other variations, but parallel-connected cells in general suffer severe problems. The buffer converter is directly connected to the DC bus and thus under that full voltage stress of the DC bus voltage. Consequently, for the added buffer converter, high-voltage, relatively slow-switching transistors have to be used, which limits the achievable switching frequency, leading to a large filter inductor, L_f. In other words, the voltage stress of the parallel-connected cells is lower bounded by the bus voltage and the current stress is lower bounded by the DC current. Therefore, it is not possible to build a parallel connected cell with IVI < 1 or TSS $< V_{bus} \times I_{dc}$. Note that as discussed in Section 2.2, the energy density of inductors are 500 to 1000 times lower than that of capacitors. The volume reduction from the smaller energy storage capacitor is often offset by the volume overhead introduced by the buffer converter itself. Most comparable parallel connected cell design in the literature [38, 41, 51–54] have filter inductors on the order of several mH, resulting in a very large inductor volume.

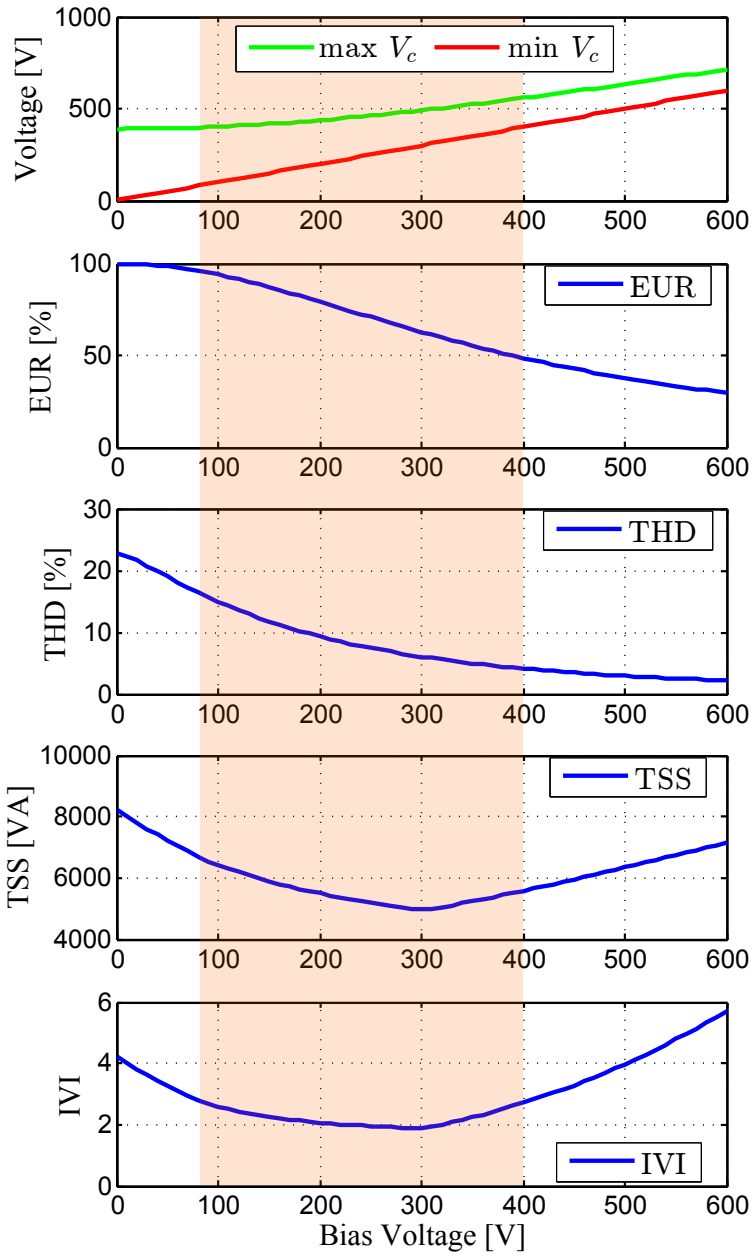


Figure 3.8: Voltage swing range of the energy storage capacitor, EUR, THD, TSS and IVI of half-bridge buck cell and half-bridge boost cell as a function of DC bias voltage in the energy storage capacitor. These plots are generated with $C_s = 70$ μF.

Another major limitation of parallel-connected cells is the efficiency penalty incurred by the buffer converter. As illustrated in (2.1), an average of $\frac{2}{\pi}P_{ave}$ power pulsation is flowing into and then out of the buffer cell in each cycle. Therefore, to the first order, the overall

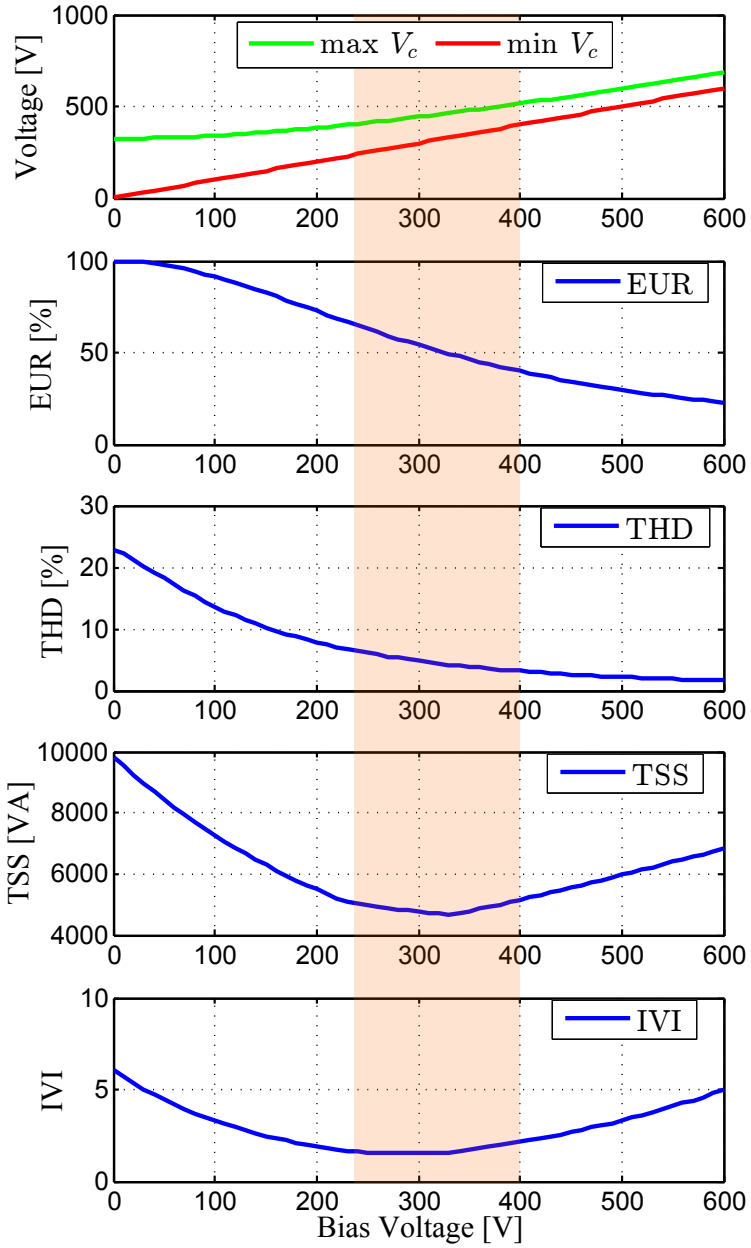


Figure 3.9: Voltage swing range of the energy storage capacitor, EUR, THD, TSS and IVI of half-bridge buck cell and half-bridge boost cell as a function of DC bias voltage in the energy storage capacitor. These plots are generated with $C_s = 100$ μF.

efficiency of the entire AC-DC converter is approximately

$$\eta \approx \eta_{main} - \underbrace{\frac{2}{\pi}(1 - \eta_{buf})}_{\text{efficiency penalty}} , \tag{3.21}$$

where η_{main} is the efficiency of the inversion/rectification stage and η_{buf} is the efficiency

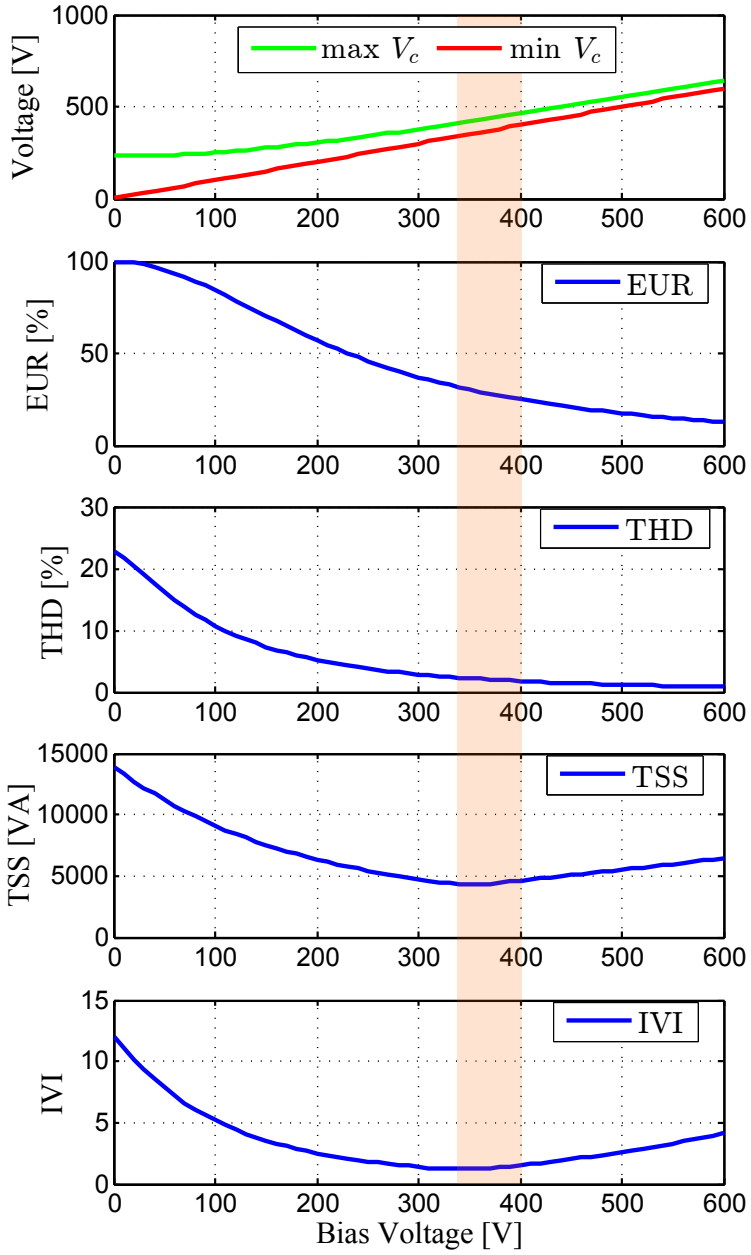


Figure 3.10: Voltage swing range of the energy storage capacitor, EUR, THD, TSS and IVI of half-bridge buck cell and half-bridge boost cell as a function of DC bias voltage in the energy storage capacitor. These plots are generated with $C_s = 200$ μF.

of the buffer converter. Even if the buffer converter can be made efficient through careful design (which is challenging given the high TSS), since it is processing a large portion of the total power, it can still incur significant power loss. High power loss typically results in larger heat sinking devices (heat sink and fans), which further undermine the goal of high power density.

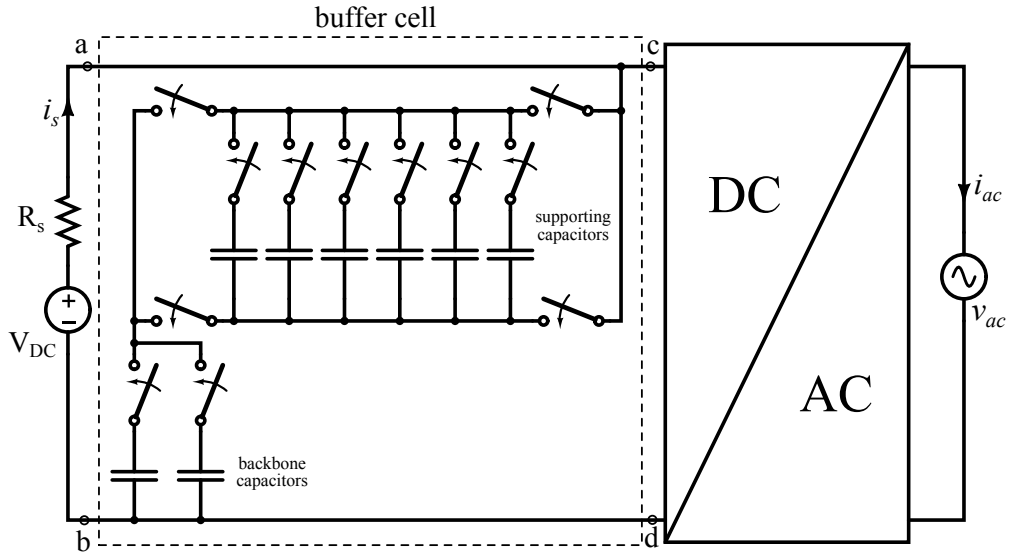


Figure 3.11: Schematic of a stacked switched capacitor cell [13, 44]. Note there are n backbone capacitors mainly for energy storage and m supporting capacitors mainly for voltage regulation.

To summarize this analysis, EUR is typically not the most important metric when designing for high power density. Since inductor volume often dominates the overall volume, it is more important to design for low TSS and IVI while maintaining a reasonable EUR. The buffer cells to be discussed next follows this method.

3.4 Stacked switched-capacitor cell

An alternative approach to magnetic-based parallel-connected cells is the stacked switched-capacitor (SSC) buffer [13, 44]. One embodiment of the SSC buffer is shown in Fig. 3.11, which consist of two backbone capacitors and six supporting capacitors. The operation of the SSC buffer is very involved and interested readers are referred to [13] for details.

On a very high level, the SSC buffer consists of an array of capacitors and switches. As the capacitors charge and discharge, the SSC buffer reconfigures the array in different series and parallel combinations to regulate the DC bus voltage. Obviously, this configuration is free of magnetic components, so large inductor volume is no longer a concern. Compared to a magnetic-based converter that continuously processes the buffer power, the SSC buffer takes advantage of the natural stacking of capacitor voltages to maintain the DC bus voltage and only exercises the switches a few times in each line cycle to adjust the stacking. Hence, the power loss associated with the SSC architecture is greatly reduced.

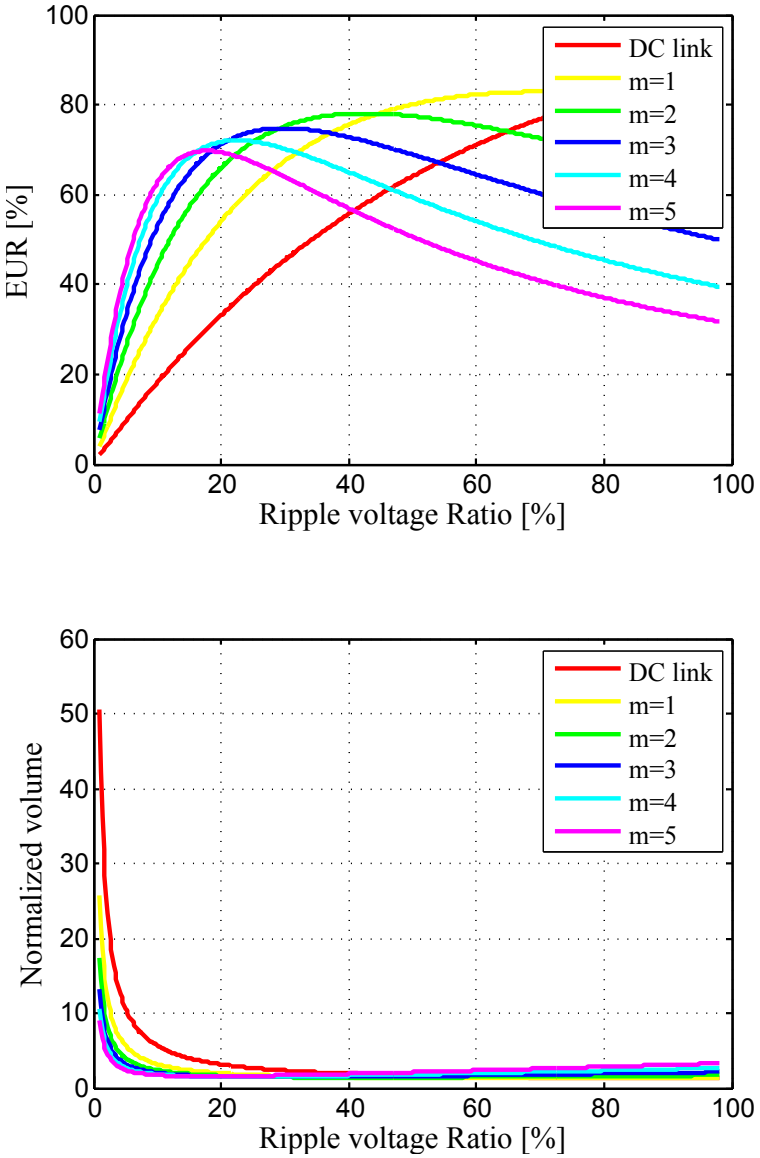


Figure 3.12: The energy utilization ratio (EUR) and SSC capacitor volume (normalized over the volume at 100% EUR with passive DC link capacitor) as a function of the ripple voltage ratio on the DC bus. The number of backbone capacitors is one and the number of supporting capacitors is m shown in the legend. The EUR and normalized volume of passive DC link capacitor solution is plotted as a reference.

While magnetic-based parallel-connected cells can theoretically eliminate the DC bus ripple completely, SSC only limits the ripple to certain percentage by design. Therefore, similar to the passive DC link capacitor decoupling, the EUR of SSC is limited by the allowed ripple on the DC bus. The EUR and normalized capacitor as a function of the allowed ripple on the DC bus is plotted in Figs. 3.12 to 3.14 for different number of backbone and supporting capacitors. SSC offers significant improvement over passive DC link capacitor, but the EUR

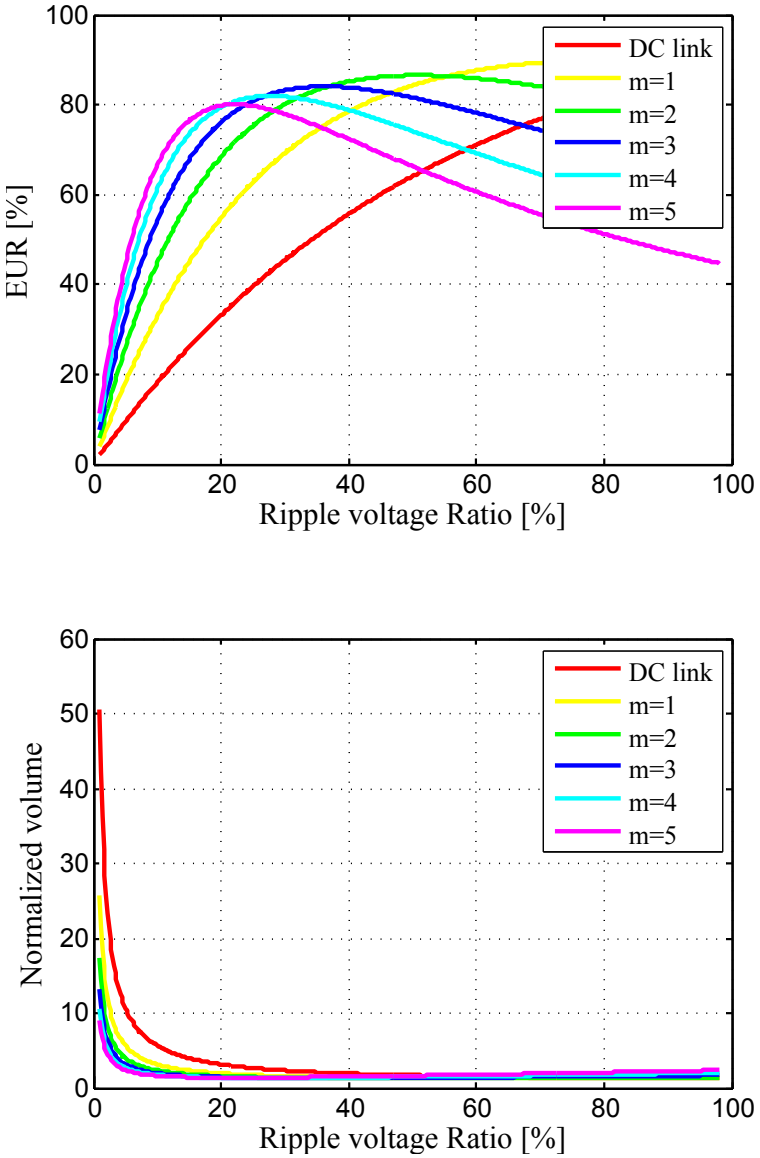


Figure 3.13: The energy utilization ratio (EUR) and SSC capacitor volume (normalized over the volume at 100% EUR with passive DC link capacitor) as a function of the ripple voltage ratio on the DC bus. The number of backbone capacitors is two and the number of supporting capacitors is m shown in the legend. The EUR and normalized volume of passive DC link capacitor solution is plotted as a reference.

is relatively low when only a small ripple is allowed on the DC bus. This is because the configurations of SSC are discrete in nature, so the bus voltage experiences a discontinuous jump whenever the SSC reconfigures. To meet a strict ripple requirement (e.g., a few percent), a complicated circuit with a large number of backbone and supporting capacitors has to be built. The total switch count of SSC is given as $n+m+4$, so the number of transistors is large, leading to a high TSS although the voltage stress on each individual transistor is

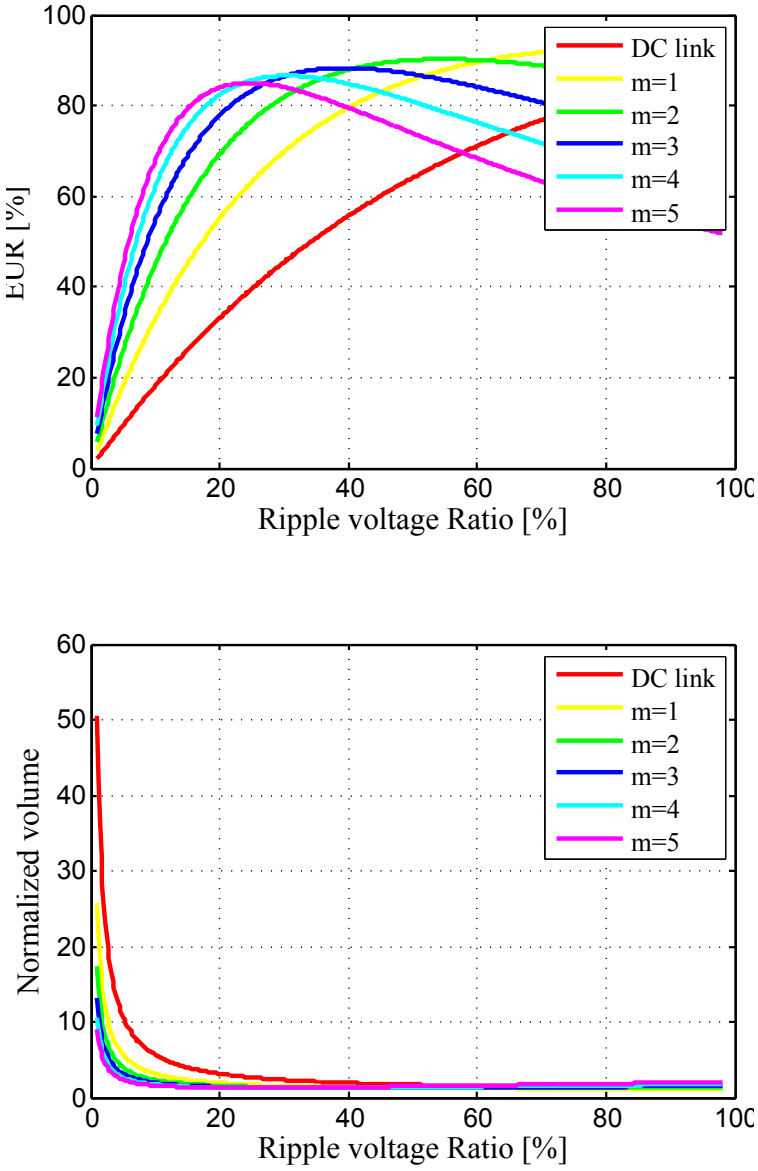
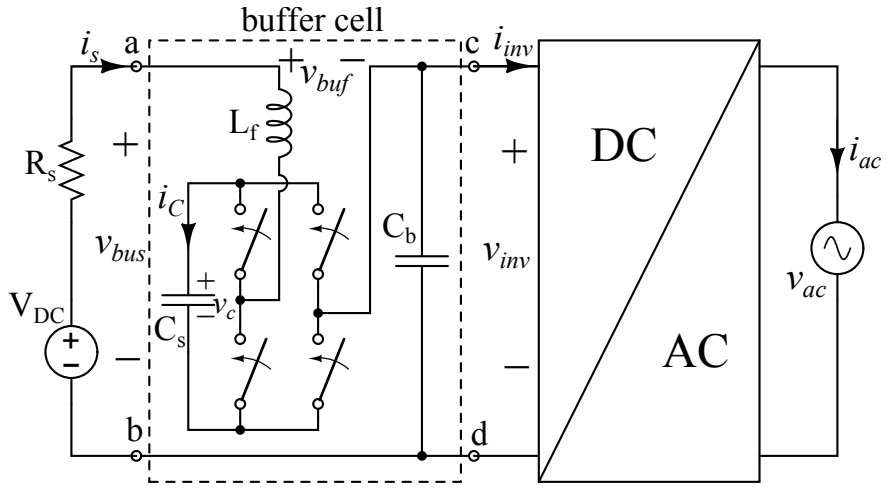


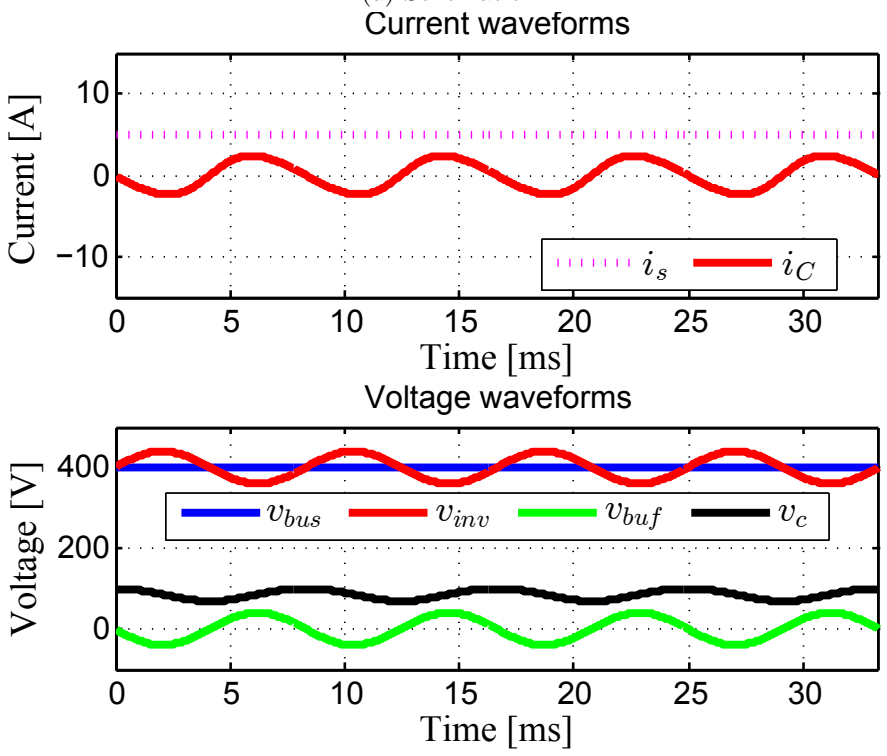
Figure 3.14: The energy utilization ratio (EUR) and SSC capacitor volume (normalized over the volume at 100% EUR with passive DC link capacitor) as a function of the ripple voltage ratio on the DC bus. The number of backbone capacitors is three and the number of supporting capacitors is m shown in the legend. The EUR and normalized volume of passive DC link capacitor solution is plotted as a reference.

reduced compared to magnetic-based parallel connected cells. Therefore, despite the fact that no inductor is needed in SSC, the large number of switches and their auxiliary circuits (i.e., the signal level shifting and gate driving circuit) occupy a large PCB area, undermining the goal of high energy density. The above analysis is summarized in Table 3.1.

3.5 Series-connected cell



(a) Schematic.



(b) Waveforms.

Figure 3.15: Schematic and operating waveforms of the series connected cell (series voltage compensator in [58, 59]). The waveform is simulated with $C_s = 200$ μF and $C_b = 150$ μF. The DC bias on C_s is 100 V.

Despite the negative impact on the volume, inductors are generally necessary in active decoupling buffers to continuously regulate the bus voltage and minimize ripple. However, if we want to avoid high voltage stress on the inductor, the buffer converter cannot be

connected across the DC bus. A series-connected buffer cell is proposed [58, 59] as shown in Fig. 3.15a. For the parallel-connected cell and SSC cell, the inversion stage is directly interfaced with the DC bus, i.e., $v_{inv} = v_{bus} = v_{buf}$ in Fig. 3.15; series-connected cell, however, is connected in series with the inverter, i.e., $v_{bus} = v_{buf} + v_{inv}$. The bulk energy storage capacitor, C_b, is allowed to have a relatively large ripple to improve EUR, while the a series-connected full-bridge converter with a supporting capacitor, C_s, changes its output voltage v_{buf} complimentary to the ripple on C_b (the ripple in v_{inv}), such that the DC bus voltage is maintained constant, as shown in Fig. 3.15b. Note that this is similar to SSC in the sense that the stacking of two capacitors with complimentary voltage maintains the bus voltage. C_b is similar to the backbone capacitors and C_s is similar to the supporting capacitors in SCC. The difference is that now the voltage of C_s is regulated through a full-bridge converter instead of directly stacking on top of C_b, so very smooth and continuous regulation can be achieved. The series connection of the buffer converter allows the buffer converter to see only the voltage ripple magnitude, so the voltage stress on the buffer converter and its inductor is greatly reduced. Moreover, the buffer converter only process the power corresponding to the ripple voltage, so the efficiency penalty on the overall system is also reduced. The performance metrics calculated for the series-connected cell is listed in Table 3.1. Note that this result is calculated for the particular parameter selection given in Fig. 3.15, which has not been optimized. Even so, series-connected cells have shown superior performance especially on TSS and IVI. A systematic procedure to optimized series-connected cell is still an area of ongoing research.

Note that this configuration does affect the operation of the inversion stage to some extent. The input to the DC side of the inversion stage is no longer a constant DC but with a large 120 Hz waveform. This by itself is usually not a problem if the control loop of the inversion stage has enough bandwidth. However, the voltage on the DC side has to be always higher than the AC side on an H-bridge converter. This means the voltage swing on C_b is limited. For example, for the little box challenge design, the voltage amplitude of the AC output has to be 340 V. This effectively limits the voltage swing of C_b to only 60 V above and below the 400 V bus, as shown in Fig. 3.15b. Therefore, although series-connected cell offers some flexibility to tradeoff EUR for TSS and IVI, the range of tradeoff is limited. If the headroom between AC side voltage and DC side voltage is smaller due to system requirements (e.g., some PFC front ends under extreme cases may take high line voltage of 264 V RMS AC and output 375 V DC), then the room left for series-connected optimization might be too small. After all, the ripple is only reduced on one side while the other side that is directly connected to the capacitor lacks voltage regulation, which is unacceptable in many applications.

3.6 Dependent decoupling buffer

All the aforementioned buffer solutions in this chapter are classified as "independent decoupling" as their operation is independent of the AC/DC converter operation. The "independent decoupling" buffers, despite their topological variations, all serve as an inherently "add-on" component to the converter system. This "add-on" characteristics determines that all "independent decoupling" buffers suffer at least from two shortcomings: the buffer stage requires extra active components to build (i.e., increased active component count, not only the power transistors but also components for control implementation); the buffer stage will always reduce the overall efficiency of the system (despite the fact that this efficiency reduction might be very small, as in the series-stacked buffer architecture to be presented).

Another class of active buffer solutions, referred to as "dependent decoupling" here, has been proposed to solve these shortcomings. This class of solutions feature the integration of the active buffer hardware and control into the inversion/rectification stage, to reduce the switch count and to improve the overall efficiency. Now since the two parts are merged, their control and operation are no longer independent but tightly coupled, thus referred to as "dependent decoupling".

"Dependent decoupling" is closely related to "independent decoupling" in terms of circuit structure. In fact, one can often derived a "dependent decoupling" structure from its "independent decoupling" counterpart, or vice versa. This derivation is often referred to as multiplexing. As an example, one can start with a half-bridge split-cap buffer cell and a full-bridge inverter given in Fig. 3.16; the adjacent two half-bridge structures in the buffer cell and full-bridge inverter has certain hardware redundancy and can be multiplexed together. Furthermore, the inductor in the full-bridge inverter can split into two halves (same in total inductance and inductor volume) and one-half can be shared with the buffer cell to eliminate the original buffer cell inductor. The resulting structure has been proposed in [41, 43] and referred to as active-filter-integration (AFI). The operation and control of AFI has been well studied and interested readers are referred to [43] for details. It has been shown in [43] that unlike "dependent decoupling" buffers that always reduce the overall system efficiency, AFI can actually improve the system efficiency at heavy load range, although it still reduces system efficiency at light load range.

Although the operation of "dependent decoupling" solutions will not be discussed in detail, it should be pointed out that the reduced component count in these structures comes at the cost of reduced operation flexibility. The essence of "dependent decoupling" is to modulate the common mode voltage of the AC output. The energy storage capacitor is moved to the output to be charged and discharged by the common mode voltage to provide energy

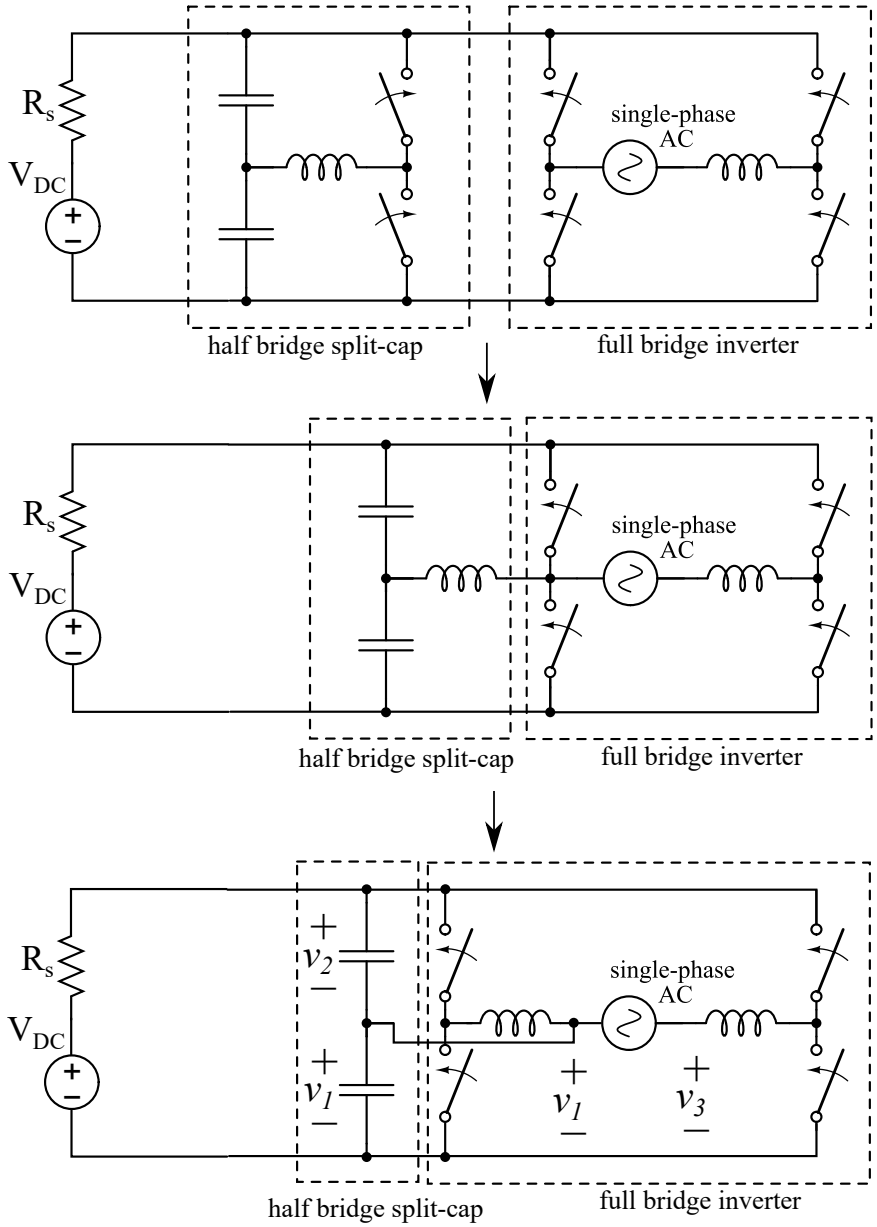


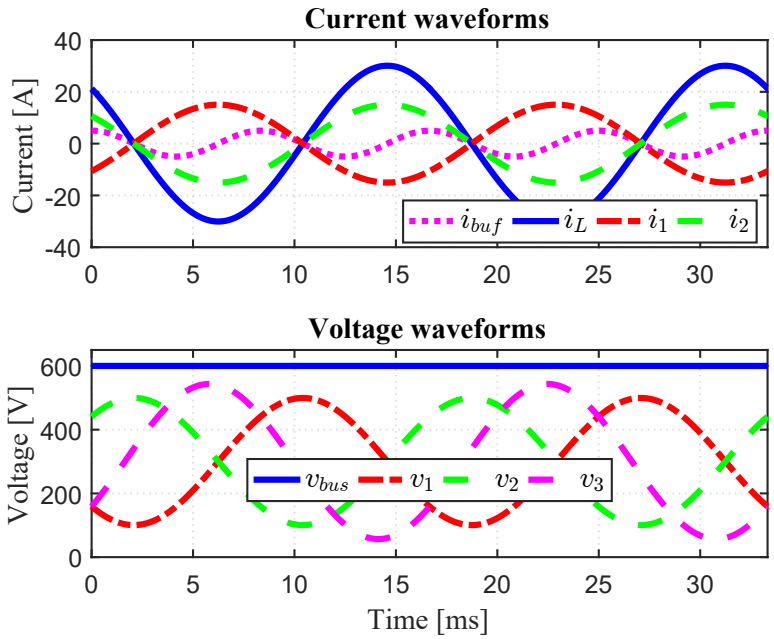
Figure 3.16: Step-by-step derivation of a dependent decoupling buffer structure from a half-bridge split-cap independent decoupling solution.

buffering. This means that the output common mode voltage is fully determined by the buffering requirement and is no longer an extra degree of freedom in the design. Recall that in full-bridge inverter it is preferable to set the common mode output voltage to zero to reduce the voltage stress as well as common mode EMI. Now with the common mode voltage used for energy buffering, the DC bus voltage must be raised to a higher value to allow enough headroom for the AC output waveform.

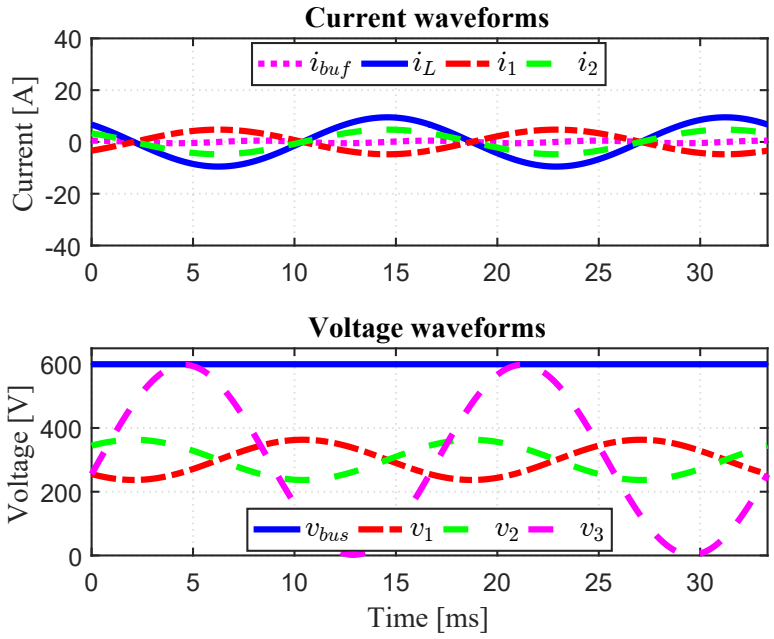
Take the AFI structure as an example, whose operation waveform is plotted in Fig. 3.17.

The full load operating condition is the same as the independent half-bridge split-cap buffer discussed before in Fig. 3.7 (i.e., per little box challenge requirements), but the bus voltage in the AFI structure has to be raised to accommodate higher voltage. In other words, in Fig. 3.17, the swing of v_1 and v_2, which is determined by the energy buffering requirement (or equivalently, by the load power level), remains the same as in Fig. 3.7b. However, since one side of the output terminal is tied to v_1, the other side of the output terminal, v_3, must go to higher voltage on top of v_1 to generate high enough AC output voltage. The worst-case condition happens at light load, when the v_1 remains close to half of the DC bus voltage. The bus voltage needs to be twice as high as the AC output amplitude in this case, which far exceeds the commonly used 400 V bus voltage. A DC bus voltage higher than necessary would require higher-voltage-rated devices in the inversion/rectification stage. These devices as well as the high voltage stress itself would increase the power loss in the inversion/rectification stage. Therefore, although AFI can improve heavy load efficiency if the system is fixed, the system could have been designed to be more efficient without AFI. The high voltage stress is especially a problem for the FCML to be discussed in later chapters, so in this work "dependent decoupling" will not be further considered.

Note that AFI is not the only "dependent decoupling" buffer and many others can be derived similarly from their independent counterparts. For example, the structure proposed in [60] can be derived from an independent half-bridge buck buffer cell. The above remarks on AFI generally apply to other "dependent decoupling" buffers as well.



(a) Full load operation of AFI.



(b) Light load operation of AFI.

Figure 3.17: Operating waveforms of the AFI structure.

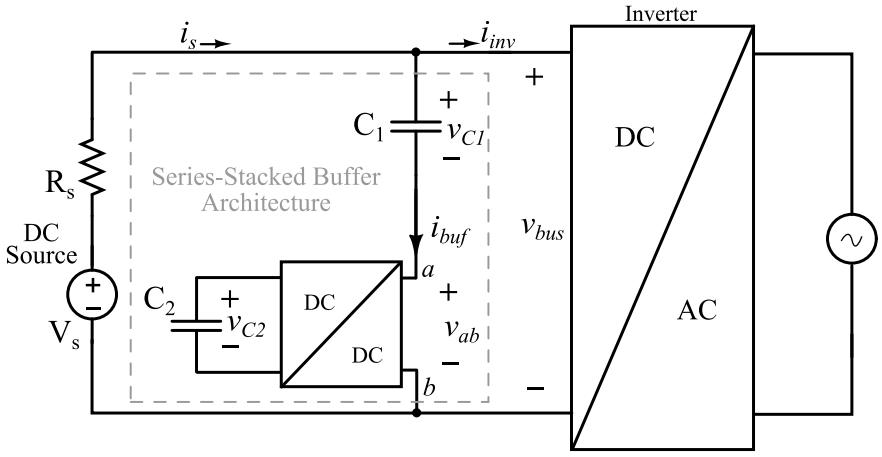
CHAPTER 4

OPERATION PRINCIPLE OF THE SERIES-STACKED BUFFER ARCHITECTURE

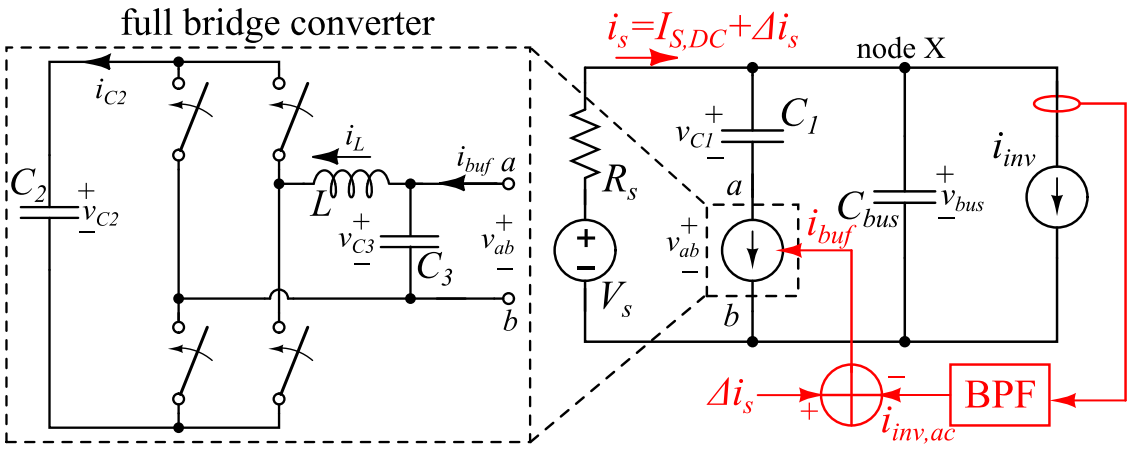
Based on the review in Chapter 3, we can make the observation that a good buffer cell for independent decoupling should make use of magnetic-based converters for its continuous voltage regulation capability to meet strict ripple requirement while allowing for flexible tradeoff between the energy storage capacitor volume and inductor volume of the magnetic-based converter. Specifically, the full voltage stress of the DC bus should not fall all on the buffer converter; instead, the voltage stress should be blocked mostly by the energy storage capacitor while the buffer converter only withstands the ripple voltage; the design should allow free adjustment of the ripple voltage for the best balance between capacitor and inductor volume. The buffer should be highly efficient, ideally as efficient as the capacitor passive decoupling solution, to avoid degradation of the system efficiency. The series-stack buffer presented in this chapter is such a structure. It allows for flexible tradeoff across a very wide range to achieve very high efficiency and power density while tightly regulating the DC voltage.

4.1 Analysis of operation

The schematic of the proposed buffer architecture is shown in Fig. 4.1. Here, C_1 is the main energy storage capacitor and is allowed a relatively large ripple (e.g., 20% or more of the nominal voltage) to improve its EUR. Unlike conventional active decoupling solutions that interface the DC bus through a parallel-connected buffer converter, C_1 is stacked in *series* with the buffer converter across the DC bus. With proper control (the control implementation is presented in Chapter 5), the buffer converter can behave as a controlled bidirectional current source to source/sink any instantaneous current difference between the DC side current i_s and the AC side current i_{inv}. Capacitor C_1 is then charged and discharged in series with the converter to buffer the energy. Capacitors C_3 and C_{bus} are both small filter capacitors to absorb the switching transients, whose effect can be ignored at line frequency. With the aforementioned current control, the voltage across node a and b (i.e., v_{ab}) naturally



(a) High-level schematic of the proposed buffer architecture.



(b) Medium-level schematic of the proposed buffer architecture with a simplified circuit schematic of the full-bridge converter implementations. The DC/AC converter is abstracted as a current sink. The buffer control scheme is highlighted in red color.

Figure 4.1: Diagrams of the proposed buffer architecture.

varies contrary to the voltage change of C_1 (i.e., $v_{C1} + v_{ab} = \text{constant}$). Moreover, since the instantaneous current difference (i.e., i_{buf}) sums up to zero within a twice-line-frequency cycle, the energy is balanced each cycle and the buffer converter does not need an active energy source to fulfill its current source function. A support capacitor C_2 is used to maintain the necessary voltage for the correct operation of the buffer converter. Waveforms illustrating the aforementioned operation is shown in Fig. 4.2.

There are several possible topological implementations of the buffer converter, among which the full-bridge topology and the non-inverting buck-boost topology show the most promise. A full-bridge implementation is shown in Fig. 4.1b and is used in the following analysis to illustrate the operation of the proposed buffer architecture. The analysis presented here is general. It applies to non-inverting buck-boost and other topologies as well.

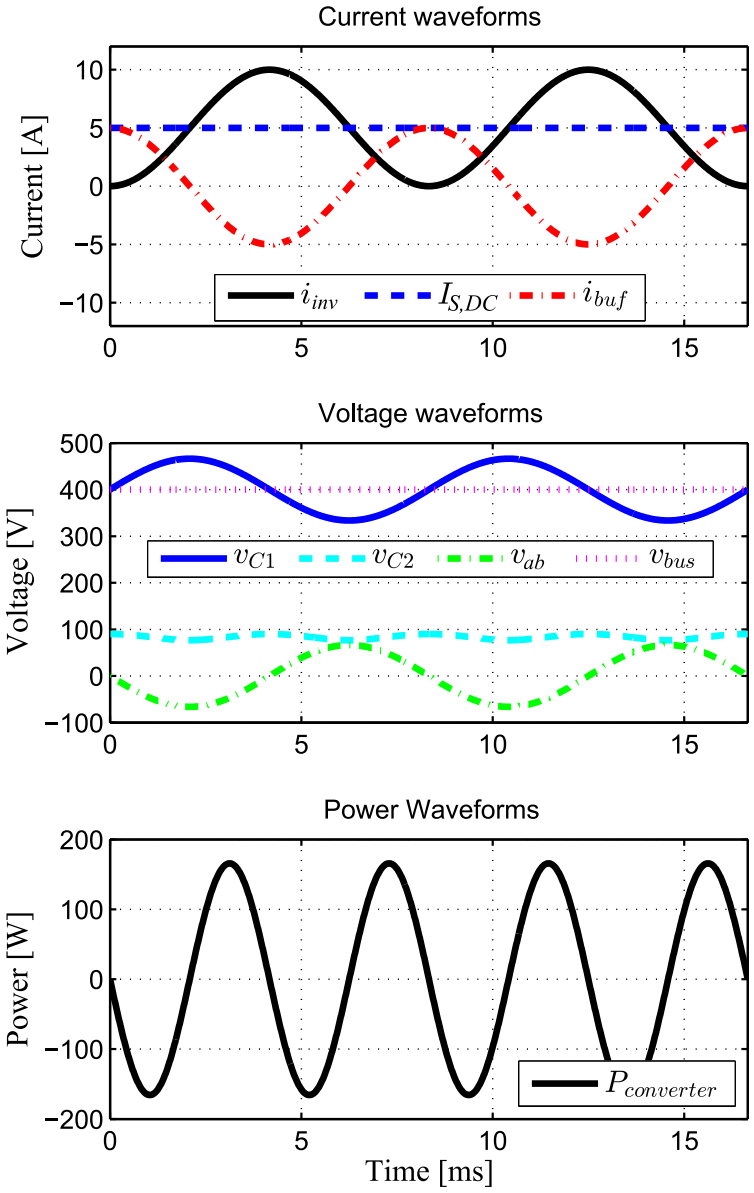


Figure 4.2: Key waveforms illustrating the operation of the proposed buffer. The waveforms are calculated for the little box challenge design exampled outlined in Section 1.1 (2 kW load power, 400V bus voltage).

Consider a single-phase inverter with unity power factor, as shown in Fig. 4.1a. The inverter input power is given as

$$P_{inv,in} = v_{bus} i_{inv}, \tag{4.1}$$

where v_{bus} is the DC bus voltage and i_{inv} is the current flowing into the inverter. Its output power is given as

$$P_{inv,out} = v_{ac} i_{ac} = V_{AC} sin(\omega t) \times I_{AC} sin(\omega t) = V_{AC} I_{AC} \frac{1 - cos(2\omega t)}{2}, \tag{4.2}$$

where ω is the line angular frequency, V_{AC} and I_{AC} are the AC output voltage and current amplitude, respectively. Assuming a certain inverter efficiency η, it is easy to show that

$$P_{inv,out} = \eta P_{inv,in} \Rightarrow i_{inv} = \frac{\eta V_{AC} I_{AC}}{v_{bus}} \frac{1 - cos(2\omega t)}{2}. \tag{4.3}$$

Given a constant v_{bus}, the inverter input current i_{inv} resembles the shape of a shifted sine wave, whose average equals the average input current from the DC source, $I_{S,DC}$ (i.e., $< i_{inv} >= I_{S,DC}$), as shown by the current waveforms in Fig. 4.2. To maintain a constant DC bus voltage, the current through the buffer branch, i_{buf}, should take up the instantaneous difference between i_{inv} and $I_{S,DC}$. In our proposed architecture, this can be achieved with appropriate control of the full-bridge converter, as presented in Chapter 5. Then, by KCL at node X in Fig. 4.1b, the small filter capacitor C_{bus} should have no current (except for the switching frequency filtering) and therefore maintain a constant bus voltage. The instantaneous *change* of charge and voltage on C_1 is given by

$$\Delta q_1 = \int i_{buf} dt, \quad \Delta v_{C1} = \frac{\Delta q_1}{C_1}. \tag{4.4}$$

Since the aforementioned current control ensures a constant bus voltage,

$$\Delta v_{ab} = -\Delta v_{C1}. \tag{4.5}$$

As will be shown in Section 6.1, the buffer converter uses a small inductor and is designed to switch at a high frequency (several hundred kHz). Its switching ripple and other dynamics can thus be ignored in the line frequency analysis. Assuming bipolar pulse width modulation (PWM) control of the buffer converter, the voltages of its two ports (i.e., v_{ab} and v_{c2} in Fig. 4.1b) can be related by the converter duty ratio d as

$$\frac{v_{ab}}{v_{C2}} = 2d - 1 \ . \tag{4.6}$$

Similarly, the currents of the two ports of the full-bridge converter in Fig. 4.1b can be related by the converter duty ratio d as

$$\frac{i_{ab}}{i_{C2}} = \frac{i_{buf}}{i_{C2}} = \frac{1}{2d-1} \ , \tag{4.7}$$

since the buffer current i_{buf} flows through port ab. From (4.7) and (4.4) , the change of charge on C_2 can be obtained as

$$\Delta q_2 = \int i_{C2} dt = \int (2d-1) i_{buf} dt = (2d-1)\Delta q1. \tag{4.8}$$

Thus, the instantaneous charge on C_2 is given as

$$q_2 = Q_{2,init} + \Delta q_2 = Q_{2,init} + (2d-1)\Delta q_1, \tag{4.9}$$

where $Q_{2,init}$ is the initial charge on C_2 at the beginning of every twice-line-frequency cycle. Moreover, from (4.6) it can be derived that

$$v_{C2} = \frac{1}{2d-1} v_{ab} = \frac{1}{2d-1}(\Delta v_{ab} + V_{ab,init}), \tag{4.10}$$

where $V_{ab,init}$ is the initial voltage across terminal a and b at the beginning of every twice-line-frequency cycle. As discussed in Chapter 5, $V_{ab,init}$ can be set by appropriate control in a practical implementation. Choosing $V_{ab,init} = 0$ by design and substituting (4.4) and (4.5) into (4.10) gives

$$v_{C2} = -\frac{1}{2d-1}\frac{\Delta q_1}{C_1}. \tag{4.11}$$

Combining (4.11) and (4.9) through $q_2 = C_2 v_{C2}$ renders

$$\Delta q_1 m^2 + Q_{2,init} m + C_2 \frac{\Delta q_1}{C_1} = 0, \tag{4.12}$$

where $m = 2d - 1$ is the conversion ratio of the full-bridge converter. The above analysis applies to non-inverting buck-boost converter and other converter topologies as well, except that the conversion ratio m needs to be changed accordingly.

In (4.12) the only operation-dependent variable is Δq_1, which is fully determined by the inverter current i_{inv} according to (4.4). $Q_{2,init}$, C_2 and C_1 are all selected by the component and control design choices. Solving (4.12) for m will give the instantaneous conversion ratio and duty ratio of the buffer converter, from which all the voltages and current waveforms can be calculated according to (4.5) through (4.11). The waveforms in Fig. 4.2 are obtained

through these calculations.

4.2 Numerical example

In order to illustrate the operation of the proposed buffer architecture and to establish a common baseline for comparison, consider a numerical example according to the specifications outlined in the Google/IEEE little box challenge. The complete specifications are listed in Table 1.1 and relevant ones are repeated here for convenience: a 2 kW, 60 Hz inverter/rectifier with 400 V DC bus voltage and up to 3% ripple (±6 V around 400 V) [8]. Note that this example is chosen only for illustrative purposes; the proposed architecture is applicable to a much larger voltage and power range. If one can design an ideal magnetic-based buffer converter to charge and discharge the buffer capacitor(s) between 406 V to 0 V, it can be calculated from (2.5) that only 64 μF of buffer capacitor is required (at the price of larger buffer converter volume and lower efficiency, as discuss in Section 2.4). This capacitor volume represents the ideal case where the rated voltage is fully utilized for energy storage. On the opposite extreme, if only a conventional passive decoupling solution is used, at least 1.1 mF is required for the DC bus capacitor bank to maintain less than 3% ripple. Moreover, if practical ripple current limitations of electrolytic capacitors are taken into consideration in a passive filtering solution, even larger capacitors are typically needed. Practical active decoupling solutions will result in capacitor requirement somewhere between the two aforementioned extremes.

If in this example, we choose to allow a 130V (32%) ripple on C_1, then its capacitance is determined through (4.4) to be 100 μF. Furthermore, C_2 is chosen to be 430 μF (exact design guideline for C_2 sizing is provided in Section 4.3). Using the equations derived in Section 4.1, all the component voltages and currents for this 2 kW example can be calculated. Figure 4.2 plots some key voltage waveforms calculated in Matlab to illustrate the operation of the buffer for one line cycle.

As shown in Fig. 4.2, the current stress on the buffer converter depends on the ripple current (i.e., maximum of i_{buf}) while the voltage stress on the buffer converter (i.e., maximum of v_{C2}) is less than 25% of the bus voltage. Such low voltage stress allows for the use of low voltage rating transistors with low device capacitance and low on-resistance. Figure 4.2 also plots the instantaneous power processed by the buffer converter, which is defined as $P_{conv} = v_{ab} i_{buf}$. While the *peak* power of the entire buffer architecture is 2 kW, the *peak* power processed by the converter is only 166 W, less than 8.4% of that of the entire buffer architecture. Since the converter is only processing a fraction of the full power, the converter

power rating (and thus physical size) can be made small. Furthermore, the overall efficiency is approximately

$$\eta \approx \eta_{main} - \underbrace{\frac{2}{\pi}(1-\eta_{buffer}) \times 8.4\%}_{\text{efficiency penalty}} , \tag{4.13}$$

which is considerably higher than a conventional active decoupling architecture, as given by (3.21).

4.3 Design constraints

Equation (4.12) reveals important design guidelines for the buffer converter. To achieve the aforementioned benefits, the choice of components values and operating parameters has to meet certain constraints for the design to be practical. For a practical full-bridge converter, the conversion ratio is constrained by

$$-1 < m < 1 \tag{4.14}$$

to avoid overmoludation. The choice of components values and operating parameters (i.e., C_1, C_2, $Q_{2,init}$) should guarantee that for all Δq_1 values within a line cycle, (4.12) has a solution for m within the range of (4.14). Therefore, the design constraint on the values of C_1, C_2 and $Q_{2,init}$ is

$$\left| \frac{-Q_{2,init} + \sqrt{Q_{2,init}^2 - 4\Delta q_1^2 \frac{C_2}{C_1}}}{2\Delta q_1} \right| < 1 \tag{4.15}$$

and

$$\delta = Q_{2,init}^2 - 4\Delta q_1^2 \frac{C_2}{C_1} \geqslant 0, \tag{4.16}$$

where δ is the discriminant of (4.12). Substituting $Q_{2,init} = C_2 V_{2,init}$ and simplifying (4.16) results in

$$\frac{1}{2} C_2 V_{C2,init}^2 \geqslant \ 2\frac{\Delta q_{1,max}^2}{C_1} \ . \tag{4.17}$$

This result indicates that for proper operation, the support capacitor C_2 needs to have a certain minimum *initial energy* stored at the beginning of each cycle. This can be ensured through appropriate sizing of C_2 and proper precharge during system startup. Furthermore,

substituting $Q_{2,init} = C_2 V_{2,init}$ and simplifying (4.15) results in

$$\frac{C_2}{C_1 + C_2} V_{C2,init} > |\Delta v_{C1,max}| = |\Delta v_{ab,max}|. \tag{4.18}$$

This result indicates that the lowest value of v_{C2} has to be larger than the maximum ripple of v_{ab} (i.e., as shown in the voltage waveforms in Fig. 4.2, the dashed blue signal has to be higher than the dash-dotted red signal any time within a cycle), which can be ensured by proper sizing of C_1 and C_2 and proper precharge of C_2. To facilitate calculation, (4.17) and (4.18) can be written as

$$\sqrt{C_1 C_2} V_{C2,init} \geqslant 2|\Delta q_{1,max}| \tag{4.19}$$

and

$$\frac{C_1 C_2}{C_1 + C_2} V_{C2,init} > |\Delta q_{1,max}|, \tag{4.20}$$

where $\Delta q_{1,max}$ is a known variable determined by the load. The parameters C_1, C_2 and $V_{2,init}$ need to be selected within these constraints in the design. In fact, it can be derived that (4.19) holds as long as (4.20) is satisfied, so in practice (4.20) is a sufficient design constraint. Based on the aforementioned constraint, the circuit parameters of the example in Fig. 4.2 are chosen as $C_1 = 100\ \mu F$, $C_2 = 430\ \mu F$, $V_{2,init} = 90\ V$. Note that although the capacitance of C_2 is larger than C_1, C_2 is rated at a much lower voltage, so its physical volume in a practical implementation will be smaller than that of C_1, as demonstrated in Section 6.1.

In general, given the full-load inverter current, the selection of capacitors C_1 and C_2 can be optimized for the smallest volume under the constraint defined in (4.20). The choice of other components such as L and C_3 is based on efficiency and ripple considerations in the same way as in typical converter designs, and is introduced in Section 6.1. Although the above analysis is for a full-bridge converter, it applies to non-inverting buck-boost converter and other circuit topologies as well, as long as (4.14) is modified accordingly. The full-bridge converter was chosen here because it enables higher capacitor utilization of C_1, as it allows for bipolar voltage swing. A benefit of using a non-inverting buck-boost converter is that it relaxes the energy storage requirement on C_2, since it does not require v_{C2} to be larger than v_{ab}. The optimal topology for the smallest overall size depends on the bus voltage and load current of the application, as well as practical implementation issues such as component selection. A detailed comparison is left for future work. The rest of this document will focus on the full-bridge topology for control implementation and experimental verification.

4.4 Optimal sizing

The sizing of the capacitors can be performed based on (4.12). For symmetry and the best use of component voltage rating, it is chosen by design that $V_{ab,init} = 0$. The other parameters, i.e., $V_{C2,init}$, C_1, C_2, can be sized for the smallest volume, thus the highest power density under certain constraints. The constraints are to guarantee the design is practical, that is, the solutions for conversion ratio m exists and $-1 < m < 1$ for the full-bridge converter considered in this design. These constraints can be derived as

$$\begin{cases} \delta = Q_{2,init}^2 - 4\Delta q_1^2 \frac{C_2}{C_1} \geqslant 0, \\ \left| \frac{-Q_{2,init}+\sqrt{\delta}}{2\Delta q_1} \right| < 1, \end{cases} \Rightarrow \begin{cases} \sqrt{C_1 C_2} V_{C2,init} \geqslant 2|\Delta q_{1,max}|, \\ \frac{C_1 C_2}{C_1+C_2} V_{C2,init} > |\Delta q_{1,max}|, \end{cases}$$
$$\Rightarrow \frac{C_1 C_2}{C_1 + C_2} V_{C2,init} > |\Delta q_{1,max}|, \tag{4.21}$$

where δ is the discriminant of (4.12). Here, (4.21) suggests that for a given $\Delta q_{1,max}$, which is determined by the peak load power, the design parameters, $V_{C2,init}$, C_1 and C_2, are free variables to adjust within the constraint.

While the sizing of the capacitors is determined by analysis at twice line frequency, the sizing of the buffer converter filter inductor needs to be determined based on the buffer converter switching frequency. There is a well-known tradeoff between efficiency and inductor volume via switching frequency. The sizing of the inductor and selection of switching frequency is complicated by at least two problems: first, within certain range, smaller inductor volume can be obtained by sacrificing efficiency, while the heatsink volume is likely to dominate the design as a result; second, an accurate calculation of the power loss is difficult and requires sophisticated models, which may be too complicated to provide design insights. For example, the optimization process in [61, 62] starts with experimentally quantifying the components characteristics, such as loss, under various conditions; the converter loss is then estimated and the volume of the heatsink is incorporated in the optimization process by assuming certain cooling system performance index (CSPI) [63]; the resulting temperature information can be applied to update the loss estimation, and the optimization continues as an iterative process. Such optimization approach can yield accurate design with close-to-optimal power density and should be carried out as the last step before hardware prototyping, when the component selection and operating range are narrowed down. However, for the case of series-stacked buffer design in this dissertation, this approach has certain limitations. The design space (primarily in terms of voltage stress) for the series-stacked buffer is wide; an attempt to cover the design space accurately might require characterizing a lot of components and

the optimization requires a considerable amount of work, while providing limited analytical insight. Instead, the purpose of this dissertation is to provide an intuitive understanding of the design tradeoff and serve as the first pass to narrow down the design space before more detailed optimization. Therefore, this dissertation adopts a series of simplifications of the design specifications and the loss model.

The task for inductor sizing is to determine its value as a function of the design variables ($V_{C2,init}$, C_1 and C_2), specifically $V_{C2,init}$ here. The voltage stress on the buffer converter is $V_{C2,init}$, as can be observed from Fig. 4.2; if we select a higher $V_{C2,init}$ in the design, transistors with higher voltage ratings must be used. As a simplification to the analysis, as $V_{C2,init}$ is adjusted, the conduction and switching loss of the power converter and inductor current ripple are kept the same (by adjusting the transistor size and switching frequency). It should be noted that the conduction and switching loss of the converter arises from multiple sources and contains multiple degree of freedom to optimize in each operating range [64–66]. A more realistic and complicated model, while more accurate, will impair the generality of the analysis. A common practice for simplification is to relate the power loss to the stress of the switches [67]. More specifically, since we observe that the inductor current (ignoring switching ripple) is the same in the series-stacked buffer architecture regardless of the choice of $V_{C2,init}$, approximately the conduction loss and switching loss of the converter is related the conductance of the switches, G, the voltage stress of the switches, V, and the switching frequency, f_{sw}, as follows [67]:

$$P_{cond} \propto G, \quad P_{sw} \propto f_{sw} G V^2. \tag{4.22}$$

While this proportional relation is insufficient for a detailed loss estimate, it is good for a first order approximation to understand the design tradeoff. To keep both the conduction loss and switching loss the same, the switching frequency should be scaled as $f_{sw} \propto \frac{1}{V^2}$. Moreover, since $\Delta I \propto V/(L f_{sw})$, to keep the current ripple the same as well as the power loss, the inductor value has to be scaled as

$$L = K_l V_{C2,init}^3, \tag{4.23}$$

where K_l is a factor determined by the load power level (2 kW in this case), the designed power loss, inductor current ripple and the characteristics of the switch used. For the first pass, power loss of 20 W (efficiency of 99% for the buffer) and ripple current of 1 A is targeted. Such high target efficiency can be achieved relatively easily due to the low voltage stress and partial power processing features of the series-stacked buffer. This efficiency target is chosen

as we intended the series-stacked buffer to be a replacement for the conventional electrolytic capacitors with comparable loss. Moreover, a high efficiency also eases the thermal design. For the switches, GaN transistors from EPC are considered as the voltage rating of available products falls well into the range of this design. Based on these conditions and data from prototypes, to the first order we estimate that $K_l = 1.2894 \times 10^{-10}$ H/V^3. Again it should be noted that this parameter estimate, together with (4.23), is not intended for a detailed optimization but rather a starting point in a first pass design. Moreover, the optimization results to be presented shows that the optimal value of design variables, $V_{C2,init}$, C_1 and C_2, are relatively insensitive to the specific value of K_l.

Now we consider the sizing of the buffer circuit. For such energy buffering applications, the passive components dominate the circuit volume. This can be verified by the hardware prototype as presented in Section 6.1, where GaN transistors take up negligible space. The volume of the heatsink is not considered in this optimization as we have fixed the power loss. The volume of the entire circuit can thus to first order be approximated by that of the passive components. Moreover, the passive component volume can be estimated by the peak amount of energy stored within a cycle divided by the energy density of the components. A survey of energy density has been conducted on certain surface mount capacitors and inductors with suitable voltage and current rating for our design example [10]. The result shows that the best types of capacitors at different voltage levels have approximately the same energy density. Therefore, to simplify the sizing procedure, according to the survey, we assume the same energy density of $\rho_C = 0.5$ J/cm^3 for capacitors regardless of its voltage level. It can also be observed from the survey that the energy density of the best types of capacitors on most voltage levels is 600 to 1000 times higher than that of the inductors. Therefore, we make the simplifying approximation that $\rho_C = 800\rho_L$, where ρ_L is the energy density of the inductors.

Under these simplifying assumptions, the total volume of the buffer circuit can be approximated as

$$V_{tot}(C_1, C_2, V_{C2,init}) = \underbrace{\frac{\frac{1}{2}C_1(V_{1,init} + \frac{|\Delta q_{1,max}|}{C_1})^2}{\rho_C}}_{\text{volume of } C_1} + \underbrace{\frac{\frac{1}{2}C_2 V_{C2,init}^2}{\rho_C}}_{\text{volume of } C_2} + \underbrace{\frac{\frac{1}{2}K_l V_{C2,init}^3 I_{buf.max}^2}{\rho_L}}_{\text{volume of } L}, \tag{4.24}$$

where $|\Delta q_{1,max}|$, $I_{buf.max}$, K_l, ρ_C, ρ_L and $V_{1,init} = V_{bus}$ are known values and C_1, C_2 and

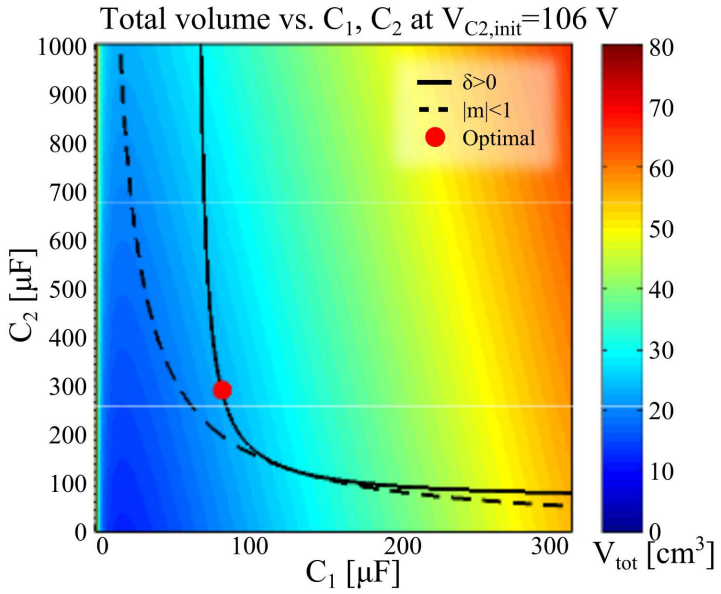


Figure 4.3: The total circuit volume of the series-stacked buffer as a function of C_1 and C_2 for $V_{C2,init} = 105\ V$. The optimal design parameters that renders the smallest overall volume is highlighted.

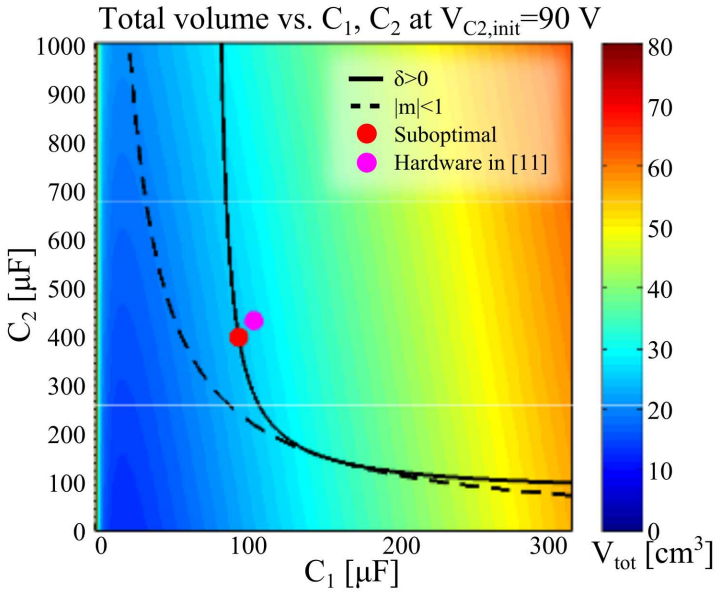


Figure 4.4: The total circuit volume of the series-stacked buffer as a function of C_1 and C_2 for $V_{C2,init} = 90\ V$. The suboptimal design parameters under this voltage stress and the design parameters used in [46] are highlighted.

$V_{C2,init}$ are the variables that can be adjusted to minimize V_{tot}, subject to the constraints in (4.21). This optimization problem can be solved with the method of Lagrange multiplier [68]. The augmented objective function is

$$\mathcal{L}(C1, C2, V_{C2,init}, \lambda) = V_{tot}(C_1, C_2, V_{C2,init}) + \lambda G(C_1, C_2, V_{C2,init}), \tag{4.25}$$

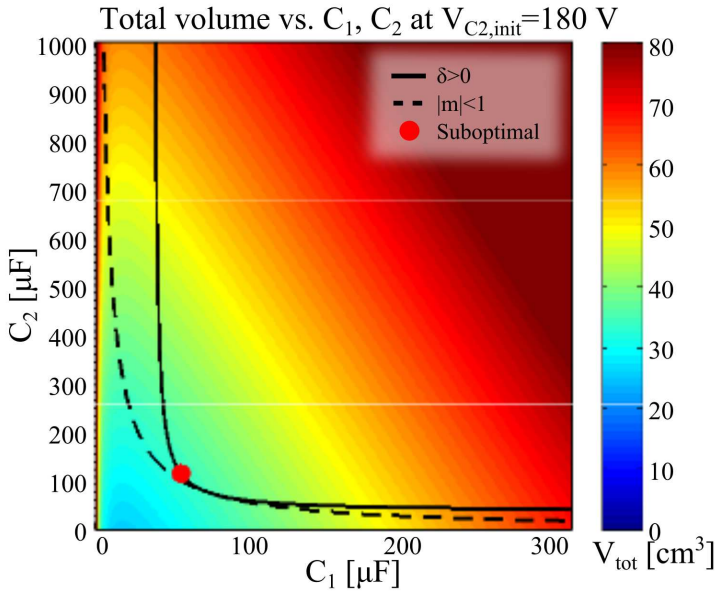


Figure 4.5: The total circuit volume of the series-stacked buffer as a function of C_1 and C_2 for $V_{C2,init} = 180\ V$. The suboptimal design parameters under this voltage stress are highlighted. The overall volume increases dramatically because of the increased inductor volume.

where we define

$$G(C_1, C_2, V_{C2,init}) = \frac{C_1 C_2}{C_1 + C_2} V_{C2,init} - |\Delta q_{1,max}|. \tag{4.26}$$

To find the minimum point, we can solve

$$\nabla \mathcal{L} = 0 \Rightarrow \begin{cases} \frac{\partial \mathcal{L}}{\partial C_1} = \frac{1}{2\rho_C}(V_{1,init}^2 - \frac{|\Delta q_{1,max}|^2}{C_1^2}) + \lambda \frac{C_2^2}{(C_1+C_2)^2} V_{C2,init} = 0, \\ \frac{\partial \mathcal{L}}{\partial C_2} = \frac{1}{2\rho_C} V_{C2,init}^2 + \lambda \frac{C_1^2}{(C_1+C_2)^2} V_{C2,init} = 0, \\ \frac{\partial \mathcal{L}}{\partial V_{C2,init}} = \frac{1}{\rho_C} C_2 V_{C2,init} + \frac{3}{2\rho_L} K_l V_{C2,init}^2 I_{buf.max}^2 + \lambda \frac{C_1 C_2}{C_1+C_2} = 0, \\ \frac{\partial \mathcal{L}}{\partial \lambda} = \frac{C_1 C_2}{C_1+C_2} V_{C2,init} - |\Delta q_{1,max}| = 0. \end{cases}$$

$$\Rightarrow \begin{cases} C_1 = 80\ \mu F, \\ C_2 = 298\ \mu F, \\ V_{C2,init} = 106\ V. \end{cases} \tag{4.27}$$

The component selection calculated in (4.27) renders the optimal circuit volume given the design requirement and all the aforementioned assumptions. This result is visualized in Fig. 4.3, where V_{tot} is plotted as a function of C_1 and C_2 with $V_{C2,init} = 105\ V$. As $V_{C2,init}$ is fixed in Fig. 4.3, the selection of the inductor is fixed. Then C_1 and C_2 can be chosen within the limit of (4.21) for the smallest total volume. Due to practical considerations such as discrete voltage breakdown values of the transistors, it is often not possible to design

Table 4.1: Estimated buffer converter volume

Architecture	Voltage Stress	Total Volume	Capacitor Volume	Inductor Volume	C_1	C_2	L
Series-stacked	90 V (built in [46])	25.4 cm^3	23.5 cm^3	1.9 cm^3	91 μF	396 μF	90 μH
Series-stacked	105 V (optimal)	25.0 cm^3	22.0 cm^3	3.0 cm^3	80 μF	299 μF	149 μH
Series-stacked	180 V	33.6 cm^3	18.5 cm^3	15.0 cm^3	54 μF	115 μF	752 μF
Full ripple port	400 V	175.3 cm^3	10.2 cm^3	165.0 cm^3	N/A	64 μF	8.3 mF

exactly at the optimum point. For example, the design in [46] takes a smaller value of $V_{C2,init}$ to use the transistors rated at 100 V, which results in a reduction in the inductor volume and a slightly larger increase in the capacitor volume, as shown in Fig. 4.4. A hardware prototype has been built successfully under the guidance of this design procedure as shown in Fig. 6.2. More details of this prototype is presented in [46]. The practical parameters used in this prototype are highlighted in Fig. 4.4. On the other hand, a higher value of $V_{C2,init}$ (i.e., higher voltage stress) can reduce the necessary volume for capacitors, but the inductor volume increases dramatically, as shown in Fig. 4.5. Table 4.1 summarize results from Figs. 4.3 to 4.5.

CHAPTER 5

CONTROL AND CAPACITOR VOLTAGE BALANCING

While (4.12) reveals the duty ratio of the proposed buffer architecture during its operation, it is not the most suitable form for real-time control implementation. Instead, we propose a current hysteresis control method to reduce the required real-time computation. Moreover, real-world factors such as loss and measurement error may greatly affect the performance of the buffer. This chapter presents the control scheme that solves these challenges and enables a practical implementation.

5.1 Buffer current control

The key to maintaining a constant bus voltage is to precisely control the buffer current i_{buf} to match the difference between the DC source current $I_{S,DC}$ and the inverter current i_{inv}, as shown in Fig. 5.1. This difference equals to the AC component of i_{inv}, since $I_{S,DC}$ and i_{inv} have the same *average* value.

The inverter current i_{inv} is therefore measured and band-pass filtered to extract its double-line-frequency component (i.e., $i_{inv,ac}$) and used as the reference for i_{buf}, as illustrated pictorially in Fig. 5.1. The bandpass filter consists a of low-pass filter in the analog sensing circuit and a digital moving average filter in the micro-controller. The low-pass filter in the analog sensing circuit is intended to filter out the switching ripple of the inverter. The moving average filter at 120 Hz is implemented in the micro-controller to obtain the DC component, and the measured signal is substracted by the DC component. This effectively forms a high-pass filter to remove the DC component. Note that i_{buf} should take the opposite value of $i_{inv,ac}$, i.e., $i_{buf} = -i_{inv,ac}$, as indicated in the figure.

Inductor current hysteresis control is employed in this application to ensure that i_{buf} closely follows the reference. The widely used constant frequency feedback control techniques such as average current-mode control [69] is not used as it is challenging to implement in this application: although current-mode control with bi-directional power transfer capabilities has been proposed [70] in others scenarios, small signal analysis of the full-bridge buffer

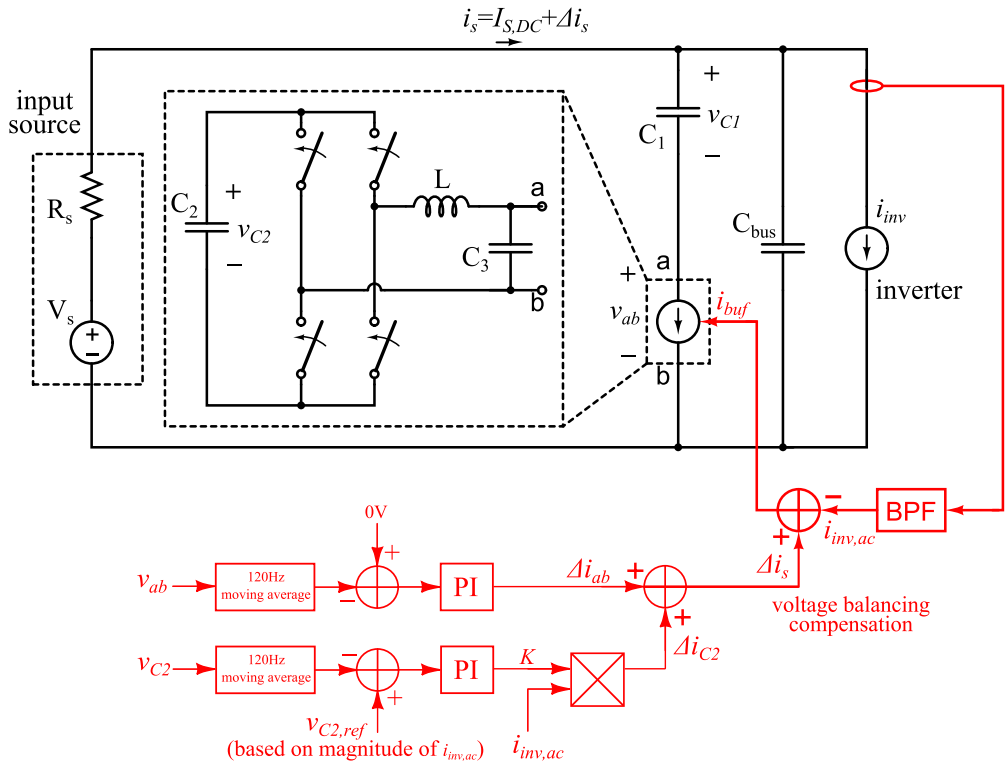


Figure 5.1: Mid-level schematic of the buffer architecture highlighting the control scheme.

converter in this architecture reveals that a low frequency right half plane zero (RHP) exist in the system. The frequency of this RHP approaches DC when i_{buf} approaches zero value (which happens every cycle given its sinusoidal nature), making the system very hard to stabilize. Given these small signal characteristics of the proposed architecture, the inductor current hysteresis control is chosen instead.

Note that the proposed current control method reacts only to the AC component but not DC component of i_s, so the buffer branch behaves like a virtually infinite capacitor to the twice-line-frequency current, while it does not affect the DC bus voltage level at all. The DC bus voltage level is set by other circuits external to the buffer (e.g., the PFC front end in a AC/DC converter), so the proposed buffer circuit can be seamlessly integrated into existing AC/DC or DC/AC converter as a DC bus capacitor replacement, without changing the existing design or control method of these systems.

5.2 Capacitor C_1 voltage balancing

Since the main capacitor C_1 is connected in series with the buffer converter, ideally i_{buf} should be a pure 120 Hz AC waveform such that the voltage across C_1 is balanced in each

cycle. In steady-state operation, the cycle average (i.e., DC component) of v_{C1} should equal the bus voltage and the average of v_{ab} should be zero. In practice, errors from multiple sources exist in the current hysteresis control, so i_{buf} might contain a small DC component. This DC offset error, if left unchecked, will keep charging or discharging C_1 over multiple cycles and cause the average values of v_{C1} and v_{ab} to drift. As mentioned in Section 4.3, the amplitude of v_{ab} has to remain smaller than that of v_{C2} for the correction operation of the full-bridge buffer converter. Therefore, this drift, if left uncompensated, will accumulate and eventually disrupt the operation of the buffer converter. In our proposed control scheme, v_{ab} is measured and averaged every 120 Hz cycles. As shown in Fig. 5.1, the error between the average of v_{ab} and its reference value (i.e., 0 V) is passed through a PI controller to generate a DC correction term Δi_{ab}. This term is added to the reference of i_{buf} to correct this DC offset, such that the buffer current is pure AC.

5.3 Capacitor C_2 voltage balancing

In the proposed architecture, C_2 is charged through the buffer converter and since the buffer current i_{buf} is pure AC, ideally the voltage across C_2 should be balanced every cycle such that its average value remains constant. In practice, however, the buffer converter incurs certain power loss while charging and discharging C_2 in a cycle. If uncompensated, such loss will gradually decrease the average voltage of C_2 over multiple cycles to the point that v_{C2} is lower than v_{ab} and the normal operation of the full-bridge converter is disrupted. Care has to be taken in any effort to directly extract additional current from the DC bus to charge C_2, since it will create a DC offset in i_{inv} and cause C_1 imbalance. This would conflict with the control loop that balances C_1. Adding a dedicated auxiliary circuit to draw power from the DC bus to charge C_2 and compensate for this loss is also undesirable since it contradicts the goal of small converter volume and low component voltage stress. In this work, we develop a compensation scheme that makes use of the existing small bus voltage ripple to provide extra energy to C_2 without affecting C_1. The derivation of this compensation scheme follows.

Consider the buffer current reference i_{buf} in Fig. 5.1 where a compensation term $\Delta i_{C2}(t)$ is added such that

$$i_{buf} = -i_{inv,ac} + \Delta i_{C2} \ , \tag{5.1}$$

where $i_{inv,ac}$ is the AC component of i_{inv} as discussed in Section 5.1. At the same time, in

periodic steady state, the DC component of i_{inv} should equal the DC source current i_s, i.e.,

$$< i_{inv} > = I_{S,DC} \ . \tag{5.2}$$

By KCL at the output node,

$$i_s = i_{buf} + i_{inv} \ . \tag{5.3}$$

Substituting (5.1) and (5.2) into (5.3) renders

$$i_s = (-i_{inv,ac} + \Delta i_{C2}) + (< i_{inv} > + i_{inv,ac}) = I_{S,DC} + \Delta i_{C2} \ . \tag{5.4}$$

As i_{buf} flows through C_1, the instantaneous voltage on C_1 is

$$v_{C1}(t) = V_{C1,DC} + \frac{\int_0^t i_{buf} d\tau}{C_1} \ . \tag{5.5}$$

Moreover, in steady state,

$$V_{C1,DC} = V_s - R_s \times I_{S,DC}. \tag{5.6}$$

Ignoring the effect of the small filter capacitor C_{bus}, it can be shown that

$$v_{C1} + v_{ab} = v_{bus} = V_s - R_s \times i_s \ . \tag{5.7}$$

Substituting (5.4), (5.5) and (5.6) into (5.7), the voltage across terminal a and b of Fig. 5.1 is given as

$$\begin{aligned} v_{ab} &= V_s - R_s \times (I_{S,DC} + \Delta i_{C2}) - v_{C1} \\ &= -\Delta i_{C2} R_s - \frac{\int_0^t i_{buf} d\tau}{C_1} \ . \end{aligned} \tag{5.8}$$

Furthermore, based on (5.5), maintaining the average voltage on C_1 every twice line frequency cycle requires

$$v_{C1}(\frac{1}{120}) = v_{C1}(0) = V_{C1,DC} \quad \Rightarrow \quad \int_0^{\frac{1}{120}} i_{buf} d\tau = 0. \tag{5.9}$$

Since $i_{inv,ac}$ is pure AC at 120 Hz,

$$\int_0^{\frac{1}{120}} i_{inv,ac} d\tau = 0. \tag{5.10}$$

Combining (5.1), (5.9) and (5.10) yields the constraint on the compensation term Δi_{C2}, i.e.,

$$\int_0^{\frac{1}{120}} \Delta i_{C2} d\tau = 0. \tag{5.11}$$

This constraint suggests that a good compensation term for C_2 voltage balancing would be a pure AC signal at 120 Hz.

The net energy flowing into the buffer converter within *one cycle* is

$$E_{conv} = \int_0^{\frac{1}{120}} v_{ab} i_{buf} dt. \tag{5.12}$$

Substituting (5.8) and (5.1) into (5.12) results in

$$\begin{aligned} E_{conv} &= -\int_0^{\frac{1}{120}} \Delta i_{C2} R_s i_{buf} dt - \frac{1}{C_1} \int_0^{\frac{1}{120}} \left(\int_0^t i_{buf} d\tau \right) i_{buf} dt \\ &= -\int_0^{\frac{1}{120}} \Delta i_{C2} R_s (-i_{inv,ac} + \Delta i_{C2}) dt \\ &\quad - \frac{1}{C_1} \int_0^{\frac{1}{120}} \left(\int_0^t (-i_{inv,ac} + \Delta i_{C2}) d\tau \right) (-i_{inv,ac} + \Delta i_{C2}) dt. \end{aligned} \tag{5.13}$$

Furthermore, we can make the observation that if Δi_{C2} takes the form

$$\Delta i_{C2} = -K i_{inv,ac}, \tag{5.14}$$

where K is a multiplying factor, (5.14) certainly satisfies the constraint outlined in (5.11) since $i_{inv,ac}$ is a pure AC waveform at 120 Hz. Moreover, with Δi_{C2} given by (5.14), the buffer converter net energy given by (5.13) can be simplified as follows,

$$\begin{aligned} E_{conv} &= -\int_0^{\frac{1}{120}} -K i_{inv,ac} R_s (-1-K) i_{inv,ac} dt \\ &\quad - \frac{1}{C_1} \int_0^{\frac{1}{120}} \left(\int_0^t (-1-K) i_{inv,ac} d\tau \right) (-1-K) i_{inv,ac} dt \\ &= -K(K+1) R_s \int_0^{\frac{1}{120}} i_{inv,ac}^2 dt - \frac{(1+K)^2}{C_1} \int_0^{\frac{1}{120}} \left(\int_0^t i_{inv,ac} d\tau \right) i_{inv,ac} dt. \end{aligned} \tag{5.15}$$

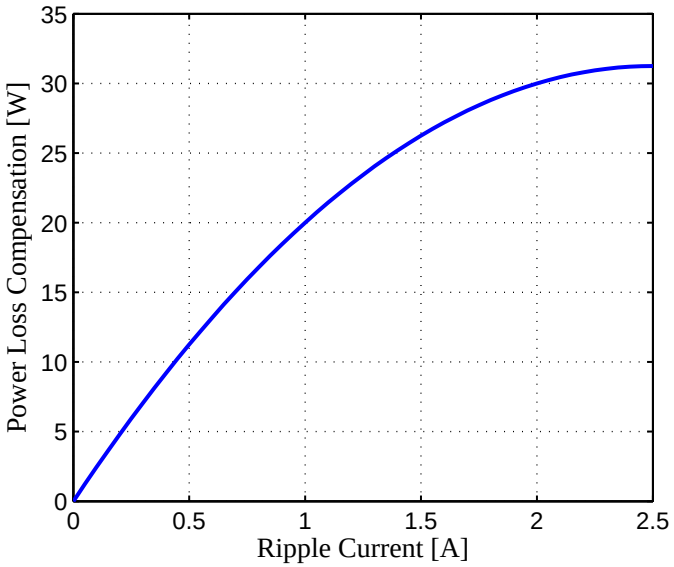


Figure 5.2: The power provided by the proposed C_2 compensation scheme as a function of the input current ripple amplitude under full-load condition.

Note that since $i_{inv,ac}$ is a pure sine wave, $\int_0^t i_{inv,ac} d\tau$ will be exactly out of phase with $i_{inv,ac}$. Thus, the integral of their product over a full cycle is zero. Therefore, the second term in (5.15) equals zero and

$$E_{conv} = -K(1+K)R_s \int_0^{\frac{1}{120}} i_{inv,ac}^2 dt. \tag{5.16}$$

As long as $-1 < K < 0$, the net energy will be larger than zero to provide loss compensation to the buffer converter. At the same time, this compensation will not affect the average voltage on C_1 since it satisfies (5.11). The average power loss compensation this scheme can provide is given by

$$P_{comp} = E_{conv} f, \tag{5.17}$$

where f is the twice line frequency. Note that in principle, this compensation scheme is effective not only with pure 120 Hz waveform but also when higher-order harmonics are present, such as in certain power factor correction (PFC) applications.

To implement this compensation, the average value of v_{C2} is measured every cycle. A PI controller is employed to adjust K between -0.5 and 0 based on the error between the measured average and desired reference value of v_{c2} to maintain the average voltage level of C_2, as shown in Fig. 5.1. Essentially, this compensation scheme intentionally adjusts i_{buf}

to slightly mismatch $i_{inv,ac}$ to create a small DC bus ripple represented by $\Delta i_{C2} R_s$. As will be shown in the experiment, in steady-state operation, the bus voltage ripple is typically less than 2% of the nominal bus voltage in the entire load range, while providing enough compensation to maintain C_2 voltage. During startup, as the DC bus voltage is increasing, the C_2 voltage balancing loop naturally charges C_2 to the desired voltage level.

Figure 5.2 plots the power loss compensated by this scheme as a function of the input current ripple amplitude during full-load (2 kW) operation of the buffer. The maximum amount of energy compensation that this scheme is able to provide in each cycle can be calculated from (5.16) with $K = -0.5$. Under full-load condition, this compensation scheme can compensate for an average power loss of up to 31 W. Given that the buffer converter is only processing an average power of about 100 W as discussed in Section 4.2, the proposed compensation scheme is practically feasible, even for very low efficiency converters. As the load current decreases, the compensation capability decreases as well, but the power that needs to be processed by the buffer converter also decreases, so the power loss is also reduced. A light load control scheme will be introduced in Section 5.5 to further reduce the power loss at light load condition. The proposed compensation scheme thus scales well with different load power levels.

It is important to note that besides loss compensation, this C_2 voltage balancing feedback loop also improves current matching of i_{buf} to $i_{inv,ac}$. While the C_1 voltage balancing feedback loop eliminates the offset error (DC component) as discussed in Section 5.2, the C_2 voltage balancing feedback loop corrects the gain error (AC component magnitude mismatch). To see this, suppose the magnitude of i_{buf} is considerably smaller than that of $i_{inv,ac}$ because of a gain error. This mismatch will cause a undesirable ripple on the DC bus voltage. Conceptually, this mismatch has the same effect as if there is no gain error, but the multiplying factor K is too close to -0.5. As a result, according to (5.16), C_2 will have more energy compensated than the loss, so v_{C2} will increase. The C_2 voltage balancing feedback loop will then adjust K and thus Δi_{C2} to balance v_{C2}. This effectively corrects the mismatch between i_{buf} and $i_{inv,ac}$ with Δi_{C2}, except for the small amount of mismatch intentionally introduced for C_2 compensation. In other words, the C_2 voltage balancing loop will minimize the gain error of current matching and thus the DC bus voltage ripple, while maintaining sufficient compensation to C_2 to keep its average voltage at the desired level.

Table 5.1: Buffer design example

application requirements	nominal power	2 kW
	nominal input current	5 A
	DC source voltage	450 V
	DC source resistance	10 Ω
circuit parameters	main capacitor C_1	100 μF
	support capacitor C_2	430 μF
	filter inductor L_f	94 μH
	filter capacitor C_3	1 μF
	DC bus capacitor C_{bus}	5 μF
	current hysteresis band	$I_{ref} \pm 1$A

5.4 Simulation

A simulation in PLECS is performed to verify this design. The values of the circuit parameters are listed in Table 5.1. In this table, the design requirements are specified according to the Google little box design example [8] and the circuit parameters are chosen following the design procedure presented in Section 4.3.

5.4.1 Steady-State Simulation

The steady-state operation of the series-stack buffer architecture under full load condition (2 kW) is simulated and a zoomed-in plot of one line cycle is shown in Fig. 5.3. Practical factor such as loss in the buffer converter, bandwidth limitation on the sensor, quantization in the controller, etc. are all considered and reflected in the simulation, and the proposed control scheme are fully implement to maintain the voltage balance.

5.4.2 Transient Simulation

The two voltage balancing control loops maintain the voltages on the capacitors during steady-state operation and also make them settle quickly to a new steady state in case of a load transient. To demonstrate the effect of these voltage balancing control loops, a simulation example is illustrated in Fig. 5.4. The simulation condition is the same as in Table 5.1 expect that the load power experiences a step change. As shown in Fig. 5.4, no compensation loop is activated initially, so the average voltage of C_2 keeps decreasing owing to the converter loss. Once the compensation loops are activated (at $t = 30$ ms), the average value of v_{C2} is regulated. Since this compensation scheme takes advantage of the existing ripple, it does not add much extra ripple to the DC bus in steady state, as illustrated by

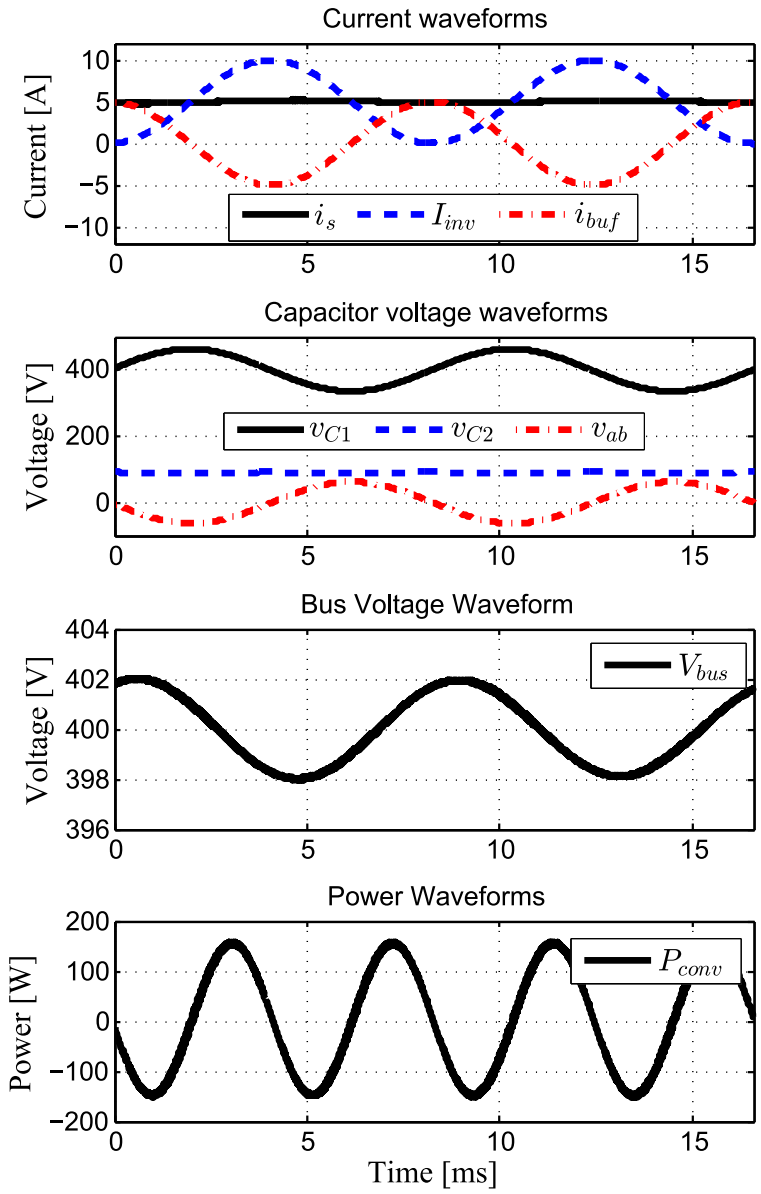


Figure 5.3: Simulation waveforms in PLECS illustrating steady-state operation of the series-stacked buffer architecture. Note that i_{C2} in the simulation contains current ripple due to the converter switching, while the i_{C2} waveform shown in this figure is a low-pass filtered version for better clarity of illustration.

the bus voltage waveform of Fig. 5.4. In the event of a load change, the C_1 compensation loop quickly adjusts the average value of v_{C1} such that the bus voltage settles to the new steady state within just a few cycles. The average value of v_{C2} is maintained throughout this process.

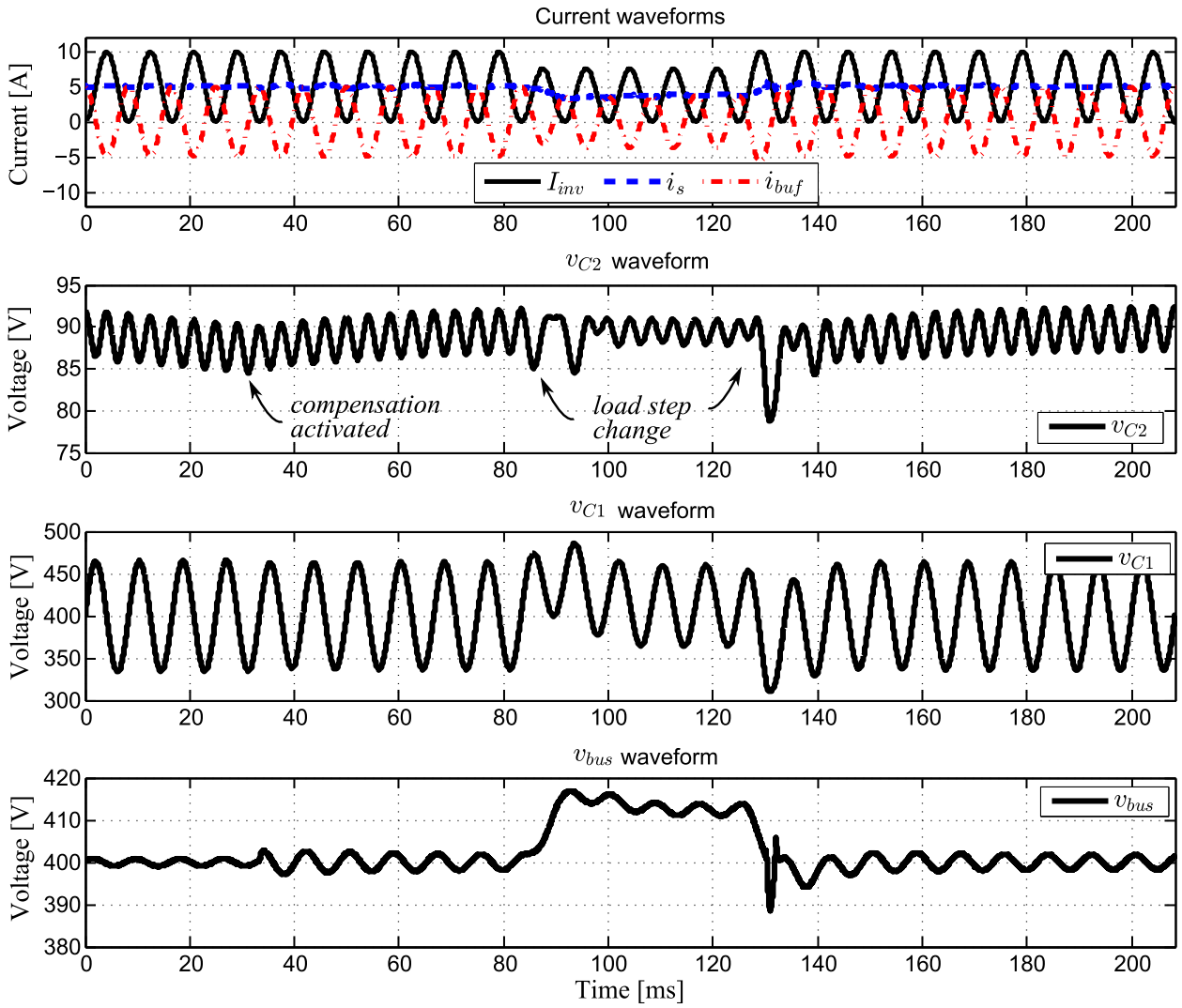


Figure 5.4: Simulation waveforms in PLECS illustrating the effects of the voltage balancing compensation loops during transients. Initially, no compensation loop is activated. At $t = 30$ ms, both compensation loops are activated. At $t = 83.3$ ms, the load current takes a step change from 5 A to 3.75 A. At $t = 125$ ms, the load current takes a step change from 3.75 A to 5 A.

5.5 Considerations for light load and reactive load conditions

As shown by (5.4), the compensation term Δi_{C2} adds a ripple to the DC input current. Some applications require the ripple current to be smaller than a certain percentage of the DC value (e.g., 20% in [8]), which imposes a limit on the value of K. At the same time, the amount of buffer converter power loss that can be compensated is quadratically proportional to the AC component of the inverter current $i_{inv,ac}$, as calculated in (5.16). Note that the buffer converter current ideally equals to $i_{inv,ac}$. Therefore, to adequately compensate the

buffer converter power loss while still staying within DC side ripple specifications, the buffer converter power loss needs to scale quadratically with $i_{inv,ac}$ as well. In other words, the buffer converter power loss needs to scale quadratically with the buffer converter current.

The power loss calculation of synchronous buck/full-bridge type converters has been thoroughly studied in the literature [64–66] and this dissertation will not repeat the details. At a high level, the conduction related losses (MOSFET on-resistance, capacitor ESR, winding and sensing resistance) scale quadratically with the converter current which aligns well with the loss compensation capability as discussed above. The switching related losses scale quadratically with the voltage (capacitive turn-on), or linearly with the product of both (MOSFET overlap), or other factors (core loss, gate drive loss). To align scaling of these switching losses with the converter current as well, we also need to scale the converter voltage with converter current. We observe that the highest voltage applied on the buffer converter switches is v_{C2}; at the same time, as the load current decreases, the magnitude of v_{ab} decreases proportionally as well. Therefore, as long as v_{C2} stays above the peak value v_{ab}, it can be adjusted according to the magnitude of $i_{inv,ac}$ to minimize loss. To this end, the reference value for v_{C2} in the aforementioned PI control loop is set to be proportional to the magnitude of $i_{inv,ac}$, such that the switching losses (except for the gate drive loss and core loss) now scale quadratically with the load current. Lastly, the width of the hysteresis band for the current hysteresis control is adjusted according to the load current magnitude as well. This adjustment changes both the inductor current switching ripple and the converter switching frequency to dynamically balance the conduction losses and the switching losses, such that the remaining core loss and gate drive loss is alleviated at light load and the overall power loss is at a minimum. Since it is not easy to precisely calculate all the power losses, the equations for scaling the reference of v_{C2} and the hysteresis band are determined through empirical fine-tuning after first-order loss calculations.

The proposed buffer architecture and control scheme work naturally with reactive loads without any modification. It only requires some care to be taken in the hardware implementation: since i_{inv} will have negative instantaneous value with reactive load, the current measurement hardware needs to be capable of bidirectional current measurement.

CHAPTER 6

SERIES-STACKED BUFFER HARDWARE PROTOTYPE AND EXPERIMENTAL RESULTS

6.1 Hardware prototype

A hardware prototype has been built to demonstrate the proposed buffer architecture. Table 6.1 lists the main components used and Fig. 6.1 provides a simplified schematic of the prototype.

The main capacitor C_1 is implemented with two hundred thirty-nine 2.2 μF, 450 V ceramic capacitors. This capacitance, at first glance, seems to be much larger than the 100 μF calculated for C_1 in Section 4.2. This is because the voltage de-rating of multi-layer ceramic capacitor (MLCC) has to be considered. For the selected capacitor, 2.2 μF is the capacitance at zero voltage bias, while the effective capacitance at 400 V is only approximately 0.43 μF [10]. Therefore, 239 capacitors yield a total capacitance of 103 μF at 400 V. Similarly, one hundred twenty-six 15 μF, 100 V ceramic capacitors are used for C_2, yielding a total capacitance of 433 μF at 80 V considering de-rating. Capacitors C_3 and C_{bus} are only for switching frequency filtering purposes and are implemented with only a small number of capacitors.

Each current signal used for control is measured with a current sensing resistor and a LT1999 amplifier. Each voltage signal is measured with a resistor voltage divider and a LT1990 difference amplifier. A TMX320F28377D micro-controller is used to process these signals, execute the proposed control scheme and generate the PWM signal for the power stage. Signals of v_{C2}, v_{ab} and i_{inv} are sampled by the on-chip analog-to-digital converter (ADC) and i_L is connected to the built-in analog comparator of the micro-controller. The PWM module of the selected micro-controller can directly achieve SR latch logic necessary for the inductor current hysteresis control while still allowing for insertion of PWM dead-time, therefore providing an ideal one-chip solution for the proposed control scheme. A flyback DC-DC converter is also implemented as an auxiliary supply to draw control power from the DC bus.

The power stage is implemented with EPC2016C GaN switches on a custom-made half-

Table 6.1: Component listing for the active energy buffer

Component	Mfr. & Part number	Parameters	Notes
GaN FETs	EPC EPC2016C	100 V, 16 mΩ	
Capacitors (C_{bus})	TDK C5750X6S2W225K250KA × 10	450 V, 2.2 μF	0.431μF @400V
Capacitors (C_1)	TDK C5750X6S2W225K250KA × 239	450 V, 2.2 μF	0.431μF @400V
Capacitors (C_2)	TDK CGA9P3X7S2A156M250KB × 126	100 V, 15 μF	3.44μF @80V
Capacitors (C_3)	TDK C3225X5R2A225M230AB × 2	100 V, 2.2 μF	
Inductors (L_1, L_2)	Vishay IHLP6767GZER470M11	8.6 A, 47 μH	
Power isolators	Analog Devices ADuM5210		
Logic level shifters	Texas Instruments SN74LV4T125PWR		
Micro-controller	Texas Instruments TMX320F28377D		
Current Sensing Amp	Linear Technology LT1999		
Voltage Sensing Amp	Linear Technology LT1990		

Table 6.2: Hardware prototype volume breakdown

Total rectangular box volume	80.0 cm^3 (4.88 inch^3)
Total energy storage component volume	32.9 cm^3 (2.01 inch^3)
C_{bus} volume	0.7 cm^3 (0.043 inch^3)
C_1 volume	19.1 cm^3 (1.16 inch^3)
C_2 volume	9.0 cm^3 (0.55 inch^3)
Inductor volume	4.1 cm^3 (0.25 inch^3)
Power density by box volume	25 W/cm^3 (410 W/inch^3)
Power density by component volume	60.8 W/cm^3 (995 W/inch^3)

bridge module PCB. The low transistor voltage stress allowed by this architecture enables the use of this 100 V GaN FET, switching at hundreds of kHz for small inductor size. In this implementation, the switching frequency varies between 100 kHz to 350 kHz due to the current hysteresis control.

Annotated photographs of the hardware prototype are shown in Fig. 6.2. Most of the ICs including the GaN modules and the micro-controller are placed on the front side of the board while the energy storage components (i.e., C_1, C_2, L_1 and L_2) are placed on the backside. Table 6.2 lists the volume breakdown of the prototype. It should be noted that the current hardware prototype is designed to fit with a single-phase inverter together into one enclosure for the best overall power density, as shown in Fig. 6.3. More details about the inverter and the entire system is presented in [9,71]. As highlighted in Table 6.2, the enclosed box volume is still considerably larger than the total component volume. Further size reduction is thus expected through layout optimization if the buffer is considered as a standalone unit.

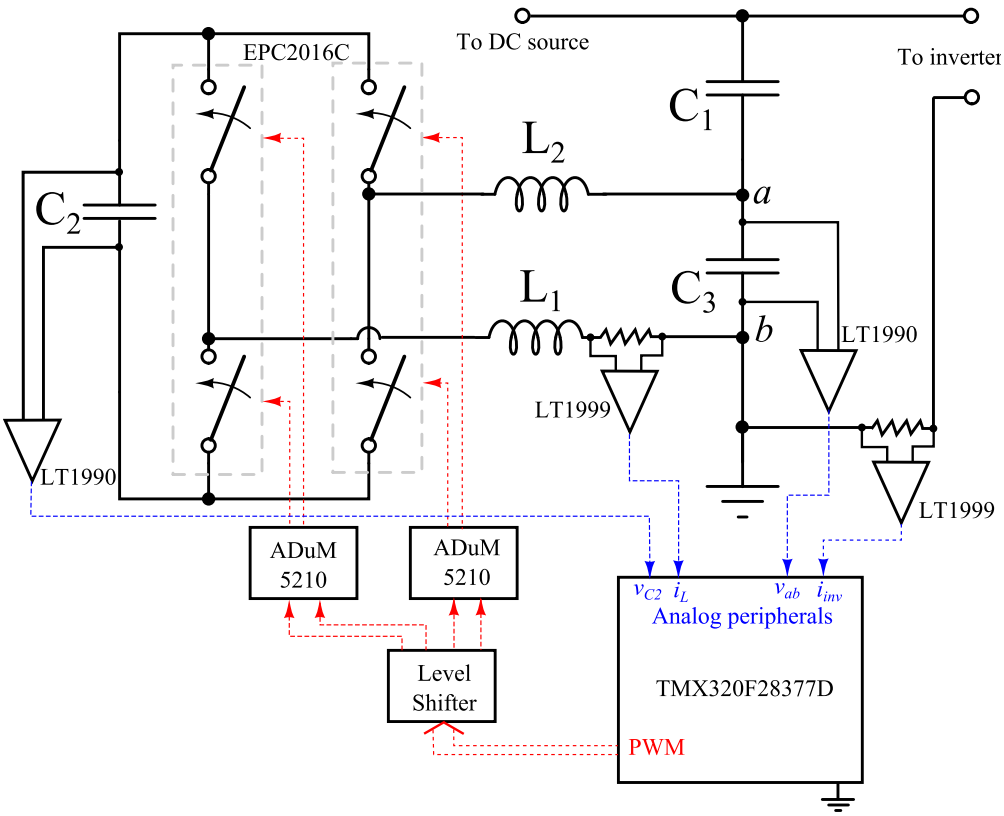


Figure 6.1: Schematic of the hardware prototype. Control outputs (PWMs) are highlighted in red and control inputs (measurements) are highlighted in blue. The gate driver for GaN transistors and the resistor voltage dividers for v_{C2} and v_{ab} measurement are omitted for simplicity.

6.2 Digital control implementation

The control of the active buffer is implemented in the TMX320F28377D micro-controller. The logic flow of the series-stacked buffer together with a multilevel inverter (as they share the same controller in a complete inverter system) is illustrated in Fig. 6.4. The program is based on a fixed frequency interrupt at 120 kHz to performance sampling and calculation, and adjusts the duty ratio accordingly. All the control discussed in Chapter 5 has been implemented.

6.3 Experimental setup

Experiments are performed on the hardware prototype to verify the performance of the proposed buffer architecture. The experiment is configured as in Fig. 6.5, according to the specifications in [8], where a power supply (Magna-Power XR1000) is connect to the DC side

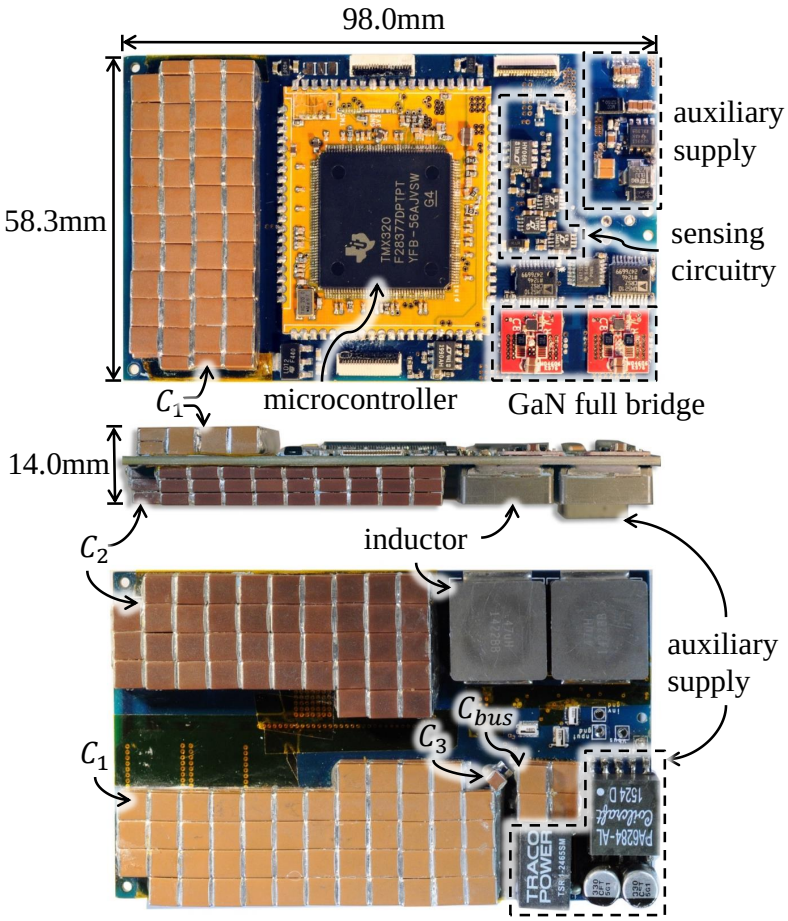


Figure 6.2: Hardware prototype.

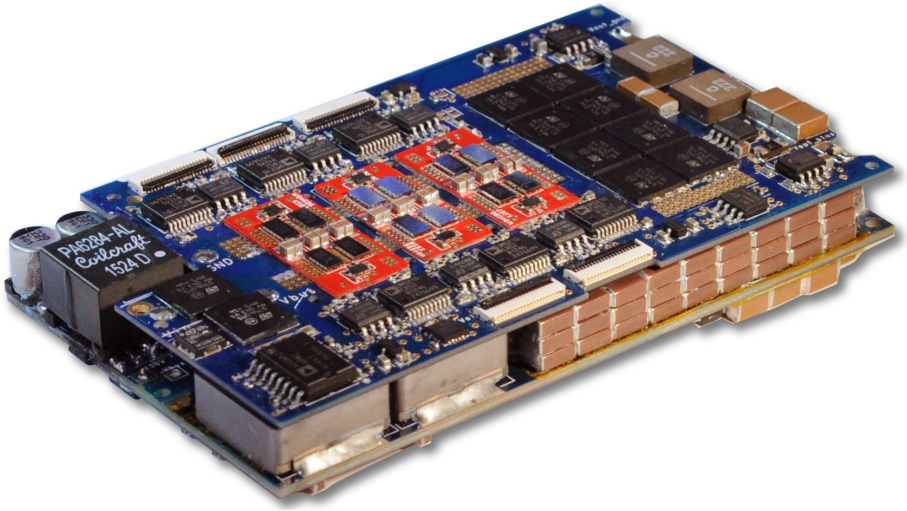


Figure 6.3: Hardware prototype of the complete inverter system fitting together.

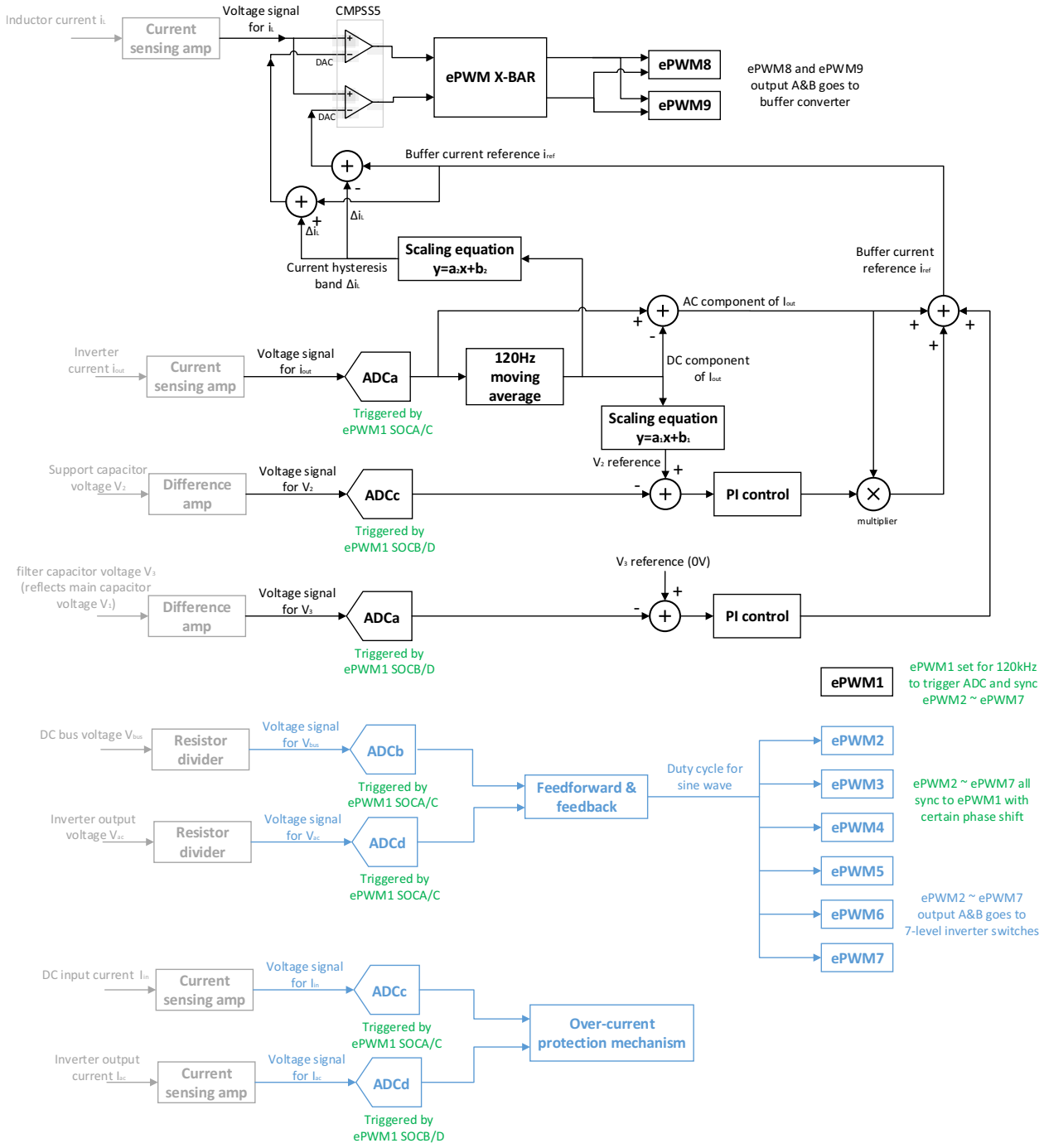


Figure 6.4: The control flow implemented in the F28377D micro-controller.

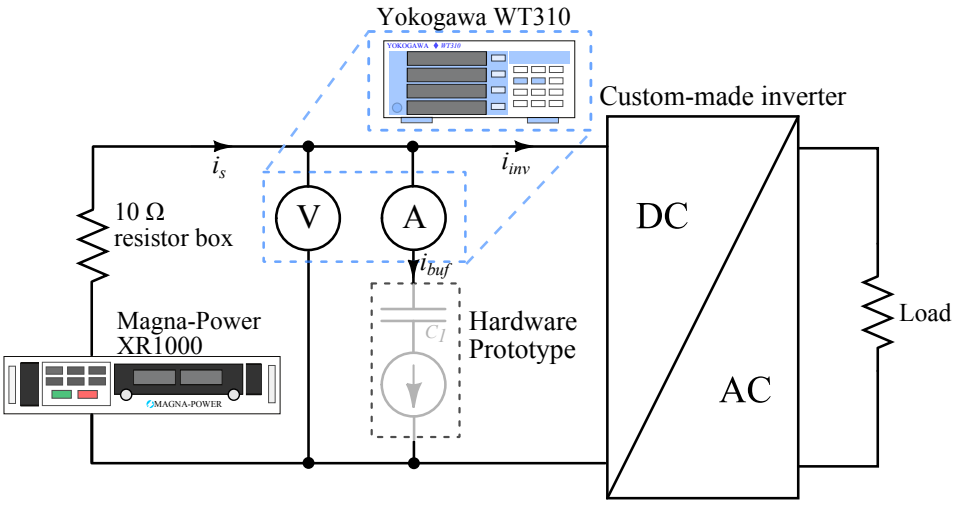


Figure 6.5: Experimental setup.

of the buffer through a 10 Ω resistor and a custom-made 2 kW inverter as shown in Fig. 6.3 is connected to the AC side of the buffer.

6.4 Experimental results

6.4.1 Steady-state operation in full-load condition

Figures 6.6 and 6.7 illustrate the operation of the buffer architecture in the experiments. The DC source voltage is set to 450 V. The inverter load is drawing a 10 A peak-to-peak *shifted* sinusoidal current i_{inv} and the control of the buffer converter enforces a buffer current i_{buf} equal to the AC component of i_{inv}, as shown in Fig. 6.7. Note that Fig. 6.7 shows the waveform of $-i_{buf}$ instead of i_{buf}, to allow for easier illustration that i_{buf} resembles the shape of the AC component of i_{inv}. Also note that the buffer capacitors also function as the input capacitor of the inverter, so the current ripple due to inverter switching (at 120 kHz for the inverter used here) is present in i_{inv} and i_{buf}. A low-pass filter is applied to the measured i_{inv} in the control implement such that the control will only respond to the double-line-frequency ripple but not to the switching ripple. Because of the buffer operation, the input current i_s is an almost constant 5 A with a small ripple.

As observed from the experimental measurement in Fig. 6.6, the main buffer capacitor C_1 has a large voltage swing of 120 V, indicating high energy utilization of this capacitor. Due to the buffer control, the voltage across terminal a and b varies complimentary to this voltage swing such the sum of these two, i.e., the bus voltage, remain nearly a constant

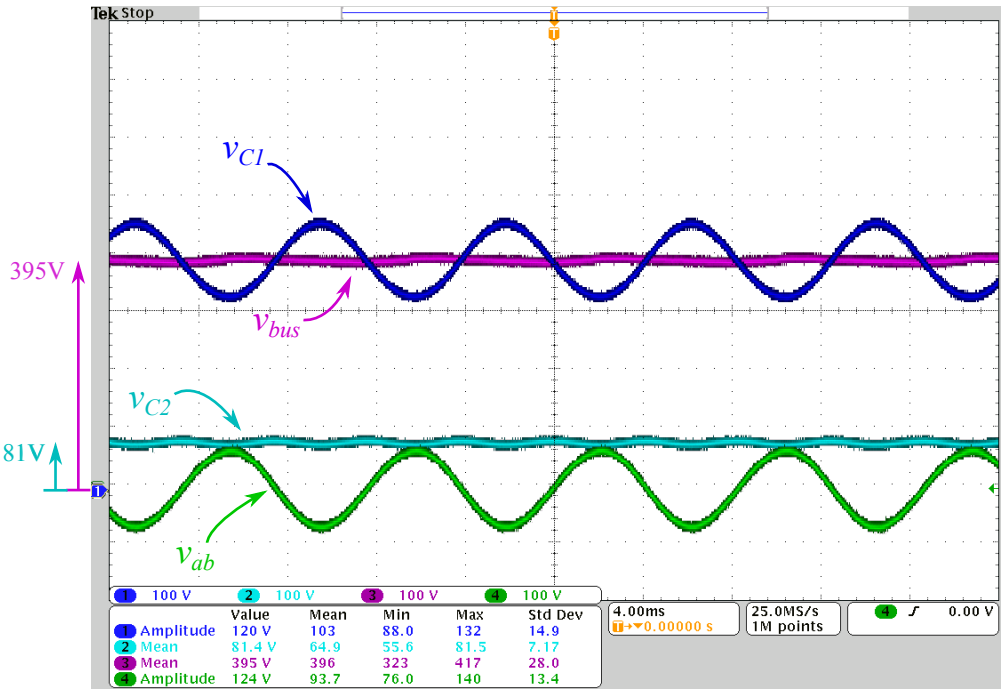


Figure 6.6: Experimental waveforms of the C_1 voltage v_{C1}, C_2 voltage v_{C2}, bus voltage v_{bus} and terminal ab voltage v_{ab} during the full-load operation of the buffer.

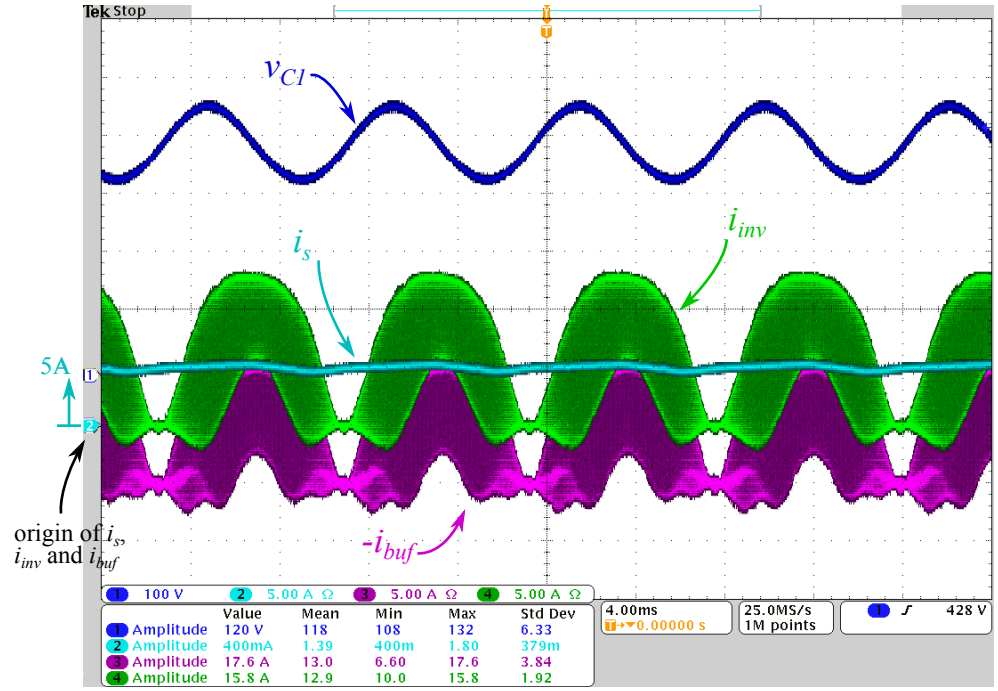


Figure 6.7: Experimental waveforms of the C_1 voltage v_{C1}, input current i_s, inverter current i_{inv} and buffer current in its reverse direction $-i_{buf}$ during the full-load operation of the buffer.

with only very small ripple below 5 V as shown in Fig. 6.6. The v_{ab} waveform is symmetric with respect to zero, indicating that the C_3 PI compensation loop described in Fig. 5.2) is functioning properly to remove the DC offset in the buffer current. Moreover, the voltage of C_2 is held at 80 V with small ripple, indicating that the v_{C2} PI compensation loop is indeed extracting extra power from the bus voltage ripple to compensate for the buffer converter power loss and maintain the power balance of C_2.

As a benchmark reference, in order to achieve the same 5 V bus voltage ripple with conventional passive decoupling, C_1 would have to be as large as 2654 μF, which can be calculated according to (2.5). Note that in the experiment, the DC source is 450 V with a 10 Ohm resistor. During full-load operation the bus voltage is 400 V, but with very light load, the bus voltage rises to close to 450 V. If DC link capacitors are used, the capacitors have to be rated at 450 V, which is approximately the same voltage rating for C_1 in the series-stacked buffer prototype. If electrolytic capacitors were used (we consider Nichicon UCP2W121MHD6 as an example) for this 2654 μF capacitance, at least 95 cm^3 is required for the capacitance. In practice, designers should consider the RMS current rating, the temperature rise limit and component lifetime, which typically results in even larger volume when electrolytic capacitors are used. If the same type of long-lifetime, low-loss ceramic capacitors were used, this capacitance would result in a volume of 506 cm^3, much larger than the volume listed in Table 6.2.

6.4.2 Light-Load Operation and Input Current Ripple

As discussed in Section 5.5, the ripple in the input current needs to meet strict requirements, so special light-load considerations are taken in the control to ensure that input current ripple scales with power level. This part of the experimental is to verify this light-load functionality in the control.

The operation of the buffer under full-load (2 kW) conditions is illustrated in Fig. 6.8. The inverter load is drawing a 10 A peak-to-peak *shifted* sinusoidal current. The buffer converter, controlled by the aforementioned scheme, draws certain current to cancel out the AC component of the load current. A voltage swing of 130 V is measured across C_3 (i.e., v_{ab}), suggesting that C_1 has approximately the same amount of ripple and its energy potential is being adequately exploited. Despite the large ripples on C_1 and C_3, they cancel each other out and the DC bus voltage is nearly constant at 400 V with only a very small ripple of less than 5 V (1.25%), which is utilized for C_2 compensation. The voltage of C_2 is held at approximately 81 V, indicating that the v_{C2} PI compensation loop is indeed extracting extra

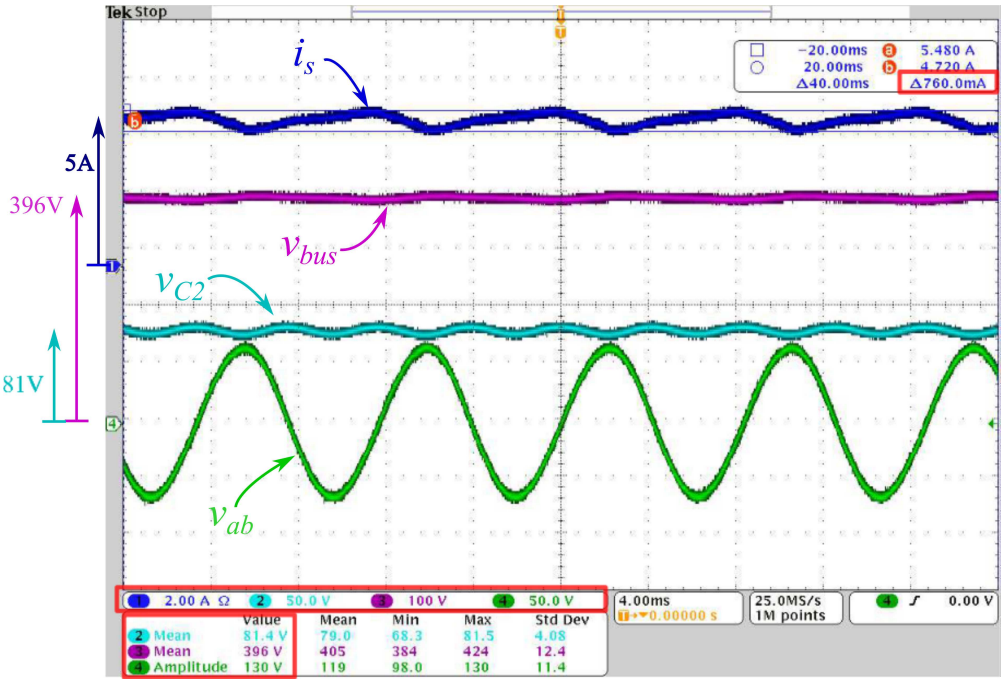


Figure 6.8: Experimental waveforms of the input current i_{in} (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage v_{bus} (channel 3) and C_3 voltage v_{C3} (channel 4) in the full-load (2 kW) condition. The input current ripple is 760 mA as highlighted on the top-right corner.

power from the bus voltage ripple to compensate the converter power loss and maintain the power balance of C_2. At the same time, the C_3 voltage waveform is symmetrical with respect to zero, indicating that the v_{C1}, v_{C3} PI compensation loop is functioning properly to remove the DC offset in the buffer current. As a result, the input current is approximately constant at 5 A with a ripple as small as 760 mA (15%).

The operation of the buffer in the half-load (1 kW) condition is illustrated in Fig. 6.9 and in the quarter-load (0.5 kW) condition is illustrated in Fig. 6.10 (note the y-axis scales are different in Figs. 6.8, 6.9 and 6.10). As marked in Figs. 6.8, 6.9 and 6.10, while the load power level decreases, the average input current decreases. The reference of v_{C2} is also reduced accordingly to reduce the buffer converter power loss such that smaller ripple is needed for loss compensation, as discussed in Section 5.5. As shown in Fig. 6.9 and Fig. 6.10, the input current ripple indeed scales down with the average input current value. Figure 6.11 plots the input current ripple as a function of the average input current. Because of the light-load control scheme, the ripple stays well below 20% except for very light-load conditions. In very light-load conditions, as the input ripple current becomes very small, the effect of the DC bus filter capacitor C_{bus} absorbing part of the ripple current can no longer be neglected, which impairs the loss compensation capability specified in (5.16). Therefore, the current

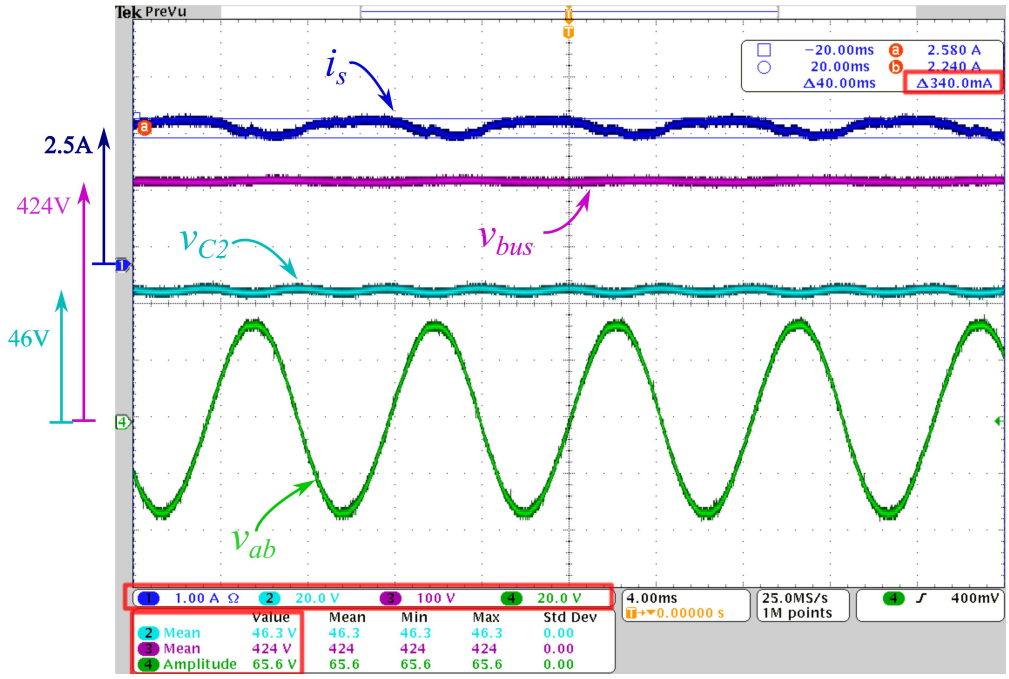


Figure 6.9: Experimental waveforms of the input current i_{in} (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage v_{bus} (channel 3) and C_3 voltage v_{C3} (channel 4) in the 50% load (1 kW) condition. The input current ripple is 340 mA as highlighted on the top-right corner.

ripple saturates at about 200 mA in very light-load conditions.

6.4.3 Transient response

Figure 6.12 demonstrates the buffer architecture responding to a load step change from 25% to 50%. The bus voltage settles to the new steady state within a few cycles and the voltages of C_2 and C_3 return to the reference value after a short transient, suggesting the effectiveness of the proposed control scheme. The input current ripple increases during this transient to provide extra energy to charge up C_2. Similarly, the transient of a load step change from 100% to 75% is shown in Fig. 6.13.

6.4.4 Reactive load operation

Figure 6.14 demonstrates the buffer architecture operating with a reactive load. The output of the inverter is connected to a 2 kVA load with 0.72 leading power factor. Compared to the 2 kW pure resistive load operation in Fig. 6.8, the average input current is lower and the bus voltage is higher in this reactive load condition due to smaller real power, but the

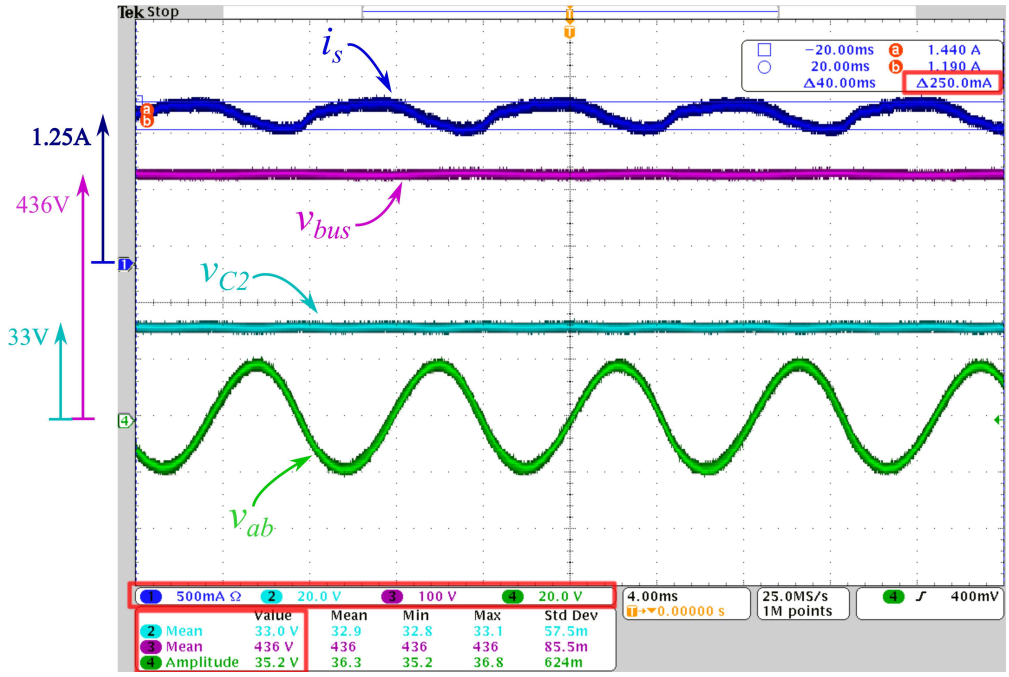


Figure 6.10: Experimental waveforms of the input current i_{in} (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage v_{bus} (channel 3) and C_3 voltage v_{C3} (channel 4) in the 25% load (0.5 kW) condition. The input current ripple is 250 mA as highlighted on the top-right corner.

magnitude of v_{C3} and the average of v_{C2} is almost the same given that the load current i_{out} is of the same magnitude. The buffer architecture operates the same with a lagging reactive load, since leading and lagging load with the same power factor will give identical load current i_{out}.

6.4.5 Startup

The startup sequence of the entire system including the inverter and the series-stacked buffer is shown in Fig. 6.15. Upon startup, the system is connected to the 450 V DC source and 10 Ω resistor through a soft-start circuit. This soft-start circuit is essentially a MOSFET in linear region to limit the inrush current into the capacitors. More details about this soft-start circuit is introduced in [9]. Such inrush current limiting mechanism is often found in systems with DC link capacitors as well. As the soft-start circuit is enabled, the buffer converter is switching at a constant duty ratio of 0.5, such that $v_{ab} = 0$. Therefore, C_1 is connected across the DC bus and is gradually charged up. Once the bus voltage reaches a certain level (200 V in this case), the buffer converter changes the duty ratio to 1, which effectively connect C_2 and C_1 in series, so both of them are being charged and the bus voltage

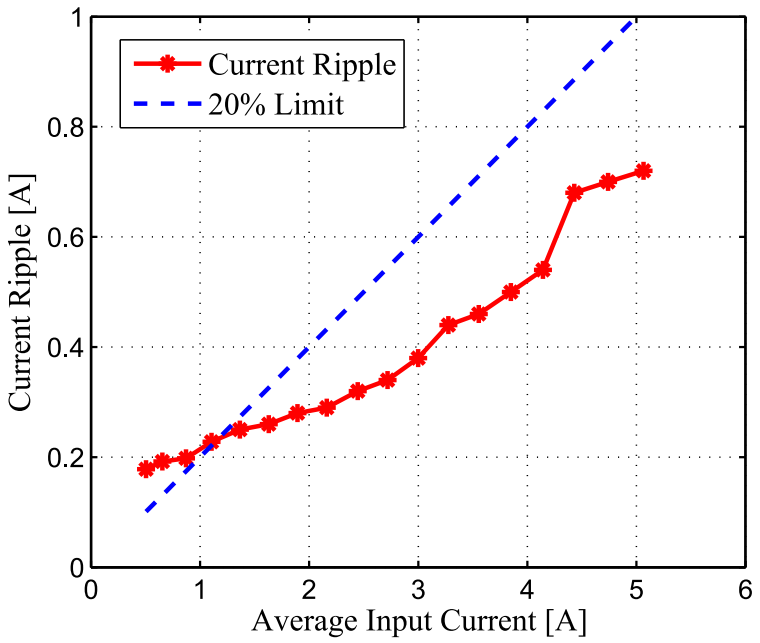


Figure 6.11: Current ripple in DC source current i_s under different power levels. Each power level is indicated by its average DC source current.

continues to rise. When the bus voltage reaches 300 V, the inverter is enabled and starts the AC output. This is in accordance with the requirement in [8]. Once there is AC output, current and voltage ripple are present on the DC side, then the loss compensation loop presented in Section 5.3 can effectively balance all the voltages. Therefore, all the control loops during normal operation are enabled at this point. The voltage on C_2 is automatically adjusted to the right value according to the load power, as discussed in Section 5.5. Note that in Fig. 6.15 the voltage on C_2 is regulated to a relatively low value as it is a light-load condition. The bus voltage continues to rise to above 400 V and then the soft-start circuit is bypassed by a fully on switch, which completes the startup sequence. Note that it is preferable to start with a light load on the AC side, as it is the case for Fig. 6.15. This is because once the AC output is enabled, the input current i_s increases depending on the load power level, which puts additional thermal burden on the soft-start circuit. Light-load condition reduces the time needed for the bus voltage to rise from 300 V to 400 V and the power loss on the soft-start circuit.

6.4.6 Efficiency measurement

The efficiency of the hardware prototype is evaluated. Since the power loss is very small compared to the total processed power, care must be taken to perform accurate power

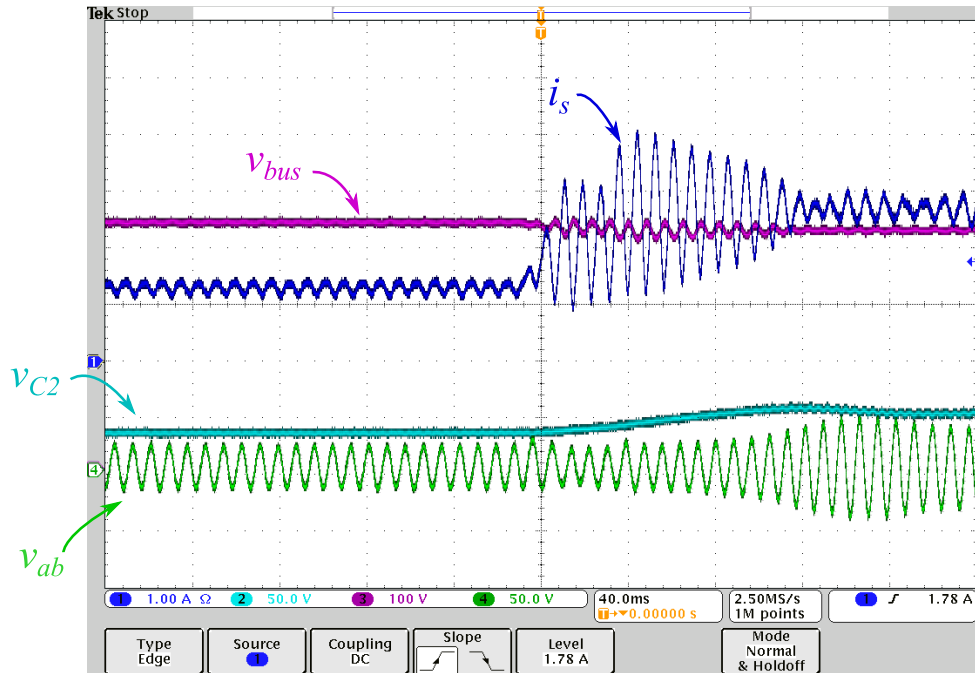


Figure 6.12: Experimental waveforms of the input current i_{in} (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage v_{bus} (channel 3) and C_3 voltage v_{C3} (channel 4) during a 25% load to 50% load step transient.

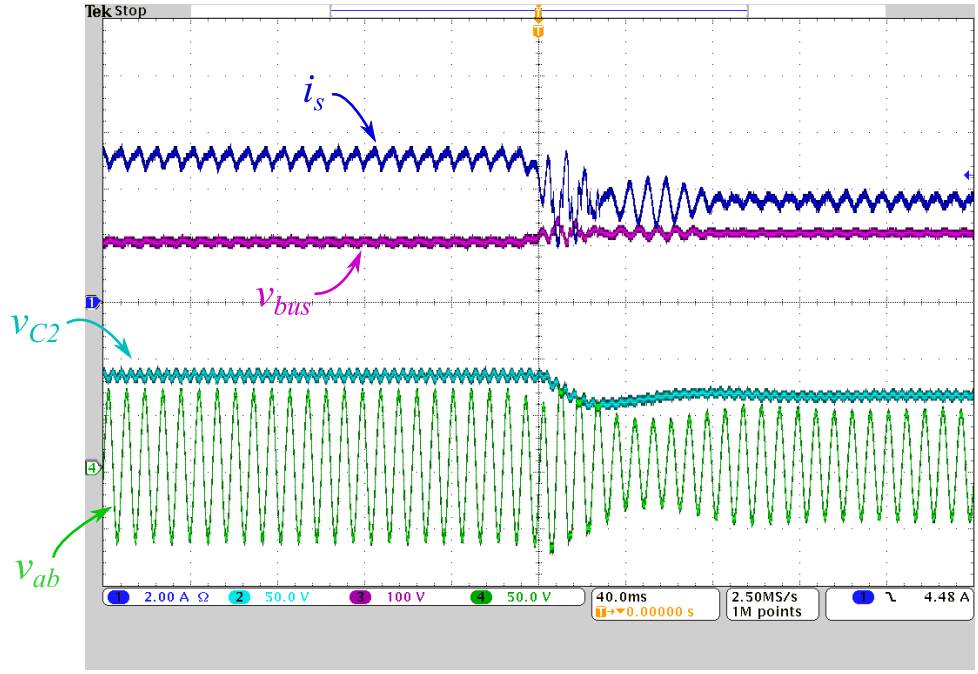


Figure 6.13: Experimental waveforms of the input current i_{in} (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage v_{bus} (channel 3) and C_3 voltage v_{C3} (channel 4) during a 100% load to 75% load step transient.

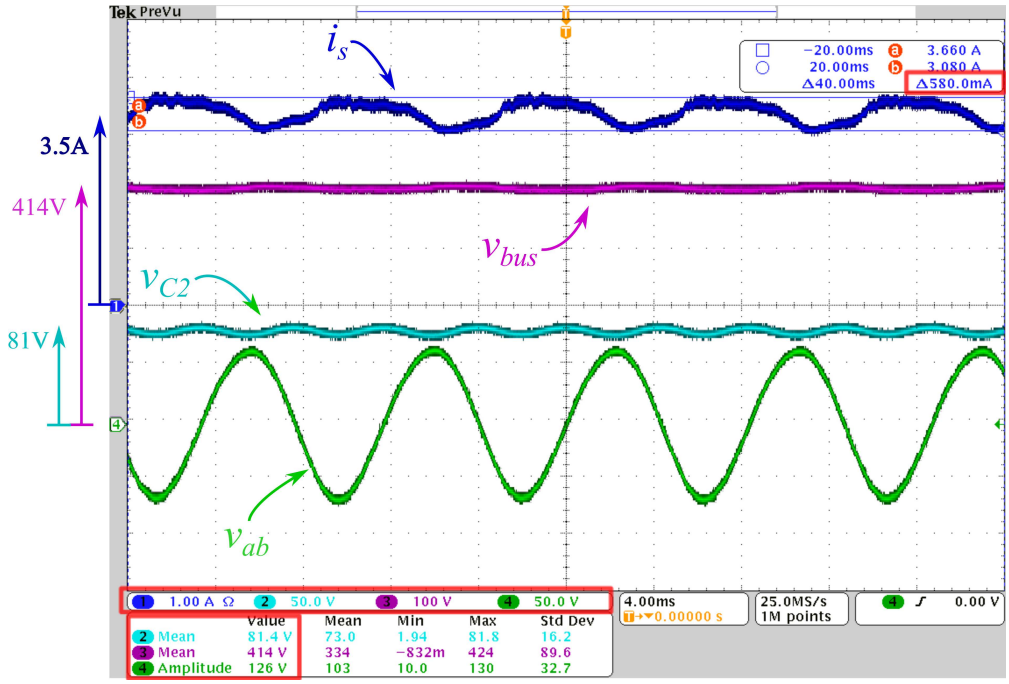


Figure 6.14: Experimental waveforms of the input current i_{in} (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage v_{bus} (channel 3) and C_3 voltage v_{C3} (channel 4) in a reactive load (2 kVA, PF = 0.72) condition.

measurement free from the interference of ripples, etc. To this end, we adapt the efficiency measurement setup intended for evaluating film and ceramic capacitors (both of which have very small loss factor) from [10]. A Yokogawa WT310 digital power meter is connected as shown in Fig. 6.5. The integration function of a Yokogawa WT310 power meter is used to measure the energy flowing into and out of the buffer branch for many line cycles. The ratio of the integrated outflow and inflow of the energy gives the buffer efficiency. The power measurements are conducted and integrated for 30 seconds. The efficiency measurement result is plotted in Fig. 6.16.

Note that the measured efficiency *excludes* controller and gate driver loss. This is because the auxiliary power (including micro-controller, gate driver, sensing circuit and cooling fans) is shared between the buffer circuit and the custom-made inverter. The auxiliary power for both of them is generated by the same auxiliary supply circuit when the full system is running. It is difficult to include the auxiliary power of the buffer part in the digital meter measurement as shown in Fig. 6.5. Instead, we estimate the auxiliary power for the buffer circuit alone is about 2.5 W. A detailed efficiency and loss breakdown of the overall inverter system is presented in [9].

As analyzed in Section 4.2, since the buffer converter is processing only a fraction of

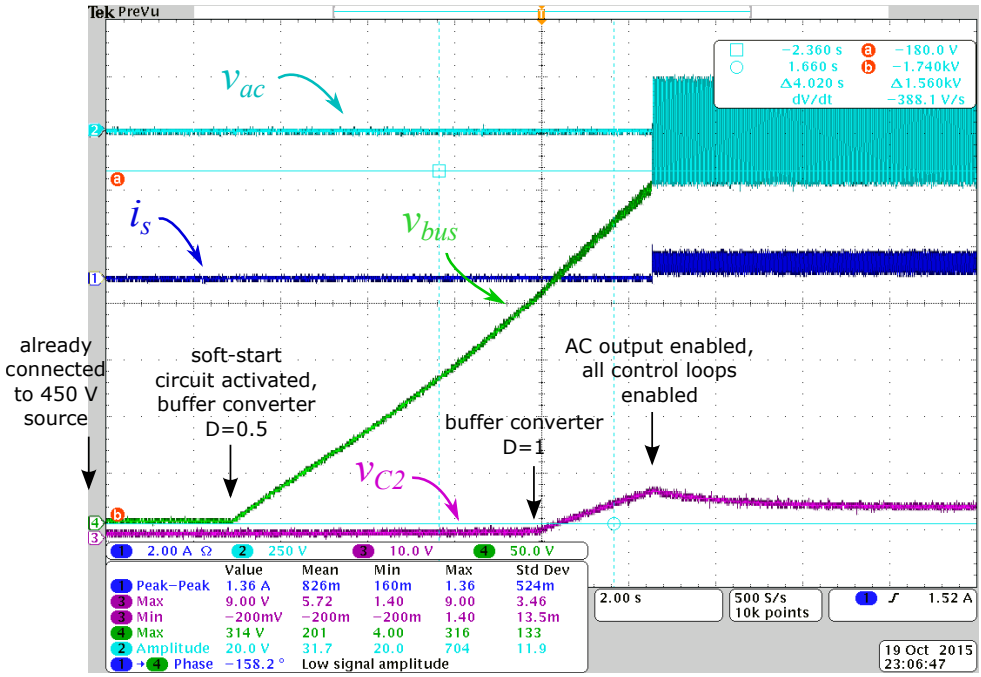


Figure 6.15: Experimental waveforms of the input current i_s (channel 1), inverter AC output voltage v_{ac} (channel 2), C_2 voltage v_{C2} (channel 3) and bus voltage v_{bus} (channel 4) during the startup.

the total power, the overall efficiency of the buffer architecture is decoupled from the buffer converter efficiency, yielding a very high efficiency. The partial power processing architecture and control scheme together result in a buffer efficiency higher than 99% across a wide load range, which is even comparable to the efficiency of passive decoupling with film or ceramic capacitors.

6.5 Comparison to literature

In this section, the proposed series-stacked buffer is compared with the state-of-the-art solutions in the literature. The difficulty for this comparison is that although there are a large number of papers on active decoupling, very few publish the result of hardware volume or power density. Some of the papers do not report efficiency as well. In fact, to the best of our knowledge, among publications before the year of 2016, only [13] directly gives the power density of the decoupling circuit. The power density in [72] is given together with an inverter and the power density of the decoupling stage alone cannot be inferred from the available information. A few other papers on active decoupling such as [36, 41, 72] provide certain information (component selection, photograph of the hardware prototype, etc.) from

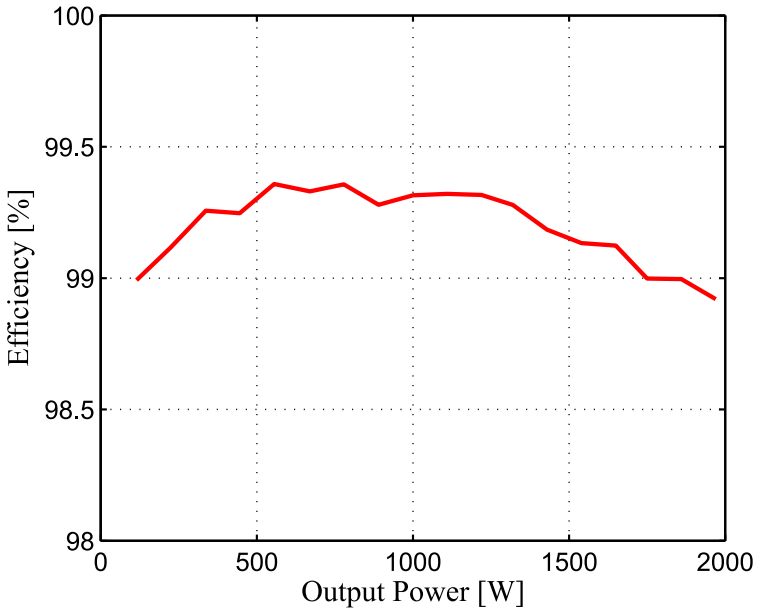


Figure 6.16: The efficiency of the buffer architecture as a function of the output power level with 450 V DC source voltage (DC bus voltage varies due to the 10 Ω source resistor).

which we make our best effort estimation. Many other solutions in the literature either do not provide enough hardware information for an estimate, or have power density similar to or lower than those compared have. The comparison result is listed in Table 6.3, where the nominal power, measured efficiency, hardware volume (by component volume and/or by the volume of the rectangular enclosure), power density (by component volume and/or by the volume of the rectangular enclosure) and ripple on the DC bus are compared. In general, the power density of comparable solutions in the literature is at least an order of magnitude lower compared to the series-stacked buffer architecture proposed in this work.

It should be noted that the recent Google/IEEE little box challenge unveils a few high power density single-phase inverter designs. Many of these designs incorporate high power density decoupling circuits. Although details of most of the designs are not available in the literature, upon the completion of this dissertation, three such designs were published. The performance metrics of these designs as presented in the papers are listed in the last three rows in Table 6.3. We note that our solution achieves the highest power density among these designs, and an efficiency that is close to the best passive solution.

Compared to other solutions in Table 6.3, the fundamental reason for the superior power density and efficiency achieved by the series-stacked buffer architecture is that the series-stacked topology allows for flexible tradeoff between the volume of the energy storage capacitors and the filter inductor and enables greatly increased efficiency owing to its partial power processing characteristics. In previous magnetic-based topologies such as [36, 38, 40, 41], the

filter inductor is under the full voltage stress of the bus voltage, so the filter inductor is typically much larger than the energy storage capacitor. The SSC topology [13] is on the opposite extreme where no inductor is used but the capacitor volume is relatively large. There is a middle ground where the inductor volume is balanced with capacitor volume for the minimum overall volume, but these aforementioned solutions do not allow trade-off between inductors and capacitors. Alternative topologies that allow such tradeoffs are first proposed conceptually in [73]. The work in [58, 59] represents an earlier attempt on developing a topology that allows such tradeoff, where the buffer converter only process the capacitor ripple voltage and the relative volume of the inductor and capacitors can be adjusted by choosing the magnitude of the capacitor ripple voltage allowed. However, the range of tradeoff is limited by the operating voltage of the AC/DC converter in the system, as analyzed in Section 3.5.

The proposed series-stacked topology is the first one to allow free tradeoff across the full voltage range. The magnitude of v_{ab} in Fig. 5.1 basically determines the volume of inductors and capacitors in the series-stacked buffer architecture and its value can be chosen anywhere between 0 and V_{bus} to minimize the overall volume. Moreover, as the technology of inductor and capacitor develops, the optimal point of their tradeoff might change. New designs of series-stacked buffers can readily adopt these changes, while the previous solution, again, does not allow such tradeoff. A key issue that previously made practical realizations of the application of the series-stacked buffer difficult is the average current mismatch problem due to the series connection of two components with different losses. In this work, we have presented a control scheme that solves this problem with no additional power stage hardware requirement.

Table 6.3: Comparison of the proposed series-stacked buffer and previous work in the literature

Reference	Decoupling Method	Power Level (W)	Efficiency	Volume ($inch^3$)	Energy Density ($W/inch^3$)	Bus Voltage Ripple
this work	series-stacked buffer (active)	2000	above 98.9%, peak 99.4%	by component: 2.01, by rectangular box: 4.88	by component: 995, by rectangular box: 410	2.5%
Chen et al. TPELS 2013 [13]	stacked switched-capacitor (active)	135	above 95.2%, peak 97%	by component: 1.7	by component: 79.4	20% (estimated)
Tang et al. TPELS 2015 [41]	symetrical half-bridge buffer (active)	1000	98% (estimated)	by component: >35 (estimated)	by component: <57 (estimated)	3% (estimated)
Wang et al. TPELS 2011 [36]	full ripple port buffer (active)	15000	98% (estimated)	by rectangular box: 347.8 (estimated)	by rectangular box: 43 (estimated)	5% (estimated)
Lyu et al. JESTPE 2016 [72]	series voltage compensator (active)	2000	above 92.7%, peak 96.3%	by rectangular box: 36.54 (including inverter)	by rectangular box: 55 (including inverter)	3%
Neumayr et al. ECCE Asia 2016 [61]	full ripple port buffer (active)	2000	peak 98.7%	by component: 2.9 (no cooling), by rectangular box: 4.7 (with cooling)	by component: 689 (no cooling), by rectangular box: 425 (with cooling)	<3%
Zhao et al. JESTPE 2016 [62]	LC filter (passive)	2000	peak 99.8% (estimated)	by component: 4.3 (estimated)	by component: 465 (estimated)	<3%
Zhao et al. APEC 2016 [35]	front-end buck converter (active)	2000	peak 99.6%	by rectangular box: 6.6	by rectangular box: 303	0.8%

CHAPTER 7

REVIEW OF FLYING CAPACITOR MULTILEVEL TOPOLOGY

The previous discussion from Chapter 3 to Chapter 6 addresses the high power density implementation of twice-line-frequency power pulsation decoupling. The fundamental idea of leveraging capacitor energy storage and minimizing magnetic components can be further explored in the second task of power transfer and waveform conversion between AC and DC. The technique that embodies this idea is the flying capacitor multilevel topology. A 1.5 kW PFC front end converter per Table 1.2 will be consider throughout Chapter 7 to Chapter 9 to illustrate this idea.

7.1 Motivation

For grid-connected power supply applications, PFC is often required to improve the power quality and conform to industrial standards (e.g., IEC 61000-3-2, Energy Star program, etc.). As discussed in Chapter 1, many of these AC-DC systems are volumetrically constrained, so achieving higher power density as well as high efficiency has become an important requirement.

Wide band-gap semiconductors (GaN and SiC) have been used in many recent works to improve power density [74–77]. These devices offer significant improvements in terms of fundamental figures of merit compared to their silicon counterparts. The switching frequency can thus be increased by an order of magnitude or more, enabling the use of smaller passive components in the converter circuit. However, despite the advances in semiconductors, the basic converter topology remains relatively unchanged. As will be discussed, in conventional topologies the merits of wide band-gap semiconductors have not been fully exploited. A further increase in the power density of PFC front ends would require more advanced topology as well.

Flying capacitor multilevel (FCML) converters have been conventionally used in high voltage and high power DC-AC applications [78–80]. It has been demonstrated recently that in several-hundred-volt, kilowatt-scale inverter applications, FCML converters also of-

fer considerable efficiency and power density advantages compared to many conventional topologies [9, 71, 81–85]. The FCML converter in these applications features low voltage stress on transistors and high switching frequency, allowing the design to take full advantage of the recent development of high-speed GaN transistor technologies with voltage ratings around 100 V [86].

The work presented explores the use of flying capacitor multilevel (FCML) converters in several-hundred-volt, kilowatt-scale PFC applications to further improve the power density and efficiency compared to state-of-the-art solutions. A seven-level FCML boost converter is developed as the PFC front end of a 1.5 kW, universal-input AC-DC rectifier system. The design allows for very high switching frequency, reduced filter inductor voltage stress and thus a significant reduction in the filter inductor size, while maintaining low switching loss and high overall efficiency.

7.2 Conventional boost (2-level) topology

For kilowatt level applications, boost converter remains the prevalent topology for PFC front ends. In a typical system, the AC line voltage is rectified by an active or diode full-bridge to produce a rectified voltage, then converted to a higher DC voltage (e.g., 400 V) by the boost converter. There are many other variations of this setup (e.g., bridgeless PFC, interleaving, etc.), but the basic circuit characteristics remains the same as a single boost converter. The power density of these conventional topologies has been improved by the wide band-gap semiconductors, but they still suffer a few shortcomings:

1. Magnetic components: In practice, the power density of power electronics system is often limited by the magnetic components; in conventional boost topology, the inductor must be sized to filter the full (0 to V_{out}) switch node voltage, which requires a large inductance to limit inductor current ripple. This leads to large core size, which may not be easily reduced by simply increasing the switching frequency due to inductor loss limitations.

2. Transistor voltage ratings: The transistors in a boost converter should be rated for a higher voltage than the output voltage plus enough margins. The high voltage rating inevitably increases the switching and conduction loss of either Si or wide band-gap transistors compared to their low-voltage-rated counterparts. Such loss limits the switching frequency of the converter and further contributes to large magnetic components and limited power density.

3. Electromagnetic interference (EMI) challenges: The improved switching characteristics of wide band-gap transistors enable faster turn-on and turn-off, which reduces device switching loss and allows for increased switching frequency. However, the faster switching transitions also give rise to more a challenging EMI environment. In a boost converter the switching node rapidly transitions between V_{out} and 0, causing large dv/dt transitions at this node, which leads to voltage ringing and overshoots due to the parasitic inductance. The larger packaging and layout necessary for high-voltage-rated transistors are also likely to give rise to more such parasitics. The ringing and overshoot can in turn requires higher voltage rating. In addition, large EMI filters are required which further decreasing the power density of the system.

4. Thermal management: In a boost converter, a large portion of the power loss is concentrated on the two transistors. While EMI considerations require a compact layout, it would create a single hot spot on the PCB and impose challenges to provide necessary cooling for the transistors.

7.3 Flying capacitor multilevel topology

The FCML topology can greatly alleviate the problems of the conventional boost topology. An in-depth comparison between these two topologies can be found in [87] and [71]. This section only briefly reviews the operation of an FCML converter to illustrate its advantages. The circuit schematic of an FCML converter is shown in Fig. 7.1 and the associated operation waveforms are plotted in Fig. 7.2. In a typical PFC application, assuming proper control has been implemented, the input to the converter is a rectified sinewave v_{rec} and the output is a constant DC voltage v_{out}. In this analysis, a seven-level FCML converter with 240 V (RMS) input and 400 V output is taken as an example. The switching node voltage, v_{sw} in Fig. 7.1, can have seven different levels, i.e., V_{out}, $\frac{5}{6}V_{\text{out}}$, $\frac{4}{6}V_{\text{out}}$, $\frac{3}{6}V_{\text{out}}$, $\frac{2}{6}V_{\text{out}}$, $\frac{1}{6}V_{\text{out}}$, and 0 V, depending on the duty ratio of the FCML converter. These different voltage levels form six voltage segments in which the pulse width modulation (PWM) can be operated, as shown in Fig. 7.2a. For example, when v_{rec} is in between $\frac{1}{6}V_{\text{out}}$ and $\frac{2}{6}V_{\text{out}}$, the circuit is modulated to produce a switching node voltage with a pulse train between $\frac{1}{6}V_{\text{out}}$ and $\frac{2}{6}V_{\text{out}}$ as well. Thus, the voltage pulses magnitude seen by the inductor, i.e., $(v_{\text{rec}} - v_{\text{sw}})$ shown in Fig. 7.2c, is always smaller than $\frac{1}{6}V_{\text{out}}$, which represents a reduction by a factor of six compared to the conventional boost converter. In this example, the inductor voltage stress is only 67 V even though the output voltage is as high as 400 V.

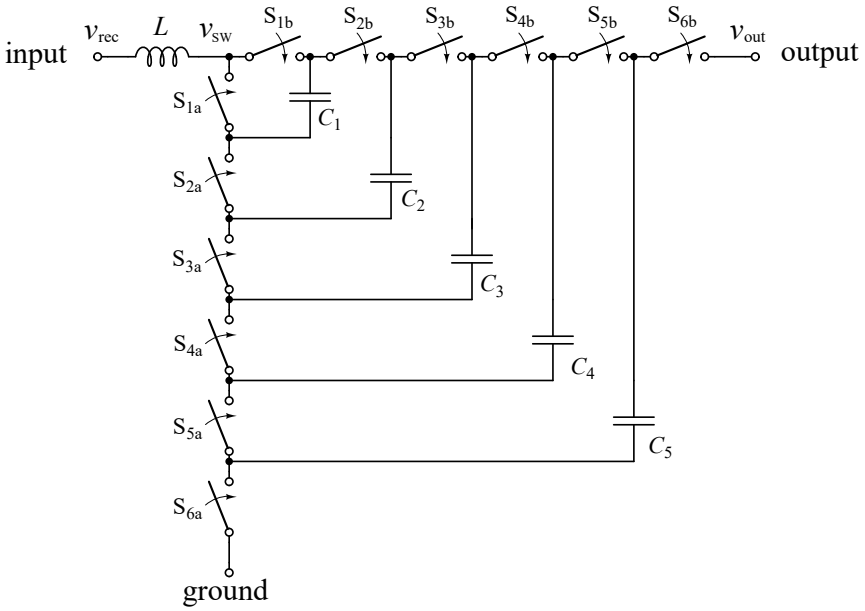


Figure 7.1: Schematic drawing of a seven-level FCML converter.

To generate the intermediate voltage levels, flying capacitors, $C_1 \sim C_5$, are placed in-between the series-connected switches $S_{1a} \sim S_{6b}$. For the n-th capacitor in an FCML converter with N levels, the nominal voltage is given by

$$V_{c,n} = \frac{n}{N-1} V_{\text{out}} \ . \tag{7.1}$$

As a result, the voltage stress of each switch, given by the difference between the voltages of adjacent capacitors, is reduced by a factor of $N-1$ compared to that of a conventional boost converter, i.e.,

$$V_{\text{switch}} = \frac{V_{\text{out}}}{N-1} \ . \tag{7.2}$$

The switch control signals for the FCML converter use identical frequency f_{sw} and duty ratio (i.e., D for all low side transistors $S_{1\text{a}} \sim S_{6\text{a}}$ and $1-D$ for all high side transistors $S_{1\text{b}} \sim S_{6\text{b}}$), but with phase shifts such that they are evenly distributed across a single switching period. Therefore, for a seven-level converter, the phase shift between PWM signals is 60 degrees, as shown in Fig. 7.2d. By comparing the switching node voltage (Fig. 7.2c) and the gate signals (Fig. 7.2d), one can see that in one complete transistor switching period, all the switches only make one pair of transitions, and yet six voltage pulses at the switching node are produced. In general, for an N-level FCML, a switching node frequency of $(N-1)f_{\text{sw}}$ is achieved with a transistor switching frequency of only f_{sw} [88]. The overall steady-state voltage conversion ratio of the FCML converter is consistent with the duty ratio of every

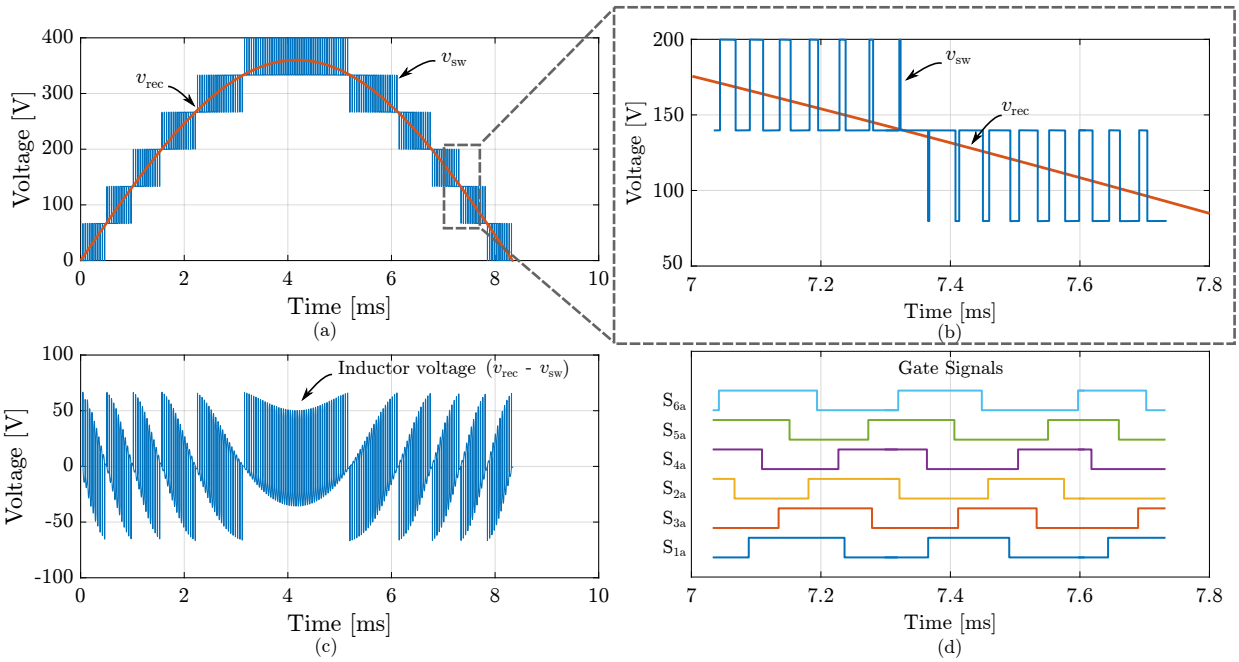


Figure 7.2: (a) Rectified input voltage and switching node voltage. (b) Switching node voltage zoomed in. (c) Inductor voltage ($v_{\text{rec}} - v_{\text{sw}}$). (d) Gate signals zoomed in.

transistor, i.e.,

$$V_{\text{out}} = \frac{1}{1-D} V_{\text{rec}} \ . \tag{7.3}$$

From the analysis of the FCML converter operation, it is clear that the FCML topology alleviates many of the aforementioned problems with a boost topology:

1. Magnetic components: With a seven-level converter, the voltage ripple seen by the inductor is reduced by a factor of six while the frequency seen by the inductor is increased by a factor of six. The worst-case ripple of the inductor current in an N-level FCML converter is proportional to the voltage and inversely proportional to the frequency, i.e.,

$$\Delta I_{L,\text{max}} = \frac{0.25 V_{\text{out}}}{(N-1)^2 f_{\text{sw}} L} \ , \tag{7.4}$$

   where f_{sw} is the transistor switching frequency (i.e., PWM frequency). Thus, the filter inductor of the seven-level converter can be reduced by a factor of 36 compared to a conventional boost converter with the same current ripple.

2. Transistor voltage ratings: As suggested by (7.2), the FCML topology allows for the use of low voltage GaN transistors in a high voltage system (e.g., 100 V rated devices for a 400 V output voltage). Lower voltage rating transistors have lower on-state

resistance and lower output capacitance compared to their high voltage counterparts, enabling a higher efficiency and/or an increased switching frequency.

3. EMI challenges: Although addressing the EMI challenge is not the focus of this work, it is expected that the FCML topology helps reduce EMI due to the smaller voltage transition between levels, lower voltage rated transistors used and higher effective switching frequency. It has been experimentally shown in [71] that a similar FCML converter design requires much a smaller EMI filter compared to the conventional boost topology.

4. Thermal management: While a boost converter and an FCML converter can be design to have very similar efficiency, the FCML topology can spread the transistor power loss across multiple transistors as opposed to a single hot spot in boost converter. Therefore, the FCML converter has larger surface area for more effective cooling.

In addition, the frequency-multiplying feature of the FCML topology also provides a control advantage in the increasingly used digital control of power electronics. For digital PWM, there is a well-known tradeoff between PWM frequency, PWM resolution and modulator clock frequency / area of delay line [89]. In a conventional boost topology, high PWM frequency is required to achieve high switching node frequency, so very high modulator clock frequency and/or very large area for delay lines is required for adequate PWM resolution. In comparison, the FCML topology has only moderate requirement on the PWM modulator since high frequency PWM is not needed to achieve high switching node frequency.

In summary, the aforementioned features of the FCML topology, especially the drastic reduction in the filter inductor, make the FCML converter topology a very promising solution for digitally controlled, high-power-density and high-efficiency PFC front end. The focus of this part of the dissertation is therefore to provide a complete circuit and digital control design and implementation for this FCML converter based PFC front end converter.

CHAPTER 8

CONTROL FOR PFC OPERATION

While the proposed seven-level FCML converter enables high efficiency and power density, its unique characteristics also introduce challenges to control its PFC operation. This chapter discusses the PFC control, identifies the challenges and proposes the solution.

8.1 Overview

The full system of the PFC front end is shown in Fig. 8.1. The design specifications and key parameters are listed in Table 8.1 (specifications reprinted from Table 1.2). The line voltage input v_{AC} is processed by an active full-bridge rectifier commuting at line frequency to generate a rectified sine wave v_{rec}, then boosted by the seven-level FCML converter to a constant output voltage v_{out}. As will be shown in Section 9.1, the topology with seven voltage levels is selected in this design as it provides the best balance between filter inductor volume, circuit complexity and available transistor ratings. To achieve high power density, a filter inductor as small as 44 μH (as opposed to mH in a comparable boost topology design) and a high effective switching frequency are chosen for the seven-level FCML converter per the analysis in Section 7.2. It is well known that the output power of the PFC front end is a shifted sine wave pulsating at twice line frequency due to the nature of single-phase AC input. An energy buffer is therefore needed at the output to decouple the power pulsation from the DC load. Since the focus for now is the PFC front end only, a simple passive decoupling method is used. That is, a large electrolytic capacitor bank C_{buf} is added in addition to the output filter capacitor of the FCML converter. For a fair comparison between different PFC front end designs, C_{buf} is *not* consider as part of the PFC front end when we evaluate the power density. The series-stacked buffer can later be adopted to optimize the power density of the overall system.

Synchronous boost converter operating in continuous conduction mode (CCM) is the common choice of operation mode in kilowatt level PFC applications for efficiency considerations. For the same reason, the seven-level FCML boost converter in this design is implemented as

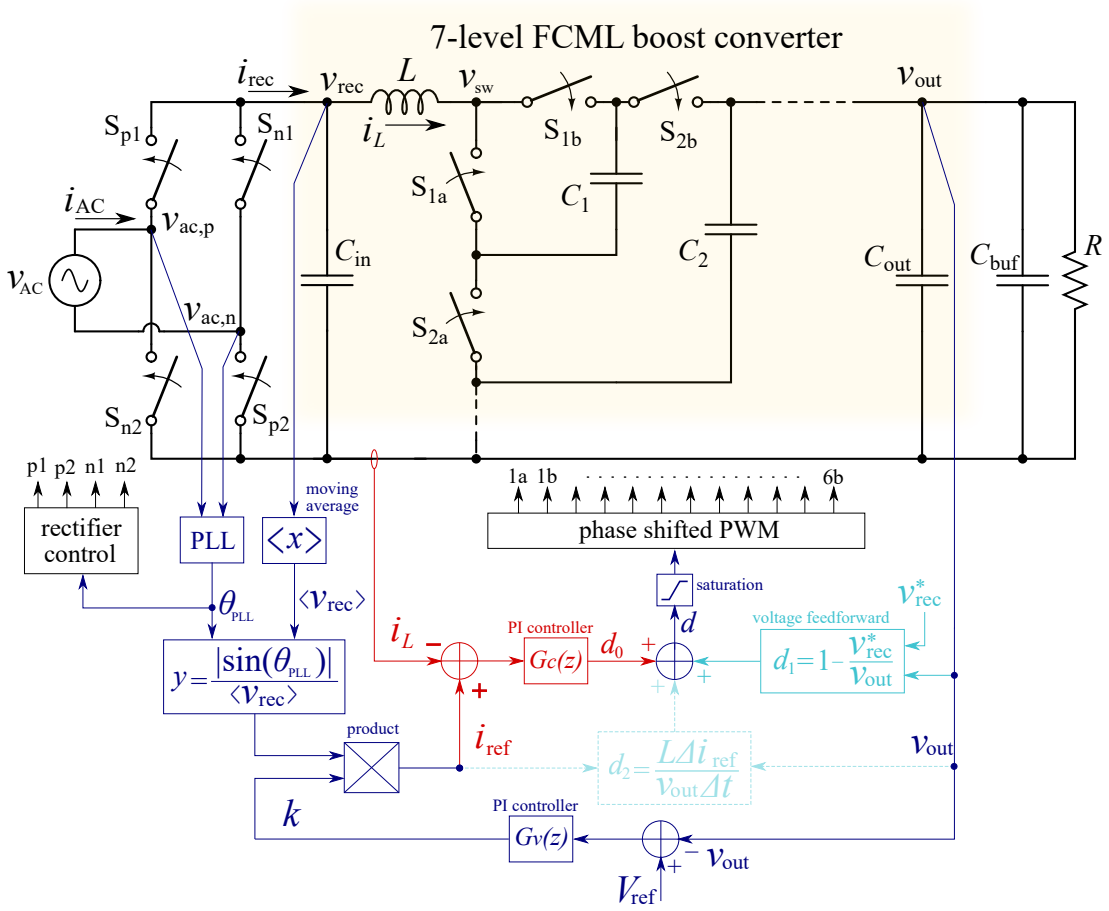


Figure 8.1: Schematic drawing of the proposed PFC converter together with control diagrams implemented in a micro-controller. The control scheme consists of inner current feedback loop (red), outer voltage feedback loop (blue) and voltage feedforward (turquoise). The analog sensing circuits (e.g., resistor divider, amplifier, etc.) interfacing the power stage and the micro-controller are omitted in this drawing.

a synchronous converter operating in CCM. A PFC control scheme similar to the classical multi-loop control [90, 91] is designed and implemented in a micro-controller as shown in Fig. 8.1. An inner current loop regulates the inductor current i_L to follow a desired current reference i_{ref} generated in phase with v_{rec}. An outer voltage loop adjusts the magnitude of the current reference i_{ref} to regulate the output voltage v_{out}. A voltage feedforward control term is also included to offset the disturbance due to changing input voltage and improve the control performance. With the feedforward and two feedback loops working together, the converter can achieve close-to-unity power factor and constant output voltage while maintaining a small input current THD. The rest of this section discusses the key control elements in detail.

Table 8.1: Specifications and key component selection of the PFC converter prototype

Specifications	Value
Input voltage	90 Vac – 260 Vac (RMS)
Output power	1500 W
Output voltage	400 Vdc
Output voltage ripple	< 5 V
Power factor	> 0.98
Input current THD	$< 3.5\%$
Transistor switching frequency	150 kHz
Effective switching node frequency	900 kHz
Input filter inductor L	44 μH
Input filter capacitor C_{in}	0.2 μF
Output filter capacitor C_{out}	10 μF
Flying capacitors C_1 - C_5	5 μF
Twice-line-frequency buffer capacitor C_{buf}	1560 μF

8.2 Reference current i_{ref}

Generating a low-harmonic, in-phase current reference i_{ref} for the inner current control loop is the first step toward unity power factor and low input current THD. A straightforward implementation adopted by many previous works [91–95] is to directly scale the measurement of v_{rec}, i.e.,

$$i_{\text{ref}} = k\frac{v_{\text{rec}}}{< v_{\text{rec}} >^2} \ , \tag{8.1}$$

where $< v_{\text{rec}} >$ is the line-cycle average of v_{rec}. Note that $\frac{1}{<v_{\text{rec}}>^2}$ is included in (8.1) such that the control loop design is compatible with a universal AC input voltage (i.e., 90 Vac to 260 Vac). That is, different magnitude of v_{rec} will not affect the loop gain of the outer voltage loop and v_{rec} is used only to determine the shape and phase of i_{ref}. The magnitude of i_{ref} is determined by a multiplying factor k provided by the outer voltage feedback loop.

Despite its simplicity in implementation, the direct scaling method suffers from noise spikes in v_{rec} measurements. The input current exhibits oscillations following a noisy reference and the current spike in turn introduces more noises in v_{rec} measurements, especially near incidents of input current zero-crossing. Moreover, with direct scaling, harmonics in the utility main voltage will also couple into the current reference and degrades the input current THD. Although these problems can be solved with sufficient analog or digital filtering, such sufficient filtering may introduce an unacceptable phase delay between i_{ref} and v_{rec}.

To precisely match the phase of the input current to the input voltage and reject dis-

turbance due to measurement noise, a phase-locked loop (PLL) based on adaptive notch filter [96] is adopted is this design. The PLL takes the measurements of the line voltage (i.e., $v_{\mathrm{ac,p}} - v_{\mathrm{ac,n}}$ in Fig. 8.1) and extracts the phase angle of its fundamental line frequency component θ_{PLL}. Then (8.1) can be modified to calculate i_{ref} as

$$i_{\mathrm{ref}} = k\frac{|\sin(\theta_{\mathrm{PLL}})|}{< v_{\mathrm{rec}} >} , \tag{8.2}$$

where $|\sin(\theta_{\mathrm{PLL}})|$ is the rectified value of a smooth sine wave and $< v_{\mathrm{rec}} >$ is nearly constant due to the low-pass nature of line-cycle average. Therefore, i_{ref} now has very low noise and distortion, allowing for very low input current THD. Note that the cycle average value $< v_{\mathrm{rec}} >$ is still needed in (8.2) to maintain a voltage loop gain independent of the universal AC input voltage.

8.3 Inner current loop

The task of the inner current loop is to generate the correct duty ratio d for the seven-level FCML converter to ensure that i_L closely follows i_{ref}. To study the dynamics of the FCML converter, we first make the observation that the flying capacitors in this design (i.e., C_1 to C_5) are two orders of magnitude smaller than the buffer capacitor C_{buf} connected to the output. In the frequency range of interest to the PFC control (i.e., up to tens of kilohertz), the effect of the flying capacitors on the circuit dynamics can be ignored compared to C_{buf}. We can exclude the switching frequency behavior of the FCML converter by applying switching cycle averaging, i.e., $v_{\mathrm{sw}} = (1-d)v_{\mathrm{out}}$. Then the dynamics of the FCML converter can be approximated by that of a boost converter, i.e.,

$$L\frac{\mathrm{d}i_L}{\mathrm{d}t} = v_{\mathrm{rec}} - (1-d)v_{\mathrm{out}} , \tag{8.3}$$

$$C\frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t} = (1-d)i_L - \frac{v_{\mathrm{out}}}{R} , \tag{8.4}$$

where d is the duty ratio of the low side transistors, R is the DC load resistance, L is the inductance of the FCML converter and C is the total capacitance connected to the FCML converter output (i.e., $C = C_{\mathrm{buf}} + C_{\mathrm{out}}$). The values of these components are listed in Table 8.1. These values are selected to meet the design specifications and optimize the power density, which are not necessarily preferable for the PFC control as shown later in this section. In this dynamic system v_{out}, i_L are the state variables and d, v_{rec} are the inputs. v_{rec} is often considered as a disturbance to the system. It is straightforward to apply small

signal approximation [69] to linearize (8.3) and (8.4) to get the control input to inductor current transfer function [97]

$$G_{i_L d} = \frac{\tilde{i}_L}{\tilde{d}} = \frac{2V_{\text{out}}}{R(1-D)^2} \cdot \frac{1 + \frac{sRC}{2}}{1 + \frac{sL}{R(1-D)^2} + \frac{s^2LC}{(1-D)^2}} \tag{8.5}$$

as well as the disturbance to inductor current transfer function

$$G_{i_L v_{\text{rec}}} = \frac{\tilde{i}_L}{\tilde{v}_{\text{rec}}} = \frac{1}{R(1-D)^2} \cdot \frac{1 + sRC}{1 + \frac{sL}{R(1-D)^2} + \frac{s^2LC}{(1-D)^2}} \quad . \tag{8.6}$$

With a controller G_c to close the inner current feedback loop, the small signal input current can be expressed as [69]

$$\tilde{i}_L = \frac{G_c G_{i_L d}}{1 + G_c G_{i_L d}} \tilde{i}_{\text{ref}} + \frac{G_{i_L v_{\text{rec}}}}{1 + G_c G_{i_L d}} \tilde{v}_{\text{rec}}. \tag{8.7}$$

As discussed in Section 8.2, i_{ref} is ideally generated in phase with v_{rec}, i.e., $\tilde{i}_{\text{ref}} = R_{\text{eq}}^{-1} \tilde{v}_{\text{rec}}$, where R_{eq} is the desired equivalent resistance of the input port. Note that R_{eq} is a known value that only changes with output power, i.e., $R_{\text{eq}} = R\frac{V_{\text{rec}}^2}{V_{\text{out}}^2}$. Then (8.7) can be further simplified to

$$\tilde{i}_L = \Big(\underbrace{\frac{G_c G_{i_L d} R_{\text{eq}}^{-1}}{1 + G_c G_{i_L d}}}_{Y_1} + \underbrace{\frac{G_{i_L v_{\text{rec}}}}{1 + G_c G_{i_L d}}}_{Y_2} \Big) \tilde{v}_{\text{rec}} = Y \tilde{v}_{\text{rec}}, \tag{8.8}$$

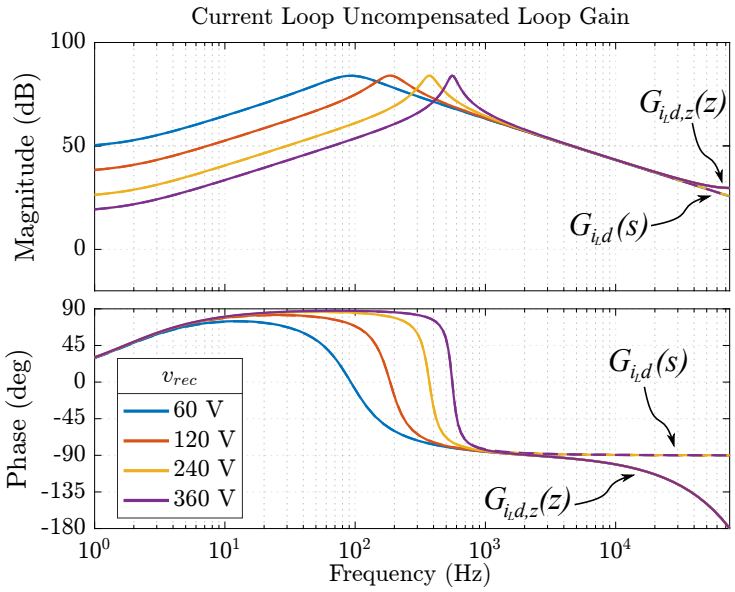
which readily gives the small signal admittance of the input port. According to (8.7), since the reference signal i_{ref} as well as v_{rec} contains DC component as well as AC component at twice line frequency and its harmonics, an adequate loop gain $G_c G_{i_L d}$ is needed at these frequencies to ensure that i_L closely tracks i_{ref} and the disturbance from v_{rec} is rejected. In other words, since ideally we would like the input port to appear resistive, i.e., $\tilde{i}_{\text{L}} = R_{\text{eq}}^{-1} \tilde{v}_{\text{rec}}$, we can make the observation from (8.8) that this requires an adequate loop gain $G_c G_{i_L d}$ such that Y_2 approaches zero while Y_1 reduces to R_{eq}^{-1} and dominates the total admittance Y.

Before we further consider the loop gain, it is important to note that all the above derivations are performed in the continuous-time domain to facilitate understanding, but the digital controller interacts with a sampled version of the system. Therefore, direct discrete-time modeling of the system has been performed. The transfer function given in (8.5) as well as its discrete counterpart (denoted as $G_{i_L d,z}$) are evaluated with the parameters in Table 8.1 and plotted in Fig. 8.2a. The discrete-time modeling process is mathematically involved and

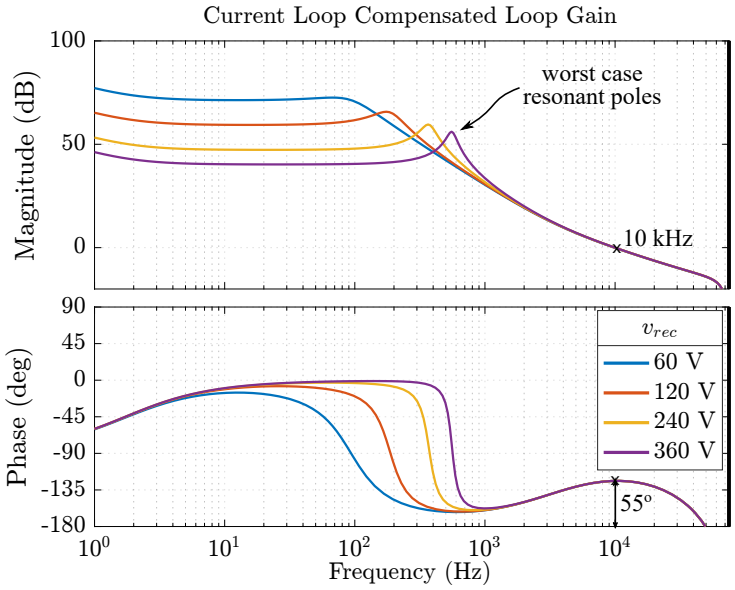
here we only show the result, but interested readers are referred to [98]. Symmetrical modulation is used in this design to minimize aliasing in the input current measurement and the modulation delay is calculated accordingly when evaluating $G_{i_L d,z}$. According to Fig. 8.2a, there is a significant phase lag due to the modulation delay in a digitally controlled system, which must be considered to ensure system stability. Therefore, in the following analysis we consider only the discrete model $G_{i_L d,z}$. A type-II compensator [99] denoted as $G_{c,z}$ is implemented in the micro-controller to stabilize the feedback loop with closed-loop bandwidth of 10 kHz. The compensated loop gain is shown in Fig. 8.2b.

For $G_{i_L d,z}$, a pair of resonant poles occur at $f_o = \frac{1-D}{2\pi\sqrt{LC}}$. It can be observed from Fig. 8.2b that starting from the crossover frequency, if we traverse the loop gain magnitude curve from right to left, the loop gain increases at 40 dB per decade as the frequency decreases until the resonant poles at f_o. Left to f_o, the loop gain magnitude remains flat expect for very low frequency. In other words, with a certain crossover frequency, the loop gain at twice line frequency (100 Hz or 120 Hz) might be limited by the resonant poles. The frequency of the resonant poles f_o varies within each line cycle according to the instantaneous value of v_{rec} (since $1 - D = \frac{V_{\text{rec}}}{V_{\text{out}}}$). The highest resonant pole frequency (i.e., worst-case condition) occurs at the peak input voltage under high line condition. For a conventional PFC design with a boost converter, the filter inductor L is typically large (i.e., on the order of mH), leading to the worst-case f_o below 100 Hz. The gain at twice line frequency is therefore not affected and a loop gain crossover frequency of 10 kHz results in 80 dB gain at twice line frequency. Such high gain is adequate to achieve a close-to-unity power factor according to the aforementioned analysis on (8.7) and (8.8). However, for the seven-level FCML converter in this work, the inductor is two orders of magnitude smaller than that in a typical design of an equivalent boost converter. The worst-case resonant pole frequency f_o in this design thus occur well above 100 Hz, as illustrated in Fig. 8.2b. With 10 kHz crossover frequency, the loop gain at twice line frequency could be below 40 dB. As given in (8.8), the admittance of the seven-level FCML converter in this case is plotted in Fig. 8.3a. As expected, the loop gain is inadequate to reject the disturbance and the disturbance term Y_2 in the input admittance starts to dominate above 100 Hz. The total admittance Y exhibits a large variation of magnitude at different frequencies, resulting in distortion of the input current and thus high THD. Its phase has a large leading phase angle at twice line frequency (i.e., 33°), leading to poor power factor and zero-crossing distortion [100].

For conventional boost based PFC with large filter inductors, the current phase leading problem is negligible at line frequency. However, it becomes an important issue with high frequency AC input (i.e., a few hundred hertz to a few kilohertz) in airborne system or other microgrid applications. Therefore, this problem has been well analyzed in the literature [92,



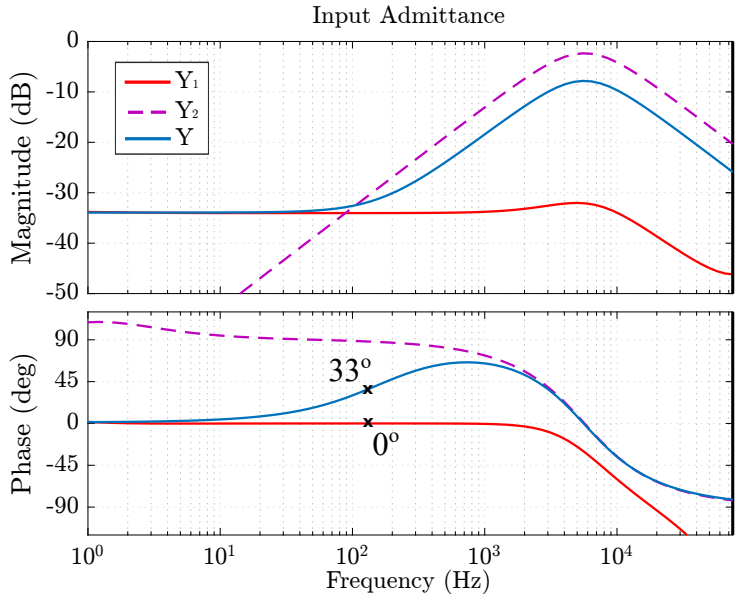
(a) Uncompensated current loop gain $G_{i_L d}(s)$ and $G_{i_L d,z}(z)$. Note the phase lag introduced by the digital control delay near sampling frequency.



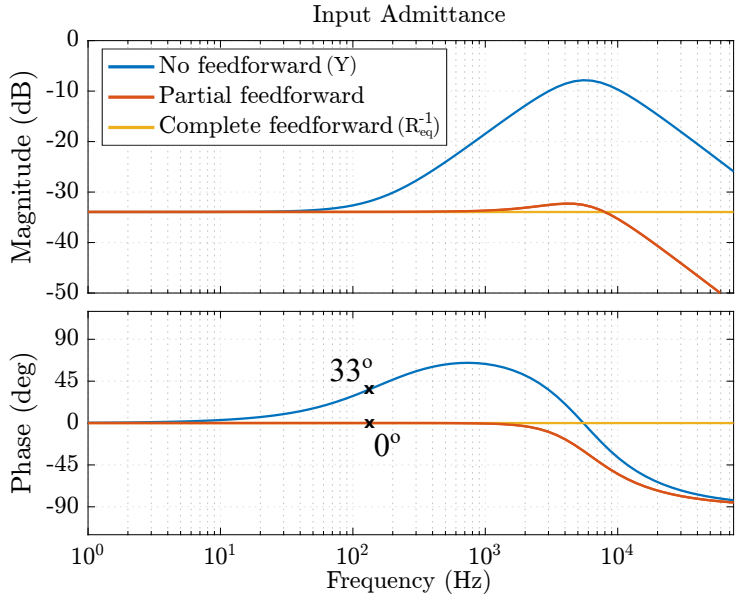
(b) Compensated current loop gain $G_{c,z}(z)G_{i_L d,z}(z)$. The feedback loop is closed at 10 kHz with 55° phase margin.

Figure 8.2: Loop gain of the inner current feedback loop (highlighted in red in Fig. 8.1). The magnitude and phase varies with different instantaneous input voltage v_{rec}.

93, 101] and various solutions has been proposed [91–93, 95, 97]. The phase-leading problem in the seven-level FCML converter happens in a different scenario with line-frequency and small inductors, but the root cause is essentially the same, so most of these solutions are



(a) Input admittance of the seven-level FCML converter with no feedforward but only feedback control as specified in (8.8).



(b) Comparison of input admittance with and without feedforward control.

Figure 8.3: Input admittance of the seven-level FCML converter with different control methods at peak input voltage.

applicable to the seven-level FCML converter control.

A straightforward method to suppress the current phase leading is to ensure enough gain at twice line frequency by increasing the crossover frequency by an order of magnitude or

more. In digitally controller power converters, it is a common practice to select the crossover frequency to be an order of magnitude lower than the sampling frequency such that the phase lag caused by the modulation delay will not significantly degrade the achievable phase margin. It is also a common practice to sample at the switching frequency to minimize sample aliasing due to switching ripple. In the FCML converter, we can even sample at the effective inductor frequency Nf_{sw} (i.e., 900 kHz as listed in Table 8.1) to allow for high closed-loop bandwidth. However, such high sampling frequency requires high-sampling-rate ADC and high-bandwidth analog sensing circuitry (e.g., current sensing amplifier). Therefore, while high crossover frequency is indeed an option for the seven-level FCML converter, we decide to use alternative solutions with less demanding sensing hardware requirement. In our control design, the sampling is performed at transistor switching frequency (i.e., 150 kHz) and the current feedback loop is designed to have 10 kHz crossover frequency as shown in Fig. 8.2b. The current phase leading problem is solved with feedforward control.

8.4 Feedforward control

The cause of the current leading problem is the disturbance from v_{rec} on i_L. Since v_{rec} can be directly measured from the circuit and its effect on the dynamics of i_L is completely defined in (8.3), a feedforward control term can be added to the duty ratio to anticipate the disturbance from v_{rec} and cancel out its effect. Suppose that we calculate a feedforward control input d_{ff} according to the following equation

$$d_{ff} = 1 - \frac{v_{\text{rec}}}{v_{\text{out}}} + \frac{L}{v_{\text{out}}} \frac{\mathrm{d}i_{\text{ref}}}{\mathrm{d}t}. \tag{8.9}$$

All the variables in (8.9) are either internal signal in the micro-controller or can be measured from the circuit, so we can calculate the duty ratio in real-time to use as the feedforward control input. One can easily verify (by substituting d_{ff} of (8.9) for d of (8.3)) that such feedforward control completely cancels out the disturbance and i_L will precisely follows i_{ref}. In other words, (8.8) reduces to $\tilde{i}_{\text{L}} = R_{\text{eq}}^{-1}\tilde{v}_{\text{rec}}$ for the entire frequency range. This method is referred to as complete feedforward in [92]. The same result has been obtained through feedback linearization in [91]. Ideally, no current feedback loop is necessary if (8.9) is implemented. In practice, the current feedback control is still needed to compensate for component variations, digital control delay and other non-idealities. The feedback term d_{fb} is combined with the feedforward term d_{ff} to form the control input to the seven-level FCML

converter as shown in Fig. 8.1, i.e.,

$$d = d_{ff} + d_{fb} = (1 - \frac{v_{\text{rec}}}{v_{\text{out}}} + \frac{L}{v_{\text{out}}}\frac{\mathrm{d}i_{\text{ref}}}{\mathrm{d}t}) + d_{fb}. \tag{8.10}$$

Because i_{ref} only changes at line frequency and the inductor L is especially small in the seven-level FCML converter, the contribution from the derivative term is very small compared to the voltage ratio term in (8.10). Therefore, the derivative term can be dropped to simplify the calculation, i.e.,

$$d = d_{ff} + d_{fb} = (1 - \frac{v_{\text{rec}}}{v_{\text{out}}}) + d_{fb}. \tag{8.11}$$

The missing term will mostly be compensated for by the feedback without noticeable degradation of the PFC performance. This simplification is referred to as partial feedforward in [92]. One can substitute (8.11) into (8.3) and (8.4) and go through the same steps from (8.5) to (8.8) to derive the input admittance in this case. The resulting input admittance under partial feedforward is plotted and compared with complete feedforward and no feedforward in Fig. 8.3b. The input admittance under partial feedforward approach constant R_{eq}^{-1} with almost zero phase shift up to a few kilohertz, enough to guarantee satisfactory PFC performance. Therefore, partial feedforward is implemented in the hardware prototype. Note that feedforward implemented directly in the form of (8.11) may suffer from measurement noise. Any noise in the v_{rec} measurement, especially near current zero-crossing, will directly affect the duty ratio and thus the input current. In our implementation, a signal equivalent to the line frequency component of v_{rec} is reconstructed from the moving average of v_{rec} and the PLL, i.e.,

$$v_{\text{rec}}^{*} = \frac{\pi}{2} < v_{\text{rec}} > |\sin(\theta_{\text{PLL}})|. \tag{8.12}$$

v_{rec}^{*} is used instead of v_{rec} in the implementation of (8.11).

8.5 Outer voltage loop

The outer voltage loop design follows the same approach as the conventional boost converter PFC. The outer voltage loop regulates the output voltage to the desired DC value (i.e., 400 V) by scaling the magnitude of the input current. As shown in Fig. 8.1, the output voltage loop provides a multiplying factor k to the current loop reference. The bandwidth of the two control loops are well separated by design (the inner current loop is three orders of magnitude faster than outer voltage loop) such that for the voltage loop, the behavior of the current loop can be approximated as an ideal current source. As a result, the transfer

function from the multiplying factor k to the output voltage V_{out} is given as [69]

$$G_{vk} = \frac{\tilde{v_{\text{out}}}}{\tilde{v_{\text{c}}}} = \frac{v_{\text{rec}}^2}{< v_{\text{rec}} >^2 V_{\text{out}}} \cdot \frac{1}{Cs}. \tag{8.13}$$

A PI controller is implemented to compensate the voltage loop gain. The crossover frequency of the voltage loop is designed to be below 10 Hz to attenuate the output voltage ripple at twice line frequency. Such low bandwidth negatively affects the transient response of the converter during start-up and load step changes. Techniques such as load current feedforward can be implemented to improve the output dynamics [91].

8.6 Simulation

Simulation is performed in PLECS to verify the control design under various load and input voltage conditions. The seven-level FCML converter is constructed as shown in Fig. 7.1 and the control flow illustrated in Fig. 8.1 are implemented in C-script blocks to emulate the micro-controller. Figure 8.4 shows one example where the input voltage is 240 Vac and the load power is 1.5 kW. The switching node voltage v_{sw} of the seven-level FCML converter exhibits the staircase waveform following the shape of v_{rec} and the output voltage v_{out} is well regulated at 400 V. As the feedforward control cancels out most of the disturbance from the input voltage, the input current to the seven-level FCML i_{rec} follows the reference i_{ref} generated from PLL very closely and unity power factor is achieved. Figure 8.4 also plots the duty ratio contribution from the feedforward term, the feedback term and the derivative term as in (8.10). Note that the control is implemented as (8.11) and the derivative term is not used in control, but shown here for comparison purpose. Most of the control input d is formulated by the partial feedforward. The feedback loop only provides very small modifications to compensate for non-idealities such as delay in the feedforward calculation. The contribution from the derivative term is indeed small enough to justify the simplification from (8.10) to (8.11). Note that as shown in Fig. 8.4, due to the discontinuity introduced by the active rectifier, the feedback term exhibits a "jump" at zero-crossing. Ideally, we would like the feedback term to change abruptly at zero-crossing, such that all the non-ideality is fully compensated and i_L always follows i_{ref} perfectly. But in practice, the PI controller output takes a short time to adjust. In other words, the sharp transition of i_{ref} contains high harmonics that are difficult to track with moderate control bandwidth. As a result, the input current exhibits a small spike near zero-crossing, which has also observed in the experiments in Section 9.2. This is one of the reasons why measurements near zero-crossing

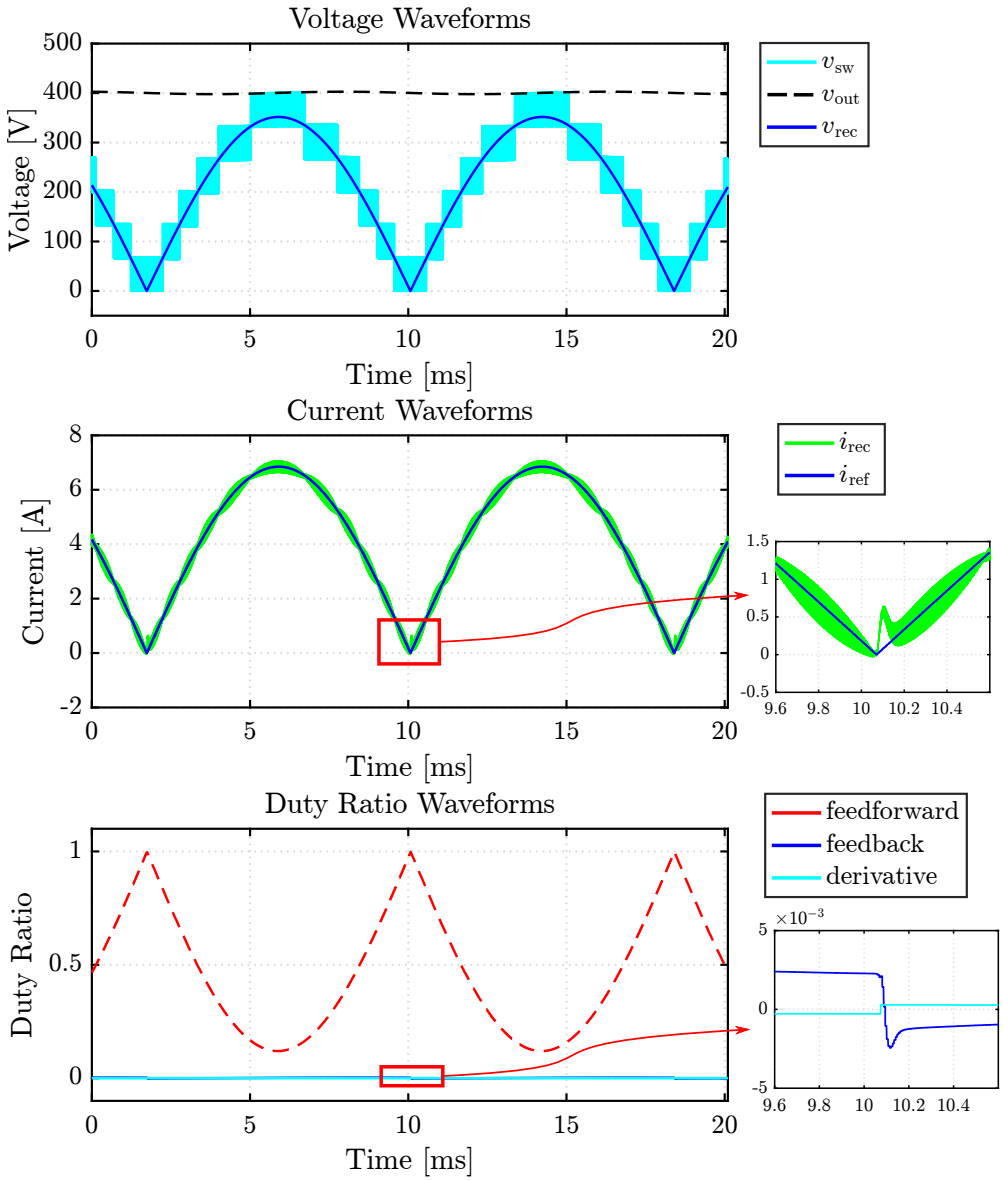


Figure 8.4: Simulation waveforms under the condition of 240 Vac input, 1.3 kW load power.

are subject to more noises and spikes as mentioned previous. Nevertheless, as shown in Section 9.2, this current spike has very limited impact on the input current THD expect for extremely light load conditions.

CHAPTER 9

FCML PFC FRONT END HARDWARE PROTOTYPE AND EXPERIMENTAL RESULTS

9.1 Hardware prototype

A hardware prototype of the seven-level FCML converter based PFC front end is designed according to the specifications in Table 8.1 and implemented as shown in Fig. 9.1 and Fig. 9.2. All the elements shown in Fig. 8.1 except C_{buf} and R are included in the hardware prototype. The important components used in the prototype are listed in Table 9.1. The practical implementation of these key elements is discussed in this chapter.

9.1.1 Power stage

The power stage consists of the active rectifier and the seven-level FCML converter. The switches in the active rectifier (i.e., S_{p1}, S_{p2}, S_{n1}, S_{n1} in Fig. 8.1) are each implemented by four MOSFETs in parallel to reduce conduction loss. The 400 V, seven-level FCML converter has a nominal transistor voltage stress of 67 V, so 12 of 100 V rated GaN transistor are used. Each GaN transistor has much smaller power loss compared to its high voltage counterparts. While the combined power loss of all the GaN transistors is comparable to that of a conventional boost converter, this loss is distrusted among the GaN transistors in a relatively large area, allowing more surface for effective cooling.

The flying capacitors and the input filter inductor are placed on the back side of the PCB. As analyzed in Section 7.2, the volume of the inductor is much reduced due to the FCML topology, despite a small volume overhead of the flying capacitors. A seven-level design provides a good balance between the inductor and capacitor volume. A greater number of levels would result in the flying capacitors dominating the overall volume, while a smaller number of levels does not reduce the inductor volume enough. Besides the absolute volume reduction, the FCML topology also allows much flexibility to choose the dimension of the inductor to improve the form factor of the entire prototype. A low-profile inductor is chosen to match the height of the stacked flying capacitors, as illustrated by the side view in Fig. 9.1,

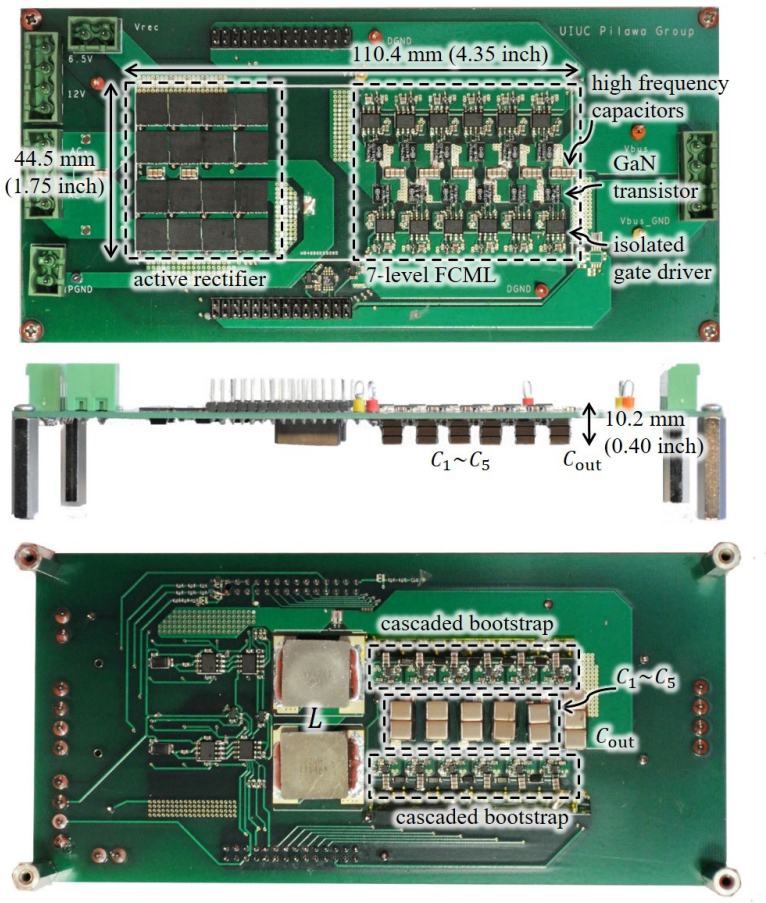


Figure 9.1: Front, side and back view of the hardware prototype with key components highlighted.

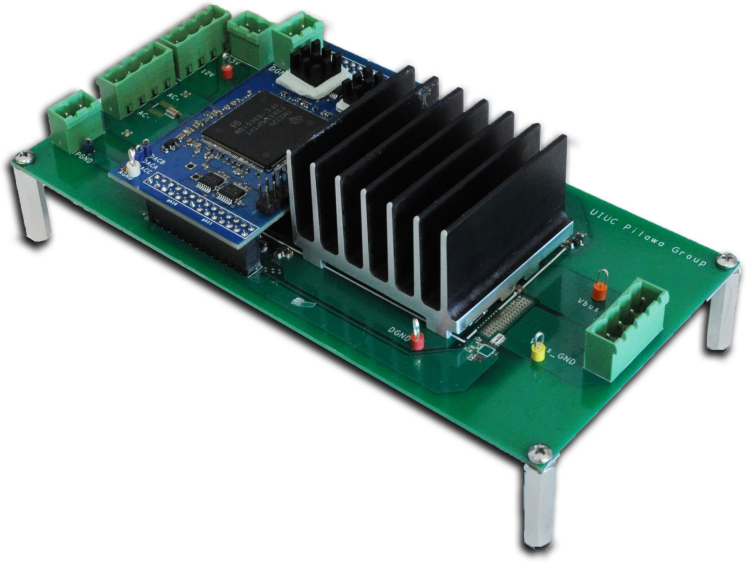


Figure 9.2: Hardware prototype with the controller board and heatsink installed.

Table 9.1: Component listing of the hardware prototype

Function block	Component	Mfr. & Part number	Parameters
seven-level FCML	GaN FETs	GaN Systems GS61004B	100 V, 15 mΩ
	Capacitors ($C_1 \sim C_5$)	TDK C5750X6S2W225K250KA × 6	450 V, 2.2 μF
	Capacitors (C_{out})	TDK C5750X6S2W225K250KA × 9	450 V, 2.2 μF
	Capacitors C_{in})	TDK C2012X7T2W473K125AE × 6	450 V, 0.047 μF
	Inductors (L)	Vishay IHLP6767GZER220M01 × 2	23 A, 22 μH
Cascaded bootstrap	Isolated gate drivers	Silicon Labs SI8271GB-IS	
	Bootstrap diodes	Vishay VS-2EFH02HM3/I	
	Adjustable LDO	Texas Instrument TPS71501DCKR	
	Capacitors (C_b)	Murata ZRB18AR61E106ME01L × 4	25 V, 10 μF
Active rectifier	MOSFET	STMicroelectronics STL57N65M5	650 V, 61 mΩ
	Gate driver	Fairchild Semiconductor FAN73932MX	
Controller board	Logic level shifters	Texas Instruments SN74LV4T125PWR	
	Microcontroller	Texas Instruments TMX320F28377D	

such that the overall system fits into a smaller rectangular volume.

The GaN transistors in the seven-level FCML converter feature low on-resistance *and* low output capacitance compared to its silicon counterparts. Therefore, the current-voltage overlap during the switching transition contributes the most significantly to the transistor power loss. So the current-voltage overlap needs to be minimized to improve efficiency. On the other hand, fast switching transition induces voltage ringing across the transistor drain and source terminal. Excessive voltage ringing can cause gate oscillation or voltage breakdown. Therefore, care must be taken to minimize the commutation loop parasitic inductance by improving layout and adding high-frequency decoupling capacitor. At the same time, adequate gate resistance must be added to the gate driving loop to slow down the turn-on transition. The best resistance value is often determined by a trial-and-error process. A detailed discussion on the parasitics and voltage ringing for FCML topology can be found in [71]. Another important issue with the FCML converter is the voltage balancing of flying capacitors, i.e., how close the flying capacitor voltages stay to its nominal value specified in (7.1). While active balancing techniques have been proposed in the literature [102–104], they require either high bandwidth measurement of the switching node (i.e., higher than the effective switching node frequency) or high common mode voltage measurement of all the flying capacitors, both of which impose practical challenges. Instead, the seven-level FCML converter in this design relies on a natural balancing mechanism provided by the small power loss in the inductor. More detailed explanation of the balancing mechanism can also be found in [71].

9.1.2 Cascaded bootstrap

The seven-level FCML converter requires floating power supply to the gate drivers of all transistors. In previous work, the gate driver power is mostly provided by isolated converters. One such example is the ADuM 5210 from Analog Devices used in [71, 102], which features much smaller volume compared to other comparable isolated converters. However, the efficiency of ADuM 5210 is typically below 30% and the output voltage is limited to 5.5 V, while the GaN transistors from GaN Systems require 6 V gate driving voltage to reduce on-resistance. Other isolated converts might result in the gate driving circuit being much larger than the GaN transistor itself. Therefore, to achieve a very compact design and provide 6 V gate driving voltage, a cascaded bootstrap scheme is implemented as shown in Fig. 9.3. The cascade scheme is an extension of the conventional bootstrap scheme in a buck converter and follows similar operating principal and design procedures to size the bootstrap capacitor. Interested readers can refer to [105–107] for design details and discussions on issues such as overcharge due to bode diode conduction, etc. On a high level, the bootstrap capacitor C_{b} of a certain level gets charged when the transistor of the adjacent lower level conducts. For example, in Fig. 9.3, $C_{\mathrm{b,4a}}$ is charged by $C_{\mathrm{b,5a}}$ through $\mathrm{D_{5a}}$ when $\mathrm{S_{5a}}$ conducts. At each level, the bootstrap capacitor voltage decrease by one diode forward voltage from previous level. The input voltage to the entire bootstrap circuit is selected to be 16 V to ensure sufficient voltage at the highest level after considering the worst-case voltage drop. An LDO is placed at each level to supply well-regulated 6 V to the gate driving circuit.

It should be emphasized again that C_b can only be charged when the transistor of the lower level conducts. We can make the observation from Fig. 8.4 that the duty ratio of the seven-level FCML converter approaches one near the AC zero-crossing, resulting in very short conduction time of the high side transistors (i.e., $\mathrm{S_{1b}} \sim \mathrm{S_{6b}}$). Therefore, high side bootstrap capacitors might not be able to maintain a high enough voltage near AC zero-crossing instances if the bootstrap capacitor is too small. Therefore, C_{b} in this design is sized up considerably (i.e., 40 μF) compared to DC-DC applications [105] to ensure high enough voltage anytime in an entire line cycle.

9.1.3 Controller

A custom-made control board is attached to the main power board as shown in Fig. 9.2. The control board integrates a TI F28377D micro-controller and its supporting circuit (e.g., voltage regulators, etc.). The control flow outlined in Fig. 8.1 is fully implemented in the micro-controller. The micro-controller converts the duty ratio value calculated by the con-

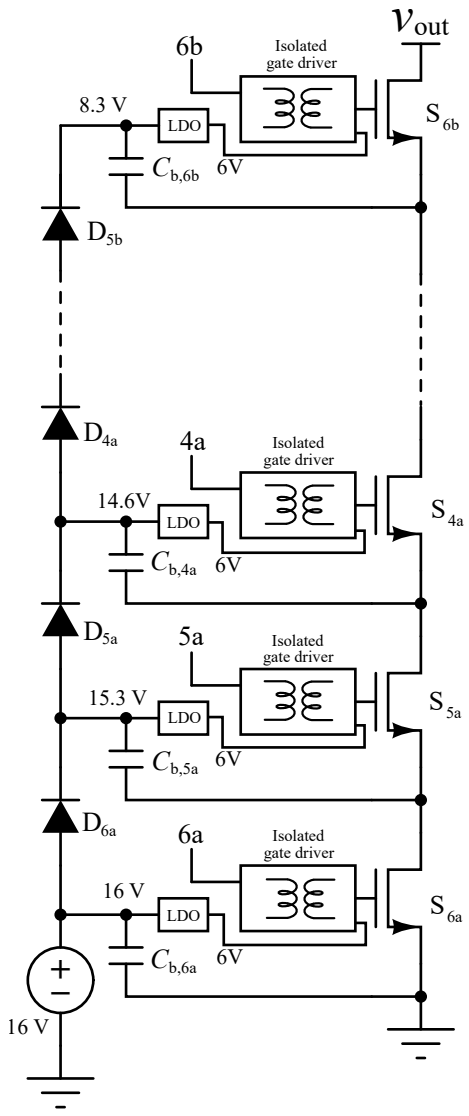


Figure 9.3: Schematic drawing of the cascaded bootstrap scheme to provide floating gate driving power to the FCML converter.

trol loop into 12 channels of phase-shifted PWM signals to control the seven-level FCML converter. All the ADC sampling and control loop calculations are synchronized with the transistor PWM at 150 kHz.

9.2 Experimental results

The hardware prototype has been tested in various experiments to verify its performance. The experiment setup consists of an AC voltage source (Pacific power source 112-AMX),

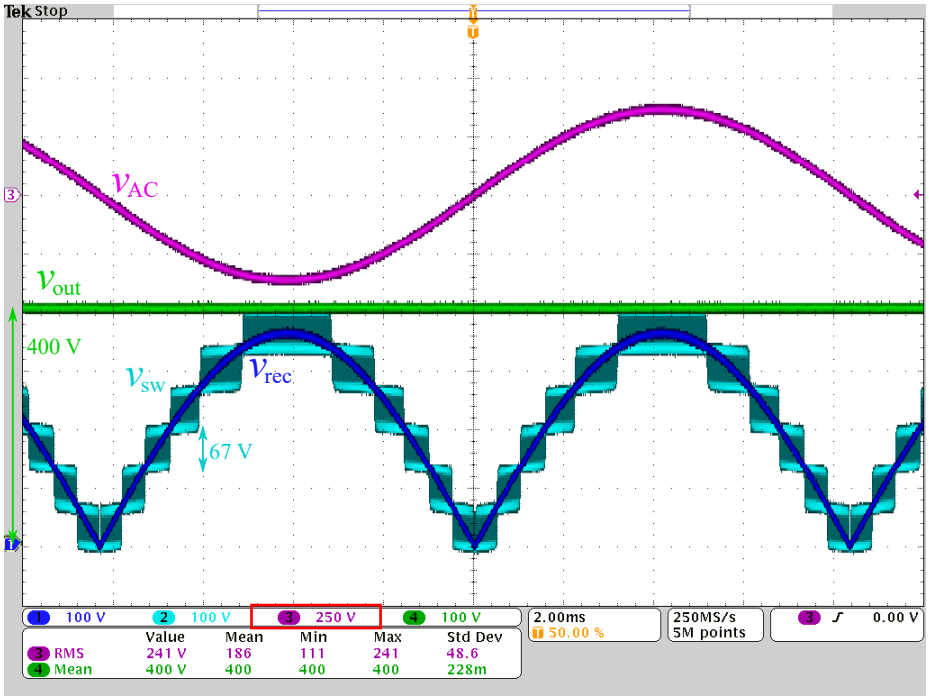
a DC load (Chroma 63204 DC electronic load) and two digital power analyzers (Yokogawa WT310) to measure the input and output specifications.

The first experiment is to verify the multilevel operation of the seven-level FCML converter. This is illustrated in Fig. 9.4 for both high line and low line conditions. The output voltage is boosted to 400 V while the switching node voltage v_{sw} exhibits staircase waveform with 67 V increments. In high line condition, the switching node voltage v_{sw} transition through all seven levels from 0 V to v_{out} and follows the trajectory of the rectified input voltage v_{rec}, as expected from Fig. 7.2 and Fig. 8.4. In low line condition, only the lowest four levels are exercised as the peak of v_{rec} is lower than the fourth level.

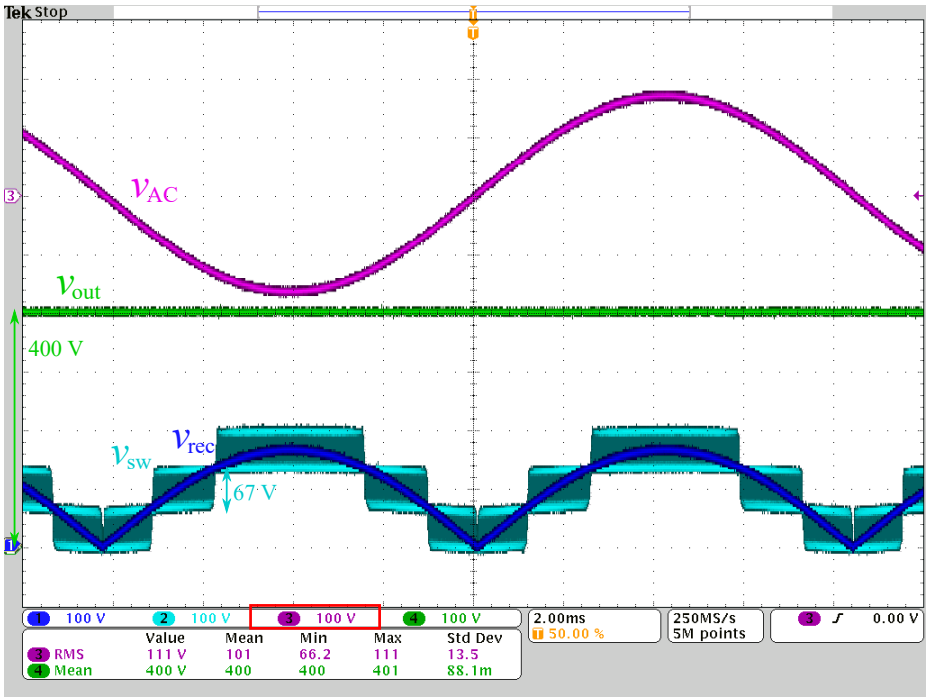
The PFC operation under high line and low line condition is shown in Fig. 9.5 and Fig. 9.6. The performance measured with the digital power analyzers (i.e., efficiency, power factor and input current THD) across the entire load range is plotted in Fig. 9.7. In both light load and heavy load conditions, the input current is well in phase with the input voltage; the measured power factor is close to unity across the entire load range, demonstrating the effectiveness of the proposed control scheme. It can be observed from Fig. 9.6a that in high line voltage, light load condition, there is a small phase lead of i_{AC} to v_{AC}. This is due to the current flowing through the input filter capacitor C_{in} [95]. This current is at its largest with high input voltage and its effect is the most noticeable when the current into the converter is small. Nevertheless, the impact of the input capacitor current on the power factor is much smaller in this design compared to most conventional solutions as the a seven-level FCML topology allows for much smaller input filter capacitor. Interested readers can refer to [95] for a comparison.

According to Fig. 9.5 and Fig. 9.6, in light load conditions, current spikes can be easily observed at current zero-crossing as predicted in Fig. 8.4. The input current THD is negatively affected by the spikes but remains well below typical regulatory limits [74]. Similar spikes occur in heavy load conditions as well but the effect on input current THD is negligible. In heavy load conditions, the voltage imbalance of flying capacitors become larger as shown in Fig. 9.5b and Fig. 9.6b but stay bounded well below the transistor voltage rating.

The efficiency of hardware prototype is measured and plotted in Fig. 9.7a. Note that the AC source used in the experiment (112-AMX) has a maximum current limit, so the power of the hardware prototype can only be tested up to 600 W under low line voltage condition and up to 1500 W under high line condition. The efficiency measurement includes the power loss in the output buffer capacitor C_{buf} but does *not* include the power consumed by the cascaded bootstrap circuit and the control circuit, which is about 0.5 W and 1.9 W, respectively. The peak efficiency of 99.07% occurs at about half of the nominal load. With the power stage dimension marked in Fig. 9.1 (i.e., 44.5 mm $\times$ 110.4 mm$\times$ 10.2 mm), the PFC front end

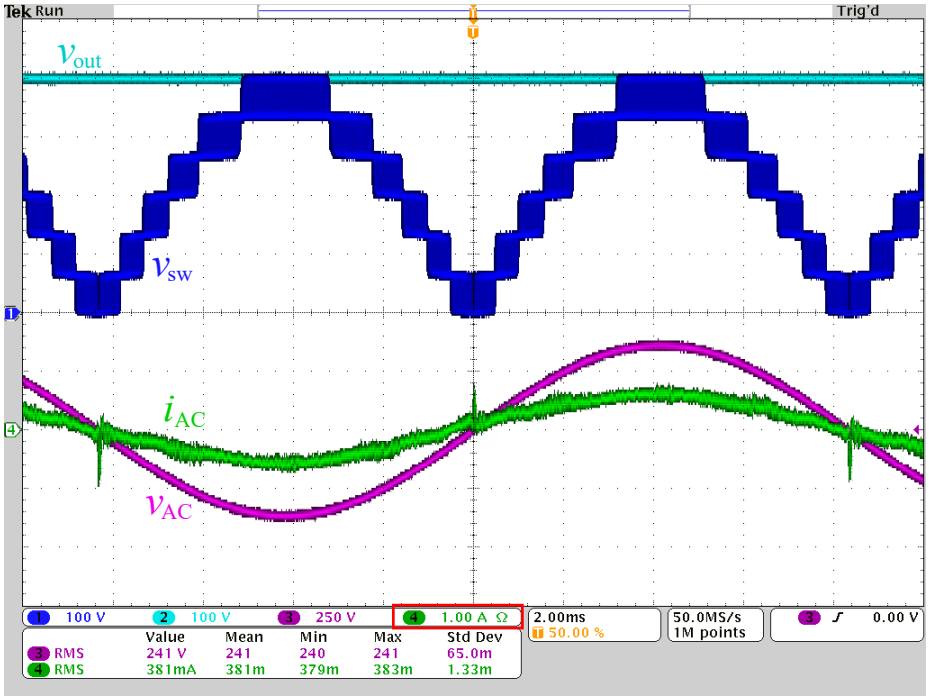


(a) High line voltage (240 V) condition.

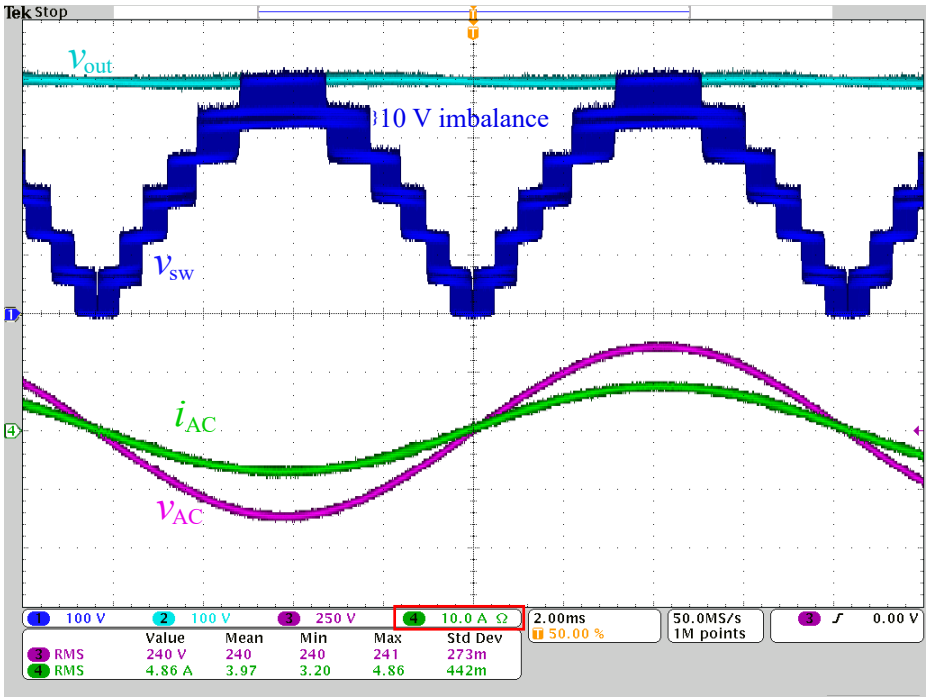


(b) Low line voltage (120 V) condition.

Figure 9.4: Waveforms illustrating the operation of the seven-level FCML converter.

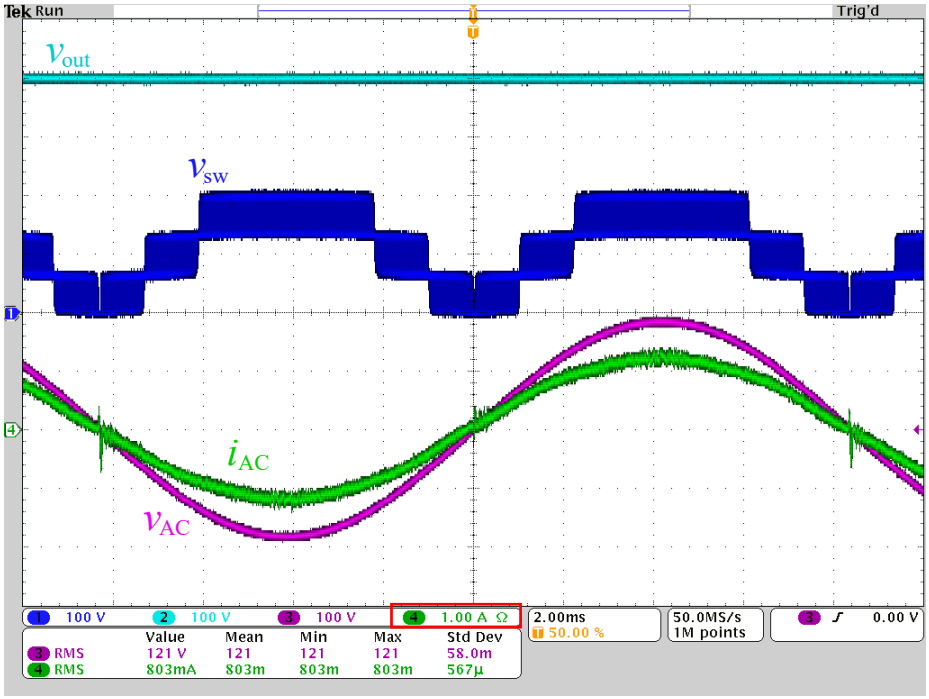


(a) Light load (100 W) operation.

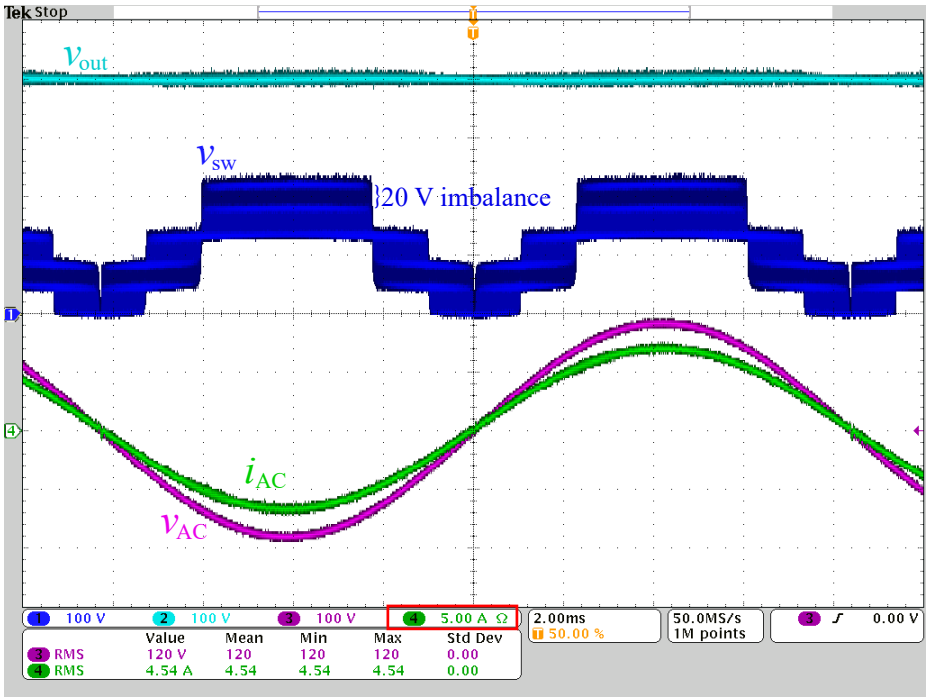


(b) Heavy load (1300 W) operation.

Figure 9.5: Waveforms illustrating the PFC operation under high line voltage (240 V) condition. Note the difference in y-axis scale for the current waveform.

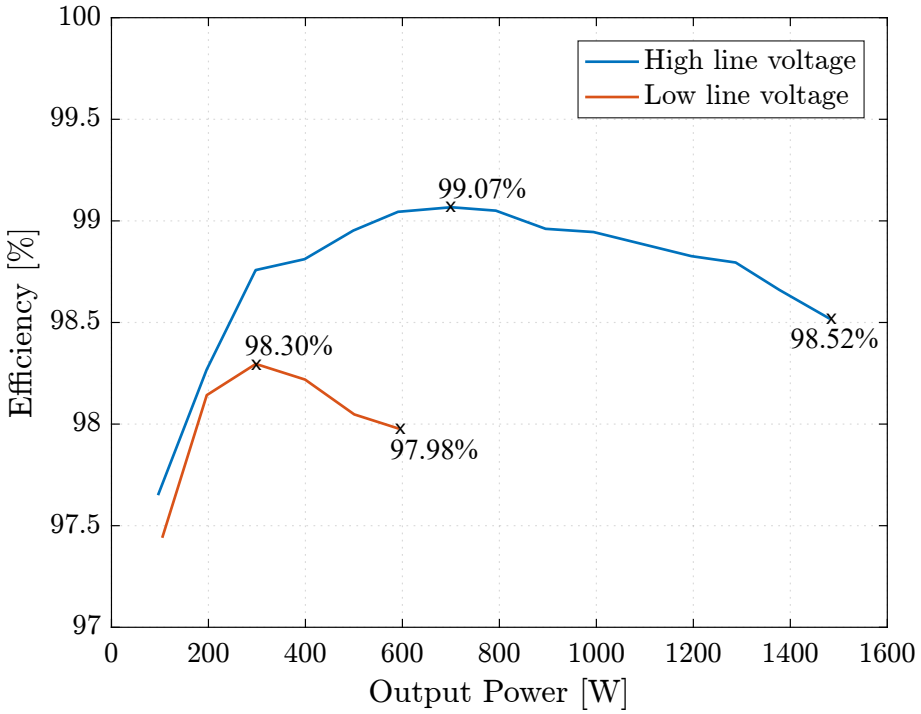


(a) Light load (100 W) operation.

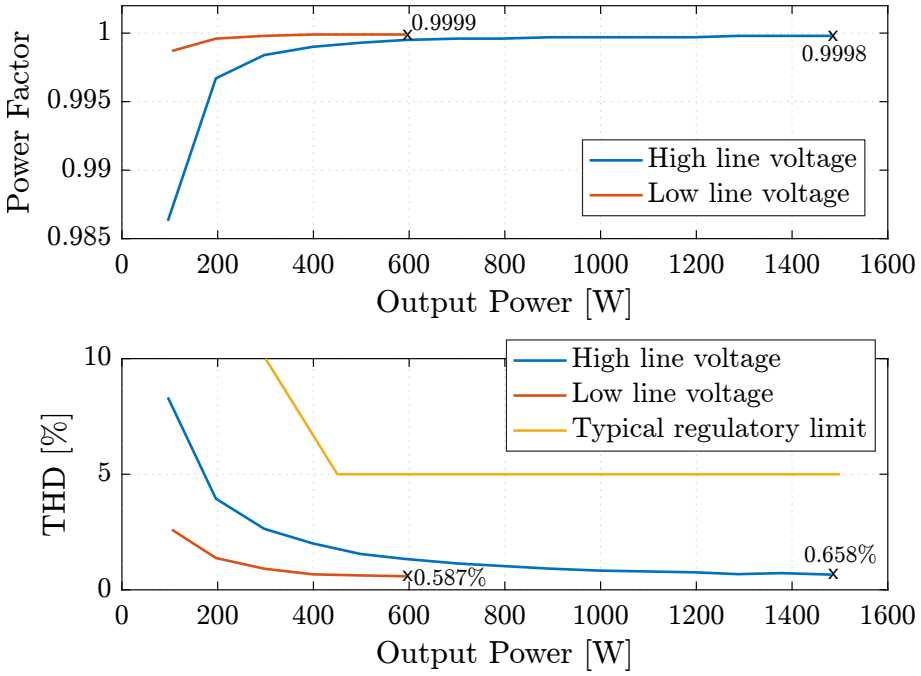


(b) Heavy load (600 W) operation.

Figure 9.6: Waveforms illustrating the PFC operation under low line voltage (120 V) condition. Note the difference in y-axis scale for the current waveform.



(a) Efficiency.



(b) Input power factor and input current THD.

Figure 9.7: Measured performance of the hardware prototype under high line voltage (240 V) and low line voltage (120 V).

achieves 29.9 kW/dm^3 (i.e., 490 W/in^3) power density by rectangular box volume. If we only the consider the volume of components (i.e., assuming an optimal layout and packaging), power density as high as 37.8 kW/dm^3 (i.e., 620 W/in^3) can be expected. The volume of the heatsink is often considered when evaluating the power density as well. However, the large heatsink as shown in Fig. 9.2 is unnecessary given the high efficiency of this converter and a much smaller heatsink would suffice. The current heatsink design unnecessarily degrade the overall power density and we are in the process of improving the heatsink design. Therefore, we consider the whole system with and without heatsink attached separately to allow for a fair comparison to other work.

9.3 Comparison to literature

The experimental efficiency and power density of this work is compared with selected work in the literature and commercial PFC front end products. We make our best effort interpretation of the available information from the literature and the comparison result is compiled in Table 9.2. Although most of these designs target high efficiency as well as high power density, it is difficult to compare them in an absolutely fair manner as they are designed to different specifications. Different works may optimize only the PFC front end or the full system. The EMI filter and output buffer capacitor also may or may not be included in the efficiency and power density calculation, and these components may have different impact on efficiency and power density given different system specifications (e.g., DC output voltage ripple). Therefore, the purpose of Table 9.2 is not to compare the absolute numbers but to provide prospective on the potential efficiency and power density improvements through the FCML approach. The seven-level FCML converter also provides improved power factor and input current THD performance across the load power range compared to most existing solutions. It is hard to summarize them concisely in the table and interested readers can refer to each reference for a detailed comparison.

Table 9.2: Comparison of this work and previous works in the literature

Reference	Topology & Features	Power (W)	Efficiency	Volume ($inch^3$)	Power Density ($W/inch^3$)	Notes
this work	seven-level FCML	1500	full load: 98.52%, peak: 99.07%	by component: 2.01, by rectangular box: 4.88	by component: 620, by rectangular box: 490	*not* including EMI filter, and energy buffer
Liu et al. JESTPE 2016 [74]	interleaved MHz triangular current mode totem-pole bridgeless	1200	full load: 98.7%, peak: 98.8%	by rectangular box: 5.54	by rectangular box: 220	*not* including EMI filter and energy buffer
Vicor GP-MPFC1H21 [108]	N/A	1400	full load: 95%	by rectangular box: 7.2	by rectangular box: 195	*not* including EMI filter and energy buffer
SynQor PFCU390HPx07 [109]	N/A	700	peak and full load: 96%	by rectangular box: 3.7	by rectangular box: 189	*not* including EMI filter and energy buffer
Raggl et al. TIE 2009 [110]	interleaved boost	315	full load: 96.6%	by rectangular box: 3.33	by rectangular box: 95	including EMI filter and energy buffer
Biela et al. IPEC 2010 [111]	triangular current mode totem-pole bridgeless	3000	full load: 98.3%	by rectangular box: 36.5	by rectangular box: 83	including EMI filter and energy buffer
Lange et al. TPELS 2015 [112]	diode-clamped 3-level boost	3000	peak: 98.6%, full load: 97.9%	by rectangular box: 116	by rectangular box: 25.8	including EMI filter and energy buffer

CHAPTER 10

CONCLUSION AND FUTURE WORK

10.1 Summary

This dissertation presents architecture, topology and control for an order-of-magnitude power density improvement in AC-DC converters. A 2 kW single-phase inverter and a 1.5 kW single-phase PFC front end have been successfully demonstrated with such high power density. The entire work boils down to two basic ideas: the series-stacked buffer architecture for twice-line-frequency power pulsation decoupling and the flying capacitor multilevel topology for power conversion between AC and DC.

To summarize the reason why this work achieves these superior features compared to conventional solutions, a few ideas stand out as the key enablers. The first idea is to leverage the high energy density of capacitors over inductors for energy transfer and storage; this idea leads to the structure of the series-stacked buffer (i.e., capacitor through a full-bridge converter to form "active inductor"); this ideas also leads to the use of flying capacitors to tradeoff inductor sizes in the FCML topology, similar to the soft-charging ideas explored in [113–115]. The second idea is that instead of blocking the high DC bus voltage with switches directly, the bulk voltage is blocked by capacitors; for both series-stacked buffer and the FCML converter, such arrangement mitigates the voltage stress on the active circuit, so fast-switching transistors can be employed, which enables the use of switching frequency to tradeoff for energy density. The third idea to that instead of directly processing the full power, the series-stacked buffer architecture controls the full power by actively processing only a fraction of it. By avoiding processing the full power in the first place, the overall system efficiency is no longer limited by the power converter efficiency and a highly efficient system can be built with less efficient converters, similar to ideas explored in [116–119].

10.2 Future work

10.3 Future work for the series-stacked buffer

The goal of this research is to maximize the power density of single-phase AC-DC converter system while maintaining a high efficiency. A good solution toward this goal involves comprehensive consideration on energy storage element property, circuit structure, control method, loss mechanism and thermal management. Through comprehensive review and quantitative comparison, it is determined that the most important factor in this case is the sizing of energy storage element, that is, the balance between capacitor volume and inductor volume. Previous AC-DC converter systems in the literature (for both buffer and inverter/rectifier) do not allow the design to make tradeoffs freely, so these solutions tend to fall on either extreme of the tradeoff, resulting in low power density or poor efficiency.

The series-stacked buffer architecture is different compared to the previous solutions as it allows flexible tradeoff between the capacitor volume and inductor volume. Therefore, further research on this topic should continue to focus on these ideas. The following aspects are therefore proposed for the upcoming work.

First, although the series-stacked buffer presented in this document demonstrate superior performance compared to previous solutions in the literature, it is actually not optimized and still has room for improvement. The current design is based primarily on the convenience to use available components and the form factor to fit with the inverter for the little box challenge design requirement. As shown in Fig. 6.2, the volume of capacitors is much larger than the inductor, suggesting that it might be over the optimal point of the tradeoff. A systematic way to optimize the design requires not only the aforementioned tradeoff but also consideration on the property of the circuit element (especially the specific power density of capacitors and inductors), the power loss and the thermal management. A good modeling of the volumetric impact from these factors and a systematic way to optimize the overall system should be studied in future work.

Second, while he series-stacked buffer architecture achieves significant volume reduction on the inductor through the series connection of the capacitor and buffer converter, the EUR of the capacitors still have room for improvement. A half-bridge buck buffer cell can achieve EUR about 50% or higher for smaller capacitor volume but suffers from large inductor volume. A natural approach to reduce inductor size besides series-stacking is the FCML topology. The high THD of a half-bridge buck buffer cell as analyzed in Section 3.3 is not a severe problem for the FCML topology, because also the multilevel topology can achieve fast

dynamics due to small inductor. The control for the FCML based half-bridge buck buffer will be very similar to the FCML PFC control developed in this dissertation.

Third, while the Google/IEEE little box challenge project [71] demonstrates that the series-stacked buffer and the FCML converter integrates well to form a high-efficiency high power density system, what has not been demonstrated is the grid-connected operation. How the series-stacked buffer affects the dynamics of the FCML converter when designing the feedback loop for the grid-connected operation needs to be further studied and the hardware of the full system (PFC or grid-connected inverter) needs to be demonstrated.

Lastly, the application of the series-stacked buffer is not limited to twice-line-frequency buffering. Due to the high switching frequency of the low voltage transistors in the series-stacked buffer, the control bandwidth of the series-stacked buffer can be quite high. Therefore, it can be modified to use in high-frequency AC micro-grid applications or even in switching ripple filtering for high power, slow switching converters.

10.4 Future work for the FCML PFC

While the FCML PFC prototype in this work demonstrates promising performance, more components and functionality needs to be added or modified to make it a practical system. The opportunity of improvement on the FCML PFC lies in both circuit and control design.

Firstly, although the FCML topology is expected to improve the EMI performance, it has not been demonstrated in hardware. The EMI filter in conventional design tends to degrade the power factor and THD performance of a PFC front end especially in high line condition. It has yet to be shown that an expected smaller EMI filter due to the FCML topology will reduce this degradation.

Second, the balancing issue of FCML topology remains a reliability concern. Although the imbalance of the FCML PFC front end is unbounded and within voltage rating limits in the experiments, it is not guaranteed in all designs. However, voltage balancing is not easy to address. The causes of imbalance have not been fully understood, despite some discussion in the literature. The control method to correct imbalance imposes high requirement on the analog sensing circuitry. Therefore, voltage balancing of FCML converter is a problem that requires in-depth study.

Third, the grid-connected bidirectional operation of the system should be explored. One important application of the AC-DC system presented here is the grid integration of battery storage. A control scheme allowing transition between the operating modes for both the series-stacked buffer and FCML converter needs to be developed.

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