ANALYSIS AND DESIGN OF COMPACT AND EFFICIENT HIGH STEP-UP FLYING CAPACITOR MULTILEVEL CONVERTERS

BY

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THESIS

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ABSTRACT

This thesis explores the possibilities to improve the power density (power to volume ratio) and the efficiency of DC-DC boost converters by using Flying Capacitor Multilevel (FCML) converter topology. DC-DC boost converters are widely used in electrical systems for stepping up the source DC voltage to higher levels. For many applications that are constrained by power consumption and physical space for installation, power converters with high efficiency and power density are preferred. A conventional DC-DC boost converter has many limitations with regard to achieving high power density and efficiency at high voltage gain, such as high switching loss, high voltage stress on main switches and large inductor volume. The FCML converter topology utilizes high energy density capacitors and inductors to store and transfer energy, which brings many inherent properties to overcome many limitations of conventional DC-DC boost converters. This thesis will present the analysis and design process for a FCML boost converter hardware prototype.

To my family and friends, for their love and support.

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CHAPTER 1

INTRODUCTION

In many electrical systems, the source DC voltage needs to be stepped up to higher levels. For example, in a photovoltaic grid-connected power systems [1], the DC voltage generated by the solar panels needs to be stepped up before connecting to the grid-tied inverters. In medical power electronics such as the X-ray power generator [2] and pulse electric field (PEF) related applications [3, 4], a high DC voltage is essential for creating a strong electric field. In such applications, kilovolts output voltage is created from input voltage of hundreds of volts at kilowatt power level.

The conventional boost converter is a basic and common topology for voltage step-up. The inductor stores energy from the source and releases it to the load under different configurations defined by the states of the two switches in the circuit, so the boost converter is categorized as a switched-inductor converter. Since the inductor is the only component for energy storage and transfer, and the energy density (stored energy over volume ratio) of inductors is relatively low, the physical volume tends to dominate the total converter size at high power levels and conversion ratios. The switches will also need to block full output voltage. Since the switches are usually implemented with semiconductor switches such as MOSFETs, larger device size is usually required to withstand higher blocking voltages. The device will then have higher on-resistance and parasitic capacitance, which will increase conduction loss and switching loss, respectively.

Many efforts have been made to overcome such limitations in the conventional boost converter. In [5], techniques to build high step-up converters with higher efficiency and smaller size are reviewed. Many techniques, even though managing to solve particular problems, brought trade-offs with other aspects of the converter design, resulting in marginal improvements on the overall size and efficiency. For example, one can cascade two boost converters to achieve higher gain and reduce voltage stress on individual stages. However, the combined size of the converter is usually much larger, and the losses of two stages sometimes add up to a higher value [6–8]. Increasing the switching frequency in boost converters will reduce the required transferred energy by the inductor, thus smaller inductors can be used, but the switching loss will increase as a trade-off.

The switched-capacitor (SC) converter is another type of converter that can achieve large step-up ratios. It utilizes the high energy density of capacitors to transfer energy, resulting in much higher power density than conventional inductive DC-DC buck or boost converters. However, SC converters have their own issues such as charge redistribution loss and no ability for output load regulation [9], therefore their usage is mainly in low power applications.

Hybrid inductive/capacitive converters are a combination of SC converters and conventional switched-inductor converters. They can achieve high power density by utilizing the high energy density of capacitors, while still allowing load regulation, and the charge redistribution loss in SC converters can also be eliminated by the extra inductors [7, 10, 11]. Intermediate voltage levels can be created by switching the capacitors in different configurations, thus some hybrid converters are also referred to as multilevel converters. The multilevel design allows lower voltage rating switching devices to be used for high voltage applications. Among the multilevel and hybrid converter topologies, the flying-capacitor multilevel (FCML) converter topology can be constructed using low voltage switches and smaller passive devices to achieve high power density and efficiency [12, 13].

This thesis explores the use of the FCML converter in a large voltage step-up operation. A 100 V to 1000 V, 820 W hardware prototype is implemented with GaN switches and high energy density ceramic capacitors as a proof of concept.

CHAPTER 2

CONVENTIONAL BOOST CONVERTERS

A basic boost DC-DC converter is shown in Fig. 2.1. Two switches allow the converter to operate in two states over one switching cycle. In state 1, as shown in Fig. 2.2a, S_1 is open and S_2 is closed. The voltage across the inductor is V_{in}, and the inductor current is ramping up with the rate that can be decided by Eq. (2.1). In state 2, as shown in Fig. 2.2b, S_2 is open and S_1 is closed, and the voltage across the inductor is (V_{in} - V_{out}), which is negative in a boost converter. Such negative voltage causes the inductor current to ramp down according to Eq. (2.1). The voltage across the inductor and the resultant current waveform is shown in Fig. 2.3. In the steady state, the inductor should not have any net change in stored energy over one switching period, so the flux linkage in one switching period on the inductor, defined by Eq. (2.2), should equal to zero. Moreover, the average inductor current should equal to the input current as denoted in Fig. 2.3. As we defined the duty ratio D to be the portion in one period that the circuit is in state 1, the relation between input and output voltage as in Eq. (2.3) can be obtained.

$$V_l = L\frac{di}{dt} \tag{2.1}$$

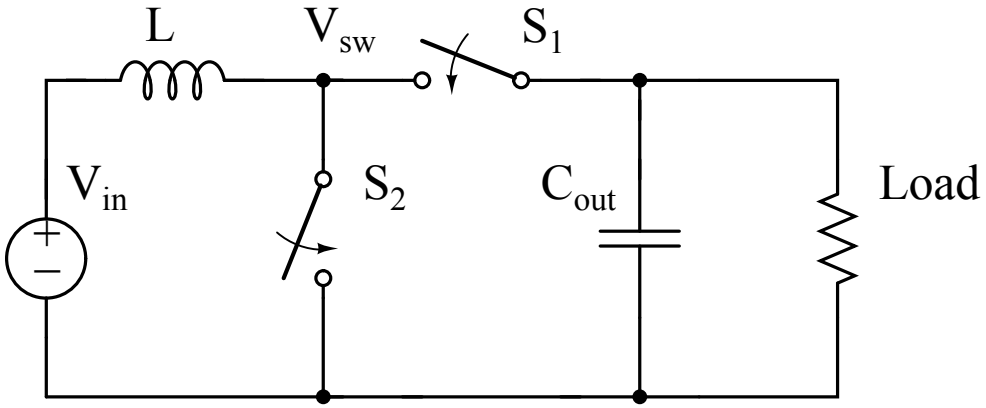
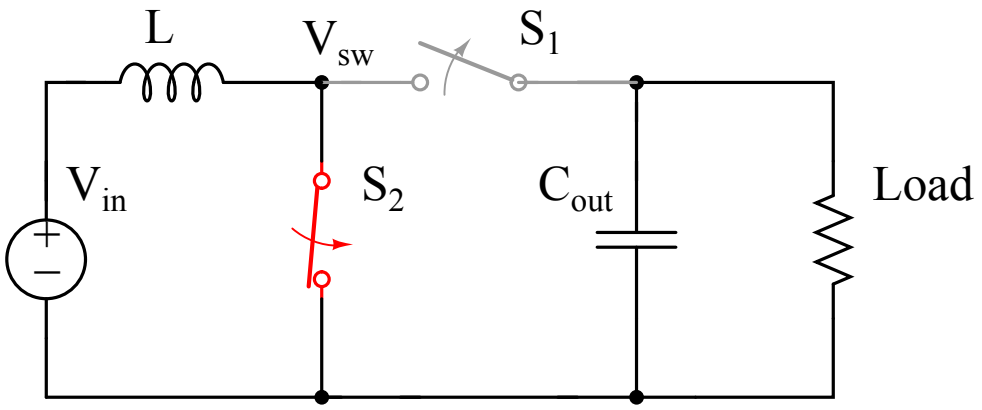
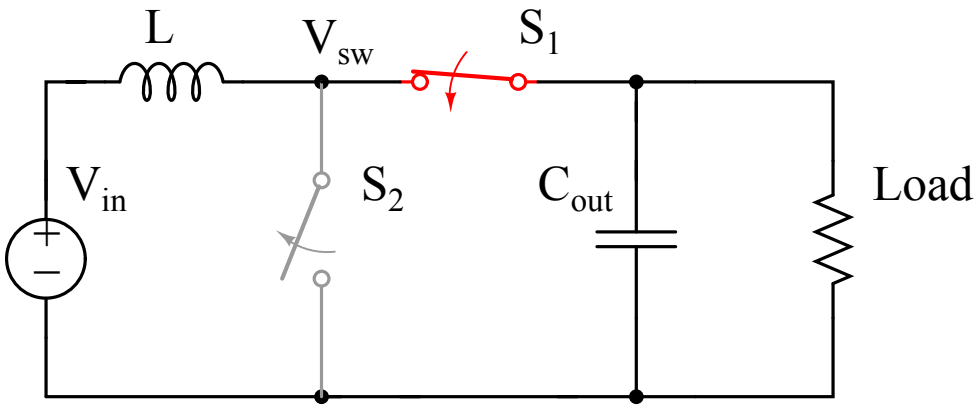


Figure 2.1: Schematic of a convention boost converter.



(a) State 1



(b) State 2

Figure 2.2: Switching states in a boost converter.

$$\lambda = \int_0^T V_l dt = 0 \tag{2.2}$$

$$V_{\text{out}} = \frac{V_{\text{in}}}{1 - D} \tag{2.3}$$

It can be seen from the circuit diagrams in state 1 and state 2 that both switches S_1 and S_2 have to block voltage of V_{out} when they are off and carry peak current of I_{in} when they are on. For the high step-up scenario, where $V_{\text{out}} >> V_{\text{in}}$, higher voltage rating switching devices are needed in the converter given a fixed V_{in}. However, higher voltage rating semiconductor switches such as MOSFETs often come with larger on-resistance and larger parasitic capacitance. Larger on-resistance brings higher conduction loss, and larger parasitic capacitance slows down the switching transition as it takes longer to charge and discharge the input capacitance of the MOSFETs, which will increase the overlap switching loss. To a certain

voltage level, the availability of suitable switching devices on the market will become another implementation issue.

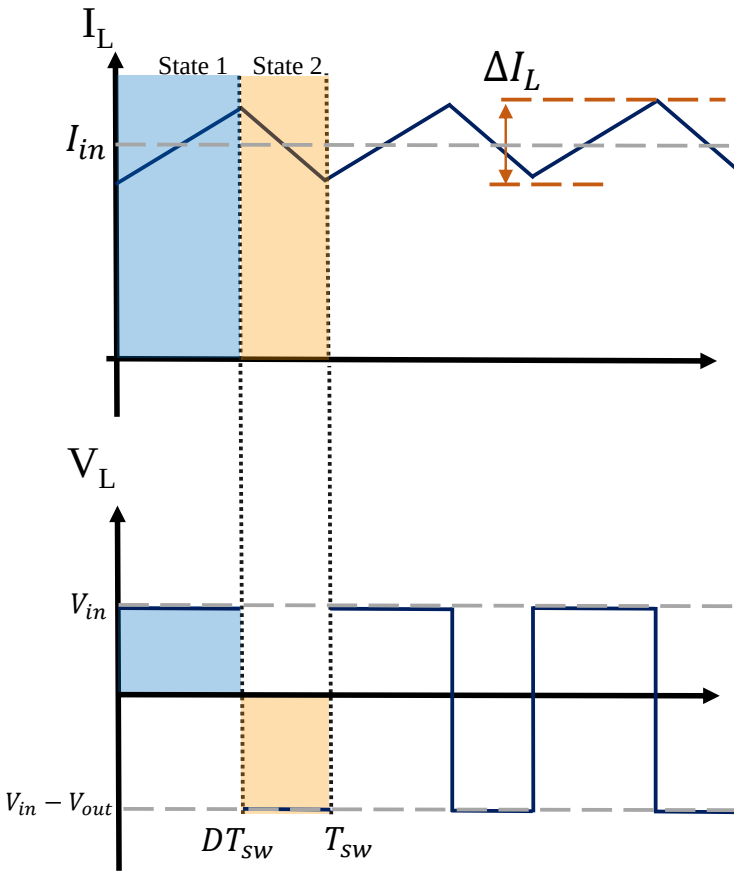


Figure 2.3: Inductor voltage and current in a convention boost converter.

Another major obstacle for a conventional boost converter to improve power density is the large size of magnetic components. This is fundamentally due to the low energy density of inductors. The inductance in a boost converter can be derived from Eq. (2.1) to be

$$L_{\text{Boost}} = \frac{DV_{\text{in}}}{\Delta I_L f_{\text{sw}}} \tag{2.4}$$

where ΔI_{L} is the current ripple on the inductor and f_{sw} is the switching frequency.

The energy stored in a inductor is defined as

$$E_{\text{L}} = \frac{1}{2} L i^2 \tag{2.5}$$

The peak energy stored in the inductor then can be obtained:

$$E_{\text{peak}} = \frac{DP_{\text{in}}}{2f_{\text{sw}}}(1 + \frac{1}{\alpha} + \frac{\alpha}{4}), \alpha \in (0, 2] \tag{2.6}$$

where α is the ratio between current ripple and average input current. Since we are only analyzing continuous-conduction mode (CCM) boost converters, the largest value of α is 2. In state 1, the energy delivered from the source to the inductor can be calculated by multiplying the input power and the corresponding time length to be

$$E_{\text{transfer}} = \frac{DP_{\text{in}}}{f_{\text{sw}}} \tag{2.7}$$

This energy is reflected in the inductor current ripple, as the current changes from $(I_{\text{in}} - \frac{\Delta I}{2})$ to $(I_{\text{in}} + \frac{\Delta I}{2})$ in Fig. 2.3. Then we can rewrite Eq. (2.6) to be

$$E_{\text{peak}} = \frac{E_{\text{transfer}}}{2}(1 + \frac{1}{\alpha} + \frac{\alpha}{4}) \tag{2.8}$$

We often use the term $\frac{E_{\text{transfer}}}{E_{\text{peak}}}$ to describe the energy utilization rate of the inductor. When the ripple is the largest as $\alpha = 2$, the energy utilization rate is 1, which means the inductor only stores the energy it needs to transfer from the source to the load in one switching period.

In a boost converter, E_{peak} should never exceed the maximum energy an inductor can store, otherwise the inductor will saturate. For a given core material, the maximum energy an inductor can store is given by

$$E_{\text{max}} = \frac{{B_{\text{sat}}}^2}{2\mu} V_{\text{Volume}} \tag{2.9}$$

where B_{sat} and μ are the saturation flux density and permeability of the inductor core. Given this constraint, it can be concluded that the size of the inductor is proportional to the peak stored energy for a given core material. From Eq. (2.6) and Eq. (2.3), it can be seen that in order to generate higher DC voltage with the same input voltage and power, a higher duty ratio is needed, resulting in higher peak stored energy in the inductor given that the current ripple and switching frequency remain constant. Equation (2.6) suggests that in order to shrink the volume of the inductor, one can decrease the required peak stored energy by either increasing the switching frequency or allowing larger inductor current ripple (increasing α). In other words, one can lower E_{transfer} by switching the converter faster, or increase α to increase the energy utilization rate of the inductor. Since there is a certain

amount of energy loss during every switching transition, increasing the switching frequency will increase such power loss. Larger inductor current ripple will cause higher Root-Mean-Square (RMS) conduction loss on the inductor windings as well as on the switches and other parasitic resistance in the converter circuit. Sometimes thicker winding is used to withstand the high current in the inductor, resulting in even larger physical size of the inductor than the ones with lower inductance. Large current ripple also means large flux swing, which leads to higher core loss per volume in the core.

To conclude, in a boost converter, one can reduce the peak stored energy in the inductor by decreasing E_{transfer} or allowing larger current ripple for higher energy utilization rate. However, both methods will sacrifice converter efficiency. This limitation motivates research efforts to reduce the peak stored energy in the inductor with little trade-off or even improvement on the efficiency to achieve good balance between passive component size and converter efficiency.

CHAPTER 3

FLYING CAPACITOR MULTILEVEL CONVERTERS

3.1 Overview

The concept of FCML converters was first introduced in [14]. There are many types of multilevel converters such as FCML, Modular Multilevel Converter (MMC), Neutral-Point Clamp Converter and others [15]. Multilevel designs were first investigated for building inverters with higher rated voltage and lower THD. In general, multilevel converters create intermediate voltage levels during the operation such that lower voltage rating switching devices can be used for high voltage applications, where higher voltage rating switching devices were not available given certain converter topologies. For example, a four-level multilevel converter was built with the highest rating IGBTs available at that time for a 4.5 MW motor drive [16]. The intermediate voltage levels also lower the THD of the output waveform if the converter is operating as an inverter [15].

Recently, the FCML converter is also studied as a type of hybrid DC-DC converters, in which both inductors and capacitors store and transfer energy during the conversion process. The capacitors share the energy storage requirements with the inductor such that the peak stored energy in the inductor is reduced. The FCML converter is shown to have abilities to achieve high power density and high efficiency in medium voltage and power applications thanks to the latest development of high energy density and low loss ceramic capacitors [12, 13]. The energy density of a component is defined as the energy stored in the component divided by the physical volume. The energy stored in a capacitor is given by

$$E_{\mathrm{C}} = \frac{1}{2} C v^2 \tag{3.1}$$

The energy stored by the inductor is given in Eq. (2.5)

The survey in [13, 17] showed that modern ceramic capacitors have achieved an energy density on average 100 times higher than the inductors, as plotted in Fig. 3.1. This fundamental characteristic guarantees the research effort to build high power density converters

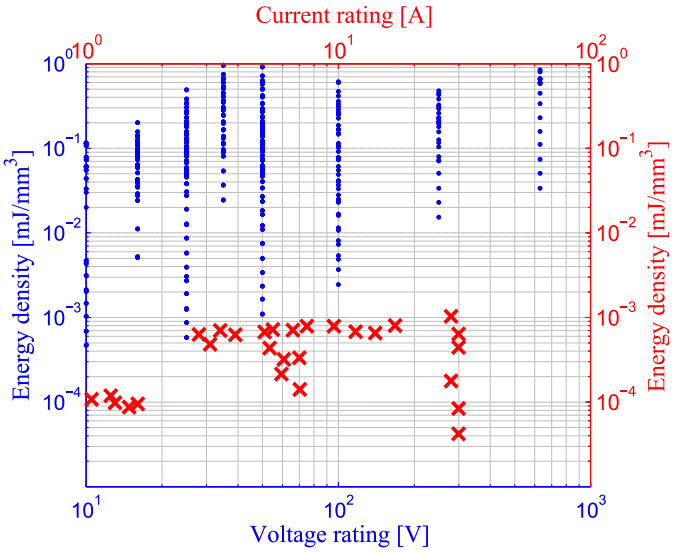


Figure 3.1: The energy density of selected capacitors from TDK (blue) and selected inductors from Coilcraft (red) in [17].

with the FCML topology.

3.2 Principle of operation

The FCML converter is built up with single switching cells as shown in Fig. 3.2. A single switching cell contains two switches and a flying capacitor. An N-level FCML will have $(N-2)$ flying capacitors and $2(N-1)$ switches. The switches are controlled with phase shifted pulse width modulation (PSPWM) [14, 15]. Each switch is controlled by a pulse width modulation (PWM) signal with a duty ratio of D, and is phase-shifted by $\frac{360^\circ}{N-1}$ from the adjacent PWM signals.

In the steady state, the N-level FCML boost converter naturally balances the voltages across $(N-2)$ flying capacitors, each of which holds voltage of $\frac{V_{\text{out}}}{N-1}$, $\frac{2V_{\text{out}}}{N-1}$, ..., $\frac{(N-2)V_{\text{out}}}{N-1}$ [14]. For example, in the seven-level FCML converter shown in Fig. 3.3, C_1 has a voltage of $\frac{V_{\text{out}}}{6}$, C_2 has a voltage of $\frac{2V_{\text{out}}}{6}$, etc.

Example PWM switching patterns of the converter are illustrated in Fig. 3.4 with a duty ratio of 0.9 and 60° phase shift for a seven-level FCML converter. To understand the energy transfer process among capacitors, let us start with the shaded time frames in Fig. 3.4 and Fig. 3.5 and the corresponding circuit states with the current flow paths indicated in Fig. 3.6. During the time frame (a), S_1 is open while the rest of the switches remain closed,

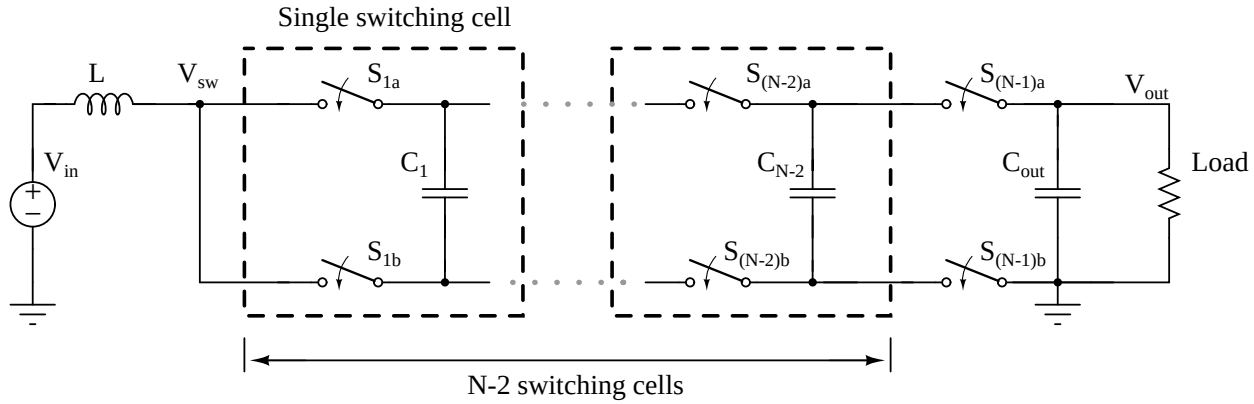


Figure 3.2: Schematic of a N-level FCML boost converter.

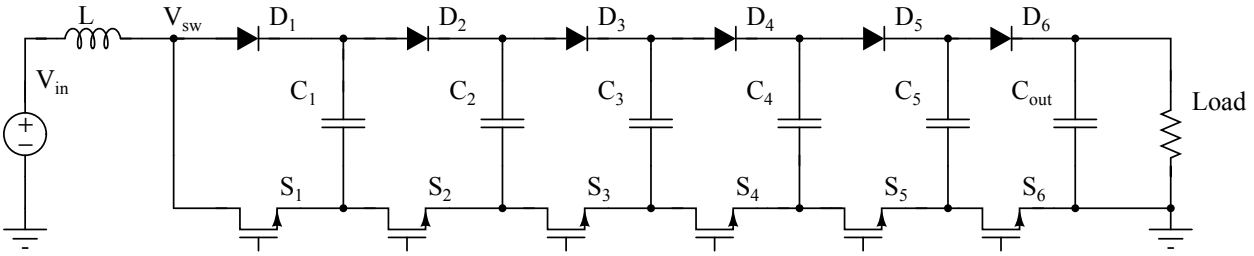


Figure 3.3: Schematic of a seven-level FCML boost converter.

and the switching node labeled V_{sw} in Fig. 3.3 will connect to C_1 and to the ground so the inductor current is charging C_1 as shown in Fig. 3.6a. The voltage on C_1 starts to rise as shown in Fig. 3.5 (in this plot, voltages of C_1 and C_2 are normalized by $\frac{V_{\texttt{out}}}{6}$). The voltage ripple $\Delta V_{C_{\texttt{fly}}}$ on C_1 can be calculated by Eq. (3.2). At the end of the shaded area (a), the maximum voltage stress is seen by the switch S_1 as shown in Eq. (3.3). In shaded area (b), S_2 is off while the rest of the switches remain closed as shown in Fig. 3.6b. The switching node voltage V_{sw} equals to the voltage of C_2 minus the voltage of C_1, so the switching node voltage is $\frac{V_{\texttt{out}}}{6} - \Delta V_{C_{\texttt{fly}}}$. At the end of the shaded area (b) in Fig. 3.5, C_1 is discharged back to the nominal voltage $\frac{V_{\texttt{out}}}{6}$, and the voltage of C_2 rises by $\Delta V_{C_{\texttt{fly}}}$, while the switching node voltage rises to $\frac{V_{\texttt{out}}}{6} + \Delta V_{C_{\texttt{fly}}}$.

$$\Delta V_{C_{\texttt{fly}}} = \frac{I_{\texttt{in}} T_{\texttt{FCML}} (1 - D)}{C_{\texttt{fly}}} \tag{3.2}$$

$$V_{switch} = \frac{V_{\texttt{out}}}{N - 1} + \Delta V_{C_{\texttt{fly}}} \tag{3.3}$$

This charging and discharging process continues among adjacent flying capacitors, utilizing both the inductor and capacitors to transfer energy to the load. It also creates the frequency

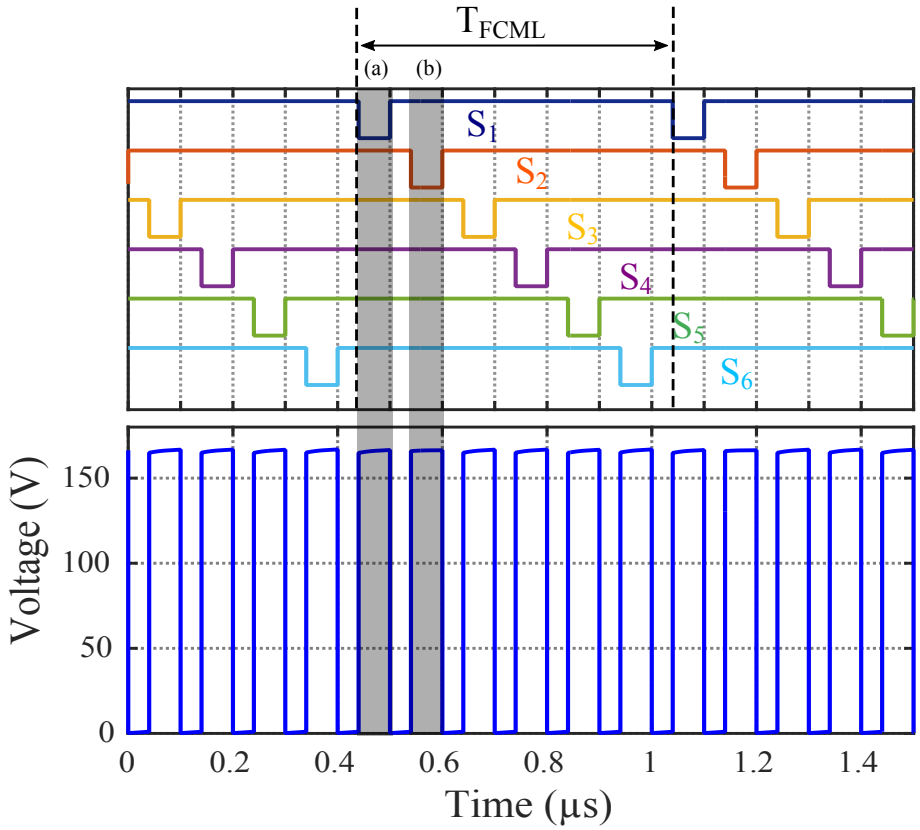


Figure 3.4: Example PSPWM signals with duty ratio of 0.9 (top) and the corresponding switching node voltage (bottom).

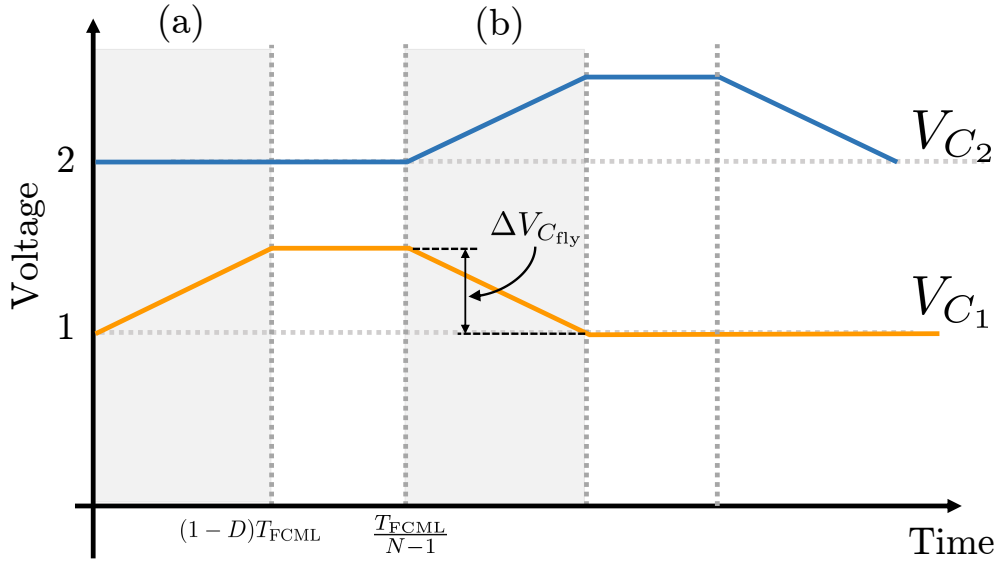


Figure 3.5: C_1 and C_2 voltage waveforms (voltages are normalized by $\frac{V_{\text{out}}}{6}$).

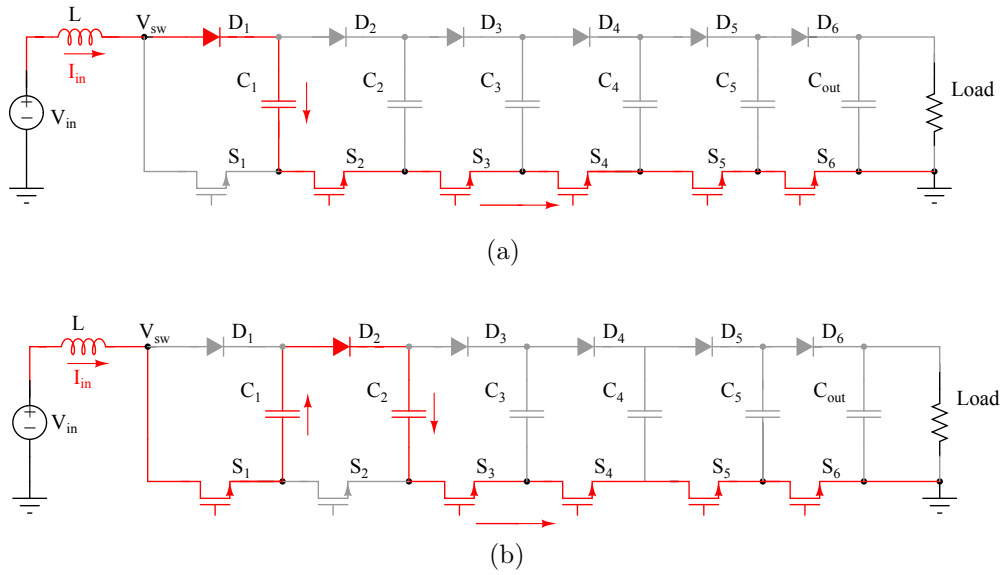


Figure 3.6: Current path when S_1 is open (top) and S_2 is open (bottom).

multiplication effect on the inductor in the FCML converter. Figure 3.4 shows PSPWM signals on the top and resultant switching node voltage V_{sw} with 100 V input voltage on the bottom. Provided that the flying capacitor voltages are balanced, the switching node in Fig. 3.3 is switched between 0 V and $\frac{V_{\text{out}}}{N-1}$ given a duty ratio greater than $\frac{N-2}{N-1}$, and it stays at $\frac{V_{\text{out}}}{N-1}$ for $(1-D)T_{\text{FCML}}$ of the time, and it has a frequency that is $(N-1)$ times (six times in this case) of the switching frequency of any individual switch. The switching period of individual switches is denoted as T_{FCML} as illustrated in Fig. 3.4. The frequency multiplication effect on the inductor in FCML converter reduces the inductance compared to conventional, two-level converters. This was quantitatively analyzed in [18], which also included the volume of the added capacitors to provide a comprehensive converter size comparison. The equation for calculating the output inductance of FCML buck converters is also given in [18]. By exchanging the output and input voltage terms, the equation for the input inductance of FCML boost converter can be written as Eq. (3.4).

$$L_{\text{FCML}} = \frac{V_{\text{in}} - (1-D)(N-1)V_{\text{in}}}{\Delta I_L f_{\text{FCML}}(N-1)} \tag{3.4}$$

$$V_{\text{out}} = \frac{V_{\text{in}}}{1-D} \tag{3.5}$$

$$L \times f_{\text{FCML}} \geqslant 0.5(1-D)^2(D - \frac{N-2}{N-1})R_{\text{out}}, D \geqslant \frac{N-2}{N-1} \tag{3.6}$$

Applying volt-second balance condition on the inductor L, the overall voltage conversion

ratio of the FCML boost converter in CCM can be simplified to Eq. (3.5). Notice that this voltage conversion relation is the same as a regular boost converter. Since the ratio between the current ripple and the average input current α has to be less than or equal to two for CCM operation, condition in Eq. (3.6) is derived from Eq. (3.4). If such condition is not met, the converter will operate in discontinuous-conduction mode (DCM), where the conversion ratio will be different.

3.3 Sizing the passive components in FCML converters

By going through similar calculation as for a conventional boost converter in Chapter 2, peak stored energy in the inductor in FCML converters with duty ratio higher than $\frac{N-2}{N-1}$ can be expressed as

$$E_{\text{peak, FCML}} = \frac{(1-(1-D)(N-1))P_{\text{in}}}{2f_{\text{FCML}}(N-1)}(1+\frac{1}{\alpha}+\frac{\alpha}{4}), D \geqslant \frac{N-2}{N-1} \tag{3.7}$$

Similarly, we can find the energy that is delivered from the source to the inductor

$$E_{\text{transfer, FCML}} = \frac{(1-(1-D)(N-1))P_{\text{in}}}{f_{\text{FCML}}(N-1)} \tag{3.8}$$

Notice that if $N = 2$, Eq. (3.7) can be simplified to Eq. (2.6). This shows that the conventional boost converter can be viewed as a two-level FCML converter. Inserting $N = 7$ for the proposed converter and $N = 2$ for a conventional boost converter into Eq. (3.7), the inductor size of the FCML converter is calculated to be 13.5 times smaller than that of the conventional boost converter, given the same input power, conversion ratio and current ripple requirements.

Comparing the construction of Eq. (2.7) and Eq. (3.8), the reduction of the transfer energy in the inductor can be seen as the result of two effects. The first one is the change of equivalent duty ratio of the switching node voltage. In Eq. (2.6), the duty ratio of the switching node voltage is the same as the duty ratio D of switching PWM signals. In Eq. (3.7), the effective duty ratio seen by the inductor is reduced to $(1-(1-D)(N-1))$. The second effect is the frequency multiplication as discussed earlier that the effective frequency at the switching node is $f_{\text{FCML}}(N-1)$. An intuitive way to understand is that for a certain power level, the passive components in the converter need to deliver a certain amount of energy to the load in one switching period. In a boost converter, the inductor stores energy from the source in state 1 and releases the stored energy to the load in state 2. And this energy is defined as E_{transfer} from Chapter 2. If the frequency is increased by $(N-1)$ times

in a conventional boost converter, the inductor only needs to store and deliver $\frac{1}{N-1}$ of the original E_{transfer} as the period is $\frac{1}{N-1}$ of the original period. Now in FCML converters, E_{transfer} is lowered not only because the frequency seen by the inductor is higher, but also because of the help from capacitors to store and transfer energy with the voltage ripple on the capacitors as plotted in Fig. 3.5, the E_{transfer} on the inductor can be further reduced than that resulted from increasing the switching frequency by $(N-1)$ times.

With more levels in an FCML converter, more flying capacitors and gate driving and level-shifting circuits are needed. However, because of the high energy density of ceramic capacitors, the total passive component volume will still decrease with increasing number of levels despite the added flying capacitors' volume [18]. The gate driving and level-shifting circuits are usually low-profile and their sizes are negligible compared to the passive components.

CHAPTER 4

HARDWARE IMPLEMENTATION

A seven-level FCML boost converter prototype with specifications shown in Table 4.1 has been built to demonstrate the potential of FCML converters to achieve high power density and efficiency for high step-up conversion applications.

Table 4.1: Specifications of the seven-level FCML boost converter prototype.

Rated power	820 W
Input voltage	100 V
Maximum output voltage	1 kV
Switching frequency	72 kHz

Figure 3.3 shows the schematic of the seven-level converter and Fig. 4.1 shows the hardware prototype. Just like in a conventional boost converter, the high-side switches can be realized with diodes, and the low-side switches need to be active switches. Thanks to the reduced voltage rating requirement, 200 V GaN switches and diodes are used, which allows lower transistor $R_{\text{ds, on}}$ and low diode forward voltage drop, respectively. Moreover, compared to high voltage MOSFET or SiC switches, lower voltage rating GaN switches reduce switching loss because of the smaller output and gate charge. The use of diodes instead of GaN transistors for the top-six switches in Fig. 3.3 is deliberate. This is because at the high duty ratio of 0.9, the diode only conducts for one-tenth of a switching period. Thus, while the diodes are generally less efficient than the GaN switches (owing to the relatively large conduction loss from their forward voltage drop), the power processed by the diodes is far smaller. By using diodes for the top switches, the circuitry required to drive an active switch in an FCML converter (such as gate drivers, signal and power level-shifters) are saved, thus there is considerable saving in Printed Circuit Board (PCB) size and component cost while the penalty in efficiency due to the forward voltage drop conduction loss of the diodes is minimal, for the high step-up scenario considered here.

The top, side and bottom views of the prototype converter are shown in Fig. 4.1, with key components annotated and a U.S. quarter for size comparison. The flying capacitors and inductors are placed on the bottom side of the PCB. GaN switches and diodes are

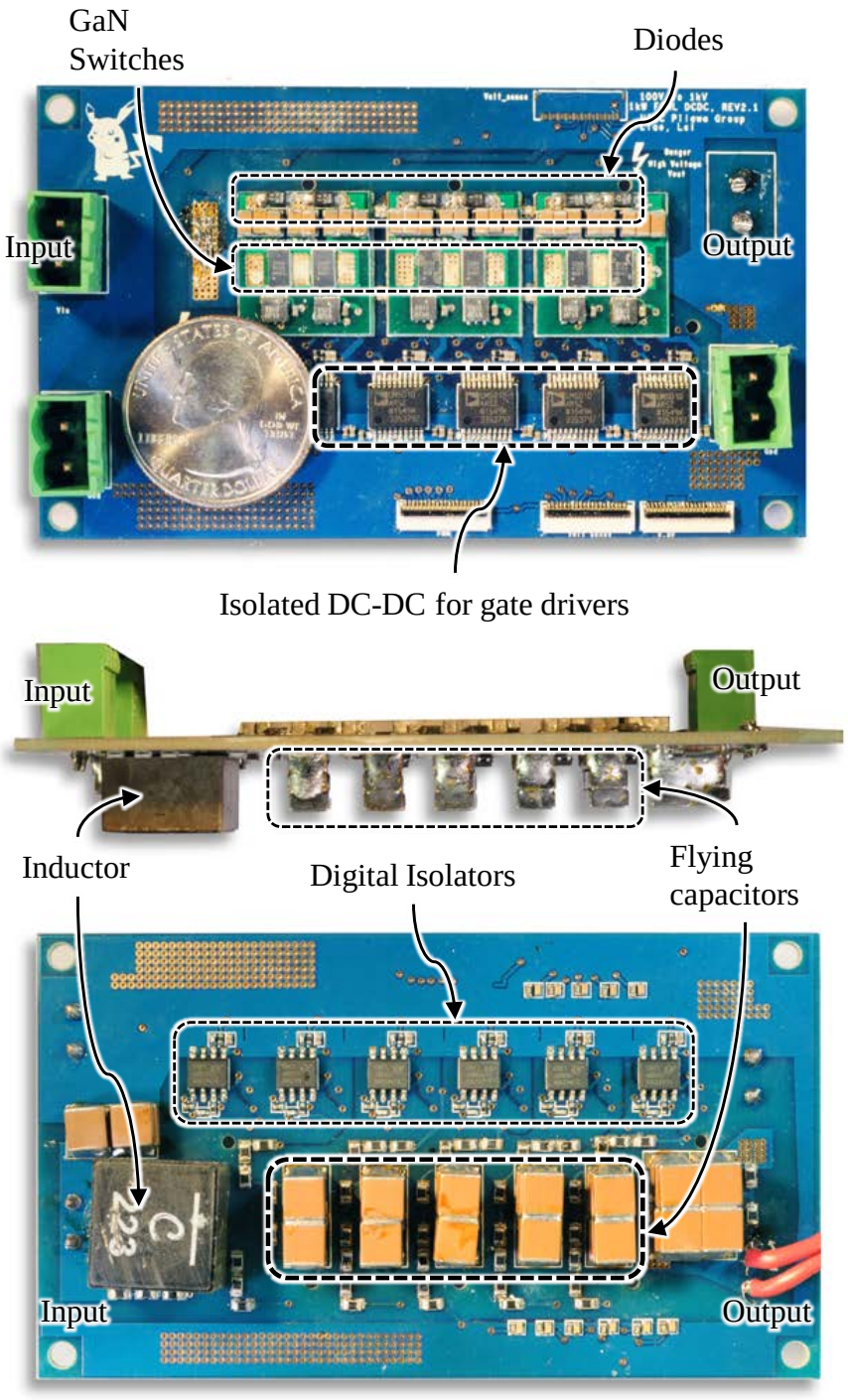


Figure 4.1: Annotated photographs of the prototype PCB with U.S. quarter.

Table 4.2: Component list of the converter PCB.

Component	Part number	Parameters
GaN switches (S_1 to S_6)	EPC 2034	200 V, 31 A, 10 mΩ
GaN gate driver	Texas Instruments LM5114	
Diodes (D_1 to D_6)	Vishay VS2EFH02	200 V, 2A
Flying capacitors ($C_1 - C_5$)	TDK C5750X6S2W225K250KA $\times$6	2.2 μF, 450 V
Inductor	Coilcraft XAL1510-223	22 μH
Digital isolators	Silicon Labs Si8423BB-D-IS	
Power isolators	Analog Devices ADUM5210	

placed on a custom switching cell (shown in green) that incorporates two gate drivers and local decoupling capacitors to minimize ringing at switch transitions. The dimension of the rectangular cuboid enclosure that only contains switches and passive components is 3.3 in $\times$ 0.67 in $\times$ 0.54 in, which is used to calculate the power stage power density. The dimension of the rectangular cuboid which includes the power stage and all the level shifting circuits is 3.3 in $\times$ 1.4 in $\times$ 0.54 in (L $\times$ W $\times$ H), which is used to calculate the converter's overall power density. A complete component list is given in Table 4.2.

4.1 Switching cells

A detailed schematic and PCB of the switching cell are presented in Fig. 4.2. Since the source node of each GaN FET is floating, the PSPWM signals from the microcontroller unit (MCU) need to be isolated. Figure 4.3 shows the complete gate driving power and signal isolation circuit. The 5 V grounded power is shifted with the on-chip isolated DC-DC converters ADUM5210 as denoted in Fig. 4.1. The PSPWM signals are isolated with RF-based signal isolator Si8423BB-D-IS on the bottom side of the main PCB. This circuit ensures the complete isolation between low voltage low power control circuit (MCU and 5 V control power etc.) and the main power stage. Techniques in [19] to generate floating gate driving power supply voltages can further shrink the PCB area needed for the level-shifting circuits as well as improve the efficiency by eliminating the relatively lossy isolated DC-DC converters. For testing the converter in this thesis, the gate driving power was supplied by an external power source. However, such external power source can be replaced with the voltages from the flying capacitors themselves by carefully controlling the start-up sequence and flying capacitor voltages [20].

The gate drivers, gate resistors, GaN switches and diodes are laid out in a compact fashion on the switching cell PCB to minimize the commutation loop and the gate driving loop to

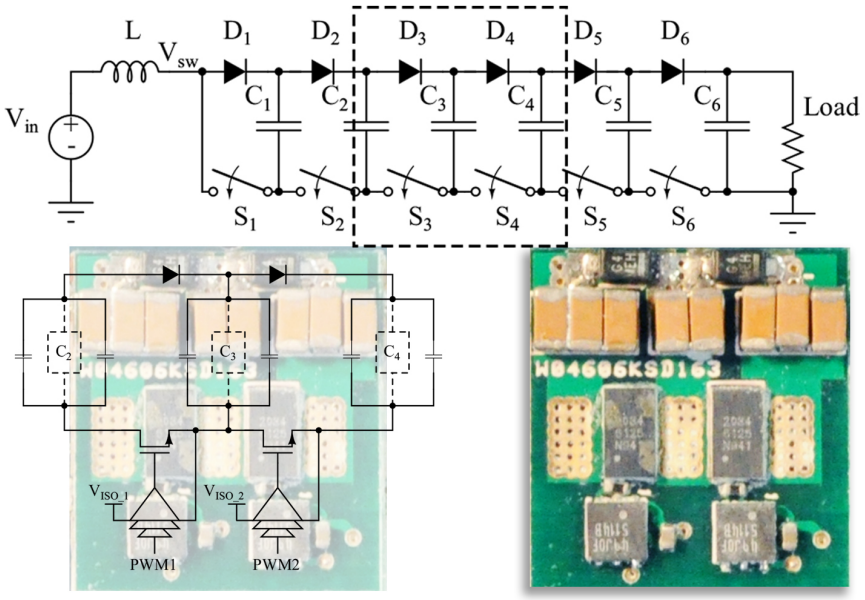


Figure 4.2: Switching cell schematic and PCB.

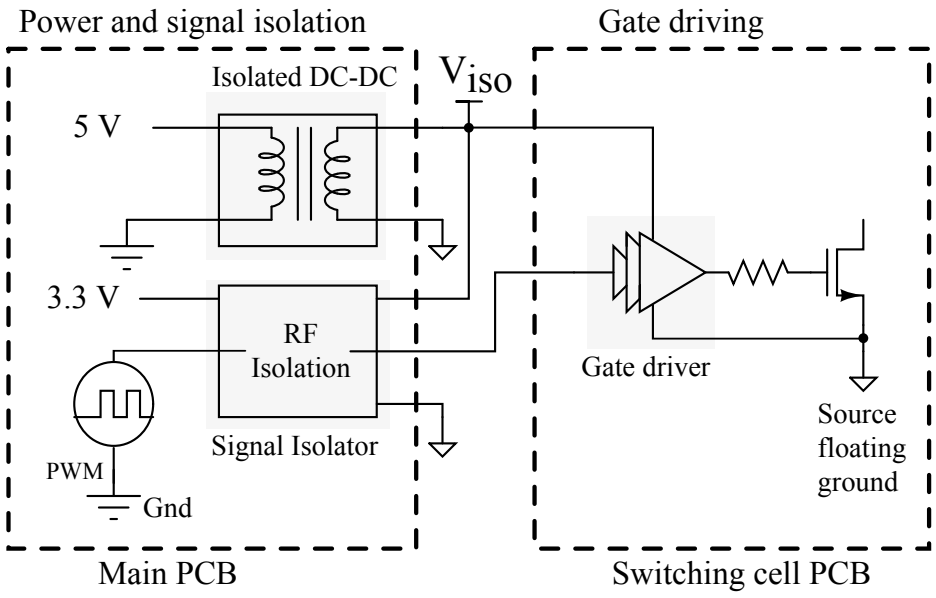


Figure 4.3: Gate driving power and signal isolation circuits for each GaN FET.

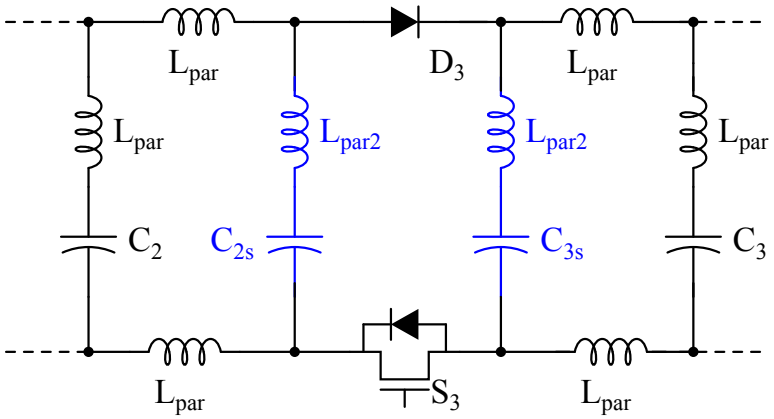


Figure 4.4: Commutation loop schematic and added decoupling paths (blue).

reduce the inductance in the PCB traces. Methods to further reduce the loop inductance such as placing additional decoupling capacitors and different layout techniques are discussed in [12, 21]. The schematic in Fig. 4.4 shows the decoupling concept. C_2 and C_3 are the flying capacitors as shown in Fig. 4.1, and C_{2s} and C_{3s} are the small decoupling capacitors on the switching cell PCB in Fig. 4.2. During switching transitions, the commutation loop can be seen as a series RLC circuit experiencing step changes of voltages. The overshoot of the step response is decided by the quality factor of the series RLC circuit as

$$Q = \frac{\sqrt{\frac{L}{C}}}{R} \tag{4.1}$$

The higher the Q, the higher the overshoot. By adding parallel decoupling paths, the effective L in the loop is smaller and the C is bigger such that Q is lower. The same analysis can be done for the gate driving loop. The gate driving loop is the loop from the output of the gate driver to the gate of the GaN FET, then returning from the source of the FET to the gate driver as shown on the right of Fig. 4.3. GaN FET has a gate capacitance that is a magnitude lower than MOSFET counterparts. Smaller C will make the Q in the circuit larger. In order to reduce the overshoot, one can increase the gate resistance or decrease the loop inductance on the PCB with compact layout. Increasing the gate resistance will increase the switching loss because of longer turn-on time. Lower L in the loop will allow the usage of smaller gate resistance such that lowering the overshoot will not sacrifice too much on switching loss.

All these efforts have enabled a GaN-based seven-level structure without large voltage overshoot during switching, something that to date have impeded the development of high

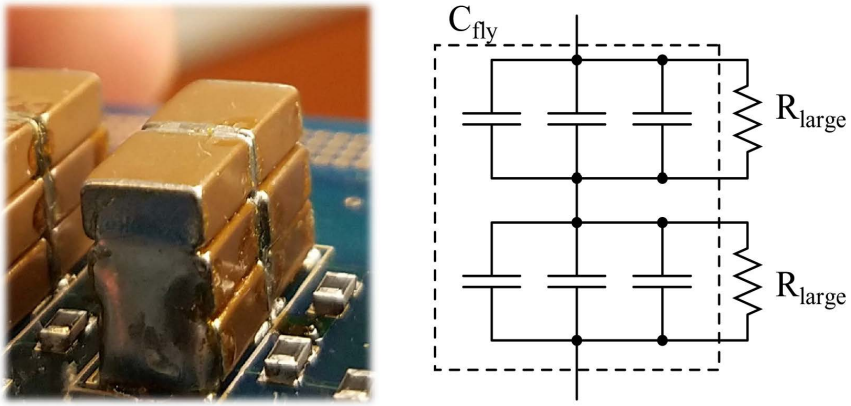


Figure 4.5: Single flying capacitor implementation.

(i.e. $\geqslant 5$) level FCML boost converters. Moreover, since this converter relies on the natural balancing properties of the FCML topology, this symmetrical board layout also helps minimize the parasitic effects that will cause unbalanced charge/discharge cycles on flying capacitors that in turn lead to voltage imbalance among flying capacitors. Imbalanced capacitor voltages increase the drain-source voltage, which can lead to switch failure if the blocking voltage exceeds the switch rating. This modular construction also facilitates the manufacturing and debugging process, where the switching cells can be tested for functionality individually before being assembled onto the converter board and quickly replaced if switch failure occurs.

4.2 Flying capacitors

Ceramic capacitors are used as the flying capacitors, since they have much higher energy density than film capacitors and much lower ESR and ESL than electrolytic capacitors [22]. One important design consideration is that with ceramic capacitors, the capacitance at full rated voltage can be reduced by a factor of 4 to 10, compared to the rated value at zero bias voltage [22]. This change in capacitance can greatly affect the natural balancing of the flying capacitor voltages, as well as the voltage ripple on each flying capacitor. Imbalance of the flying capacitor voltages and large capacitor voltage ripple can lead to switch failure if the switch voltage exceeds the rating, so the reduction of effective capacitance with increasing voltage has to be taken into account in the design.

Since the target output voltage of the converter is 1 kV, the flying capacitors should be rated for up to 1 kV. There are two options for implementing the flying capacitor. The

first option is to directly use 1 kV rated ceramic capacitors. One such example of ceramic capacitor with high energy density and a reasonable size is the Knowles Syfers 0.47 uF with a footprint of standard 2220 (5750 metric) package and height of 4.5 mm. However, the effective capacitance of this ceramic capacitor at 1000 V will degrade to one tenth of the nominal value, which results in an energy density of 0.183 mJ/mm^3. The second option is to construct a 1 kV capacitor using two 500 V rated ceramic capacitors from TDK in series. The capacitance only degrades to one fourth of its nominal value when operating at the full rated voltage. This results in an effective energy density of 0.78 mJ/mm^3, which is four times larger than using the 1000 V capacitor. Overall, the volume of a set of flying capacitor (say C_5), is 71.25 mm^3 for an effective capacitance of 0.825 μF, by using a total of six of the 500 V capacitors as shown in Fig. 4.5.

One challenge of this approach is the voltage balance between two capacitors connected in series. In the application considered here, series voltage imbalance is exacerbated by the combination of high-current and high-frequency charge and discharge cycles of the capacitors. Moreover, the reduced capacitance with voltage rating of the ceramic capacitors presents yet another challenge in this regard, as any capacitor with too high voltage will see a decrease in capacitance. When charged with the same current as the other capacitor in the series-connected set, it will thus see a larger increase in voltage, further increasing the imbalance. This voltage imbalance, if large enough, will cause voltage overstress on one capacitor and fail the capacitor. To solve this issue, two balancing resistors are placed as shown in Fig. 4.5. The balancing resistors' rated voltage and resistance should be large enough to bias the capacitors and dissipate very low power simultaneously. For the prototype, a resistance of 330 kΩ is found to be sufficient to balance the capacitors while only dissipating maximum power of 0.6 W on each resistor.

As mentioned earlier, the capacitance of ceramic capacitors becomes smaller at higher voltage bias, so C_4 and C_5 will have smaller capacitance than the rest of the flying capacitors during the operation of the converter. For this reason, when C_4 and C_5 are connected with inductor in series as shown in Fig. 4.6, the largest capacitor voltage ripple is expected, which will be seen by switch S_5. With maximum input current of 10 A, maximum output voltage of 1 kV, switching frequency of 72 kHz and flying capacitor capacitance of 0.825 μF, the voltage stress on S_5 is calculated by Eq. (3.2) and Eq. (3.3) to be 177.9 V, allowing 200 V devices being used in this design.

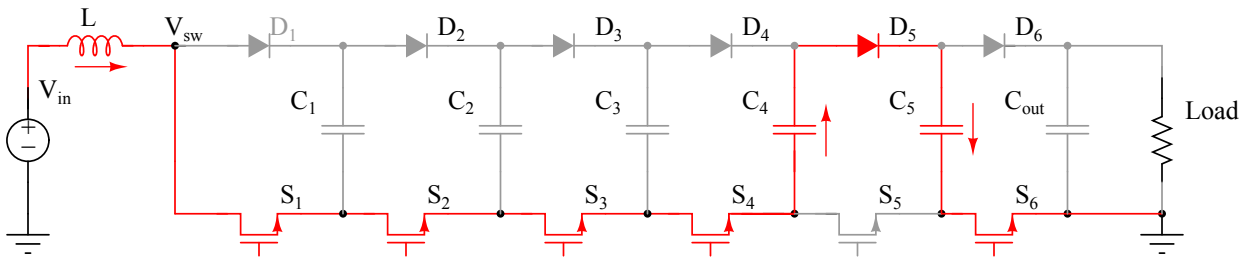


Figure 4.6: C_4 and C_5 connected in series.

4.3 Diodes

4.3.1 Reverse recovery effect of p-n junction diodes

In hard-switched converters with p-n junction diodes as power stage switches, one major source of switching loss comes from the reverse recovery effect of the p-n diodes [23]. If the p-n junction diode is forward-biased, there will be excessive minority carriers in the p-type and n-type bulk regions. When turning off the diode, such minority carriers in the bulk regions need to be removed so that the diode can begin to block reverse voltage, and since the minority carriers are diffused into the bulk region, this type of charge is called the diffusion charge. After the diffusion charge is removed and the diode is starting to block voltage, the depletion region of the p-n junction will start to grow. In other words, the diode's depletion region functions like a capacitor, which will be charged from 0 V to the full reverse voltage. And the charge transferred in this process is called the depletion charge. The removal of diffusion charge and the addition of depletion charge both generate current that is opposite to the forward-biased current direction.

Figure 4.7 shows the voltage and current waveforms of the MOSFET and diode during MOSFET turn-on in a hard-switched boost converter (the diode is the S_1 in Fig. 2.1, and the MOSFET is the S_2. The process here is switching from state 2 to state 1 in Fig. 2.2). At t_0, the MOSFET is turned-on and starts to steer away current from the diode. At t_1, the MOSFET has taken all the current from the diode and the diode current reaches zero. If it were an ideal diode, it would start to block voltage immediately and the current stays at zero. However, because of the reverse recovery effect described in the previous paragraph, the diode current will have a negative portion before it reaches zero again. From t_1 to t_2, the excessive minority carriers in the bulk region is removed. At t_2, the diode is fully off and ready to block reverse voltage. From t_2 to t_3, the depletion region is getting charged and at t_3, the diode is blocking the full reverse voltage. And the drain-to-source capacitance in the MOSFET is also discharged to 0 V.

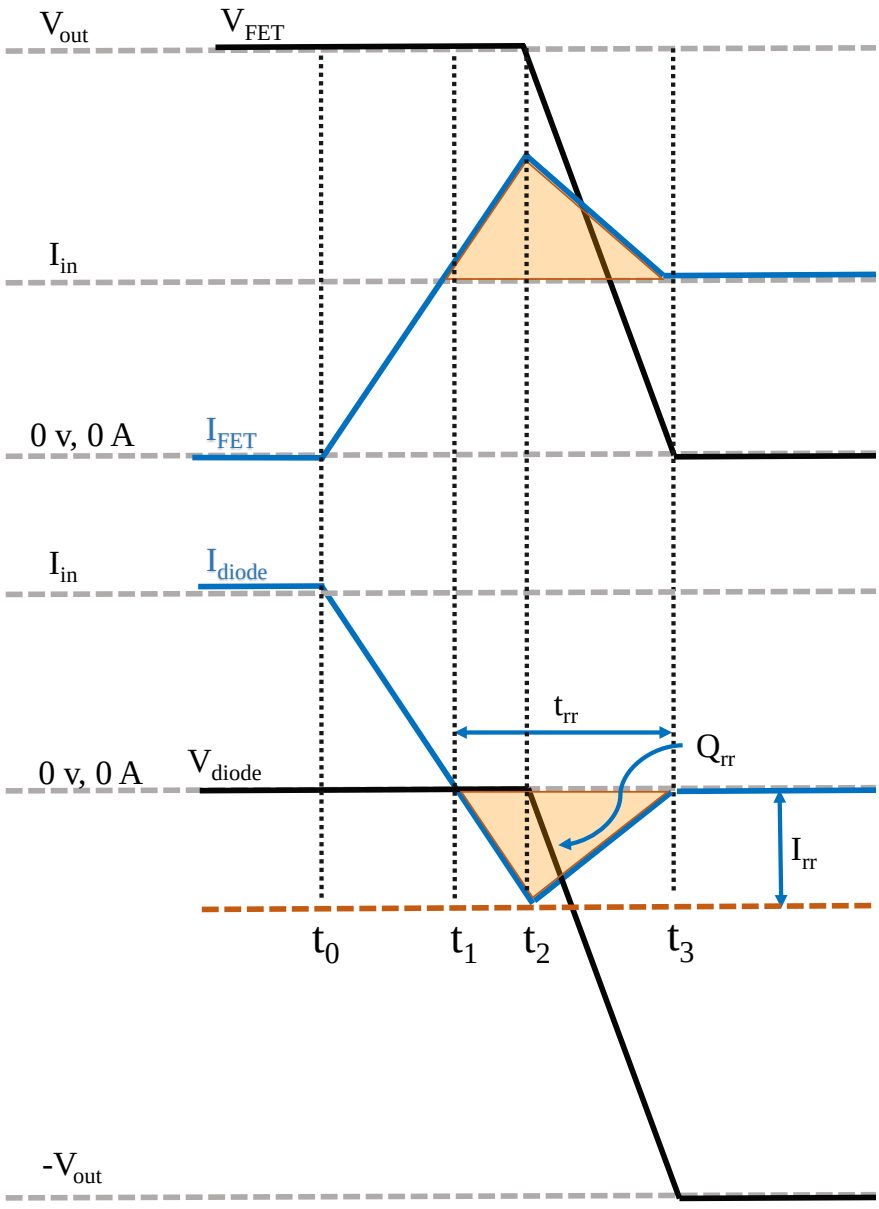


Figure 4.7: Voltage and current waveforms of MOSFET and diode during MOSFET turn-on in a hard-switched boost converter.

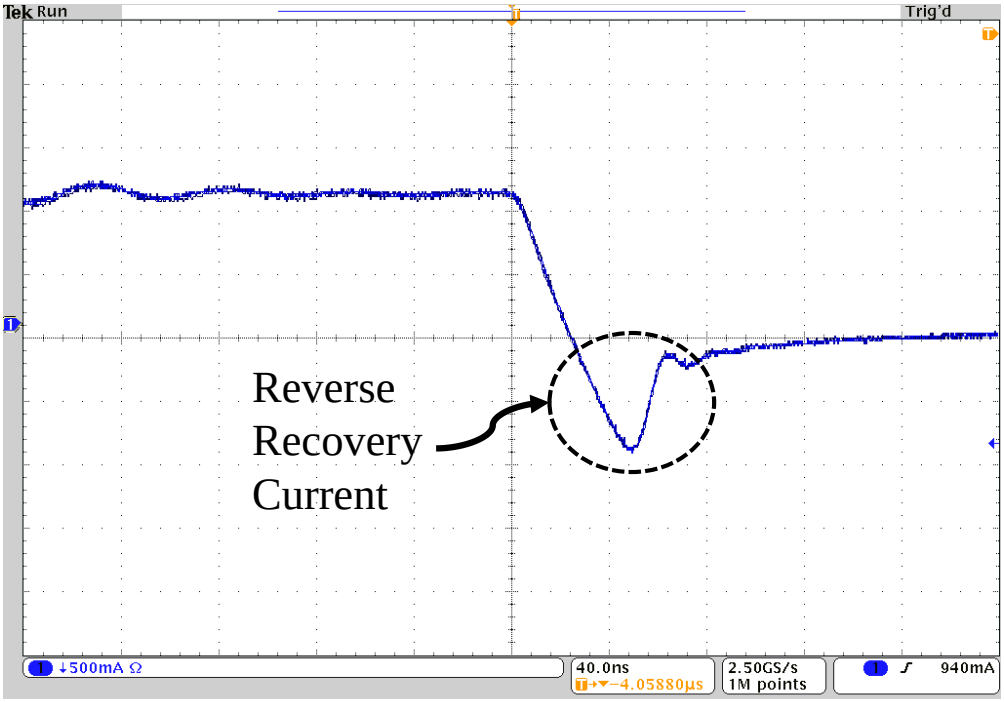


Figure 4.8: S320 Schottky diode reverse recovery current (2 V to 20 V conversion, 1 A input current).

To study the loss during this process, we first define some parameters of interests. The t_{rr} is the reverse recovery time that is t_1 to t_3 in Fig. 4.7. The Q_{rr} is the reverse recovery charge. It is the sum of the diffusion charge and depletion charge, and is represented by the shaded area in Fig. 4.7. The energy loss during reverse recovery process can be found by integrating the voltage and current product from t_1 to t_3 to be

$$E_{\mathrm{rr}} = V_{\mathrm{out}} I_{\mathrm{in}} t_{\mathrm{rr}} + V_{\mathrm{out}} Q_{\mathrm{rr}} \tag{4.2}$$

The intuitive understanding of this equation is that the reverse recovery effect introduces extra switching loss by lengthening the transition time (the first term in Eq. (4.2)) and dissipating extra charge in the MOSFET (the second term in Eq. (4.2)). Since the reverse recovery charge and time increase with increasing diode current turn-off rate $\frac{di}{dt}$, the reverse recovery effect is expected to be an important loss mechanism due to the use of fast-switching GaN switches in this work.

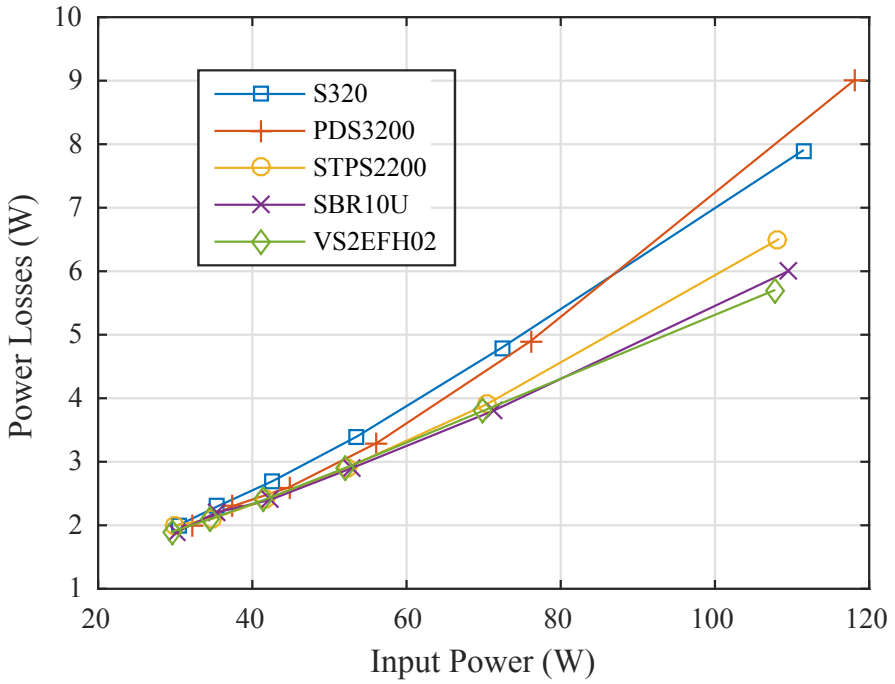


Figure 4.9: Converter power losses with different diodes (30 V to 300 V conversion, 72 kHz switching frequency).

4.3.2 Diode selection

The Schottky diode is known for having very little reverse recovery effect since it is a majority-carrier device. However, higher rating ($\geqslant$ 200 V) Schottky diodes will still produce large peak reverse recovery current because of the parallel guard-ring p-n junction diode [24]. As confirmed by [25] as well as our own measurement, the reverse recovery current is indeed found to be significant for 200 V Schottky diodes, as shown in the example converter waveform in Fig. 4.8. Another type of diode that is known for having very negligible reverse recovery behavior is the SiC diode [26]. They usually have high ($\geq 600\ V$) blocking voltage, which means they have much larger on-resistance than lower voltage rated p-n diodes in general. The model that has been tested in this work is 600 V, 3.3 A, C3D1P7060Q SiC diode from Cree. Experimental evaluation of these diodes showed that the RMS conduction loss due to large on-resistance was too high as a trade-off for low reverse recovery loss. However, the larger on-resistance of SiC did affect the natural balancing of flying capacitors, which will be discussed in Chapter 5.

Most diode manufacturers provide little information on the reverse recovery characteristics, which makes it difficult to estimate the associated losses at various operating conditions. For this reason, various types of diodes rated for 200 V have been evaluated under identi-

Table 4.3: Selected tested diodes.

Part number	Parameters	Type
Fairchild S320	200 V, 3 A	General Purpose Schottky
Diodes PDS3200	200 V, 3 A	General Purpose Schottky
STMicro STPS2200	200 V, 2 A	Power Schottky
Diodes SBR10U	200 V, 10 A	Super Barrier
Vishay VS2EFH02	200 V, 2 A	Hyperfast Reverse Recovery

cal conditions (30 V to 300 V conversion, 72 kHz switching frequency). Since the selected diodes have similar forward drop voltages, their conduction losses are well matched. For such reason, the different switching losses can be extracted from the difference in overall converter losses when using different diodes. Some major types of diodes that have been tested are general purpose Schottky, power Schottky, hyperfast recovery and super barrier diodes. Since diodes of the same categories showed similar performance, selected test results of a few typical diodes of their categories are presented in Fig. 4.9 and tested diode specifications are listed in Table 4.3.

It can be seen that the switching loss from the hyperfast reverse recovery diode is the lowest across the whole tested load range. A detailed loss breakdown based on the reverse recovery characteristics of the Vishay VS2EFH02 diode will be discussed in Chapter 5.

CHAPTER 5

EXPERIMENT RESULTS

The converter was tested with an input voltage of 100 V and duty ratio of 0.9 to generate 1 kV output voltage. Initially, the converter was constructed with six hyperfast diodes as shown in Fig. 3.3. Then several methods have been explored to reduce reverse recovery loss. The final design of the converter achieved 100 V to 1 kV conversion with 820 W maximum output power and 94.1 % peak efficiency within the tested load range.

Since 1 kV can cause significant electric shock to human body, a customized test enclosure as shown in Fig. 5.1 is manufactured to ensure safety in the lab.

5.1 Natural balancing of flying capacitor voltages

The flying capacitor voltages are monitored with National Instrument data acquisition system (PXIe-1073). Figure 5.2 shows the voltages of capacitors C_1 to C_5 and the input voltage during start-up with a 10 V input. It confirms that the flying capacitor voltages are in good balance as the voltages are around 16 V, or $\frac{V_{\mathtt{out}}}{N-1}$, apart from each other. It should be noted that the overshoot in voltages is not due to the dynamics of the converter. It is caused by the fact that the input power supply has an overshoot at the end of a fast ramping, as can be observed from the trajectory of $V_{\mathtt{in}}$.

Another way to evaluate the natural balancing performance is to monitor the switching node voltage. A converter with good natural balancing should have switching node voltage with even height pulses with $\frac{V_{\mathtt{out}}}{N-1}$ peak voltage if the duty ratio is greater than $\frac{N-2}{N-1}$ (in this case, 0.9 is greater than $\frac{5}{6}$). It can be seen from the measured switching node waveforms, for example in Fig. 5.3, that the pulses do not have even height. The slight deviation from the nominal flying capacitor voltage in the waveform is denoted as the voltage increment. The natural balancing effect damps the voltage imbalance caused by parasitics in the PCB with the series resistance in the circuit and stabilize the capacitor voltages to new steady-state values [27]. As mentioned early in the diode selection section, the larger on-resistance of SiC diodes affected the natural balancing. Figure 5.5 shows the switching node voltage of 20 V to

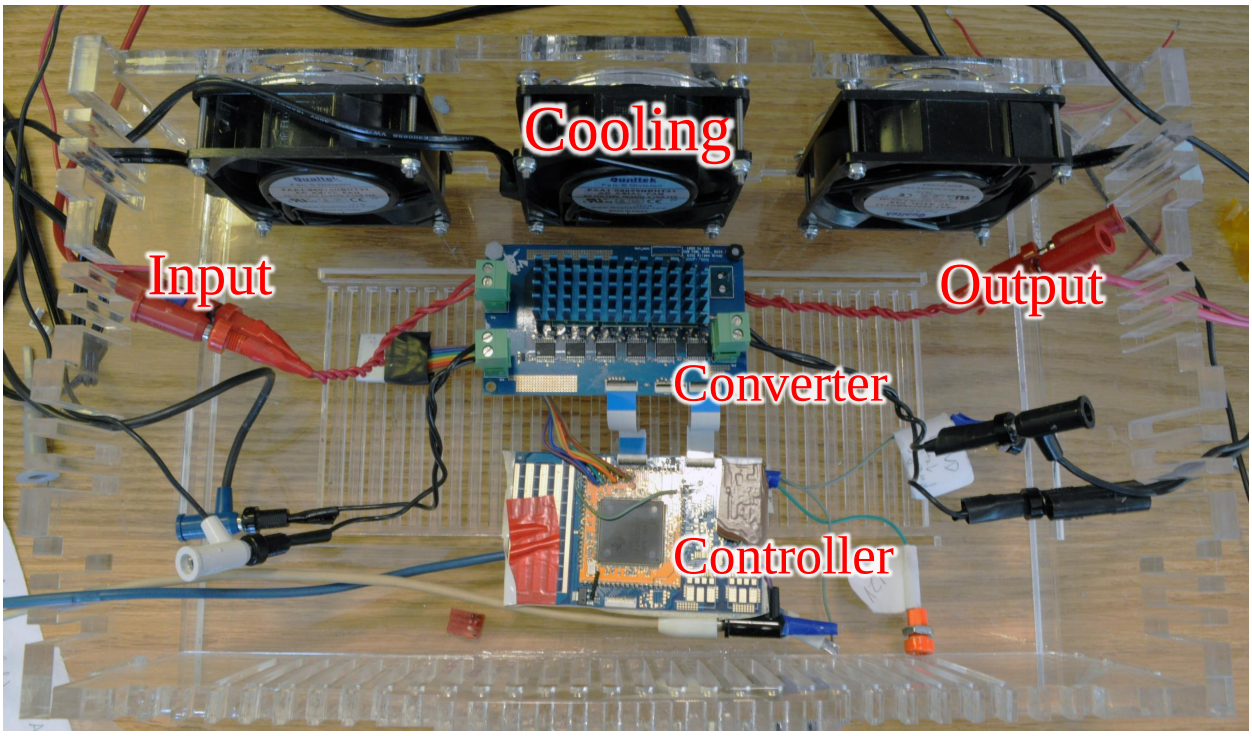


Figure 5.1: Test setup with safety enclosure.

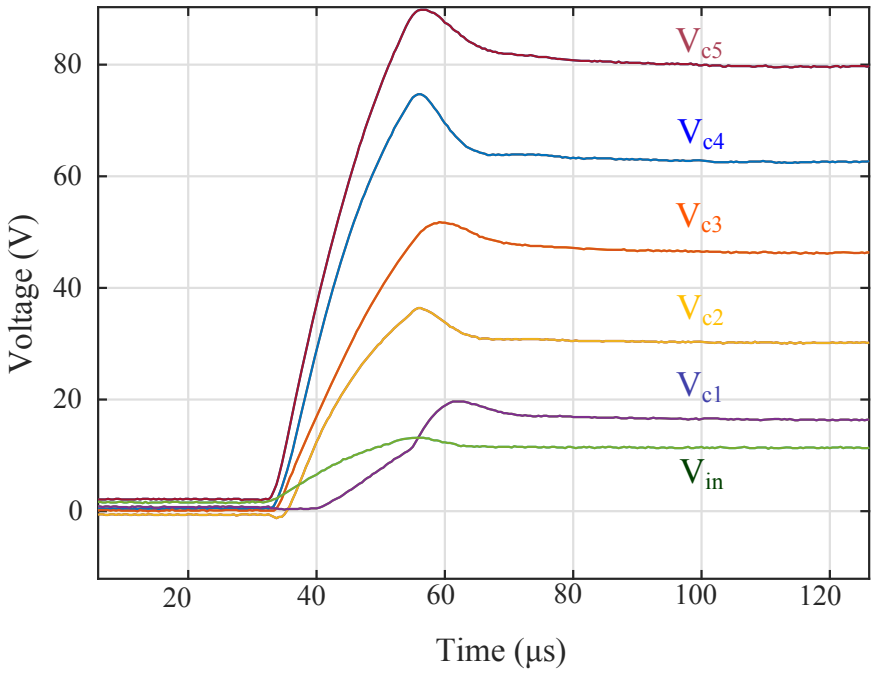


Figure 5.2: Measured flying capacitor voltages during a input voltage transient from 0 V to 10 V.

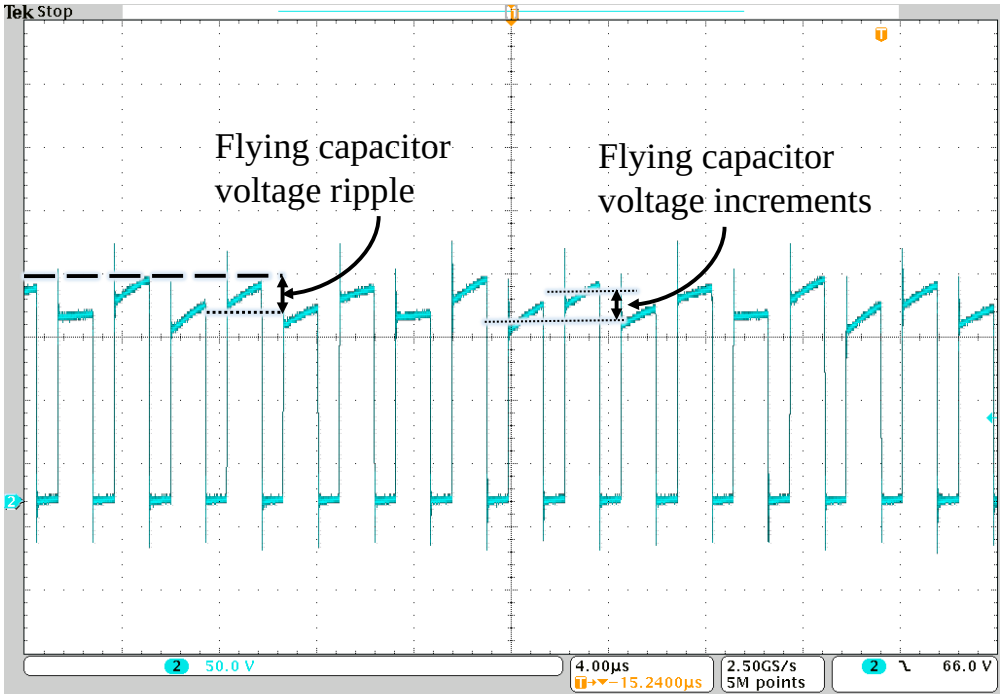


Figure 5.3: Switching node voltage ($V_{\mathtt{in}} = 100$ V, $V_{\mathtt{out}} = 914$ V, $P_{\mathtt{out}} = 750$ W).

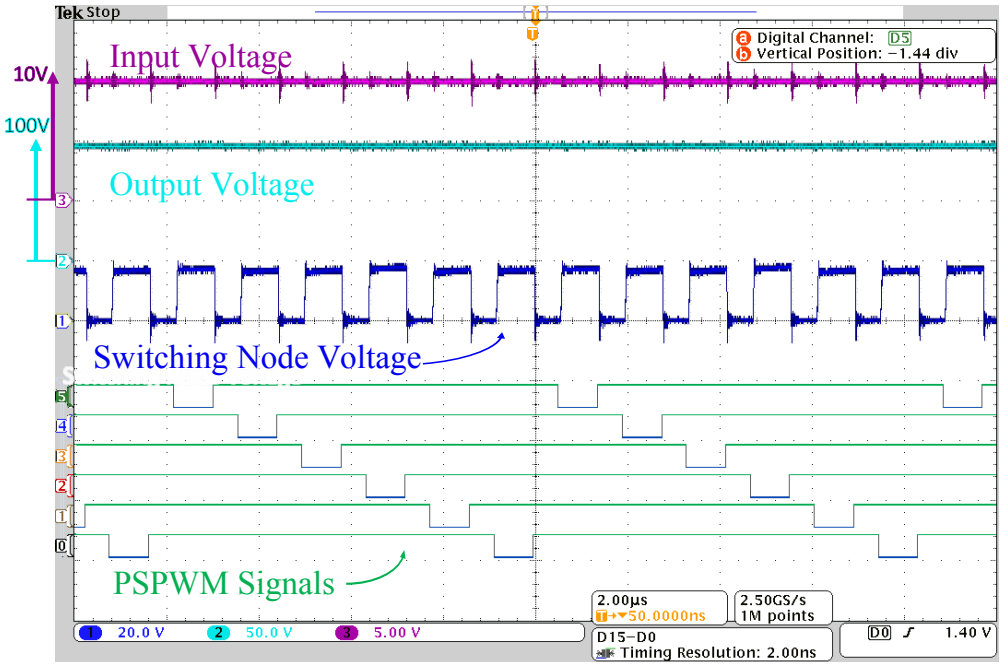


Figure 5.4: Input, output and the switching node voltages with PWM signals ($V_{\mathtt{in}} = 10$ V, $V_{\mathtt{out}} = 100$ V, $P_{\mathtt{out}} = 20$ W).

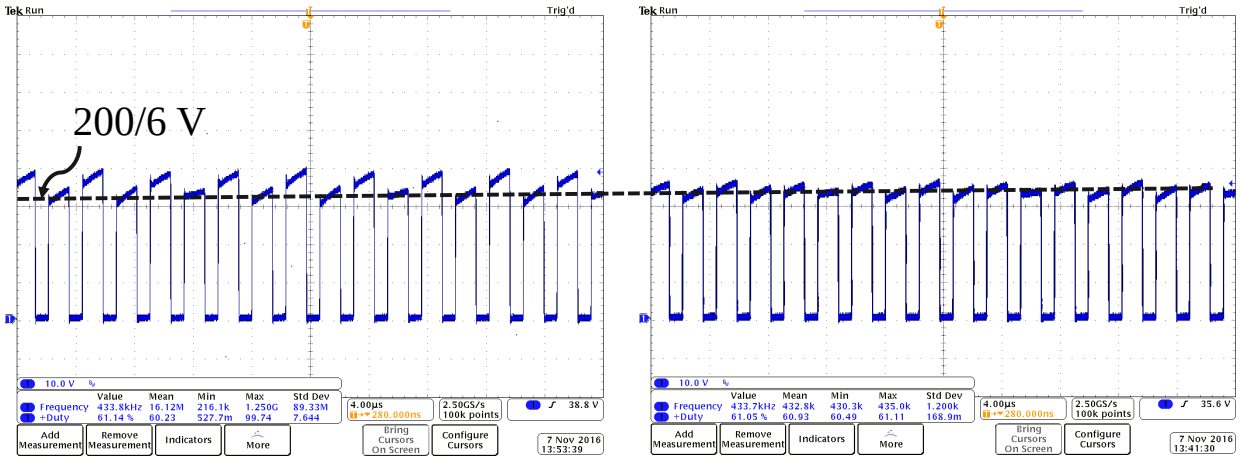


Figure 5.5: Switching node voltage with hyperfast Si diodes (left) and SiC diodes (right), 20 V to 200 V conversion, 40 W output power.

200 V conversion at 40 W with hyperfast Si diodes and SiC diodes. Drawing a line at nominal voltage of $\frac{200}{6}$ V across the two waveforms, it can be observed that the switching node is more uniform with SiC than hyperfast diodes, which proves that the series resistance will damp the voltage imbalance much faster with the cost of extra power loss. Comparing Fig. 5.4 and Fig. 5.3, it can be readily observed that the switching node voltage is considerably more uniform in the low-voltage and low-power condition. This result is consistent with the theoretical prediction in [27] that the voltage increments of flying capacitor voltage within one switching cycle is proportional to the natural balancing voltage (which is proportional to the output voltage) and inversely proportional to the flying capacitor's capacitance. At higher output voltage, the effective capacitance of flying capacitors is also smaller, which makes the flying capacitors' voltage increments even larger. As a result, in Fig. 5.3, the maximum voltage of switching node reached around 190 V with voltage increment added to the maximum switching node voltage calculated by Eq. (3.3).

5.2 Loss breakdown

The power loss can be categorized into four major sources: loss on the inductor, which includes both core loss and conduction loss; loss on the GaN FETs, which includes conduction loss and overlap switching loss; diode conduction loss; and extra switching loss introduced by diode reverse recovery effects.

The first three categories excluding the inductor core loss can be calculated fairly accurate

with the given information from the datasheets of the components. The inductor core loss can also be estimated fairly well from the loss model provided by the manufacturers.

Extra power loss introduced by the reverse recovery current can be estimated by multiplying the energy loss (obtained from Eq. (4.2)) with the switching frequency. However, since the values of Q_{rr} and t_{rr} not only change with the current turn-off rate but also with temperature, the exact loss can be hard to calculate at different power levels as the temperature changes. To reflect the effect of temperature on such loss, an assumption is made that the diode temperature rises linearly with input current, and Q_{rr} and t_{rr} also increase linearly with temperature for a first-order estimation. The Matlab script for calculating losses are presented in Appendix A.

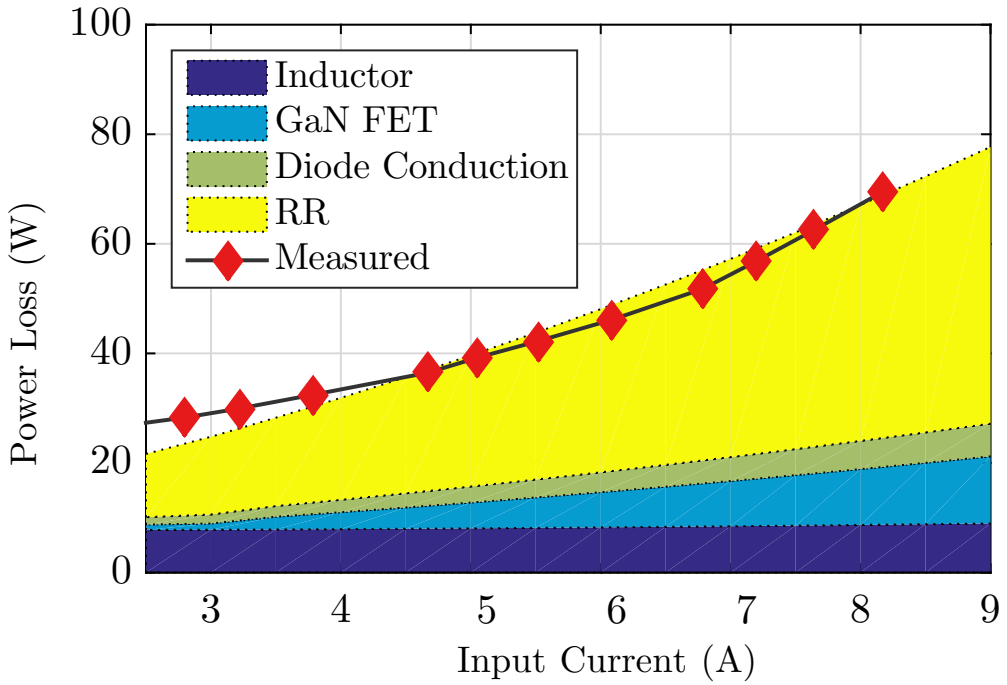


Figure 5.6: Measured loss and loss breakdown for 100 V to 1 kV conversion.

5.3 Methods to reduce reverse recovery loss

Even though effort has been made to reduce reverse recovery loss in the process of diode selection as discussed in Chapter 4, the loss breakdown estimation in Fig. 5.6 still shows that the reverse recovery loss is the largest portion of the total loss as power increases to a certain level, which brings up the discussion of how to alleviate such loss with other possible techniques. The method that has been implemented in [25] to alleviate this type of loss is to

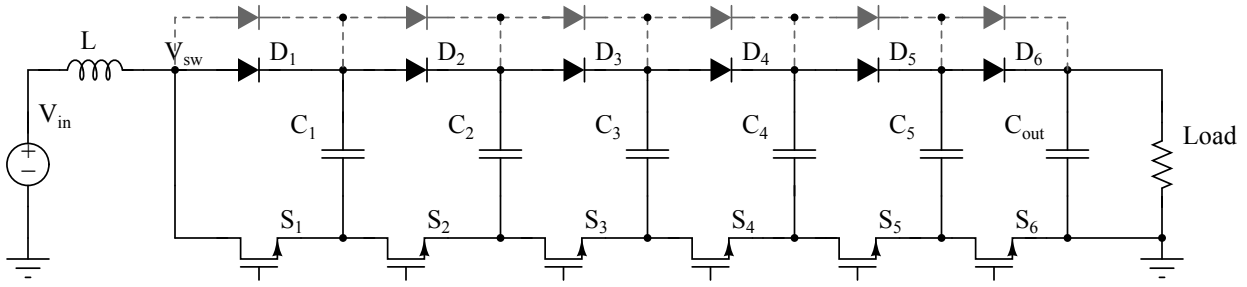


Figure 5.7: Converter with extra parallel diodes.

connect four lower voltage rating Schottky diodes in series to function as a single high voltage rating device. Since each of them has negligible reverse recovery effect because they have no guard-ring p-n diode as in the higher voltage rating Schottky diodes, this configuration will introduce minimum reverse recovery loss. However, this design will increase the total diode forward drop loss and reduce the overall conversion ratio. It is also uncertain that the voltage is shared equally among diodes when they are reverse-biased, and if it is not, possible damage could happen to the devices.

5.3.1 Parallel diodes

The first method that has been implemented in this thesis is to parallel-connect each diode with another diode as shown in Fig. 5.7. This method turned out to be very effective and managed to bring significant reduction of overall losses. As shown in Eq. (4.2), the reverse recovery loss increases with the input current. Moreover, as mentioned in Section 4.3, the value of Q_{rr} and t_{rr} both change with temperature, which will vary with input current as well. For first-order estimation, we assume a linear relationship between current and temperature. Because of the assumption, the reverse recovery loss will be proportional to the square of the input current. With two diodes sharing the current that used to be carried by one diode, the temperature of each diode will rise much slower as input current increases, which means at the same input current, the values of Q_{rr} and t_{rr} are much lower. The reverse recovery loss is expected to be reduced by nearly half because of the assumed linearities as mentioned above.

One of the common-known problems for paralleling diodes is the thermal run-away effect caused by unequal sharing of current and temperature between diodes. The thermal run-away effect is the result of a positive feedback loop between diode's forward drop voltage and temperature. If there is a little mismatch of temperature between two diodes, the hotter diode will have lower forward drop voltage such that it will carry more current, and the

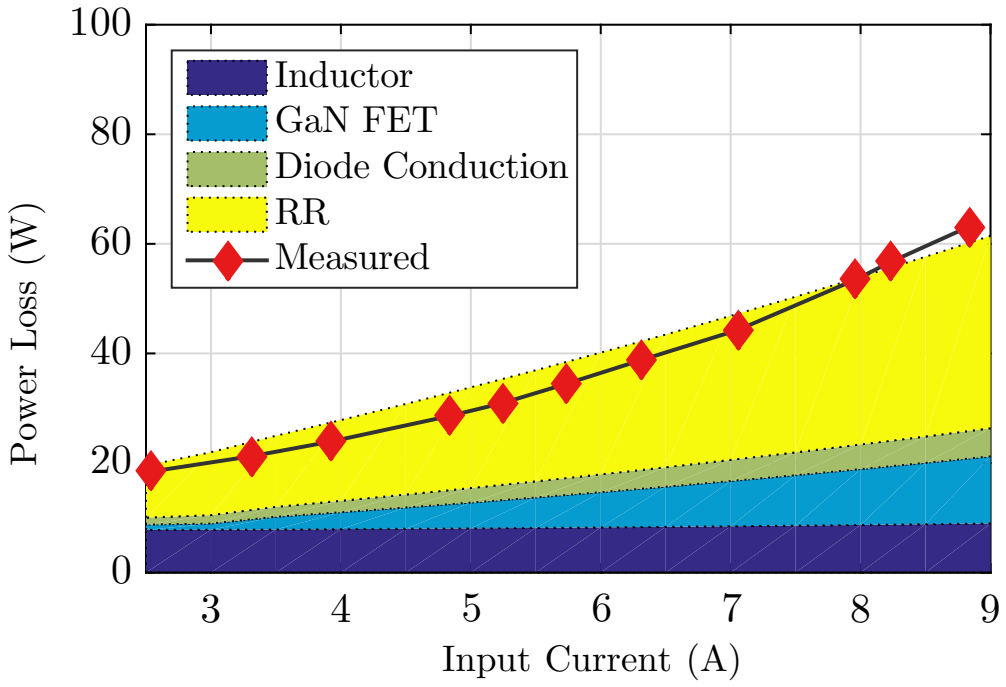


Figure 5.8: Measured loss and loss breakdown for 100 V to 1 kV conversion with extra parallel diode.

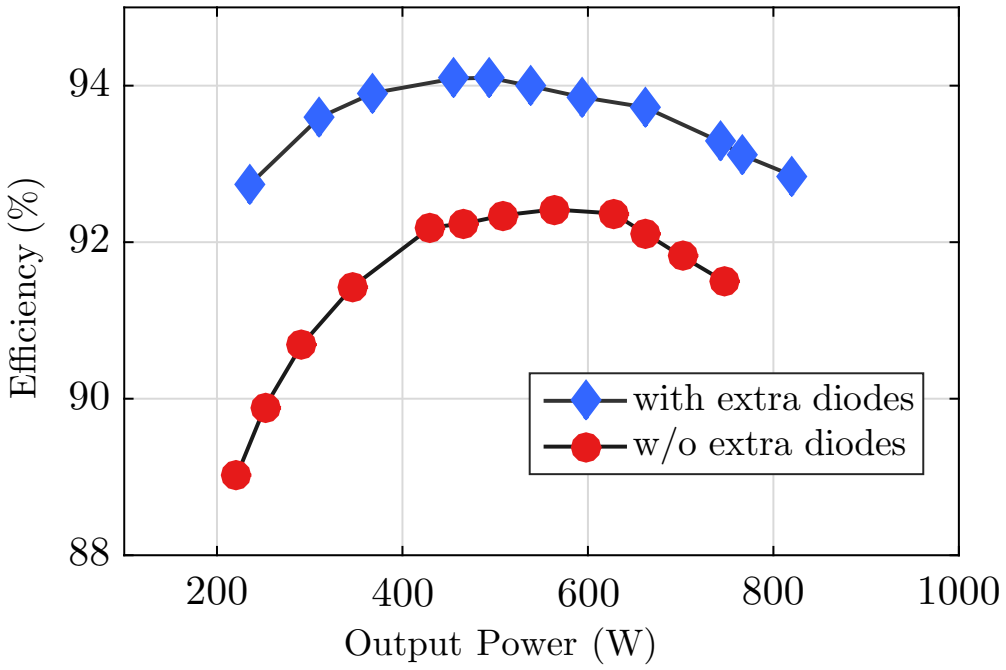


Figure 5.9: Efficiency plots for 100 V to 1 kV conversion with and without extra parallel diodes.

difference in temperature will be enlarged. The end result is one diode will carry most of the current and get much hotter than the other. To avoid the thermal run-away effect, all parallel-connected diode pairs are installed under the same thermal substrate such that the heat can be shared evenly among diodes. Figure 5.8 shows the calculated loss breakdown and the measured loss with two diodes in parallel for 100 V to 1 kV conversion from 2.5 A to 10 A input current. As a comparison in Fig. 5.6 with the original configuration, both the calculated loss from the loss model and the experiment results are approximately 10 W lower at 8 A input current with extra parallel-connected diodes, and the converter was able to achieve 94.1% peak efficiency across the full tested load range as shown in the efficiency plot of Fig. 5.9.

5.3.2 QSW-ZVS

Another potential method to improve the efficiency is to apply Quasi Square Wave Zero Voltage Switching (QSW-ZVS) technique in [28] to lower the switching loss caused by diode's reverse recovery effect. QSW-ZVS is realized by operating the converter in shallow DCM or boundary-conduction mode – i.e., the current ripple ratio α is slightly larger than two.

Figure 5.10 demonstrates how QSW-ZVS can reduce the reverse recovery loss. Because of shallow DCM operation, at t_0 the inductor current falls to zero slightly before the MOSFET turns on. As illustrated in Fig. 4.7, when the diode current reaches zero, the reverse recovery process will take place. The current turn-off rate will just equal to the inductor current ripple divided by half of the period that can be obtained from Eq. (2.1). Compared to the hard-switched case where the diode current is switched by the MOSFET from full input current to zero in few nanoseconds, QSW-ZVS will introduce much lower reverse recovery charge and much shorter recovery time due to low current turn-off rate. At t_1, the diffusion charge is removed from the bulk region so the diode can start blocking reverse voltage. From t_1 to t_2, the output capacitor of the MOSFET is discharged together with the diodes depletion charge as shown in the schematic on the top of Fig. 5.10, and this amount of charge from the output capacitor of the MOSFET is denoted as Q_{oss}. At the moment the MOSFET is turning on, the voltage across drain and source of the MOSFET is already zero. Compared to the hard-switched case in Fig. 4.7, the reverse recovery charge Q_{rr} and the output charge of the MOSFET Q_{oss} are losslessly sent back to the source instead of being dissipated in the on-resistance of the MOSFET.

To test the effectiveness of QSW-ZVS, two inductors of different inductance values were used for the converter to operate in hard-switched mode and QSW-ZVS, respectively. The

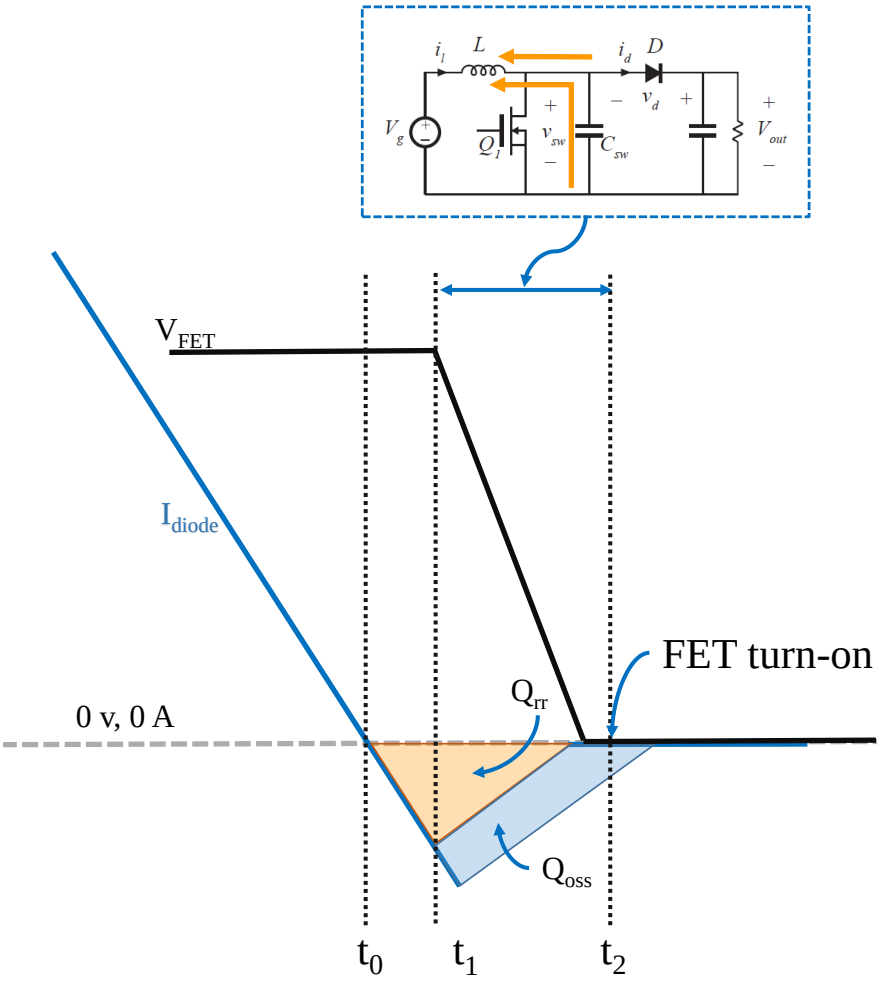


Figure 5.10: Diode current and switching node voltage during diode turn-off under QSW-ZVS [28].

Figure 5.11: Hard-switched, 30 V to 300 V conversion. $P_{\text{in}} = 106$ W, $P_{\text{out}} = 100$ W, f_{sw}= 72 kHz, L= 22 μH.

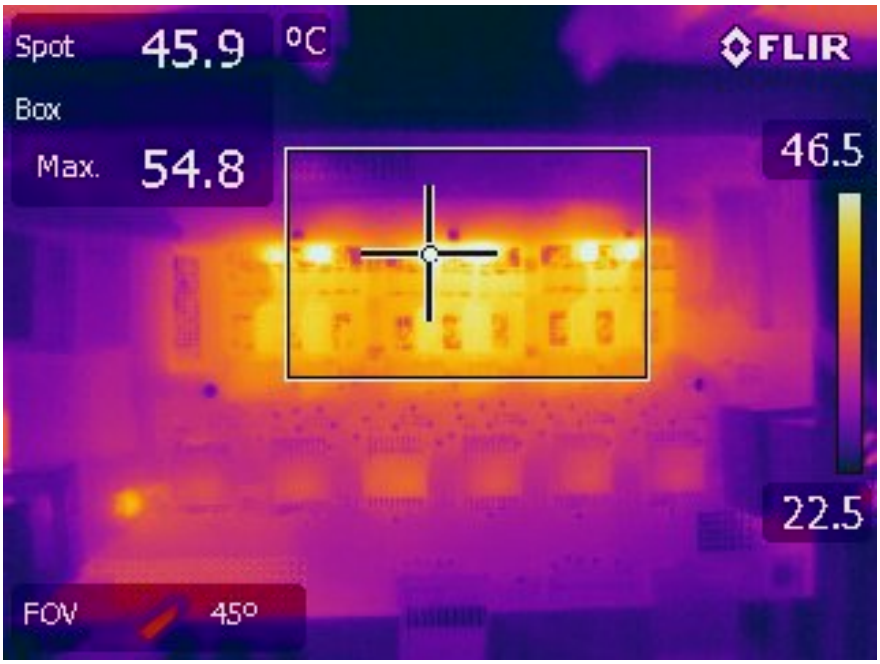


Figure 5.12: QSW-ZVS, 30 V to 300 V conversion. $P_{\text{in}} = 108.68$ W, $P_{\text{out}} = 101.99$ W, f_{sw}= 69 kHz, L= 4 μH.

Table 5.1: Comparison of recent work on high step-up converters.

	[29]	[30]	[25]	FCML boost
Rated power	450 W	250 W	2 kW	820 W
Input voltage	25-30 V	28-38 V	275 V	100 V
Max output voltage	400 V	300-980 V	2 kV	1 kV
Peak efficiency	96%	97%	84%	94.1%
Switching frequency	100 kHz	100 kHz	13.56 MHz	72 kHz
Overall power density	38 W/in^3	19 W/in^3	250 W/in^3	329 W/in^3

converter was tested for 30 V to 300 V conversion at similar power level of around 107 W. Figure 5.11 shows the thermal image of the converter in hard-switched mode with 22 μH inductor and Fig. 5.12 shows the thermal image in QSW-ZVS with 4 μH inductor. It can be seen that the temperature of the switches was lower by 5 °C in QSW-ZVS mode than the hard-switched mode. Since the current ripple is much higher in the QSW-ZVS case, the RMS conduction loss is higher. The resultant lower temperature on the switches means the total power loss on the switches, which is the sum of the switching loss and the conduction loss, has been lowered, which implies that the reduction of the switching loss is larger than the increase in conduction loss.

However, the overall converter loss turned out to be similar. Large inductor current ripple will increase the core loss in the inductor. More optimization should be done on the inductor to make sure the core loss and the physical size will not dominate. (By the time of writing this thesis, a better inductor was found with low core loss but one of the GaN FET failed during testing so the converter is not functional now.)

5.4 Comparison with other high step-up converters

Compared to other works that have explored methods for compact and efficient step-up conversion in Table 5.1, this converter showed good balance among efficiency, power density and voltage gain. In [29], a conventional boost converter is merged with Cockcroft-Walton Multiplier charge pumps to alleviate the voltage stress on individual switches. It achieved high efficiency and high voltage gain, but the large volume of required capacitors limited the power density. The converter in [30] achieved good voltage gain and efficiency with soft-switching techniques and step-up transformers, but the large size of the magnetic components resulted in low power density. In [25], the inductor size is shrank substantially by switching at very-high frequency and the switching loss is reduced by operating the converter in resonant

mode [31]. However, the multiple stage design of matching networks, transformers and rectifiers leaded to low overall system efficiency. And the passive components in matching networks and the transformer contributed a lot to the converter's total volume.

CHAPTER 6

CONCLUSIONS

This work presented the design fundamentals and practical implementation considerations of a seven-level FCML boost converter. A prototype converter with compact layout has been implemented and successfully converted 100 V to 1 kV at 820 W output power, with 94.1% peak efficiency reached at 542 W input power, achieving 687 W/in^3 (42 W/cm^3) power stage power density and 329 W/in^3 (20 W/cm^3) overall power density. Optimal implementation for flying capacitor design at high operating voltage has been discussed. Different diodes have been evaluated for their switching performances. Techniques to reduce reverse recovery loss have been explored and experimented. QSW-ZVS technique can be further investigated using inductors with lower core loss.

APPENDIX A

LOSS CALCULATION MATLAB SCRIPT

```
Iin = 2.5:0.5:10;
fsw = 72e3;
Vin = 100;
vds = 1000/6; % vout/6 for each FET
Vf = 1;
num_levels = 7;
DCR = 16e-3;
L = 22e-6;
num_d = 1; %number of parallel diodes

% switch
% Rgate external and internal driver mosfet resistance
Rgon = 15+10;
Rgoff = 1.5;
Rds = 10e-3;
% equivalent input charge to move through plateua region
Qgsw = (1.7+3.5/2)*1e-9;
% [V] gate-source threshold voltage
Vth = 2.0;
% [V] gate driver voltage
Vdrv = 5.0;
Igon = (Vdrv-Vth)/Rgon;
Igoff = Vth/Rgoff;

ton  = Qgsw/Igon;
toff = Qgsw/Igoff;

Iripple = (vds-Vin)*(0.1)/(L*fsw);
Irms = sqrt(Iripple^2/12+Iin.^2);
Ion = Iin-Iripple/2;


% conduction loss+overlap_loss on GaN
```

```
loss_gan = Irms.^2*Rds*0.9*(num_levels - 1)
+ 0.5*vds.*Ion.*(toff+ton)*fsw*(num_levels - 1);

% conduction loss on Diode
loss_diode = 0.1*(Iin*0.8/num_d+(Irms/num_d).^2/12)*(num_levels - 1)

% conduction loss on inductor DCR
loss_dcr = Irms.^2*DCR

% calculate reverse recovery loss

%di/dt during diode turn-off (A/us)
k = Ion./(num_d*ton*10^6);
% estimated Qrr and trr relations with Iin
Qrr = (log10(k).*(8.33)+(4*Iin./num_d-4)).*1e-9;
trr = (4*Iin./num_d+50-log10(k).*(10)).*1e-9;
%reverse recovery loss
loss_reverse = vds*(trr.*Iin/num_d+Qrr)*fsw*(num_levels - 1);


%total loss
loss = loss_inductor + loss_gan + num_d.*loss_diode + num_d.*loss_reverse;
```

APPENDIX B

PSPWM GENERATION SOURCE C CODE

The PSPWM signals are generated with TI C2000 microcontroller. The source code is heavily based on Yutian Lei's code for a seven-level FCML inverter in [12].

```
/*
 * 1to10_FCML
 *
 */



#include "F28x_Project.h"     // Device Headerfile and Examples Include File
#include "FCMLPhaseShift.h"


// Global variable definitions
float main_duty = DUTY;



// Local variable definiations
uint32_t PERIOD;        // period of the ePWM counter
uint16_t deadtime_r = 9;      // Rising edge deadtime - Yutian had 2...we used
    1
uint16_t deadtime_f = 3;      // Falling edge deadtime
int32 phase = 360/(num_levels-1);        // phase shift of each ePWM, in
    degrees
int32 sysclk = 120000;  // system clock, in kHz
//int32 num_levels;


float ps2_float;
float ps3_float;
float ps4_float;
```

```
float ps5_float;
float ps6_float;
float ps7_float;

int32 ps2;      // phase shift for ePWM2
int32 ps3;
int32 ps4;
int32 ps5;
int32 ps6;
int32 ps7;
//int32 offset = 2;

int32 num_points;   // number of points in a complete sine wave
float step;
int32 index = 1;            // current position in sine wave

//dither variables

// Functino definitions
void Init_cputimer_sin_TMU()
{

    // Initialize GPIO for unfolder PWM
    GPIO_SetupPinMux(0, GPIO_MUX_CPU1, 0);
    GPIO_SetupPinOptions(0, GPIO_OUTPUT, GPIO_PUSHPULL);
    GPIO_SetupPinMux(1, GPIO_MUX_CPU1, 0);
    GPIO_SetupPinOptions(1, GPIO_OUTPUT, GPIO_PUSHPULL);
    GPIO_WritePin(0, 1);
    GPIO_WritePin(1, 0);
    // setup sine wave number of points and step size
    num_points = PERIOD*2;
    //num_points = sysclk/120/10*2;     // Duty ratio update frequency is 10
    kHz
    step = 1.0/num_points;

    // CPU Timer 0

    // Make sure timer is stopped:
    CpuTimer0Regs.TCR.bit.TSS = 1;

    // Initialize timer period to maximum:
    int32 timer0_period = sysclk*1000/fundamental_frequency/num_points;
    CpuTimer0Regs.PRD.all  = timer0_period;
```

```
72
73      // Initialize pre-scale counter to divide by 1 (SYSCLKOUT):
74      CpuTimer0Regs.TPR.all  = 0;
75      CpuTimer0Regs.TPRH.all = 0;
76
77      // Reload all counter register with period value:
78      CpuTimer0Regs.TCR.bit.TRB = 1;
79
80      CpuTimer0Regs.TCR.bit.TIE = 1;          // Enable timer 0 interrupt
81
82      // Start the timer
83      CpuTimer0Regs.TCR.bit.TSS = 0;
84  }
85
86
87
88  void Init_phase_shifted_pwm()
89  {
90
91      // enable PWM1, PWM2, PWM3, PWM4, PWM5, PWM6
92      CpuSysRegs.PCLKCR2.bit.EPWM1=1;
93      CpuSysRegs.PCLKCR2.bit.EPWM2=1;
94      CpuSysRegs.PCLKCR2.bit.EPWM3=1;
95      CpuSysRegs.PCLKCR2.bit.EPWM4=1;
96      CpuSysRegs.PCLKCR2.bit.EPWM5=1;
97      CpuSysRegs.PCLKCR2.bit.EPWM6=1;
98      CpuSysRegs.PCLKCR2.bit.EPWM7=1;
99
100     // Initialize GPIO pins for ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM6
101     // These functions are in the F28M36x_EPwm.c file
102     InitEPwm2Gpio();
103     InitEPwm3Gpio();
104     InitEPwm4Gpio();
105     InitEPwm5Gpio();
106     InitEPwm6Gpio();
107     InitEPwm7Gpio();
108
109     PERIOD = sysclk/switching_frequency;     // ePWM timer period
110
111     // Phase shift for each ePWM
112     ps2_float = 0;
113     ps3_float = (phase*1.0/360.0);
114     ps4_float = (phase*2.0/360.0);
```

```
115     ps5_float = (phase*3.0/360.0);
116     ps6_float = (phase*4.0/360.0);
117     ps7_float = (phase*5.0/360.0);
118
119     ps2=((int)(PERIOD*ps2_float))%PERIOD;
120     ps3=((int)(PERIOD*ps3_float))%PERIOD;
121     ps4=((int)(PERIOD*ps4_float))%PERIOD;
122     ps5=((int)(PERIOD*ps5_float))%PERIOD;
123     ps6=((int)(PERIOD*ps6_float))%PERIOD;
124     ps7=((int)(PERIOD*ps7_float))%PERIOD;
125
126
127     InitEPwm_1();                              // Initialize each ePWM
128     InitEPwm_2();
129     InitEPwm_3();
130     InitEPwm_4();
131     InitEPwm_5();
132     InitEPwm_6();
133     InitEPwm_7();
134
135
136 }
137
138
139
140 void InitEPwm_1()
141 {
142
143     EPwm1Regs.TBPRD = PERIOD;                    // Set timer period
144     EPwm1Regs.TBCTR = 0x0000;                    // Clear counter
145
146     // Setup TBCLK
147     EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count up
148     EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;        // Disable phase loading for
      the first ePWM, this becomes the master ePWM
149     EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio to SYSCLKOUT
150     EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;          // Same frequency as main
     clock
151     EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;      // send sync output signal
      when counter is zero
152
153     // Setup compare
```

```
154     EPwm1Regs.CMPA.bit.CMPA = PERIOD*main_duty;               // initial 50%
    duty ratio
155
156     // Set actions
157     EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;                // Set PWM3A on Zero
158     EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;
159
160     // Active high complementary PWMs and Setup the deadband
161     EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
162     EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
163     EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
164     EPwm1Regs.DBRED.bit.DBRED = deadtime_r;
165     EPwm1Regs.DBFED.bit.DBFED = deadtime_f;
166
167 }
168
169 void InitEPwm_2()
170 {
171
172     EPwm2Regs.TBPRD = PERIOD;                             // Set timer period
173     EPwm2Regs.TBPHS.bit.TBPHS = ps2;              // Phase is 0
174     EPwm2Regs.TBCTR = 0x0000;                              // Clear counter
175
176     // Setup TBCLK
177     EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count up
178     EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;         // Enable phase loading
179     EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;        // Clock ratio to SYSCLKOUT
180     EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;           // Same frequency as main
    clock
181     EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;       // pass sync in to sync
    out
182
183     // Setup compare
184     EPwm2Regs.CMPA.bit.CMPA = PERIOD*main_duty;               // initial 50%
    duty ratio
185
186     // Set actions
187     EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;                // Set PWM3A on Zero
188     EPwm2Regs.AQCTLA.bit.ZRO = AQ_SET;
189
190
191     // Active high complementary PWMs - Setup the deadband
192     EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
```

```
193     EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
194     EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;
195     EPwm2Regs.DBRED.bit.DBRED = deadtime_r;
196     EPwm2Regs.DBFED.bit.DBFED = deadtime_f;
197
198 }
199
200 void InitEPwm_3()
201 {
202
203     EPwm3Regs.TBPRD = PERIOD;                       // Set timer period
204     EPwm3Regs.TBPHS.bit.TBPHS = ps3;             //
205     EPwm3Regs.TBCTR = 0x0000;                     // Clear counter
206
207     // Setup TBCLK
208     EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count up
209     EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE;        // Enable phase loading
210     EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio to SYSCLKOUT
211     EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1;          // Same frequency as main
    clock
212     EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;       // pass sync in to sync
    out
213     // Setup compare
214     EPwm3Regs.CMPA.bit.CMPA = PERIOD*main_duty;              // initial 50%
    duty ratio
215
216     // Set actions
217     EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;               // Set PWM3A on Zero
218     EPwm3Regs.AQCTLA.bit.ZRO = AQ_SET;
219
220     // Active high complementary PWMs - Setup the deadband
221     EPwm3Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
222     EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
223     EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;
224     EPwm3Regs.DBRED.bit.DBRED = deadtime_r;
225     EPwm3Regs.DBFED.bit.DBFED = deadtime_f;
226
227 }
228
229 void InitEPwm_4()
230 {
231
232     EPwm4Regs.TBPRD = PERIOD;                       // Set timer period
```

```
233     EPwm4Regs.TBPHS.bit.TBPHS = ps4;              //
234     EPwm4Regs.TBCTR = 0x0000;                     // Clear counter
235
236     // Setup TBCLK
237     EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count up
238     EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE;        // Enable phase loading
239     EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;      // Clock ratio to SYSCLKOUT
240     EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;         // Same frequency as main
    clock
241     EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;      // pass sync in to sync
    out
242     // Setup compare
243     EPwm4Regs.CMPA.bit.CMPA = PERIOD*main_duty;             // initial 50%
    duty ratio
244
245     // Set actions
246     EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;              // Set PWM3A on Zero
247     EPwm4Regs.AQCTLA.bit.ZRO = AQ_SET;
248
249     // Active high complementary PWMs - Setup the deadband
250     EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
251     EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
252     EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL;
253     EPwm4Regs.DBRED.bit.DBRED = deadtime_r;
254     EPwm4Regs.DBFED.bit.DBFED = deadtime_f;
255
256
257 }
258 void InitEPwm_5()
259 {
260
261     EPwm5Regs.TBPRD = PERIOD;                       // Set timer period
262     EPwm5Regs.TBPHS.bit.TBPHS = ps5;              //
263     EPwm5Regs.TBCTR = 0x0000;                     // Clear counter
264
265     // Setup TBCLK
266     EPwm5Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count up
267     EPwm5Regs.TBCTL.bit.PHSEN = TB_ENABLE;        // Enable phase loading
268     EPwm5Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;      // Clock ratio to SYSCLKOUT
269     EPwm5Regs.TBCTL.bit.CLKDIV = TB_DIV1;         // Same frequency as main
    clock
270     EPwm5Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;      // pass sync in to sync
    out
```

```
271     // Setup compare
272     EPwm5Regs.CMPA.bit.CMPA = PERIOD*main_duty;              // initial 50%
    duty ratio
273
274     // Set actions
275     EPwm5Regs.AQCTLA.bit.CAU = AQ_CLEAR;                // Set PWM3A on Zero
276     EPwm5Regs.AQCTLA.bit.ZRO = AQ_SET;
277
278     // Active high complementary PWMs - Setup the deadband
279     EPwm5Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
280     EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
281     EPwm5Regs.DBCTL.bit.IN_MODE = DBA_ALL;
282     EPwm5Regs.DBRED.bit.DBRED = deadtime_r;
283     EPwm5Regs.DBFED.bit.DBFED = deadtime_f;
284
285
286 }
287 void InitEPwm_6()
288 {
289
290     EPwm6Regs.TBPRD = PERIOD;                              // Set timer period
291     EPwm6Regs.TBPHS.bit.TBPHS = ps6;                //
292     EPwm6Regs.TBCTR = 0x0000;                           // Clear counter
293
294     // Setup TBCLK
295     EPwm6Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count up
296     EPwm6Regs.TBCTL.bit.PHSEN = TB_ENABLE;        // Enable phase loading
297     EPwm6Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio to SYSCLKOUT
298     EPwm6Regs.TBCTL.bit.CLKDIV = TB_DIV1;          // Same frequency as main
    clock
299     EPwm6Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;       // pass sync in to sync
    out
300     // Setup compare
301     EPwm6Regs.CMPA.bit.CMPA = PERIOD*main_duty;              // initial 50%
    duty ratio
302
303     // Set actions
304     EPwm6Regs.AQCTLA.bit.CAU = AQ_CLEAR;                // Set PWM3A on Zero
305     EPwm6Regs.AQCTLA.bit.ZRO = AQ_SET;
306
307     // Active high complementary PWMs - Setup the deadband
308     EPwm6Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
309     EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
```

```
310     EPwm6Regs.DBCTL.bit.IN_MODE = DBA_ALL;
311     EPwm6Regs.DBRED.bit.DBRED = deadtime_r;
312     EPwm6Regs.DBFED.bit.DBFED = deadtime_f;
313
314
315 }
316
317 void InitEPwm_7()
318 {
319
320     EPwm7Regs.TBPRD = PERIOD;                                   // Set timer period
321     EPwm7Regs.TBPHS.bit.TBPHS = ps7;                    //
322     EPwm7Regs.TBCTR = 0x0000;                                   // Clear counter
323
324     // Setup TBCLK
325     EPwm7Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count up
326     EPwm7Regs.TBCTL.bit.PHSEN = TB_ENABLE;          // Enable phase loading
327     EPwm7Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;        // Clock ratio to SYSCLKOUT
328     EPwm7Regs.TBCTL.bit.CLKDIV = TB_DIV1;           // Same frequency as main
    clock
329     EPwm7Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;       // pass sync in to sync
    out
330     // Setup compare
331     EPwm7Regs.CMPA.bit.CMPA = PERIOD*main_duty;                 // initial 50%
    duty ratio
332
333     // Set actions
334     EPwm7Regs.AQCTLA.bit.CAU = AQ_CLEAR;                // Set PWM3A on Zero
335     EPwm7Regs.AQCTLA.bit.ZRO = AQ_SET;
336
337     // Active high complementary PWMs - Setup the deadband
338     EPwm7Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
339     EPwm7Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
340     EPwm7Regs.DBCTL.bit.IN_MODE = DBA_ALL;
341     EPwm7Regs.DBRED.bit.DBRED = deadtime_r;
342     EPwm7Regs.DBFED.bit.DBFED = deadtime_f;
343
344
345 }
346
347
348 __interrupt void cpu_timer0_isr(void)
349 {
```

```
350     index++;
351
352
353
354 #ifndef CONST_DUTY
355 //   if (index<=num_points/2){
356 //       main_duty = 1 -  __sinpuf32(argument);
357 //   }
358 //   else {
359 //       main_duty = 1 + __sinpuf32(argument);
360 //   }
361
362 //   main_duty = 0.5*(1+__sinpuf32(argument));
363     float argument=step*index;
364     main_duty = 0.5+(0.45*(__sinpuf32(argument)));
365     if (main_duty < .002){
366         main_duty = .002;
367     }
368 #endif
369
370
371
372     int32 duty = PERIOD*main_duty;
373     EPwm7Regs.CMPA.bit.CMPA = duty;
374     EPwm6Regs.CMPA.bit.CMPA = duty;                    // update duty ratio in
    ePWMs
375     EPwm5Regs.CMPA.bit.CMPA = duty;
376     EPwm4Regs.CMPA.bit.CMPA = duty;
377     EPwm3Regs.CMPA.bit.CMPA = duty;
378     EPwm2Regs.CMPA.bit.CMPA = duty;
379     EPwm1Regs.CMPA.bit.CMPA = duty;
380
381
382     if (index == 1){
383         GpioDataRegs.GPACLEAR.bit.GPIO0 = 1;             // Unfolder Vout_gnd
    connects to ground
384         GpioDataRegs.GPASET.bit.GPIO1 = 1;            // Unfolder Vout_gnd
    connects to ground
385     }
386
387 #ifndef CONST_DUTY
388     if (index==num_points/2){
```

```
389             GpioDataRegs.GPASET.bit.GPIO0 = 1;                  // Unfolder Vout_gnd
    connectes to Vin
390             GpioDataRegs.GPACLEAR.bit.GPIO1 = 1;                    // Unfolder
    Vout_gnd connectes to Vin
391         }
392 #endif
393
394         if (index == num_points){
395             index = 0;
396         }
397
398 #ifdef ENHANCED_BALANCING
399
400 #endif
401         // Clear interrupt flag
402         PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
403 }
```

APPENDIX C

SCHEMATICS

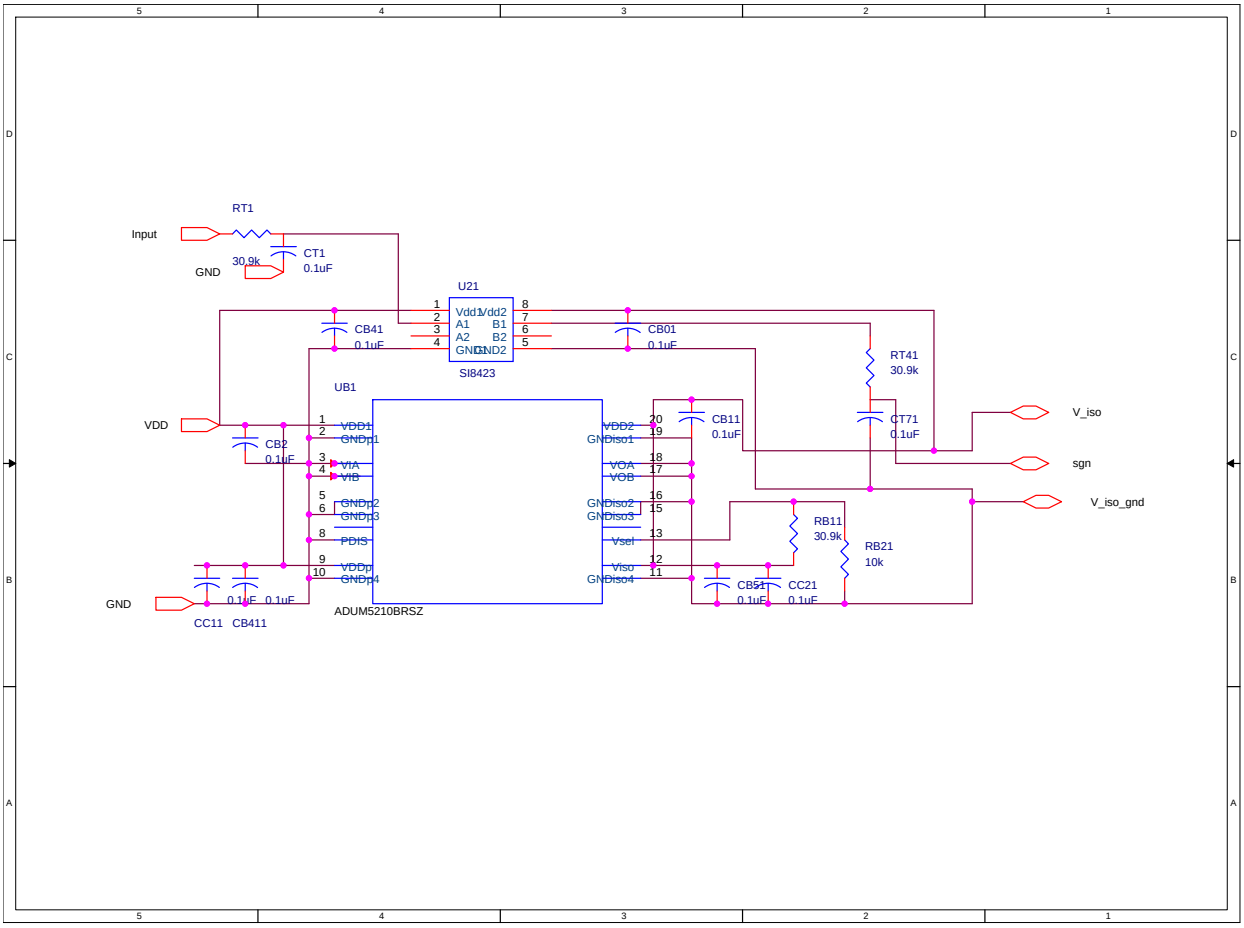


Figure C.1: Schematic of the power and signal isolation block.

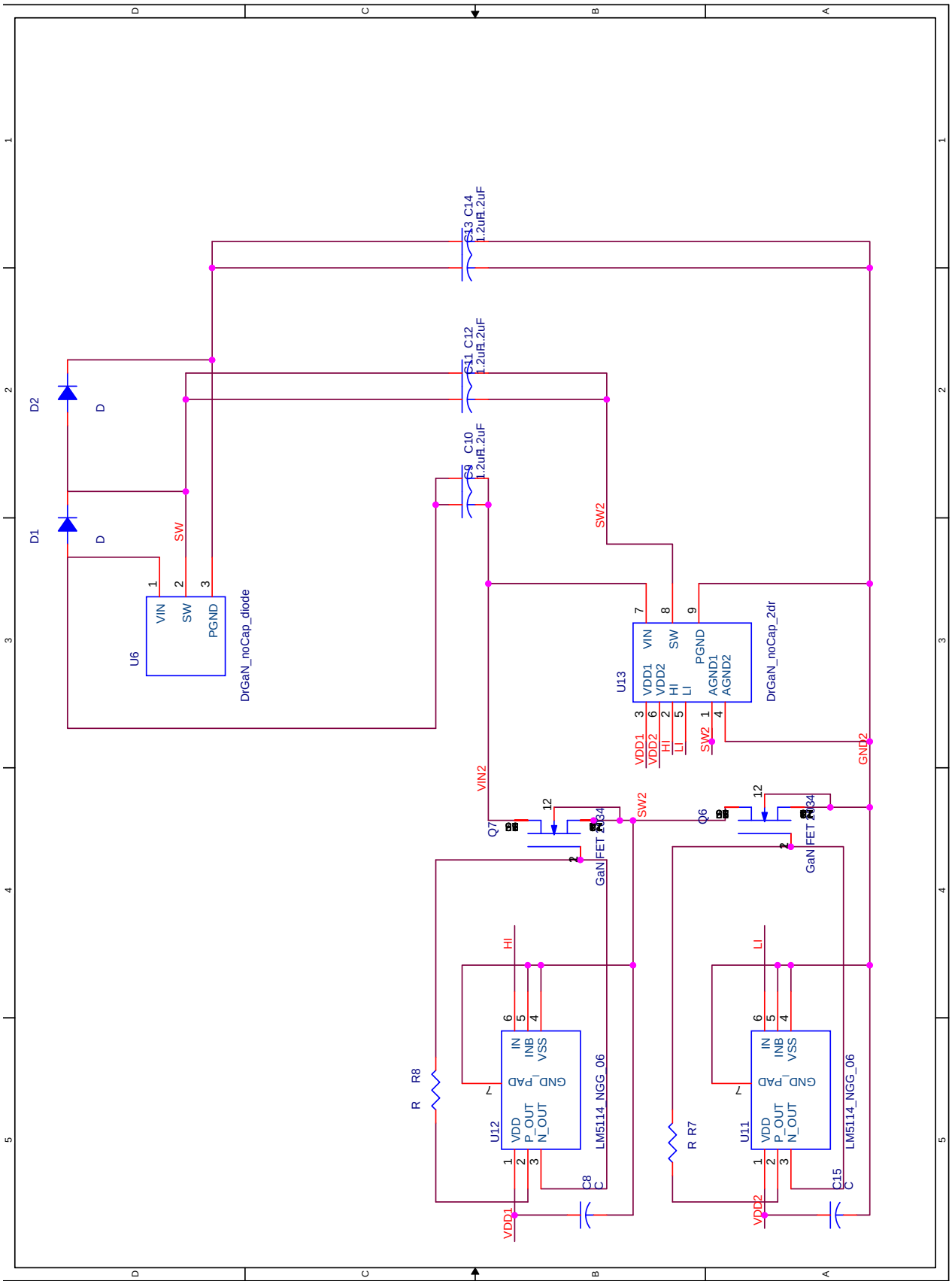


Figure C.2: Schematic of the switching cell.

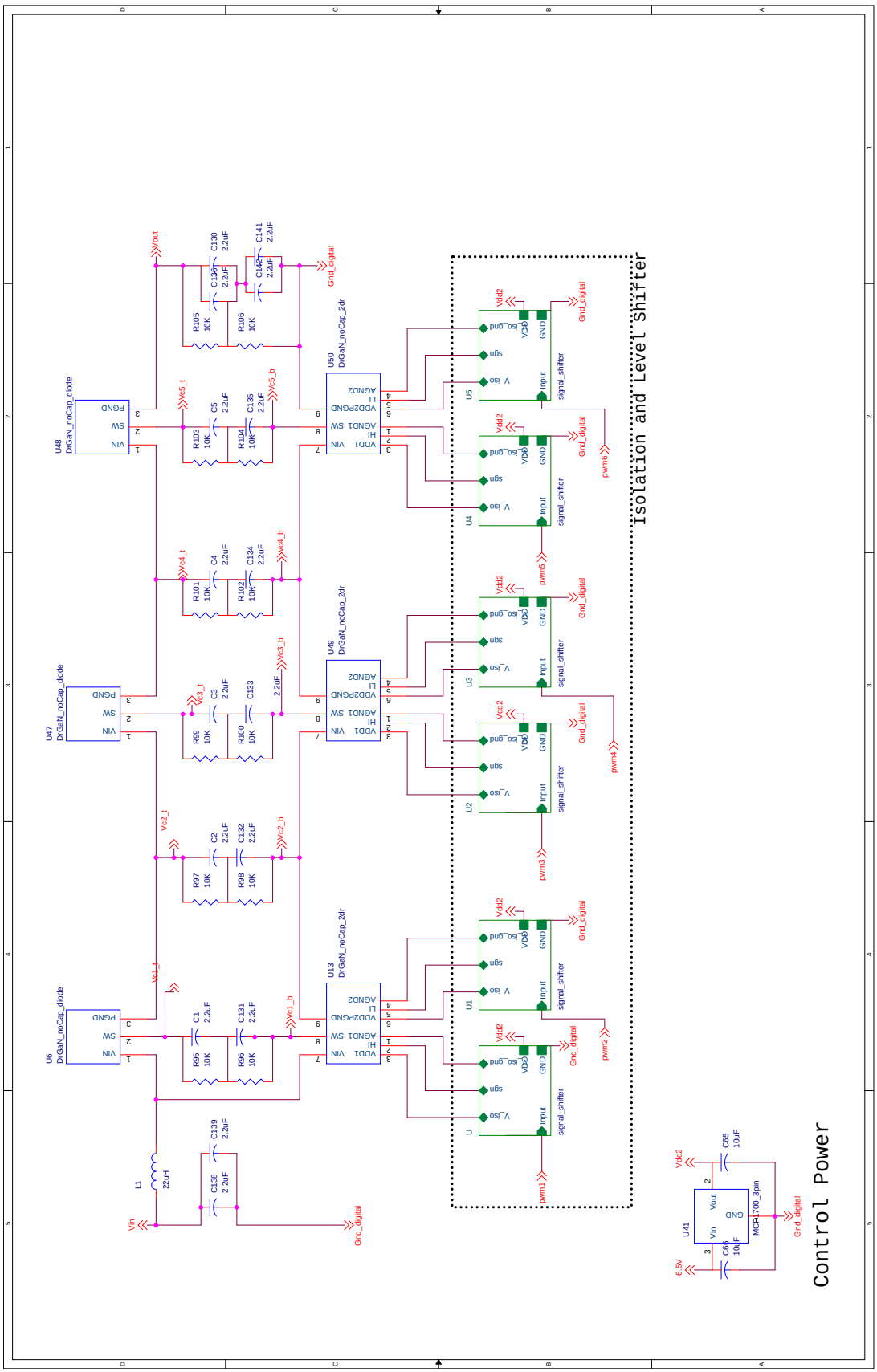


Figure C.3: Schematic of the main power converter board.

APPENDIX D

PCB LAYOUT

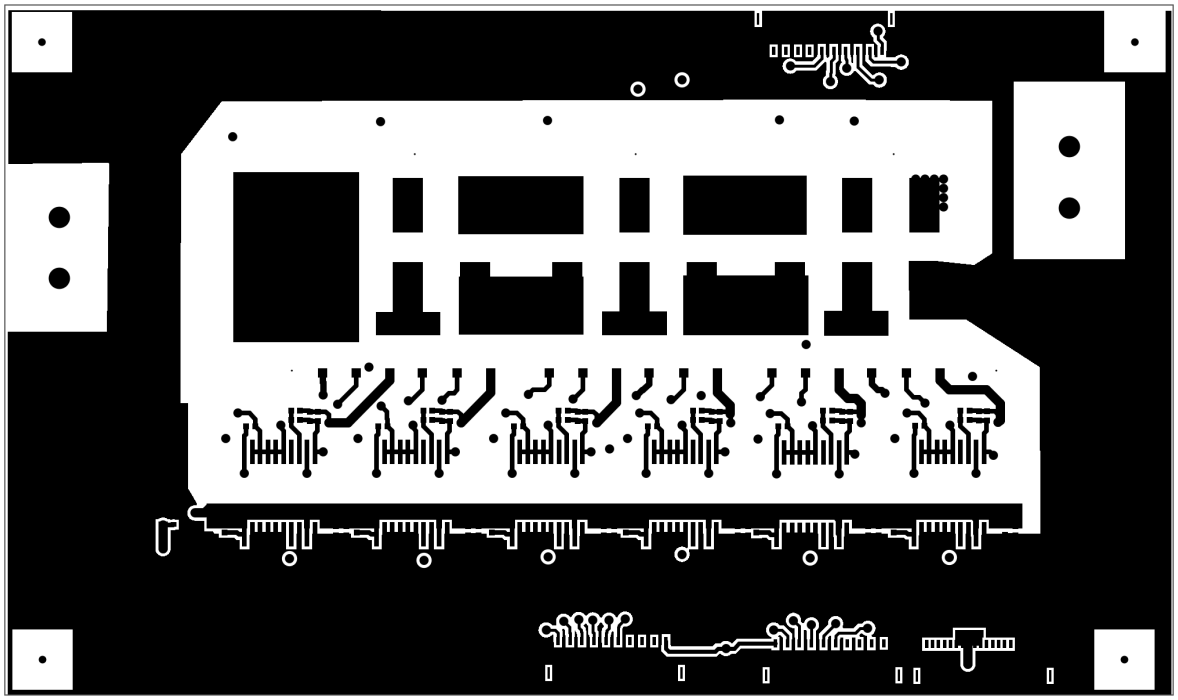


Figure D.1: Top layer of the main power converter board.

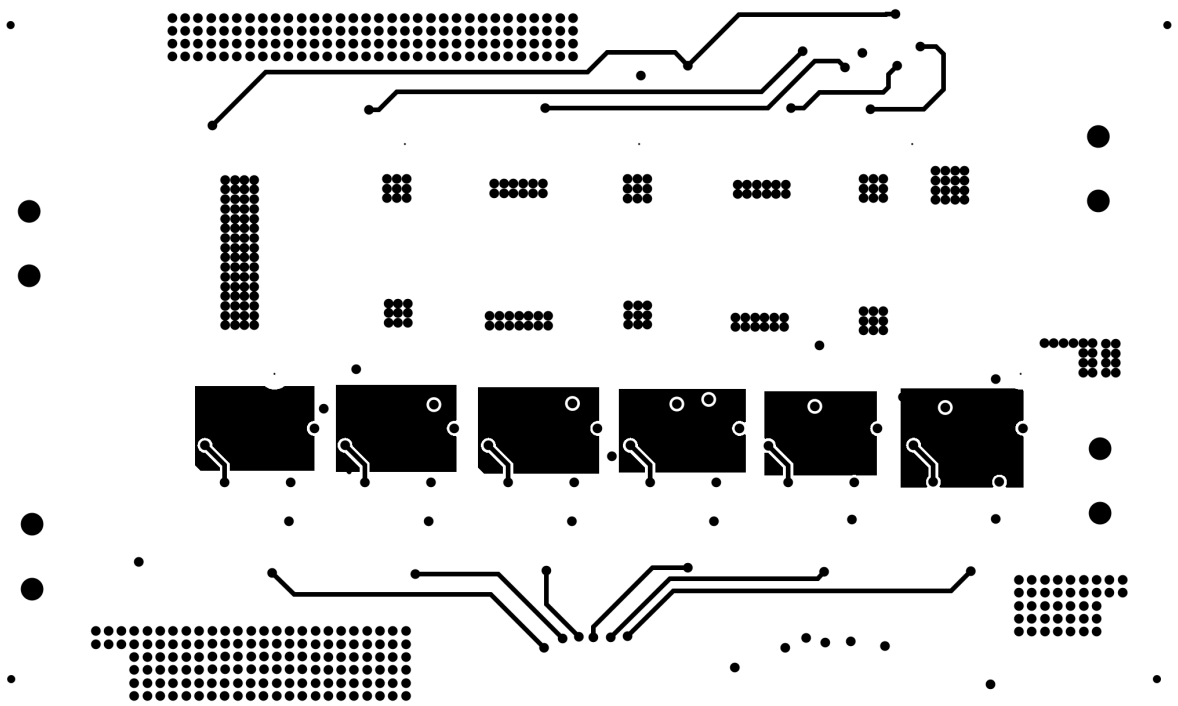


Figure D.2: Inner layer 1 of the main power converter board.

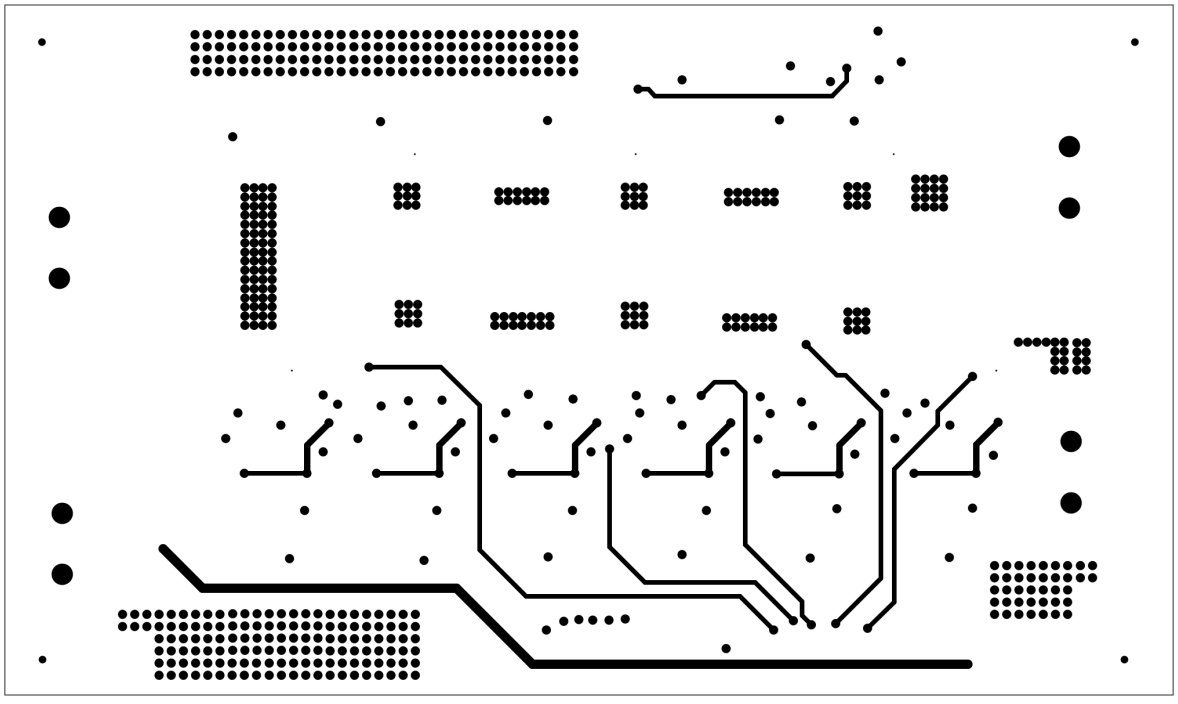


Figure D.3: Inner layer 2 of the main power converter board.

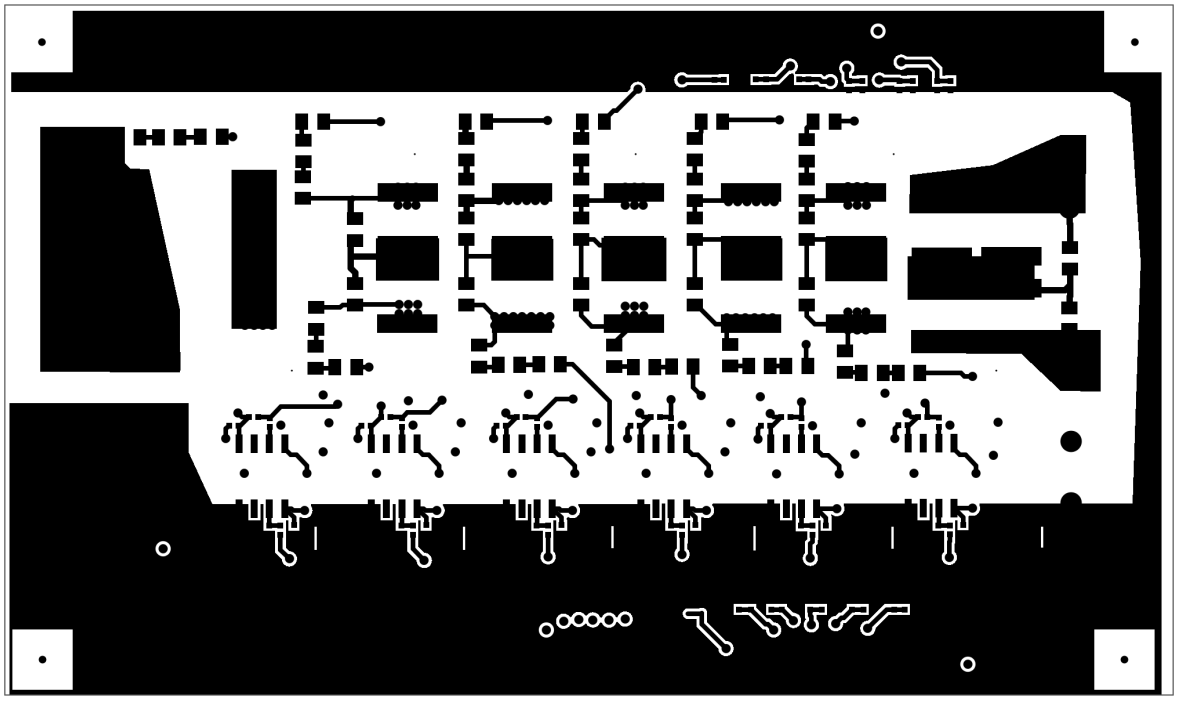


Figure D.4: Bottom layer of the main power converter board.

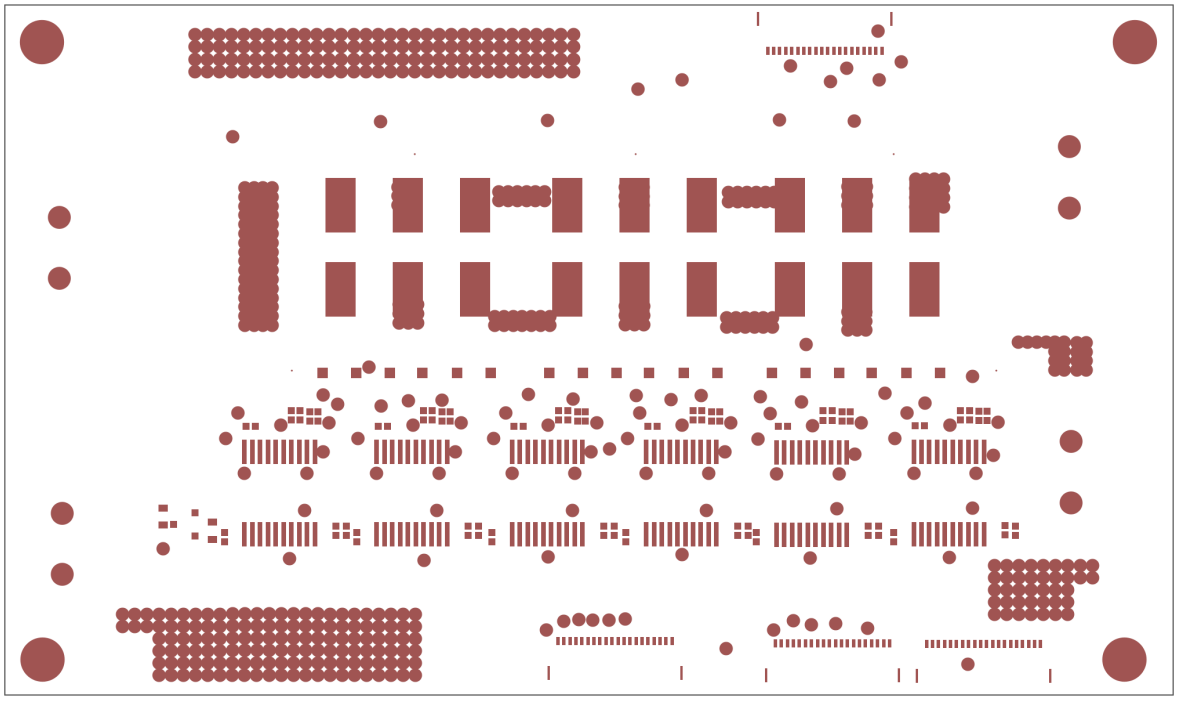


Figure D.5: Top solder mask of the main power converter board.

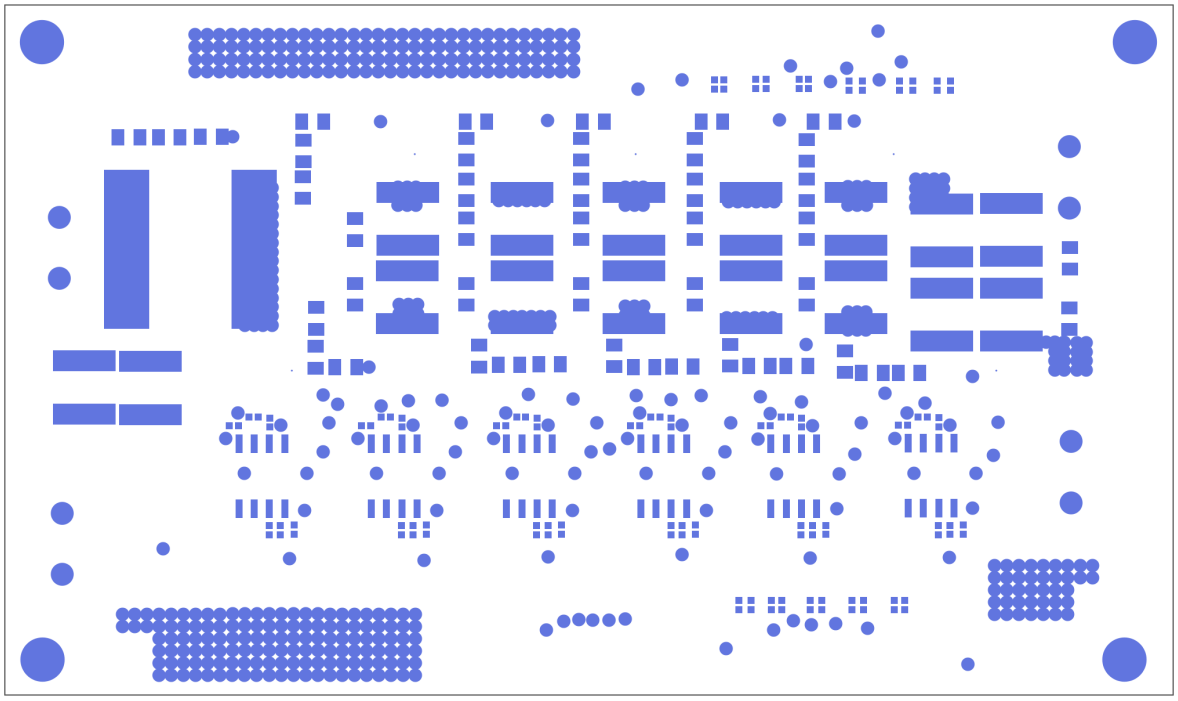


Figure D.6: Bottom solder mask of the main power converter board.

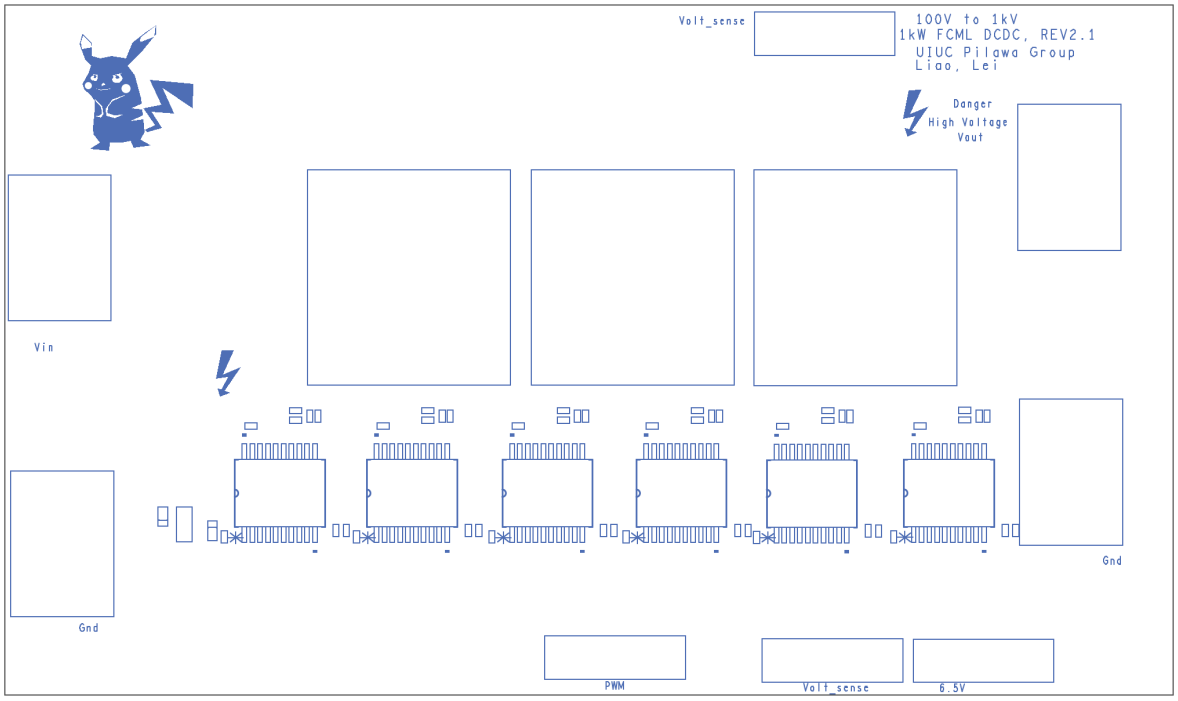


Figure D.7: Top silkscreen of the main power converter board.

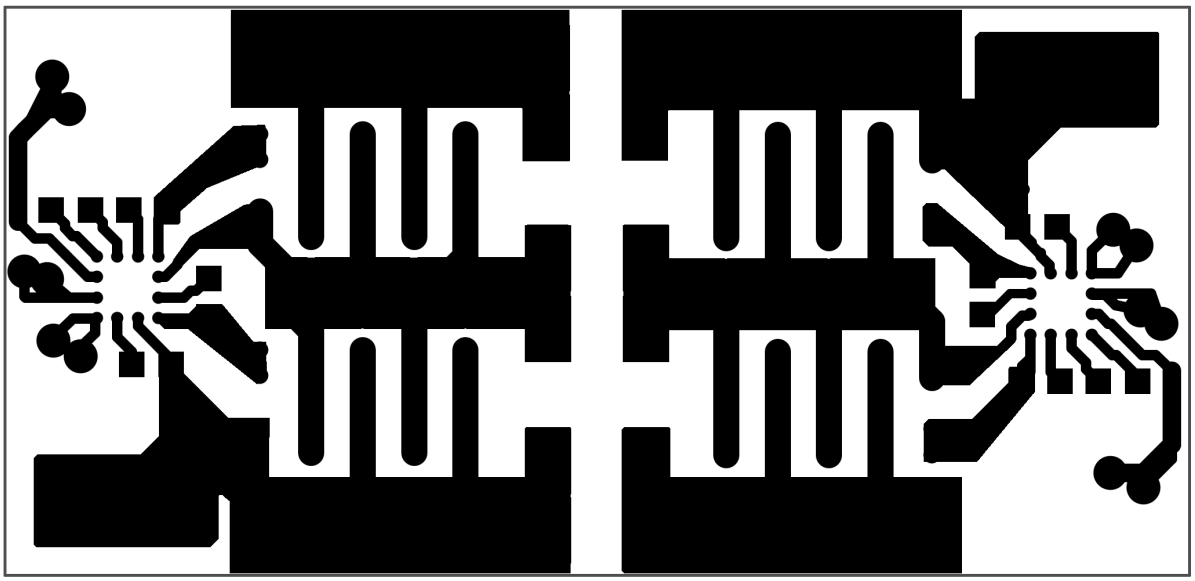


Figure D.8: Top layer of the switching cell daughter board.

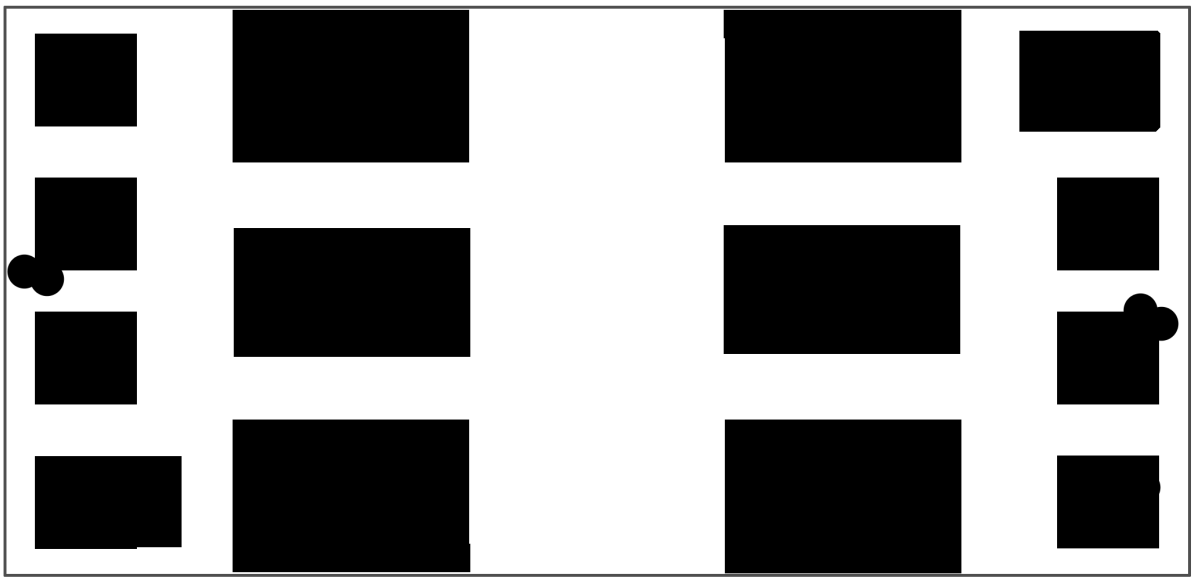


Figure D.9: Bottom layer of the switching cell daughter board.

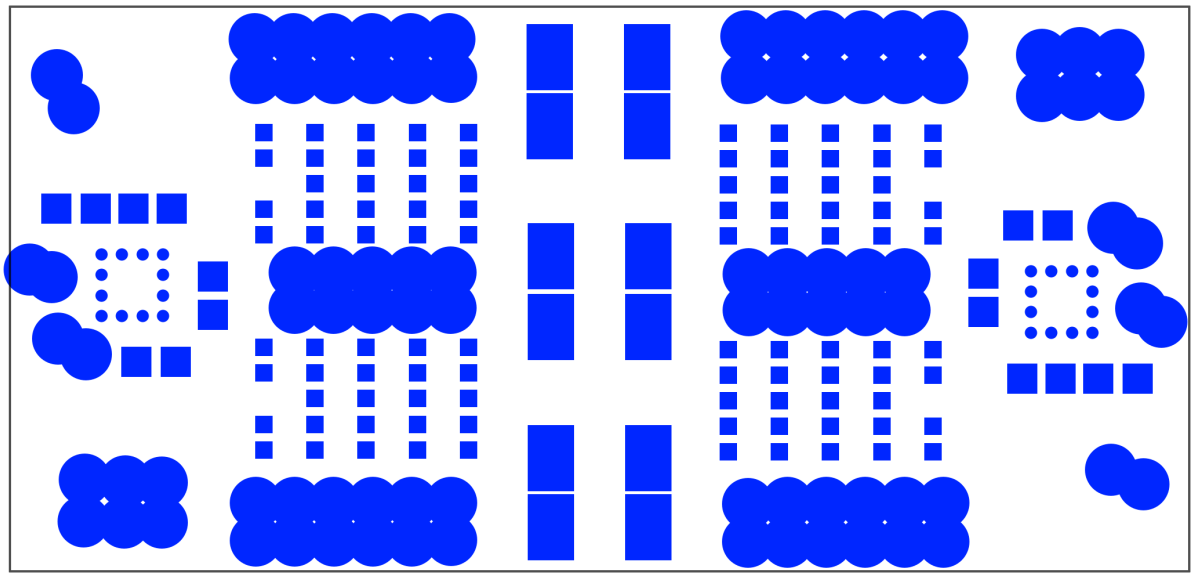


Figure D.10: Top silkscreen of the switching cell daughter board.

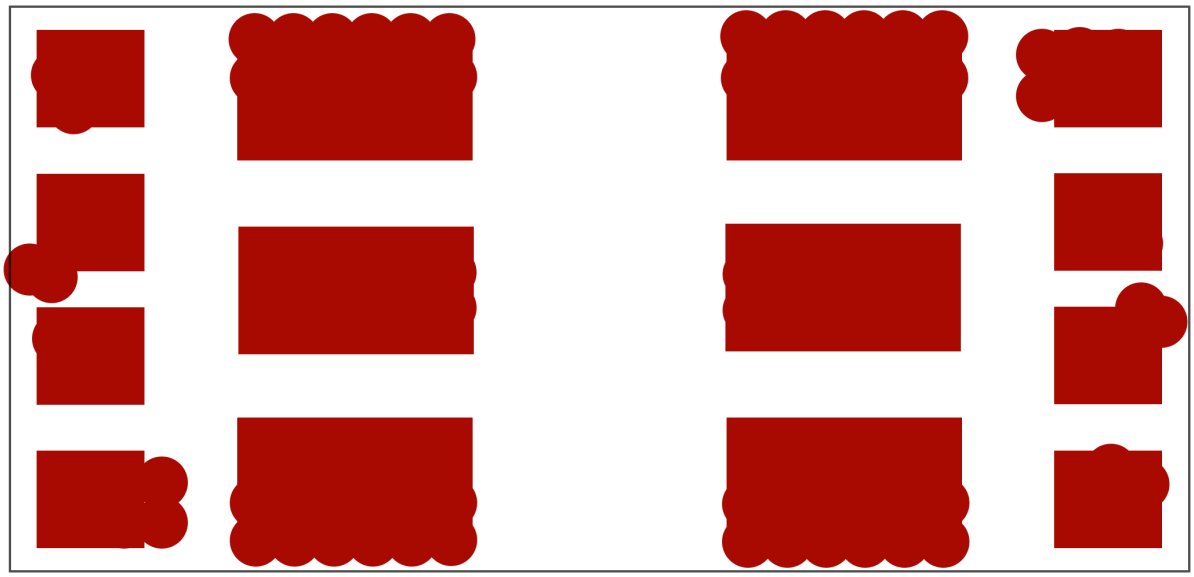


Figure D.11: Bottom solder mask of the switching cell daughter board.

APPENDIX E

HIGH VOLTAGE SAFETY BOX

The high voltage safety box is designed in SolidWorks. Then the panels were cut out of a 3/8 ” acrylic board with the laser cutter in the Open Lab.

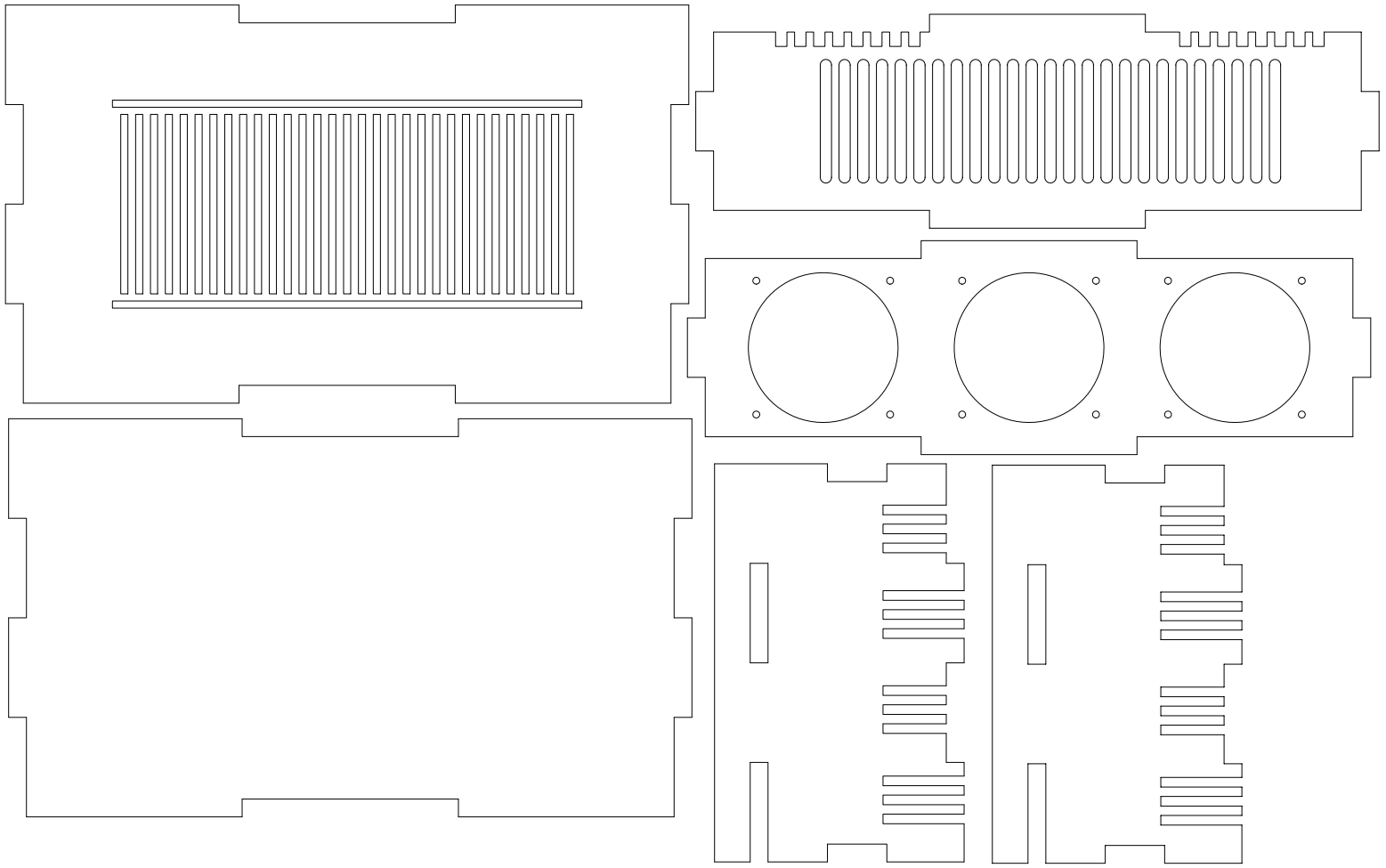


Figure E.1: Mechanical drawing of the high voltage safety box in solidworks.

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