SUCCESSIVE-APPROXIMATION-REGISTER BASED QUANTIZER DESIGN FOR HIGH-SPEED DELTA-SIGMA MODULATORS

BY

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THESIS

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ABSTRACT

High-speed delta-sigma modulators are in high demand for applications such as wire-line and wireless communications, medical imaging, RF receivers and high-definition video processing. A high-speed delta-sigma modulator requires that all components of the delta-sigma loop operate at the desired high frequency. For this reason, it is essential that the quantizer used in the delta-sigma loop operate at a high sampling frequency. This thesis focuses on the design of high-speed time-interleaved multi-bit successive-approximation-register (SAR) quantizers. Design techniques for high-speed medium-resolution SAR analog-to-digital converters (ADCs) using synchronous SAR logic are proposed.

Four-bit and 8-bit 5 GS/s SAR ADCs have been implemented in 65 nm CMOS using 8-channel and 16-channel time-interleaving respectively. The 4-bit SAR ADC achieves SNR of 24.3 dB, figure-of-merit (FoM) of 638 fJ/conversion-step and 42.6 mW power consumption, while the 8-bit SAR ADC achieves SNR of 41.5 dB, FoM of 191 fJ/conversion-step and 92.8 mW power consumption. High-speed operation is achieved by optimizing the critical path in the SAR ADC loop. A sampling network with a split-array with unit bridge capacitor topology is used to reduce the area of the sampling network and switch drivers.

To Mom, Dad and Pooja.

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LIST OF ABBREVIATIONS

$\Delta\Sigma$	Delta-Sigma
ADC	Analog-to-Digital Converter
A/D	Analog-to-Digital
CIFB	Cascade of integrators with distributed feedback and distributed input coupling
CML	Current-Mode-Logic
CMOS	Complementary metal-oxide semiconductor
CRFB	Cascade of resonators with distributed feedback and distributed input coupling
D/A	Digital-to-Analog
DAC	Digital-to-Analog Converter
DFF	D Flip-flop
DFFR	D Flip-flop with asynchronous reset
DFFS	D Flip-flop with asynchronous set
DFFSR	D Flip-flop with asynchronous set-reset
DLL	Delay-locked Loop
FFT	Fast Fourier Transform
FoM	Figure-of-merit
LSB	Least Significant Bit
MOD1	First-order Delta Sigma Modulator
MOD2	Second-order Delta Sigma Modulator

MOD5	Fifth-order Delta Sigma Modulator
MPCG	Multi-phase Clock Generator
NTF	Noise Transfer Function
OpAmp	Operational Amplifier
OSR	Oversampling Ratio
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SQNR	Signal-to-Quantization Noise Ratio
STF	Signal Transfer Function
TI	Time-interleaved

CHAPTER 1

INTRODUCTION

1.1 Motivation

Analog-to-digital converters form the basis of any signal processing system that interacts with the real world. Advances in design of signal processing systems such as wireless and wireline communications, software defined radio, Ethernet and high-definition video processing have been made possible through advances in designs of analog-to-digital converters. In recent years the increased demand for higher bandwidths of analog-to-digital converters (ADCs) has spurred further research in developing high-speed ADCs [2],[3],[4].

High-speed delta-sigma modulators are in high demand in applications such as wire-line and wireless communications, medical imaging and RF receivers [2],[3],[4]. A high-speed delta-sigma modulator requires that all components of the delta-sigma loop are able to operate at the desired high frequency. For this reason, it is essential that the quantizer used in the delta-sigma loop is able to operate at a high sampling frequency.

In this thesis we focus on the design of a high-speed time-interleaved multi-bit successive approximation based quantizer designed to operate at a sampling rate of 5GS/s. High-speed quantizers with 4-8 bit precision operating in the GHz range are nearly impossible to build using a single channel. Therefore, time-interleaved ADCs consisting of several slow sub-ADCs are needed to achieve such high sample rates, thereby increasing the total area. Successive-approximation-register (SAR) based ADCs are ideal for this application as they consist of mainly digital components that benefit from technology scaling in low-voltage CMOS processes and thus provide a high speed-to-area ratio [5]. A SAR quantizer can also provide better performance compared to other quantizers when used in a delta-sigma loop by providing

an extra order of noise-shaping. The successive approximation process generates a residue voltage on the charge re-distribution capacitor that can be exploited as the quantization error required for the delta-sigma modulator [6],[7].

1.2 Outline

This thesis is organized into seven chapters. Chapter 2 provides an introduction to analog-to-digital converters (ADC) and describes some key concepts used in the thesis. Chapter 3 provides a brief introduction the delta-sigma modulation and explains the working of some commonly used delta-sigma modulators. Chapter 4 presents the SIMULINK implementations of a first-, second- and fifth-order delta-sigma modulator. Chapters 5, 6 and 7 form the heart of this thesis. Chapter 5 explains the design of the 8-channel time-interleaved 4-bit 5GS/s successive approximation register (SAR) based ADC implemented in 65 nm CMOS. Chapter 6 provides an analysis of the critical contributors to delays in the SAR ADC loop. Chapter 7 discusses the architecture of the proposed 16-channel time-interleaved 8-bit 5GS/s ADC and optimum choices to be made while designing high-speed medium-resolution SAR ADCs. Finally, we conclude the thesis in chapter 8. Simulink models of the delta-sigma modulators implemented and transistor-level schematics of the SAR ADCs have been included in the appendices.

CHAPTER 2

DATA CONVERTERS OVERVIEW

Analog-to-digital converters (ADCs) are at the heart of any electronic system that interacts with the real world. The real world we live in is made of analog signals such as speech, medical imaging, sonar, radar, etc., i.e. signals that are continuously varying with time [8]. An analog-to-digital converter converts analog signals to digital signals, i.e. signals that exist for discrete instances of time and that have only certain discrete values. In this way an ADC enables us to convert an infinite signal into a finite signal without loss of significant information, enabling us to process this finite data for various applications. Analog-to-digital converters are critical to signal processing systems such as RF receivers, Ethernet, wireless communication, software-defined radio etc.

This chapter briefly explains the process of analog-to-digital conversion, some commonly used terminology in ADC design as well as the metrics used to evaluate the performance of an ADC. This chapter also describes two different types of commonly used data converters and explains the architecture of different ADCs and digital-to-analog converters (DACs).

2.1 Terminologies

2.1.1 Analog Signal

An analog signal is a signal that can take any value and is defined for all instances of time (t). An analog signal can have infinite values and infinite precision [9]. An analog signal is also known as a continuous-time analog signal.

2.1.2 Discrete-time Signal

A discrete-time signal is a signal that can take any value but is defined only for discrete instances of time (n) [9].

2.1.3 Digital Signal

A digital signal is a signal that is discrete in terms of both time and amplitude. That is, it exists only for discrete instances of time and can only take discrete values of the form $k\Delta$, where k is an integer and Δ is a fixed value.

2.2 Sampling

Sampling is the process of discretization of time, by which a continuous-time analog signal is converted into a discrete-time signal. Sampling enables us to represent a signal consisting of infinitely many points using a finite number of points, and thereby store the data in finite-memory devices such as computers and other electronics. The original signal can be perfectly reconstructed from a sampled signal as long as the sampling criterion given by (2.1) is satisfied. The sampling criterion states that a band-limited signal can be perfectly reconstructed as long as the sample rate (f_s) is twice its bandwidth (f_b). This is known as the Shannon-Nyquist sampling theorem.

$$f_s \geq 2 \times f_b \tag{2.1}$$

Sampling is usually the first stage in the analog-to-digital conversion process. The amplitude of the continuous-time signal is first sampled onto a capacitor after which it is quantized using a quantizer.

2.3 Quantization

The process of analog-to-digital conversion of a continuous-time signal can be decomposed into two main parts - quantization of time, better known as sampling, and quantization of the amplitude of the time-varying signal, commonly known as quantization. Quantization is the process by which a

sampled value can be represented by a binary word of a fixed length [10]. A quantizer maps a large set of input values to a smaller set [11]. Quantization is thus basically just the process of approximating an input value. The accuracy with which the quantized value matches the original input depends on the precision of the quantizer, i.e., its number of levels. The number of levels in a quantizer is usually defined as a power of 2, thus a B-bit quantizer consists of 2^B levels. The quantized value is usually represented by a digital code in binary as a one's or two's complement number. Quantization can be of two types based on the number of quantization levels – midtread quantization or midrise quantization. These are explained in detail in sections 2.3.2 and 2.3.1.

The approximating nature of quantization degrades the input signal. The difference between the quantized sample, $v[n]$, and the input sample, $u[n]$, is known as the *quantization error* or *quantization noise*, $e[n]$.

$$e[n] = v[n] - u[n] \tag{2.2}$$

A quantizer can thus be represented by its additive noise model (Fig. 2.1) where the quantized output, $v[n]$, is given by (2.3) [11].

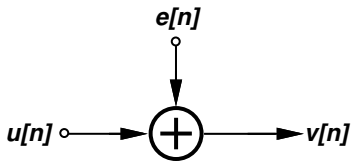


Figure 2.1: Additive Noise Model of a Quantizer

$$v[n] = u[n] + e[n] \tag{2.3}$$

The statistical model of a quantizer assumes that the quantization noise is a sample sequence of a wide-sense stationary white noise process, i.e. it is uncorrelated with the input and the probability distribution of the quantization error is uniform [11]. These assumptions of the statistical model are only valid when the quantizer is not overloaded, the input signal is complex and the quantization steps are small [11].

A quantizer is said to be overloaded when the input exceeds the full-scale range, (R_{fs}), of the quantizer. The full-scale range of a quantizer is predefined by its circuit design. The input is usually scaled down to ensure that it is within the full scale range of the quantizer, given by (2.4), where V_{ref} is a chosen reference voltage.

$$R_{fs} = 2 \times V_{ref} \tag{2.4}$$

The smallest quantization level or minimum step-size, Δ, of a B bit quantizer is given by (2.5). This is also commonly referred to as the least-significant bit (LSB) since a change in the input corresponding to Δ changes the LSB of the binary coded output [10].

$$\Delta = \frac{R_{fs}}{2^B} = \frac{2V_{ref}}{2^B} = \frac{V_{ref}}{2^{B-1}} \tag{2.5}$$

The quantization error, $e[n]$, of a quantizer with step-size Δ is bounded by (2.6) as long as the input is within the full-scale range of the quantizer. When the input is outside the full-scale range of the quantizer the quantization error increases linearly with magnitude of the input and the quantized output is clipped to the maximum quantization level [11].

$$-\frac{\Delta}{2} \leq e[n] \leq \frac{\Delta}{2} \tag{2.6}$$

Since the quantization error, e[n], is assumed to be a white noise process it has a uniform probability distribution. The probability distribution of e[n] shown in Fig. 2.2 is given by (2.7).

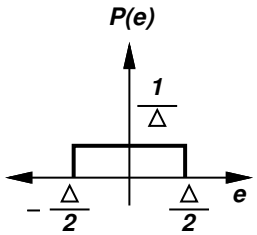


Figure 2.2: Probability Distribution of e[n]

$$P(e[n]) = \begin{cases} \frac{1}{\Delta} & -\frac{\Delta}{2} \leq e[n] \leq \frac{\Delta}{2} \\ 0 & else \end{cases} \tag{2.7}$$

The quantization noise power of the quantization error is given by its variance given by (2.8).

$$\begin{aligned} P_e &= \int_{-\infty}^{\infty} e^2 \cdot P(e)\ de \\ &= \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} \frac{e^2}{\Delta}\ de \\ &= \frac{\Delta^2}{12} \end{aligned} \tag{2.8}$$

Since the quantization error sequence is white, power spectral density[1], $S_e(\omega)$, is white as well, i.e. it is uniformly distributed over all frequencies and its power is within $\pm\pi$. The height of the one-sided power spectral density, k_e, of the quantization noise can be found from its noise power and is given by (2.10) [12].

$$P_e = \int_0^{\pi} S_e^2(\omega)\ d\omega = \pi k_e^2 = \frac{\Delta^2}{12} \tag{2.9}$$

$$k_e = \frac{\Delta}{\sqrt{12\pi}} \tag{2.10}$$

Therefore, the one-sided power spectral density of the quantization error, $S_e(\omega)$, is given by (2.11).

$$S_e(\omega) = \begin{cases} \frac{\Delta}{\sqrt{12\pi}} & 0 \leq \omega \leq \pi \\ 0 & else \end{cases} \tag{2.11}$$

2.3.1 Mid-rise Quantization

Mid-rise quantization is used when the number of levels in the required quantizer is even, i.e. it can be represented as a power of 2. Analytically, the

[1]The discrete-time angular frequency $\omega = \Omega T_s = 2\pi \frac{f}{f_s}$, where Ω – the continuous-time angular frequency, f_s – the sampling frequency and f – the continuous-time frequency.

output of a mid-rise quantizer, v[n], can be represented in terms of the input to the quantizer, $u[n]$, and the quantization step-size Δ by (2.12) [10].

$$v[n] = \Delta \left\lfloor \frac{u[n]}{\Delta} + \frac{1}{2} \right\rfloor \tag{2.12}$$

Figure 2.3 shows the number line from $-V_R$ to V_R with the ADC comparator threshold voltages and DAC output voltages marked for a 4-level (i.e. 2-bit) mid-rise quantizer. Here, V_R is the reference voltage of the quantizer.

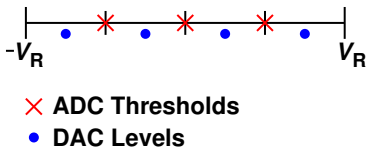


Figure 2.3: ADC Comparator Thresholds and DAC Output Levels for a 4-level Mid-rise Quantizer

2.3.2 Mid-tread Quantization

Mid-tread quantization is used when the number of levels in the required quantizer is odd. Analytically, the output of a mid-tread quantizer, v[n], can be represented in terms of the input to the quantizer, $u[n]$, and the quantization step-size Δ by (2.13) [10].

$$v[n] = \Delta \left\lfloor \frac{u[n]}{\Delta} \right\rfloor + \frac{\Delta}{2} \tag{2.13}$$

Figure 2.4 shows the number line from $-V_R$ to V_R with the ADC comparator threshold voltages and DAC output voltages marked for a 5-level mid-tread quantizer. Here, V_R is the reference voltage of the quantizer.

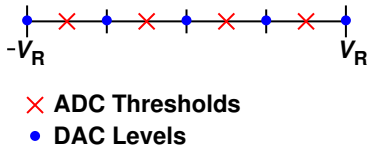


Figure 2.4: ADC Comparator Thresholds and DAC Output Levels for a 5-level Mid-tread Quantizer

2.4 Performance Metric of Data Converters

2.4.1 Signal-to-Quantization Noise Ratio

The performance of an ADC is measured by comparing the power due to the input signal content and the power due to the noise content in the quantized output. The ratio of the signal power to the quantization noise power is known as the signal-to-quantization noise Ratio (SQNR). The SQNR of a signal is usually expressed in decibels (dB). The power of a sine wave of full-scale amplitude $A = V_{ref}$ is given by (2.14) while the power of the quantization noise is given by (2.8).

$$P_{sig} = \frac{A^2}{2} = \frac{V_{ref}^2}{2} = \frac{2^{B-1}\Delta^2}{2} \tag{2.14}$$

The SQNR of the output signal of a uniform B bit quantizer with input power P_{sig} and quantization noise power P_e is given by (2.15). Thus, it can be seen that the SQNR increases by 6 dB per bit.

$$\begin{aligned} SQNR &= 10\ log_{10}\left(\frac{P_{sig}}{P_e}\right) \\ &= 6.02B + 1.76\ \text{[dB]} \end{aligned} \tag{2.15}$$

2.4.2 Spurious-Free Dynamic Range

The performance of an analog-to-digital converter is also commonly measured using its spurious-free dynamic range (SFDR). The SFDR of a signal is the ratio of the power due to its input signal to the power of the largest distortion component (known as a spurious tone or spur) in the spectrum. The SFDR of a signal is given by (2.16).

$$SFDR = 10\ log_{10}\left(\frac{P_{sig}}{P_{spur}}\right) \tag{2.16}$$

The SFDR of a uniform B bit quantizer for a sinusoidal input can be approximated using (2.17) [13].

$$SFDR = 8.07B + 3.29 \text{ [dB]} \tag{2.17}$$

2.5 Types of Data Converters

Data converters (ADCs and DACs) are categorized into two broad categories, Nyquist-rate converters or oversampling converters, based on the relationship between the frequency of the input signal, f_{in}, and the sampling rate of the data converter, f_s.

2.5.1 Nyquist-rate Converters

Data converters in which the input signal is sampled at a frequency close to the Nyquist-rate are known as Nyquist-rate converters. Usually, Nyquist-rate converters operate at 1.5 to 10 times the Nyquist-rate [12]. The quantization error in Nyquist-rate converters has a flat-band spectrum, i.e. the quantization noise is uniformly distributed among all frequencies.

2.5.2 Oversampling Converters

Oversampling converters are data converters that operate at a much higher frequency than the Nyquist-rate of the input signal. Oversampling converters are used when the input signal is bandlimited, i.e. all signals of interest are below some frequency, f_b, known as the bandwidth of the input signal. The oversampling ratio of a data converter is given by (2.18).

$$OSR = \frac{f_s}{2f_b} \tag{2.18}$$

Oversampling converters operate at oversampling ratios (OSR) of about 10 to 512. Oversampling converters are used to increase the SNR of the output of an ADC. The input is first sampled and quantized at a rate much higher than the Nyquist-rate. A high sampling frequency, f_s, causes the quantization noise to be spread over a larger frequency range (0 to $f_s/2$). Since all signals of interest are below f_b, the signals and quantization noise

outside the signal's bandwidth are then filtered out using a digital or analog filter [12]. This elimination of the out-of-band quantization noise improves the SNR of the output signal. If the filter used is a brick wall filter with transfer function, $H(\omega)$, given by (2.19), the new quantization noise power, P_e, of the filtered signal is given by (2.20) [12].

$$|H(\omega)| = \begin{cases} 1 & -\frac{\pi}{OSR} \leq \omega \leq \frac{\pi}{OSR} \\ 0 & else \end{cases} \tag{2.19}$$

$$P_e = \int_0^{\frac{\pi}{OSR}} S_e^2(\omega) \cdot |H(\omega)|^2 \, d\omega = \frac{\Delta^2}{12}\left(\frac{1}{OSR}\right) \tag{2.20}$$

Therefore, the SQNR of a B-bit oversampling converter for a sine input is given by (2.21).

$$\begin{aligned} SQNR &= 10 \, log_{10}\left(\frac{P_{sig}}{P_e}\right) \\ &= 6.02B + 1.76 + 10 \, log(OSR) \text{ [dB]} \end{aligned} \tag{2.21}$$

Increasing the OSR by two times gives a 3 dB improvement in SNR or, equivalently, improves the performance by 0.5 bits [12]. Most commonly, the SNR of oversampling converters is further improved by reducing the in-band quantization noise using noise-shaping as in delta-sigma converters. Delta-sigma converters are explained in detail in chapter 3.

2.6 Analog-to-Digital Converter Architectures

In this section, three different types of ADCs — flash ADC, SAR ADC and time-interleaved (TI) ADC — relevant to this thesis are described. The flash ADC is used as the quantizer in the delta-sigma simulink models in chapter 4, while SAR ADCs and TI ADCs are designed in chapters 5 and 7.

2.6.1 Flash Converters

Flash ADCs have the simplest and best architecture for very high-speed analog-to-digital conversion [14],[12]. A flash ADC consists of comparators and a resistor ladder. The input signal is fed to an array of comparators

and compared to a set of known references voltages generated by the resistor ladder. If the input of the comparator is greater than the reference voltage, then its output is set to 1, otherwise it is set to 0. The comparator outputs thus represent the input in a digital thermometer code which can be converted into a binary code using a decoder. Figure 2.5 shows the architecture of a 2-bit flash ADC. The flash converter thus has a very simple structure and can achieve high speeds as the input is processed by comparators in parallel. However, flash converters are not hardware efficient; a flash ADC requires $2^N - 1$ comparators to achieve N-bit resolution [14]. The number of comparators thus grows exponentially with resolution which results in large power consumption and area for resolutions above 8 bits [15].

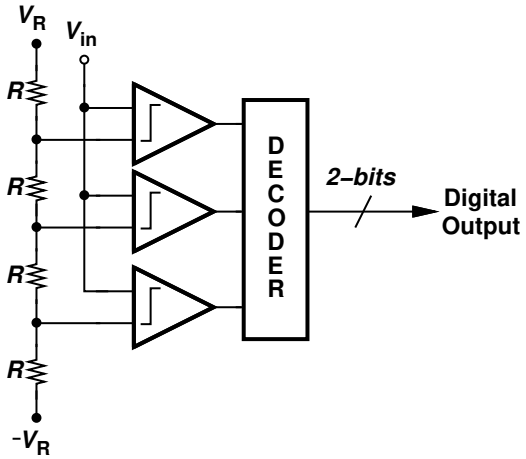


Figure 2.5: A 2-bit Flash ADC

2.6.2 Successive Approximation Converters

Successive approximation converters are widely used in applications where high-accuracy analog-to-digital (A/D) conversion is desired [12]. A basic successive approximation converter consists of a comparator, a successive approximation register (SAR) and a DAC [14]. These converters are commonly known as SAR ADCs. A SAR ADC performs a "binary search" algorithm on the input using a feedback loop. The binary search algorithm uses a divide-and-conquer strategy to find the location of a number in a sorted array. A binary search divides the search space into two each time [12]. Consider an input V_x and a reference voltage V_R. The initial search space consists of all

voltages from 0 to V_R. The algorithm first checks whether $V_x > V_R/2$ or $V_x < V_R/2$. If $V_x > V_R/2$, then the next search space is from $V_R/2$ to V_R; if not, then the next search space is from 0 to $V_R/2$. This process of dividing the search space is performed N times in an N-bit ADC. This algorithm thus brings the quantized output within 1 LSB of the input signal. An N bit SAR ADC requires N clock cycles to complete an N-bit conversion.

Figure 2.6 shows a 4-bit SAR ADC. The working of a SAR ADC consists of two phases: a sampling phase and a bit-cycling phase. During the sampling phase, the input signal is sampled onto the sampling network. A binary weighted capacitive DAC (CDAC) is used as the sampling network in Fig. 2.6. Two other sampling network topologies — split-array with fractional bridge capacitor and split-array with unit bridge capacitor — are explained in sections 2.7.2 and 2.7.3. The sampled value, V_x, is fed as input to the comparator during the bit-cycling phase. The output of the comparator, V_comp, is fed to the successive approximation register (also known as SAR logic block) which sets the value of the desired bit. At the end of the bit-cycling phase the bits $b_4b_3b_2b_1b_0$ are set to the quantized value.

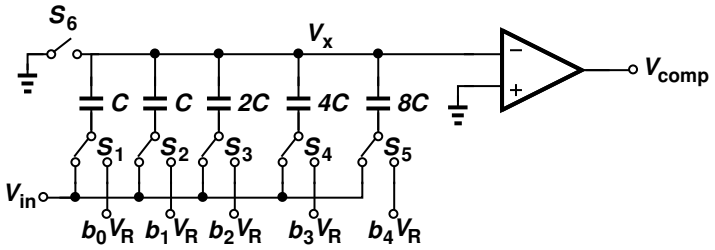


Figure 2.6: 4-bit SAR ADC with Binary Weighted Capacitor Array

During the sampling phase, the switches $S_1 - S_5$ are connected to the input, V_{in}, to sample the input signal onto the CDAC and switch S_6 is closed, grounding the node V_x. The charge on the sampling network during the sampling phase, Q_S, is given by (2.22).

$$Q_S = -16C \times V_{in} \tag{2.22}$$

At the start of the bit-cycling phase the MSB, b_4, is set to 1 while bits $b_3 - b_0$ are set to 0. Switch S_5 is thus connected to the reference voltage, V_R, while the switches $S_1 - S_4$ are connected to ground. During the bit-cycling phase switch S_6 is open. The charge on the sampling network during the

bit-cycling phase, Q_H, is given by (2.23).

$$Q_H = -V_x \times 16C + (V_R - V_x) \times 16C \tag{2.23}$$

By principle of charge conservation the total charge of the sampling network during the two phases remains the same, i.e., $Q_S = Q_H$. Therefore, the voltage on node V_x during the bit-cycling phase is given by (2.24). If $V_{in} > V_R/2$, $V_{comp} = 1$ and b_4 is set to 1, else b_4 is set to one. During the next clock cycle, the b_3 is set to 1 and the value of V_x is re-evaluated to set the value of b_3. This process goes on until all the bits are set.

$$V_x = \frac{V_R}{2} - V_{in} \tag{2.24}$$

SAR ADCs are widely used as they comprise mainly digital components. SAR ADCs thus largely benefit from technology scaling and provide a small-area and low-power solution — attributes that are highly desirable.

2.6.3 Time-interleaved Converters

Very high-speed ADCs can be realized by operating multiple ADCs in parallel where each ADC operates at a much lower speed. The different sub-ADCs operate on different phases of the clock, ensuring that each ADC acts on a different sample. An N-channel time-interleaved ADC consists of N sub-ADCs operating on clock phases separated by $2\pi/N$. Each sub-ADC operates at a frequency of f_s/N. The quantized outputs from each channel are inter-leaved using a multiplexer, giving an output produced at an effective frequency of f_s. Figure 2.7 shows an N-channel time-interleaved ADC and its corresponding clocking sequence.

The performance of a time-interleaved ADC can be highly degraded if there are mismatches among the different channels. Mismatches in timing, gain, and offset can give rise to higher noise power in the output [15]. Mismatches among the different channels can produce inter-modulation products of the input in the output spectrum, thereby increasing the noise in the spectrum. If the source of the mismatches is known, then these can be corrected by digital filtering [12].

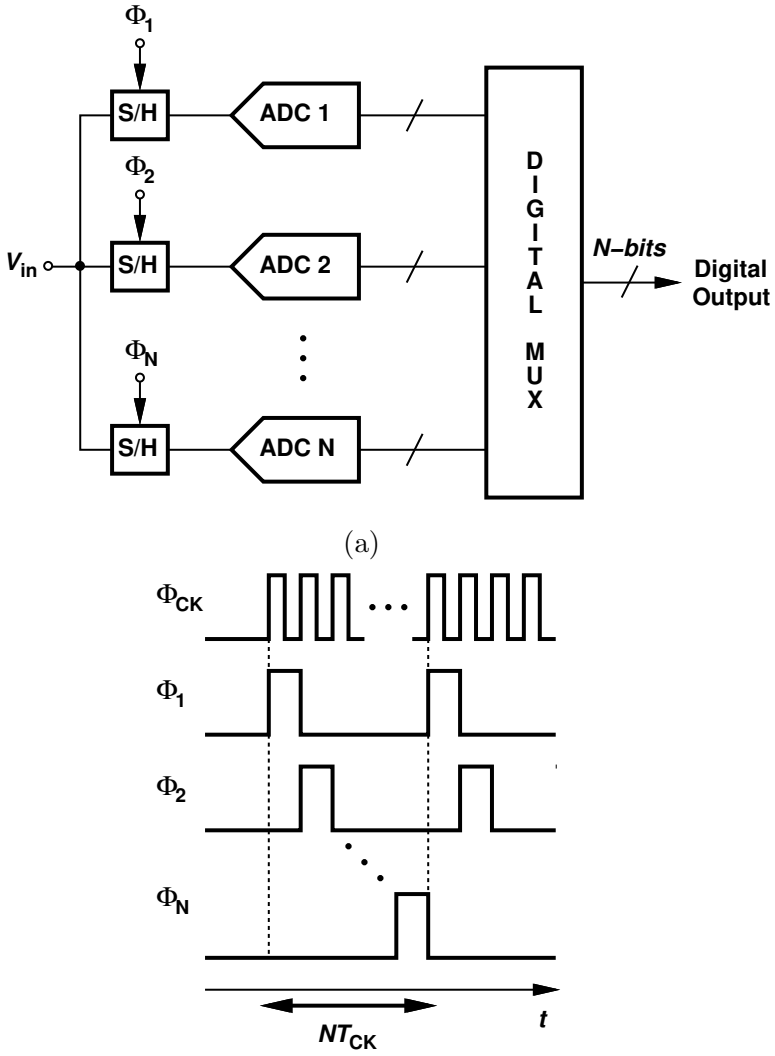


Figure 2.7: (a) A N-channel Time-interleaved ADC and (b) its Clocking Sequence.

2.7 SAR ADC Topologies

Various CDAC topologies can be used to implement the sampling network for a SAR ADC. Three SAR ADC topologies are discussed in this section.

2.7.1 Binary Weighted Capacitor Array

The binary weighted capacitor-array for an N-bit SAR ADC uses n+1 capacitors with the weight of the largest capacitor being 2^N times that of the unit capacitor. As the number of ADC bits, N, increases this results in the load capacitor size and area of the chip increasing exponentially [16]. Figure 2.6 shows a 4-bit binary weighted SAR ADC.

2.7.2 Split-Array SAR ADC with Fractional Bridge Capacitor

The issue of increased area and capacitance posed by a binary weighted capacitor array can be solved by using a split capacitor DAC. Figure 2.8 shows a 4-bit design of a split capacitor DAC. This design consists of two capacitor arrays - the LSB side (left) and the MSB (right) side - separated by a bridge capacitor connected in series between them. The size of the bridge capacitor is given by (2.25).

$$C_b = \frac{C_{total} \text{ of LSB array}}{C_{total} \text{ of MSB array}} \tag{2.25}$$

Therefore, in Fig. 2.8, the value of the bridge capacitor is given by $C_b = \frac{4C}{3C}$. The effective capacitance of the LSB side and the bridge capacitor is C; therefore, the total capacitance of the sampling network is given by 4C. The total capacitance of the sampling network is thus significantly reduced for an N-bit SAR ADC. This topology is thus very useful as the resolution of the ADC increases. A fractional capacitor, however, results in poor matching with the other capacitors and thus in erroneous values. The bridge capacitor also suffers due to the parasitic effects due to the top and bottom plate capacitances.

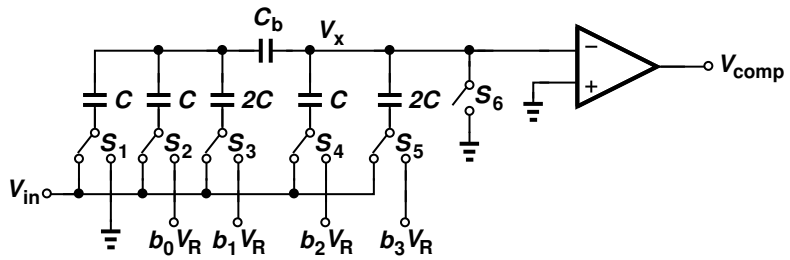


Figure 2.8: 4-bit Split-Array SAR ADC with Fractional Bridge Capacitor

2.7.3 Split-Array SAR ADC with Unit Bridge Capacitor

Figure 2.9 shows a 4-bit split-array SAR ADC using a unit capacitor. The issue of poor matching in the the split-array SAR in section 2.7.2 can be resolved by replacing the fractional bridge capacitor with a unit capacitance and removing the dummy capacitor in the LSB array. This solution introduces a 1 LSB gain error but solves the issue of matching [16]. This structure too is vulnerable to the parasitic capacitance effects introduced by the top and bottom capacitance of the bridge capacitor, thereby causing a mismatch between the LSB and MSB array, thereby degrading the overall ADC performance [16]. However, the effects of the parasitic capacitance are not significant in medium resolution $(6-8$ bit) ADCs. Therefore, this topology provides reduced area with acceptable performance and is an optimum solution for medium resolution ADCs.

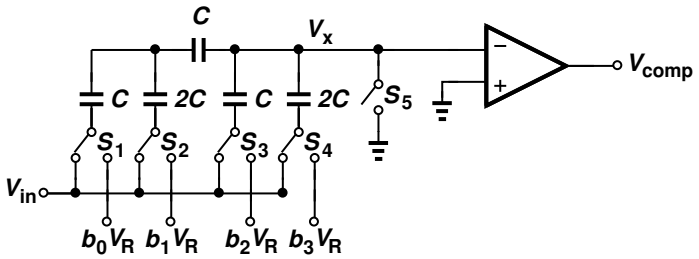


Figure 2.9: 4-bit Split-Array SAR ADC with Unit Bridge Capacitor

CHAPTER 3

DELTA-SIGMA DATA CONVERTERS

Delta-sigma (also known as sigma-delta) data converters are a type of oversampled data converters [17]. Delta-sigma data converters greatly enhance the SNR that can be achieved by oversampled converters. Thus they are extremely useful in modern voiceband, audio, and high-resolution precision industrial measurement applications that require high accuracy, up to 15-20 bits and fairly high speeds of operation (8 - 500 kS/s) [18],[19]. As mentioned in chapter 2, section 2.5.2, oversampled converters increase the performance of the ADC by sampling the input at a much higher frequency than the Nyquist frequency and then filtering out the signal within the desired frequency bandwidth [20]. This in turn filters out the out-of-band quantization noise thereby increasing SQNR performance. The basic idea behind a delta-sigma converter is that the SQNR performance of an ADC can be further improved if the in-band quantization noise of the oversampling converter can be reduced. This can be achieved using a technique called noise shaping, further explained in section 3.1.

A delta-sigma converter consists of three main components - an analog/digital filter (also known as the modulator/loop filter), a low-resolution quantizer and a DAC in a feedback loop [1]. Delta-sigma converters enable us to obtain a high-resolution ADC while using a quantizer with a much lower resolution [21]. Delta-sigma modulators can be of two types - continuous-time $\Delta\Sigma$ converters that use analog filters, or discrete-time $\Delta\Sigma$ converters that use digital filters. This work focuses on discrete-time $\Delta\Sigma$ converters. Various discrete-time $\Delta\Sigma$ converters are implemented in Simulink in chapter 4, while chapters 5-7 focus on the design of a high-speed quantizer for a high-speed delta-sigma modulator. This chapter provides a brief overview of 1^{st}, 2^{nd} and higher-order delta-sigma modulators.

3.1 Noise Shaping and First-Order $\Delta\Sigma$ Converters

3.1.1 Noise Shaping

The quantization noise in multi-bit quantizers is said to possess a white spectrum, i.e. noise introduced in a signal after quantizing (quantization noise) is uniformly distributed across all frequencies in its spectrum [11]. The increased signal-to-noise ratio attributed to delta-sigma converters is due to its property of *noise-shaping*. The loop filter in a delta-sigma converter has a high gain within the signal band, resulting in attenuation of the in-band quantization noise while amplifying the out-of-band quantization noise [1]. In this manner, noise is shaped out of the signal band improving the in-band SQNR via the loop filter. This process is thus called noise-shaping. The degree to which the in-band noise is attenuated depends on the order of the loop filter/modulator. The order of noise-shaping in a modulator refers to the order of the filter used as the loop filter. The order of the filter usually corresponds to the number of zeros in the signal band of the transfer function from the input to the output [21]. Higher attenuation and thus performance can be obtained as the order of the modulator is increased.

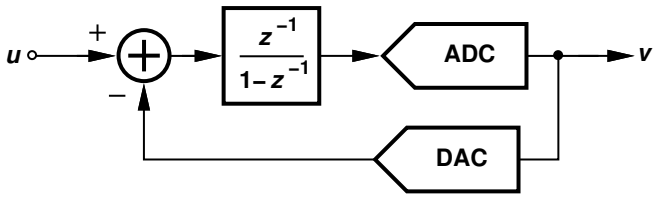
3.1.2 First-Order $\Delta\Sigma$ Modulator

A first-order delta sigma-modulator, also known as MOD1, consists of a feedback-loop comprised of a quantizer, a digital-to-analog converter and mainly a loop-filter of order 1. Figure 3.1a shows a discrete-time first-order delta-sigma modulator.

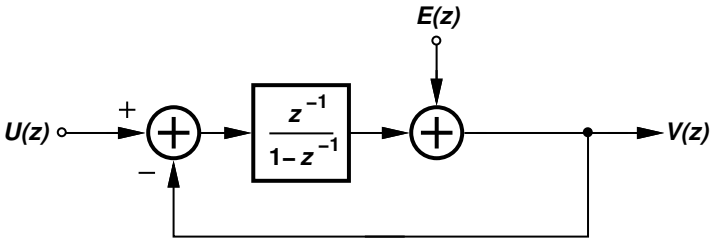
The difference between the input of the $\Delta\Sigma$ ADC, $U(z)$ and the output V(z) is first inputted to the first-order loop filter with transfer function, $L(z)$.

$$L(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{3.1}$$

The output of the loop-filter then passes through a quantizer to give the quantized output $V(z)$ of the ADC [1]. An integrator is used as the loop filter in a MOD1 design. For ease of analysis, the quantizer in Fig. 3.1a is replaced with additive noise model in Fig. 3.1b. The relationship between the input



(a)



(b)

Figure 3.1: (a) Discrete-Time First-Order (MOD1) Delta-Sigma Modulator and (b) its Linear Model [1].

$U(z)$ and output $V(z)$ is given by the signal-transfer-function (STF) given by (3.3). The relationship between the quantization noise, $E(z)$ and the output is given by the noise-transfer-function (NTF) given by (3.5) [1].

$$(U(z) - V(z))L(z) = V(z) \tag{3.2}$$

$$\begin{aligned} STF(z) = \frac{V(z)}{U(z)} &= \frac{L(z)}{1 + L(z)} \\ &= z^{-1} \end{aligned} \tag{3.3}$$

$$V(z)L(z) + E(z) = V(z) \tag{3.4}$$

$$\begin{aligned} NTF(z) = \frac{V(z)}{E(z)} &= \frac{1}{1 - L(z)} \\ &= 1 - z^{-1} \end{aligned} \tag{3.5}$$

The z-transform of the output $V(z)$ is thus given by (3.6) and its time-domain value $v[n]$ is given by (3.7) [1]. It can thus be seen that the input is passed as it is to the output while the quantization noise is high-pass filtered by the NTF.

$$\begin{aligned} V(z) &= STF(z)U(z) + NTF(z)E(z) \\ &= z^{-1}U(z) + 1 - z^{-1}E(z) \end{aligned} \tag{3.6}$$

$$v[n] = u[n-1] + e[n] - e[n-1] \tag{3.7}$$

In the frequency domain, once z is replaced by $e^{j\omega}$, the $NTF(\omega) = 1 - e^{j\omega}$. The power spectral density of the output noise, $S_q(\omega)$, is given by (3.8) [12],[1].

$$\begin{aligned} S_q(\omega) &= |NTF(\omega)|^2 \cdot S_e(\omega) \\ &= |1 - e^{j\omega}|^2 \cdot S_e(\omega) \\ &= |2\sin(\frac{\omega}{2})|^2 \cdot S_e(\omega) \end{aligned} \tag{3.8}$$

Thus, the quantization noise power within the signal band, f_b, is given by (3.9) [12].

$$\begin{aligned} P_e &= \int_0^{\frac{\pi}{OSR}} S_q(\omega)d\omega = \Big(\frac{\Delta^2}{12\pi}\Big)\Big(\frac{\pi^3}{3OSR^3}\Big) \\ &= \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \end{aligned} \tag{3.9}$$

If the signal power P_s is given by (2.14), then the maximum SQNR for a N-bit first-order delta-sigma modulator is given by (3.10) [12].

$$\begin{aligned} SQNR_{MOD1} &= 10log\left(\frac{P_s}{P_e}\right) \\ &= 6.02N + 1.76 - 5.17 + 30log(OSR) \end{aligned} \tag{3.10}$$

Therefore, doubling the OSR improves the SQNR performance by 9 dB or 1.5 bits. The noise-shaped delta-sigma modulator thus gives a much better SQNR performance than both Nyquist-rate ADCs and oversampled ADCs [12].

3.2 Second-Order $\Delta\Sigma$ Modulators

The performance of a first-order delta-sigma can further be improved by replacing the ADC in the delta-sigma loop by another delta-sigma ADC. A second-order delta-sigma modulator can thus be obtained by replacing the quantizer in a MOD1 with another MOD1 ADC. The second-order delta-sigma modulator is commonly known as MOD2 [1]. Figure 3.2 shows a discrete time second-order delta-sigma modulator. The output $V(z)$ of the modulator is given by (3.11).

$$\begin{aligned} V(z) &= STF(z)U(z) + NTF(z)E(z) \\ &= z^{-1}U(z) + (1-z^{-1})^2 E(z) \end{aligned} \tag{3.11}$$

The power spectral density of the output noise, $S_q(\omega)$, is given by (3.12) [1].

$$\begin{aligned} S_q(\omega) &= |NTF(\omega)|^4 \cdot S_e(\omega) \\ &= |1 - e^{j\omega}|^4 \cdot S_e(\omega) \\ &= |2\sin(\frac{\omega}{2})|^4 \cdot S_e(\omega) \end{aligned} \tag{3.12}$$

Thus, the quantization noise power within the signal band, f_b, is given by (3.13) [1],[12].

$$\begin{aligned} P_e &= \int_0^{\frac{\pi}{OSR}} S_q(\omega)d\omega = \Big(\frac{\Delta^2}{12\pi}\Big)\Big(\frac{\pi^5}{5OSR^5}\Big) \\ &= \frac{\Delta^2\pi^4}{60}\left(\frac{1}{OSR}\right)^5 \end{aligned} \tag{3.13}$$

If the signal power P_s, is given by (2.14), then the maximum SQNR for a

N-bit second-order delta-sigma modulator is given by (3.14) [1],[12].

$$\begin{aligned} SQNR_{MOD2} &= 10log\left(\frac{P_s}{P_e}\right) \\ &= 6.02N + 1.76 - 1.29 + 50log(OSR) \end{aligned} \tag{3.14}$$

Therefore, doubling the OSR improves the SQNR performance by 15 dB or 2.5 bits. The second-order delta-sigma modulator thus gives a much better SQNR performance than the first-order modulator.

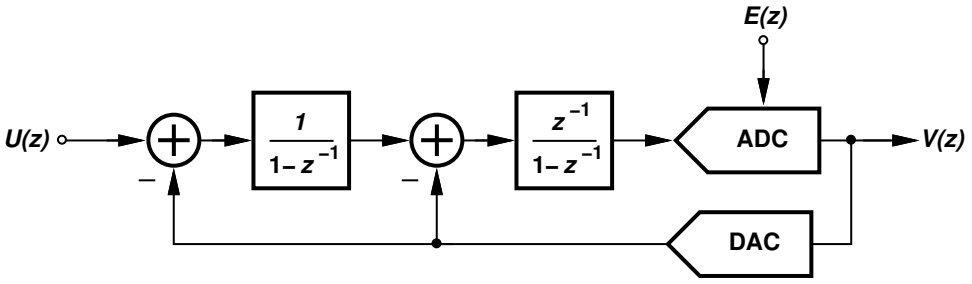


Figure 3.2: Discrete-Time Second-Order Delta-Sigma Modulator

3.3 Higher-Order $\Delta\Sigma$ Modulators

Although increasing the order of noise-shaping improves the performance of the ADC, the order cannot be increased infinitely. This is because for delta-sigma modulators above the 3_{rd} order, stability becomes a concern. While noise-shaping decreases the in-band noise of the spectrum, overall noise is added to the input signal. The delta-sigma loop causes high-frequency noise to be added to the input before it is quantized by the quantizer. As the order of noise-shaping increases, the amplitude of this noise increases as well. If the input to the quantizer exceeds its full-scale range, the quantizer saturates and the delta-sigma loop becomes unstable. Therefore, the input signal cannot occupy the full-scale range of the quantizer; room needs to be left for the shaped noise to ride on it. The ratio of the stable input range to the quantizer full-scale range is known as the *maximum stable amplitude* (MSA). The MSA of a delta-sigma modulator decreases as the order of noise-shaping increases and so the order of noise-shaping cannot be increased arbitrarily. As the

SNR of an ADC depends on the signal power, which in turn depends on the signal amplitude, the increase in SNR for higher-order modulators is limited [1].

The SNR of higher-order modulators can be improved by optimizing the poles and zeros of the loop-filter. The total noise power in the signal band is reduced by spreading the zeros, while stability is improved by moving the poles closer to the zeros as this reduces the out-of-band NTF gain [1]. Higher-order modulators require specialized loop filter architectures with optimized poles and zeros in order to ensure stability with improved SNR.

So far we have looked at delta-sigma modulators where the difference of the input (u[n]) and output (v[n]) is fed to a single-input loop filter with transfer function L(z). A delta-sigma modulator can also be constructed using a two-input loop filter. In this case the input signal, u[n], and the output signal, v[n], go through two different transfer functions, $L_0(z)$ and $L_1(z)$ respectively. The output of the two-input loop filter, $Y(z)$, is given by (3.15) and the relationship between $L_0(z)$ and $L_1(z)$, and between STF and NTF, is given by (3.16) and (3.17) [1].

$$Y(z) = L_0(z)U(z) + L_1(z)V(z) \tag{3.15}$$

$$NTF(z) = \frac{1}{1 - L_1(z)} \tag{3.16}$$

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} \tag{3.17}$$

3.3.1 Loop Filter Architectures

Two loop filter architectures that are commonly used in higher-order modulators — the cascade of integrators with distributed feedback and input coupling (CIFB) and the cascade of resonators with distributed feedback and input coupling (CRFB) structures — are described in this section.

The CIFB Structure

The CIFB structure shown in Fig. (3.3) contains a cascade of N delaying integrators. The input signal as well as feedback signal is fed to each integrator with weights a_i and b_i respectively. The signal filter transfer function $L_0(z)$ is given by (3.18) and the feedback filter transfer function $L_1(z)$ is given by (3.19) [1].

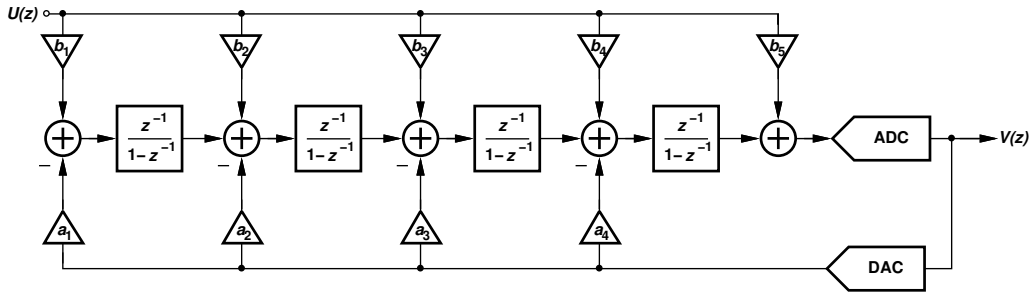


Figure 3.3: A 4^{th}-order CIFB Structure

$$L_0(z) = \frac{b_1 + b_2(z-1) + \ldots + b_{N+1}(z-1)^N}{(z-1)^N} \tag{3.18}$$

$$L_1(z) = \frac{a_1 + a_2(z-1) + \ldots + a_{N+1}(z-1)^N}{(z-1)^N} \tag{3.19}$$

The coefficients a_i set the zeros of L_1 and thus the poles of the NTF and STF, while the coefficients b_i determine the zeros of L_0 and thereby set the zeros of the STF. The zeros of the NTF can be placed at non-zero frequencies by introducing local feedback around the delaying integrators forming a resonator as shown in Fig. 3.4. The resonator is locally unstable as it has poles outside the unit circle but is embedded in a stable feedback system [1]. This is useful in high-frequency ADCs as it relaxes the speed requirements of the amplifiers used [1].

The CRFB Structure

Figure 3.5 shows a loop filter with a CRFB structure. The poles of the resonator from the CIFB structure with local feedback can be placed on the unit circle by using a CRFB structure. A CRFB structure contains a cascade of delaying and non-delaying integrators consecutively. The resonator is formed

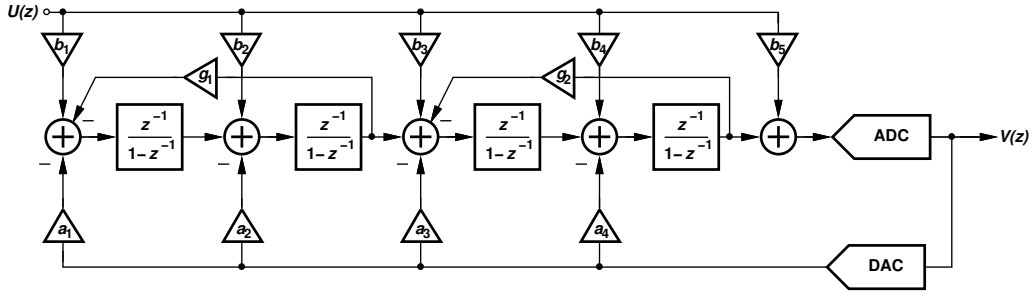


Figure 3.4: A 4^{th}-order CIFB Structure with Resonators

by local feedback around a non-delaying and delaying integrator pair with feedback coefficients g_i.

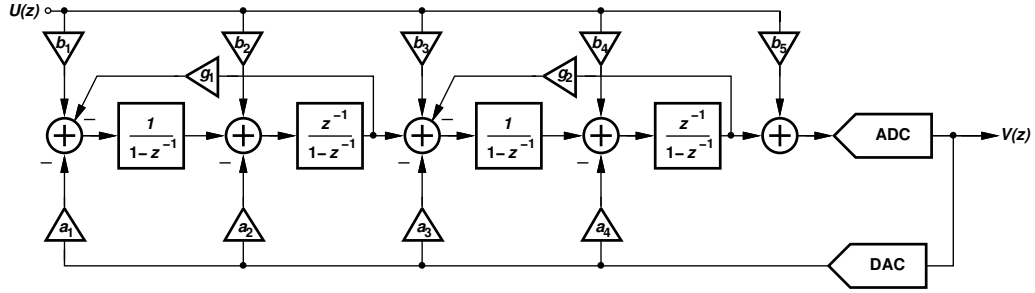


Figure 3.5: A 4^{th}-order CRFB Structure

CHAPTER 4

DELTA-SIGMA MODELING IN SIMULINK

4.1 Simulink Modeling of First-Order $\Delta\Sigma$ Modulator

The performance of a first-order delta-sigma modulator can be modeled in Simulink using basic building blocks. Figure 4.1 shows the Simulink model built to simulate the performance of a MOD1 consisting of a 5-bit quantizer. The discrete sine wave block was used to get a sampled sine wave. The discrete transfer function block was used as the loop filter and an ideal quantizer block with appropriate thresholds was used as the ADC. Figure 4.2 shows the simulated output spectrum of the Simulink model in Fig. 4.1. As expected, the SNR of the 5-bit MOD1 with an oversampling ratio of 64 is $\sim$ 81 dB.

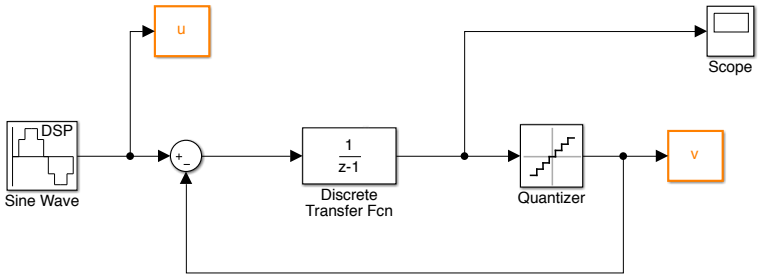


Figure 4.1: Simulink Model of a MOD1 System

4.2 Simulink Modeling of Second-Order $\Delta\Sigma$ Modulator

Figure 4.3 shows the Simulink model of a second-order delta-sigma modulator. The quantizer used in the loop is a custom 33-level flash ADC Simulink model. A 33-level digital-to-analog converter (DAC) was implemented in

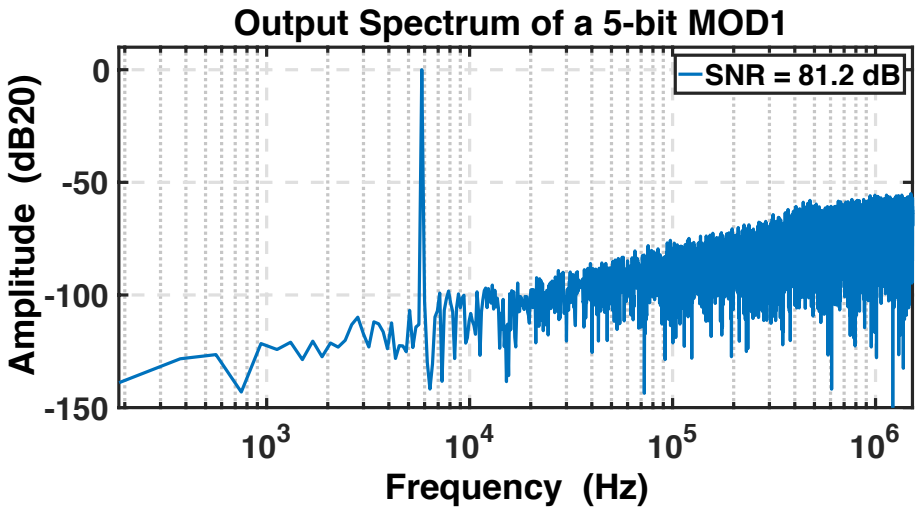


Figure 4.2: Output Spectrum of a 5-bit MOD1 with $OSR = 64$

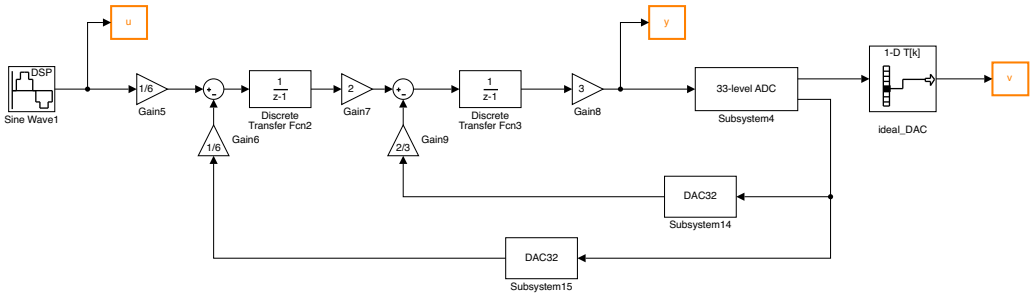


Figure 4.3: Simulink Model of a MOD2 System

Simulink to be used in the delta-sigma loop. Figure 4.4 shows the output spectrum of the simulated second-order delta-sigma modulator.

4.2.1 Flash ADC Simulink Model

The 33-level flash ADC was built using four 8-level flash ADCs shown in Fig. 4.5. The 8-level flash ADC consists of 8 comparators, modeled using the $>$ relational operator and a summing block. The summing block converts the thermometer coded output to a binary code. The resistor divider thresholds, characteristic of flash ADC, are modeled as ideal threshold values generated externally using MATLAB and inputted to the Simulink block. Figure A.1 in Appendix A shows the complete Simulink model of the 33-level ADC.

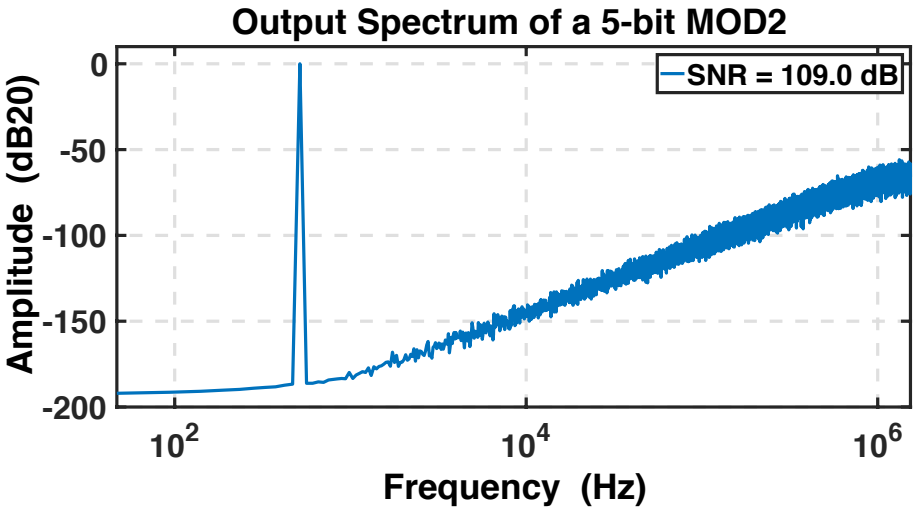


Figure 4.4: Output Spectrum of a 5-bit MOD2 with $OSR = 64$

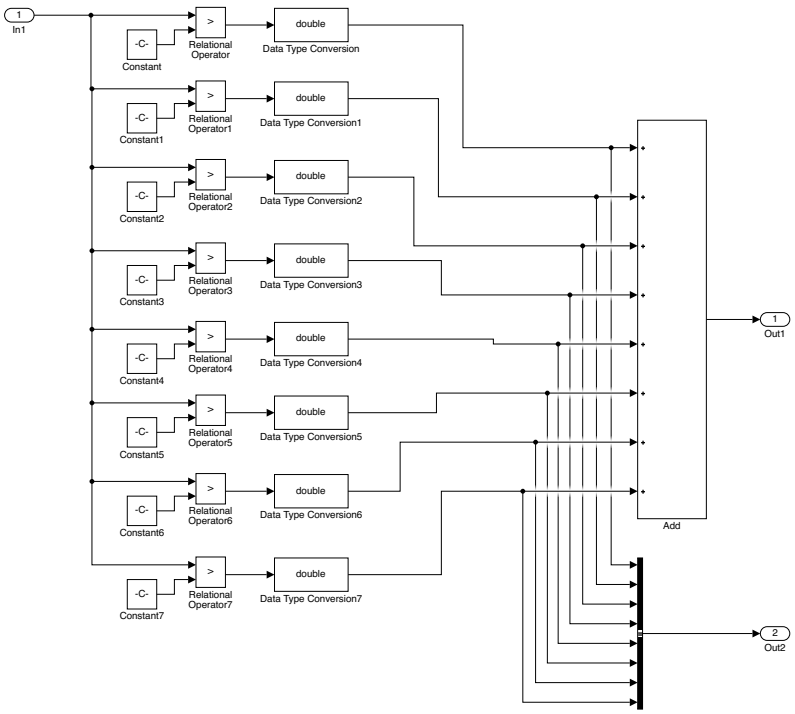


Figure 4.5: Simulink Model of an 8-level Flash ADC

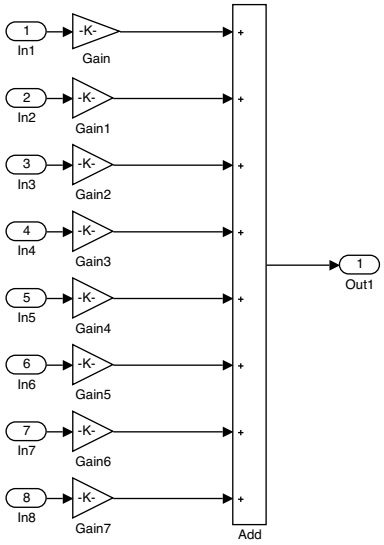


Figure 4.6: Simulink Model of an 8-level DAC

4.2.2 DAC Simulink Model

The 33 level DAC (Fig. A.2) takes the thermometer code outputted by the flash ADC as input and converts it to the appropriate quantized voltage. The DAC was implemented in Simulink using four 8-level DACs. Each 8-level DAC comprises 8 unit DACs, each providing an output equal to one LSB. Figure 4.6 shows the Simulink model of the 8-level DAC.

4.3 Simulink Modeling of Fifth-Order $\Delta\Sigma$ Modulator

4.3.1 Fifth-Order $\Delta\Sigma$ Modulator with Single-bit Quantizer

A fifth-order single-bit delta-sigma modulator (Fig. 4.7) was designed using Simulink and the delta-sigma toolbox in MATLAB. The modulator uses a loop filter with a cascade of integrators with distributed feedback and distributed input coupling structure (CIFB) shown in Fig. 4.8.

This structure consists of five delaying integrators, each with inputs as, the feedback signal from the quantizer and the input signal to the modulator with weight factors a_i and b_i. The two feedback paths, each with g_i, and the two integrators introduces four zeros as two conjugate complex pairs in the noise-transfer-function (NTF). The zeros of the NTF are optimized to

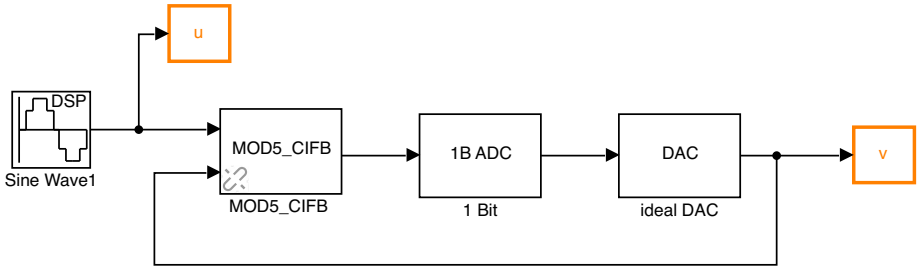


Figure 4.7: Simulink Model of a Single-bit 5^{th}-order $\Delta\Sigma$ Modulator

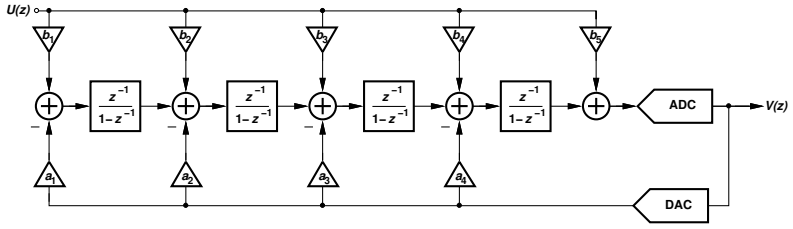


Figure 4.8: Simulink Model of Loop Filter with CIFB Structure

improve SQNR performance. The inter-stage gains of the integrators are given by the coefficient c_i. The coefficients for the loop filter are found using the delta-sigma toolbox developed by Richard Schreier [1]. The noise transfer function (NTF) and signal transfer function (STF) of the desired 5^{th} order modulator were found using simulation and are given by (4.1) and (4.2).

$$NTF_{original} = \frac{(z-1)(z^2-2z+1.003)(z^2-2z+1.008)}{(z-0.7778)(z^2-1.613z+0.6649)(z^2-1.796z+0.8549)} \tag{4.1}$$

$$STF_{original} = \frac{0.00067556}{(z-0.7778)(z^2-1.613z+0.6649)(z^2-1.796z+0.8549)} \tag{4.2}$$

In order to simplify the circuit structure all b_i except b_1 are chosen to be 0. The coefficients a_i, b_i, c_i and g_i were first found using the simulation from the NTF. The original (orig.) coefficient values were then rounded up or down to give suitable ratios to easily realize the gains using real capacitors in a circuit level design. The Simulink model was then re-simulated to ensure stability of the modulator. The modified NTF and STF of the realizable

Table 4.1: Coefficients Used in the Single-bit MOD5 CIFB Structure

i	a_i		b_i		c_i		g_i	
	Orig.	**Real.**	**Orig.**	**Real.**	**Orig.**	**Real.**	**Orig.**	**Real.**
1	0.0869	0.08	0.0869	0.1	0.1212	0.12	0.0140	0.014
2	0.1488	0.15	0	0	0.1993	0.2	0.0151	0.015
3	0.2270	0.2	0	0	0.3276	0.3	-	-
4	0.3155	0.32	0	0	0.5226	0.5	-	-
5	0.4324	0.4	0	0	1.8799	2	-	-
6	-	-	0	0	-	-	-	-

(real.) design are given by (4.3) and (4.4). Table 4.1 shows the original and realizable values for the coefficients a_i, b_i, c_i and g_i. Figure 4.9 shows the simulated output spectrum of the fifth-order delta-sigma modulator using the original and realizable coefficients.

$$NTF_{realizable} = \frac{(z-1)(z^2-1.997z+1)(z^2-1.993z+1)}{(z-0.9015)(z-0.7765)(z-0.311)(z^2-1.881z+0.9187)} \tag{4.3}$$

$$STF_{realizable} = \frac{0.00072z^2}{(z-0.9015)(z-0.7765)(z-0.311)(z^2-1.881z+0.9187)} \tag{4.4}$$

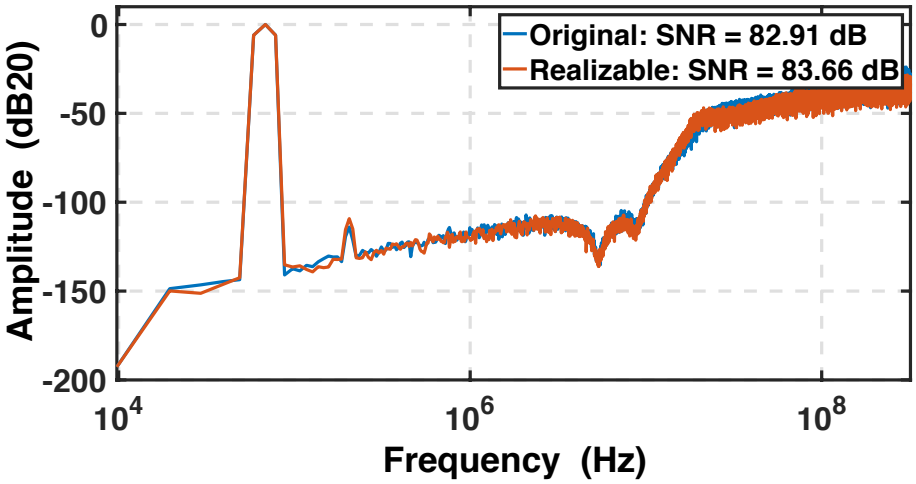


Figure 4.9: Output Spectrum of a 1-bit MOD5 with $OSR = 32$

CHAPTER 5

HIGH-SPEED MULTI-BIT QUANTIZER DESIGN

High-speed delta-sigma modulators require all components in the loop to be able to operate efficiently at a high speed. This chapter and the rest of the thesis focus on the design of a high-speed quantizer operating at a sampling rate of 5GS/s with the motivation to use it in a high-speed delta-sigma modulator. A successive approximation register based ADC is chosen as the quantizer as SAR ADCs benefit largely from technology scaling due to their highly digital implementation and also introduce an extra order of noise-shaping [6]. As the operating frequency approaches the technology limit of the CMOS transistors it is nearly impossible to build such high-speed ADCs using a single channel. Therefore, the SAR ADC is built using time-interleaving, which reduces the design strain on each single-channel ADC while enabling us to achieve high sampling rates.

This chapter focuses on the design of a high-speed time-interleaved 4-bit SAR quantizer and techniques used to ensure proper working of the various components at such a high speed. The 4-bit SAR ADC is designed to function as a sub-ADC in an 8-channel time-interleaved ADC operating at a clock frequency (f_{CK}) of 5 GHz. Each sub-ADC is designed to operate at 1/8th the clock frequency, i.e. at a frequency of 625 MHz. Multi-phase clocks are required to time-interleave the various sub-ADCs. The time-interleaved ADC can be broken into two parts: the SAR multi-phase clock generator and the SAR sub-ADC. The design of the three main blocks that constitute each SAR sub-ADC — namely, the sampling network capacitive DAC (CDAC), the comparator and the SAR logic block — will be explained in this chapter.

5.1 Multi-phase Clock Generator

The time-interleaved SAR ADC requires multiple sub-ADCs operating on different phases of the overall sampling clock. That is, the master clock operating at 5GHz is divided by 8 to get a sampling clock with a lower frequency of 625 MHz. This is done to relax the speed constraint on each sub-ADC. Multiple phases of the 625 MHz clock are generated to get 8 clocks each separated by a phase of 45 degrees. The eight sub-ADCs, each operating on a different phase of the multi-phase clock, operate on samples of the input in parallel, with each sample 200 ps apart. The outputs of the eight sub-ADCs are time-interleaved to give an effective sampling rate of 5 GS/s. Any skew in the timing of the multiphase clock would result in the wrong value being sampled, thereby introducing an error in the time-interleaving process and degrading the performance of the ADC significantly [22]. Therefore, the generation and proper alignment of the multi-phase sampling clocks is crucial to the functioning of the ADC. Mutli-phase clock generation can be done using shift registers or delay-locked loops (DLLs). A shift-register based multi-phase clock generator (MPCG) is used due to its better jitter performance. Unlike a DLL, an SR based MPCG does not accumulate jitter from one clock phase to the other. An SR based synchronous clock divider is essentially an injection locked oscillator where the injection signal, i.e. the higher frequency input clock, is injected at multiple points in the loop, thereby correcting the zero crossings and preventing jitter accumulation [23],[24]. An SR based MPCG is thus a better choice [25]. An SR based MPCG containing N DFFs also functions as a divide-by-N clock divider for N-phase clock generation [25].

The 8-phase clock generator block (shown in Appendix B.1, Fig. B.3) consists of two parts, the CML-to-CMOS converter and an 8-phase Johnson counter. The 8-phase clock generator takes as input a sine wave of frequency 5GHz and generates the master clock and 8 phases of the sampling clock at 1/8th the master clock frequency. The output of each block is buffered up to drive the next circuit stage. An external RESET signal is used to ensure that the two circuit blocks start up in the right state. Although the clock generator uses a 5 GHz master clock, it was designed to operate at a frequency as high as 6 GHz.

5.1.1 CML-to-CMOS Converter

The CML-to-CMOS block (Fig. 5.1) serves as the input block to the 8-phase clock generation circuit. It takes as input a sine wave of frequency 5 GHz and generates a square wave that swings from 0 to 1.2 V and forms the master clock. The input signal of amplitude ± 200 $mV_{pp-diff}$ is amplified using a cascade of two amplifiers. The first stage of the CML-to-CMOS block is a differential amplifier of gain 4.2 dB (Fig. 5.2). The differential implementation of the input stage amplifier cancels any common mode noise in the input signal. The second stage consists of two identical single-ended differential amplifiers with their inputs interchanged. Each of the second stage amplifiers takes as input the differential output of the first stage amplifier and amplifies them by 6.8 dB (Fig. 5.3) to obtain an output signal with rail to rail (0 to V_{DD}) output swing. The input and output common mode voltages of all the blocks are set to 600 mV.

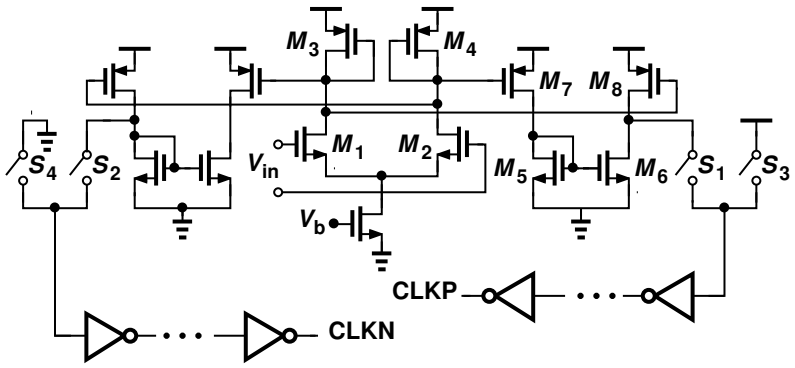


Figure 5.1: CML-to-CMOS Circuit Schematic

The output of each second stage amplifier is connected to a chain of inverters to convert the sine wave output from the second stage into a digital clock signal. The chain of inverters ensures that the output signal has the desired output drive strength. A tapering factor of 2 is used between consecutive inverters. The output of each second stage amplifier is connected to the chain of inverters via switches S_1-S_4 controlled by an external RESET signal. The outputs CLKN and CLKP of the CML-to-CMOS block depend on the orientation of these switches. When RESET is HIGH, the switches S_1 and S_2 are open and switches S_3 and S_4 are closed. Thus, CLKP is forced to V_{DD} while CLKN is forced to GND. On the other hand, when RESET is low the amplifier is directly connected to the chain of inverters and controls the

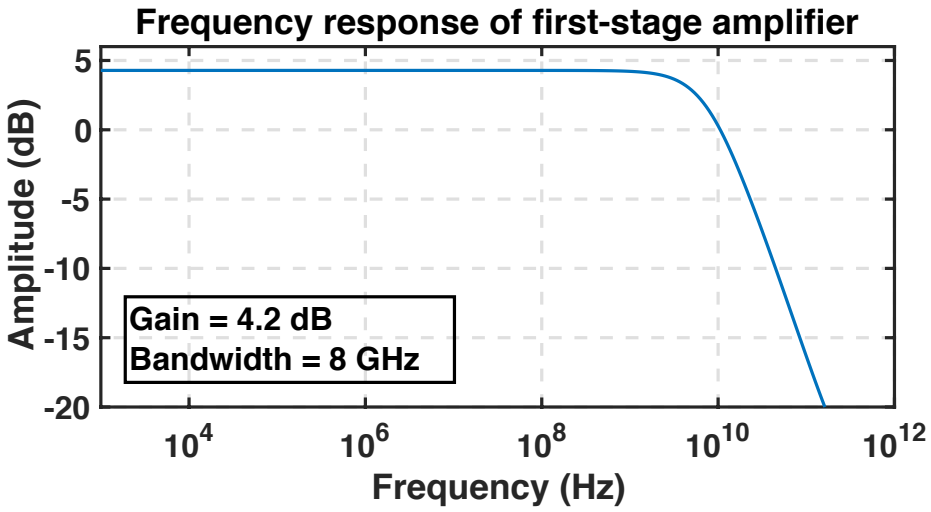


Figure 5.2: Magnitude Response of First-stage Amplifier

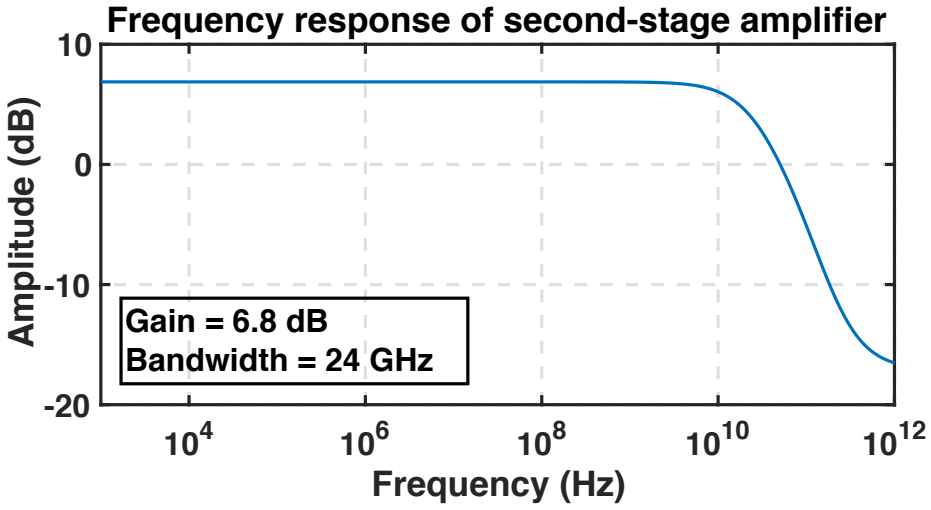


Figure 5.3: Magnitude Response of Second-stage Amplifier

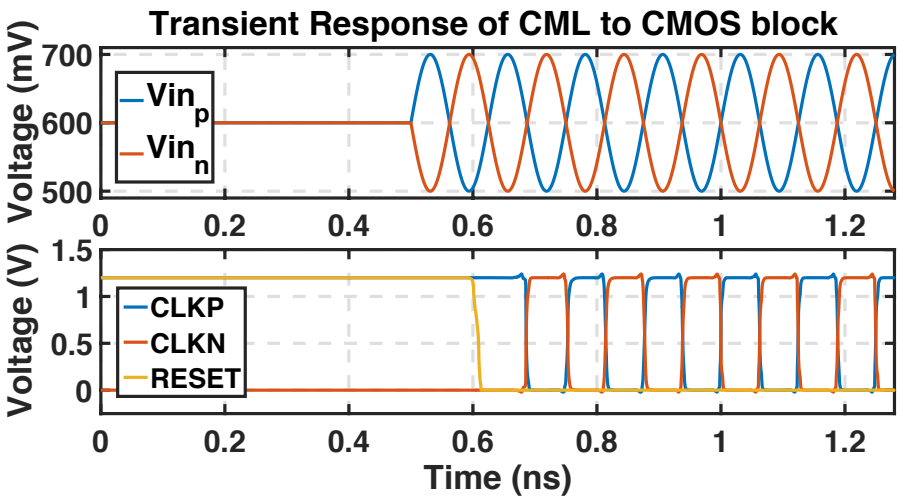


Figure 5.4: Transient Response of CML-to-CMOS Converter

outputs CLKN and CLKP. In the absence of these switches, in the situation where the input signal to the CML-to-CMOS block had not yet been applied, the input to the inverter chain would be the common mode voltage value. In this case, the inverter would arbitrarily provide a high or low output and the state of the output clock would be uncertain when the RESET signal is turned off. Figure 5.4 shows the transient response of the CML-to-CMOS converter.

5.1.2 8-phase Johnson Counter

The 8-phases of the sampling clock needed for time-interleaving are obtained using a Johnson counter. The Johnson counter satisfies a dual purpose; it generates multiple phases of the desired clock and works as a clock divider. A Johnson counter is a type of a ring counter, also known as a twisted ring counter [26]. The Johnson counter (Fig. 5.5) is formed by connecting a chain of four D flip-flops (DFFs) like in a shift-register, each clocked at the master clock frequency, f_{CK}. The output of the first DFF is fed to the input of the next and so on. However, unlike a traditional ring counter where the output of the last DFF serves as the input to the first, the complement of the output of the fourth and last DFF is fed as input to the first DFF in a Johnson counter. The output of the first D flip-flop thus toggles after N cycles of the master clock in an N chain Johnson counter giving the output a

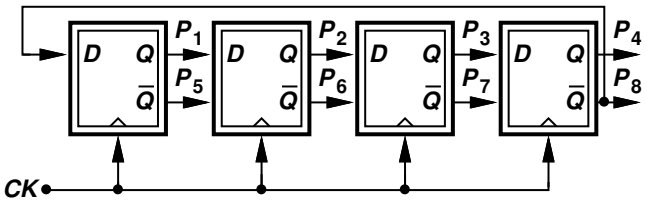


Figure 5.5: Johnson Counter with 8-phase Output

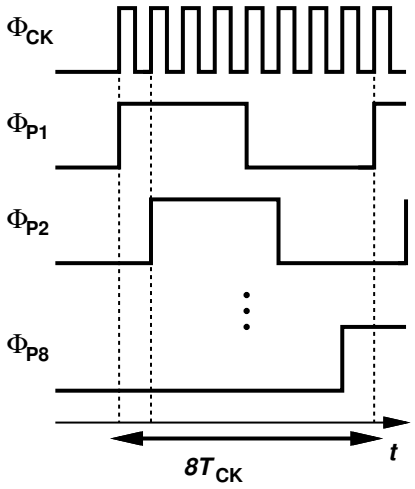


Figure 5.6: Eight Phases of the Sampling Clock

frequency of $\frac{f_{CK}}{N}$. The output of each DFF has a frequency equal to $\frac{f_{clk}}{8}$. The outputs of the four DFFs and their respective complements give the desired 8 phases of the sampling clock, with each phase 45 degrees apart. Figure 5.6 shows the master clock and the eight phases of the generated sampling clock.

Two different DFFs were examined to build the Johnson counter described above: a DFF using CML logic and a static DFF. Originally, the DFF was built using CML logic constructed using two CML D-latches (Fig. 5.7); however, due to the nature of dynamic latches, the output of the DFF and its complement are not perfect complements, i.e. they do not perfectly cross at $V_{DD}/2$. Thus, they cannot be used in the Johnson counter as both the output of the DFF and its complement are used to generate the various clock phases. Thus a static DFF was designed for this purpose. A static DFF with asynchronous reset (Fig. 5.8) to ensure a known state during chip start-up is used in the Johnson counter.

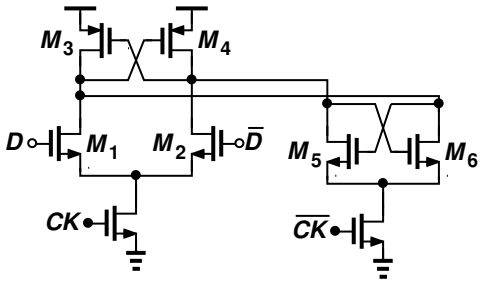


Figure 5.7: Current Mode Logic based D-latch

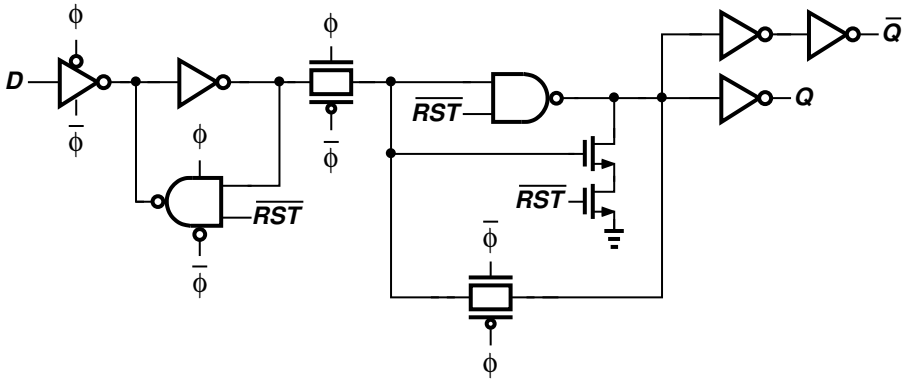


Figure 5.8: D Flip-flop with Asynchronous Reset

5.2 4-bit SAR sub-ADC

5.2.1 SAR sub-ADC Clocking Scheme

Several different clocks are used to ensure proper timing and functioning of the various blocks comprising the SAR ADC. This section explains the role of the different clocks used within one SAR sub-ADC. The operation of the sub-ADC can be broken down into two main phases: the sampling phase and the bit cycling phase. During the sampling phase the input is sampled onto the capacitors of the SAR sampling network CDAC. This input voltage is then quantized to the right value during the bit cycling phase. Five main clocks shown in Fig. 5.9 are used in the SAR ADC:

- **Sampling Clock, Φ_{PS}:** The input is sampled onto the capacitors of the sampling network when the sampling clock is HIGH. The sampling clock is generated by delaying the Early Sampling Clock.
- **Early Sampling Clock, Φ_{PSe}:** The early sampling clock is an early

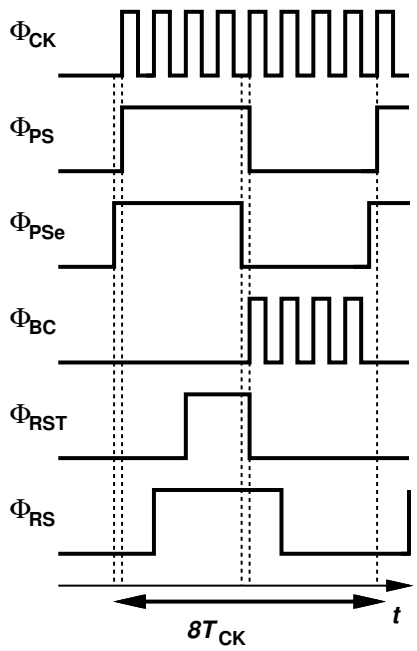


Figure 5.9: Clocks Used in the SAR sub-ADC

version of the sampling clock. It is used to set the input node of the comparator to virtual ground slightly prior to the sampling phase. This is done to ensure that no charge is pulled out of the sampling network through charge sharing when the switches connected to the virtual ground node are closed. The early clock facilitates bottom-plate sampling resulting in mitigation of input-dependent charge injection. The early sampling clock is the clock generated by the Johnson counter.

- **Bit Cycling Clock, Φ_{BC}:** The bit cycling clock is generated by gating the complement of the sampling clock with the master clock. Thus bit cycling clock is low for half the clock period while it produces pulses at the master clock frequency during the other half. The positive edge of the bit cycling clock is used to force a bit value onto the sampling network while the negative edge of the clock is used to trigger the comparator and latch the right logic value onto the selected bit. The comparator block and the SAR Logic block operate on the complement of the bit cycling clock.

- **SAR Logic Reset, Φ_{RST}:** This signal is used to reset the outputs of the D Flip-flops used in the SAR logic block to the right values prior

to the bit cycling phase. The SAR logic reset clock goes high half-way through the sampling phase. This is done to ensure that the flip-flops have enough time to reset as well as to make sure that the last bit resolved by the SAR logic block has enough time to settle down. This signal is generated by gating the sampling clock with a phase-shifted sampling clock already generated by the Johnson counter. A phase shift of 180 degree was chosen between the two clocks.

- **Re-sampling Clock, Φ_{RS}:** The re-sampling clock is used to sample the settled output of the SAR ADC at the right instant. A phase-shifted version of the sampling clock is used as the re-sampling clock.

5.2.2 Comparator

The comparator takes as input the output nodes of the sampling network and gives a decision by comparing the voltage values at the input. The comparator comprises of two blocks: the pre-amplifier and the comparator-latch.

Pre-Amplifier

The pre-amplifier (PreAmp), shown in Fig. 5.10, is the input stage of the comparator block and is used to amplify the input signal to the block as well as reduce the effect of kickback on the comparator-latch. This block is designed to have a gain of about 4.8 dB and bandwidth of 7 GHz. Figure 5.11 shows the magnitude response of the pre-amplifier block. The output of the PreAmp is connected to the input of the comparator-latch.

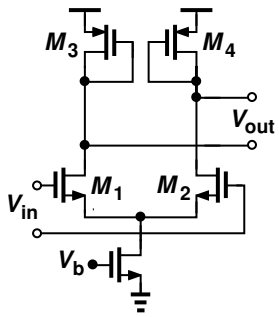


Figure 5.10: The Pre-amplifier

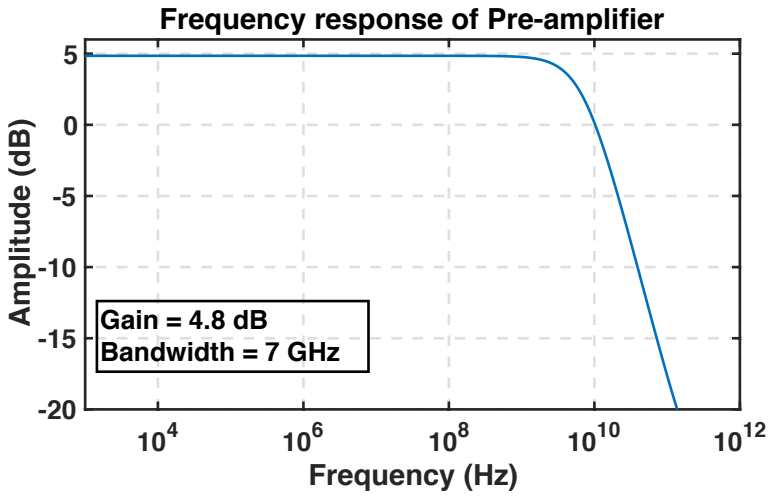


Figure 5.11: Frequency Response of the Pre-amplifier

Comparator-Latch

The comparator-latch is responsible for comparing the input voltages at the positive edge of the clock as well holding the output of the comparator to the right value once it has been resolved. The comparator-latch consists of two sub-blocks: the StrongARM latch and the set-reset latch.

- **StrongARM Latch:** A StrongARM latch [27] (Fig. 5.12) is used to resolve the input of the comparator-latch, and thus the input to the comparator block. Nodes W, X, Y, and Z of the comparator are pre-charged to V_{DD} when CLK is LOW. When the clock is HIGH the StrongARM latch is active and nodes W, X, Y, and Z give an appropriate output based on the comparator input.

- **Set-Reset Latch:** The set-reset Latch (Fig. 5.13) is used to preserve the output generated by the StrongARM latch when CLK goes LOW. The input NMOS transistors M_5 and M_6 are sized to be stronger than the PMOS transistors M_3 and M_4 in the cross-coupled latch to ensure that the outputs V_{op} and V_{on} are set by the input and not the holding action of the PMOS transistors.

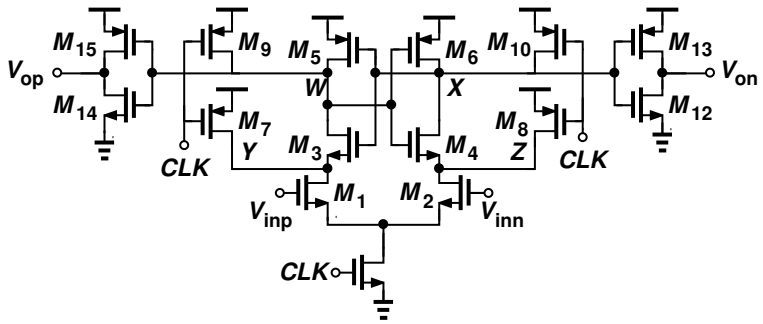


Figure 5.12: The StrongARM Latch

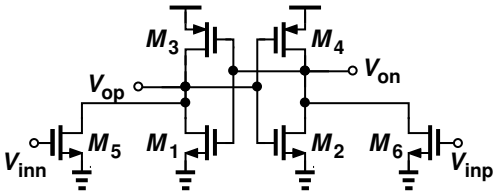


Figure 5.13: The Set-Reset Latch

5.2.3 Sampling Network

The SAR sampling network is the primary interface between the external input voltage and the SAR ADC. The sampling network consists of a binary weighted capacitive DAC as shown in Fig. 5.14, which depicts a single-ended implementation of the differential sampling network (Figures B.6 and B.7) used in the SAR ADC. The switches S_1, S_2, S_3, S_4 and S_5 are controlled by the sampling clock and are connected to V_{IN} during the sampling phase while switch S_6 controlled by the early sampling clock is connected to virtual ground. During the bit cycling phase, switches S_1, S_2, S_3, S_4 and S_5 are controlled by a signal generated by gating the bit-cycling clock with the bits outputted by the SAR logic block. The output of the sampling network is connected to the input of the comparator block.

The switches S_1, S_2, S_3, S_4, S_5 and S_6 are realized using PMOS transistors due to the high common-mode voltage used in the SAR ADC. The unit capacitor C is chosen as 10 fF. The PMOS switches S_1 and S_2 connected to the unit capacitors are chosen to be of size 1 μm. The switch sizes are scaled by the same amount as the capacitor value ensuring that the RC time constant of each branch remains the same.

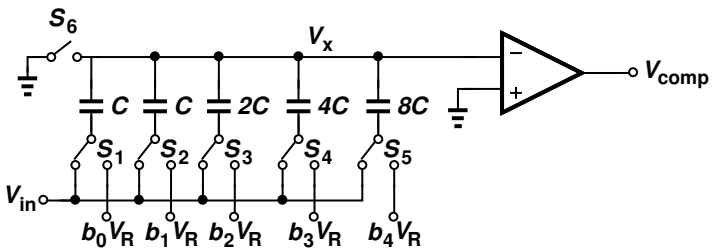


Figure 5.14: Single-ended 4-bit SAR Sampling Network Implementation

5.2.4 SAR Logic Block

The SAR logic block is responsible for implementing the bit-cycling logic that is characteristic of SAR ADCs. This block ensures that the binary number formed by the 4 bits ($b_3b_2b_1b_0$) is set to the right value during the sampling as well as the bit-cycling phase of the SAR ADC.

Figure 5.15 shows the SAR logic block for a 2-bit SAR ADC and the timing diagram of its signals. It consists of 2 chains of 3 DFFs. The top chain of DFFs, DFF1-DFF2, are clocked by the complement of the bit-cycling clock (Φ_{BC}), labeled as Φ_{CK} on Fig. 5.15. The outputs Q_1, Q_2 and Q_3 are used to SET the outputs of the bottom chain DFFs to 1 during the bit-cycling phase. The bottom chain of flip-flops, DFF4-DFF6, are each clocked by it successive DFF. During the sampling phase, the outputs Q_2, Q_3, B_0 and X are reset to 0 using the SAR logic reset signal (Φ_{RST}) while the outputs Q_1 and B_1 are set to 1. During the bit-cycling phase, at the positive edge of the clock Φ_{CK}, Q_2 goes to 1, setting B_0 to 1, this clocks DFF4 and causes B_1 to latch to the comparator value. The output B_0 is similarly latched to the comparator value at the next clock edge.

The SAR sub-ADC is designed using synchronous SAR logic as shown in Fig. 5.16. The 4-bit SAR logic block consists of 2 chains of 5 DFFs each. In order to ensure that the comparator output in our sub-ADC has sufficient time to settle, the SAR logic block is clocked using a delayed version of the clock that triggers the comparator. The SAR logic block plays a critical role in determining the maximum speed at which a single-channel SAR ADC can operate. The DFFs used in the 4-bit SAR logic block (Fig. 5.16) are optimized to reduce the delays along the critical path of the SAR logic block. The set-to-Q and clock-to-Q delays of the set-reset D flip-flops (DFFSR) used in the bottom chain of the SAR logic block contribute to the delay of this

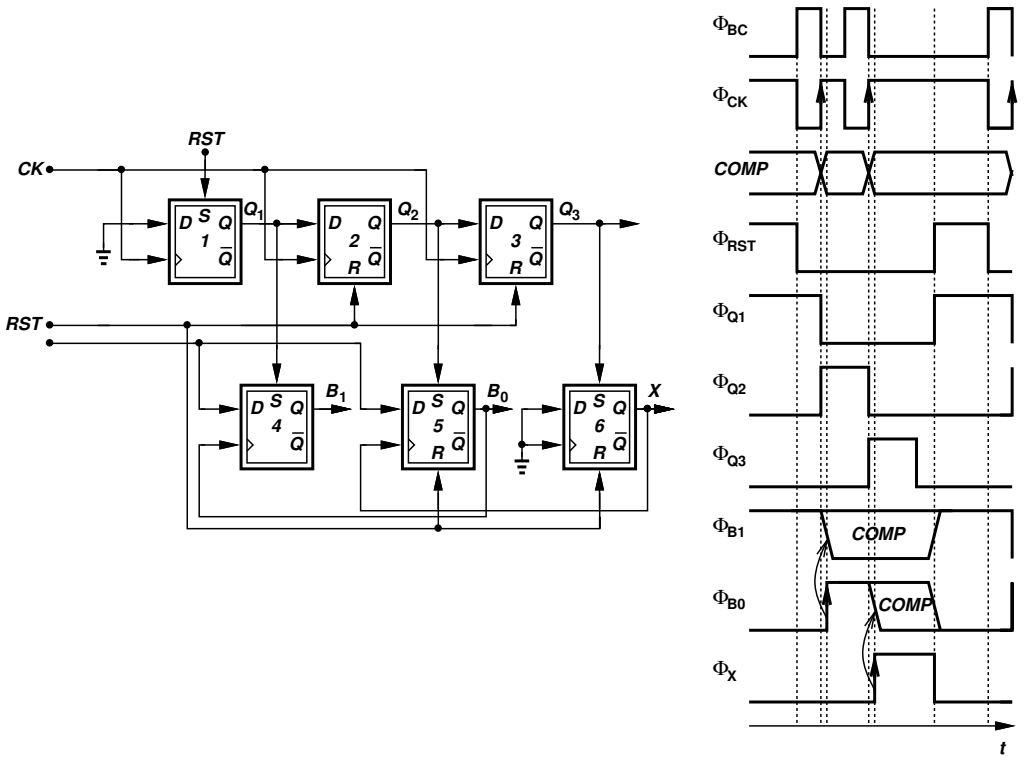


Figure 5.15: 2-bit SAR Logic Block and relevant Timing Sequence

block. The DFFSR is especially designed to ensure that the set-to-Q delay of the flip-flop is as small as possible as it is along the critical path. Figure 5.17 shows a conventional DFFSR. As seen in Fig. 5.18, the signal passes through only one gate when the set signal is HIGH for the custom DFFSR while it passes through 4 gates in the case of a conventional DFFSR. This ensures that the output is set to HIGH as soon as possible once the set signal goes HIGH. Thus, the overall delay of the SAR logic block is minimized. Chapter 6 presents a critical path analysis of the overall SAR sub-ADC as well as the SAR logic block. Figures B.12, B.13 and B.14 in Appendix B.1 show the circuit schematics of the three types of DFFs used in the SAR logic block.

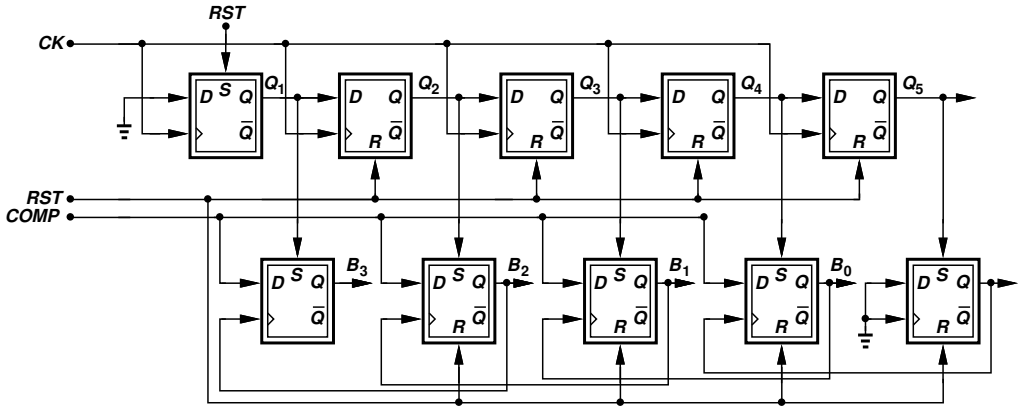


Figure 5.16: 4-bit SAR Logic Block

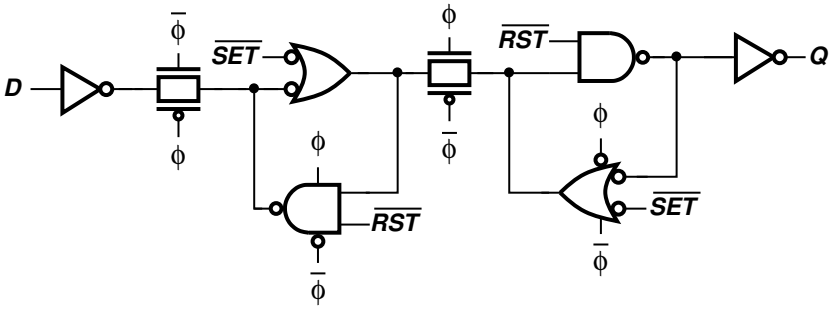


Figure 5.17: Custom Set-Reset D Flip-flop

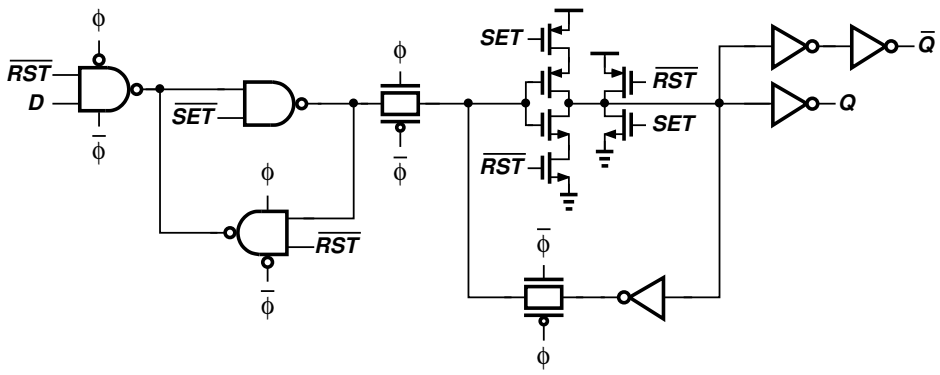


Figure 5.18: Custom Set-Reset D Flip-flop

5.3 Simulation Results

This section gives the simulation results of the single channel 4-bit sub-ADC as well as the performance of the overall 8-channel time-interleaved ADC.

5.3.1 Single-Channel Simulation Results

Figure B.2 in Appendix B.1 shows the top-level test-bench schematic of the 4-bit SAR sub-ADC implemented. The 4-bit sub-ADC was tested using the 625 MHz sampling clock frequency. The bits generated from the SAR logic block were sampled using the re-sampling clock and stored in a D flip-flop. The final sampled binary code ($b_3b_2b_1b_0$) was then converted to decimal to give the quantized output waveform. A 128-point FFT on the quantized output gives us an SNR of 23.84 dB for a low-frequency input and an SNR of 24.32 for a high-frequency (2.49 GHz) input signal. Figures 5.19 and 5.20 show the spectrum of the output for two cases. Since the sampling frequency for the single channel case does not satisfy the Nyquist theorem with this input signal, the output aliases to a lower frequency and thus apppear to be near the DC value.

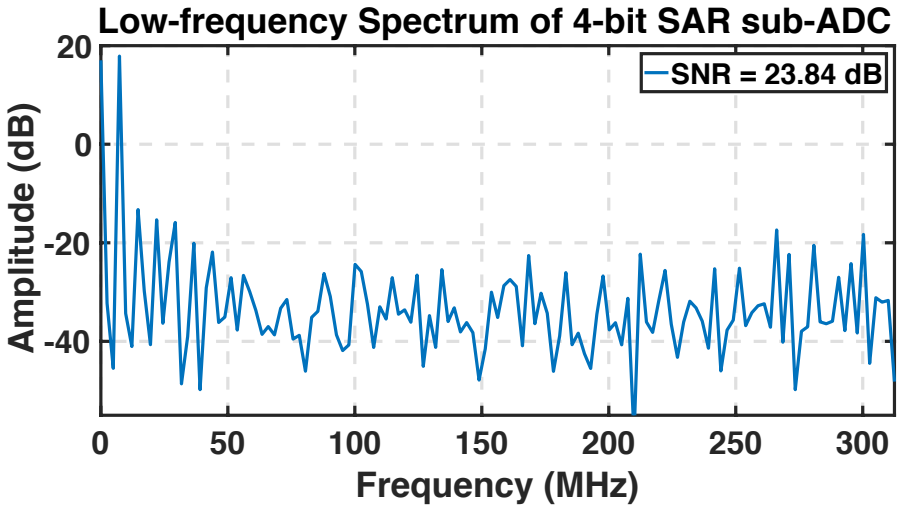


Figure 5.19: Output Spectrum of the 4-bit SAR Sub-ADC Using a Low-Frequency Input Signal

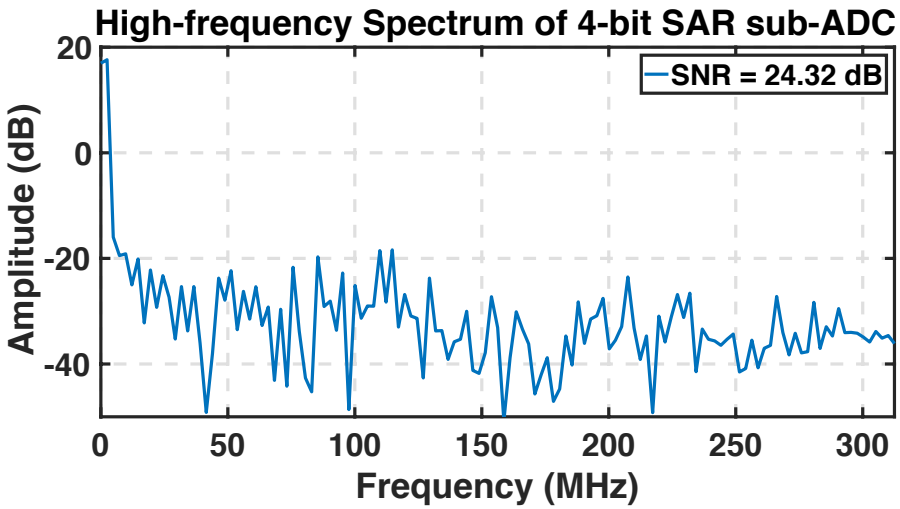


Figure 5.20: Output Spectrum of the 4-bit SAR Sub-ADC Using a High-Frequency Input Signal

5.3.2 Time-interleaved ADC Simulation Results

The single-channel 4-bit SAR ADC design is used as a sub-ADC in an 8-channel time-interleaved ADC. Eight copies of the 4-bit SAR sub-ADC each clocked at 625 MHz are operated in parallel on different phases of the sampling clock each 45 degrees apart. This causes the different sub-ADCs to operate on different input samples. The output from each of the sub-ADCs is then time-interleaved, creating an ADC operating at 8 times the frequency of each single-channel sub-ADC, i.e. at 5 GHz. Figure B.15 in Appendix B.1 shows the top-level test-bench schematic of the 8-channel time-interleaved 4-bit SAR sub-ADC implemented.

The ADC consumes a power of 42.6 mW, effective number of bits (ENOB) of 3.74 and figure-of-merit (FoM) of 638 fJ/conversion-step for an input close to Nyquist frequency. Figures 5.21 and 5.22 show the output spectra of the ADC with a low-frequency and high-frequency input respectively. The ADC achieves an SNR of 23.7 dB for a low-frequency input signal and a SNR of 24.30 dB for a high-frequency input.

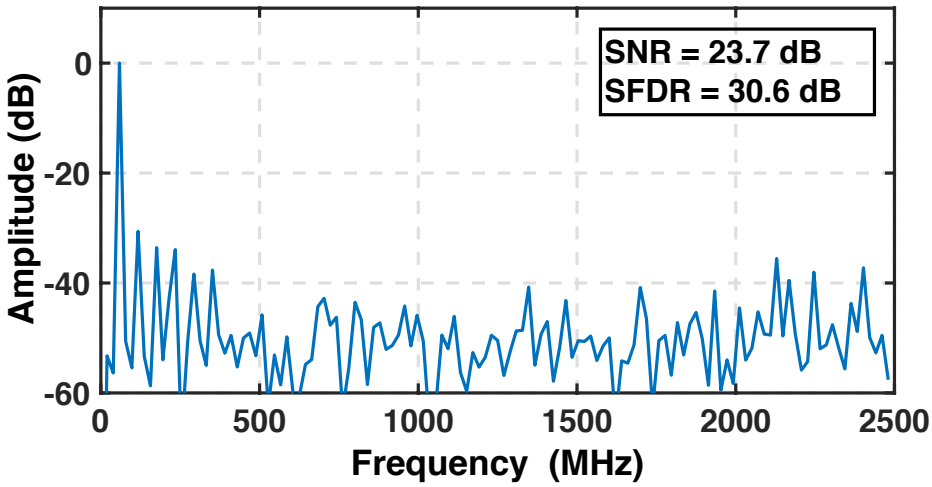


Figure 5.21: Low-Frequency Output Spectrum of 8-channel Time-interleaved SAR ADC

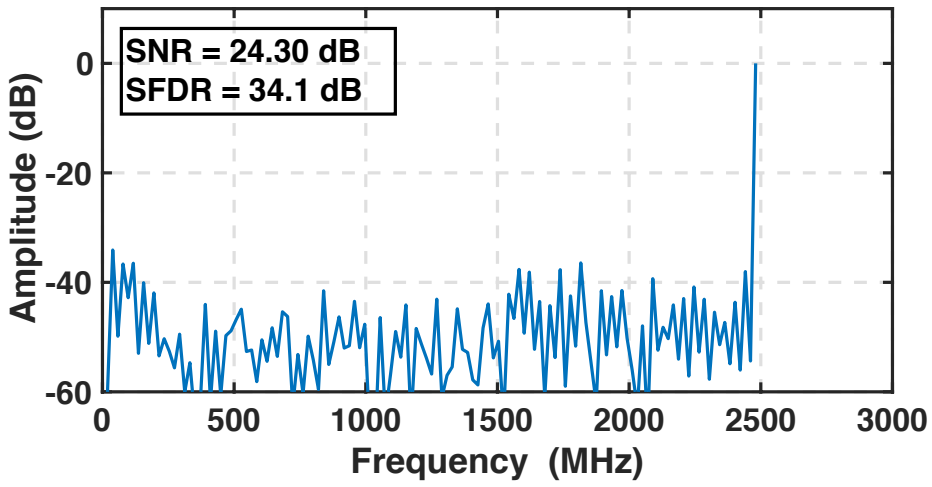


Figure 5.22: High-Frequency Output Spectrum of 8-channel Time-interleaved SAR ADC

CHAPTER 6

SAR ADC CRITICAL PATH ANALYSIS

The speed of a single-channel synchronous SAR ADC is limited by the minimum time required for the SAR loop to settle. The SAR loop shown in Fig. 6.1 consists of 4 main blocks — the Sampling Network CDAC, the Comparator, the SAR Logic Block and the Switch Drivers. The sum of the delays through these 4 blocks — the sampling network settling time (t_{DAC}), the comparator decision time (t_C), the SAR logic delay (t_{SL}) and the switch driver delay (t_D) - determine the maximum speed at which the SAR ADC can operate [28].

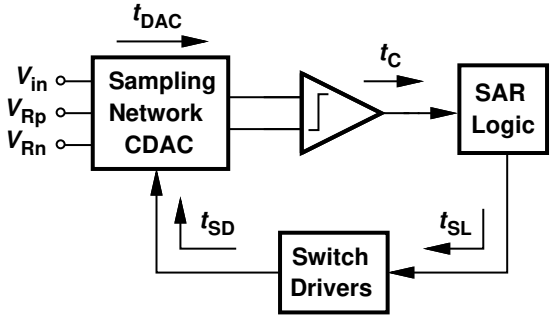


Figure 6.1: The SAR Loop

The CDAC settling time depends on the size of the capacitors and switches used. Tripathi and Murman [28] suggest an optimization method by which this delay can be reduced. The comparator decision time depends on the difference between the inputs of the comparator. The smaller the difference in the inputs, the longer it takes for the comparator output to resolve [29]. The loading of the switch drivers determines the delay through them. The smaller the load, the faster the driver and lesser the power burnt in them.

The main delay of the SAR loop is due to the digital SAR logic block. An N-bit SAR ADC using a conventional SAR logic block contains two chains of D flip-flops (DFFs) each consisting of $N+1$ DFFs. The first flip-flop in each

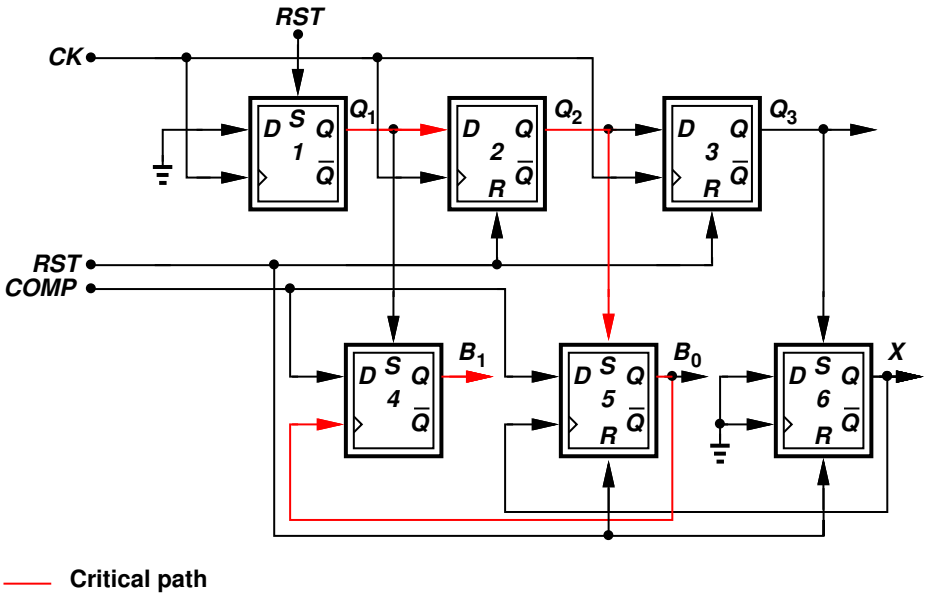


Figure 6.2: A 2-bit SAR Logic Block

chain is a DFF with an asynchronous set (DFFS). The top chain consists of N DFFs with an asynchronous reset (DFFR) while the bottom chain consists of N DFFs with asynchronous set-reset (DFFSR).

Figure 6.2 shows the SAR logic block for a 2-bit SAR ADC and Fig. 6.3 shows its timing diagram. The outputs Q_1, Q_2 and Q_3 serve as pointers to the bit being resolved and SET the outputs of the bottom chain DFFs to HIGH when clocked by Φ_{CK}. The bottom chain of flip-flops with outputs B_1 and B_0 are each clocked by it successive DFF. At the positive edge of the clock Φ_{CK}, Q_2 goes HIGH, setting B_0 HIGH, this clocks the DFF4 and causes B_1 to latch to the comparator value.

The latched value of B_1 during the bit-cycling phase is then applied to the sampling network at the next positive edge of the bit cycling-clock, Φ_{BC}. B_1 thus needs to latch to the right value within half a clock period ($\frac{T_{CK}}{2}$) after the occurrence of the rising edge of Φ_{CK}. Thus, the path from the input of DFF2 to DFF5 to the output of DFF4 forms the critical path of the SAR logic block. Since the comparator is clocked at the rising edge of Φ_{CK} as well, it is important that the comparator output settles to the right value before B_1 is clocked and latched. Thus, for proper functioning of the SAR logic block it is important that the inequality given by (6.1) is satisfied.

$$t_{CQ_2} + t_{SQ_5} > t_C + t_{SU_4} \tag{6.1}$$

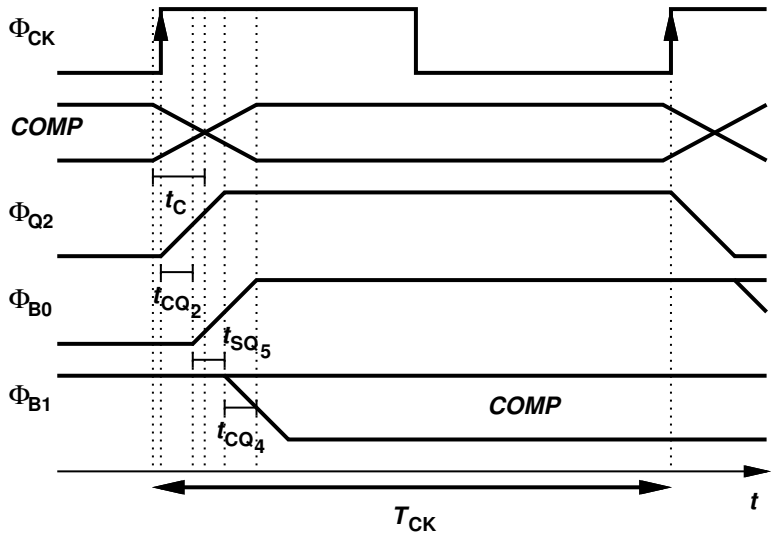


Figure 6.3: Timing Diagram of 2-bit SAR Logic Block with Critical Path Delays

$$\begin{aligned} where,\ t_{CQ_2}: &\ \text{clock-to-Q delay of DFF2} \\ t_{SQ_5}: &\ \text{set-to-Q delay of DFF5} \\ t_C: &\ \text{comparator decision time} \\ t_{SU_4}: &\ \text{set-up time of DFF4} \end{aligned}$$

The speed at which the SAR logic block can operate is thus limited by the speed of the comparator and the DFFs.

$$t_C + t_{CQ_2} + t_{SQ_5} + t_{CQ_4} < \frac{T_{CK}}{2} \tag{6.2}$$

The maximum bit-cycling frequency, $f_{CK_{max}}$ [1] is thus given by equation 6.3.

$$\therefore\ f_{CK_{max}} < \frac{1}{2(t_C + t_{CQ_2} + t_{SQ_5} + t_{CQ_4})} \tag{6.3}$$

$$where,\ T_{CK}: \text{ time period of the bit-cycling clock}$$

[1] The maximum bit-cycling frequency is the maximum frequency at which the bits in a single-channel SAR ADC can be resolved.

Table 6.1: Critical Path Delays

	Custom DFF Delay	**Conventional DFF Delay**	**% improvement**
t_C **w/ 800μV offset**	98.35 ps	98.35 ps	0%
t_C **w/ 1LSB offset**	84.7 ps	84.7 ps	0%
t_{CQ_2}	21.69 ps	34 ps	36.2%
t_{SQ_5}	20.42 ps	50 ps	59.2%
t_{CQ_4}	30 ps	42 ps	28.6%
T_{total}	**156.81 ps**	**210.7 ps**	**25.6%**

Table 6.1 shows the values of the delays in the critical path and compares the delays of the custom DFFs used in the SAR sub-ADC design with that of a conventional DFF.

CHAPTER 7

SAR QUANTIZER PERFORMANCE ENHANCEMENT

The performance of the SAR quantizer can be further enhanced by increasing the number of ADC bits. The 4-bit SAR ADC design described in chapter 5 is thus extended to form an 8-bit SAR ADC. As the number of bits in an ADC increases, the sizes of the sampling network capacitors and power consumed by buffers to drive large capacitances increase accordingly. Therefore, various design changes need to be made to ensure high-speed performance at low power for the increased ADC resolution. In this chapter, the design of a 16-channel time-interleaved 5 GS/s 8-bit SAR ADC using synchronous SAR logic and several speed enhancement techniques has been described. Each sub-ADC is designed to operate at 1/16th the clock frequency, i.e. at a sampling frequency of 312.5 MHz. Similar to the 4-bit SAR ADC, the operation of the 8-bit SAR ADC is split into two phases - the sampling phase and the bit-cycling phase. The bit-cycling phase, however, requires 8 rising edges to process the 8-bits compared to the four edges used in the 4-bit case and hence the clock frequency is divided by 1/16th. The bit-cycling clock thus consists of 8 pulses during the bit-cycling phase. The clocking scheme of the 8-bit SAR sub-ADC is the same as the 4-bit SAR in terms of the relevant clocks used in the SAR sub-ADC. The relevant clocks are also generated in same manner as they are in the 4-bit case. Similarly, the same comparator block is used in both the ADCs. The significant change in design for the 8-bit sub-ADC is made in the sampling network and the multi-phase clock generator and has been described in this chapter.

7.1 Multi-phase Clock Generator

The 8-bit SAR ADC requires 16-channel time-interleaving; thus, 16 phases of the sampling clock need to be generated. Similar to the 4-bit ADC, the multi-

phase clock generator for the 8-bit sub-ADC consists of a CML to CMOS converter followed by a Johnson counter. The 16-phases of the sampling clock are generated using a 16-phase Johnson counter. The 16-phase Johnson counter (Fig. 7.1) was built using 8 D flip-flops. The outputs of the 8 DFFs and their respective complements give the desired 16 phases of the sampling clock, with each phase 22.5 degrees apart. Figure 7.2 shows the master clock and the 16 phases of the sampling clock generated.

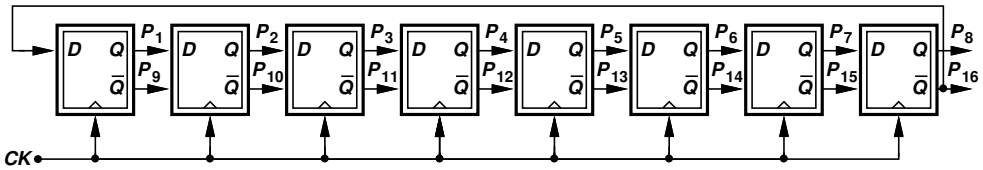


Figure 7.1: 16-phase Johnson Counter

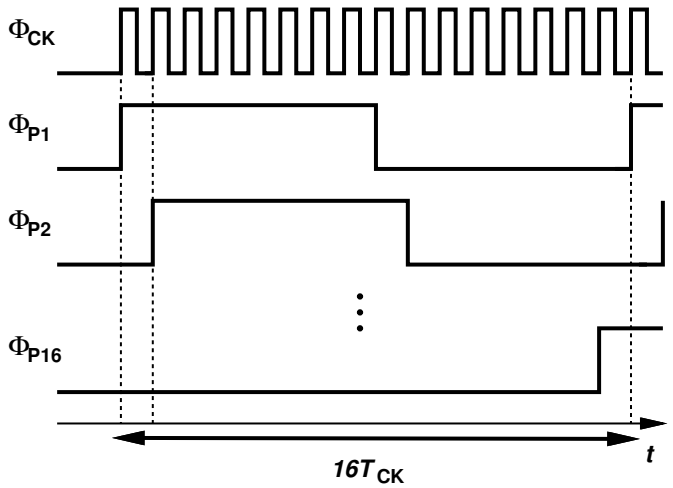


Figure 7.2: 16 Phases of the Sampling Clock

7.2 8-bit SAR sub-ADC

7.2.1 Sampling Network

Several sampling network topologies were explored before designing the sampling network for the 8-bit SAR ADC. Several sampling network topologies have been used in SAR ADCs in literature, such as binary weighted CDAC

[28], split-capacitive array DAC with unit bridge capacitor [30] and C-2C ladder [31]. In order to reduce the capacitive loading of the sampling network, the split-array topology with a unit bridge capacitor was used to design the 8-bit sampling network. The reduced capacitor size of the sampling network reduces the loading of the input buffer as well as the reference buffers, thereby reducing the power consumed by them [32].

Binary weighted CDACs are good for low-resolution SAR ADCs (< 6 bits) but as the number of bits increases the size of the capacitor array, and thus the area of sampling network, increases exponentially. An N-bit binary weighted SAR requires 2^N unit capacitors (C). The size of the sampling network capacitance can be significantly reduced by using the split-capacitor SAR. An N-bit SAR using this structure only requires $2^{\frac{N}{2}+1} - 1$ unit capacitors. Thus, the split CDAC for the 8-bit SAR sub-ADC uses 31 unit-capacitors (C) with an input loading of 16C compared to a binary-weighted CDAC that would use 256 unit capacitors with an input loading of 256C. Therefore, the input capacitance and area occupied by the sampling network is significantly reduced compared to the binary-weighted capacitor topology. A split-array with a unit bridge capacitor rather than a fractional bridge capacitor is used as a fractional bridge capacitor causes poor matching with the other capacitors [16].

Although the C-2C sampling network occupies the least area as it only requires $3 * N$ capacitors [31] for a N-bit ADC, it suffers significantly due to top and bottom-plate parasitics compared to the split-capacitor SAR. The split-capacitor SAR also suffers from top and bottom-plate parasitics of the bridge capacitor [30] as well as a 1LSB gain error [16]; however, as seen from the simulation results in section 7.3 this does not cause significant degradation in the SNR for a medium resolution ADC.

The 8-bit sampling network CDAC uses two 4-bit capacitor arrays to serve as the LSB and MSB arrays. The same capacitor array as the one designed for the 4-bit SAR is used after removing the dummy capacitors that were present in the 4-bit SAR array. Figure 7.3 shows a single-ended implementation of the differential sampling network CDAC used in the 8 bit SAR sub-ADC. The value of bridge capacitor C_b is equal to the unite capacitance C. The unit capacitance C, is designed to be as small as permitted by the thermal noise requirement, and is chosen to be of 10 fF. The switches S_1-S_9 are sized such that the RC time constant of each switch-capacitor pair is the same,

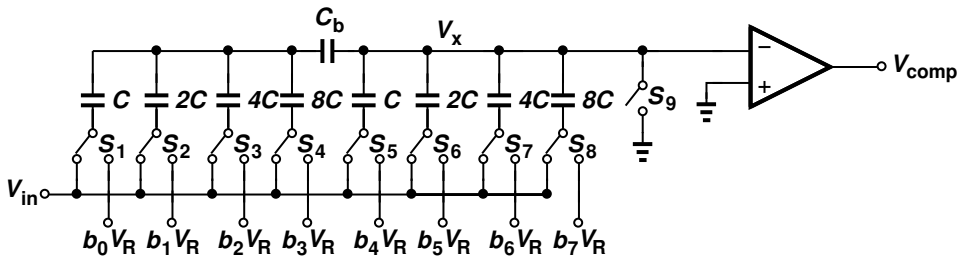


Figure 7.3: Single-ended 8-bit SAR Sampling Network Implementation

i.e. $S_1 \times C = S_2 \times 2C$. The sampling network uses all PMOS switches with the minimum sized switch, S_1 having a width of 1μm.

7.2.2 8-Bit SAR Logic Block

The 4-bit SAR logic block designed for the 4-bit SAR ADC is extended to build the SAR logic block for the 8-bit SAR. Figure 7.4 shows the 8-bit SAR logic block used in the 8-bit SAR ADC. The 8-bit implementation of the SAR logic block consists of two chains of D flip-flops (DFF) consisting of 9 DFFs each. The signals $B_7B_6B_5B_4B_3B_2B_1B_0$ gives the 8-bit output of the SAR ADC.

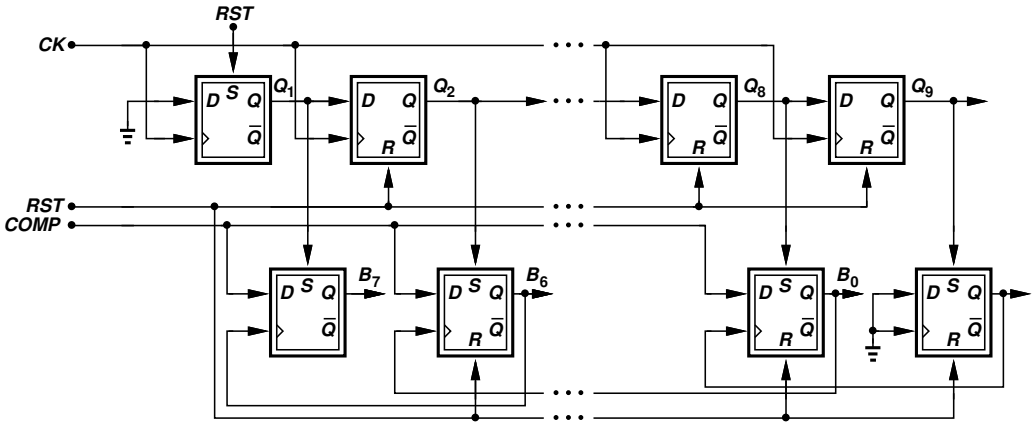


Figure 7.4: 8-bit SAR Logic Block

7.3 Simulation Results

The ADC is designed in 65 nm CMOS and uses a supply voltage of 1.2 V. A common-mode voltage of 1.1 V is used and positive and negative reference voltages of 1.3 V and 0.9 V are used respectively. This section gives the simulation results of the single channel 8-bit sub-ADC as well as the performance of the overall 16-channel time-interleaved ADC.

7.3.1 Single-Channel Simulation Results

Figure B.16 in Appendix B.3 shows the top-level test-bench schematic of the 8-bit SAR sub-ADC implemented. The 8-bit sub-ADC was tested using the 312.5 MHz sampling clock frequency. The bits generated from the SAR logic block are sampled using the re-sampling clock and stored in a D flip-flop. The final sampled binary code ($b_7b_6b_5b_4b_3b_2b_1b_0$) is then converted to decimal to give the quantized output waveform. The 8-bit SAR sub-ADC was tested using both an ideal sampling network consisting of ideal switches as well as the real sampling network consisting of the PMOS switches.

The SAR ADC consisting of the ideal sampling network gives us an SNR of 45.67 dB which is close to the expected value of 50 dB for an 8-bit ADC. The SAR ADC consisting of the real sampling network gives us an SNR of 45.09 dB for a low-frequency input signal which is a little lower than expected. Figure 7.5 shows the frequency spectrum of the output for the two sampling network cases. Figure 7.6 shows the output spectrum for a high-frequency input signal of 2.49 GHz. Since the sampling frequency for the single channel case does not satisfy the Nyquist criterion with this input signal, the output aliases to a lower frequency and thus apppears to be near the DC value. The SNR in this case is 44.17 dB.

This degradation in SNR can be attributed to two factors: the race condition in the SAR logic block and the parasitic effects at the capacitor input node. On further examining the circuit, it is seen that there is a race condition between when the right comparator output is latched onto the output bits of the SAR logic block and when the next bit is applied to the sampling network during the bit-cycling phase. A frequency of 5 GHz does not provide the output of the SAR logic block sufficient time to settle to the right value within half a clock cycle. The effects of this race can be mitigated by op-

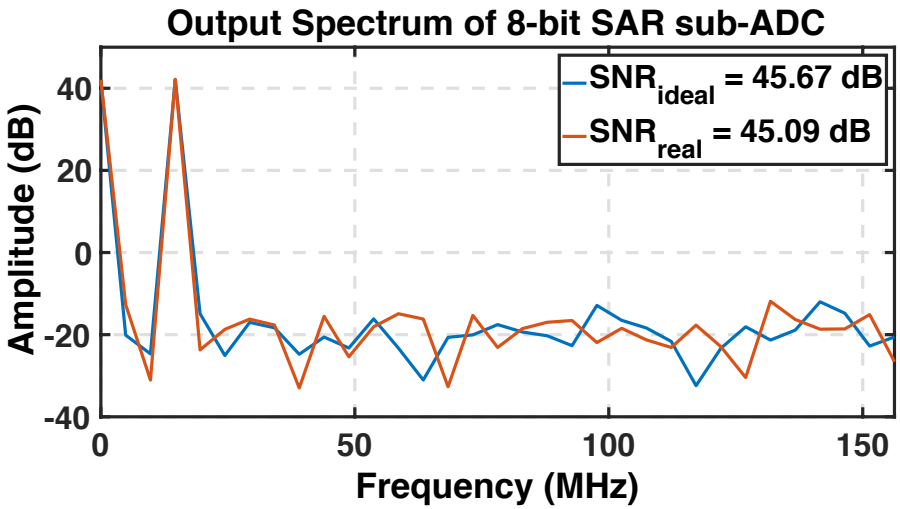


Figure 7.5: Low-Frequency Output Spectrum of the 8-Bit SAR sub-ADC Using Ideal and Real Switches

erating the SAR ADC at a lower frequency. This issue can also be resolved by reducing the duration of the sampling phase and increasing the time for the bit-cycling phase. This would provide a longer time for bit-cycling to occur and thus give the SAR logic outputs a longer time to settle. The parasitic capacitance resulting from the top and bottom plate capacitance of the bridge capacitor introduces a mismatch between the LSB and MSB array. This in turn contributes to the degradation in the SAR ADC's performance. Capacitors can be connected across the bridge capacitor and in parallel with the LSB array to combat the effect of the parasitic capacitance introduced at the comparator input [16].

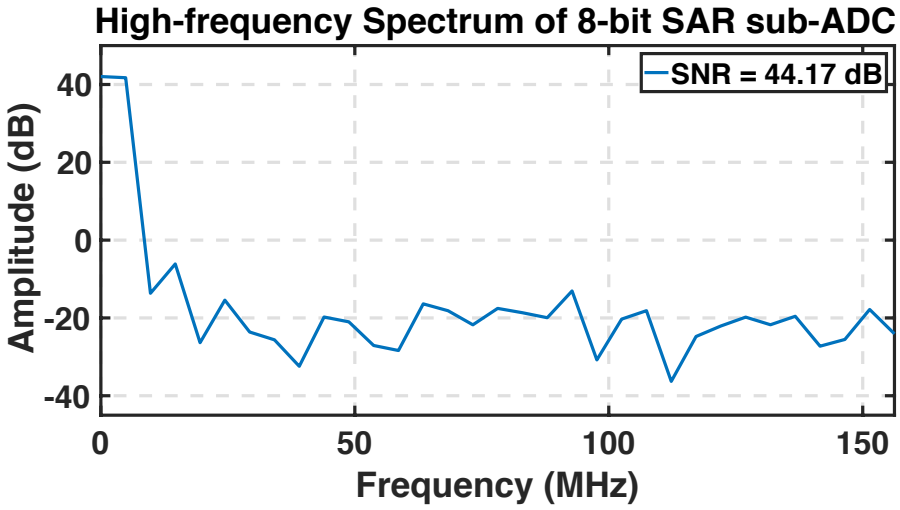


Figure 7.6: Output Spectrum of the 8-bit SAR Sub-ADC Using a High-Frequency Input Signal

Table 7.1: Power Breakdown

	Power [mW]	**Percentage**
Comparator	29.70	32.00%
Clock	56.40	60.80%
SAR Logic	6.36	6.85%
Reference	0.36	0.38%
Total	**92.8**	**100%**

7.3.2 Time-interleaved ADC Simulation Results

The single-channel 8-bit SAR ADC design is used as a sub-ADC in a 16-channel time-interleaved ADC. Sixteen copies of the 8-bit SAR sub-ADC each clocked at 312.5 MHz are operated in parallel on different phases of the sampling clock each 22.5 degrees apart. This causes the different sub-ADCs to operate on different input samples. The output from each of the sub-ADCs is then time-interleaved, creating an ADC operating at 16 times the frequency of each single-channel sub-ADC, i.e. at 5 GHz. Figure B.22 in Appendix B.3 shows the top-level test-bench schematic of the 16-channel time-interleaved 8-bit SAR sub-ADC implemented.

The ADC consumes a power of 92.8 mW at 5 GS/s when the input is at Nyquist frequency. Table 7.1 shows a breakdown of the power consumed by the different circuit components.

Figures 7.7 and 7.8 show the output spectra of the ADC with low-frequency and high-frequency inputs respectively. The degradation in SNR for a high-frequency input is due to the timing mismatch in time-interleaving.

An input close to Nyquist frequency gives SNR of 41.5 dB and a SFDR of 46.3 dB. The effective number of bits (ENOB) at Nyquist of the ADC given by (7.1) is 6.60 and the Walden figure-of-merit (FoM) given by (7.2) is 191 fJ/conversion-step. Table 7.2 summarizes the performance of the ADC and compares it with state-of-the-art ADCs [33].

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02} \tag{7.1}$$

$$FoM = \frac{Power}{2^{ENOB} \times f_S} \text{ [J/conv-step]} \tag{7.2}$$

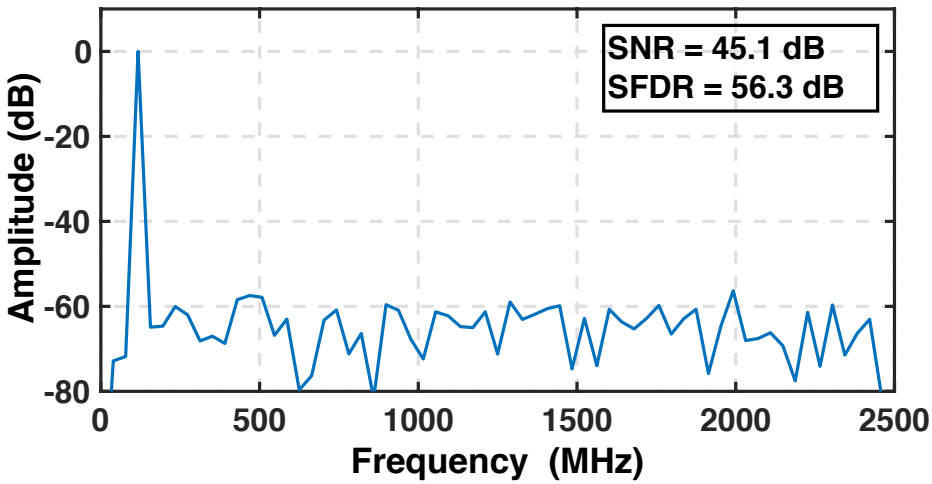


Figure 7.7: Low-Frequency Output Spectrum of 16-channel Time-interleaved SAR ADC

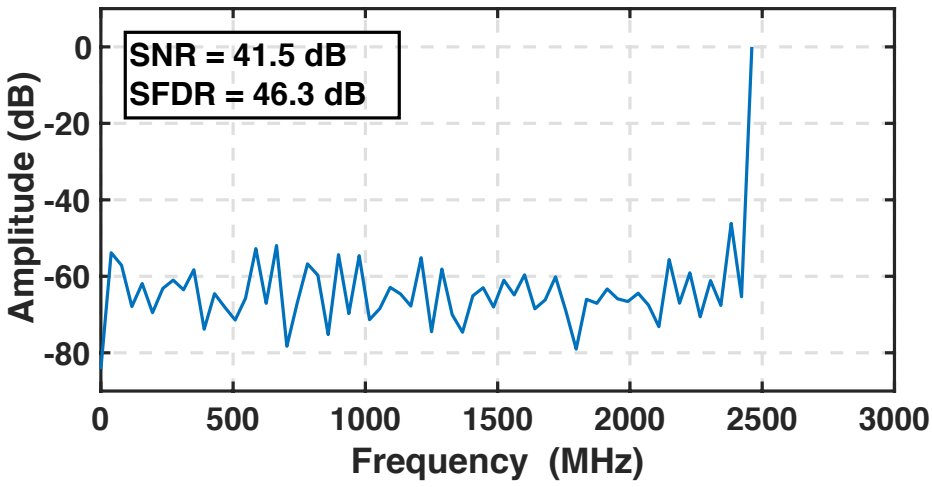


Figure 7.8: High-Frequency Output Spectrum of 16-channel Time-interleaved SAR ADC

Table 7.2: Performance Comparison

	This work	**[34]**	**[35]**	**[36]**	**[31]**	**[37]**
Architecture	Ti-SAR	Ti-SAR	Ti-SAR	Folding Flash	Ti-SAR	Ti-Pipeline
Technology [nm]	65	40	45	40	65	350
Resolution [bits]	8b	8b	6b	7b	7b	8b
Sampling Rate [GS/s]	5	2	5	2.2	2.5	4
Supply Voltage (V)	1.2	-	1	1.1	1.1	3.3
Power [mW]	92.8	54.2	50.0	27.4	50.0	4600.0
SNDR [dB]	41.5	39.4	30.8	37.4	34	39.1
SFDR [dB]	46.3	55.13	43	44	45	-
ENOB	6.60	6.25	4.8	5.9	5.4	6.20
FoM [fJ/conv-step]	191	355	39	205.7	555.1	15642

CHAPTER 8

CONCLUSION

In this thesis high-speed successive approximation register based analog-to-digital converters are implemented in 65 nm CMOS with the motivation to use them in a high-speed delta-sigma modulator. An 8-channel 4-bit time-interleaved SAR analog-to-digital converter operating at a sampling rate of 5GS/s is implemented using synchronous successive approximation logic. A single channel in the 4-bit ADC achieves a signal-to-noise ratio (SNR) of 23.84 dB for a low-frequency input and SNR of 24.32 dB for an input signal close to Nyquist. The 8-channel time-interleaved 4-bit SAR ADC consumes power of 42.6 mW, achieves ENOB of 3.74 and FoM of 638 fJ/conversion-step. The time-interleaved ADC achieves SNR of 23.7 dB for a low-frequency input and SNR of 24.3 dB for a high-frequency input signal.

The implementation of the 4-bit SAR ADC is extended to 8-bit to implement an 8-bit SAR ADC operating at a sampling rate of 5GS/s using 16-channel time-interleaving. The single-channel sub-ADCs achieve SNR of 45.09 dB and 44.17 dB for low- and high-frequency input signals respectively. The 16-channel time-interleaved 8-bit SAR ADC achieves ENOB of 6.6 bits, figure-of-merit of 191 fJ/conversion-step and power consumption of 92.8 mW. The 8-bit time-interleaved ADC achieves SNR of 41.5 dB and SFDR of 46.3 dB for input signals close to Nyquist.

The high-speed operation of the SAR ADCs is achieved by optimizing the delays in the SAR loop. A critical path analysis for the delays in a SAR ADC using synchronous SAR logic and an analysis of the maximum achievable frequency of operation has also been presented.

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APPENDIX A

SIMULINK MODELS

This appendix contains the Simulink models used to implement the MOD2 and MOD5 ADCs.

A.1 Second-order Delta-Sigma Modulator Simulink Models

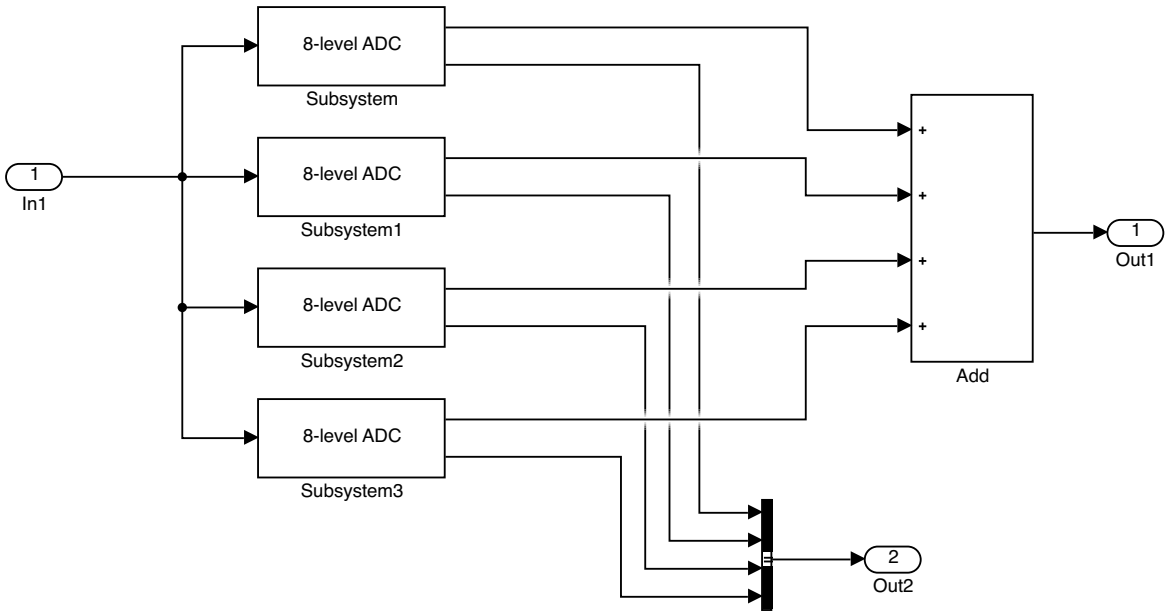

Figure A.1: Simulink Model of 33-level Flash ADC

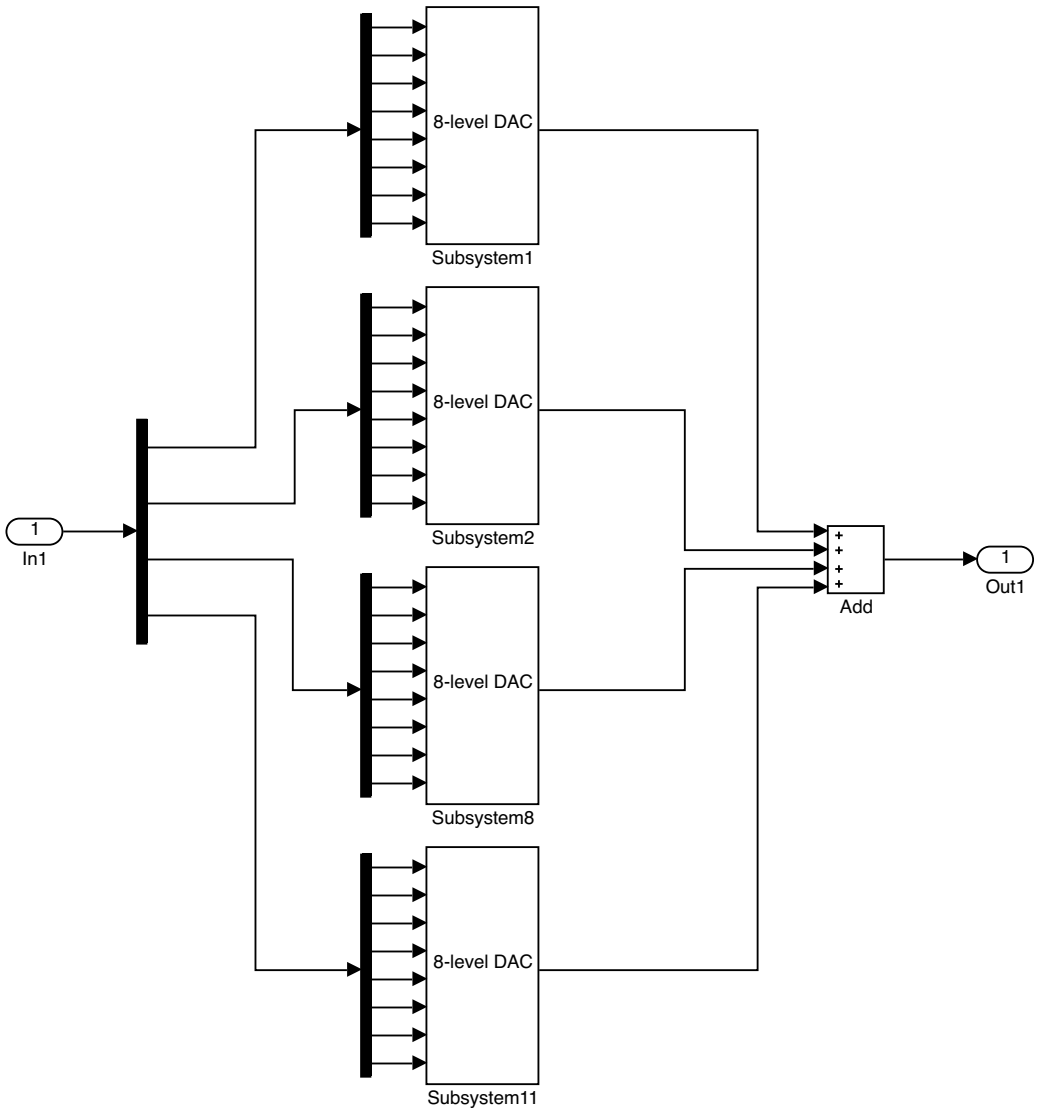

Figure A.2: Simulink Model of 33-level DAC

APPENDIX B

CADENCE SCHEMATICS

This appendix contains Cadence schematics of the 4-bit SAR sub-ADC, the 8-channel TI 4-bit SAR ADC, the 8-bit SAR sub-ADC and the 16-channel TI 8-bit SAR ADC.

B.1 4-Bit SAR sub-ADC Schematics

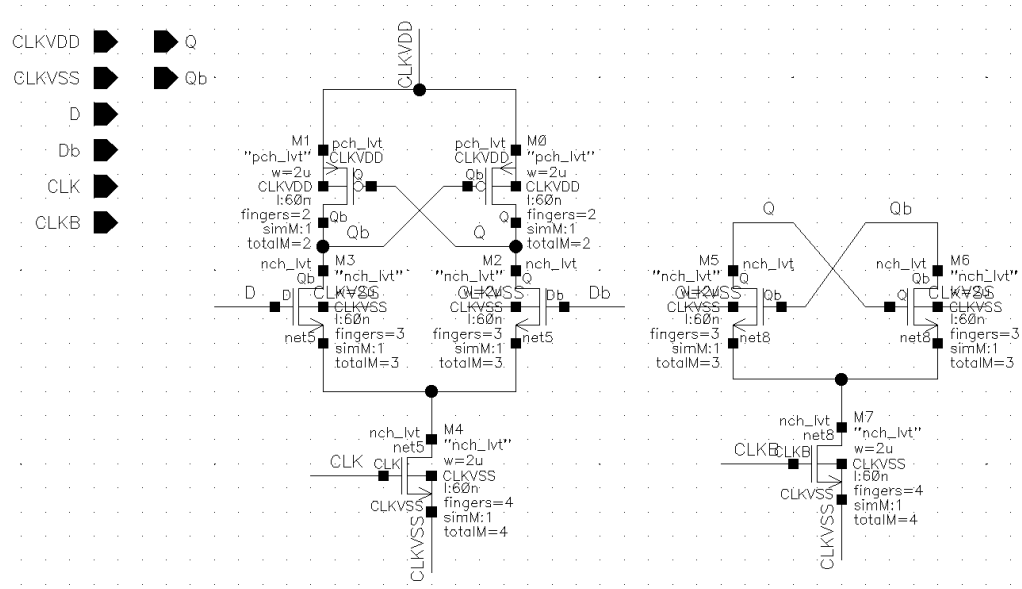

Figure B.1: CML D-Latch

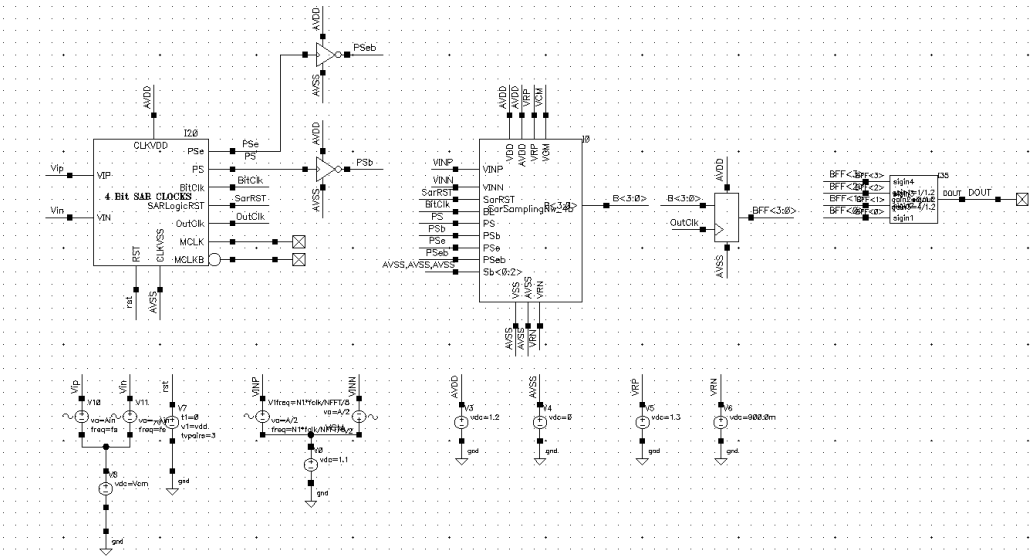

Figure B.2: Top-level Test-bench Schematic for 4-bit SAR ADC

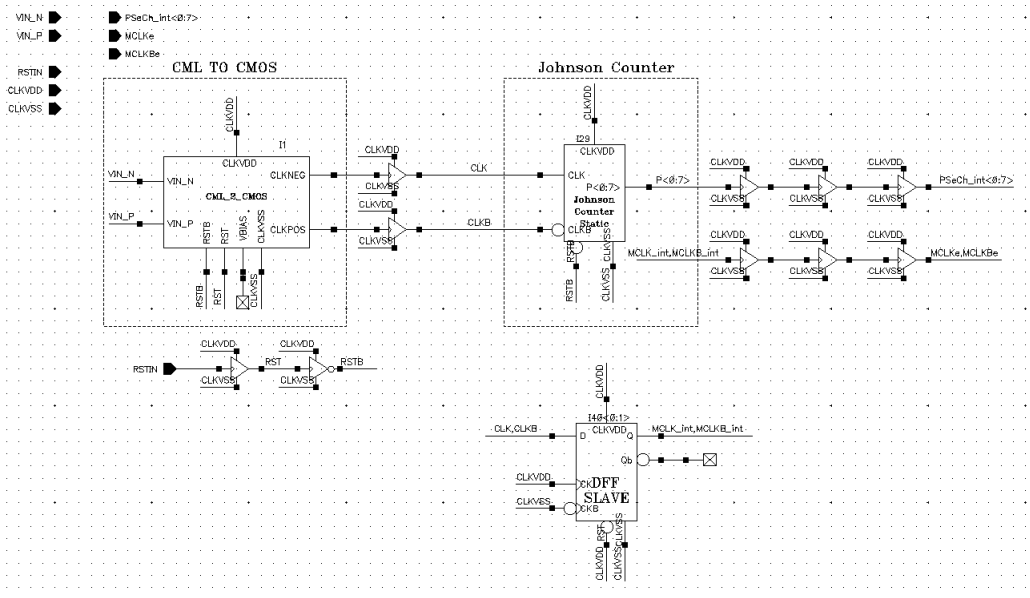

Figure B.3: 8 Phase Clock Generator

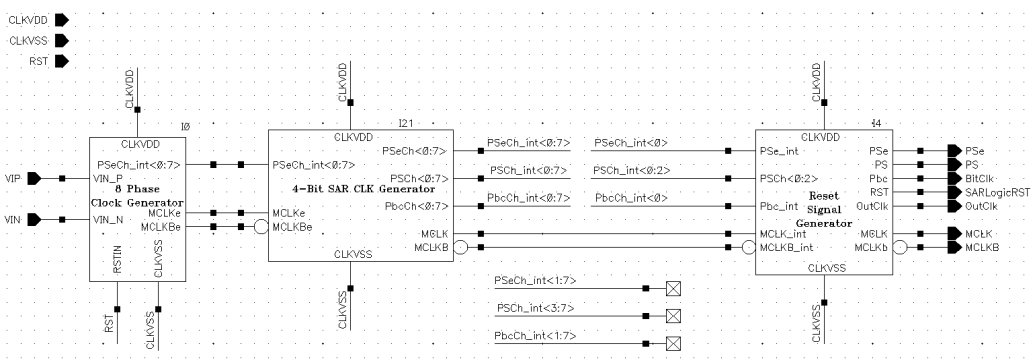

Figure B.4: Clocks for 4-Bit SAR

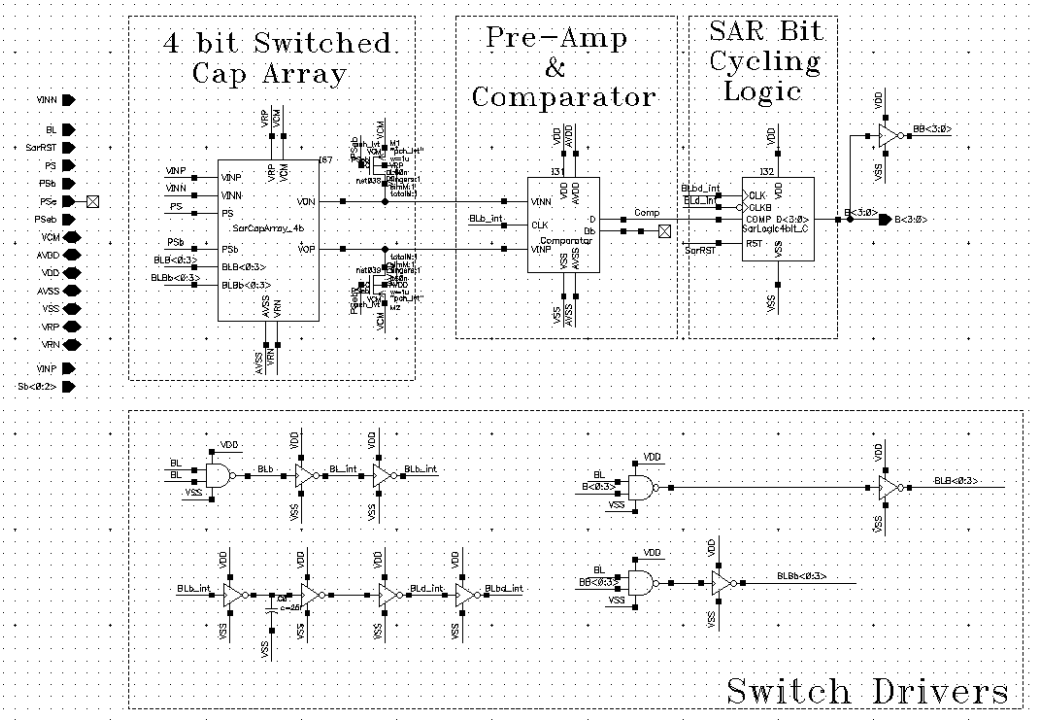

Figure B.5: 4-bit SAR ADC

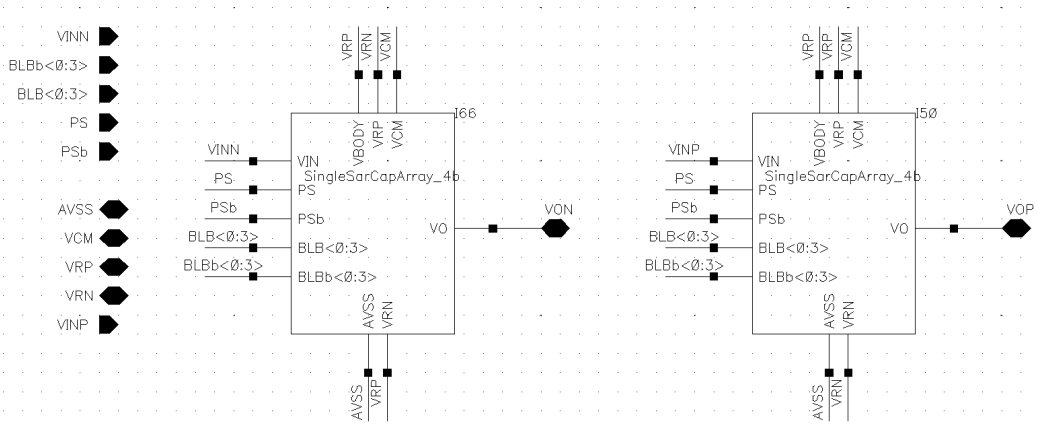

Figure B.6: 4-bit Differential SAR Sampling Network

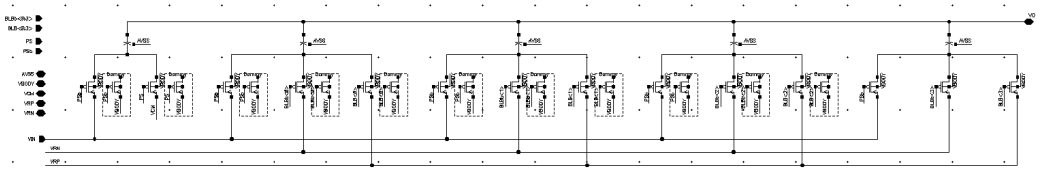

Figure B.7: Differential Half-circuit of 4-bit SAR Sampling Network

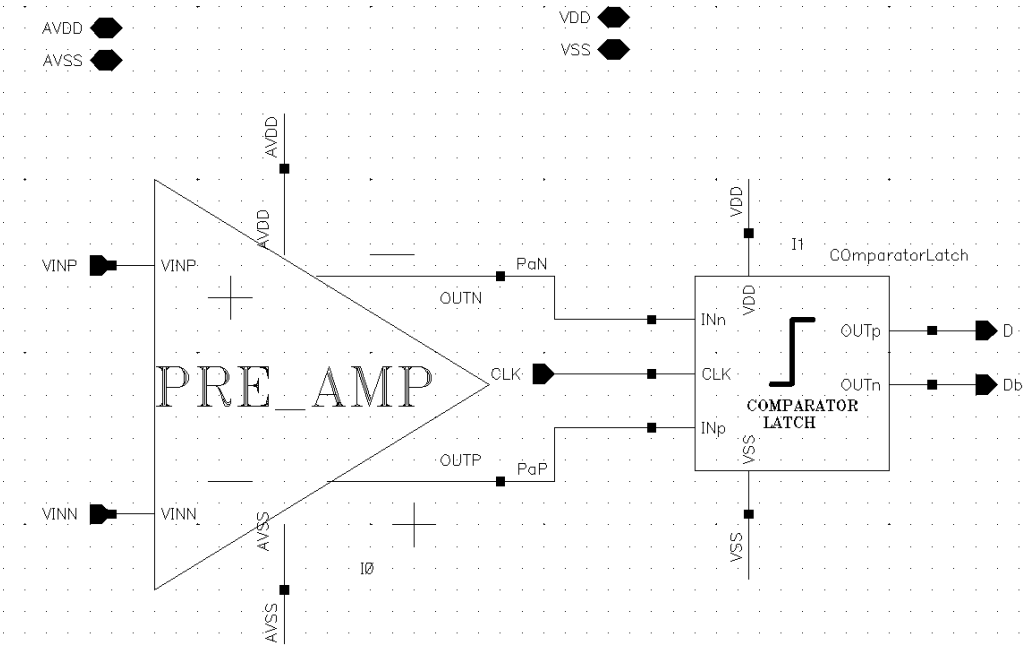

Figure B.8: The Comparator Block

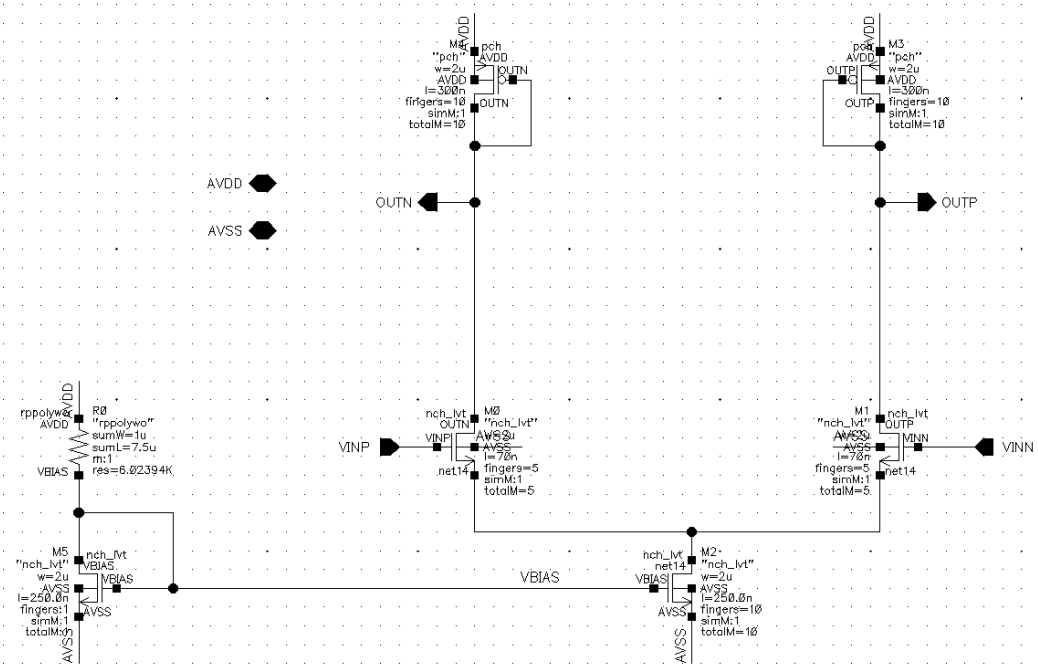

Figure B.9: The Pre-amplifier

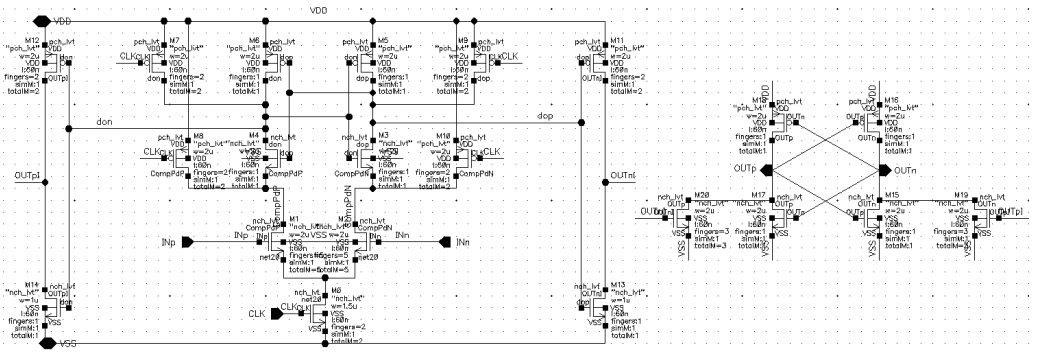

Figure B.10: The Comparator-latch

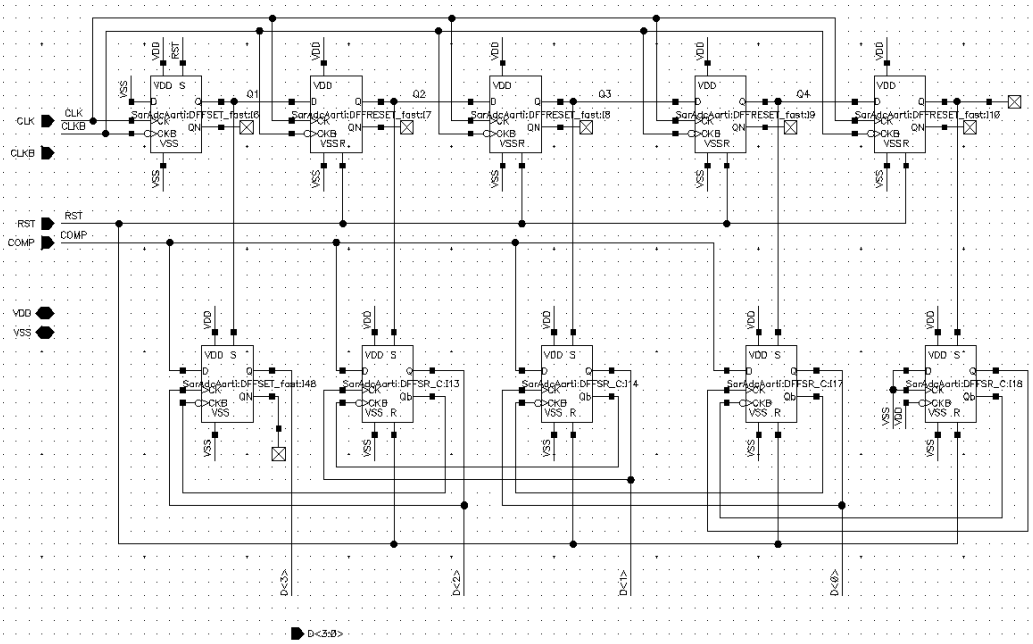

Figure B.11: 4-bit SAR Logic Block

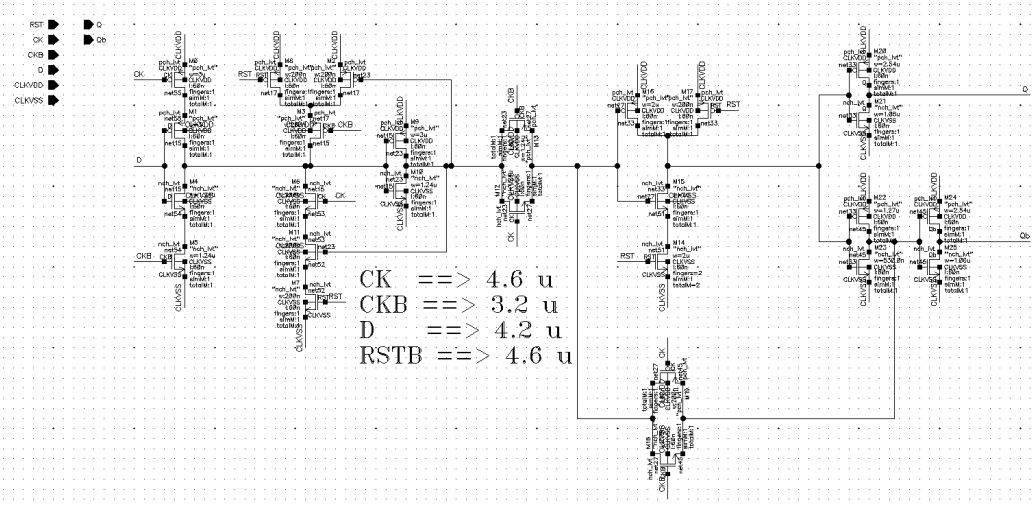

Figure B.12: D Flip-flop with Asynchronous Reset

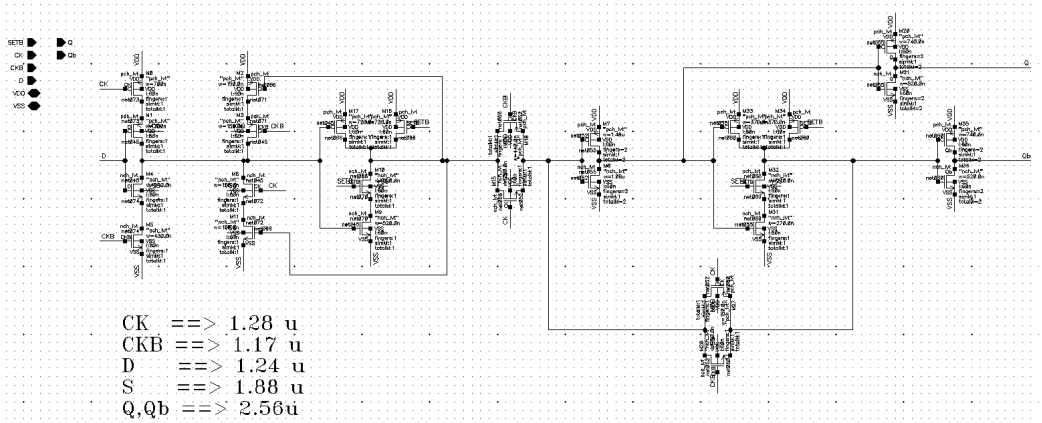

Figure B.13: D Flip-flop with Asynchronous Set

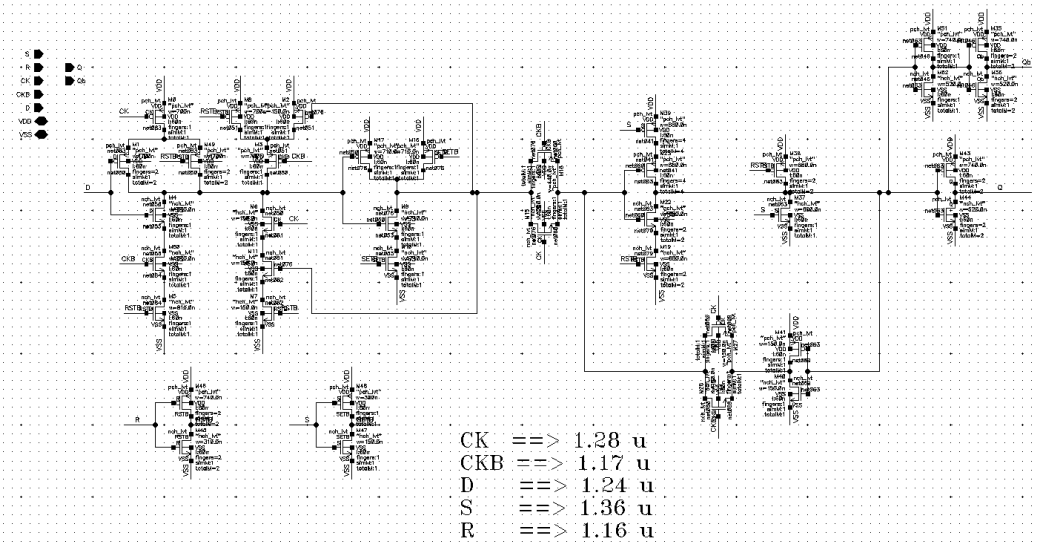

Figure B.14: D Flip-flop with Asynchronous Set-Reset

B.2 8-channel Time-interleaved 4-Bit SAR ADC Schematics

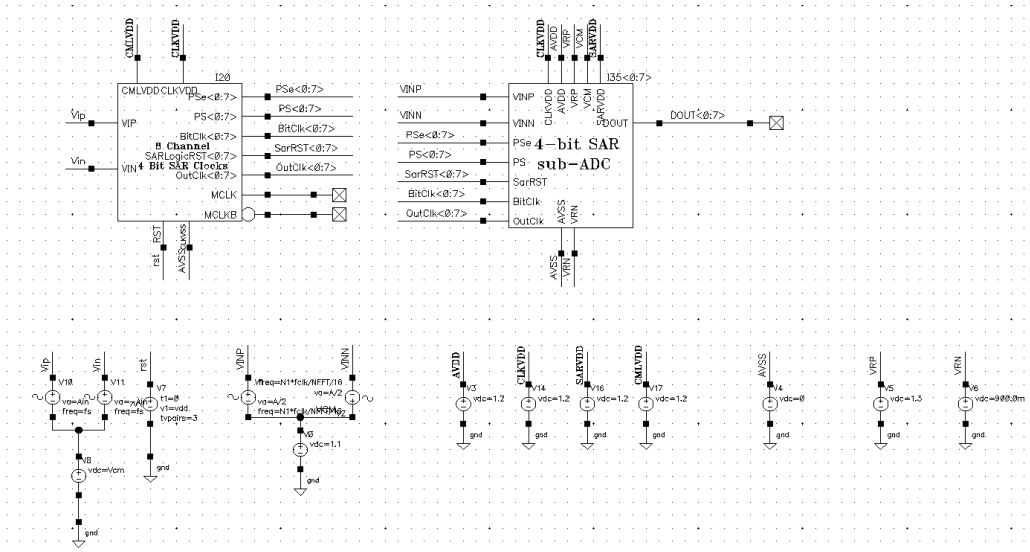

Figure B.15: Top-level Test-bench Schematic for 8-channel Time-interleaved 4-bit SAR ADC

B.3 8-Bit SAR sub-ADC Schematics

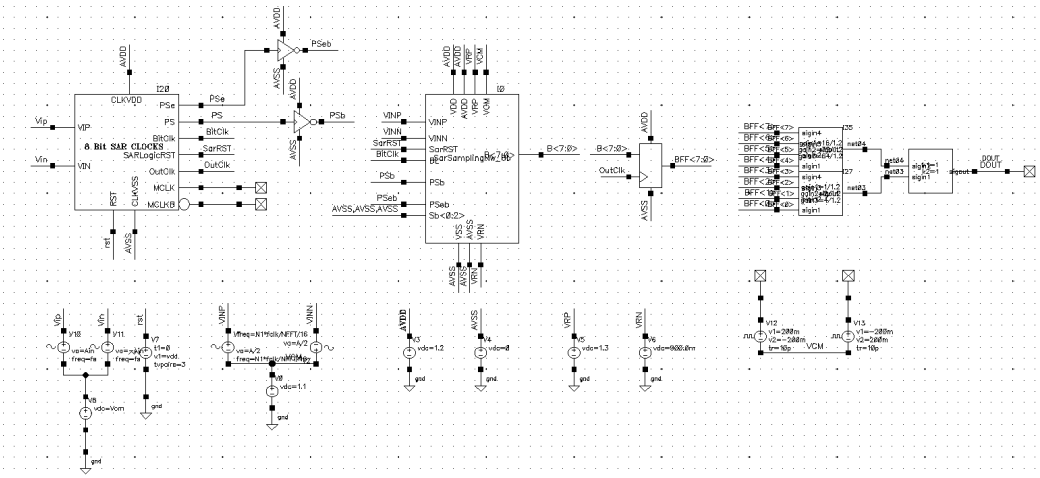

Figure B.16: Top-level Test-bench Schematic for 8-bit SAR ADC

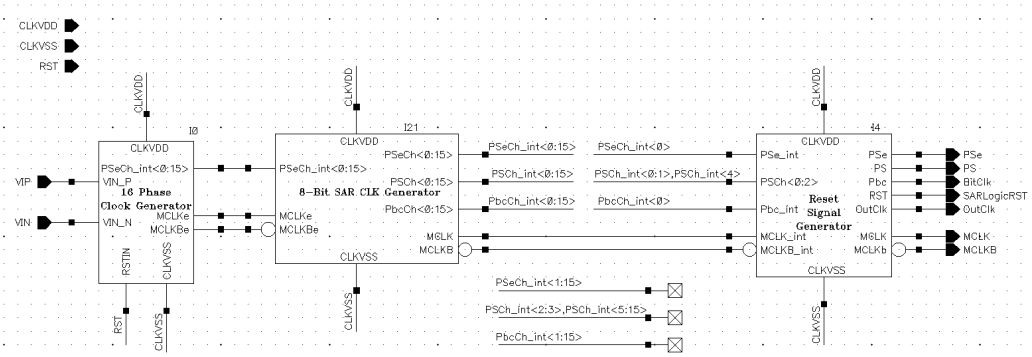

Figure B.17: Clocks for 8-bit SAR ADC

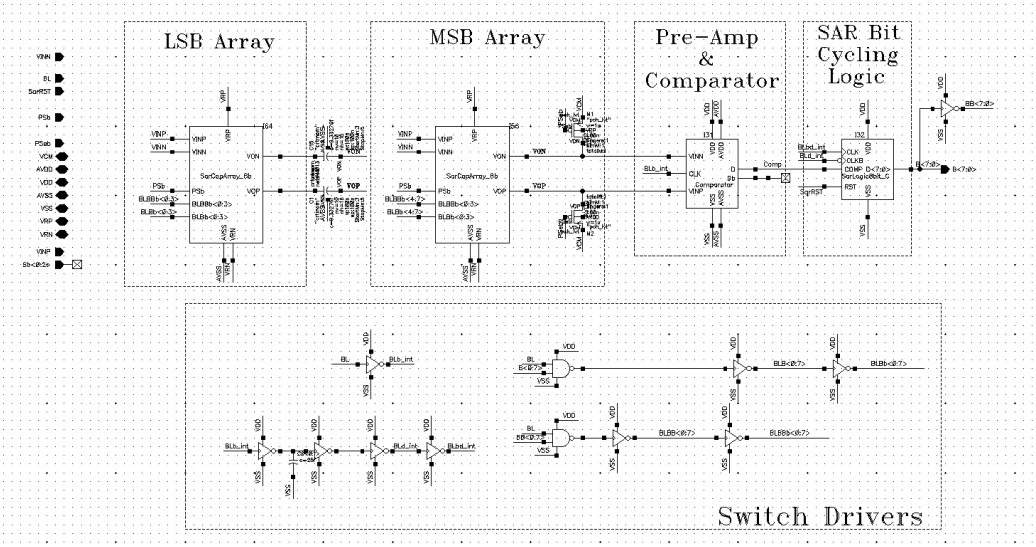

Figure B.18: 8-bit SAR sub-ADC

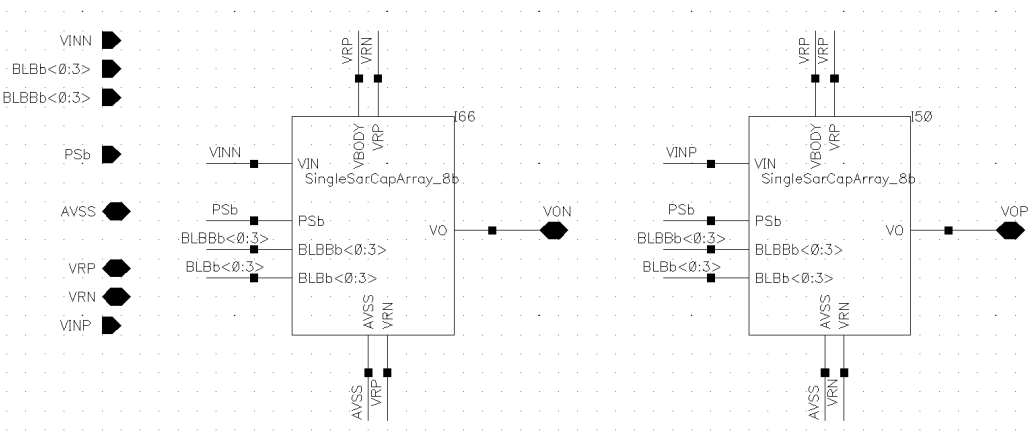

Figure B.19: 8-bit SAR Sampling Network

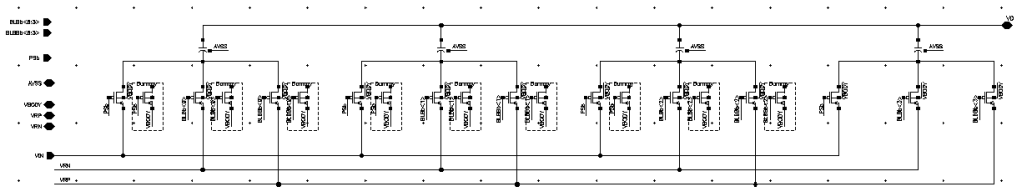

Figure B.20: Differential Half-circuit of 8-bit SAR Sampling Network

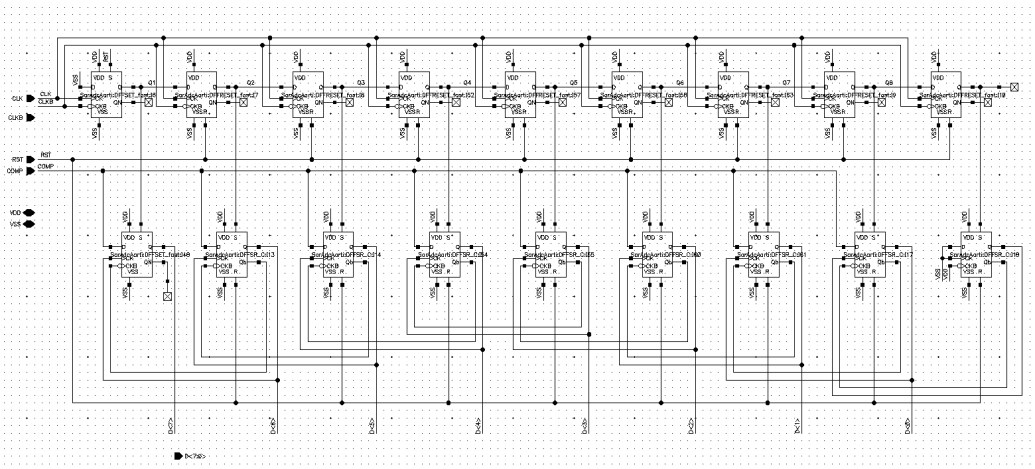

Figure B.21: 8-bit SAR Logic Block

B.4 16-channel Time-interleaved 8-Bit SAR ADC Schematics

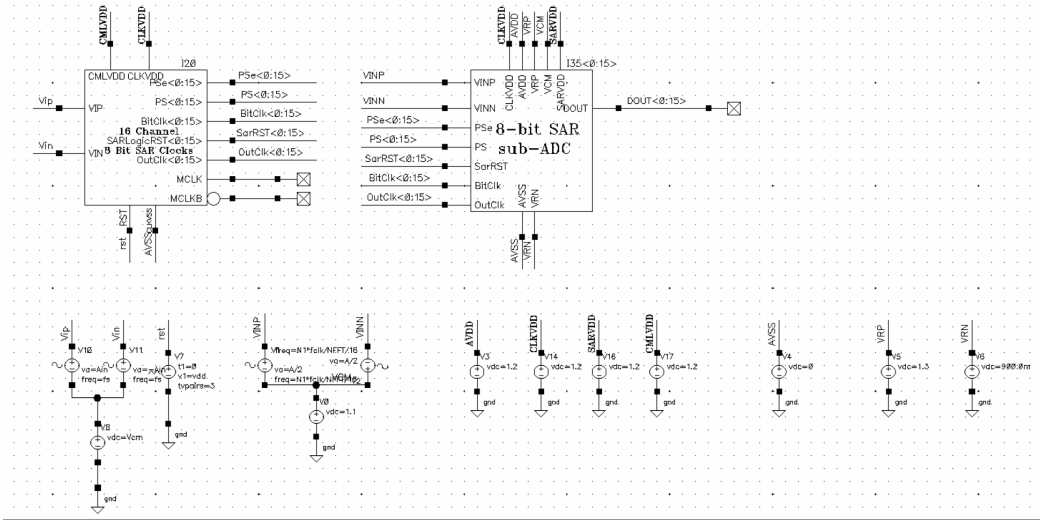

Figure B.22: Top-level Test-bench Schematic for 16-channel Time-interleaved 8-bit SAR ADC