HIGH-PERFORMANCE POWER CONVERTERS LEVERAGING CAPACITOR-BASED ENERGY TRANSFER

BY

YUTIAN LEI

DISSERTATION

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Doctoral Committee:

Assistant Professor Robert C.N. Pilawa-Podgurski, Chair
Associate Professor Kiruba Sivasubramaniam Haran
Professor Philip Krein
Associate Professor Pavan Kumar Hanumolu
Assistant Professor Minjie Chen, Princeton University

ABSTRACT

The increasing demand for high performance power conversion systems continuously pushes for improvement in efficiency and power density. This dissertation focuses on a topological effort to efficiently utilize the active and passive devices. In particular, a hybrid approach is adopted, where both capacitors and inductors are used in the voltage conversion and power transfer process.

Conventional capacitor-based converters, called switched-capacitor (SC) converters, suffer from poor efficiency due to the inevitable charge redistribution process. With a strategic placement of one or more inductors, the charge redistribution loss can be eliminated by inductively charging/discharging the capacitors, a process called soft-charging operation. As a result, the capacitor size can be greatly reduced without reducing the efficiency. A general analytical framework is presented, which determines whether an arbitrary SC topology is able to achieve full soft-charging operation with a single inductor. For topologies that cannot, a split-phase control technique is introduced, which amends existing two-phase controls to completely eliminate the charge redistribution loss. In addition, alternative placements of inductors are explored to extend the family of hybrid converters.

The hybrid converters can have two modes of operation, the fixed-ratio mode and pulse width modulated (PWM) mode. The fixed-conversion-ratio hybrid converters operate in a similar manner to that of a conventional SC converter, with the addition of a soft-charging inductor. The switching frequency of such converters can be adjusted to operate in either zero current switching (ZCS) mode or continuous conduction mode (CCM), which allows for the trade-off of switching loss and conduction loss. It is shown that the capacitor and inductor values can be selected to achieve a minimal passive component volume, which can be significantly smaller than that of a conventional SC converter or a magnetic-based converter. On the other hand, PWM-based hybrid converters generate a PWM rectangular wave as the terminal voltage to the inductor, similar to the operation of a buck converter. In contrast to conventional SC converters, such hybrid converters can achieve lossless and continuous regulation of the output voltage. Compared to buck converters, the required inductor is greatly reduced, as well as the switch stress. A 80 – 170 V input, 12 – 24 V output prototype PWM Dickson converter is implemented using GaN switches. The measured peak efficiency is 97%, and high efficiency can be maintained over the entire input and output operating range. In addition, the similarity between multilevel converters (for example, flying capacitor multilevel (FCML) converters) and the PWM-based hybrid SC converters is discussed. Both types of

converters can be seen as a hybrid converter which uses both capacitors and inductors for energy transfer. A general framework to compare these converters, along with conventional buck converters, is proposed. In this framework, the power losses (including conduction loss and switching loss) are kept constant, while the total passive component volume is used as the figure of merit.

Based on the principle of maximizing energy utilization of passive components, a 7-level FCML converter and an active energy buffer are designed and implemented for single phase dc-ac applications. In addition, the stand-alone system includes a start-up circuitry, EMC filter and auxiliary power supply. The enclosed box achieves a combined power density of 216 W/in^3 and an efficiency of 97.4%, and compares favorably against the state-of-the-art designs under the same specification.

To further improve the efficiency and power density, soft-switching techniques are investigated and applied on the hybrid converters. A zero voltage switching (ZVS) technique is introduced for both the fixed-ratio mode and the PWM mode operated hybrid converters. The previous hardware prototypes are modified for ZVS operation, and prove the feasibility of simultaneous soft-charging and soft-switching operation.

Last but not the least, some of the practical issues associated with the hybrid converter are discussed, such as practical capacitor selection, capacitor voltage balancing and other circuit implementation challenges. Future work based on these topics is given.

In summary, these hybrid converters are suited for applications where extreme efficiency and power density are critical. Through efficient utilization of active and passive devices, the hybrid topologies can offer a greater optimization opportunity and ability to take advantage of technology improvement than is possible with conventional designs.

To my parents, my grand-parents and my wife.

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CHAPTER 1

INTRODUCTION

The use of switch-mode power supplies is prevalent in applications involving the generation and consumption of electrical power. For instance, in data centers, power converters are needed to convert the 400 V dc bus voltage, down to 12 V for each server, and then to 1 V for CPUs. In electric vehicles, dc-ac converters are used to drive the electric motor. In power systems, more and more power electronics are used to interface renewable energy sources with the grid. The most desirable features of power converters are high power density, high efficiency, high reliability and low cost, but there are always trade-offs among these attributes. For example, a high-efficiency converter usually employs a lower switching frequency and thus has a larger size. A converter with a simple structure and a low component count is likely to have high reliability, but often cannot utilize the components as efficiently as a more complicated topology. Meanwhile, high-performance converters incur a higher cost due to the use of advanced components, control and manufacturing processes. Different applications rank these features with different priorities.

Due to the growing trend of electrification, more applications and functions are realized by means of electricity, and thus power electronics are playing an increasingly pivotal role, since they directly affect the overall performance of these systems. In many performance driven applications, achieving simultaneous high efficiency and high power density is most important, and oftentimes the associated complexity and cost can be accepted. The goal of this work is to explore ways to enable further improvement of the power density and efficiency of converters.

Switch-mode power converters in general have four major elements: active devices, passive components, topology, and control. Passive components are capacitors and inductors, which are used to store and transfer energy during each switching cycle. Energy density, which is energy storage capability stored by the component divided by the volume, is a major metric for passive devices. The quality factor, which determines the amount of loss generated by the passive components, is another important aspect. Active devices are semiconductor switches (such as MOSFETs) and diodes, which realize the switching functions. Lower on-state resistance of the switches (or lower forward voltage drop of the diodes) can reduce the conduction loss of the converter. Lower output charge, Q_{oss}, and gate charge, Q_{g}, can reduce the switching loss. Topology is how the active and passive components are connected. It determines the voltage and current stress of the active and passive components, and how effectively and efficiently these devices are used. Last but not the least, control is used to realize the topology as well as other goals of the converter, such as current

regulation, voltage regulation and fault protection. There are also other aspects of a practical converter, including packaging and cooling, which are also gaining in importance as the efforts in pushing the power density boundary continue [1]. In order to improve the performance of the power converters, progress is being made on all fronts. For example, the growing usage of planar magnetics enables high-frequency inductors and transformers with a low profile; the latest development in switch technologies, such as GaN FETs, promises significantly lower on-state resistance and output/gate charge.

This work focuses on the topology aspect of power converters, with an emphasis on the fundamental utilization of the active and passive devices. Traditionally, most common converter topologies are inductor based, meaning that the inductor is the main instrument for voltage conversion and energy transfer. Oftentimes, the capacitors are only used to filter the current ripple in order to obtain a steady voltage. Due to their relatively low energy density, the magnetic components are bulky in size, and are frequently the largest component in a converter. On the other hand, there are converters which use only capacitors in energy conversion, called switched-capacitor (SC) converters [2–11]. The SC converters are shown to have a lower switch stress at high conversion ratios, but they require a large volume of capacitors and cannot regulate the output voltage efficiently. As a result, they are most commonly used as low power fully integrated converters. Recently, there has been a trend to use a hybrid approach, in which both the inductor and capacitors are actively involved in power transfer. This work explores the possible ways inductor and capacitors can be efficiently utilized together in a converter. It will be demonstrated that utilizing both capacitors and inductors can yield significant power density and efficiency improvement. The thesis is outlined as follows.

Chapter 2 introduces switched-capacitor (SC) converters and reviews the fundamental limit caused by the charge-sharing process of capacitor-based energy transfer. It then introduces the soft-charging concept, which aims to eliminate the charge-sharing power loss and improve the capacitor utilization of SC converters by the addition of a small inductor at the output. A general analytical framework is presented, which can be used to determine if an arbitrary SC topology is able to take full advantage of the soft-charging operation. A split-phase control technique is introduced for the hybrid Dickson converter and enables it to achieve full soft-charging operation, which is not possible with conventional two-phase control. Chapter 2 concludes with hardware prototypes that demonstrate the superior power density and efficiency of the hybrid converters over conventional SC converters.

While Chapter 2 presents from concept to circuit implementation, how soft-charging operation can be achieved with a single inductor at the output, Chapter 3 explores alternative inductor placements. In addition, it provides a method to optimally choose the capacitor and inductor values so that the total passive component volume can be minimized. It then compares various soft-charging topologies based on their switch stress and component volume, as a guide for topology selection.

Chapter 4 focuses on the other drawback of SC converters, which is the inability to regulate

the output voltage efficiently. A regulation technique is presented that achieves lossless output voltage regulation for the hybrid SC converters, by using PWM operation similar to that of a buck converter, but without requiring additional switches from existing SC topology. Combining the split-phase control from Chapter 2 and the regulation technique, a hybrid Dickson converter prototype with a wide range of input and output voltage is implemented, and can maintain a high efficiency across the operating range.

While Chapters 2 and 3 show that the fixed-conversion-ratio hybrid SC converters have a better performance over conventional SC and buck converters, Chapter 5 attempts to analytically show that the regulating, PWM-based hybrid converter proposed in Chapter 4 also has a superior performance compared to buck converters, especially in large conversion ratio applications. A general framework is developed that can be used to compare different hybrid and non-hybrid topologies. In this framework, the power losses of the converters are designed to be the same, and the total passive component volume is used to reflect the performance of a converter. Flying capacitor multilevel (FCML) converters and the hybrid Dickson converters are used as examples of converters that utilize both capacitor and inductor for energy transfer. It is shown that both of these converters can achieve much higher power density at the same power loss level, compared to conventional buck converters. Converter prototypes are also implemented to support the theoretical analysis.

Based on the concept of high energy utilization, Chapter 6 presents the design and implementation of a flying capacitor multilevel converter and an active energy buffer for single phase dc-ac or ac-dc applications. The multilevel topology reduces the voltage ripple seen by the inductor and increases the equivalent ripple frequency, both of which reduce the required inductor size. On the other hand, the flying capacitors are designed with a large voltage ripple at the switching frequency, resulting in a high energy utilization. Therefore, both the capacitors and inductor are small and a high power density design is possible. For the active energy buffer, a new series-stacked topology is proposed, which is able to achieve high energy utilization of the capacitor and high efficiency simultaneously. The combined inverter and buffer, together with the heat-sink, achieve a power density of 216 W/in^3 and an efficiency of 98.4%.

A common technique to reduce converter size and improve efficiency at high frequency operation is to use soft-switching techniques. In Chapter 7, some zero voltage switching (ZVS) techniques are explored for hybrid converters, enabling potentials for an even higher power density by minimizing the switching loss and drain-source voltage ringing. Hardware prototypes from the previous sections are modified to support ZVS operation, and measured results show a significant efficiency increase for the fixed-ratio hybrid converter, and improved light-load efficiency for the PWM hybrid converter.

Chapter 8 discusses some of the practical issues associated with the hybrid converter, such as practical capacitor selection, capacitor voltage balancing and other circuit implementation challenges. It also suggests some future work based on these topics. Finally, conclusions are given in Chapter 9.

CHAPTER 2

SOFT-CHARGING OPERATION - IMPROVING THE CAPACITOR UTILIZATION OF SC CONVERTERS

In this chapter, the hybrid converters are obtained by adding one or more inductors to existing conventional SC topologies. It will be shown that with the additional inductors, the charge-sharing loss of SC converters can be eliminated – an operation called *soft-charging*. As a result, the capacitor values can be reduced, thereby significantly improving the power density of SC converters. In addition, it is shown that resonant and soft-charging SC converters are closely related and it is possible to use similar techniques to analyze and synthesize both types of converters. Then a formal method is presented to analyze arbitrary SC topologies to determine their suitability for full soft-charging operation with a single additional inductor. It is found that the series-parallel and Fibonacci topologies are able to achieve full soft-charging operation, while the Dickson topology can achieve partial soft-charging operation. A split-phase control method is then introduced to completely eliminate charge-sharing loss for the Dickson converter. Moreover, simulation and hardware results are provided to validate the proposed technique and analysis, and to demonstrate the improved power density and efficiency of the hybrid converters.

2.1 Background on Switched-Capacitor Converters

In this section, the background on SC converters is presented, and the charge-sharing loss mechanism explained. Figure 2.1 shows the energy density (energy storage capability per unit volume) of some surface mount capacitors and inductors.[1] It can be seen that on average, the energy density of capacitors is higher than that of inductors by a factor of 10 – 100. A similar trend can be observed for chip-integrated capacitors and inductors. Therefore, for the same amount of stored energy, capacitors can be less than one tenth the size of inductors. This is the fundamental motivation why energy transfer by capacitors should be considered. In addition, SC converters also tend to achieve a higher efficiency at large voltage conversion ratios, due to their efficient utilization of switches [12]. These advantages make SC converters desirable for a broad range of applications, including voltage balancing [3, 4], energy buffering [5], CMOS integrated power conversion [6, 8, 13] and renewable energy harvesting [9].

[1] Energy of inductor is calculated as $\frac{1}{2}LI_{\text{sat}}^2$, where I_{sat} is the saturation current of the inductor. The energy of capacitor is calculated by $\frac{1}{2}CV^2$. The energy density of the X7R ceramic capacitors has accounted for the derating of capacitance value with DC bias.

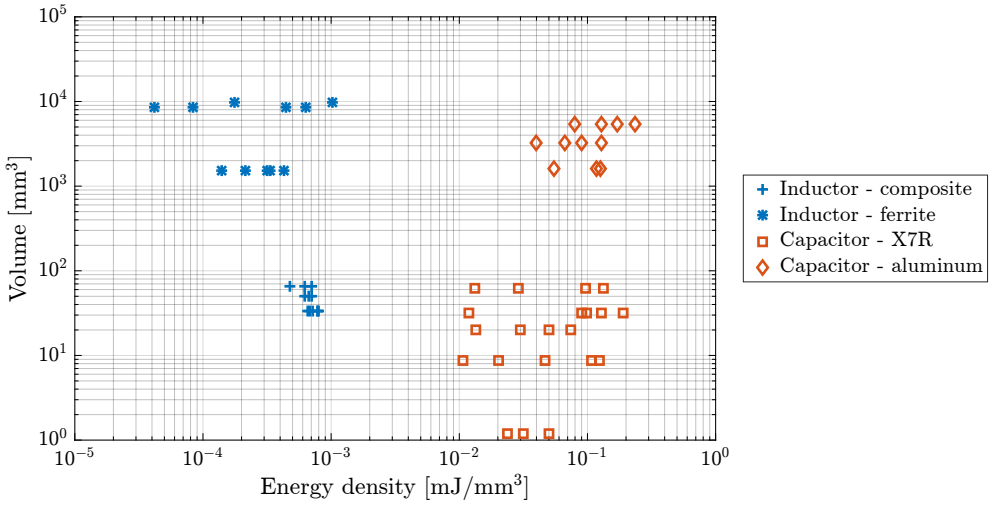
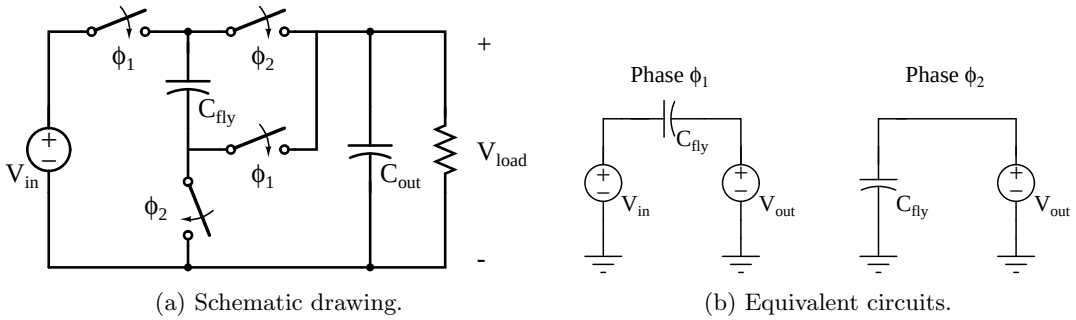


Figure 2.1: Energy density of selected inductors and capacitors.



(a) Schematic drawing. (b) Equivalent circuits.

Figure 2.2: A simple 2-to-1 SC converter.

A simple conventional 2-to-1 SC converter is shown in Fig. 2.2a. There are two pairs of switches, operating with a non-overlapping 50% duty ratio. In Phase ϕ_1, the flying capacitor, C_{fly}, is in series with the output, while in Phase ϕ_2, C_{fly} is in parallel with the output, as shown in the equivalent circuits in Fig. 2.2b. The no-load steady state solution of the circuit is $V_{C_{\text{fly}}} = V_{\text{out}} = \frac{1}{2}V_{\text{in}}$.

A generic SC converter model as shown in Fig. 2.3 is commonly used to capture the steady-state characteristics of an SC converter. The model consists of an ideal fixed-conversion-ratio stage with an output-referred impedance [14]. The output impedance directly reflects the efficiency of the converter, and incorporates both the conduction loss and the capacitor charge-sharing loss. This impedance is usually plotted against the switching frequency or capacitance value to reveal the characteristics of the SC converters. A typical such plot is shown in Fig. 2.4, which shows two asymptotic operating regions for SC converters: the fast switching limit (FSL) and the slow switching limit (SSL) [12] [15–18]. The FSL occurs at high switching frequencies, when the dominating loss is the conduction loss due to the resistance of the switches as well as the ESR of the capacitors. As can be seen in Fig. 2.4, the output impedance in the FSL region is independent of the switching frequency. On the other hand, the SSL occurs at low switching frequencies, when the

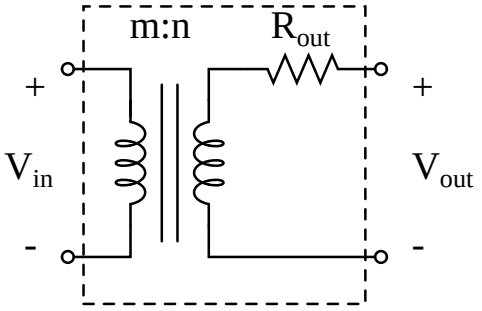


Figure 2.3: Generic steady-state model of a switched-capacitor converter.

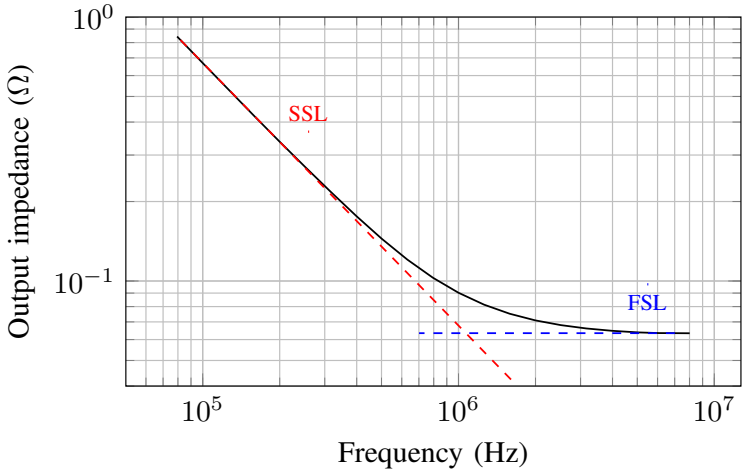


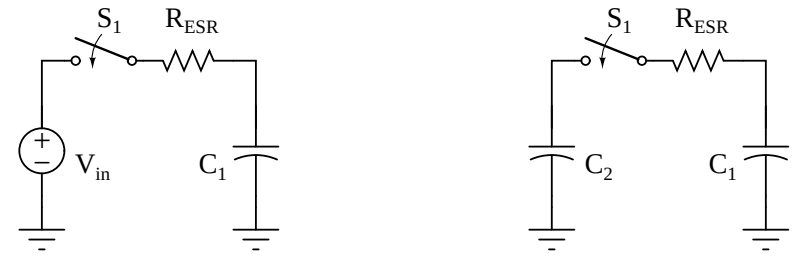
Figure 2.4: Output impedance of a typical SC converter.

output impedance is dominated by the charge-sharing loss of the capacitors during the charge redistribution process at phase transitions. The SSL impedance depends on the switching frequency and capacitor values, and cannot be reduced by lowering the series resistance. In-between the FSL and SSL, the output impedance can be approximated [19] or obtained analytically [20] and numerically [18].

Based on the model in Fig. 2.3, the efficiency of an SC converter is given by

$$\eta = \frac{\frac{n}{m}V_{\text{in}} - R_{\text{out}}I_{\text{out}}}{\frac{n}{m}V_{\text{in}}}. \tag{2.1}$$

Evidently, to maximize the efficiency, the output impedance, R_{out} should be minimized. One straightforward way to reduce R_{out} is to simply increase the switching frequency so that the converter operates in the FSL region. However, it is often not favorable to do so, since the transistor switching losses, as well as the bottom plate capacitance losses in integrated SC converters, increase as the switching frequency increases. Alternatively, increasing the flying capacitor values can push the FSL region of operation to a lower frequency, but it inevitably increases the circuit size and cost, undermining the energy density advantage of capacitors.



(a) Capacitor charged by a voltage source.

(b) Capacitor charged by another capacitor.

Figure 2.5: Basic capacitor charging scenarios.

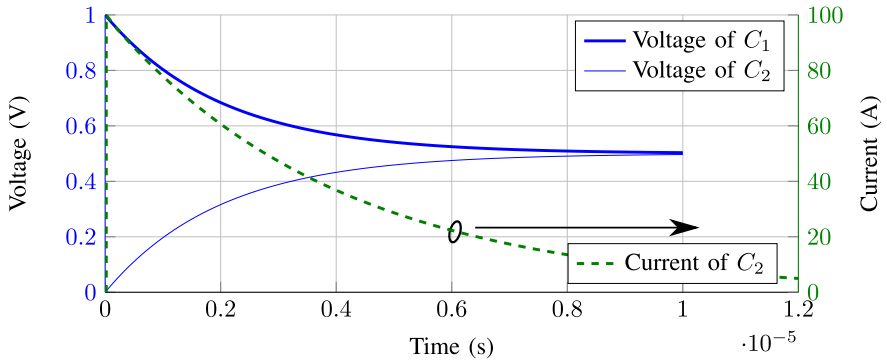


Figure 2.6: Capacitor voltages and current waveform in charge redistribution process.

Fundamentally, the SSL power loss is the result of charging/discharging the capacitor with a constant voltage source or another capacitor, as illustrated in Fig. 2.5a and Fig. 2.5b respectively. All switching states of an SC converter can be reduced to these two basic scenarios. Without loss of generality, we will examine case 2 (Fig. 2.5b) more closely since case 1 (Fig. 2.5a) can be seen identical to case 2 with C_2 being infinite. When the switch, S_1, closes, since the capacitor voltage cannot change instantaneously, the mismatch of the initial capacitor voltages will be present across the series resistor, resulting in a large instantaneous current as shown in Fig. 2.6. The power loss incurred for complete charge redistribution for the schematic showing in Fig. 2.5b can be easily calculated and is given by

$$\begin{aligned} P_{\text{loss}} &= \frac{1}{4} C_1 (V_{C1(t=0)} - V_{C2(t=0)})^2 f_{\text{sw}} \\ &= \frac{1}{4} C_1 \Delta V_{(t=0)}^2 f_{\text{sw}} \,, \end{aligned} \tag{2.2}$$

assuming $C_1 = C_2$. This equation is valid provided that the duration of each phase is much larger than the time-constant of the circuit, i.e. in SSL region of operation. As seen in Eq. (2.2), this power loss does not depend on the value of the series resistance. Instead, it depends on the initial voltage difference between the capacitors. Additionally, in periodic steady state operation, the initial difference in capacitor voltages in one cycle of operation is due to the charge transfer in the

previous cycle, and thus is proportional to the current drawn by the load and inversely proportional to the capacitor values and the switching frequency. These relations are summarized below.

$$\Delta V \propto \frac{1}{f_{\text{sw}}}, \frac{1}{C_{\text{fly}}}, I_{\text{out}}, \tag{2.3}$$

where C_{fly} represents the overall flying capacitor value, and for the circuit in Fig. 2.5b, it is simply C_1. Substituting (2.3) into the power loss equation in (2.2), we have

$$P_{\text{loss}} \propto \frac{1}{f_{\text{sw}}}, \frac{1}{C_{\text{fly}}}, I_{\text{out}}^2. \tag{2.4}$$

Combining Eq. (2.4) and Fig. 2.3, one can see that the power loss due to the charge sharing process manifests as an output impedance which is inversely proportional to the capacitance value and the switching frequency, giving the SSL region of operation in Fig. 2.4. For more complex SC converters, more complicated charge sharing scenarios (involving multiple capacitors in series or parallel) will arise, but the general relationship stays the same, as shown by the analytical results given in [12].

Another way to look at the limitation imposed by the charge-sharing loss is to examine the energy utilization of the capacitors, μ_C, which is defined as the energy transfered by the capacitor in a cycle, divided by the peak energy stored by the capacitor [5]. For a fixed amount of energy delivered to the load, high energy utilization means a lower stored energy and smaller capacitor size, and vice versa. For a single capacitor, it is given by

$$\mu_C = \frac{\frac{1}{2}C(V + \frac{1}{2}\Delta V_C)^2 - \frac{1}{2}C(V - \frac{1}{2}\Delta V_C)^2}{\frac{1}{2}C(V_C + \Delta V_C)^2}, \tag{2.5}$$

where ΔV_C is the change in capacitor voltage, and V_C is the nominal capacitor voltage. It can be simplified to

$$\mu_C = \frac{2\frac{\Delta V}{V}}{(1 + \frac{1}{2}\frac{\Delta V}{V})^2}\,. \tag{2.6}$$

It can be seen that the utilization of the capacitor can be improved by allowing a larger ΔV. However, from Eq. (2.2), the power loss of the converter increases quadratically as ΔV increases, resulting in a fundamental conflict. As an example, the efficiency and capacitor utilization of the 2-to-1 converter in Fig. 2.2a are plotted in Fig. 2.7. For small capacitor voltage ripple, efficiency decreases linearly and utilization increase lineary, approximately. In order to achieve a 95% efficiency, the capacitor utilization is less than 10%, meaning that the capacitor needs to store 10 times more energy than it delivers to the load.

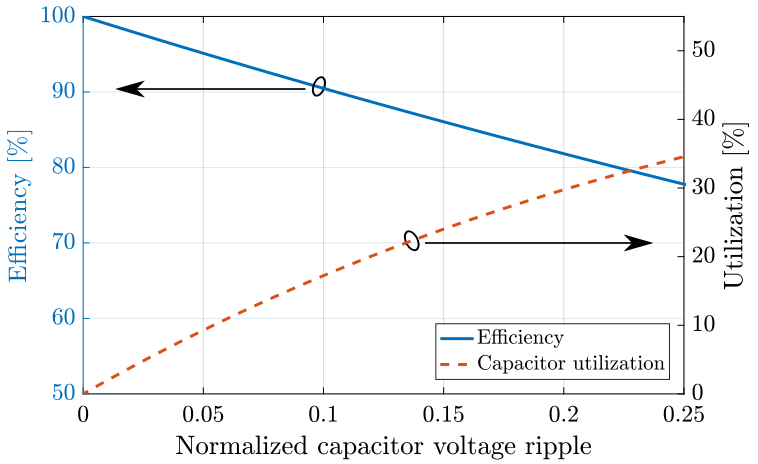


Figure 2.7: Capacitor voltages and current waveform in charge redistribution process.

2.2 Soft-charging Operation with an Inductor

In order to eliminate the capacitor charge sharing loss and improve the utilization of capacitors, the soft-charging technique was proposed [21]. In soft-charging operation, a controlled current load is placed in the charging/discharging paths of the capacitors. The majority of the voltage mismatch between the capacitors and the input/output will be present across the current load, instead of across the switch resistance. With this technique, the capacitor charging loss that is present in conventional SC converters is recovered through the controlled current load. As a result, smaller capacitance can be used without sacrificing the efficiency, despite the resultant larger capacitor voltage ripples. This is the key benefit of soft-charging operation. In practice however, the majority of the loads are voltage-source loads or current-source loads with large decoupling capacitors. Therefore, an interfacing element typically has to be inserted between the SC converters and the voltage-source load. Buck converters can be such an interfacing element, providing controlled charging/discharging of the capacitors while regulating the output voltage [21, 22]. Since an inductor allows instantaneous change of its terminal voltage, it can also act as a controlled current load [19, 23]. In fact, the buck converter is able to facilitate soft-charging operation precisely because of the inductor it contains.

This section investigates soft-charging operation of SC converters by adding an inductor to form an LC filter at the output node of the voltage step-down topologies. The inductor permits its terminal voltage to change instantaneously to accommodate the voltage mismatch between the flying capacitors and the load during phase transitions. Furthermore, it will be shown that resonant operation can also be achieved using the same technique.

To illustrate the technique, the hybrid 2-to-1 SC converter with an output LC filter is shown in Fig. 2.8. Figure 2.9 plots the simulated output impedance as a function of frequency for both the original SC converter (Fig. 2.2a), as well as the hybrid converter (Fig. 2.8). It can be seen that for the original SC converter, the output impedance reduces as the frequency increases, while leveling

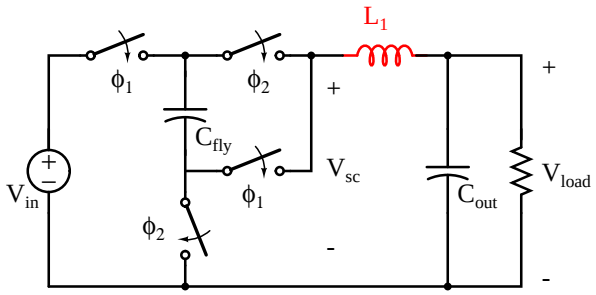


Figure 2.8: A 2-to-1 SC converter with an inductor.

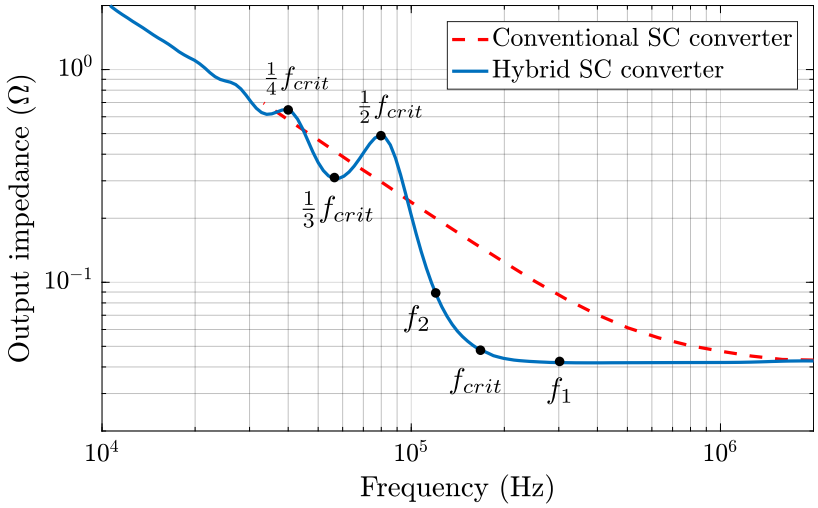


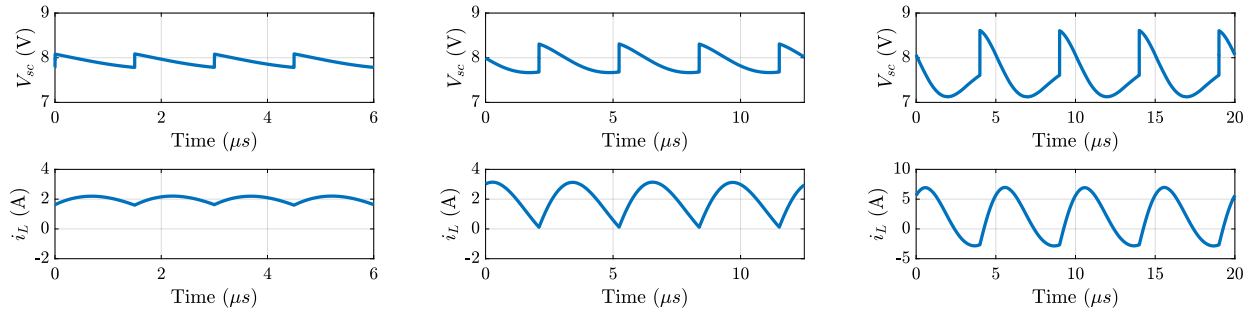
Figure 2.9: Simulated output impedance vs frequency.

off at high frequencies, marking the transition from SSL to FSL. The output impedance curve is more complicated for the hybrid converter, but a few key observations can be made. First, with the additional inductor, the hybrid converter is able to reach the same minimum impedance at a much lower switching frequency, due to the elimination of the current transient and associated loss. Therefore, the proposed converter can achieve the same efficiency as conventional SC converters while using a significantly lower switching frequency, or equivalently, significantly smaller flying capacitor values. The second observation is that, at lower frequencies, the output impedance oscillates around the SSL impedance of the conventional SC converter.

The minimum frequency at which the converter is able to stay in FSL operation can be defined as f_{crit} and for the hybrid converter in Fig. 2.8, it is given by the resonant frequency of the circuit:

$$f_{\text{crit}} = \frac{1}{2\pi\sqrt{LC}}, \tag{2.7}$$

where L is the added inductance and C is the collective capacitance in series with the inductor. In the case of the example SC converter in Fig. 2.8, the capacitance is simply C_{fly}. For more complex SC converter topologies, this equivalent capacitance can be obtained by calculating the

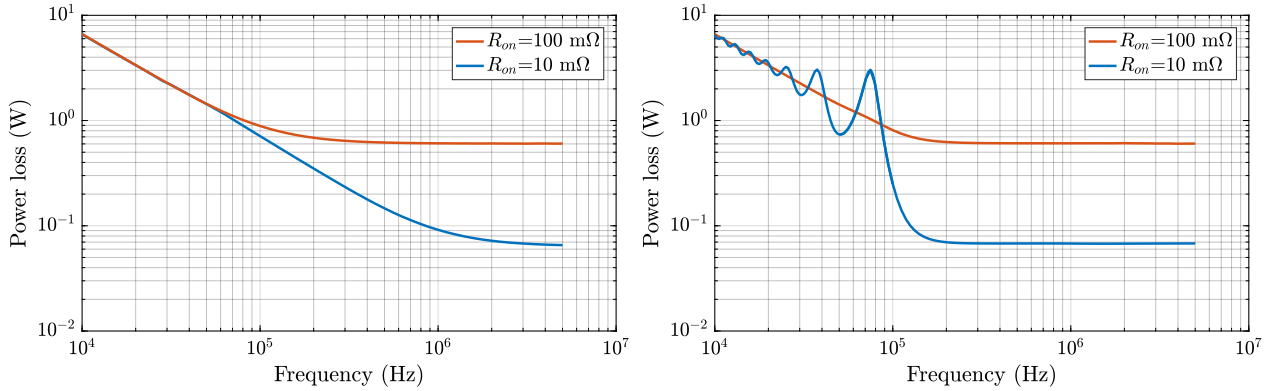


(a) $f_{sw} = f_1 > f_{crit}$. (b) $f_{sw} = f_{crit}$. (c) $f_{sw} = f_2 < f_{crit}$.

Figure 2.10: SC stage voltage (V_{sc} in Fig. 2.8) and inductor current of the modified 2-to-1 converter.

equivalent series and parallel connected capacitance at the inductor input node for each phase. For instance, for the 4-to-1 Dickson converter shown later in Fig. 2.13, the effective capacitance in Phase 1 is $(C_1 \parallel C_2 + C_3)$ and the capacitance in Phase 2 is $(C_2 \parallel C_3 + C_1)$. Both phases have the same equivalent capacitance of $1.5C_1$ assuming $C_1 = C_2 = C_3$. For converter topologies that have different equivalent capacitance in each phase (such as the Fibonacci and series-parallel), there is a critical frequency for each phase, and the overall critical frequency is the weighted average of the individual frequencies according to the duty ratio.

To understand the frequency dependent behavior of the modified SC converter, the terminal voltage before the inductor (V_{sc} in Fig. 2.8) as well as the inductor current are shown in Fig. 2.10 at 3 different frequencies - the resonant frequency (f_{crit}) as well as below and above the resonant frequency (f_2 and f_1, respectively). It can be seen that, above the resonant frequency, the current waveform (Fig. 2.10a) is smooth and has a small ripple, due to the filtering effect of the inductor. Moreover, since the flying capacitor is always in the same current path as the inductor, the conventional current spikes of the capacitor are eliminated, and the capacitors transfer charges in soft-charging mode, with no charge-sharing loss. The effect of this can be seen directly from Fig. 2.9, where for switching frequencies larger than the critical frequency, the SC converter has the minimum FSL output impedance. As the switching frequency is reduced, the current waveform has larger ripple, while having the same average value, since the load current is kept constant. At the resonant frequency, f_{crit}, the inductor current takes the shape of a rectified sinusoid, and the current reaches zero at moments of phase transitions, as shown in Fig. 2.10b. Thus, zero current switching (ZCS) can be achieved at the resonant frequency. As can be seen in Fig. 2.9, the impedance of the converter at resonance is slightly larger than the FSL impedance. This is because the sinusoidal current has larger RMS value than the near constant current in FSL operation. As the switching frequency is reduced further (Fig. 2.10c), the inductor current drops negative during each cycle, resulting in a much larger RMS current for the same average power delivered. This is why the impedance increases sharply for $f_{sw} < f_{crit}$. At one half of the resonant frequency defined by (2.7),



(a) Conventional SC converter.

(b) Soft-charging SC converter.

Figure 2.11: Power loss at different frequencies for different $R_{ds,on}$ values, for the circuit in Figs. 2.2a and 2.8. Simulation parameters: $C = 10\ \mu F$, $L = 0.1\ \mu H$.

the current becomes nearly a full-wave sinusoid, giving a peak impedance in Fig. 2.9. This peak repeats itself at lower frequencies when the current waveform has multiple periods of the full-wave sinusoid, at $f_{sw} = \frac{1}{n} f_{\text{crit}}$, where n is an integer and $n \geq 2$. Therefore, f_{crit} given in (2.7) sets the lower bound on the switching frequency for which near FSL impedance in soft-charging operation can be achieved.

Therefore, the reduction in frequency and capacitance with soft-charging operation can be achieved but at the expense of adding an inductor. While the trade-off between the capacitor values and inductor values should be evaluated on a case-by-case basis, in general, adding an inductor results in better utilization of passive components than simply using larger capacitance. For a traditional SC converter circuit, whether the high current transient takes place is determined by the time constant of the circuit, $R_{\texttt{ESR}}C$, where $R_{\texttt{ESR}}$ is the series resistance in each conducting branch and C is the capacitance in each branch. Thus the critical frequency at which the conventional SC converter enters FSL operation is

$$f_{crit} = \frac{1}{2\pi R_{\texttt{ESR}} C}\,. \tag{2.8}$$

It can be seen that the switching frequency is inversely proportional to the product of the equivalent series resistance and capacitance. Thus, for a given desired critical frequency, the capacitance must be increased if the resistance is lowered. This limitation can be clearly seen in Fig. 2.11a, where the power loss of a pure SC converter is plotted against two different switch $R_{ds,on}$ values. Even when the $R_{ds,on}$ of the switch is reduced by a factor of 10, to see a factor of 10 reduction in the power loss, one needs to increase the switching frequency by a factor of 10, or equivalently, increase the capacitor values by a factor of 10. This is due to the inversely proportional relationship among the resistance, capacitance and switching frequency. On the other hand, with the additional inductor presented here, the critical frequency is decoupled from the series resistance, and only depends

on the inductance and the capacitance, as shown in (2.7). The effect can be seen in Fig. 2.11b, where a reduction in the series resistance instantly brings a nearly equal reduction in power loss, without the need to increase the capacitance nor the frequency. Therefore, the addition of the inductor gives the designer the choice of using smaller on-state-resistance switches and introduces a new design dimension in which the converter can be optimized. Also observed in Fig. 2.11b is that oscillation does not occur for the case of $R_{on} = 100$ mΩ. This is because the system is over-damped ($\frac{R}{2}\sqrt{\frac{C}{L}} < 1$) for large resistance values. In this case, the RC time constant starts to dominate the frequency response of the system again, and soft-charging operation does not take place. As a result, there is no change in power loss by adding the small inductor, as can be seen by comparing the red dotted lines in Fig. 2.11a and Fig. 2.11b. In this case, a larger inductance would have been needed to achieve a reduction in power loss in the SSL region. Therefore, in addition to the critical switching frequency requirement given in (2.7), the soft-charging (as well as resonant) SC converters need to be designed such that the system is under-damped ($\frac{R}{2}\sqrt{\frac{C}{L}} < 1$). Nevertheless, a lower series resistance is one of the goals for power converters aiming for high conversion efficiency, especially for applications with small load resistances. This naturally coincides with the design goal of the soft-charging SC converters. In discrete implementations, the addition of the inductors often results in overall improvement in energy utilization of the passive components. While the inductor is more difficult to integrate than the capacitors given the current IC technology, the energy density and quality of integrated inductors are improving as more advanced processes are adopted [24–26], and the proposed converter is able to take advantage of the progress and advancement of technologies in inductors, capacitors and switches simultaneously.

2.3 Analyzing an Arbitrary SC Topology for Soft-Charging Operation

It has been shown in the previous section that resonant and non-resonant soft-charging operation are closely related and both modes of operation can be achieved with a single additional inductor. Since resonance with the inductor at the output can be viewed as a particular case of soft-charging operation at a special switching frequency, only the term, soft-charging, is used in this section for convenience. The example used was a 2-to-1 SC converter, which easily satisfies the second condition given in Section 2.2, which states that to achieve full soft-charging operation, there can be no voltage mismatch among the flying capacitors during phase transitions. The example 2-to-1 SC converter satisfies this condition easily since it only has a single flying capacitance. More complicated SC converters have multiple flying capacitors connected in a number of different configurations. Therefore, it is of great interest to determine whether this proposed technique can be broadly applied to other SC converter topologies. To answer this question, a general method is derived in this section to determine if an arbitrary SC converter topology can operate in resonance or soft-charging operation with the addition of an output inductor [27, 28].

In essence, the proposed method examines the charge flow characteristics of an SC converter

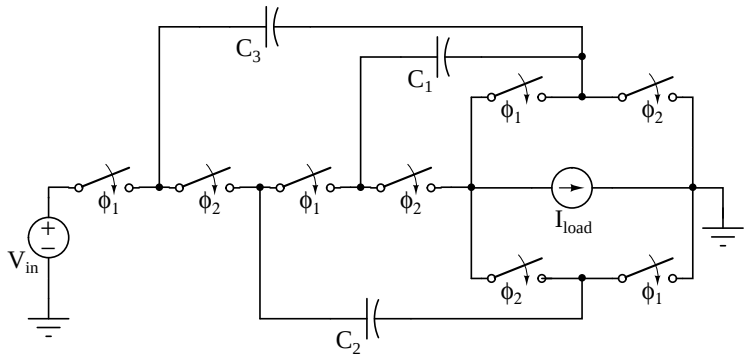
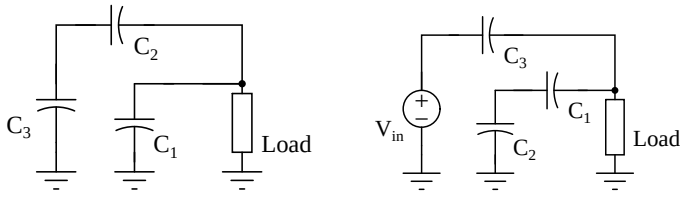


Figure 2.12: 4-to-1 Dickson topology.



(a) Phase 1. (b) Phase 2.

Figure 2.13: 4-to-1 Dickson topology in each phase.

topology and observes the change in capacitor voltage subject to Kirchhoff's voltage law (KVL) constraints. In each phase of the SC converter, the voltage across a capacitor changes according to the charge flow in the given phase. When the converter switches to the next phase, KVL poses new constraints on each component. Complete soft-charging is achieved if and only if the ideal capacitor network satisfies KVL at all times, including at phase transitions. If during any period, the KVL constraint is not satisfied, the voltage discrepancy will appear across the series resistances, resulting in a charge transfer impulse. The KVL constraint is present whether soft-charging or resonant operation is of interest, and thus the analysis presented in this section applies to both operations.

2.3.1 General analysis using Dickson converter as an example

The analysis method in this work is illustrated with a 4-to-1 SC converter in Dickson configuration [6, 29, 30] shown in Fig. 2.12. To simplify the analysis, a constant current source is used as the load for this and all following examples, while we note that a practical implementation would use a magnetic-based converter or an inductor. The two phases of the Dickson topology are shown in Fig. 2.13a and Fig. 2.13b respectively. In each phase of Fig. 2.13, the circuit consists of a number of closed loops, and a KVL equation can be written for each loop. For a circuit with n nodes and b components, a total of $b - (n - 1)$ independent KVL loop equations exist. For example, the following two independent KVL equations can be written for Phase 1 of the Dickson converter

(Fig. 2.13a):

$$\begin{cases} V_{in} - V_{C3} - V_{out} = 0 \\ V_{C2} - V_{C1} - V_{out} = 0\,, \end{cases} \tag{2.9}$$

and for Phase 2 (Fig. 2.13b):

$$\begin{cases} V_{C3} - V_{C2} - V_{out} = 0 \\ V_{C1} - V_{out} = 0\,. \end{cases} \tag{2.10}$$

These KVL equations can be written in a matrix-vector-product form as

$$\mathbf{A_i v^i} = \mathbf{0}, \tag{2.11}$$

where $\mathbf{A_i}$ is called the reduced loop matrix of the ith phase [31] and the voltage vector $\mathbf{v}$ is defined as

$$\mathbf{v} = [v_{in}\, v_{c1}\, v_{c2}\, v_{c3}\, v_{out}]^T \tag{2.12}$$

$$= [v_{in}\, \mathbf{v_c}^T\, v_{out}]^T\,. \tag{2.13}$$

In this analysis, the entries of the loop matrices are positive if the circuit element is traversed from the negative terminal to the positive terminal and vice versa. Combining the definitions in Eqs. (2.11) and (2.12) and the KVL equations in Eqs. (2.9) and (2.10), the loop matrices are found to be

$$\mathbf{A_1} = \begin{bmatrix} 1 & 0 & 0 & -1 & -1 \\ 0 & -1 & 1 & 0 & -1 \end{bmatrix} \text{ and } \mathbf{A_2} = \begin{bmatrix} 0 & 0 & -1 & 1 & -1 \\ 0 & 1 & 0 & 0 & -1 \end{bmatrix}.$$

Denoting the voltage vector at the start of phase 1 as $\mathbf{v^1}$, KVL analysis yields

$$\mathbf{A_1 v^1} = \mathbf{0}, \tag{2.14}$$

which captures the KVL constraints given by Eq. (2.9) at the moment when the converter has begun Phase 1 operation. At the end of Phase 1, the voltage vector becomes $\mathbf{v^1} + \mathbf{\Delta v^1}$, creating a second KVL constraint:

$$\mathbf{A_1}(\mathbf{v^1} + \mathbf{\Delta v^1}) = \mathbf{0}, \tag{2.15}$$

where $\mathbf{\Delta v}$ represents the change in voltage due to charge being delivered to the load, and is in the form of $[\Delta v_{in}\, \mathbf{\Delta v_c}^T\, \Delta v_{out}]^T$, similar to the voltage vector in Eq. (2.12) . Since *both* Eq. (2.33) and Eq. (2.34) must be satisfied, a resulting constraint is that the vector $\mathbf{\Delta v}$ must satisfy

$$\mathbf{A_1 \Delta v^1} = \mathbf{0}. \tag{2.16}$$

From a circuit intuition point of view, Eq. (2.16) describes the fact while the individual node voltages can (and will) change as a result of charge transfers, the sum of the changes in a KVL

loop must be zero. Similarly for Phase 2, we have

$$\mathbf{A_2 \Delta v^2} = \mathbf{0}. \tag{2.17}$$

Note that the Δv_{in} component of $\mathbf{\Delta v^i}$ is typically zero since the input voltage is considered constant. This information can be included in the loop matrices by adding a row of [1 0 0 0 0] to both $\mathbf{A_1}$ and $\mathbf{A_2}$, resulting in $\mathbf{A_{1m}}$ and $\mathbf{A_{2m}}$ respectively, where the subscript m indicates a modified reduced loop matrix. Correspondingly, Eq. (2.16) and Eq. (2.17) become

$$\mathbf{A_{1m} \Delta v^1} = \mathbf{0} \tag{2.18}$$

$$\mathbf{A_{2m} \Delta v^2} = \mathbf{0}\,. \tag{2.19}$$

The solution to Eq. (2.18) and Eq. (2.19) represents the set of permissible voltage changes that satisfy KVL and $\Delta v_{in} = 0$. This solution is the nullspace of $\mathbf{A_{1m}}$ and $\mathbf{A_{2m}}$, by definition. Let $\mathbf{w}$ and $\mathbf{u}$ be the collective bases for nullspaces of $\mathbf{A_{1m}}$ and $\mathbf{A_{2m}}$ respectively. It follows that any solution to Eq. (2.18) and Eq. (2.19) can be represented by a linear combination of the basis vectors:

$$\mathbf{\Delta v^1} = a_1 \mathbf{w_1} + a_2 \mathbf{w_2} \tag{2.20}$$

$$\mathbf{\Delta v^2} = b_1 \mathbf{u_1} + b_2 \mathbf{u_2}\,. \tag{2.21}$$

In the case of the 4-to-1 Dickson converter, such bases can be found[2] as

$$\mathbf{w} = \left\{ \begin{bmatrix} 0 \\ 0.607 \\ 0.763 \\ -0.157 \\ 0.157 \end{bmatrix} \begin{bmatrix} 0 \\ -0.482 \\ 0.131 \\ -0.613 \\ 0.613 \end{bmatrix} \right\} \text{ and } \mathbf{u} = \left\{ \begin{bmatrix} 0 \\ 0.362 \\ 0.398 \\ 0.761 \\ 0.362 \end{bmatrix} \begin{bmatrix} 0 \\ 0.518 \\ -0.664 \\ -0.146 \\ 0.518 \end{bmatrix} \right\}.$$

For conventional SC converters, we have the additional constraint that

$$\mathbf{\Delta v^1} = -\mathbf{\Delta v^2}\,, \tag{2.22}$$

from the condition of periodic steady-state operation. This is because in a capacitive network, the voltage changes must sum up to zero in a full switching cycle. Combining Eq. (2.20) Eq. (2.21) and Eq. (2.22), we have

$$a_1 \mathbf{w_1} + a_2 \mathbf{w_2} + b_2 \mathbf{u_1} + b_2 \mathbf{u_2} = 0\,. \tag{2.23}$$

[2]For example, by using the command "null" in Matlab, which will yield a set of orthonormal basis vectors.

Note that Eq. (2.23) can be written in a matrix form as

$$\begin{bmatrix} \mathbf{w_1} & \mathbf{w_2} & \mathbf{u_1} & \mathbf{u_2} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ b_1 \\ b_2 \end{bmatrix} = \mathbf{0}\,. \tag{2.24}$$

For the conventional Dickson SC converter, no solution for Eq. (2.24) can be found, except for the trivial case of zero. This means that no voltage change exists for the circuit that satisfy KVL at all times. This result is reassuring and consistent with the behavior of conventional SC converters, where it has been shown in the previous sections that this instantaneous voltage mismatch at phase transitions is what gives rise to the power loss. Hence, conventional SC converters have to rely on high switching frequency or larger capacitor values to minimize the voltage mismatch and the associated power loss.

However, with soft-charging operation, the SC stage output node is connected to an inductor, and the inductor voltage is allowed to change instantaneously during phase transitions, as opposed to the capacitor voltages, which must be continuous. Stated in another way, the parameter Δv_{out} defined previously is no longer a state variable in a switch-linear circuit, and can be discontinuous. As a result, the change in output voltage in Phase 1 due to the current load, Δv_{out}^1, does not necessarily equal $-\Delta v_{out}^2$. Therefore, the inductor introduces one more degree of freedom to the system. To mathematically express this additional degree of freedom, the bases $\mathbf{w}$ and $\mathbf{u}$ can be modified by removing the last element in each column (the entry that represents Δv_{out}), resulting in the new bases $\bar{\mathbf{w}}$ and $\bar{\mathbf{u}}$. Now, replacing the bases in Eq. (2.24) with the newly formed $\bar{\mathbf{w}}$ and $\bar{\mathbf{u}}$, we obtain for the soft-charging converter:

$$\begin{bmatrix} \bar{\mathbf{w}}_\mathbf{1} & \bar{\mathbf{w}}_\mathbf{2} & \bar{\mathbf{u}}_\mathbf{1} & \bar{\mathbf{u}}_\mathbf{2} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ b_1 \\ b_2 \end{bmatrix} = \mathbf{0}\,. \tag{2.25}$$

Mathematically, the matrix in Eq. (2.25) has a reduced rank compared to the one in Eq. (2.24), and thus a non-zero solution can be found.

Solving Eq. (2.25) for the Dickson converter, we obtain

$$\begin{bmatrix} a_1 \\ a_2 \\ b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} 0.120 \\ -0.697 \\ -0.607 \\ -0.364 \end{bmatrix}. \tag{2.26}$$

The voltage change vectors in each phase can then be found using Eq. (2.20) Eq. (2.21), yielding

$$\mathbf{\Delta v^1} = \begin{bmatrix} 0 \\ 0.408 \\ 0 \\ 0.4088 \\ -0.408 \end{bmatrix} \text{ and } \mathbf{\Delta v^2} = \begin{bmatrix} 0 \\ -0.408 \\ 0 \\ -0.408 \\ -0.408 \end{bmatrix}. \tag{2.27}$$

Note that the original bases are used to obtain the voltage change at each node. From Eq. (2.27), it can be seen that the net change in the capacitor voltages is zero (i.e., each column adds to zero), except for the last entry. This entry represents Δv_{out}, which is the node that can be discontinuous owing to the soft-charging operation. Having obtained the change in capacitor voltage required to satisfy KVL in each phase, we can then calculate the required capacitance for soft-charging operation as:

$$C_j = q_j / \Delta v_{cj}\,, \tag{2.28}$$

for each capacitor j. Equation (2.38) requires the charge that flows into each flying capacitor to be found for each phase. For any well-posed switched-capacitor topology, a charge flow vector can be obtained for each phase either by inspection [12] or Kirchhoff's current law [15]. In this work, the charge flow vector is defined as the vector of charge that flows into the positive terminal of each element in the circuit and is given in the form of

$$\mathbf{q} = \begin{bmatrix} q_{in} & q_{c1} & q_{c2} & q_{c3} & q_{out} \end{bmatrix}.$$

The charge flow vectors for the Dickson converter of this example are found to be

$$\mathbf{q^1} = \begin{bmatrix} -1 & 1 & -1 & 1 & 2 \end{bmatrix} \text{ and } \mathbf{q^2} = \begin{bmatrix} 0 & -1 & 1 & -1 & 2 \end{bmatrix}.$$

Together with the voltage change vector found in Eq. (2.27), the capacitor values are obtained using Eq. (2.38) and are simplified as follows.

$$\begin{bmatrix} C_1 \\ C_2 \\ C_3 \end{bmatrix} = \begin{bmatrix} 1 \\ \infty \\ 1 \end{bmatrix}.$$

It can be seen that the Dickson topology can achieve complete soft-charging only when $C_2 = \infty$ and $C_1 = C_3$. In practice, this means that it can *approach* soft-charging with a C_2 large enough compared to C_1 and C_3. As can be seen from Eq. (2.27), the output voltage ripple has the same magnitude as the voltage ripple of C_1 and C_3 under soft-charging operation. Thus, for soft-charging operation with the Dickson converter, a designer would want to minimize the charging/discharging loss by maintaining a relatively large C_2/C_1 ratio while keeping the output ripple of the SC stage

tolerable with a second-stage converter or an inductor.

To summarize, the following steps are used to determine whether any given SC topology is compatible with soft-charging or resonant operation using a single inductor connected to the output of the SC stage:

1. Obtain the reduced loop matrix for each phase ($\mathbf{A_1}$ and $\mathbf{A_2}$) using KVL analysis.
2. Add a row of [1 0 0 ... 0] to $\mathbf{A_1}$ and $\mathbf{A_2}$, obtaining $\mathbf{A_{1m}}$ and $\mathbf{A_{2m}}$.
3. Find the collective nullspace bases of $\mathbf{A_{1m}}$ and $\mathbf{A_{2m}}$ ($\mathbf{w}$ and $\mathbf{u}$ respectively).
4. Remove the last row of $\mathbf{w}$ and $\mathbf{u}$ to obtain $\bar{\mathbf{w}}$ and $\bar{\mathbf{u}}$.
5. Use Eq. (2.25), Eq. (2.20) and Eq. (2.21) to find the change in capacitor voltages.
6. Find the charge transfer vector for each capacitor [12, 15].
7. Use Eq. (2.38) to find the capacitance values required for soft-charging.

As demonstrated in this section, for a two-phase SC dc-dc converter, if a capacitor voltage change vector, $\mathbf{\Delta v_c}$, can be found to satisfy KVL at all times, and the resultant capacitor values required are practical (finite and positive), the given topology is able to perform soft-charging and resonant operation and will exhibit no charging/discharging loss. Otherwise, at least one loop of the circuit will not be able to perform soft-charging, and the benefit will be limited.

2.3.2 Simulation verification

To verify that the analytical method is correct, the Dickson converter shown in Fig. 2.12 is simulated using LTSpice with simulation parameters given in Tables 2.1 and 2.2. A total capacitance of 30 μF is used for the flying capacitors. In hard-charging (conventional) operation, an additional 100 μF output capacitor is added in parallel to the current load while there is no output capacitance in the soft-charging simulation. The converters are operated at a fixed duty ratio of 0.5. The simulated power losses are plotted in Fig. 2.14. It can be seen that the hard-charging power loss decreases linearly as switching frequency increases, while leveling off at high frequency, showing

Table 2.1: Simulation parameters.

V_{in}	5 V
I_{load}	2 A
R_{on}	10 mΩ
R_{ESR}	1 mΩ
$C_{\text{o, hard-charging}}$	100 μF
$C_{\text{o, soft-charging}}$	0.1 μF

Table 2.2: Flying capacitor values.

Configuration	C_1 (μF)	C_2 (μF)	C_3 (μF)
Hard-charging	10	10	10
Soft-charging 1	10	10	10
Soft-charging 2	5	20	5

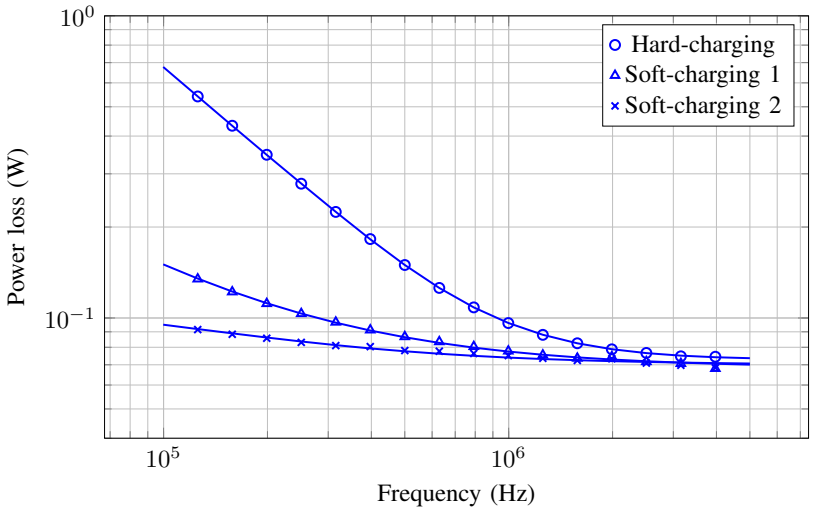


Figure 2.14: Power loss of Dickson converter at different frequencies.

the transition from SSL to FSL. In soft-charging operation, a significant reduction in power loss at lower frequencies is seen when the capacitors are such that $C_1 = C_2 = C_3$, as in the hard-charging case. However, a more prominent reduction is seen when the capacitor values are chosen such that $C_2/C_1 = 4$, plotted in Fig. 2.14 as "Soft-charging 2". This confirms that the Dickson converter can approach full soft-charging by maintaining a high C_2/C_1 ratio, as predicted by the analysis in this work.

The currents through the capacitor C_2 of the Dickson SC converter (Fig. 2.12) in hard-charging and soft-charging operations with the converter switching at 250 kHz are shown in Fig. 2.15. The different waveforms are shifted apart in the time axis for clearer observation. It can be seen that under hard-charging condition, the capacitor current resembles the exponential discharge, as expected. With soft-charging 1, both the magnitude and the width of the impulse are reduced, while the tail of the exponential decay is raised. In the soft-charging 2 case, with capacitor values selected according to the analysis result, the height and the width of the impulse are further reduced and current waveform resembles more of a square wave. The transient effect is not completely eliminated, due to the fact that perfect soft-charging cannot be achieved. To quantify the change in the current waveform, the RMS and the average currents through the capacitor for one phase duration are calculated and tabulated in Table 2.3. It can be seen that while in all cases the capacitor supplies the same average current over a phase duration, the RMS value of the current

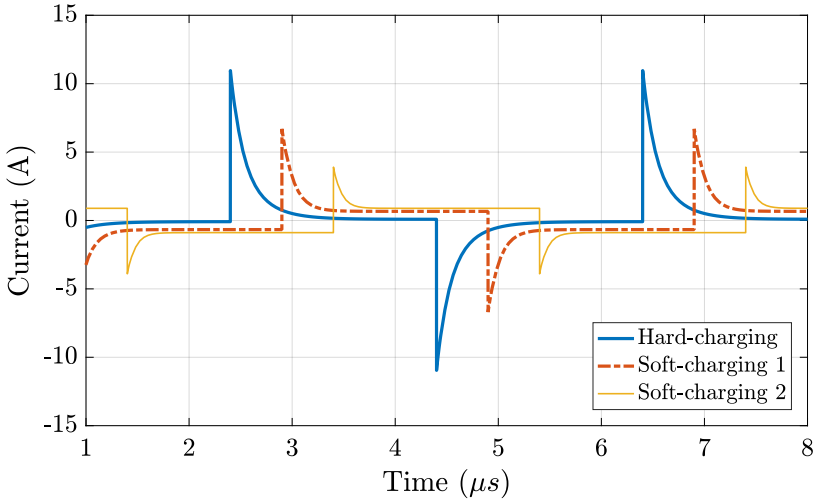


Figure 2.15: Current waveform of capacitor C_2 of the Dickson SC converter.

Table 2.3: The RMS and average current of capacitor C_2 in a single phase.

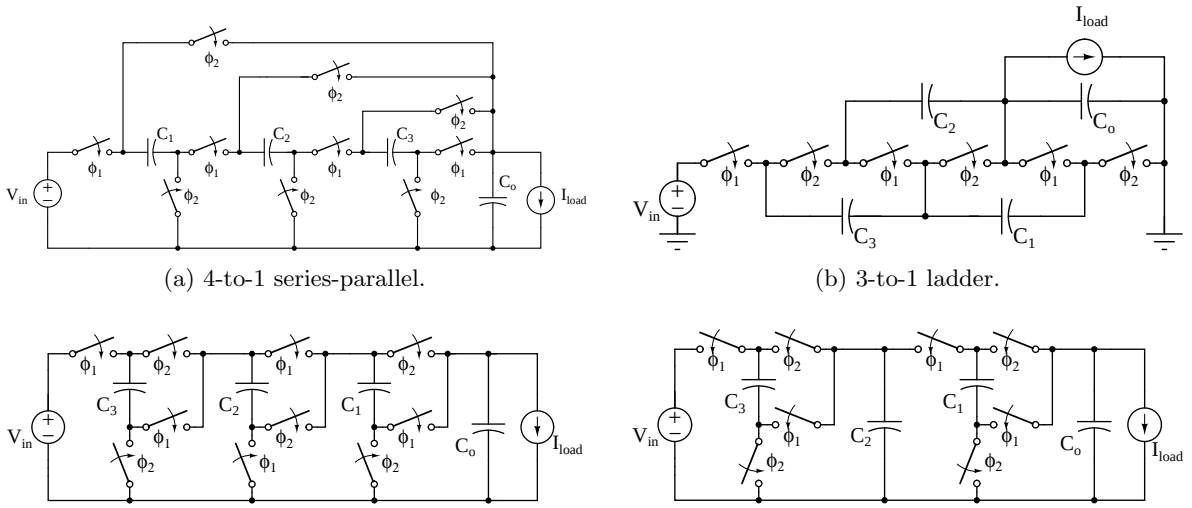
Configuration	RMS current (A)	Average current (A)
Hard-charging	2.19	1.00
Soft-charging 1	1.40	1.00
Soft-charging 2	1.11	1.00

decreases from hard-charging operation to soft-charging operation. Again soft-charging 2 is an improvement over soft-charging 1. Thus, the soft-charging operation reduces the impedance in the SSL region due to the improvement in the charging and discharging current waveform.

2.3.3 Application to other topologies

The general analysis method proposed is applied to four additional commonly used two-phase switched-capacitor converter topologies: series-parallel, ladder, Fibonacci and doubler. The schematic drawings are shown in Fig. 2.16a, 2.16b, 2.16c and 2.16d respectively. The same analysis is repeated for each of them and the results are shown in Fig. 2.17.

It can be seen that for the series-parallel converter, a simple requirement for soft-charging is that all the flying capacitors have the same value. Under soft-charging condition, the output voltage ripple is shown to be equal to $N-1$ times the change in any of the capacitor voltages, where N is the conversion ratio. These observations agree with the experimental work in [21]. In addition, the Fibonacci converter is also found capable of soft-charging operation with equal capacitors. On the other hand, for the ladder configuration, one can see that a negative capacitance is needed on C_2 for soft-charging operation, which is not achievable. This means that the change in capacitor voltage of C_2 is in the opposite direction of what is required to satisfy KVL. Thus, the single-output ladder topology is not compatible with soft-charging without modification, and a limited



(a) 4-to-1 series-parallel.

(b) 3-to-1 ladder.

(c) 5-to-1 Fibonacci.

(d) 4-to-1 doubler.

Figure 2.16: Common switched-capacitor converter topologies.

$$\mathbf{\Delta v} = \begin{bmatrix} \Delta v_{in} \\ \Delta v_{c1} \\ \Delta v_{c2} \\ \Delta v_{c3} \\ \Delta v_{out} \end{bmatrix}, \mathbf{C} = \begin{bmatrix} C_1 \\ C_2 \\ C_3 \end{bmatrix}$$

(a) General.

$$\mathbf{\Delta v^1} = \begin{bmatrix} 0 \\ 1 \\ 1 \\ 1 \\ -3 \end{bmatrix}, \mathbf{\Delta v^2} = \begin{bmatrix} 0 \\ -1 \\ -1 \\ -1 \\ -1 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad \mathbf{\Delta v^1} = \begin{bmatrix} 0 \\ 1 \\ 1 \\ 1 \\ -2 \end{bmatrix}, \mathbf{\Delta v^2} = \begin{bmatrix} 0 \\ -1 \\ -1 \\ -1 \\ -1 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} 1 \\ -2 \\ 1 \end{bmatrix}$$

(b) Series-parallel. (c) Ladder.

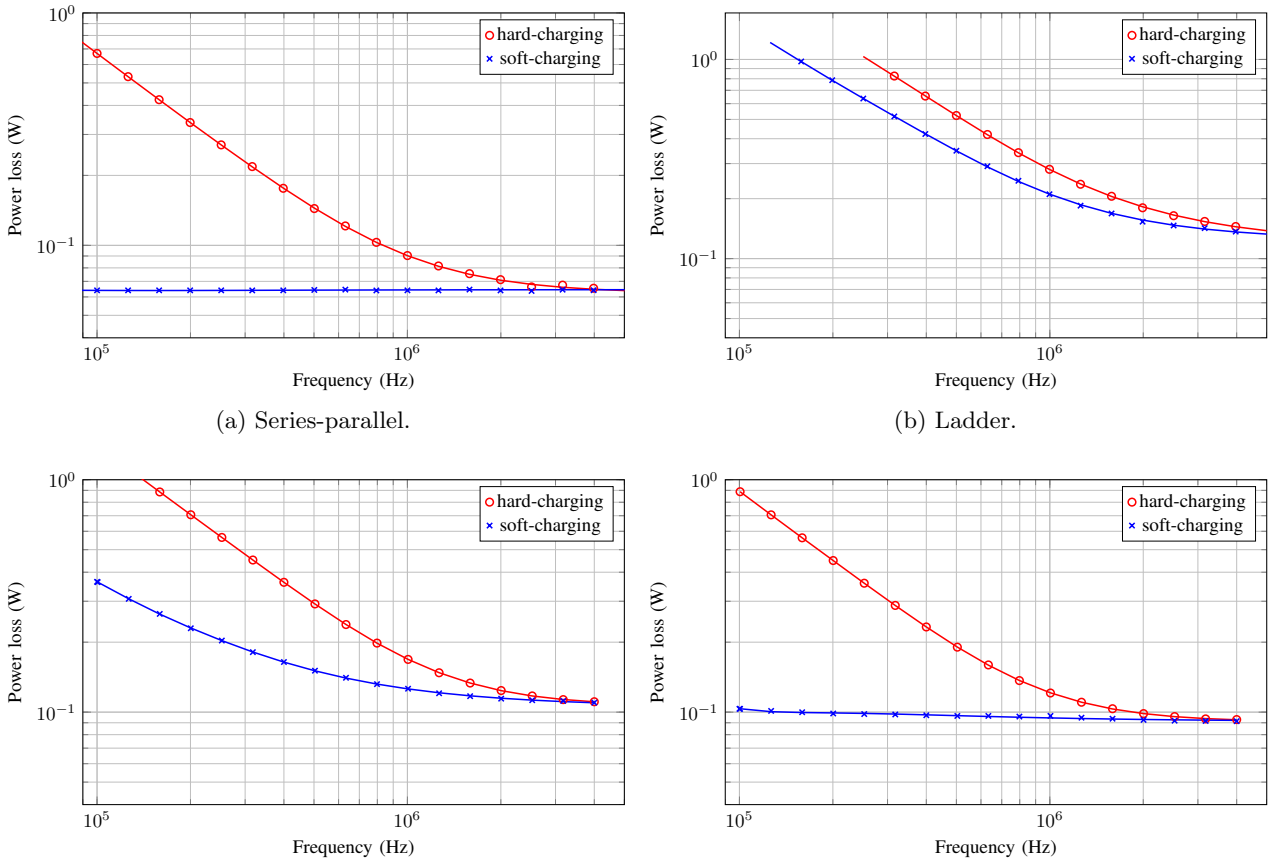
$$\mathbf{\Delta v^1} = \begin{bmatrix} 0 \\ 2 \\ -1 \\ 1 \\ -3 \end{bmatrix}, \mathbf{\Delta v^2} = \begin{bmatrix} 0 \\ -2 \\ 1 \\ -1 \\ -2 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad \mathbf{\Delta v^1} = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \\ -1 \end{bmatrix}, \mathbf{\Delta v^2} = \begin{bmatrix} 0 \\ -1 \\ 0 \\ 0 \\ -1 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} 1 \\ \infty \\ \infty \end{bmatrix}$$

(d) Fibonacci. (e) Doubler.

Figure 2.17: Voltage change vectors and relative capacitor values for soft-charging operation.

improvement is expected. As for the doubler converter, both C_1 and C_2 have to be infinite for complete soft-charging, indicating a partial soft-charging capability similar to that of the Dickson converter.

To verify the analysis results, the circuits shown in Fig. 2.16 are simulated with the same pa-



(a) Series-parallel.

(b) Ladder.

(c) Doubler.

(d) Fibonacci.

Figure 2.18: Power loss of hard-charging and soft-charging SC converters from LTSpice simulation.

rameters as those of the Dickson converter. Equal flying capacitors are used in all cases. Again, a constant current source is used as the load instead of an inductor to simplify the simulation and remove the effect of resonance, since in practice, operation below the critical frequency is to be avoided as shown in Section 2.2. The corresponding power loss curves are plotted in Fig. 2.18. It should be noted that the power loss values are not intended for cross-comparison between different SC topologies. Rather, it is the reduction of the power loss by changing from hard-charging operation to soft-charging operation that is of key interest here. For both the series-parallel converter and the Fibonacci converter, soft-charging operation results in a significantly lower power loss in SSL region than in the hard-charging case, and the loss is almost independent of the frequency. The ladder configuration only receives very limited benefit from soft-charging and a strong frequency dependency is still seen on the power loss plotted in Fig. 2.18b. The doubler converter shows moderate improvement with soft-charging. These simulation results agree with the prediction of the analytical technique presented earlier.

Since the Fibonacci converter is shown to be able to achieve full soft-charging operation, it is

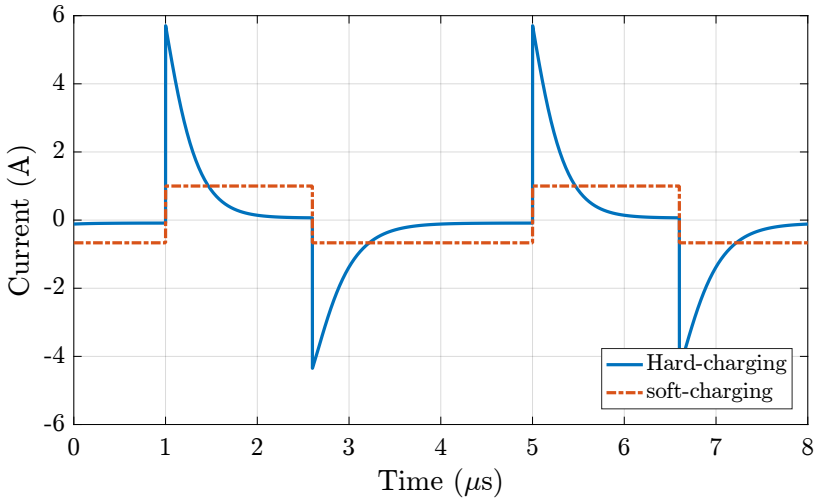


Figure 2.19: Current waveform of capacitor C_3 of the Fibonacci converter.

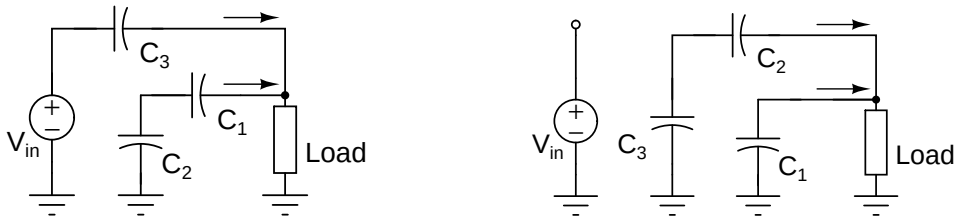
Table 2.4: The RMS and average of the absolute current of capacitor C_2 of the Fibonacci converter.

Configuration	RMS current (A)	Average current (A)
hard-charging	1.45	0.800
soft-charging	0.816	0.800

useful to examine the current waveform of the Fibonacci converter, as shown in Fig. 2.19. It can be seen that the waveform in soft-charging operation is a square wave, confirming that the current transient associated with capacitor charge redistribution has been eliminated. Table 2.4 shows the RMS and average of the absolute values of the current through capacitor C_3 of the Fibonacci converter. It can be seen that now the RMS current is almost equal to the average current in the soft-charging case, ensuring the lowest power loss.

2.4 Achieving Complete Soft-charging Operation for Dickson Converter using Split-Phase Control

In the previous section, it has been shown that the Dickson converter is not able to achieve complete soft-charging operation. Flying capacitor values can be adjusted such that the converter approaches soft-charging operation, but the resultant configuration has capacitors with uneven values connected in series, which reduces the capacitor utilization. In this section, a control method to achieve complete soft-charging operation is proposed, without incurring additional components.



(a) Phase 1. (b) Phase 2.

Figure 2.20: Two-phase operation of a 4-to-1 Dickson converter.

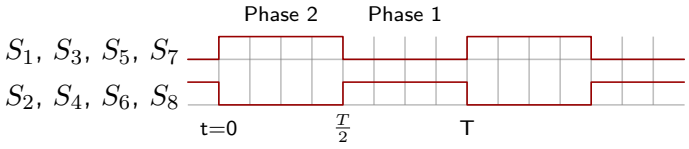


Figure 2.21: Gate signals of switches for two-phase operation of Dickson converter. High represents ON and low represents OFF.

2.4.1 Incomplete soft-charging operation with conventional two-phase control

The control signals for the two-phase operation are given in Fig. 2.21 and the equivalent circuits are reproduced in Fig. 2.20, and as can be seen, the converter simply operates at a 50% duty ratio.

For conventional (hard-charging) operation, the flying capacitor network is directly connected to the output, with a large output capacitance C_o acting as a voltage-source load. Thus, a large current transient occurs during the phase switching instances due to the capacitor voltages mismatch and the resultant charge redistribution process. The current waveforms for the capacitors of the converter in SSL operation are shown in Fig. 2.22, using the simulation parameters given in Table 2.5. It can be seen that there is a large impulse current through each capacitor (and thus through switches) at phase transitions.

In soft-charging operation, the output capacitance is removed so that the output voltage of the SC stage can change instantaneously to compensate for the difference in capacitor voltages. By eliminating the voltage mismatch and the resultant current impulse, soft-charging SC converters

Table 2.5: Simulation parameters.

V_{in}	40 V
I_{load}	2 A
f_{sw}	100 kHz
$R_{ds,on}$	10 mΩ
R_{ESR}	1 mΩ
C_1, C_2, C_3	10 μF
$C_{o,hard-charging}$	100 μF
$C_{o,soft-charging}$	None

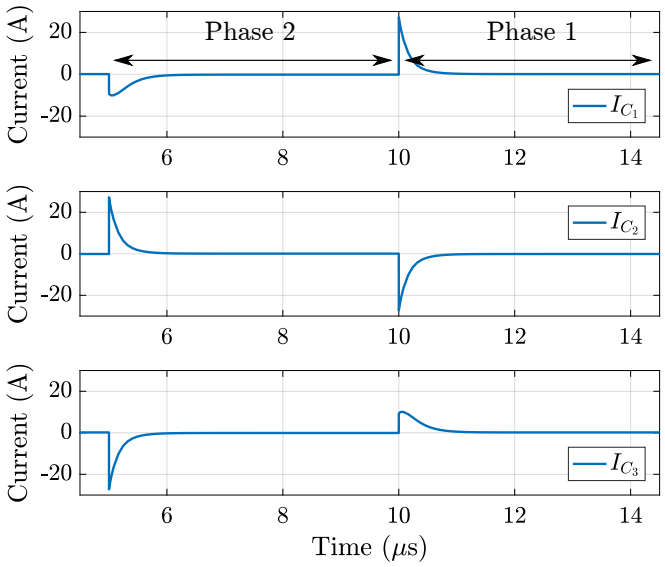


Figure 2.22: Capacitor current waveforms of the Dickson SC converter in conventional *two-phase hard-charging* operation. Simulation parameters are given in Table 2.5.

exhibit the same behavior as an SC converter in FSL, while operating at a switching frequency corresponding to the SSL region of a conventional design. While the current load ensures that there is no transient current drawn from the SC converter due to the voltage mismatch between the capacitor network and the final output node, complete soft-charging operation also requires that there is no voltage mismatch among the internal capacitor connections of the SC stage, so that there is no charge redistribution within the flying capacitor network, as analyzed in the previous section. For example, by applying KVL to the equivalent circuits in Fig. 2.13, the following requirements can be found for soft-charging operation.

$$\text{Phase 1: } V_{in} - V_{C_3} = V_{C_2} - V_{C_1} \tag{2.29}$$

$$\text{Phase 2: } V_{C_3} - V_{C_2} = V_{C_1} \tag{2.30}$$

However, constraints (2.29) and (2.30) *cannot* be satisfied during the transition between phases when the Dickson converter is operated with a conventional, two-phase control scheme. Figure 2.23 shows the voltage and current waveforms of interest during the transition from Phase 2 to Phase 1. It can be seen that, due to the charging and discharging process in Phase 2, the two voltage values, $(V_{in} - V_{C_3})$ and $(V_{C_2} - V_{C_1})$, are different and diverging. Thus, when the converter transitions to Phase 1 and forces the two nodes to have the same voltage, charge redistribution occurs, which results in the large current impulse as seen in the bottom plot of Fig. 2.23, which shows the current through capacitor C_2 of Fig. 2.12. A similar scenario happens at the start of Phase 2, when $(V_{C_3} - V_{C_2})$ is always greater than V_{C_1}, making it also a hard-charging transition from Phase 1 to Phase 2. From a circuit intuition point-of-view, the voltage mismatch is due

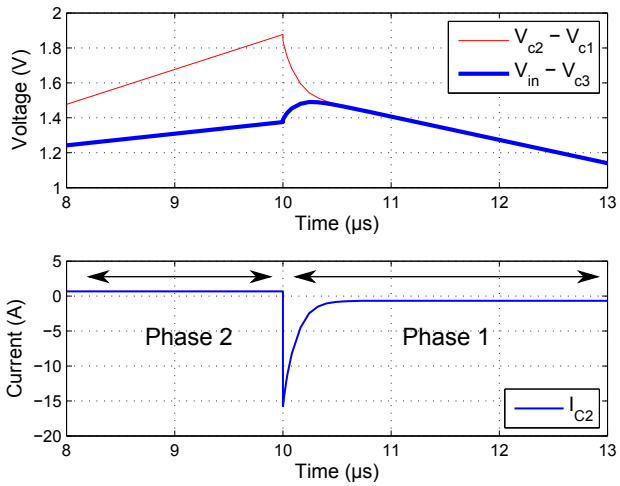


Figure 2.23: Voltage and current waveforms for two-phase soft-charging operation of the Dickson converter.

to the asymmetry in the capacitor connection, particularly for the outermost (C_3) and innermost capacitor (C_1). As can be seen in Fig. 2.13, these two capacitors are in series with another capacitor in one phase but not in the other phase. As a result, not all current paths have the same equivalent capacitance, giving rise to voltage mismatch when transitioning to the other phase of operation. Therefore, unlike topologies such as series-parallel and Fibonacci, the Dickson SC converter cannot achieve complete soft-charging operation, despite using a current load. The current waveforms of all capacitors for the Dickson converter with a current-source load are plotted in Fig. 2.24. Comparing it to the hard-charging case in Fig. 2.22, while the magnitude and width of the current impulse are reduced with two-phase soft-charging operation, there is still significant transient effect and associated losses, owing to the internal capacitor voltage mismatch.

2.4.2 Complete soft-charging operation with split-phase control

To ensure that each branch in the capacitor network results in the same voltage at the output node, we propose the split-phase control of the Dickson converter, with two secondary phases introduced [32–34], as shown in Fig. 2.25. Phase 1a and 2a are the same as Phase 1 and Phase 2 in the original operation, while the Phase 1b configuration is a subset of Phase 1 and the Phase 2b configuration is a subset of Phase 2. The switching sequence is Phase 1b $\rightarrow$ Phase 1a $\rightarrow$ Phase 2b $\rightarrow$ Phase 2a. As can be seen from the schematic in Fig. 2.25c, in Phase 1b, C_2 discharges and C_1 charges, and thus $(V_{C_2} - V_{C_1})$ decreases while $(V_{in} - V_{C_3})$ remains constant. The circuit can transition from Phase 1b to Phase 1a when $(V_{C_2} - V_{C_1})$ equals $(V_{in} - V_{C_3})$, i.e., when (2.29) is satisfied. This process is illustrated in the voltage and current waveforms of Fig. 2.26. As can be seen, with the introduction of the additional "buffer" phase, 1b, KVL is satisfied during phase transitions and the current transient can be eliminated. Similarly, the circuit transitions from

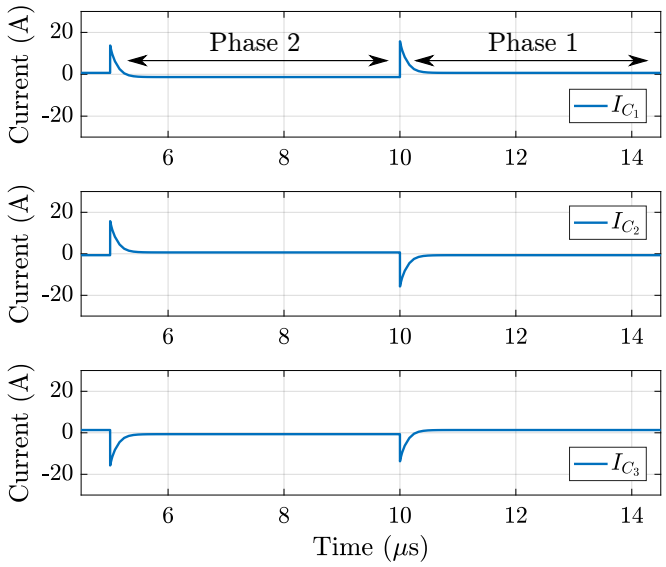


Figure 2.24: Capacitor current waveforms of the Dickson SC converter in *two-phase soft-charging* operation. Simulation parameter are given in Table 2.5.

Table 2.6: The average, RMS and peak values of current of capacitor C_2 in a single half period. Simulation parameters are as in Fig. 2.27.

Configuration	Average (A)	RMS (A)	Peak (A)
Hard-charging	1.00	3.52	27.3
Soft-charging, two-phase	1.00	1.91	15.8
Soft-charging, split-phase	1.00	1.15	2.00

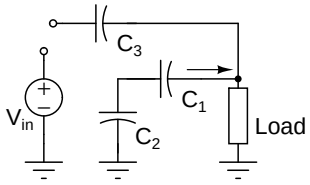
Phase 2b to Phase 2a when (2.30) is satisfied. The effect on the overall current waveform can be seen in Fig. 2.27, which shows the currents through all the capacitors in one complete switching cycle. It can be seen that, in contrast to the waveforms in Fig. 2.22 and Fig. 2.24, all of the currents have no transient component, and are of a constant value in each phase.

To quantify the improvement in the power transfer, the average, RMS and peak values of capacitor current for a half-period duration are calculated and tabulated in Table 2.6. For SC converters, the average capacitor current represents the delivered power, and is hence held fixed in this comparison. The RMS current reflects the conduction loss of the switches and capacitors, and should be as close to the average value as possible for high-efficiency operation. It can be seen that two-phase soft-charging operation reduces the RMS and peak values of the capacitor current, but to a limited extent. On the other hand, the proposed split-phase control achieves both the lowest RMS values and the lowest peak values. By eliminating the current transient, the converter efficiency can be improved and the current stress of the devices reduced.

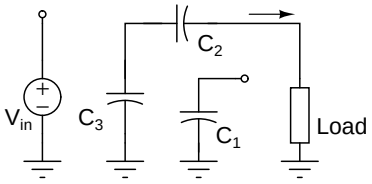
The switch control signals to achieve the proposed split-phase operations are shown in Fig. 2.28. It can be seen that compared to the original two-phase control in Fig. 2.21, the proposed switching

(a) Phase 1a.

(b) Phase 2a.



(c) Phase 1b.



(d) Phase 2b.

Figure 2.25: Split-phase operation of a 4-to-1 Dickson converter. Switching sequence: 1b→1a→2b→2a.

sequence only delays the turn-on of two switches (S_5 and S_8). Thus, generating the extra phases in the split-phase operation does not increase the switching frequency of the switches, and therefore introduces no added switching loss. Another advantage of the proposed split-phase control is the scalability of the technique. Even though the technique is illustrated with a 4-to-1 Dickson converter with only three flying capacitors, it can be applied to Dickson converters with larger conversion ratios without introducing more secondary phases [32]. This is because only the switch that connects to the input voltage and the switch that connects to the innermost capacitor (C_1) need to be delayed. Additional switches for higher conversion ratios follow the original gate signals as do switch S_6 and S_7. Therefore, there is no increase in control complexity as the conversion ratio increases.

2.4.3 Output impedance comparison

The output referred impedance of an SC converter encapsulates both the capacitor charge transfer loss and the conduction loss of the converter and is widely used to characterize the performance of such converters [14–16]. The output impedance can be calculated as

$$R_{out} = \frac{\frac{V_{in}}{N} - V_{out}}{I_{out}}, \tag{2.31}$$

where N is the conversion ratio. For a given switching frequency and converter volume, it is desirable to have an output impedance that is as low as possible. To illustrate the benefit of the split-phase soft-charging operation, the 4-to-1 step-down Dickson converter is simulated using Spice with simulation parameters given in Table 2.1. In the hard-charging operation, the duty ratio is fixed to 0.5 (as is convention) while the duty ratio of the split-phase operation is as found

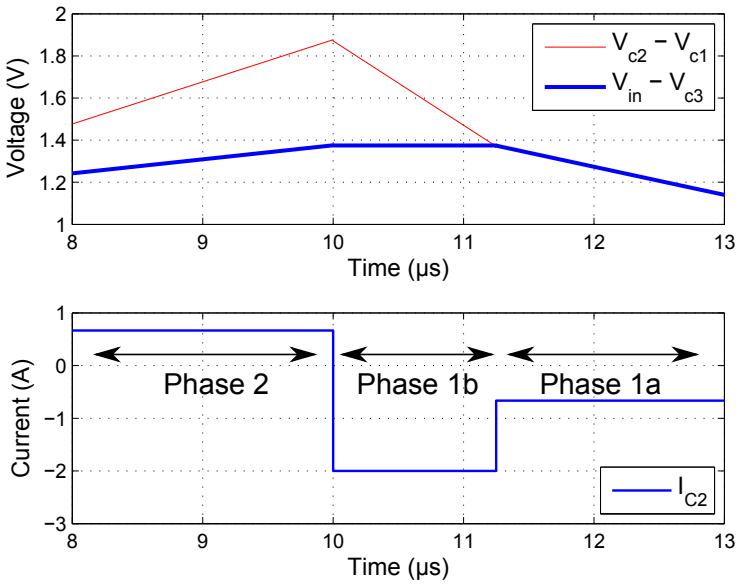


Figure 2.26: Voltage and current waveforms for split-phase soft-charging operation of the Dickson converter.

analytically in Section 2.4.4. The output impedance is plotted against switching frequency in Fig. 2.29. It can be seen that the conventional hard-charging Dickson converter shows two regions of asymptotic behavior as found in previous literature [12]. At low frequencies (slow switching limit, SSL), when the power loss due to the current transient dominates, the impedance decreases as the switching frequency increases. The impedance reaches a constant at high frequencies (fast switching limit, FSL), when the resistive conduction loss dominates. With two-phase soft-charging operation, the impedance in the SSL region is reduced significantly, owing to the current-source load. However, there is still non-negligible frequency dependent behavior since complete soft-charging operation cannot be achieved with two-phase Dickson converter. With the proposed split-phase control, however, it can be seen that now the output impedance is both low and independent of the switching frequency, due to the complete elimination of the charge transfer losses. Therefore, using split-phase control, soft-charging Dickson converters can achieve significant efficiency and power density improvement. It should be noted that the impedance at high frequencies in split-phase operation is slightly higher than the FSL impedance of the conventional two-phase operation. This is due to the fact that in the added phases (Phase 1b and Phase 2b), there is one path less that delivers current to the load, resulting in a slightly increased effective switch resistance. However, this increase in conduction loss will diminish as the converter conversion ratio increases.

2.4.4 Extending the analysis

While the preceding section presents an intuitive understanding of why the split-phase control eliminates the current transient in the operation of the Dickson converter, it is beneficial to for-

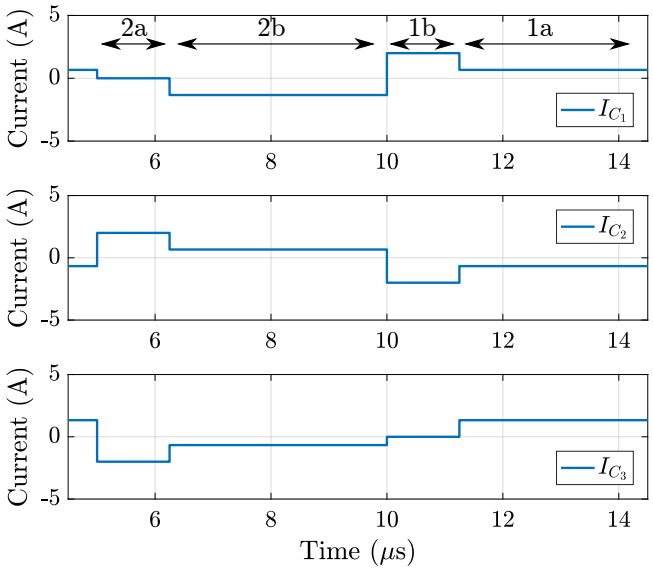


Figure 2.27: Capacitor current waveforms of the Dickson SC converter in *split-phase soft-charging* operation. Simulation parameters are given in Table 2.5.

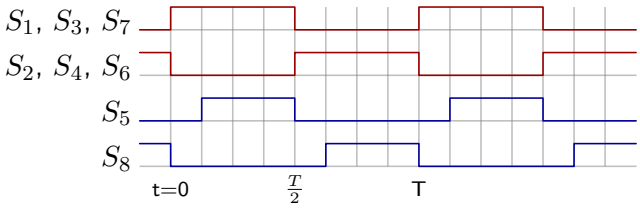


Figure 2.28: Gate signal for split-phase operation of the Dickson converter. High represents ON and low represents OFF.

mulate a general analysis. Existing numerical analysis methods such as that proposed in [18] can provide accurate predictions on the performance of SC converters. Instead, this work focuses more on analytical tools that provide additional insights into the operation of the proposed control. In Section 2.3, an analytical method was presented that determines whether an arbitrary SC topology is able to achieve complete soft-charging operation. However, the method is developed for an SC converter with two phases, and for the proposed split-phase control, a total of four different circuit states are present. Hence, the method is extended in this section to a higher number of phases. With a higher number of phases, the duty ratio of each phase becomes unknown. Therefore, unlike in Section 2.3 [28], where the capacitor values required by soft-charging operation are found given the expected duty ratio, the objective here is to find the corresponding duty ratios for complete soft-charging operation, given a set of capacitor values.

As explained in the previous section, complete soft-charging can be achieved if and only if the internal capacitor network satisfies KVL at all times, including at phase transitions. The aim of the analysis is thus to find the set of charge flow vectors for the capacitors, such that the corresponding

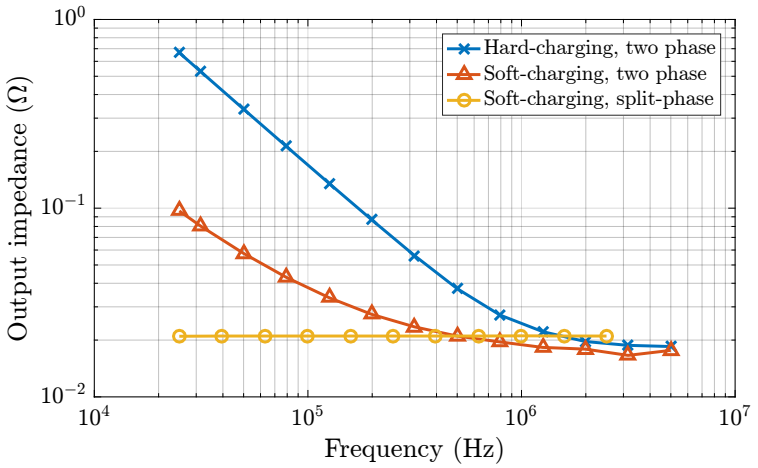


Figure 2.29: Simulated output impedance of the Dickson converter.

capacitor voltage changes result in node voltages that satisfy KVL during all phase transitions. To represent the KVL constraint, a voltage vector is first defined for the circuit elements as

$$\mathbf{v} = \begin{bmatrix} v_{in} & \mathbf{v_c}^{\mathrm{T}} & v_{out} \end{bmatrix}^{\mathrm{T}}, \tag{2.32}$$

where $\mathbf{v_c}$ is a column vector of the capacitor voltages. In each phase of Fig. 2.25, the circuit consists of a number of closed loops, where a KVL equation can be written for each loop. These KVL equations can be lumped into a matrix-vector product form [31] as

$$\mathbf{A_i v^i} = \mathbf{0}, \tag{2.33}$$

where $\mathbf{A_i}$ is called the reduced loop matrix for the ith phase. In this analysis, the entries of the loop matrices are positive if the circuit element is traversed from the negative terminal to the positive terminal and vice versa. At the end of phase i, the voltage vector becomes $\mathbf{v^i} + \mathbf{\Delta v^i}$, due to charge being delivered to the load, and the KVL equations become

$$\mathbf{A_i}(\mathbf{v^i} + \mathbf{\Delta v^i}) = \mathbf{0}. \tag{2.34}$$

From (2.33) and (2.34), we have from the property of linear circuits:

$$\mathbf{A_i \Delta v^i} = \mathbf{0}. \tag{2.35}$$

Similar to the voltage vector, a charge flow vector is defined as the vector of charge that flows into the positive terminal of each element in the circuit and is given in the form of

$$\mathbf{q} = \begin{bmatrix} q_{in} & \mathbf{q_c}^{\mathrm{T}} & q_{out} \end{bmatrix}^{\mathrm{T}}, \tag{2.36}$$

where $\mathbf{q_c}$ is a column vector of charges that flow into the flying capacitors. In the ith phase, KCL equations can be expressed by

$$\mathbf{B_i q^i} = \mathbf{0}, \tag{2.37}$$

where $\mathbf{B_i}$ represents the reduced incidence matrix of the topology [31]. Entries of $\mathbf{A_i}$ and $\mathbf{B_i}$ can be directly obtained from KVL and KCL equations of the circuit. Moreover, for a capacitor, the change in voltage and the charge flow is related by

$$q_c = C\Delta v_c\,. \tag{2.38}$$

In addition, for periodic steady-state operation, there is also a condition being that the net charge that flows into a capacitor in a period is zero:

$$\sum_{phases} \mathbf{q_c^i} = \mathbf{0}. \tag{2.39}$$

Combining the constraints given by Eqs. (2.35) and (2.37) to (2.39), a set of non-zero charge vectors ($\mathbf{q^i}$) required for soft-charging operation can be obtained. A detailed derivation of the charge flow vectors from the constraints for the 4-phase Dickson converter in Fig. 2.25 is provided in the appendix and only the result is given in this section. Using equal flying capacitor values, the final charge vectors are found to be

$$\mathbf{q^i} = \begin{bmatrix} q_{in} \\ q_{c3} \\ q_{c2} \\ q_{c1} \\ q_{out} \end{bmatrix}, \mathbf{q^{1a}} = \begin{bmatrix} -2 \\ 2 \\ -1 \\ 1 \\ 3 \end{bmatrix}, \mathbf{q^{2a}} = \begin{bmatrix} 0 \\ -1 \\ 1 \\ -2 \\ 3 \end{bmatrix},$$
$$\mathbf{q^{1b}} = \begin{bmatrix} 0 \\ 0 \\ -1 \\ 1 \\ 1 \end{bmatrix}, \mathbf{q^{2b}} = \begin{bmatrix} 0 \\ -1 \\ 1 \\ 0 \\ 1 \end{bmatrix}. \tag{2.40}$$

From the definition in (2.36), the last entries in the charge vectors are the amount of charge delivered to the load. Assuming a constant current load, the last entry of each of the charge vectors is thus in proportion to the relative duration of each phase. Since the total charge delivered to the load in a period is 8 units $(3 + 3 + 1 + 1)$, we derive that for complete soft-charging operation of the Dickson converter with equal flying capacitance, the duty ratio of each phase is

$$D^{1a} = \frac{3}{8},\ D^{2a} = \frac{3}{8},\ D^{1b} = \frac{1}{8},\ D^{2b} = \frac{1}{8}. \tag{2.41}$$

Table 2.7: Duty ratio of each phase for the Dickson topology at different conversion ratios.

Conversion ratio	4:1	6:1	8:1	N:1
D_{1a}	$3/8$	$4/12$	$5/16$	$(N+2)/4N$
D_{2a}	$3/8$	$4/12$	$5/16$	$(N+2)/4N$
D_{1b}	$1/8$	$2/12$	$3/16$	$(N+2)/4N$
D_{2b}	$1/8$	$2/12$	$3/16$	$(N+2)/4N$

Table 2.8: Switching sequences.

Sequence 1:	Phase 1b → Phase 1a → Phase 2b → Phase 2a
Sequence 2:	Phase 2a → Phase 2b → Phase 1a → Phase 1b
Sequence 3:	Phase 1a → Phase 2a → Phase 1b → Phase 2b

These duty ratios are what were used to obtain the simulation results in Fig. 2.27. In addition, the required duty ratio for complete soft-charging operation varies with the native conversion ratio. Similar analysis has been carried out for conversion ratios of 6:1 and 8:1, and the results are shown in Table 2.7. It can be seen that, as the conversion ratio increases, the duty ratios of the "a" phases approach 0.25 each and those of "b" phases approach 0.25 each. Thus, there is no extreme duty ratio as the conversion ratio increases.

Another useful result that can be obtained from the analysis is that soft-charging operation can be achieved regardless of the order of the switching phases, since the preceding derivation does not rely on the sequence of the phases. With the proposed split-phase control, there are four phases. These four phases can be ordered to form six distinct periodic sequences in total, and three representative ones are shown Table 2.8. While Sequence 1 is the same sequence obtained from the voltage balance intuition in Section 2.4.2, Sequence 2 is the reverse of Sequence 1; and in Sequence 3, the two original phases (Phase 1a and 2a) are adjacent instead of being separated by the secondary phases. The duration of each phase is still given by the constraint of Eq. (2.41).

Figure 2.30 shows the simulated current waveforms for these switching sequences. It can be seen that all three of the switching sequences result in a non-impulse current, showing that complete soft-charging operation can be achieved for each switching sequence. This is a particularly useful result: as will be discussed in Section 2.5, the intuitively devised sequence (Sequence 1), cannot be easily implemented due to practical constraints, whereas other sequences may yield practical and feasible solutions.

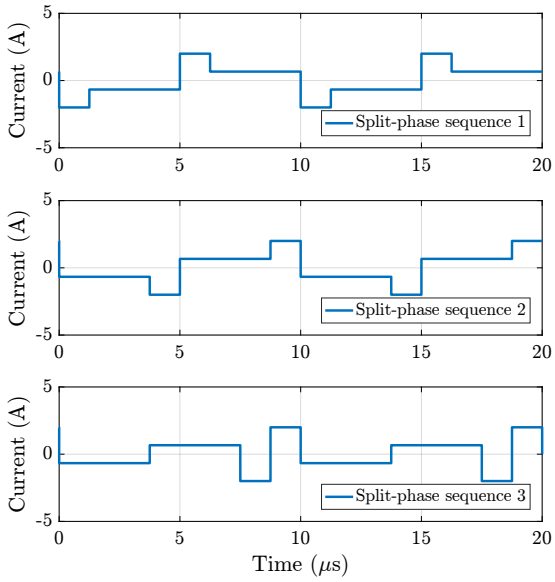


Figure 2.30: Current waveform of capacitor C_2 of the Dickson SC converter under different switching sequences.

2.5 Experimental Results

In this section, the proposed theories and techniques are validated with hardware results. A hybrid Dickson prototype is implemented, which can be reconfigured to operate in hard-charging, two-phase soft-charging and split-phase soft-charging mode.

The Dickson converter has a conversion ratio of 8 to 1 and its schematic drawing is shown in Fig. 2.31. A total of 12 GaN switches are used, together with seven flying capacitors. The design specification can be found in Table 2.9 while a full component listing is provided in Table 2.10. A photograph of the hardware prototype is shown in Fig. 2.32. All the components are placed on the

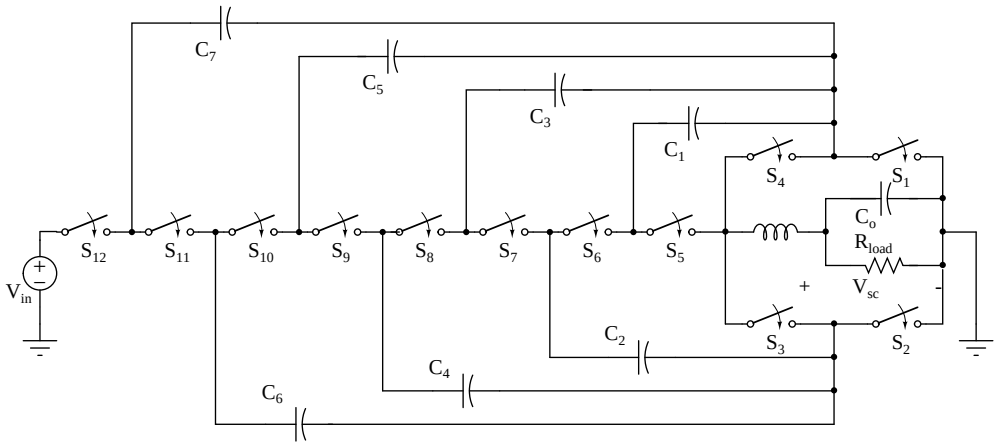


Figure 2.31: Schematic drawing of the two-phase soft-charging Dickson SC converter.

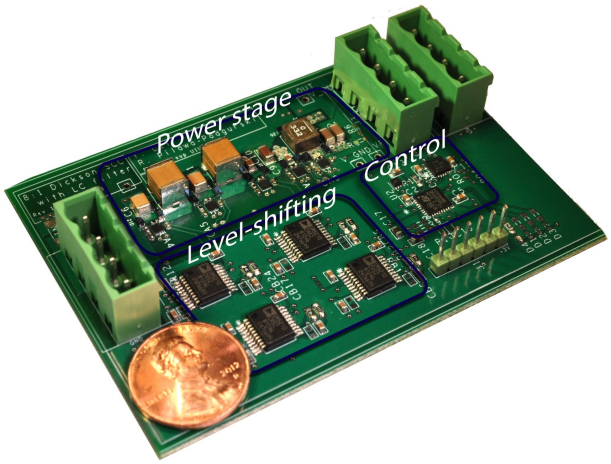


Figure 2.32: Annotated photograph of the experimental converter prototype, with a US penny added for scale.

top side of the PCB for clear illustration.

First, the two-phase conventional (hard-charging) and two-phase soft-charging operations are compared. For the conventional configuration, the flying capacitors are all 2.2 μF. For the two-phase soft-charging configuration, capacitors of 2.2 and 0.22 μF, and an inductor of 3.3 μH are used, so that it can approach soft-charging operation, according to the analytical results in Section 2.3. The volume of the passive components of the two configurations are given in Table 2.11. The total volume of the passive components of the hybrid SC converter with the inductor is 454 mm^3 while that of the pure SC converter is 682 mm^3. It can be seen that even with the additional inductor, the volume of the proposed converter is still smaller than that of the pure SC converter, thanks to the improved utilization of capacitors due to soft-charging.

The measured efficiencies of the prototype at various load currents are plotted in Fig. 2.33. It can be seen that not only is the efficiency of the soft-charging converter always higher than that of the conventional hard-charging converter, but it also drops at a slower pace as the current increases, due to the lower output impedance. The efficiency represents an approximate 2x power loss reduction at 53 W. For both cases, the measured efficiencies do not include the power loss due to control circuit and gate drivers. The combined losses of these components are approximately 0.5 W, which is mainly attributed to the poor efficiency of the level-shifting circuit used to power the gate drivers. Overall, the experimental results demonstrate that the soft-charging SC converter simultaneously

Table 2.9: Tested specifications.

V_{in}	200 V DC
Conversion ratio	8:1
P_{out}	53 W
f_{sw}	250 kHz

Table 2.10: Component listing of the proposed converter.

Component	Part number	Parameters
S_{12}, S_5 - S_1	EPC2014	40 V, 16 mΩ, 10 A
S_{11} - S_6	EPC2007	100 V, 30 mΩ, 6 A
C_7, C_5	C1812X224K2RACTU	250 V, 0.22 μF
C_6, C_4	C2220C225MAR2CTU	250 V, 2.2 μF
C_3	C0805C224K1RACTU	100 V, 0.22 μF
C_2	C3216X7S2A225K160AB	100 V, 2.2 μF
C_1	C1608X7R1H224K080AB	50 V, 0.22 μF
C_o	C3216X5R1V226M160AC	35 V, 22 μF
Inductor	XAL5030-332	3.3 μH
Level-shifters	ADUM5210	
Microcontroller	STM32f051	

Table 2.11: Passive components volume comparison.

	Conventional	Soft-charging
Capacitor volume (mm^3)	681.8	378.9
Inductor volume (mm^3)	-	75.0
Total volume (mm^3)	681.8	453.9

achieves higher efficiency and higher power density than the conventional SC converter.

To see the similarity between resonant and soft-charging operations, the current through the inductor is shown in Fig. 2.34 at three different switching frequencies. As can be seen, for $f_{sw} = f_{crit}$ (Fig. 2.34b), the current is sinusoidal and reaches zero at each phase transition, and thus ZCS operation is achieved. For $f_{sw} > f_{crit}$ (Fig. 2.34a), the current has a much smaller ripple and the converter operates near FSL. For $f_{sw} < f_{crit}$ (Fig. 2.34c), the current goes negative in each phase. These experimentally obtained waveforms closely resemble the simulated waveforms in Fig. 2.10, with some voltage spikes as a result of switching dead-time in the practical implementation. Therefore, the hardware not only shows that soft-charging operation is able to achieve a high efficiency with smaller passive component footprint, but also confirms that resonant operation can be achieved at the specified frequency using the same technique.

Next, two split-phase soft-charging configurations are implemented, whose parameters are given in Table 2.12. The first split-phase configuration is to demonstrate the power density improvement by reducing the flying capacitance, while the second one is to demonstrate efficiency improvement by reducing the switching frequency and keeping the same capacitance compared to hard-charging. It should be noted that in practice, a soft-charging converter is most likely designed to achieve a combination of both. A photo of the power stage of the prototype in soft-charging configuration 1 is shown in Fig. 2.35.

The waveforms in this section are captured with soft-charging configuration 1. The voltage V_{sc} (from Fig. 2.31) as well as the switch gate signals are shown in Fig. 2.36. V_{sc} decreases during each

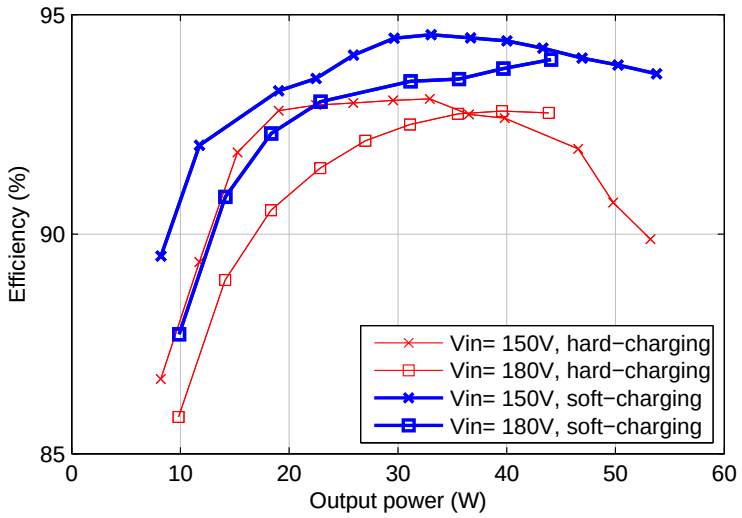
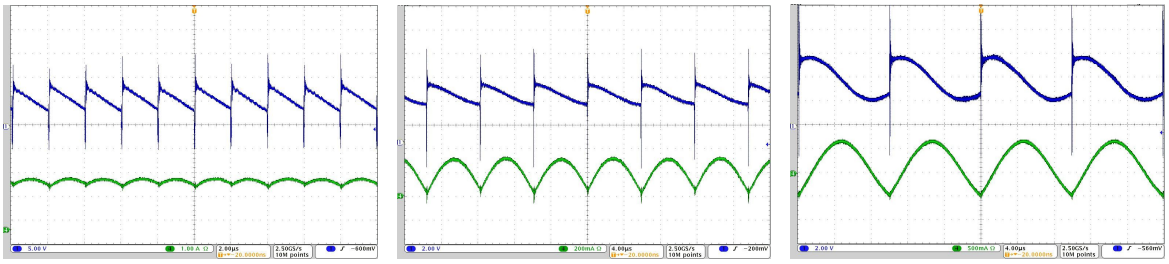


Figure 2.33: Measured efficiency for soft-charging and conventional SC converter prototypes.



(a) $f_{sw} = 250$ kHz $> f_{crit}$ (b) $f_{sw} = 90$ kHz $= f_{crit}$ (c) $f_{sw} = 50$ kHz $< f_{crit}$

Figure 2.34: SC stage voltage (V_{sc} in Fig. 2.31) (upper) and inductor current (lower).

phase due to the charging and discharging of capacitors, and jumps up after each major transition. Therefore V_{sc} resembles a sawtooth waveform. It can be seen that V_{sc} has a relatively large ripple, which is the result of the increased voltage ripple on the flying capacitors. This increased ripple is the key to enable smaller capacitors in soft-charging SC converters. The absolute slope of V_{sc} increases as load current increases. The flying capacitor and switching frequency should be chosen such that the voltage ripple on V_{sc} is a reasonable value, say 10% - 20% of the maximum output voltage value, since the ripple magnitude adds to the voltage stress of the switches. It can also be seen from the V_{sc} waveform in Fig. 2.36, that V_{sc} goes to about -2.0 V at every major phase transition. This is due to the dead-time implemented to prevent current shoot-through. During

Table 2.12: Design specifications and parameters.

	Hard-charging	Split-phase Prototype 1	Split-phase Prototype 2
f_{sw}	250 kHz	250 kHz	50 kHz
Inductor	-	3.3 μH	3.3 μH
Flying capacitors	2.2 μF	0.47 μF	2.2 μF

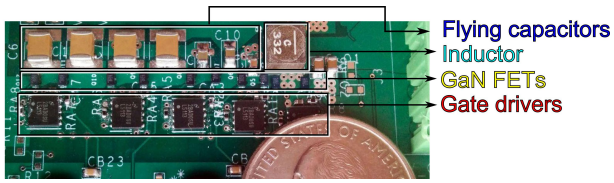


Figure 2.35: Photo showing the power stage of the hardware prototype of the proposed 8-to-1 Dickson SC converter. A US quarter is included for scale.

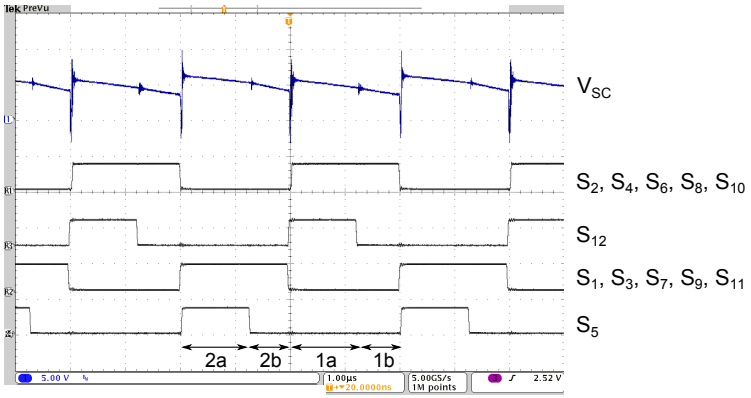


Figure 2.36: Output voltage (V_{sc} in Fig. 2.31) (top) and switching functions (lower). Bandwidth of the waveform capture is 1 Gsamples/s.

the dead-time, the equivalence of the body diode of the GaN devices is forced to conduct by the inductor, and the forward voltage of roughly 1.4 V [35] appears negatively on V_{sc}. The dead-time can be tuned to achieve the maximum efficiency of the converter [35], but the process is not carried out for this prototype. In addition, the output LC filter should be designed such that the ripple on V_{sc} in worst load condition results in an acceptable output voltage ripple at the output of the LC filter. This however, can be easily achieved since the ripple on V_{sc} is much smaller than what is commonly present at the input of the LC filter of a PWM magnetic converter. The output voltage after the inductor (V_{out}) is shown in Fig. 2.37. It can be seen that the ripples on V_{sc} are filtered by the LC circuit and the output is a steady dc voltage with 50 mV of ripple at 1A of load current.

The switching signals as seen in Fig. 2.36 are slightly different from those used in simulation (Fig. 2.28). This is because using the original phase sequence (1b $\rightarrow$ 1a $\rightarrow$ 2b $\rightarrow$ 2a) results in negative V_{ds} voltages across some of the switches, due to the large voltage ripples during the operation. Bidirectional blocking switches would have to be used, which would increase the complexity of the circuit and reduce the efficiency. Since it has been shown by the analysis in Section 2.4.4 that complete soft-charging operation can be achieved regardless of the switching sequence, the actual sequence used by the hardware prototype is Sequence 2 in Section 2.4.4 (i.e., 2a $\rightarrow$ 2b $\rightarrow$ 1a $\rightarrow$ 1b). This switching sequence results in no negative V_{ds} voltage on any of the switches so that the converter operates properly using the GaN FETs.

To demonstrate the soft-charging operation, the capacitor voltages are measured for both two-phase control and split-phase control. The simulated and measured waveforms for two-phase control

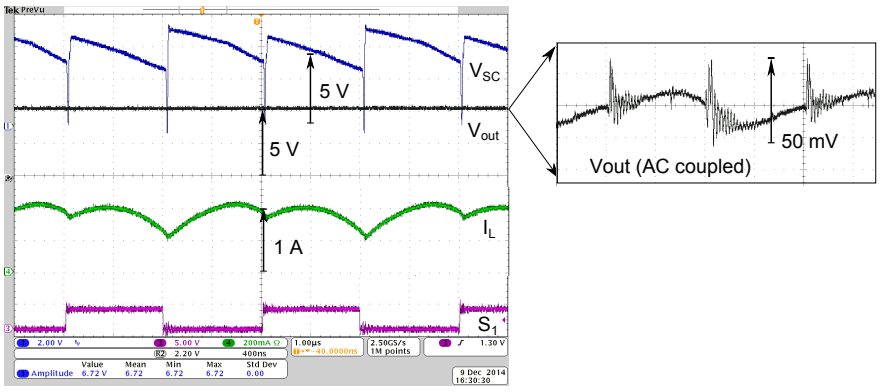
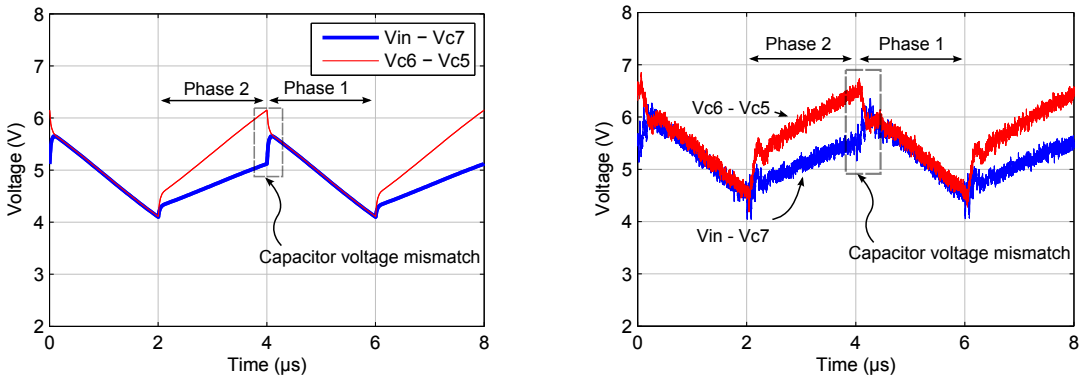


Figure 2.37: Converter voltage before (V_{sc} in Fig. 2.31)) and after (V_{out}) the LC filter, as well as inductor current. $V_{in} = 40$ V and $I_{load} = 1$ A. Waveform capture is band-limited to 25 Msamples/s for the AC coupled waveform.



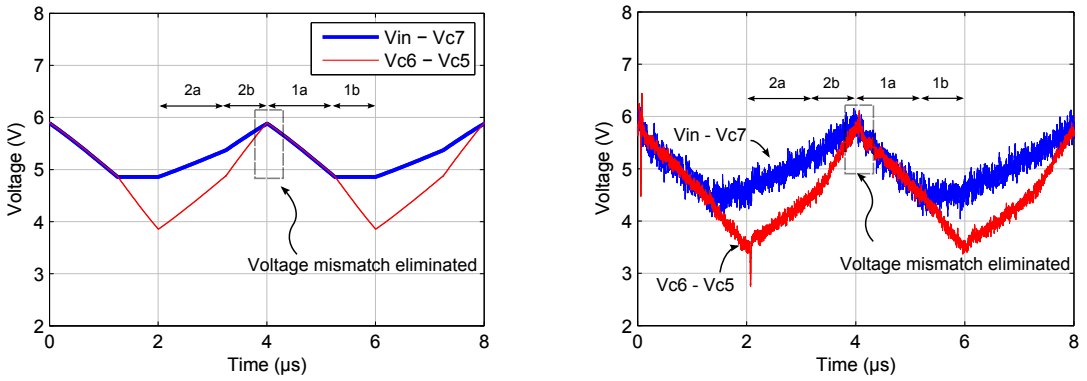
(a) Simulation. (b) Experiment.

Figure 2.38: Capacitor voltage mismatch during *two-phase* soft-charging operation.

are shown in Fig. 2.38. The experimental waveform clearly shows the mismatch in voltage $V_{in} - V_{c7}$ and $V_{c6} - V_{c5}$ during the transition between Phase 2 and Phase 1, as expected from the analysis and simulation. On the other hand, as shown in Fig. 2.39, the voltage mismatch has been eliminated by using the proposed split-phase control, as the two sets of voltages converge right before the switching occurs.

The efficiency of the soft-charging converter configuration 1 in split-phase operation is plotted in Fig. 2.40. It can be seen that the converter achieves a peak efficiency of 95% at the rated load. It should be noted that the efficiency at light load can be improved by scaling down the switching frequency, provided that the constraint given in Eq. (2.7) is still satisfied.

For a direct comparison of the output impedance, the second split-phase configuration is used, since it has the same capacitor values as the hard-charging converter. The only difference between this prototype and the hard-charging one is the extra inductor to make the LC filter. The additional inductor incurs an approximately 10% increase in the components volume of the power stage, but the penalty in volume is much less significant when the total enclosed box volume of the



(a) Simulation. (b) Experiment.

Figure 2.39: Capacitor voltage mismatch eliminated with *split-phase* soft-charging operation.

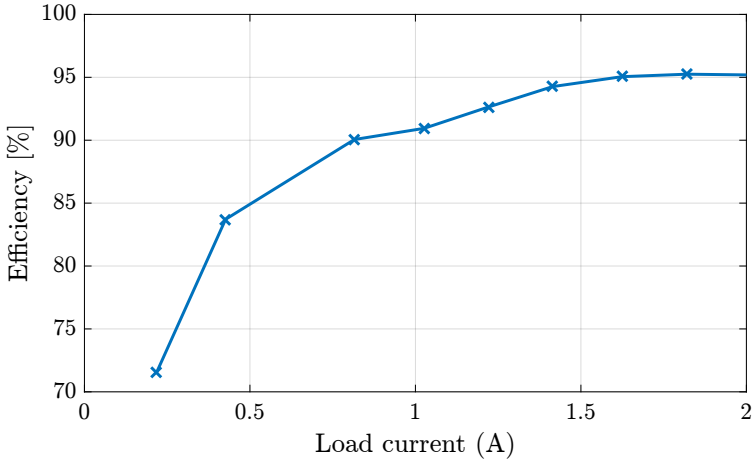


Figure 2.40: Measured efficiency of converter prototype in split-phase operation with soft-charging configuration 1, at $V_{in} = 150$ V.

power stage is considered. The output impedance is plotted against the switching frequency in Fig. 2.41, and is calculated from (2.31) using the measured data. It can be seen that similar to the simulation results, the output impedance in hard-charging operation increases as frequency decreases. Two-phase soft-charging operation reduces the impedance at low switching frequencies while the proposed split-phase operation results in the lowest output impedance. For example, to achieve the same output impedance as the split-phase operation at 100 kHz, the two-phase soft-charging operation requires a switching frequency of approximately 200 kHz while the hard-charging converter has to switch at over 500 kHz. Moreover, it can be seen in Fig. 2.41 that the measured data closely match the simulated values, especially at higher switching frequencies. At lower switching frequencies, the experimental values of all three cases are larger than expected. This can be attributed to the tolerance of the flying capacitor used (up to 20%). Since the split-phase control assumed equal capacitor values for soft-charging operation, different capacitor values will

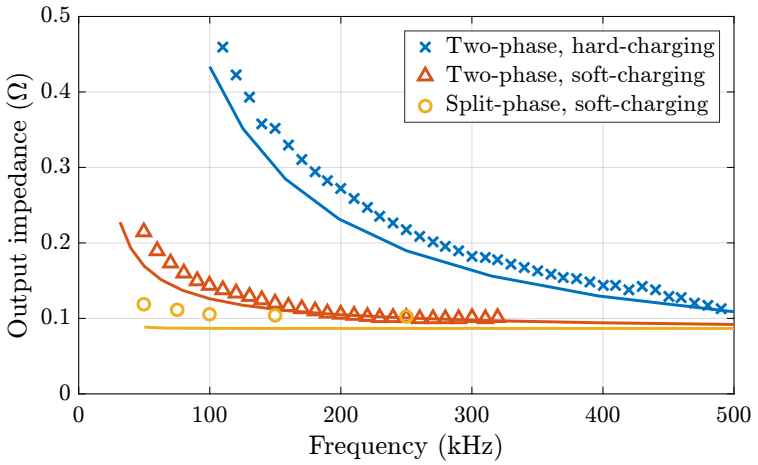


Figure 2.41: Output impedance calculated from measured data. Simulated values are shown as solid lines for reference.

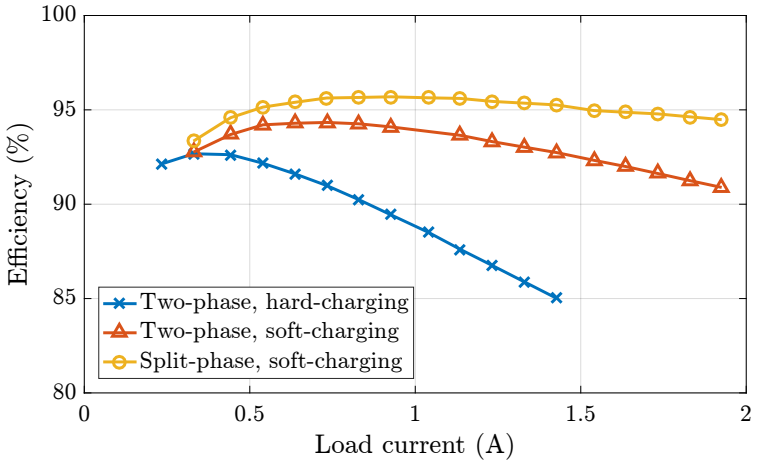


Figure 2.42: Measured efficiency of the Dickson converter in deep SSL region. $V_{in} = 40$ V, $f_{sw} = 100$ kHz.

result in some degree of capacitor charging/discharging loss and are not modeled in the simulation.

In addition, the efficiencies of the converters in the SSL region are compared in Fig. 2.42, using the split-phase configuration 2. It can be seen that soft-charging operation brings significant efficiency improvement while the proposed split-phase control has the highest efficiency. The split-phase soft-charging operation also has the smallest drop in efficiency as the load increases, due to its smallest output impedance. At a load current of 2 A, the split-phase reduces power loss by 30% compared to two-phase soft-charging operation, and by 75% compared to the projected power loss with the hard-charging operation. It should be noted that both the output impedance measurements and the efficiency measurements are obtained using reduced input voltage and output current rather than the rated values. This is to prevent the conventional hard-charging converter from breaking due to the excessive heat when the converter is operating inefficiently with high output impedance

in the SSL region. The hardware results also demonstrated that indeed the split-phase control is effective for a Dickson converter with a conversion ratio that is higher than the analyzed 4-to-1.

2.6 Chapter Summary

In this chapter, the fundamental cause of capacitor charge sharing loss is examined. A soft-charging concept is introduced, which eliminates the charge sharing loss by introducing a current source in the circuit. The elimination of the charge sharing loss reduces the output impedance of SC converters in the SSL region to the same level of the FSL region. An inductor is shown to satisfy the requirement of the current source load. Another requirement for soft-charging is that there is no charge sharing loss internal to the switched-capacitor topology. A general method is proposed, which can be used to analyze an arbitrary SC converter topology and determine whether full soft-charging can be achieved. It is found that among the classic topologies, the series-parallel and Fibonacci converters are able to achieve full soft-charging operation with equal capacitor values. The Dickson converter can only approach soft-charging operation with uneven capacitor values, while the Doubler and ladder converters can only achieve partial soft-charging operation. One approach to achieve soft-charging is explored. Capacitors are selectively charged and discharged so that when switches turn on, no KVL violation happens for the ideal circuit. The technique, named split-phase control, is applied to Dickson converter, and it has been shown that SSL loss can be completely eliminated. Hardware prototypes have been implemented to support the analysis.

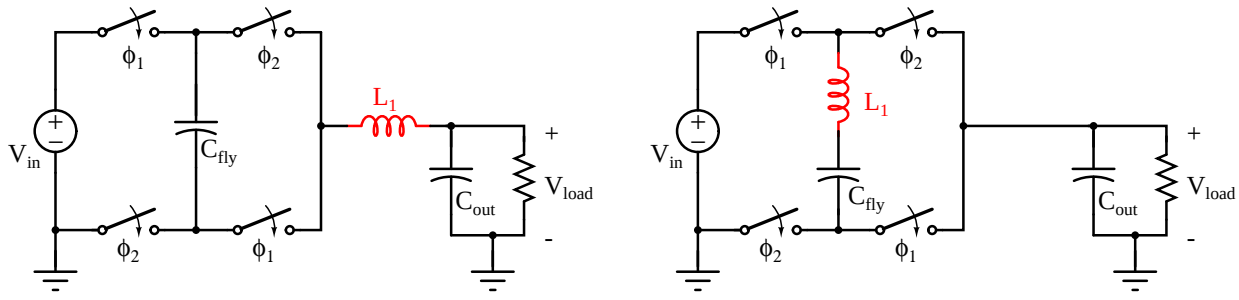
CHAPTER 3

DESIGN AND COMPARISON OF FIXED-RATIO HYBRID CONVERTERS

In the previous chapter, it has been shown that soft-charging (both resonant and non-resonant) operation for the two-phase series-parallel and Fibonacci converter can be achieved with a single inductor at the output node in step-down configurations (input node in step-up configurations). For Dickson converter, split-phase control is introduced to achieve complete soft-charging operation. In this chapter, alternative locations to add inductors to SC topologies, as well as the converter's sensitivity to component tolerance are investigated (Section 3.1). In addition, since the extra inductor introduces an additional design space, the inductor and capacitor values can be selected to achieve the minimal total passive component volume. Such a design process is presented in Section 3.2. Furthermore, different hybrid SC topologies are compared in Section 3.3, based on switch stress and the optimized component volume to reveal the advantages and disadvantages of the respective topologies.

3.1 Soft-charging Operation with Multiple Inductors

Another way to augment SC converters is to add an inductor in series with the flying capacitor (Fig. 3.1b) as opposed to adding one at the output (Fig. 3.1a). For the example 2-to-1 topology shown in Fig. 3.1b, the simulated output impedance is plotted in Fig. 3.2. It can be seen that



(a) 2-to-1 converter with inductor at the output.

(b) 2-to-1 converter with inductor in series with the flying capacitor.

Figure 3.1: Common switched-capacitor converter topologies.

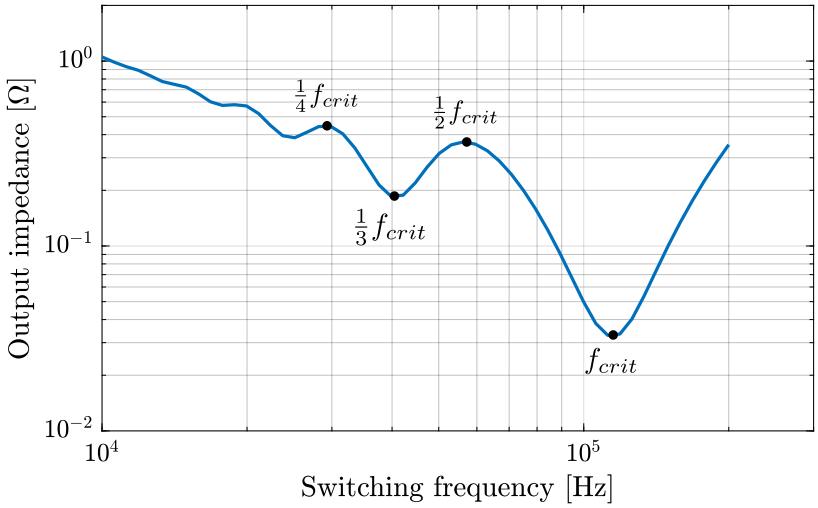


Figure 3.2: Simulated output impedance vs. frequency.

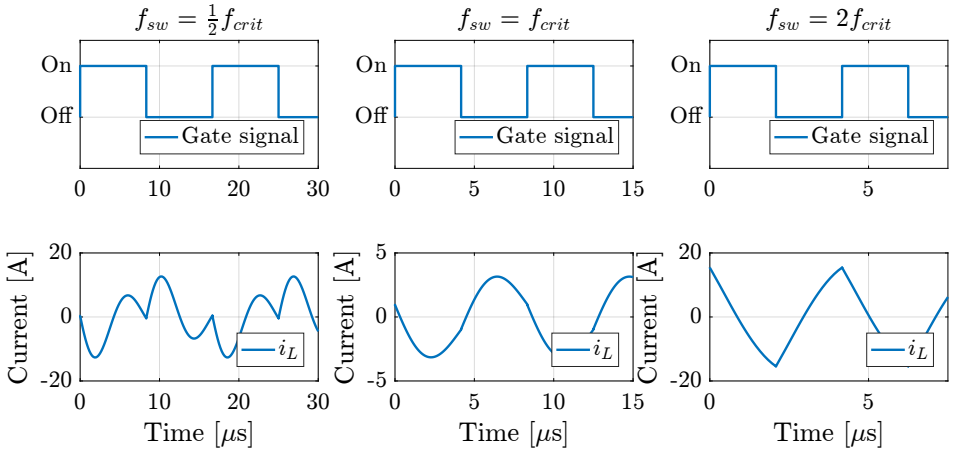


Figure 3.3: Operating waveforms for the hybrid converter in Fig. 3.1b.

for switching frequency that is lower than or equal to the critical frequency, the converter behaves similarly to the plot in Fig. 2.9. However, for switching frequency that is higher than the critical frequency, the impedance increases sharply, in contrast to the flat curve in Fig. 2.9. The inductor current waveforms are shown in Fig. 3.3, together with gate signal indicating the two different circuit states. For the case $f_{sw} = f_{crit}$, the inductor current resembles a full-wave sinusoid, charging the capacitor in one state and discharging the capacitor in the other. For the case $f_{sw} = \frac{1}{2}f_{crit}$, the inductor current becomes a full-wave sinusoid within each state, resulting in a large circulating current and associated power loss. For $f_{sw} > f_{crit}$, the resonant tank becomes inductive, and the current looks like a triangular wave with an approximately 90° phase shift. Again, the current is both positive and negative within one state, resulting in a large conduction loss, and the sharply increasing output impedance. Therefore, the most viable way to operate such a converter is at the resonant frequency of the circuit.

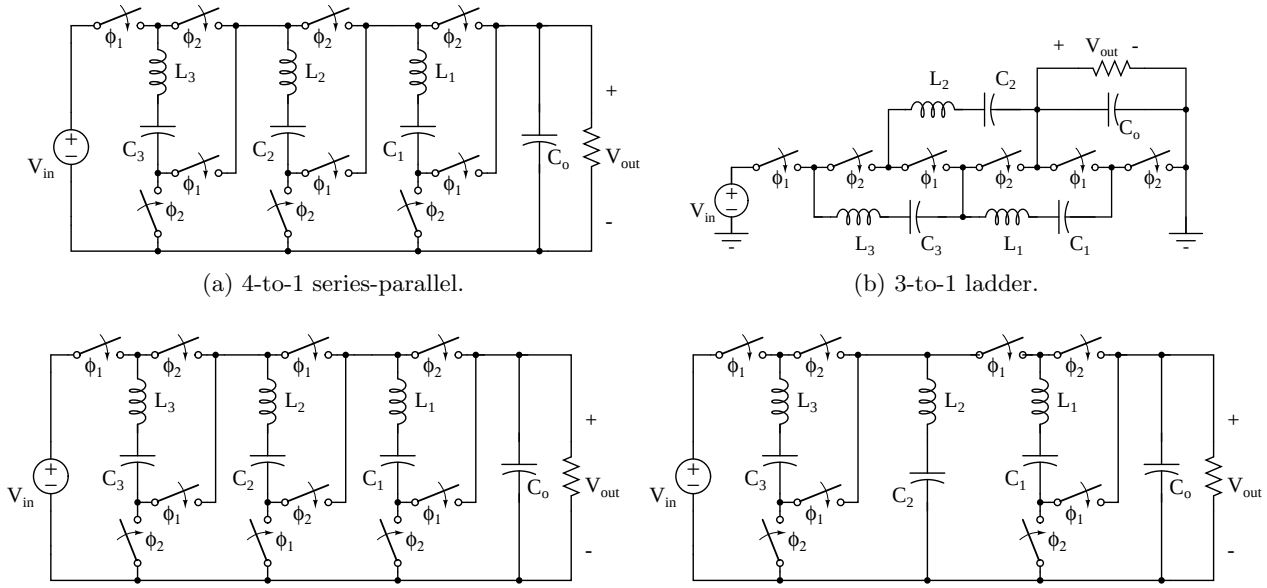
The concept can be extended to all existing SC topologies, by adding an inductor in series to each of the flying capacitors. In this way, each flying capacitor is replaced with an LC resonant tank. The modified versions of the classic topologies are shown in Fig. 3.4, and their corresponding output impedance is plotted in Fig. 3.5. It can be seen that they all have shapes similar to that of the impedance of the basic 2-to-1 topology, and have minimal impedance at the resonant frequency of the circuit, due to the soft-charging operation. The reason why soft-charging operation can be achieved by adding an inductor to all flying capacitors can be understood as follows. Since each switched element is an LC resonant tank, they can be connected either in series or parallel or a combination of these. Regardless of how these elements are connected in each state, the resonant frequency is always $\frac{1}{2\pi\sqrt{LC}}$, provided that all the resonant tanks have the same LC time constant. When operating at the resonant frequency, all the capacitors will be resonantly charged in one state and discharged in the other state, resulting in no charge-redistribution loss.

It should be noted that while the feasibility of soft-charging operation is demonstrated in this section, practical constraints can influence whether the converter can be realized with devices such as MOSFETs. For example, in practice, perfect ZCS cannot always be achieved due to capacitor and inductor tolerance. In this case, the path for the current to flow during the deadtime needs to be investigated, to make sure that the voltages across the switches do not exceed their rating. On the other hand, an advantage of the inductor-in-series approach is that during normal operation, the inductor shields switches from the capacitor voltage ripples, and thus the switch voltage rating is always the nominal voltage, and thus the capacitors are allowed to have a large ripple without increasing the switch stress. Table 3.1 summarizes the two ways to augment inductors in the circuit from different perspectives.

Table 3.1: Inductor placement.

	Inductor at output	Inductor in series
Operating frequency	$f_{\text{sw}} \geq f_{\text{crit}}$	$f_{\text{sw}} = f_{\text{crit}}$
Duty ratio	According to the charge vectors	50%
Applicability	Applicable to selective topologies	Applicable to all SC topologies [1]
Switch ratings	Increased by capacitor voltage ripple	Capacitor voltage ripple shielded by inductor
Regulation capability	Regulation possible	Regulation complicated

It should be noted that these two ways to augment the inductor presented here are two extreme examples. It is possible to find more ways to augment the inductor by placing inductors in series with some, but not all of the flying capacitors. For example, the doubler converter shown in Fig. 2.16d can be seen as a cascade of two basic 2-to-1 structures , if $C_2 \gg C_1$ & C_3. Therefore, hybrid SC converters can be obtained by cascading the structures in either Fig. 3.1a or Fig. 3.1b, giving rise to the topologies in Fig. 3.6a and Fig. 3.6b, respectively. In this work, they are referred to as cascaded doubler or cascaded 3-level converters. Converters obtained in this way require that $C_{\text{mid}} \gg C_1$ & C_2, so that C_{mid} does not take part in the resonant operation. As a result, the volume of C_{mid} could dominate the size of the capacitors, if they have the same energy density. One way to avoid the penalty is to interleave two phases of the cascaded converters and connect



(a) 4-to-1 series-parallel.

(b) 3-to-1 ladder.

(c) 5-to-1 Fibonacci.

(d) 4-to-1 doubler.

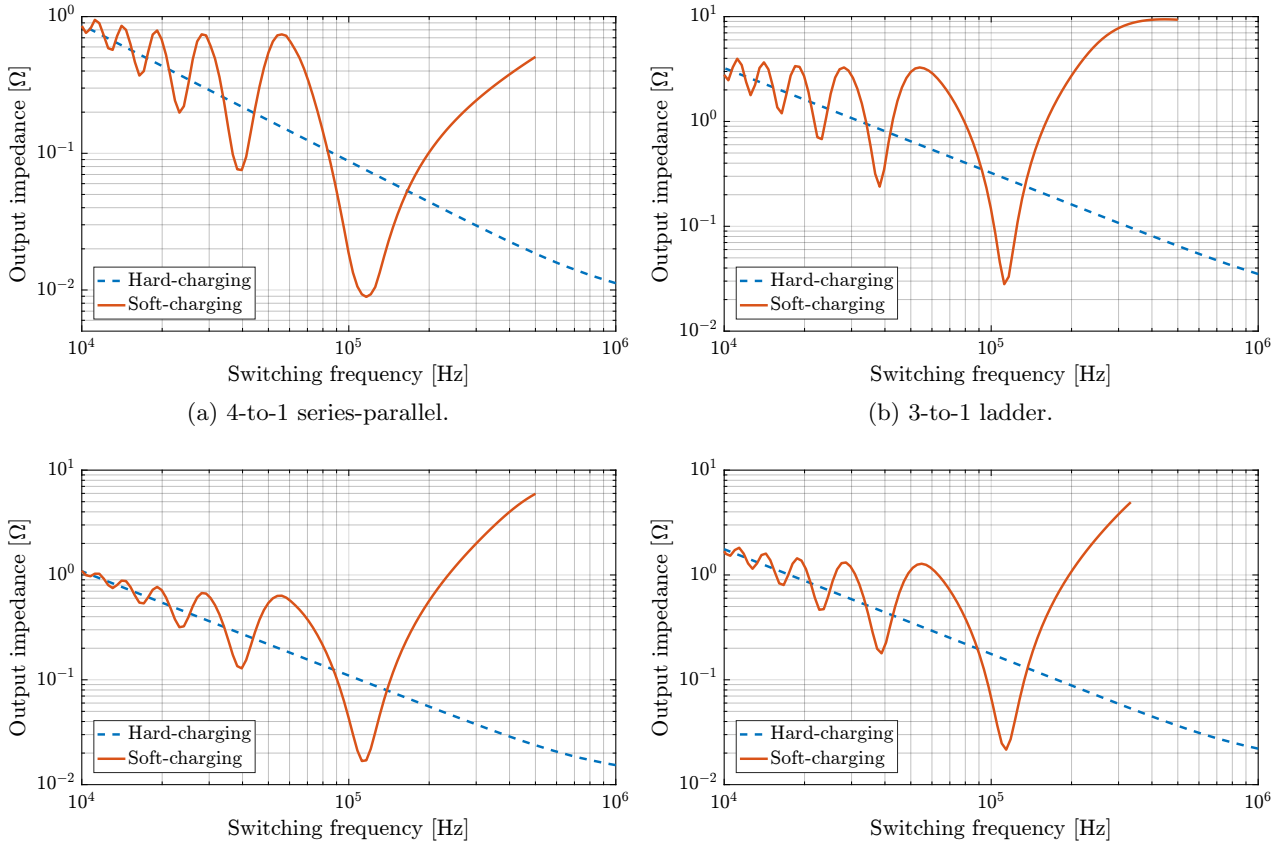
Figure 3.4: Hybrid SC converter topologies obtained by adding an inductor in series to each flying capacitor.

them at the input, middle and output point, and operate them 180° out of phase. This way, both the input filter and C_{mid} can be significant reduced.

Another issue associated with hybrid SC converters is how the output impedance or power loss changes when the capacitor values deviate from the nominal values. Here, the sensitivity of the output impedance with respect to the tolerance of the flying capacitor values is investigated for the series-parallel converter. The different capacitor values used in the simulation are shown in Table 3.2 and the simulated impedance is shown in Fig. 3.7. It can be seen that for both types of inductor placement, there is minimal change in the output impedance for a small variance in capacitor values ($< 20\%$). When the mismatch is severe (50%), the impedance is noticeably higher, due to the increase in charge redistribution loss. The series inductance structure is affected more by the severe capacitor mismatch, due to the steeper slope of the impedance curve. In addition, non-ZCS introduced by the mismatch will introduce additional problems in practical implementation.

Table 3.2: Capacitors values used in simulation.

	C_1	C_2	C_3
Matched capacitors	20 μF	20 μF	20 μF
$\pm$20% mismatch	16 μF	20 μF	24 μF
$\pm$50% mismatch	10 μF	20 μF	30 μF



(a) 4-to-1 series-parallel.

(b) 3-to-1 ladder.

(c) 5-to-1 Fibonacci.

(d) 4-to-1 doubler.

Figure 3.5: Output impedance plots for resonant SC topologies.

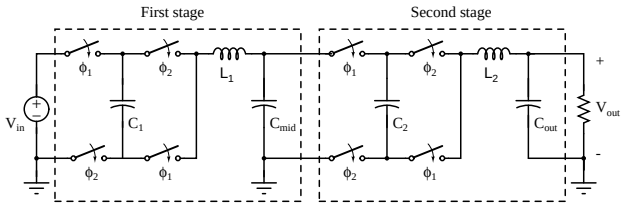
3.2 Inductor and Capacitor Selection

For the soft-charging hybrid SC converters, the minimum frequency with low conduction loss is the resonant frequency of the circuit. As has been mentioned, the added inductor offers an additional design space by allowing the designer to adjust the values of capacitors and inductors to reach a certain resonant frequency, while minimizing the total passive component volume. In this section, the design process is carried out from the energy storage perspective.

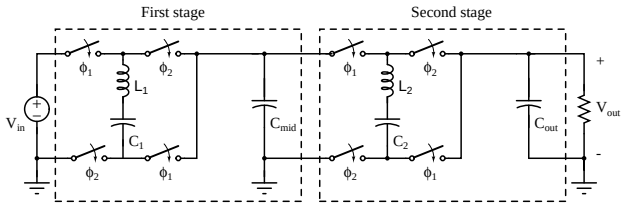
Often, the volume of a passive component is determined by the peak energy it needs to store. Therefore, the passive component volume can be calculated as the peak energy stored by the capacitor (or inductor) divided by the volumetric energy density of the capacitor (or inductor). For a converter with multiple capacitors and inductors, the total passive component volume is given by

$$\mathrm{V}_{\mathrm{tot,hybrid}} = \frac{\frac{1}{2}\sum CV^2}{\rho_{E,C}} + \frac{\frac{1}{2}\sum LI^2}{\rho_{E,L}}, \tag{3.1}$$

assuming that the capacitors have the same energy density $\rho_{E,C}$, and the inductors have the same

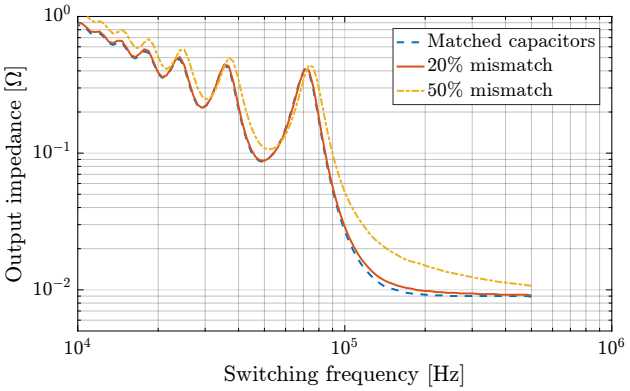


(a) Inductor at the output at each stage.

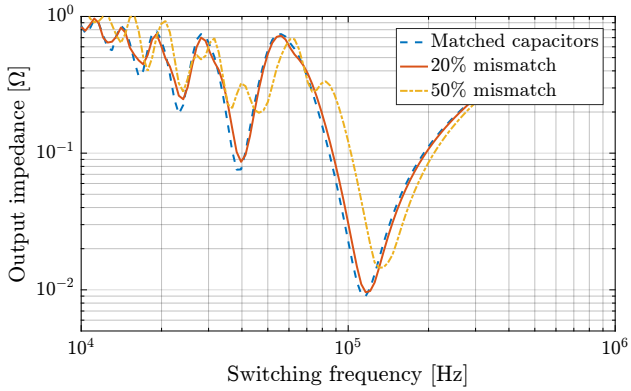


(b) Inductor in series with flying capacitors.

Figure 3.6: Cascaded hybrid doubler topologies.



(a) Inductor at the output.



(b) Inductor in series to capacitor.

Figure 3.7: Output impedance plots for hybrid SC topologies with capacitor mismatch.

energy density $\rho_{E,L}$. Now, the capacitor voltage and the inductor current can be expressed in terms of V_{out} and I_{out}, respectively, giving

$$\mathrm{V}_{\text{tot,hybrid}} = \frac{k_C C V_{\text{out}}^2}{\rho_{E,C}} + \frac{k_L L I_{\text{out}}^2}{\rho_{E,L}}, \tag{3.2}$$

where k_C and k_L are topology dependent parameters, and L and C are the equivalent values to achieve a resonant frequency of f_{sw}. By using Q as the quality factor of the resonant tank given by $\sqrt{\frac{L}{C}}\frac{1}{R_{\text{load}}}$, and $f_{\text{sw}} = \frac{1}{2\pi\sqrt{LC}}$, Eq. (3.2) can be rearranged to form Eq. (3.3).

$$\mathrm{V}_{\text{tot,hybrid}} = \frac{1}{2\pi}\left(\frac{1}{Q}\frac{k_C}{\rho_{E,C}} + Q\frac{k_L}{\rho_{E,L}}\right)\frac{P_{\text{out}}}{f_{\text{sw}}}\,. \tag{3.3}$$

For a given set of P_{out}, f_{sw}, k_C, k_L, $\rho_{E,C}$ and $\rho_{E,L}$, Eq. (3.3) can be differentiated with respect to Q to obtain the quality factor that minimizes the total passive component volume:

$$Q^* = \sqrt{\frac{k_C}{k_L}}\sqrt{\frac{\rho_L}{\rho_C}}\,. \tag{3.4}$$

It can be seen that Q^* only depends only on topology dependent factors (k_C and k_L), and component

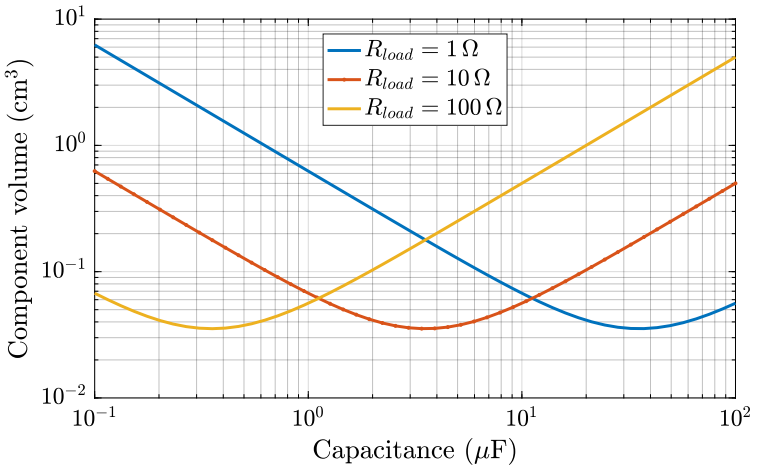


Figure 3.8: Plot of total passive component volume against capacitance value. Parameter values used are: $f_{\text{sw}} = 100$ kHz, $P_{\text{out}} = 100$ W.

energy densities ($\rho_{E,C}$ and $\rho_{E,L}$), and is independent of the output power or switching frequency. From Q^*, and the worst case R_{load}, the optimal inductor and capacitor values can be calculated. Substituting Eq. (3.4) into Eq. (3.3), the minimized volume for a resonant SC converter is then given by

$$\text{V}_{\text{tot,min}} = \frac{1}{\pi}\left(\sqrt{\frac{k_C k_L}{\rho_{E,L}\rho_{E,C}}}\right)\frac{P_{\text{out}}}{f_{\text{sw}}}\,. \tag{3.5}$$

As expected, the total volume is proportional to the output power and inversely proportional to the switching frequency. It also depends on the energy density of the components and how effectively the components are utilized.

The optimization process can be graphically interpreted in Fig. 3.8, where the total component volume is plotted against the capacitance value. Intuitively, since capacitor volume depends on the voltage and inductor current depends on the current, a higher capacitance should be used for applications with low voltage and high current (low R_{load}), while a higher inductance should be used for applications with high voltage and low current (high R_{load}).

3.3 Comparison of Topologies

In this section, the different hybrid converters obtained from Chapter 2 are compared. The inductor-at-output configuration of the hybrid converters is used, since it has the same energy storage requirement as the inductor-in-series configuration. The metrics used are the switch stress and total passive component volume. By assuming the same switching frequency, a lower total switch stress indicates a potentially lower conduction loss, lower switching loss and smaller switch size. The switch stress is defined as the

$$\text{Total switch stress } = \sum_{\text{switches}} V_{ds} I_{ds}, \tag{3.6}$$

where V_{ds} is the voltage rating of the switch, and I_{ds} is the current through the switch. In this work, the rms current through the switch over a complete switching cycle is used. Since one can express V_{ds} using the output voltage ($\beta_v V_{\text{out}}$), and I_{ds} using the output current ($\beta_i I_{\text{out}}$), the normalized switch stress can be defined as

$$\text{Normalized switch stress} = M_s = \frac{\text{total switch stress}}{V_{\text{out}} I_{\text{out}}} = \sum_{\text{switches}} \beta_v \beta_i. \tag{3.7}$$

The total switch stress can be seen as the total switch power rating necessary to deliver a certain power to the output.

The normalized switch stresses of the previously discussed soft-charging resonant topologies at different conversion ratios are shown in Fig. 3.9 in log-linear scale. The switch stress of a buck converter is also included as a reference. It can be seen that the switch stress for the buck converter, the FCML converter and the series-parallel converter increases linearly as the conversion ratio increases, resulting in a high switch power rating for a given output power. The cascaded 3-level converter shows smaller switch stress at higher conversion ratios, while the Dickson converter (with full soft-charging operation) achieves the lowest switch stress and quickly approaches a constant as the conversion ratio increases.

To compare the total passive component volume, the normalized passive component stress is defined as

$$M_p = \frac{\text{total passive component volume}}{\frac{1}{\rho_{E,L}} \frac{P_{\text{out}}}{f_{sw}}}, \tag{3.8}$$

where the denominator is the volume of an inductor needed to store the amount of energy delivered to the load in each switching cycle. Combining with the optimized passive component volume in Eq. (3.5), the normalized passive component stress for hybrid SC converters is given by

$$M_{p,\text{hybrid}} = \frac{1}{\pi} \left(\sqrt{\frac{k_C k_L \rho_{E,L}}{\rho_{E,C}}} \right). \tag{3.9}$$

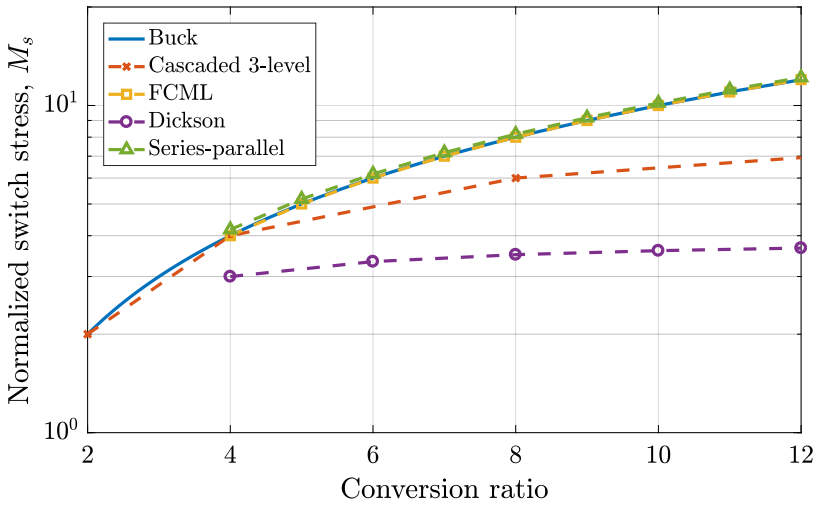


Figure 3.9: Normalized switch stress for various resonant converters. Lower is better.

For the buck converter, k_C in Eq. (3.2) is zero. In addition, it is assumed that the inductor current ripple is twice the average current (i.e. the converter is operating at boundary conduction mode), so that the utilization of the inductor is maximized. Then, the inductor volume for a buck converter can be simplified to

$$\mathrm{V}_{\mathrm{tot,buck}} = \frac{k_L}{\rho_{E,L}} \frac{P_{\mathrm{out}}}{f_{sw}}, \tag{3.10}$$

where $k_L = 2(1-D)$, and D is the duty ratio. Therefore, the normalized passive component volume for a buck converter is simply given by

$$M_{p,\mathrm{buck}} = k_L \,. \tag{3.11}$$

By comparing Eq. (3.9) and Eq. (3.11), it can be seen that in order for the hybrid topologies to achieve a smaller volume, the energy density of the capacitors need to be much higher than that of the inductors (i.e. $\rho_{E,C} \gg \rho_{E,L}$).

The normalized passive component volumes of different topologies are plotted in Fig. 3.10 in log-linear scale, with a $\frac{\rho_{E,C}}{\rho_{E,L}}$ ratio of 80. It can be seen that all of the hybrid converters perform significantly better than the buck converter, especially at small conversion ratios. Among the hybrid converters, series-parallel and the cascaded 3-level have the smallest volume, thanks to the lower voltage stress on the capacitors.

By comparing Fig. 3.9 and Fig. 3.10, it can be observed that in general, resonant topologies that have high switch stress tend to have smaller volume, and vice versa. This allows the designers to choose the topologies based on available switch and passive component technologies. In addition, since for a fixed switching frequency, the switch stress represents the power loss, while the passive component volume reflects the converter size, the performance of these converters also shows another facet of the fundamental efficiency and power density trade-off. In order to directly compare the converter, the overall performance figure of merit (FOM) is obtained by multiplying the switch

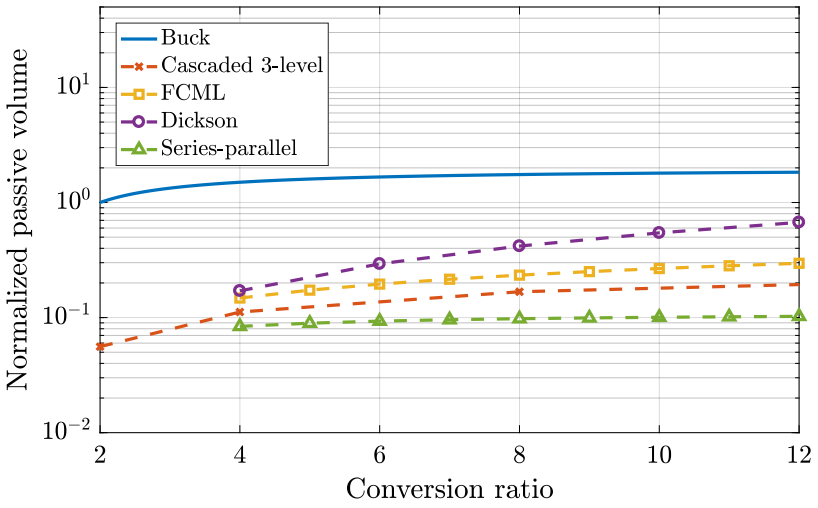


Figure 3.10: Normalized passive component volume for various resonant converters. Lower is better.

stress and the component volume, as given by Eq. (3.12).

$$\text{FOM} = M_s M_p \tag{3.12}$$

It is based on the general trade-off that a converter with smaller switch stress can operate at a higher switching frequency for the same conduction and switching loss, which results in reduction in passive component volume. Therefore, combining both metrics can be indicative of the overall performance potential of the converter. The combined FOM is plotted in Fig. 3.11 in log-linear scale. It shows that all of the hybrid topologies out-perform the buck converter by a wide margin. In a addition, a few interesting results can be learned. It can be seen that both series-parallel and cascaded 3-level converters achieve lower FOM than other hybrid topologies. Despite being a popular SC topology, the series-parallel has not been a widely used SC topology for performance reasons, due to the use of high voltage switches. Yet, by considering both the passive component and switches, it has the lowest FOM, thanks to the low voltage capacitors. Likewise, cascaded converters are usually not favored in the literature, due to the perception that cascading converters results in processing the"power twice". However, by considering the total switch and passive component utilization, cascaded 3-level hybrid converters can be excellent candidates for converters with high efficiency and power density.

It should be noted that the weights of the switch stress and the passive component volume in the overall FOM can be adjusted to reflect characteristics of available technologies, and the final performance for different topologies can be different than what is plotted here. The goal of this section is to establish the method to compare the topologies.

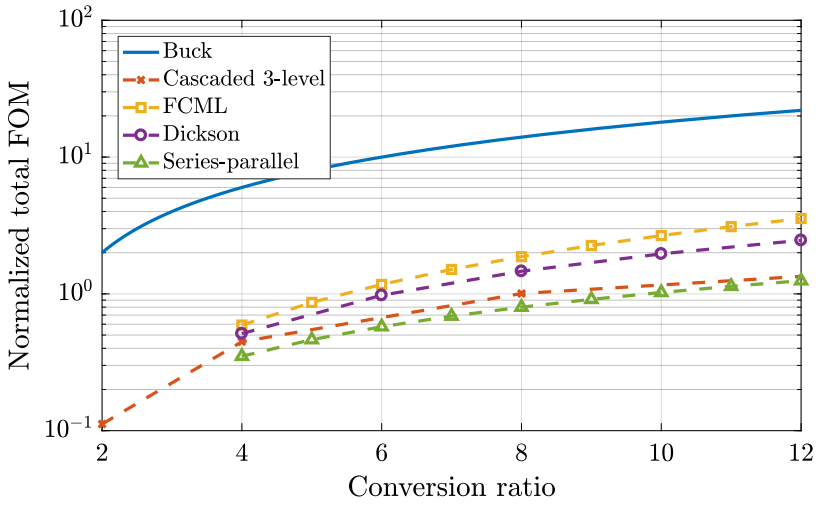


Figure 3.11: Normalized passive component volume for various resonant converters. Lower is better.

3.4 Chapter Summary

In this chapter, alternative inductor placements are first discussed. It is found that by placing an inductor in series to each flying capacitor, complete soft-charging operation can be achieved, if the converter operates at the resonant frequency. However, whether the converter is implementable depends on practical considerations, such as the current direction during the deadtime. It is also found that hybrid converters can tolerate about 20% of component mismatch, without a noticeable increase in power loss. In addition, the optimal capacitor and inductor values to achieve the smallest passive component size are analytically obtained. Various hybrid topologies are compared based on switch stress and the optimized component values. It is found that cascaded 3-level converters and series-parallel converters have a better performance compared to the others.

CHAPTER 4

VOLTAGE REGULATION OF HYBRID SC CONVERTERS

4.1 Motivation

The second well-known drawback of conventional SC converters is their inability to losslessly regulate the output voltage [15,16,36]. The term "lossless regulation" means that the power loss of the converter is not influenced by the voltage regulation, if the circuit elements are assumed to be ideal (i.e., ideal switches, capacitors and inductors). While magnetics-based PWM voltage source converters operate on the concept of lossless regulation, it is not possible for pure SC converters. This is again due to the voltage source characteristic of the capacitors. SC converters can only operate with a fixed conversion ratio determined by the topology. The ideal efficiency of a conventional SC converter while regulating the output voltage is shown in Fig. 4.1. It can be seen that the efficiency decreases linearly as the output voltage is reduced from the nominal value. While the conversion ratio can be changed by re-configuring the topologies dynamically, as shown by the dotted line in the plot, it is difficult to achieve a fine voltage resolution and the utilization of the components can be poor due to the redundancy. There are many attempts to alleviate the regulation problem of the SC converters. Typical usage of conventional converters is to cascade it with a buck or boost converter [37]. The SC stage is responsible for the bulk of the voltage conversion and the buck or boost is responsible for regulation. These conventional two-stage designs use conventional SC converters, which have poor capacitor utilization as discussed in Chapter 2. The merged two-stage design in [21,22] improves the capacitor utilization using the theory shown in Chapter 2, but the feed-forward plus voltage hysteresis control can be complicated. A "MultiTrack" architecture is presented in [38], where a ladder based SC converter is combined with transformers to form a voltage conversion stage of galvanic isolation. A PWM stage with an additional inductor is used in front to achieve voltage regulation.

This chapter approaches the regulation problem with a single stage design, by utilizing the soft-charging inductor and PWM switching technique. Therefore, in contrast to the fixed-ratio operation of the hybrid converter, a family of PWM-based hybrid converter is introduced. It will be shown that proposed hybrid SC converter is able to regulate the output voltage continuously, and can compare favorably against both the conventional SC converters and the buck converters.

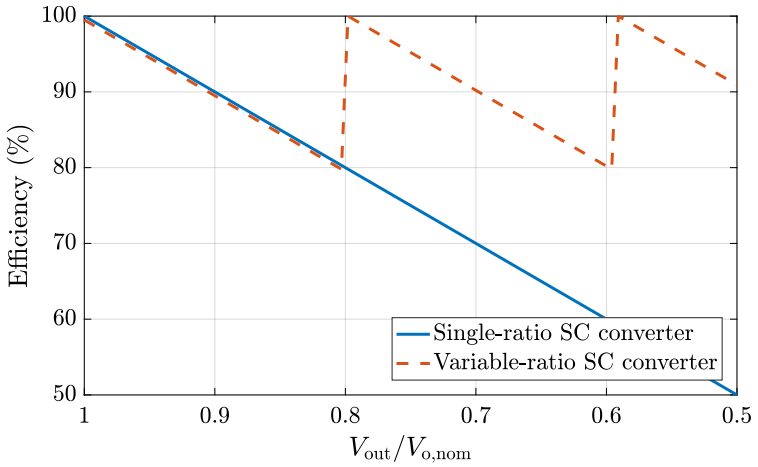


Figure 4.1: Efficiency of conventional SC converter when regulating the output voltage.

4.2 Proposed Method

The proposed technique is illustrated with the hybrid (soft-charging) Dickson converter presented in Chapter 2, whose schematic is repeated here in Fig. 4.2. However, the operating details and component sizing of the two are quite different. Two switching phases responsible for voltage regulation have been introduced. The equivalent circuit states in one complete switching cycle are shown in Fig. 4.3. In order to achieve both split-phase control and PWM regulation, there are six states in total. Phase $1a$ and $2a$ are the original circuit states in the operation of a conventional Dickson SC converter. They determine the native conversion ratio of the converter, which is 4-to-1 for the schematic shown in Fig. 4.2. The reasons for the additional phases are explained as follows.

Phase 3 is the regulation state for voltage regulation. The technique used here is similar to the pulse width modulation (PWM) of a buck converter. By periodic steady-state operation, the average voltage across an inductor is zero. Therefore, the output voltage (defined as the bottom terminal of the inductor in Fig. 4.2) can be reduced by reducing the average switching node voltage (defined as the top terminal of the inductor in Fig. 4.2). Therefore, a regulation circuit state (Phase 3) is created, by shorting the switching node to ground for a certain amount of time during the full switching period. This is accomplished by turning on all the bottom 4 switches (S_1 to S_4) at the same time and keeping all other switches off. Using conventional duty ratio representation, if the total duration of a switching cycle is T and the duration of Phase 3 is $(1-D)T$, then the output voltage is given by

$$V_{out} \approx \frac{DV_{in}}{N}, \tag{4.1}$$

where $N:1$ is the native conversion ratio of the original Dickson converter. In this way, the output voltage can be regulated by adjusting the relative duration of Phase 3 and other phases, i.e., the duty ratio D. It should be noted that the regulation state appears twice in each complete

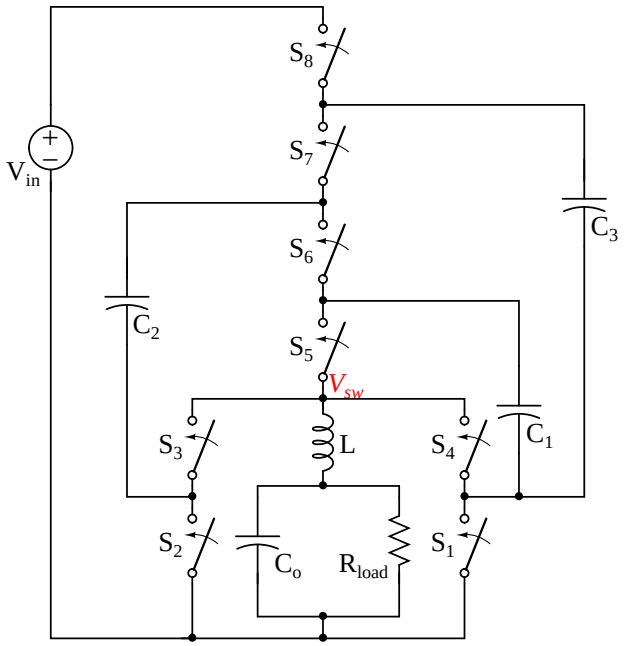
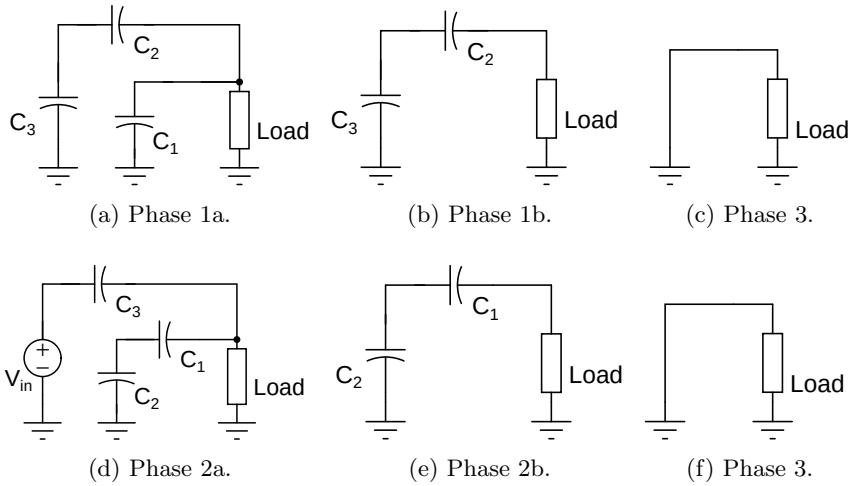


Figure 4.2: Schematic of the proposed regulated soft-charging Dickson converter.

switching cycle, effectively doubling the pulse frequency seen by the inductor, without an increase in transistor switching frequency.

Phase $1b$ and Phase $2b$ are the additional phases introduced by split-phase operation to ensure no voltage mismatch among capacitors during phase transitions. As shown in Section 2.4, with conventional two-phase control, when the circuit transitions between Phase $1a$ and Phase $2a$, some capacitor voltages inevitably add up such that KVL for the ideal circuit is violated [39]. Consequently, large impulse currents circulate through the flying capacitors and create excessive power loss. This can be seen from Fig. 4.4, in which the switching node voltage, inductor current and flying capacitor currents are plotted for conventional two-phase control with PWM regulation. It can be seen that, despite the continuous inductor current, all the capacitor currents have a transient impulse during switch transitions, giving rise to high power loss. To eliminate this undesirable operation mode, Phase $1b$ and Phase $2b$ are introduced to selectively charge and discharge the relevant capacitors through the load. As a result of these buffer states, when the circuit transitions to the original Phase $1a$ and $2a$, KVL is satisfied. The effect of the additional phases is shown in Fig. 4.5, where the same converter is operated with split-phase control. It can be seen that, even when the capacitance is reduced by 10 times compared to the previous case, the impulse current can still be effectively eliminated. To ensure complete soft-charging operation, the ratio of the duration of a phases and b phases is fixed. For a 4-to-1 Dickson converter, the duration of the a phases needs to be three times that of the b phases, as shown in Section 2.4. It should be noted that the introduction of the regulation phase does not change this phase timing, since none of the flying capacitors conduct any current during the regulation phase. Therefore, for complete soft-charging



(a) Phase 1a. (b) Phase 1b. (c) Phase 3.

(d) Phase 2a. (e) Phase 2b. (f) Phase 3.

Figure 4.3: Equivalent circuits in one complete switching cycle.

operation and lossless regulation of the output voltage, the duty cycle of each phase is given by:

- Phase $1a$: $\frac{3}{8}D$ Phase $1b$: $\frac{1}{8}D$
- Phase $2a$: $\frac{3}{8}D$ Phase $2b$: $\frac{1}{8}D$
- Phase 3: $\frac{1}{2}(1-D)$

The gate control signals to achieve the proposed switching scheme are shown in Fig. 4.6. It can be seen that signals q_2, q_{2s} and $\bar{q_2}$ are 180° phase shifted versions of signals q_1, q_{1s} and $\bar{q_1}$. In addition, $\bar{q_1}$ is complementary of q_1 and $\bar{q_2}$ is complementary of q_2. It should be noted that while the control scheme may seem complicated with six gate signals and six circuit states, there is only *one* independent control signal (D), and all other signals can be derived from it. Additionally, each switch still only makes two transitions during one complete switching period, and therefore there is no increase in device switching frequency (and thus switching loss) compared to the conventional operation.

4.3 Design Considerations

In this section, converter design approaches for the hybrid SC converter are discussed, including how to select capacitor values, inductor value and switches.

For soft-charging SC converters without regulation, the inductor is chosen such that the switching frequency, f_{sw}, is equal to or higher than the LC resonant frequency of the converter, in order to

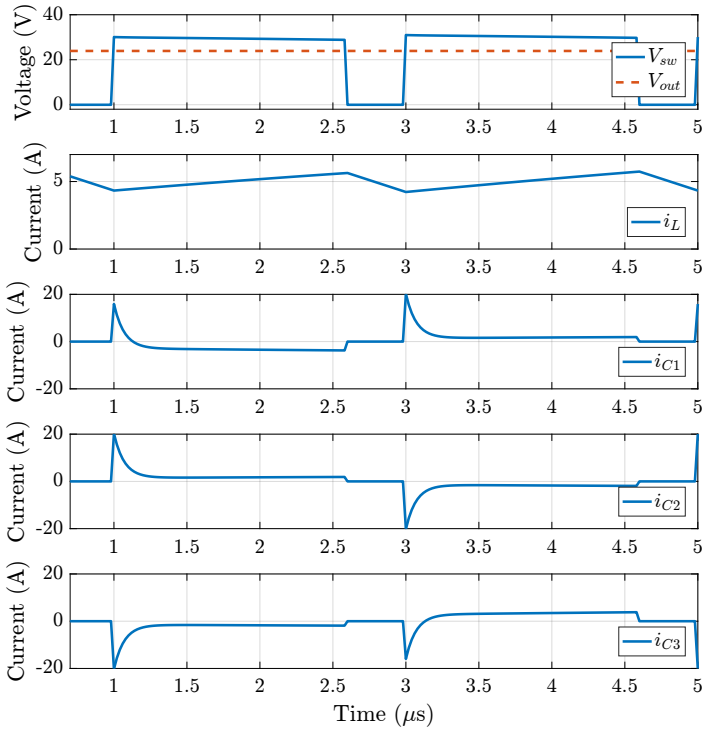


Figure 4.4: Waveforms with *two-phase* regulated operation. $C_1 = C_2 = C_3 = 4.7$ μF, f_{sw} =250 kHz, I_{load}= 5 A.

ensure elimination of the power losses associated with charge sharing [28,40]. For the 4-to-1 Dickson SC converter, this leads to a requirement of

$$f_{sw} \geq \frac{1}{2\pi\sqrt{1.5LC}}, \tag{4.2}$$

assuming each of the flying capacitor has a value of C. In that case, a design should trade off the values of C, L and f_{sw} in order to achieve efficiency and power density targets. However, with the proposed PWM operation, another factor that decides the inductor value and switching frequency is the inductor current ripple. Similar to the design of a buck converter, a reasonably small inductor current ripple is usually desired for efficiency reasons. Thus, using the current ripple as a constraint, the inductor of the hybrid SC converter is given by

$$L_{SC} = \frac{V_{out}(1 - \frac{V_{out}N}{V_{in}})}{2f_{sw,sc}\Delta I_L}, \tag{4.3}$$

where V_{in} is the input voltage, V_{out} is the output voltage, and $N : 1$ is the native conversion ratio. The factor of two in the denominator is due to the fact that the pulse frequency seen by the inductor is twice the switching frequency of the transistors, as discussed in the previous section. For

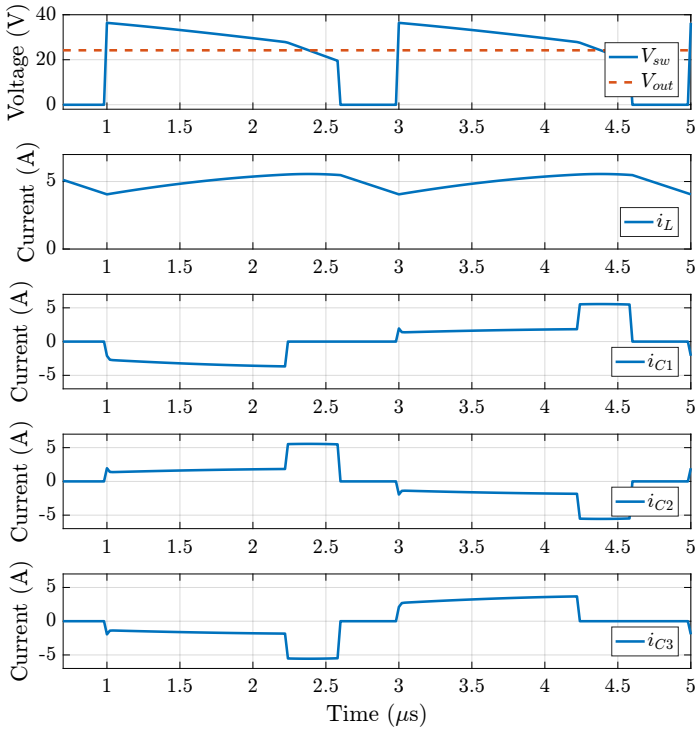


Figure 4.5: Waveforms with *split-phase* regulated operation. $C_1 = C_2 = C_3 = 0.47$ μF, f_{sw} =250 kHz, I_{load}= 5 A.

comparison, the inductor required by a buck converter is given by (5.5), again using the inductor current ripple as a constraint.

$$L_{buck} = \frac{V_{out}(1 - \frac{V_{out}}{V_{in}})}{f_{sw,buck}\Delta I_L} \tag{4.4}$$

By taking the ratios of (4.3) to (5.5), as given by (5.7), the inductance required by the hybrid converter can be normalized by that required by the buck converter.

$$\frac{L_{SC}}{L_{buck}} = \underbrace{\frac{1 - \frac{NV_{out}}{V_{in}}}{1 - \frac{V_{out}}{V_{in}}}}_{K_d} \times \underbrace{\frac{f_{sw,buck}}{2f_{sw,sc}}}_{\frac{1}{2}K_f} \tag{4.5}$$

It can be seen that the first component, K_d, is always less than one, and approaches zero when $\frac{V_{out}}{V_{in}}$ approaches $\frac{1}{N}$. Intuitively, this is due to the fact that the SC stage acts like a "pre-step-down" stage that reduces the input voltage seen by the inductor. The second component, $\frac{1}{2}K_f$, is also less than one in most cases. This is because the SC converter can usually operate at a higher switching frequency than a buck converter, owing to a better device utilization [19]. Therefore, as shown by (5.7), the inductor of the hybrid SC converter is much smaller than that of a buck converter,

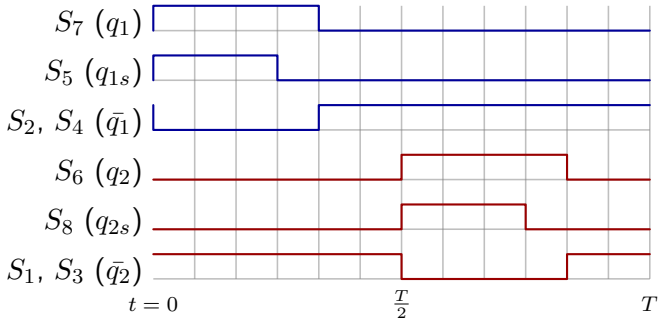


Figure 4.6: Gate signal for regulated split-phase operation of the Dickson converter in one switching period. High represents ON and low represents OFF.

resulting in the superior power density of the hybrid converter.

Table 4.1: Voltage ratings on switches.

Switch	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Voltage rating (assuming no ripple)	$\frac{1}{N}V_{in}$	$\frac{1}{N}V_{in}$	$\frac{1}{N}V_{in}$	$\frac{1}{N}V_{in}$	$\frac{1}{N}V_{in}$	$\frac{2}{N}V_{in}$	$\frac{2}{N}V_{in}$	$\frac{1}{N}V_{in}$
Voltage rating (assuming 10% ripple)	$\frac{1}{N}V_{in}$	$\frac{1}{N}V_{in}$	$\frac{1}{N}V_{in}$	$\frac{1}{N}V_{in}$	$\frac{1.1}{N}V_{in}$	$\frac{2.1}{N}V_{in}$	$\frac{2.1}{N}V_{in}$	$\frac{1.1}{N}V_{in}$

The required capacitor value can be calculated using the amount of charge that flows through the capacitor in a switching cycle (Q_c) and the permissible voltage ripple on the capacitors (ΔV_c). For the 4-to-1 Dickson converter, an approximate expression is given by (6.2), where I_{load} is the load current. The exact values would need methods similar to charge multiplier analysis [12, 28].

$$C_{fly} = \frac{Q_c}{\Delta V_c} = \frac{I_{load}}{3 f_{sw} \Delta V_c}. \tag{4.6}$$

As can be seen, a higher capacitor voltage ripple leads to a lower capacitor value. In conventional SC converters, this voltage ripple gives rise to the capacitor charge redistribution loss, and thus is usually kept very small for high efficiency. On the other hand, soft-charging SC converters can operate with substantially higher ripple without attendant loss increases, and hence their superior power density. Nevertheless, the voltage ripple also adds to the voltage rating of the switches, and thus should be kept reasonable. For example, one can impose a voltage ripple that is, say, 10% of the nominal output voltage, to limit the maximum voltage seen by the transistors.

The conventional Dickson converter has switch ratings that are either $\frac{1}{N}V_{in}$ or $\frac{2}{N}V_{in}$. With the split-phase technique and PWM operation, the proposed converter has the same overall switch ratings as conventional ones. However, as mentioned above, the increased voltage ripples on the capacitors are added onto the rating of the switches. Assuming the capacitor voltage ripple is chosen to be $0.1(\frac{1}{N}V_{in})$, the exact ratings are given in Table 4.1. It can be seen that the increase

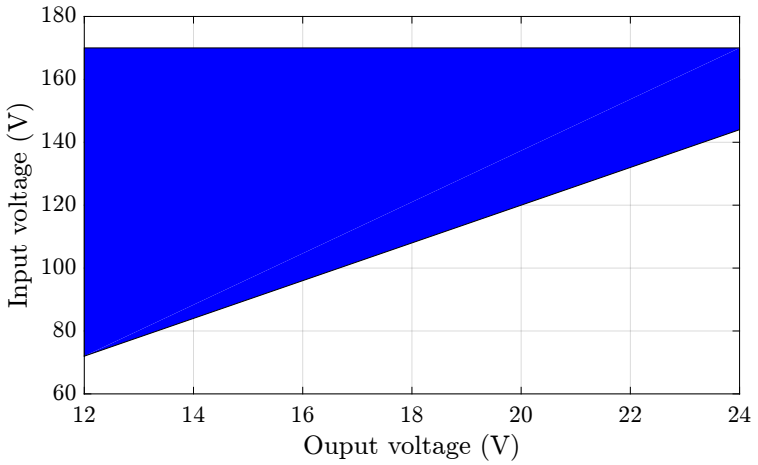


Figure 4.7: Operating range for the designed converter.

Table 4.2: Design specifications.

V_{in}	170 V DC
P_{out}	70 W
V_{out}	12 - 24 V DC
f_{sw}	250 kHz

in switch voltage rating is quite limited using the design guideline presented here.

4.4 Hardware Verification

In order to validate the proposed design, a converter prototype is implemented. The nominal input voltage is 170 V. The converter has a native 6:1 conversion ratio, but supports a wide input and output range by PWM operation. The full operating range achieved is shown in the shaded area of Fig. 4.7. Since the PWM operation can only reduce the output voltage, the lower bound on the input voltage is given by $6V_{out}$. A photograph of the converter is shown in Fig. 4.8, together with a US quarter for scale. All the components are placed on the top side of the PCB. The tallest component is the inductor, which has a thickness of 3.5 mm. Such a thin profile is enabled by the reduction in inductor size owing to the switched-capacitor stage. The design specification is given in Table 4.2 and a component listing is provided in Table 4.3. As can be seen, switches S_1 to S_4 are low voltage and high current devices, while switches S_5 to S_{10} are chosen to have higher voltage and lower current capability, according to the discussion in Section 4.3.

Waveforms of the switching node voltage, output voltage, inductor current and the gate signals are captured and shown in Fig. 4.9. It can be seen that the switching node voltage has the same trapezoidal shape as in simulation. The inductor current is approximately triangular, similar to that of a buck converter.

Table 4.3: Component listing of the converter prototype.

Component	Part number	Parameters
S_4 - S_1	EPC2015	40 V, 4 mΩ, 33 A
S_{10} - S_5	EPC2007	100 V, 30 mΩ, 6 A
D_1, D_2	Toshiba CRS08	
C_5 - C_3	TDK C4532X7T2E105K250KA	250 V, 1.0 μF
C_2, C_1	TDK C2012X7S2A105K125AB	100 V, 1.0 μF
C_o	TDK C3216X5R1V226M160AC	35 V, 22 μF
Inductor	Vishay IHLP-5050CE-01	6.8 μH, 9 A
Gate drivers	TI LM5113	
Level-shifters	Analog Device ADUM5210	
Microcontroller	TI Piccolo F28035	

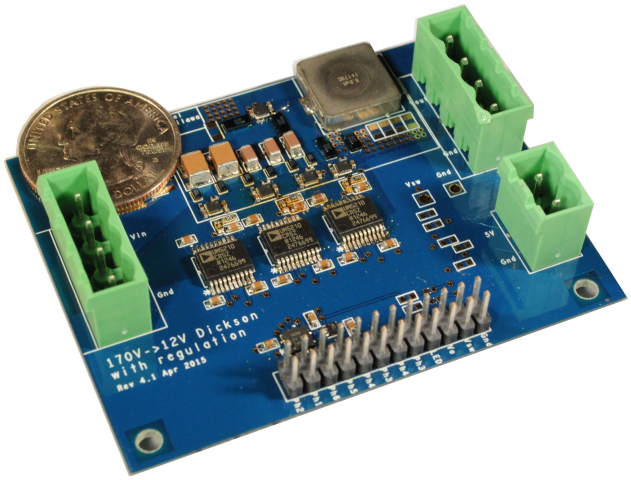


Figure 4.8: Photo of the converter prototype. A US quarter is included for scale.

The efficiency of the prototype with a 12 V constant output voltage is shown in Fig. 4.10a, as the load current and input voltage vary. It can be seen that, at light load, higher input voltage results in a lower efficiency, due to the higher switching loss. At heavy load, the difference in efficiency across input ranges narrows, since the conduction loss starts to dominate. For example, there is a reduction of only 1% in efficiency when the input voltage increases from 85 V to 150 V at 4 A load. Furthermore, even though a few discrete input voltages are given in the plot, the achievable conversion ratios are continuous, thanks to the PWM regulation. This is in contrast to conventional SC converters with one or multiple native conversion ratios, whose high efficiency is only possible at selected conversion ratios.

Similar to a buck converter, during the dead-time of the switches, the switching node voltage can be negative owing to the conduction of body diode. The GaN devices have large equivalent "body diode" voltage drop of approximately 2 V, as can be seen from the negative part of V_{sw} in Fig. 5.4. The efficiency of the converter can be affected at large load current due to high conduction loss during "body diode" conduction. Thus, an anti-parallel diode with a low forward drop voltage is

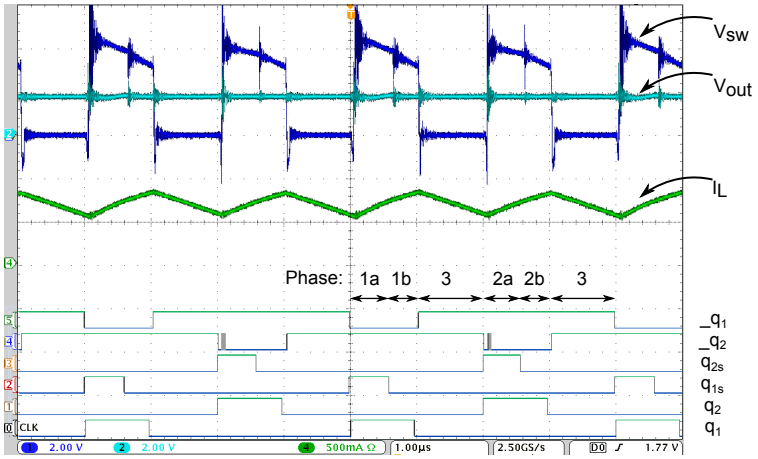
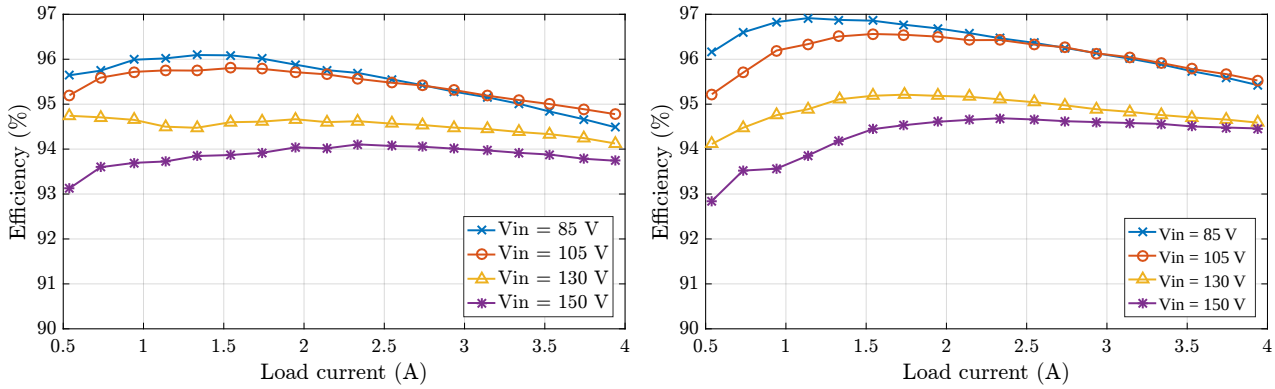


Figure 4.9: Waveforms showing the split-phase PWM operation of the converter prototype.



(a) Without the anti-parallel diodes.

(b) With the anti-parallel diodes.

Figure 4.10: Measured efficiency of the converter prototype with a constant 12 V output.

placed across the switching node and ground. The effect of the diodes on the converter efficiency is illustrated by comparing Fig. 4.10a and Fig. 4.10b. It can be seen that by including the anti-parallel diodes, the peak efficiency is increased from 96% to nearly 97%. The efficiency at full load is also increased by 0.5% for most input ranges.

The efficiency of the converter with 24 V output is shown in Fig. 4.11. It can be seen that the converter efficiency can be maintained at above 96% at 3 A load current and at different input voltages. Furthermore, the efficiency curve is very flat across the load range. This demonstrates the high conversion efficiency possible with the hybrid converter.

For converters with such high power density and compact size, the output power is often limited by thermal constraint. The thermal design becomes difficult due to the extremely small size of the GaN devices. For this prototype, a 3D printed heat sink made of brass is placed on top of the converter to aid the cooling of the GaN switches. Because the highest converter thickness is the inductor, the heat sink is designed such that the overall thickness after mounting on the GaN

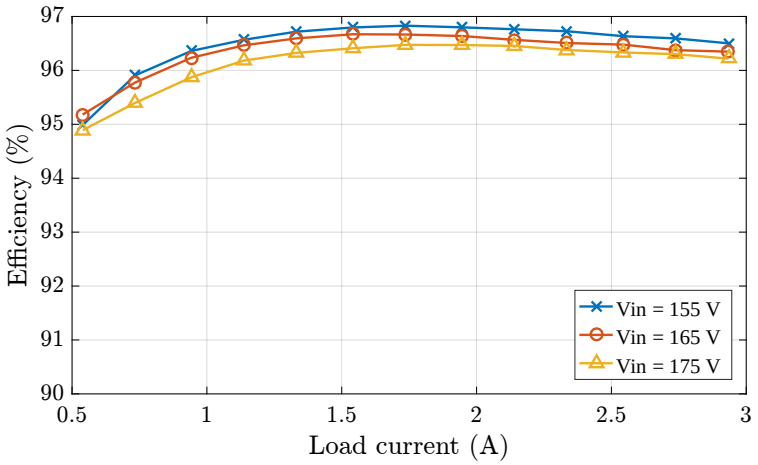


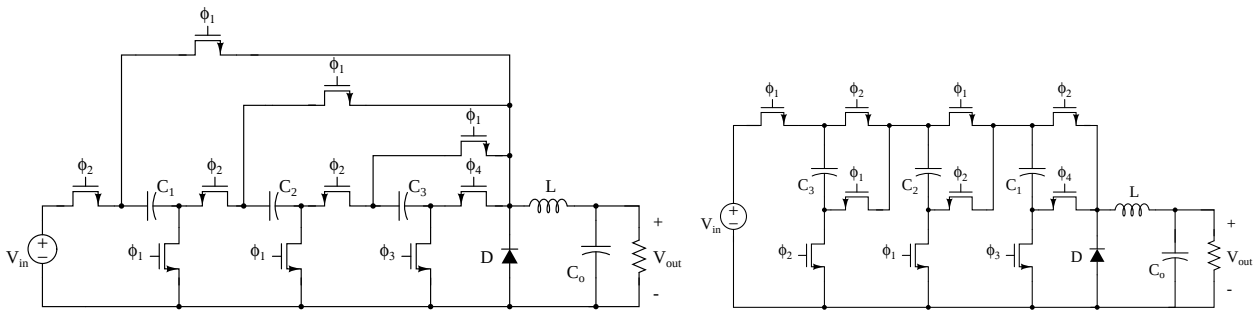
Figure 4.11: Measured efficiency of the converter prototype with a constant 24 V output voltage.

Figure 4.12: Power stage of the converter prototype with the 3D printed heat sink attached. A US penny is on the left for scale.

devices is the same as the inductor, thus making the best use of vertical space. Figure 4.12 shows the heat sink covering the GaN devices. The volume of the converter power stage is 0.254 in^3. It is calculated by taking a rectangular box containing the power stage, including the thickness of the PCB (1.6 mm). The calculation includes all passive and active devices, plus gate drivers, but does not include the level-shifting circuitry and the microcontroller. With a tested power of 70 W, the power density is 276 W/in^3. As demonstrated in this section, the proposed converter is able to simultaneously achieve high efficiency and high power density.

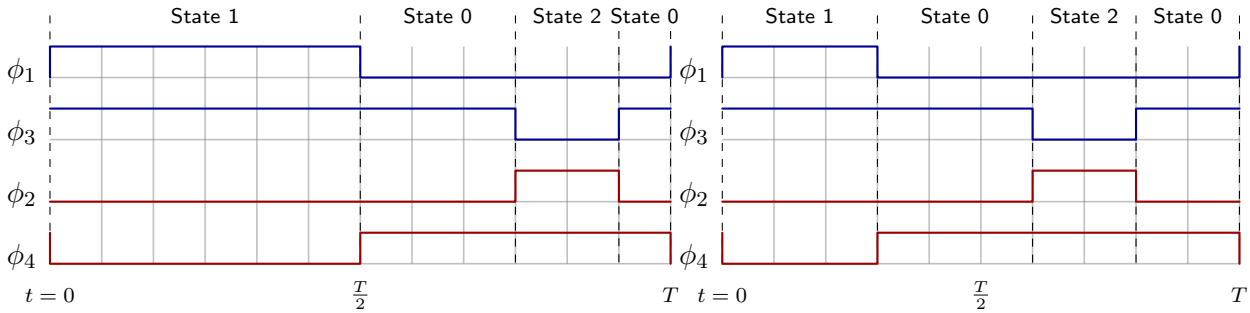
4.5 Extension to Other SC Topologies

The PWM technique presented in this chapter is not limited to the Dickson SC converter alone. In fact, any SC converter that is able to achieve soft-charging operation with an inductor at the output can utilize PWM for regulation. For example, among the traditional SC topologies, it has been shown that series-parallel and Fibonacci converters are able to achieve full soft-charging operation in Chapter 2. A 4-to-1 series-parallel converter and a 5-to-1 Fibonacci converter with the



(a) Series-parallel. (b) Fibonacci.

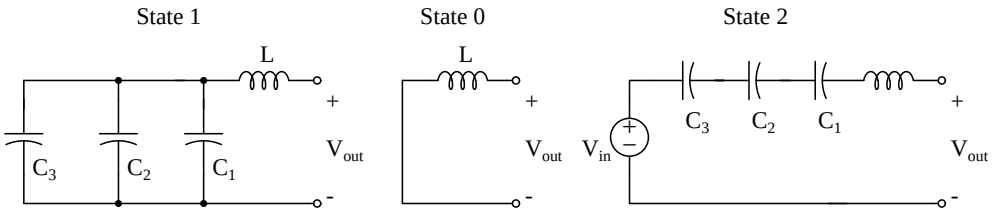
Figure 4.13: PWM hybrid SC converters with gate signals and optional diodes.



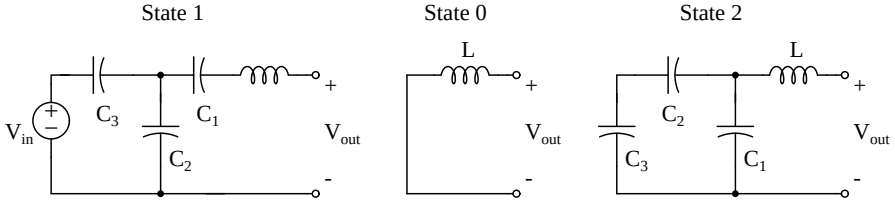
(a) Series-parallel converter with 0.67 PWM duty ratio. (b) Fibonacci converter with 0.5 PWM duty ratio.

Figure 4.14: Gate signals for the PWM hybrid SC converters.

additional inductors are shown in Fig. 4.13, together with optional diodes added to the switching node to improve the efficiency of GaN implementations. Since these converters also have switches that can pull the switching node before the inductor to ground, they can also achieve lossless output voltage regulation using the same PWM technique. The gate signals for the PWM operation are shown in Fig. 4.14, and the equivalent circuits for different states are shown in Fig. 4.15. The circuits shown in Fig. 4.13 are simulated, and waveforms are shown in Fig. 4.16. In order to balance the capacitor voltages in steady state, the durations of the two State 0's are kept the same. This ensures that the average inductor currents in State 1 and State 2 are the same. As shown in Fig. 4.16, the inductor current ripple is smaller for the Fibonacci converter, due to the more even duration of State 1 and State 2.



(a) Series-parallel.

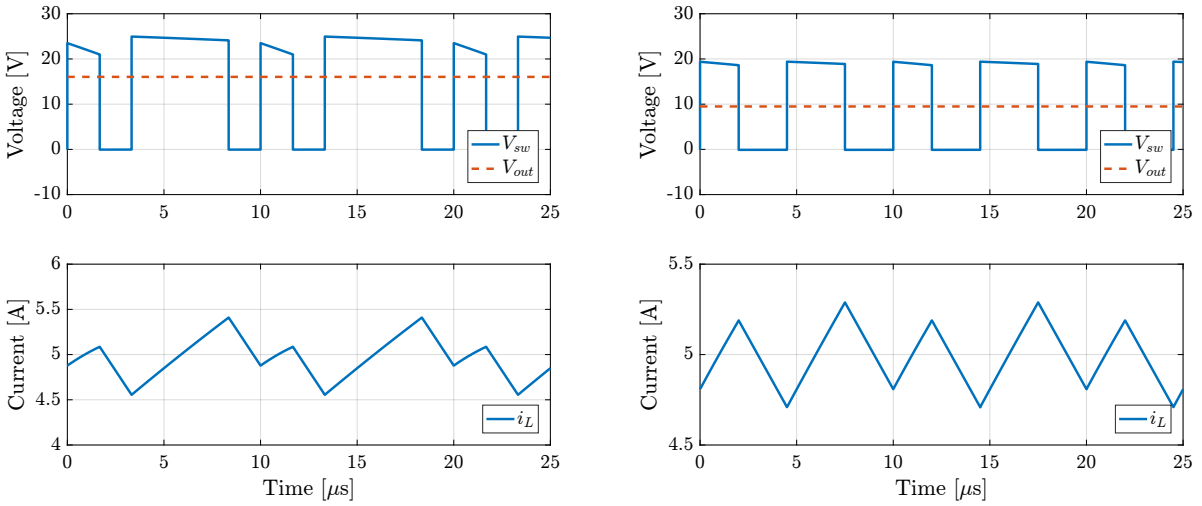


(b) Fibonacci.

Figure 4.15: Equivalent circuits of hybrid SC converters in PWM operation.

4.6 Chapter Summary

In this chapter, a high-efficiency PWM hybrid SC converter is proposed, which is ideal for large step-down/step-up applications. It overcomes the fundamental constraints of conventional SC converters by adding a small inductor. Split-phase control method is implemented to eliminate the charge sharing loss, and PWM regulation technique is utilized to achieve lossless regulation of the output voltage. Design approaches and considerations are presented for such converters. A 170 V to 24 V regulated SC converter with a wide input/output voltage range is implemented to demonstrate the effectiveness of the proposed approach. The converter prototype achieves a peak efficiency of 97% and is able to maintain high efficiency under voltage regulation. The converter prototype simultaneously achieves high efficiency and power density that can be hard to achieve with conventional SC converters or buck converters.



(a) Series-parallel converter with 0.67 PWM duty ratio.

(b) Fibonacci converter with 0.5 PWM duty ratio.

Figure 4.16: Equivalent circuits of hybrid SC converters in PWM operation.

CHAPTER 5

DESIGN AND COMPARISON OF HYBRID SC CONVERTERS

5.1 Motivation

The previous chapter has shown that the hybrid SC converters are able to achieve a higher power density and efficiency compared to conventional SC converters. The addition of the soft-charging inductor significantly improves the energy utilization of the capacitors. In this chapter, it will be shown that, compared to conventional magnetic based converters, the addition of the capacitors also improves the energy utilization of the inductor. A general framework to evaluate different topologies that employ both capacitors and inductors is attempted.

The applications of interest are those involve large voltage step-down/step-up ratios. For instance, 380 V to 12 or 48 V conversions are required to deliver power to servers in data centers. Likewise, in off-line applications, PFC front-ends generate near 400 VDC that is often stepped down to 12–24 V. High step-up boost converters are used to interface PV panels with the grid [41]. At lower voltage levels, microprocessors are powered by voltage regulation modules which convert the 12 V DC bus to 1–1.6 V. In these applications, the magnetic elements typically dominate the size of the converter. Therefore, in order to reduce the overall volumetric footprint, it is desirable to further reduce the inductor size without sacrificing the conversion efficiency.

Flying capacitor multilevel converters (FCMC) have received attention in medium voltage dc-ac applications due to their low device voltage ratings and increased pulse frequency seen by the inductor [42–44]. Recently, it has also been shown that the FCMC converter is able to achieve excellent power density and efficiency at low voltages (e.g., 400 V) [45]. While there has been extensive research on FCMC converters in the dc-ac domain, the use of such converters in dc-dc applications has been relatively limited. A three-level FCMC, also called three-level buck, is used in [46] for envelope tracking power amplifier and shown to be superior to conventional two-level interleaved buck converters. A four-level step-up FCMC for plug-in hybrid electric vehicles is presented in [47], but with only fixed conversion ratios (i.e., no output voltage regulation). A variant of the five-level FCMC is implemented as a bidirectional high voltage dc-dc converter in [48]. Flying capacitors can also be added to multiphase buck converters [49, 50] to reduce the device voltage stress, and a recent implementation shows significant efficiency improvement over conventional buck in high frequency-operation at 3 MHz [51].

Another type of converter that has potential in large step-up/down ratio applications is the

switched-capacitor (SC) converters [18, 52]. It has been shown that the switch utilization in SC converters is higher compared to buck or boost converters [12]. Chapters 2 and 4 have shown that by adding an inductor to SC topologies, the power density can be significantly improved, and lossless regulation can be achieved. However, comparisons against conventional buck converters are non-existent to date.

The hybrid SC converters can be regarded as multilevel converters since there are multiple intermediate voltage domains, generated by the flying capacitors. On the other hand, the FCMC can also be seen as a type of hybrid SC converter, since it combines an SC cell with an inductor. Therefore, these topologies are closely related, and the terms *multilevel SC* and *hybrid SC* refer to both types of converters in this dissertation Due to the use of flying capacitors and multiple switches, a large number of topological variations is possible for the hybrid SC converters, with some better than others. This work presents a quantitative method to compare these hybrid converters, from the perspective of the fundamental utilization of active device and passive devices. In particular, it explores the applications of FCMC converters and hybrid SC converters in dc-dc conversion, with an emphasis on a large voltage conversion ratio. Unlike previous three-level buck analysis [46], a formal comparison method is given, and the volume of the flying capacitors is taken into account. It will be shown that the hybrid SC converters have significantly reduced passive component size compared to buck converters. This work analytically shows the advantages of the multilevel converters and serves as a guide for designing these converters.

This chapter is organized as follows. Section 5.2 outlines the comparison methodology and the motivation and assumption behind. Section 5.3 analyzes the FCMC and compares it against the buck converter using the proposed methodology. Section 5.4 generalizes the methodology to hybrid SC converters and use the Dickson hybrid SC converter as an example. Experimental verification is given in Section 5.5. Finally conclusions are given in Section 5.6.

5.2 Proposed Comparison Methodology

The scope of the comparison is focused on the power stage, which in most cases determines the size and efficiency of a converter. While many additional gate driving and level-shifting circuitries can be required by the multilevel types of converters, their contribution to the size of the circuit can be small when high power applications are considered. On the other hand, in low voltage applications, these auxiliary circuits can be further miniaturized by IC integration.

When comparing topologies, a dilemma often faced is the trade-off between the complexity of the model and the accuracy of the result. Comprehensive loss and size calculations can be carried out, which may yield accurate results, but the resultant expressions are often too complicated to provide any intuitive understanding. On the other hand, simple expressions are easily comprehensible, but the theoretical results may differ significantly from reality. A compromise is struck in this work, with an emphasis on obtaining tractable expressions. The rationale is that converter design is a

multi-dimensional problem, which involves the trade-off between semiconductor conduction loss, semiconductor switching loss, inductor dc and ac loss, inductor volume, capacitor volume, etc. Each of the components (switch, inductor, capacitor) has multiple parameters that influence both the efficiency and size. There are many second-order effects that are not easily captured in equations with reasonable accuracy. An attempt to compare topologies aiming for high accuracy will likely end up designing and optimizing every topology in detail using real components, which involves a considerable amount of work and sacrifices generality and usefulness of the method along the way. Therefore, this work on topology comparison serves as the first pass in identifying the advantageous candidates among the applicable topologies. The merits and demerits of each topology can be easily spotted analytically and intuitively. It should then be followed with design methods such as the Pareto front optimization [53], which can be used to determine the final converter and design choice for an application.

In order to yield comprehensible expressions that allow sensible comparison among topologies, the following assumptions are made.

1. The losses considered are only the conduction and switching losses of the semiconductor switches, as well as the conduction loss in inductors.

2. The volume is calculated based on only the volume of the capacitors and inductors. The volume of the active devices and auxiliary circuits are neglected.

These assumptions are based on the observations that the passive components - the inductors and capacitors - usually dominate the size of a converter. On the other hand, the active switching devices usually dominate the losses in hard-switching converters, especially in continuous conduction mode (CCM) operation where the inductor current ripple is small. While the core loss and ac winding loss of the inductor also can make significant contributions to the power loss, the comparison is valid as long as it does not favor any particular topology by omitting this loss. Ceramic and film capacitors are known to have very small ESR (a few milliohms) in the frequency range of hundreds of kilohertz, and thus the power loss due to the ESR can often be neglected, as is done in this work. These losses should certainly be considered in the later design stage.

Another difficulty in comparing different topologies is that there is a trade-off between the efficiency and size of a converter. As a result, it is not enough just to compare the efficiencies of two converters, without taking into account the size of a converter, and vice versa. In order to carry out a fair comparison among topologies, in this work, the switch and inductor conduction losses are designed to be the same across the topologies, as well as the device switching losses, by choosing the appropriate switch conductance and switching frequency. With these parameters established, the required inductance or capacitance values can be obtained. This results in a single metric (passive components volume) that reflects the performance of the converter. An advantage of the proposed approach is that it is free from the effect of design trade-off for each type of converter. By scaling the design parameters such that the switching loss and conduction loss are the same for all converters, the passive component size becomes the only variable and thus the comparison can

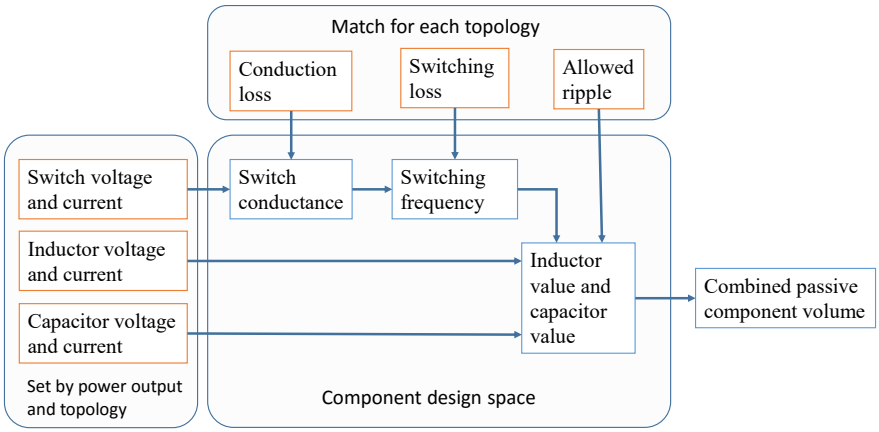


Figure 5.1: Flowchart of the proposed comparison methodology.

focus on the fundamental difference between the topologies. It should be noted here that size and efficiency are the two facets of the fundamental trade-off in converters. The choice in this work is to compare size while keeping efficiency the same, while it is certainly possible to compare the efficiency while keeping the size the same.

Following the preceding rationale, the comparison procedure is proposed as follows.

1. Determine the conductance needed for the switches in order to make the equivalent resistance of each topology the same, so that the conduction losses are the same.

2. Given the conductance and voltage rating of each switch, determine the switching frequency such that the switching losses of all the converters are the same.

3. Determine the inductance required by each topology based on the allowed inductor current ripple, the switching frequency and duty ratio.

4. Determine the capacitance required by the multilevel topologies from the allowed capacitor voltage ripple.

5. Combine the inductance and capacitance into a single passive component volume metric.

An overview of the above procedure is shown as a flowchart in Fig. 5.1. Since the buck converter is the most basic PWM step-down converter, it is used as a reference to which all topologies are compared to.

5.3 Flying Capacitor Multilevel Converters

In this section, the details of the comparison method are presented, using the FCMC converters as examples. The schematic drawing of a five-level FCMC converter is shown in Fig. 5.2. The switching node voltage, V_{sw}, can have five values (V_{in}, $\frac{3}{4}V_{\text{in}}$, $\frac{2}{4}V_{\text{in}}$, $\frac{1}{4}V_{\text{in}}$, and 0), depending on the

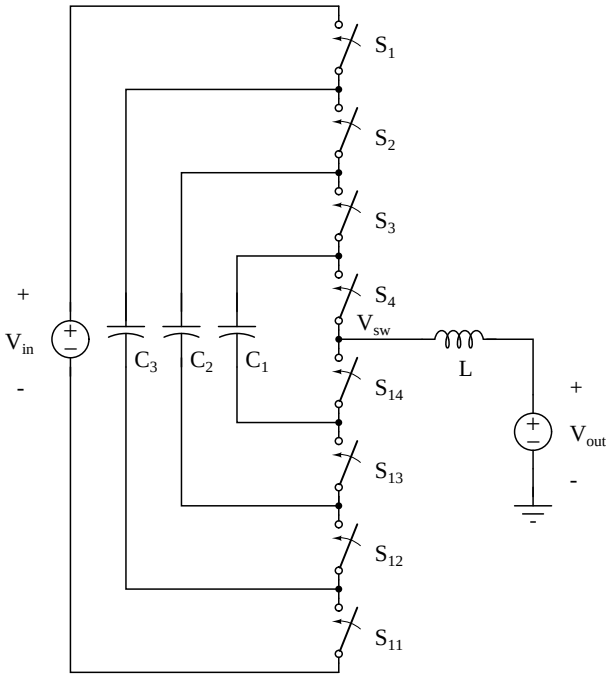
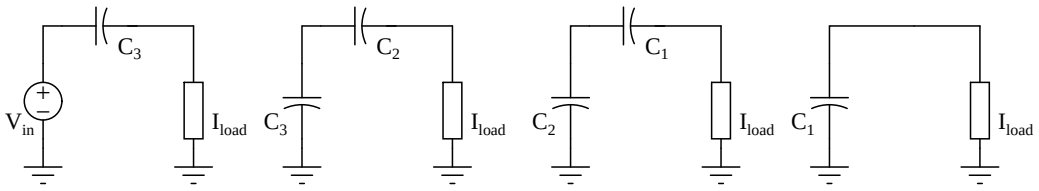


Figure 5.2: Schematic drawing of a five-level flying capacitor multilevel converter.



(a) State 1a. (b) State 1b. (c) State 1c. (d) State 1d.

Figure 5.3: Equivalent circuits for $V_{\text{sw}} = \frac{1}{4}V_{\text{in}}$.

circuit states. For each switching node voltage, there is more than one circuit state that results in the corresponding voltage. In this work, since the FCMC is used in large voltage step-down applications, it is assumed that the desired output voltage is between 0 and $\frac{1}{N-1}V_{\text{in}}$, where N is the number of levels. The corresponding switch states are shown in Table 5.1, where '1' represents on and '0' represents off. The circuit states to achieve a switching node voltage of $\frac{1}{N-1}V_{\text{in}}$ are shown in Fig. 5.3. A typical switching sequence is $1a \rightarrow 0 \rightarrow 1b \rightarrow 0 \rightarrow 1c \rightarrow 0 \rightarrow 1d \rightarrow 0$, and then back to $1a$. By observing Table 5.1 and Fig. 5.3, it can be seen that in one complete switching sequence, all the switches only make one set of transitions, yet four voltage pulses at the switching node are produced. In general, the switching node frequency is $(N-1)$ times the transistor switching frequency, for an N-level FCMC. This is known as the "multiplication" effect of the FCMC converter [42]. In addition, it should also be noted that a buck converter can be viewed as a two-level FCMC, and therefore two-level and buck are used interchangeably in the rest of this dissertation.

Table 5.1: Switch states and capacitor states corresponding to switching node voltages of $\frac{V_{\text{in}}}{N-1}$ and 0. For switches, "1" denotes on-state and "0" denotes off-state. For capacitors, "+" denotes charging state and "-" denotes discharging state.

State	V_{sw}	S_1	S_2	S_3	S_4	S_{11}	S_{12}	S_{13}	S_{14}	C_1	C_2	C_3
1a	$V_{\text{in}}/(N-1)$	1	0	0	0	0	1	1	1			+
1b	$V_{\text{in}}/(N-1)$	0	1	0	0	1	0	1	1		+	-
1c	$V_{\text{in}}/(N-1)$	0	0	1	0	1	1	0	1	+	-	
1d	$V_{\text{in}}/(N-1)$	0	0	0	1	1	1	1	0	-		
0	0	0	0	0	0	1	1	1	1			

5.3.1 Conduction loss

Following the comparison procedure proposed in Section 5.2, the first step is to make the conduction losses of the converters the same, by selecting the conductance of the switches. Since the switch pairs (S_x and S_{1x}) in Fig. 5.2 operate in a complimentary fashion, for an N-level FCMC, there are always $(N-1)$ switches that are closed and connected in series with the load. On the other hand, a buck converter (for which $N = 2$) always has one switch conducting the load current. Thus, if the conductance of the switches of a buck converter is G_{buck}, the switch conductance of an N-level FCMC, G_{FCMC}, needs to satisfy Eq. (5.1), in order to result in the same conduction loss.

$$\frac{G_{\text{FCMC}}}{G_{\text{buck}}} = N - 1. \tag{5.1}$$

It should be noted that the calculation assumes that all the switches in a converter have the same conductance. While in practice, the low side switch of the buck converter is usually chosen to have a higher conductance than the high side switch to maximize the efficiency in a large voltage step-down scenario, the same optimization can be performed on the multilevel converters, and would yield a similar benefit in terms of efficiency improvement. In general, for each different topology, the switches can be optimized so that their conductance corresponds to the RMS current through them. For simplicity, this asymmetric switch sizing is omitted from the examples used here, but can be easily included if desired.

5.3.2 Switching loss

The next step is to make the switching losses the same by choosing the switching frequency, based on previously selected switching conductance and the switch voltage ratings. Assuming the same switch technology, the switch size as well as the switching loss are often approximately proportional to the GV^2 product of the switch, where G is the conductance and V is the blocking voltage of the switch [12]. A justification for the use of the GV^2 product is provided in Appendix C.1, which presents an empirical analysis of GaN transistors that support this particular device scaling

parameter. Moreover, it is recognized here that other metrics can be used in place to represent the switching loss, in order to reflect the scaling or limitation of a particular switch technology.

In order to achieve the same switching losses for the buck converter and FCMC converter, Eq. (5.2) needs to be satisfied.

$$\sum_{\text{switches}} (GV^2)_{\text{FCMC}} \times f_{\text{FCMC}} = \sum_{\text{switches}} (GV^2)_{\text{buck}} \times f_{\text{buck}} \tag{5.2}$$

The FCMC converter has $2(N-1)$ switches, each with a voltage rating of $\frac{1}{N-1}V_{\text{in}}$, while the buck converter has two switches, each with a rating of V_{in}. Rearranging Eq. (5.2) and substituting in Eq. (5.1), the sums of the GV^2 products for the two converters are obtained in Eq. (5.3).

$$\begin{aligned} \frac{\sum(GV^2)_{\text{FCMC}}}{\sum(GV^2)_{\text{buck}}} &= \frac{G_{\text{FCMC}}}{G_{\text{buck}}} \times \frac{2(N-1) \times (\frac{1}{N-1}V_{\text{in}})^2}{2 \times V_{\text{in}}^2} \\ &= 1. \end{aligned} \tag{5.3}$$

As can be seen, the sum of the GV^2 turns out to be the same for both converters. This means that the FCMC converters can switch at the same transistor switching frequency as the buck converter for the same conduction loss and switching loss:

$$f_{\text{FCMC}} = f_{\text{buck}}. \tag{5.4}$$

In existing literature, the advantage of the FCMC is often stated to be reduced inductor current ripple compared to a buck converter, while it is implicitly assumed that the switching frequency is the same as that of the buck converter. The above analysis provides a basis for such an assumption.

5.3.3 Inductor

For efficiency reasons, the inductance value of PWM converters is usually chosen based on a certain inductor current ripple: a larger ripple allows for a smaller inductance, but results in higher ac conduction loss and magnetic core loss. The inductor current ripple in turn depends on the terminal voltages the inductor experiences during a switching cycle. As an illustration, the switching node voltages of a 2-level converter and a 5-level converter are shown in Fig. 5.4, for the case of 100 V to 12 V conversion. Using periodic steady-state constraint, the inductor value of a buck converter is given by

$$L_{\text{buck}} = \frac{(1 - \frac{V_{\text{out}}}{V_{\text{in}}})V_{\text{out}}}{\Delta I_L f_{\text{buck}}}, \tag{5.5}$$

where ΔI_L is the peak-to-peak inductor current ripple.

For the FCMC, the required inductance can be calculated in the same way. For large-step-down

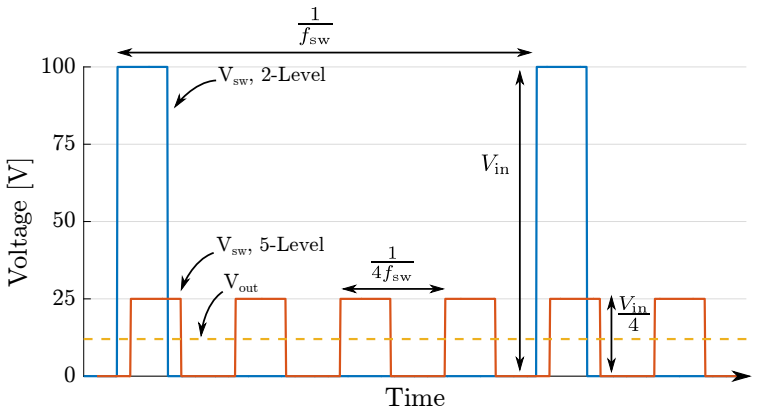


Figure 5.4: Switching node voltages (V_{sw}) and the output voltage of a 2-level and 5-level converter for 100 V to 12 V conversion.

voltage conversion ratios that satisfy $\frac{V_{\text{in}}}{V_{\text{out}}} > N-1$, the inductance is given by

$$L_{\text{FCMC}} = \frac{(1 - \frac{V_{\text{out}}(N-1)}{V_{\text{in}}})V_{\text{out}}}{\Delta I_L f_{\text{FCMC}}(N-1)}, \tag{5.6}$$

for a specified inductor current ripple, ΔI_L. As a quick check, the inductance required by the buck converter can be obtained by setting N to 2. By taking the ratio of Eq. (5.6) and Eq. (5.5), the inductance of the FCMC normalized by the inductance of the buck converter can be obtained as:

$$\frac{L_{\text{FCMC}}}{L_{\text{buck}}} = \underbrace{\frac{(1 - \frac{V_{\text{out}}(N-1)}{V_{\text{in}}})}{1 - \frac{V_{\text{out}}}{V_{\text{in}}}}}_{K_d} \underbrace{\frac{1}{N-1}}_{K_f}. \tag{5.7}$$

It can be seen that the reduction in inductor size compared to the buck converter comes from two terms. The term K_d is due to the difference in the duty ratio of the voltage pulse seen by the inductor. The duty ratio of the switching node pulse of the FCMC is $N-1$ higher due to the step-down from the flying capacitors. The second term, K_f, is due to the fact that for the FCMC, the pulse frequency seen by the inductor is $(N-1)$ times the switching frequency of each switch. To visualize the difference in the required inductance, Eq. (5.7) is plotted in Fig. 5.5, in which each curve is for an FCMC with a different number of levels. It can be seen that, as the conversion ratio, $V_{\text{in}}/V_{\text{out}}$, approaches that of the native conversion ratio of the FCMC, $(N-1)$, the inductance required goes to zero, contributed by the term, K_d. This is due to the near unity duty ratio of the switching node pulse seen by the inductor. On the other hand, as the conversion ratio increases, the effect of K_d becomes smaller, and the normalized inductance approaches a constant for each level, which is determined by K_f. Overall, the inductance required can be significantly reduced by employing the FCMC, especially if the number of levels is designed to be close to the targeted voltage conversion ratio.

The energy stored by the inductor is also calculated. Using Eq. (5.6) and using the parameter α_I to represent the ripple factor ($\Delta I_L = \alpha_I I_{\text{load}}$), the energy stored by the inductor is

$$\begin{aligned} E_{L,\text{FCMC}} &= \frac{1}{2} L_{\text{FCMC}} I_L^2 \\ &= \frac{1}{2}(1 - \frac{V_{\text{out}}(N-1)}{V_{\text{in}}}) \frac{P_{\text{out}}}{\alpha_I (N-1) f_{\text{FCMC}}}. \end{aligned} \tag{5.8}$$

Since the buck converter and the FCMC have the same inductor current magnitude, the ratio of the inductor energy is the same as inductor value:

$$\frac{E_{L,\text{FCMC}}}{E_{L,\text{buck}}} = \frac{L_{\text{FCMC}}}{L_{\text{buck}}} \tag{5.9}$$

The dc conduction losses of the inductors for the FCMC and buck converter are made the same by choosing the same dc resistance for the inductors, since they have the same RMS current. It should be noted that core loss and ac loss are neglected in this analysis. In reality when core loss and ac loss are significant, the multilevel converter losses may differ somewhat, due to the increase in frequency by a factor of $(N-1)$. Appendix C.4 investigates in detail how the core loss changes according to the inductor size and frequency scaling, and can be augmented to the main procedure if desired. In addition, while the presented method fixes conduction and switching losses, and uses the passive component volume as the comparison metric, it is by no means the only performance metric that the FCMC should be designed for. For example, the FCMC converter can be designed to have the same inductor volume and inductor loss with a lower switching frequency than the buck converter, and thus benefit from an overall higher efficiency. Therefore, the fundamental advantages of the FCMC converter are not exaggerated by excluding the ac related losses in the inductor, though the design space may be more limited.

5.3.4 Flying capacitors

The low voltage switch and small inductance are enabled by the multiple voltage levels provided by the flying capacitors. As the number of levels increases, the volume of the flying capacitors increases, and needs to be taken into account. For a multilevel converter, the energy stored by all flying capacitors can be calculated as

$$E_C = \frac{1}{2} \sum_i^m C_i V_{C,i}^2 \,, \tag{5.10}$$

where C_i is the capacitance, $V_{C,i}$ is the voltage rating of the i-th capacitor, and m is the total number of capacitors. For the FCMC converter, there are $N-2$ flying capacitors, and their voltage ratings are given by

$$V_{C,i} = \frac{i}{N-1} V_{\text{in}} \,, \tag{5.11}$$

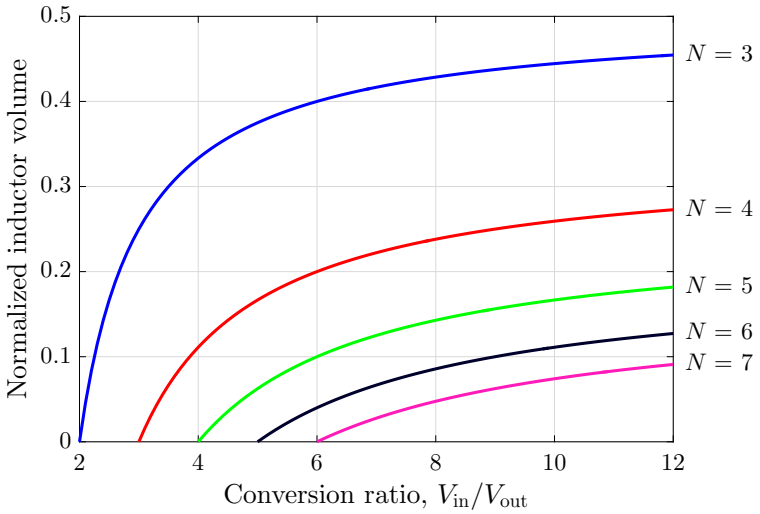


Figure 5.5: Inductance required by the FCMC normalized by that required by two-level buck. N is number of levels.

for the i-th capacitor as labeled in Fig. 5.2. With the typical design choice of having equal flying capacitors ($C_i = C_1$), the total energy stored can be obtained by substituting Eq. (5.11) into Eq. (5.10):

$$E_C = \frac{(N-2)(2N-3)}{12(N-1)} C_1 V_{\text{in}}^2. \tag{5.12}$$

The next step is to determine the capacitor value, C_1. While the capacitors have much higher energy density than inductors, it is important that the energy is utilized in the conversion process. The energy utilization of the capacitor is proportional to the voltage ripple across it. Therefore, analogous to sizing the inductor using inductor current ripple, the flying capacitor value can be obtained from the capacitor voltage ripple constraint. The flying capacitor voltages in a switching cycle are shown in Fig. 5.6. A larger voltage ripple allows for smaller capacitor values, but also adds to the maximum voltage rating of capacitors and switches. In this work, capacitor voltage ripple is chosen as a fraction of the smallest capacitor voltage rating or the smallest switch voltage rating. Thus, for the FCMC converter, the allowed peak-to-peak capacitor voltage ripple is given by

$$\Delta V_C = \alpha_V \frac{V_{\text{in}}}{N-1}, \tag{5.13}$$

where α_V is a relative ripple factor and is less than 1. Then, the capacitance required can be calculated as

$$C_1 = \frac{\Delta Q_C}{\Delta V_C} = \frac{(N-1) I_{\text{load}}\, t_c}{\alpha_V V_{\text{in}}}, \tag{5.14}$$

where ΔQ_C is the charge flowing into the capacitor in a charging period, I_{load} is the load current and t_c is the duration of one capacitor charging period before it gets discharged, as annotated in Fig. 5.6. From Fig. 5.3 and Fig. 5.6, it can be observed that each flying capacitor is only charged in one particular state and discharged in another state. The duration of each state 1 in Fig. 5.3 is

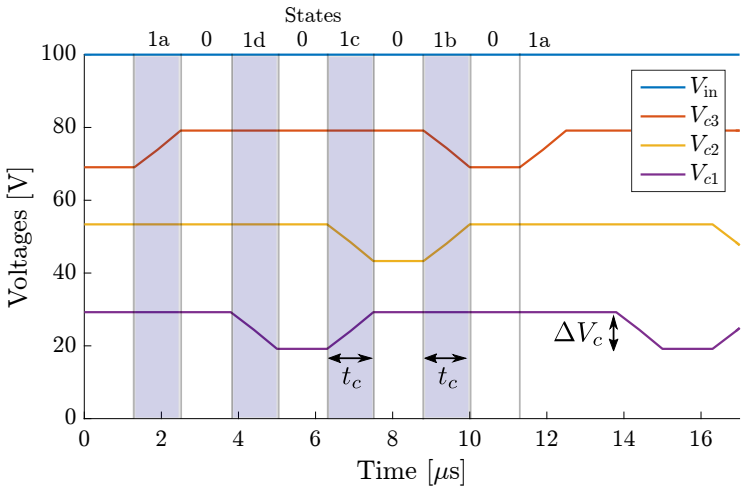


Figure 5.6: Flying capacitor voltages for 100 V to 12 V conversion.

proportional to the duty ratio and inversely proportional to the switching frequency, as given by

$$t_c = \frac{\frac{(N-1)V_{\text{out}}}{V_{\text{in}}}}{(N-1)f_{\text{FCMC}}}\,. \tag{5.15}$$

Thus, substituting Eq. (5.15) into Eq. (5.14) and simplifying, the required capacitance is obtained:

$$C_1 = \frac{(N-1)V_{\text{out}}I_{\text{load}}}{\alpha_V V_{\text{in}}^2 f_{\text{FCMC}}}\,. \tag{5.16}$$

Substituting Eq. (5.16) into Eq. (5.12) and simplifying, we obtain the energy storage of the capacitors:

$$E_C = \frac{(N-2)(2N-3)}{12}\frac{P_{\text{out}}}{\alpha_V f_{\text{FCMC}}}\,. \tag{5.17}$$

It can be seen that the energy stored by the capacitors increases by the square of the number of levels for FCMC converter.

5.3.5 Combined comparison metric

In this section, the combined volume of passive components is investigated. It is assumed that the inductor volume is proportional to the energy stored ($\frac{1}{2}LI^2$), where L is the inductance, and I is the rated (by saturation or thermal limit) current of the inductor. On the other hand, the volume of capacitors is proportional to the energy stored ($\frac{1}{2}CV^2$) by the capacitor, where C is the capacitance and V is the rated voltage of the capacitor. The justifications for these metrics are provided in Appendix C.2 and Appendix C.3.

For the FCMC, the energy storage requirement for the inductor is given by Eq. (5.8) and the energy storage requirement for the capacitor is given by Eq. (5.17). For simplicity, both Eq. (5.8)

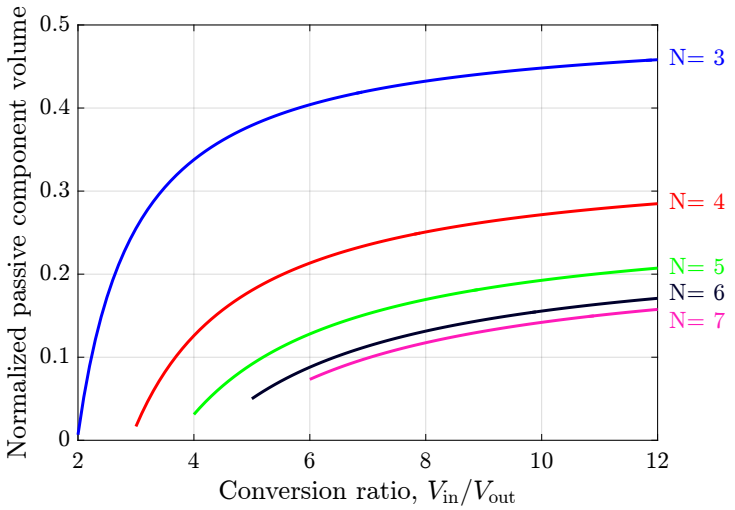


Figure 5.7: Passive component volume required by the FCMC normalized by that required by two-level buck converter.

and Eq. (5.17) use the nominal values of inductor current and capacitor voltages, by assuming a relatively small ripple. By comparing Eq. (5.17) and Eq. (5.8), it can be seen that the ratio of the energy stored by the capacitor to that of the inductor only depends on the conversion ratio, the number of levels and the percentage ripples, and is independent of the output power and switching frequency:

$$\frac{E_{C,\text{FCMC}}}{E_{L,\text{FCMC}}} = \frac{(N-1)(N-2)(2N-3)}{6(1-\frac{V_{\text{out}}(N-1)}{V_{\text{in}}})} \times \frac{\alpha_I}{\alpha_V} \tag{5.18}$$

The energy stored by the capacitors and inductors cannot be simply added together, since the energy densities of capacitors and inductors can be different by orders of magnitude. In order to compare the volume, the energy needs to be converted into a total volumetric figure of merit, as given by

$$\mathrm{V}_{\text{tot}} = \mathrm{V}_L + \mathrm{V}_C = \frac{\mathrm{E}_L}{\rho_{E,L}} + \frac{\mathrm{E}_C}{\rho_{E,C}}, \tag{5.19}$$

where $\rho_{E,L}$ and $\rho_{E,C}$ are the volumetric energy densities of inductors and capacitors respectively. Therefore, the volume ratio of the FCMC and buck converters is given by

$$\begin{aligned}\frac{\mathrm{V}_{\text{tot,FCMC}}}{\mathrm{V}_{\text{tot,buck}}} =& \frac{(\frac{\mathrm{E}_L}{\rho_{E,L}} + \frac{\mathrm{E}_C}{\rho_{E,C}})_{\text{FCMC}}}{(\frac{\mathrm{E}_L}{\rho_{E,L}})_{\text{buck}}} \\ =& \frac{E_{L,\text{FCMC}}}{E_{L,\text{buck}}}(1 + \frac{E_{C,\text{FCMC}}}{E_{L,\text{FCMC}}}\frac{\rho_{E,L}}{\rho_{E,C}}).\end{aligned} \tag{5.20}$$

By assuming an appropriate $\frac{\rho_{E,C}}{\rho_{E,L}}$ ratio, one can find the total passive component volume normal-

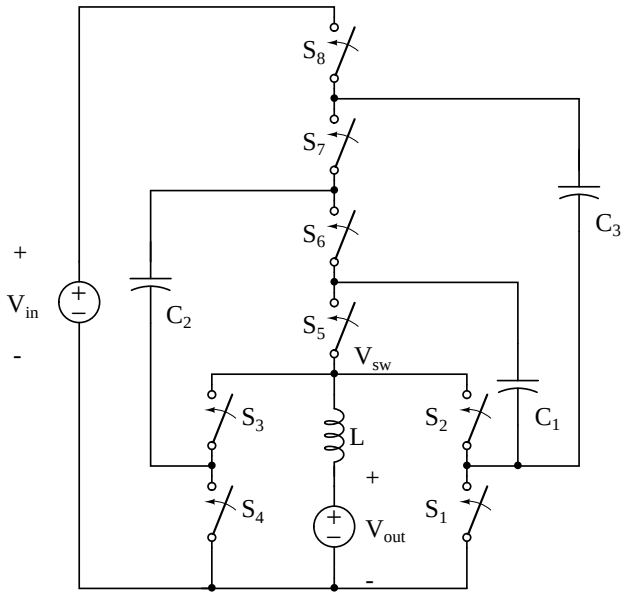


Figure 5.8: Schematic drawing of a 4-to-1 soft-charging Dickson converter.

ized with respect to that required by the two-level buck converter from Eq. (5.18) and Eq. (5.20). An example is provided in Fig. 5.7, using $\alpha_V = \alpha_I = 0.2$ and a $\frac{\rho_{E,C}}{\rho_{E,L}}$ ratio of 150, which is an average value obtained from a survey of X7R capacitors from TDK and XAL inductors from Coilcraft as shown in Appendix C.3. Comparing Fig. 5.5 and Fig. 5.7, one can observe that the increase in total volume due to the capacitors is small with fewer levels, but with more levels the capacitor size starts to be comparable to that of inductors, and further increase in the number of levels will yield minimal benefit. Therefore, the proposed method can also be used to determine the optimal number of levels of FCMC converters for a particular application. It should be noted that the exact curves in Fig. 5.7 depend on the parameters used $(\alpha_I, \alpha_V, \rho_{E,L}, \rho_{E,C})$, and will change based on the actual components selected and thus will be different for each design. The contribution here is the development of such a general and quantitative method to aid in the evaluation and design of the multilevel converters.

5.4 Generalization to Hybrid SC Converters

Another type of converter that utilizes both capacitors and inductors for energy transfer is the hybrid switched capacitor converter. In this section, the proposed analytical method is applied to hybrid SC converters, and a more generalized way to obtain the switch conductance and switching frequency is presented. One example of the hybrid SC converters is the soft-charging Dickson converter in Chapter 4, whose schematic is repeated in Fig. 5.8. The capacitor voltage ratings for the Dickson converter are the same as the FCMC converters, while the voltage ratings for the switches are $\frac{1}{N-1}V_{\text{in}}$ (for S_1, S_2, S_3, S_4, S_5, S_8) and $\frac{2}{N-1}V_{\text{in}}$ (for S_6, S_7).

An analysis following the method presented in Section 5.2 is carried out for the hybrid Dickson converter. The first step is to determine the required switch conductance such that the conduction loss of the Dickson converter is the same as that of a buck converter. The difficulty of analyzing such converters lies in the fact that multiple circuit branches conduct current to the load simultaneously, unlike in the FCMC converter, in which there is only a single current loop. Thus, a general switched-capacitor analysis approach is taken, by calculating the current through the capacitors using the charge multiplier method presented in [12], with modification to take into account of the regulation operation. It should be noted that while the conduction loss of the the FCMC converter can be easily related to the buck converter using the specific analysis in Section 5.3, it can also be formally determined by the general analysis presented in this section.

A charge multiplier vector can be defined for the switches in each phase of the topology as

$$\begin{bmatrix} a_{\text{in},j} & a_{1,j} & a_{2,j} & a_{3,j} & \dots & a_{\text{out},j} \end{bmatrix}, \tag{5.21}$$

where each element is defined as $a_{i,j} = \frac{q_{i,j}}{q_{\text{out}}}$, i.e. the charge through the ith switch in the jth phase normalized by the total charge delivered to the load over the entire switching period. The first and last elements correspond to the charge delivered by the input source and the load. The total conduction loss through the switches can be calculated from the mean squared value of the currents, and is then given by

$$P_{\text{cond}} = I_{\text{out}}^2 \sum_{j}^{\text{phases}} \frac{1}{D_j} \sum_{i}^{\text{switches}} a_{i,j}^2 R_i, \tag{5.22}$$

where D_j is the duty ratio of the jth phase, and R_i is the on-state resistance of the ith switch.

Each element of the charge multiplier vector in Eq. (5.21) can be found by summing the charges through the appropriate capacitors, which in turn can be found through KCL analysis [12, 28]. The conduction loss of the two-phase Dickson converter is calculated, and is found to approach Eq. (5.23) as N increases.

$$P_{\text{cond}} = 2 I_{\text{out}}^2 R_1, \tag{5.23}$$

For simplicity, the resistance of each switch is assumed to be the same, and is R_1. Comparing Eq. (5.23) to that of the buck converter, we know that in order to achieve the same conduction loss, the switch conductance of the Dickson converter is given by

$$\frac{G_{\text{Dickson}}}{G_{\text{buck}}} = 2. \tag{5.24}$$

The next step is to determine the switching frequency that satisfies

$$\sum (GV^2)_{\text{Dickson}} \times f_{\text{Dickson}} = \sum (GV^2)_{\text{buck}} \times f_{\text{buck}}, \tag{5.25}$$

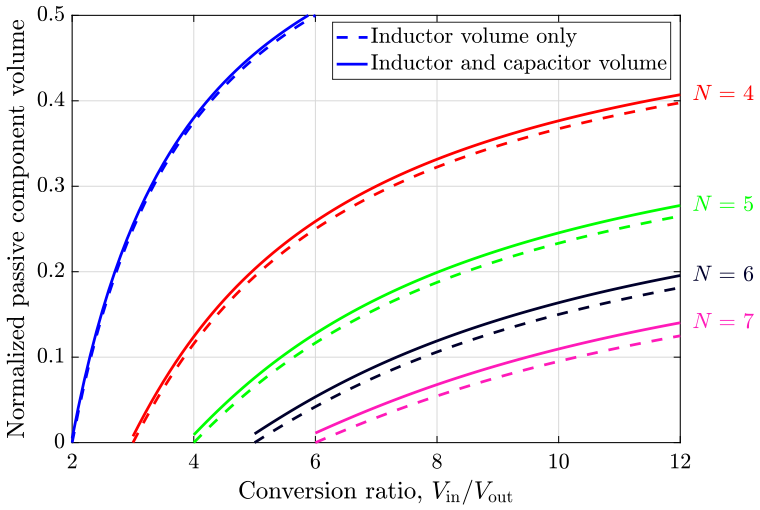


Figure 5.9: Passive component volume required by the hybrid Dickson converter normalized by that required by two-level buck converter. N is number of levels.

which can be rearranged to

$$\frac{f_{\text{Dickson}}}{f_{\text{buck}}} = \frac{G_{\text{buck}}}{G_{\text{Dickson}}} \times \frac{\sum(V^2)_{\text{buck}}}{\sum(V^2)_{\text{Dickson}}}. \tag{5.26}$$

With known switch conductance and voltage ratings, Eq. (5.26) can then be evaluated as

$$\frac{f_{\text{Dickson}}}{f_{\text{buck}}} = \frac{(N-1)^2}{4(N-1)+6}. \tag{5.27}$$

The energy stored by the inductors and flying capacitors of the hybrid Dickson converter can then be calculated in the same way as the FCMC converter, and only the final results are presented in this section. The overall passive component volume required by the Dickson converter normalized by that of the two-level buck converter is plotted in Fig. 5.9. It can be seen that similar to the FCMC converter, the Dickson converter yields significant reduction in passive component volume. However, the volume penalty introduced by the flying capacitance as the number of levels increases is much smaller compared to the FCMC, due to more efficient utilization of the capacitors by the parallel-connected branches. It can be concluded that the Dickson converter is a better topology when the number of levels and the voltage conversion ratio are large.

It should also be noted that there are other practical aspects that influence the choice of topologies, such as the available switches and capacitors. For example, the Dickson converter has fewer switches at higher conversion ratios, thus requiring fewer gate drivers and level-shifters. In addition, the control of the Dickson converter is simpler due to fewer circuit states, and the balance of flying capacitor voltages is less of an issue. On the other hand, the FCMC can provide a wide range of output (V_{in} to 0), while the Dickson converter only provides an output voltage between $\frac{V_{\text{in}}}{N-1}$ to 0.

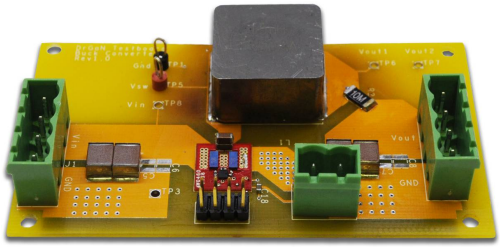
Table 5.2: Component listings.

	Buck	3-level FCMC	Hybrid Dickson
f_{sw}	200 kHz	200 kHz	250 kHz
Switches	EPC2010C x 2	EPC2001C x 4	EPC2007 x 6, EPC2015 x 4
$R_{ds,on}$	25 mΩ	7 mΩ	30 mΩ, 4 mΩ
V_{ds}	200 V	100 V	100 V, 40 V
Inductor	IHLP-8787MZ-5A	IHLP-6767GZ-11	IHLP-5050CE-01
Inductance	47 μH	22 μH	6.8 μH
I_{sat}	10.0 A	9.5 A	18 A
R_{dc}	17.3 mΩ	20.0 mΩ	19.8 mΩ
Flying capacitor value	-	4.7 uF	1.0 uF
Voltage	-	100 V x 2	250 V x3, 100 V x 2

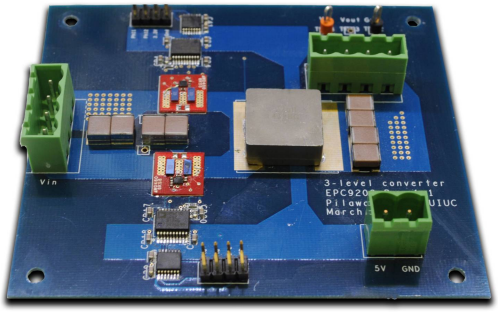
5.5 Experimental Verification

In order to experimentally validate the proposed analytical method, reference designs are developed, following the principles used in the analytical comparison, subjected to available part selection. Two converter prototypes are implemented: a buck converter and a 3-level FCMC to compare with the 7-level hybrid Dickson SC converter in Chapter 4. The converters are designed with an input voltage of 100 V and an output voltage of 12 V. An output current of 4 A has been tested without external cooling. The component listings for the converter prototypes are shown in Table 5.2. GaN switches are used on all three prototypes for similar switch performance. A voltage rating margin of approximately 2x is chosen for the switches for all three converters. The inductor is chosen to have a dc resistance of approximately 20 mΩ, so that the conduction loss is similar to that in the switches, and a current ripple of about 1.1 A. As a result, the inductor has current rating of about 10 A while the peak load tested is only 4 A. To make a fair comparison, the capacitors are also selected with a voltage that is 2x that of the rated voltage. The converter photos are shown in Fig. 5.10. It should be noted that while care has been taken in the board layout to reduce the parasitics, the component placement is not optimized for a minimum overall converter size. Therefore, the volumes of individual components are compared (inductors, capacitors and switches). This also corresponds to the comparison methodology, which does not take into account the influence on the converter size by the PCB layout.

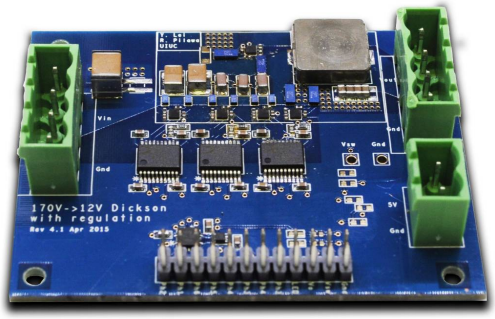
The normalized power losses (defined as $\frac{P_{\text{in}}-P_{\text{out}}}{P_{\text{in}}}$) of the converters at the rated voltages are plotted in Fig. 5.11. It should be noted that according to the comparison methodology, each converter is to be designed with the same power loss, and therefore similar power losses should be expected from all three prototypes. From Fig. 5.11, it can be seen that the power losses for the converters at 4 A load (where conduction loss dominates) are within 25% of each other. It should be noted that while we strive to follow the methodology presented here in the design of the converters, the choices in components are oftentimes limited by available parts. This partly



(a) 2-level (buck) converter.



(b) 3-level FCMC.



(c) 7-level hybrid Dickson.

Figure 5.10: Photos of converter prototypes.

explains the lower power loss for the Dickson SC converter at light load. Overall, the power losses are close to each other, and the volume comparison can be carried out on a fair ground.

The volumes of the passive components used in the prototypes are compared in Table 5.3. It can be seen that the inductor size can be reduced considerably by moving to a higher number of levels, while the additional capacitor volume is only a fraction of inductor size. The overall volume is reduced by a factor of approximately three each time, as the number of levels increased from two to three, and then to seven. It should be noted that the goal of the comparison is not to conclude that the Dickson SC converter is a better topology than an FCMC, but rather to show that a topology with more levels can result in a smaller overall volume than a topology with fewer levels. To visualize the difference in the passive component volume, photos of the passive components for the three converters are shown in Fig. 5.12.

Another advantage associated with reduced inductor size is that the inductor can have a lower

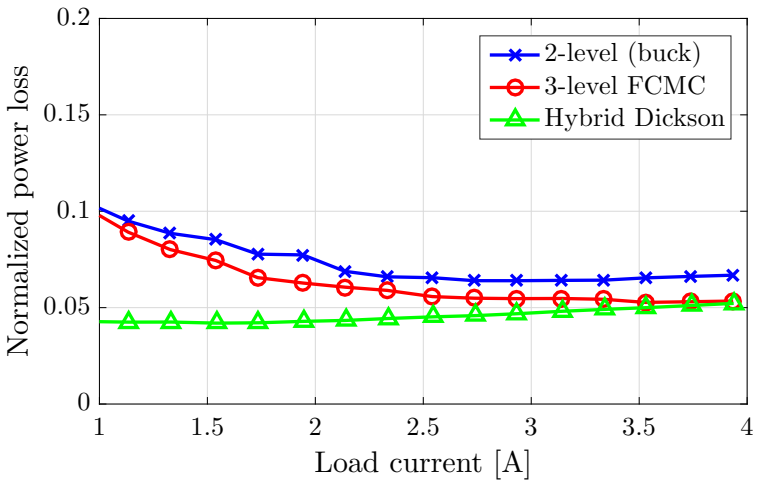


Figure 5.11: Normalized power loss comparison between the buck, 3-level FCMC, and hybrid Dickson converter.

Table 5.3: Volume comparison of passive components.

	2-level (buck)	3-level FCMC	Hybrid Dickson
Inductor	6292 mm^3	2059 mm^3	596 mm^3
Capacitor	-	125 mm^3	115 mm^3
Total	6292 mm^3	2184 mm^3	711 mm^3

height, reducing the overall profile of the design. This has a large impact on the overall volume, since the switches and control circuitry are usually very thin. This advantage can offset the additional footprint of gate drivers and level-shifters in the multilevel topologies. The PCB areas occupied by the converters are compared in Table 5.4, as well as the final volume of the overall converter. It can be seen that even for a relatively low-power application (50 W), where the auxiliary circuits can occupy a large portion of the converter area, the overall converter volume can be significantly reduced with multilevel converters.

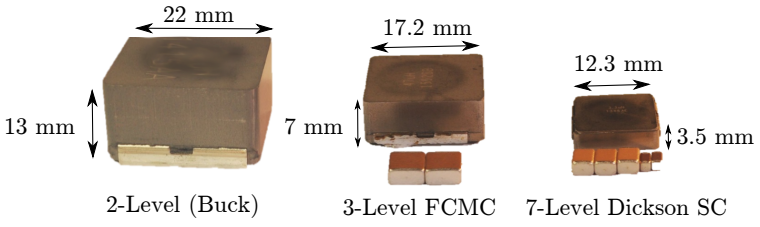


Figure 5.12: Photos of inductors and flying capacitors used by the three converter prototypes.

Table 5.4: Area and overall volume of the prototypes.

	Buck	3-level FCMC	Hybrid Dickson
Passive components (mm^2)	500	350	230
Switches and drivers (mm^2)	25	50	125
Level-shifters	-	100	300
Total area (mm^2)	525	500	655
Maximum height (mm)	13	7	3.5
Overall volume (mm^3)	6800	3500	2300

5.6 Chapter Summary

In this chapter, an analytical method to compare different multilevel and hybrid SC converters is presented, based on the fundamental active and passive device utilization. The proposed method keeps the losses of the converters the same and uses the overall passive device volume as a convenient metric to evaluate these converters. The use of multilevel converters in large step-down dc-dc conversion applications is explored. It is shown that both types of multilevel converters have significantly reduced passive component volumes, compared to two-level buck converters. The hybrid Dickson SC converter is especially suited for designs with many levels due to the efficient use of flying capacitors. Three converter prototypes are implemented to support the proposed methodology. It is shown with both theoretical analysis and hardware that these multilevel converters can achieve a higher efficiency and power density than conventional buck converters.

CHAPTER 6

DESIGN OF A SINGLE-PHASE MULTILEVEL INVERTER WITH AN ACTIVE ENERGY BUFFER

6.1 Motivation

Recent efforts in industry and academia have emphasized the reduction in the physical dimensions and weight of inverters and rectifiers for use in residential and commercial grid-interfaced applications, such as solar energy harvesting and electric vehicle battery charging. A smaller and lighter inverter can reduce the size of the overall system, and the associated cost of installation, operation and maintenance. In addition to high power density, it is also preferable to maintain high efficiency. By reducing the losses and associated heat generation, the additional power losses and size overhead introduced by the cooling efforts can be minimized.

A common inverter topology is an H-bridge operating with pulse width modulation (PWM). Compared to non-PWM inverters, which usually have a large harmonic content in the output waveform, the PWM H-bridge pushes the undesired frequency content up near the switching frequency. Thus, it is desirable to leverage a high switching frequency such that the output filter size is significantly reduced. Yet, the high-frequency switching actions result in high power loss, which limits the maximum switching frequency in practice. In-depth investigations have been carried out to quantify the power densities achievable by two-level PWM converters. Passive components and thermal management are identified as the main barrier for further power density increase [1].

A promising alternative approach is multilevel converters, which operate by generating a low-frequency staircase waveform, whose fundamental Fourier component approximates the desired sinusoidal waveform. The PWM operation can be carried out between two adjacent voltage levels of the staircase waveform. Therefore, multilevel converters require much smaller filter size for the same total harmonic distortion (THD) content and inductor current ripple. Common multilevel converter topologies include the cascaded H-bridge (CHB), diode clamped (DC), flying capacitor multilevel (FCML) [42] and the modular multilevel converters (MMC) [54–56]. The MMC has become most popular in medium (1 kV - 70 kV) and high (>70 kV) voltage applications owing to its modularity and scalability [56], as it makes use of both low voltage switches and low voltage capacitors. However, the capacitors of the MMC have a dominating voltage ripple at the fundamental frequency of the AC waveform, leading to a large energy storage requirement for the capacitors, especially for low-frequency applications [57]. While there are control techniques that inject current harmonics in the MMC arms to reduce the fundamental frequency ripple, there can be significant

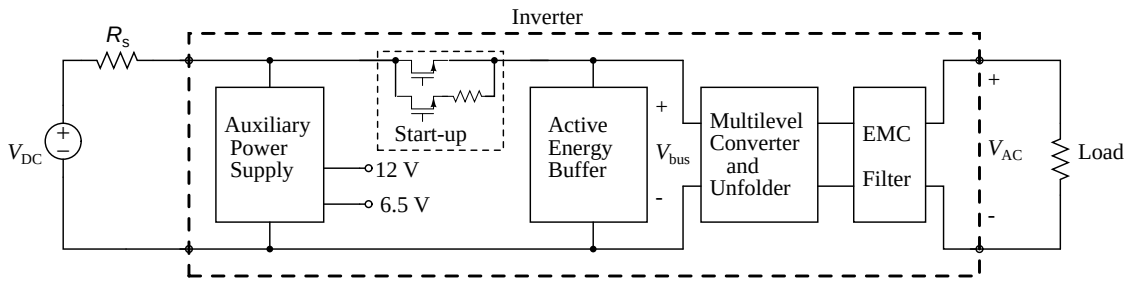


Figure 6.1: Full system overview of the single-phase inverter.

efficiency penalty due to the increased circulating current [55]. On the other hand, FCML converters (also known as multilevel buck converters in dc-dc applications) [42, 46, 58–62], and their topological variants [63, 64], alternate the charging and discharging states of the flying capacitors at the switching frequency, allowing for reduced capacitor energy storage if the switching frequency is increased [57]. Therefore, FCML converters can exhibit a higher power density and efficiency in low voltage applications ($<$ 1kV), where high energy density ceramic capacitors are readily available. Existing efforts in FCML converters mostly focus on modulation techniques [65, 66] and capacitor voltage balancing methods [43, 67], while little attention is given to the potential for high power density. Recent hardware prototypes in the low voltage range either have a small number of levels [60, 65, 66] or switch at a low frequency (less than 10 kHz) [59, 61, 64, 66].

Another challenge associated with single-phase power converters involves the twice-line-frequency power pulsation. On the ac side of the inverter, the product of the sinusoidal output voltage and current results in a twice-line-frequency (120 Hz) power ripple. On the dc side, a constant power draw is desirable. The instantaneous power mismatch requires energy to be stored by the converter. This energy storage requirement cannot be reduced by increasing the switching frequency, as it depends only on the power output and line frequency.

This work is the first practical demonstration of a 7-level FCML converter implemented using GaN switches operating at a high frequency of 120 kHz. Both the number of levels and the switching frequency are much higher than previously reported in the literature. Moreover, this work has demonstrated – for the first time – that FCML converters can achieve power densities and efficiencies significantly higher than conventional, two-level designs through an innovative switching cell implementation that achieves low inductance commutation paths and enables the theoretical advantages of the FCML converter to be realized in practice. This work also incorporates an active energy buffer architecture that utilizes a partial processing technique to drastically reduce the required buffering capacitor values compared to conventional passive decoupling capacitors, while maintaining a very high efficiency [68, 69]. Finally, the hardware prototype has been evaluated and benchmarked against some of the most sophisticated hardware designs built to date [53, 70, 71] in the highly competitive Google/IEEE Little Box Challenge [72], which attracted high quality entries from academic and industrial research groups around the world. The inverter prototype is a stand-alone box, including auxiliary converters (to power the control and gate drivers from the

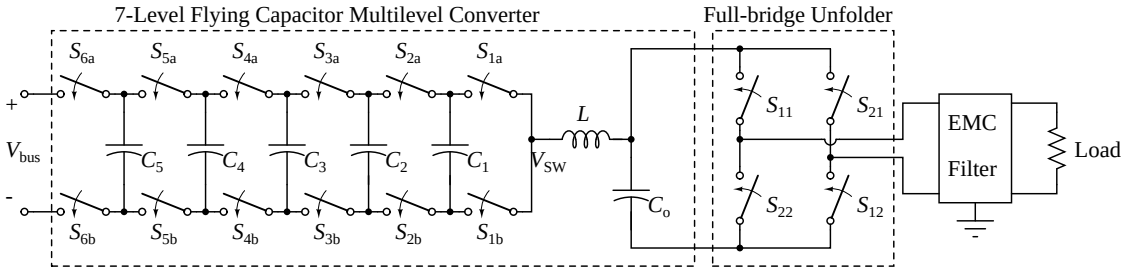


Figure 6.2: Schematic drawing of the dc-ac conversion stage, consisting of the 7-level flying-capacitor multilevel converter and the full-bridge unfolder.

450 V DC bus), start-up circuits, Electromagnetic interference compliance (EMC) filters (to meet FCC Class B requirements) and cooling fans. With rectangular dimensions of 4.02 in × 2.42 in × 0.95 in and a total volume of 9.26 in^3, the experimentally verified power density is 216 W/in^3. The measured peak efficiency is 97.6%, including the power losses from control and cooling fan.

This chapter is organized as follows: Section 6.2 provides the theory of operation and hardware implementation of the 7-level flying capacitor multilevel converter. Section 6.3 presents the operation and implementation of the active energy buffer. The design of the EMC filters is detailed in Section 6.4 and the measured experimental results for the converter prototype are provided in Section 6.5. Finally, conclusions are given in Section 6.6.

6.2 Flying Capacitor Multilevel Converter

The overall architecture of the single-phase inverter is shown in Fig. 6.1. The DC voltage source is connected to the inverter through a series resistance of 10 Ω, as prescribed by the Little Box Challenge document. At full load, the input current is 5 A, resulting in a 50 V drop across the resistance. The resistance is added to emulate the IV characteristics of a PV panel, which is one of the target application of the proposed inverter. Apart from the main multilevel converter and the active energy buffer, there is also an auxiliary converter, which generates 12 V and 6.5 V from 450 V for control and fan power, a start-up circuitry to limit the inrush current, and filters for electromagnetic emission compliance. This section presents the details of the multilevel converter block while the buffer converter block is presented in Section 6.3.

6.2.1 Principle of operation and converter design

The schematic drawing of the dc-ac conversion stage is shown in Fig. 6.2. It consists of a 7-level FCML converter and an H-bridge unfolder. The FCML converter produces a rectified sinusoidal output between 0 V and V_{bus}, while the unfolder flips the polarity of the output every 1/120 second to produce a true AC output.

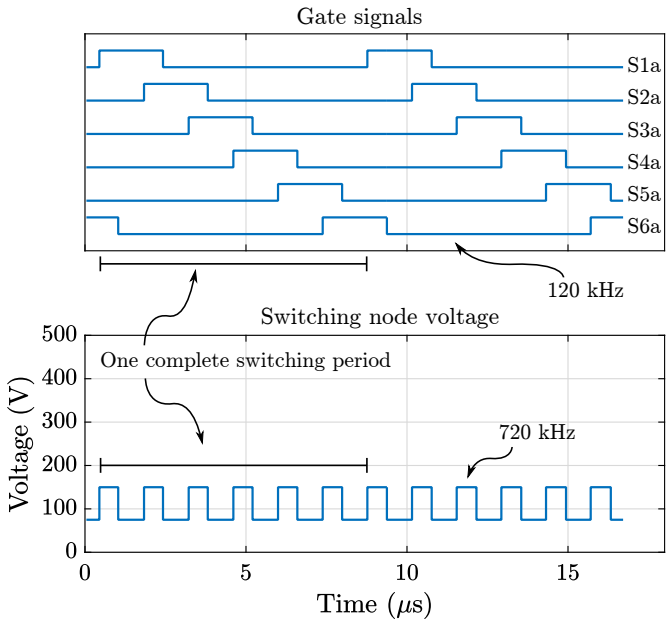


Figure 6.3: Gate signals (with high representing on state) and simulated switching node voltage (V_{sw}) at the switching frequency. While the switching frequency of individual switches is 120 kHz, the effective ripple frequency seen by the inductor is six times higher (720 kHz).

For an FCML converter with N levels, there are $(N-1)$ pairs of switches, each with an ideal voltage rating of $\frac{V_{\text{bus}}}{N-1}$. There are also $(N-2)$ flying capacitors with ratings of $\frac{V_{\text{bus}}}{N-1}$, $\frac{2V_{\text{bus}}}{N-1}$, ..., $\frac{(N-2)V_{\text{bus}}}{N-1}$, respectively. In this work, the FCML converter is operated with phase-shifted pulse width modulation (PSPWM) [42]. In this control scheme, each adjacent switch turns on and off with a phase shift of $\frac{360}{N-1}$ degrees. The signals for the "a" switches are complementary to those for the "b" switches. All the "a" switches have a duty ratio of D, and all the "b" switches have a duty ratio of $1-D$, and the average output voltage is given by DV_{bus}. Figure 6.3 shows the gate signals for the "a" switches of the 7-level converter with a duty ratio of 25%. It can be seen that each switch has a phase lag of 60 degrees from the previous one. In one complete switching period of each switch, the switching node voltage has six pulses. In addition, the pulses are in-between two intermediate voltage levels set by the flying capacitors. By modulating the duty ratio, the switching node voltage can be made to follow a rectified sinusoidal waveform, as shown in Fig. 6.4.

A major advantage of the FCML converter is the reduction in the required output filter inductor size. Compared to a conventional two-level converter, the PWM operation is between two voltage levels that are only $\frac{V_{\text{bus}}}{N-1}$ apart, where N is the number of levels. In addition, the effective pulse frequency seen by the filter inductor is $(N-1)f_{\text{sw}}$, where f_{sw} is the switching frequency of each switch. Therefore, the worst inductor current ripple of an N-level FCML converter is given by

$$\Delta i_L = \frac{0.25V_{\text{DC}}}{(N-1)^2 f_{\text{sw}} L}. \tag{6.1}$$

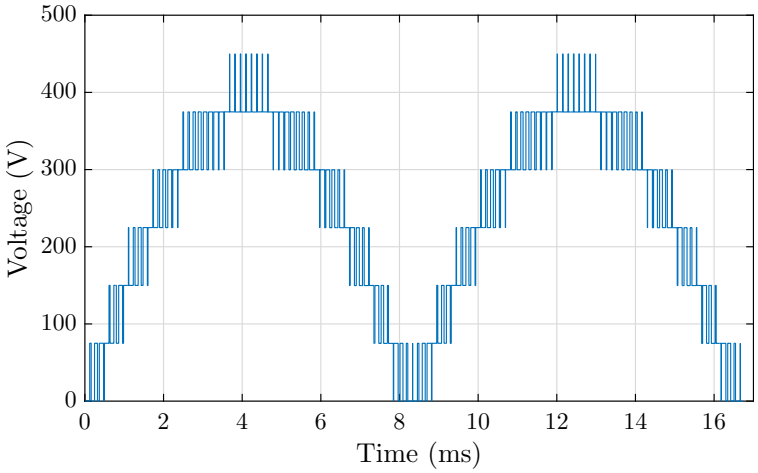


Figure 6.4: Simulated switching node voltage (V_{sw}) in $\frac{1}{60}$ of a second, showing the rectified sine-wave modulation used. Note that the switching frequency is reduced for better illustration of the PWM operation.

Thus, on an analytical level, given a certain inductor current ripple, an FCML converter can have an output inductor that is $\frac{1}{(N-1)^2}$ the size of that in a two-level converter [73]. This assumes that the switching frequency of each switch in a multilevel converter is the same as that of a two-level converter, which is a reasonable assumption in order for FCML converter to have similar conduction losses as well as switching losses compared to the two-level converters [74]. In this design, with the choice of $f_{\text{sw}} = 120$ kHz, a single 22 μH inductor is able to achieve a low current ripple of 1.2 A.

The values of the flying capacitors are designed based on the allowed voltage ripple. A higher voltage ripple enables the flying capacitor to transfer more energy in a switching cycle, and thus reduces the required capacitor values, but the large ripple also increases the voltage stress on the switches. For the FCML converters, the worst case peak-to-peak voltage ripple on capacitors needs to be below $\frac{V_{\text{DC}}}{N-1}$ by design. Otherwise, a scenario where $V_{Ci} > V_{Ci-1}$ can occur momentarily during a switching cycle, resulting in a negative voltage on the switches and forcing the body diode to turn on [75]. The capacitance of the flying capacitors is given by (6.2). With 1.5 μF as each of the flying capacitors, the voltage ripple is about 12 V.

$$C = \frac{I_{\text{out,max}}}{\Delta V_c f_{\text{sw}} (N-1)} \tag{6.2}$$

6.2.2 Hardware implementation

Several implementation challenges were met when building the high-frequency multilevel converter under area and space constraint. This section discusses the design choices and challenges, as well as our approaches to solve them.

GaN switches are selected in this work, since in general they have better figures of merit compared to silicon devices, such as a smaller $R_{ds,on}Q_{oss}$ or $R_{ds,on}Q_{gd}$ product [76]. This allows a lower

conduction loss, a higher switching frequency, and smaller filter components. In addition, the 5 V V_{gs} operating voltage, instead of 7 to 15 V of silicon MOSFETs, can also enable the use of 5 V level-shifting circuits.

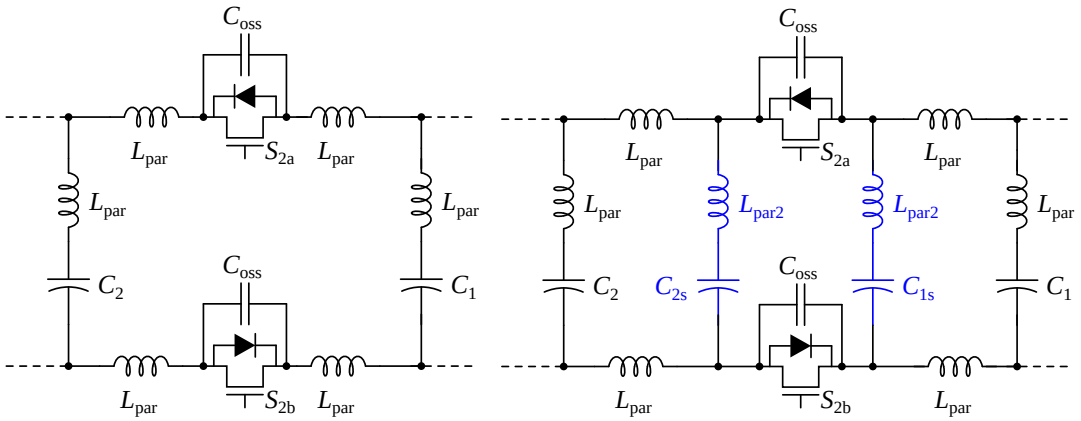
Common to all multilevel converters, the distributed switches have source voltages at different voltage domains. Therefore, floating power supplies are needed for each gate driver. While in high power applications, these auxiliary circuits account for a small fraction of the total volume, due to the large passive components, in this design, their area cannot be neglected due to the small targeted overall volume. In this work, fully integrated isolated power supplies with a 5 V output are used to deliver the power for the gate drivers at their respective floating ground. In addition, a single half-bridge gate driver is used for each pair of adjacent switches, due to their cascade connection in the FCML converter.

Another common practical implementation issue associated with multilevel converters is the capacitor voltage imbalance, which describes the scenario where the actual capacitor voltages are deviated from the ideal desired levels. Since the switch voltage stress is the difference between the voltages of adjacent capacitors, imbalanced capacitor voltages increase the drain-source voltage stress across the switches, which can lead to switch failure if the rated blocking voltage is exceeded. In order to keep the capacitor voltages within a desired set of bounds, the capacitor voltages can be monitored and actively controlled by changing the switching patterns to selectively charge or discharge one or more flying capacitors [43, 67]. Yet, these methods can be difficult to apply to inverters with a high number of levels, high switching frequency and small capacitor values, due to the high bandwidth sensing and control required, and the added area overhead. Instead, in our hardware implementations, we rely on the natural balancing property of the PSPWM scheme [77–79]. In short, the capacitor voltage imbalance increases inductor current ripple, which in turn causes power dissipation in the series resistance of the circuit, such that the capacitors are incrementally charged/discharged towards their nominal voltages. This self-balancing property can offset the adverse effect of the non-ideality in the circuits, as long as the non-ideality are small. Therefore, to minimize capacitor voltage imbalance, in this work, efforts are made towards a precise generation of the PWM gate signals using the microcontroller, and a symmetrical board layout to minimize the parasitic effects.

The switching frequency of the transistors is 120 kHz, generating an effective frequency of 720 kHz. This is substantially higher than reported in existing literature, partly owing to the use of GaN devices. The GaN switches have extremely low output capacitance, and thus the main source of switching loss is the voltage-current overlap during the switching transitions, as will be shown in Section 6.5 later. The challenge in operating the multilevel converter at such a high frequency is therefore to minimize the overlap time by increasing the $\mathrm{d}v/\mathrm{d}t$, without causing significant drain-source voltage ringing. Similar to that in a buck converter, voltage ringing can occur due to the interaction between the drain-source capacitance of the transistors and the parasitic inductance in the circuit during the fast turn-on of the high-side switch. The overshoot resulted from the ringing can exceed the drain-source breakdown voltage of the transistors.

In order to reduce the voltage ringing, the high $\mathrm{d}v/\mathrm{d}t$ loops need to be identified first. For the FCML converter, each "a", "b" switch pair operates in a complementary manner and thus forms a commutation loop in-between two flying capacitors, as shown in Fig. 6.5a. When the "a" switches turn on, the LC circuit consisting of the C_{oss} of the "b" switches and the parasitic inductance is excited by a high $\mathrm{d}v/\mathrm{d}t$ step, causing voltage ringing across the "b" switches. In general, a tight layout can help reduce the parasitic inductance. However, for FCML converter, the flying capacitors themselves have significant series inductance (ESL); and the relatively large size of these components limits how small the loop can be.

In order to reduce the parasitic inductance, a modular switching cell structure is proposed. Each cell is a daughter PCB consisting of two pairs of half-bridge connected switches with gate drivers, and small decoupling capacitors placed in parallel with the flying capacitors, in close proximity of the switches. As illustrated in Fig. 6.5b, the loop inductance can be significantly reduced due to the smaller current loop as well as the smaller ESL of the decoupling capacitors. A photo of the switching cell is shown in Fig. 6.6, with an overlay of the converter schematic. The 7-level FCML converter is constructed using three such switching cells.



(a) Without decoupling capacitors. (b) With decoupling capacitors.

Figure 6.5: Partial schematic of FCML converter including parasitic inductance and switch output capacitance.

The top, side and bottom views of the FCML inverter are shown in Fig. 6.7. To the left is the start-up circuitry in order to charge the flying capacitors and bus capacitors to their steady-state values. The flying capacitors and inductors are on the bottom side of the PCB, and are aligned in the center. Three capacitors, each with a nominal capacitance of 2.2 μF, are connected in parallel to make a single flying capacitor, so that the capacitance is at least 1.5 μF when biased at the rated voltage. To the right and on top of the PCB are the common-mode and differential-mode Electromagnetic interference (EMI) filters. A small common-mode choke that fits on the right edge on the back is not shown, since it is connected through the assembly. The GaN switches are placed in the center, distributed on the three red switching cells. The use of modular interchangeable

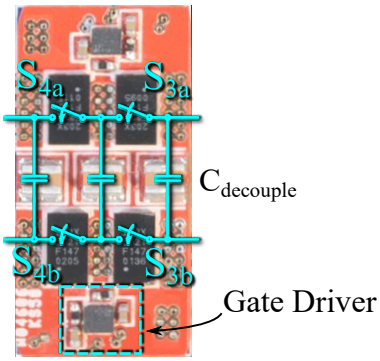


Figure 6.6: Photo of the switching cell, overlaid with a partial schematic drawing of the inverter.

switching cells also facilitates the assembly and rework of the converter during prototyping. The total thickness of the inverter is 10.3 mm and the tallest component is the inductor at 7.5 mm. This low profile is enabled by the drastically reduced inductor size with the multilevel structure as discussed previously. Finally, a component listing of the inverter board is given in Table 6.1.

Table 6.1: Component listing of the inverter board.

Component	Part number	Parameters
GaN switches (S_{1a}, S_{1b} to S_{6a}, S_{6b})	EPC 2033	150 V, 7 mΩ
GaN gate driver	Texas Instruments LM5113	100 V half-bridge
Unfolder MOSFETs ($S_{11}, S_{12}, S_{21}, S_{22}$)	STMicroelectronics STL57N65M5 $\times$2	650 V, 69 mΩ
Unfolder gate driver	Fairchild FAN73932MX	600 V half-bridge
Flying capacitors ($C_1 - C_5$)	TDK C5750X6S2W225K250KA $\times$3	2.2 μF $\times$3
Inductor	Vishay IHLP6767GZER220M11	22 μH
Digital isolators	Silicon Labs Si8423BB-D-IS	
Power isolators	Analog Devices ADUM5210	

6.3 120 Hz Input Current Ripple Compensation

The most common method to achieve twice-line-frequency power decoupling is to connect a passive capacitor bank across the dc bus. To meet the stringent ripple requirement on bus voltage and dc input current, a large volume of capacitors is required. Such a capacitor bank is typically formed by electrolytic capacitors due to their high energy density, but their high power loss, poor ripple current capability and short lifetime become a significant constraint [80]. Ceramic or film capacitors are preferable from an efficiency and reliability perspective, but they require a large volume, as their capacitance density is generally significantly lower than that of the electrolytic capacitors.

Many active decoupling approaches have been proposed in the literature to reduce the required capacitance and even allow for the use of ceramic or film capacitors [5, 70, 71, 81–84]. One common

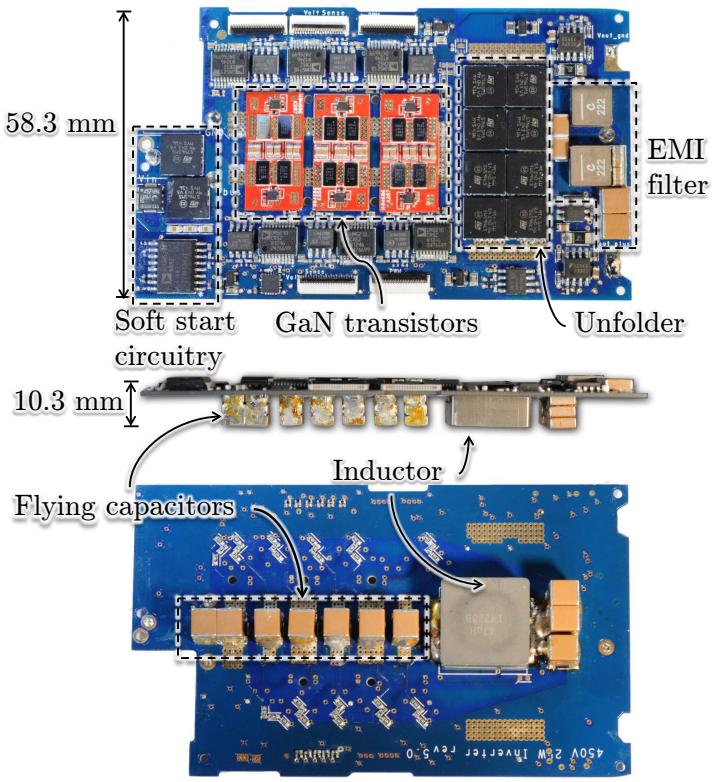


Figure 6.7: Annotated photographs of the FCML inverter board.

approach is a full ripple port converter [81, 82], where energy storage capacitors are interfaced to the dc bus through a power converter. The capacitors operate with a large voltage swing to buffer more energy, while the dc bus voltage is regulated by the ripple port converter. To achieve this functionality, the converter needs to process a large portion of the full power on average (i.e., $\frac{2}{\pi}P_{\text{out}}$, where P_{out} is the average output power of the inverter) and to withstand high voltage stress (i.e., the full dc bus voltage at least). As a result, ripple port converters can have a significant negative impact on the overall inverter efficiency. Moreover, the added volume (especially the magnetic components) can be very large and even completely offset the volume reduction from smaller energy storage capacitors.

In this work we use a series-stacked buffer architecture that overcomes the aforementioned problems. This architecture achieves very high efficiency and power density with a low complexity circuit while tightly regulating the dc bus voltage. Details on this buffer architecture are presented in [68, 69, 85], and this dissertation only provides an overview.

6.3.1 Principle of operation

The schematic drawing of the active energy buffer is shown in Fig. 6.8. In this architecture, a full-bridge converter is connected in series with a main energy storage capacitor, C_1. Unlike

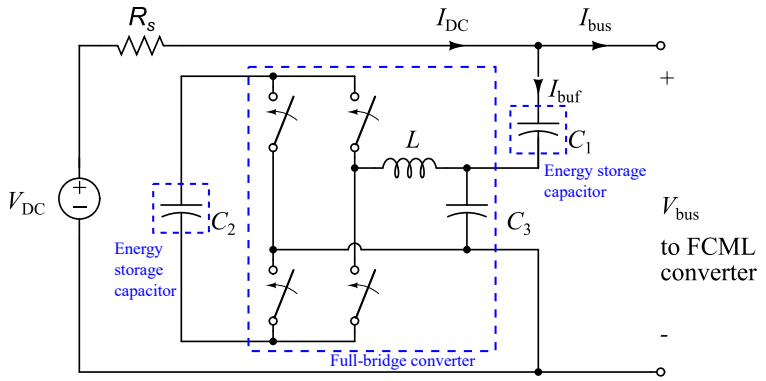


Figure 6.8: Schematic drawing of the active energy buffer. The auxiliary power supply and start-up circuit in Fig. 6.1 are omitted for simplicity.

conventional dc bus capacitors, C_1 is operated with a relatively large voltage ripple, for example at 25% of the rated voltage. Since V_{C1} has a relatively large ripple, the energy utilization is significantly increased compared to the dc bus capacitors, and much smaller capacitance is needed (eight times reduction in this design). To maintain a constant dc bus voltage, the voltage of C_3 is controlled such that its ac component is of the same magnitude but opposite sign to that of V_{C1}, as shown in Fig. 6.9. A support capacitor C_2 is used to maintain a certain voltage (higher than V_{C3}) to ensure the correct operation of the full-bridge converter, while C_3 is only a small filter capacitor to absorb the switching frequency ripple.

A key advantage of this architecture is that the full-bridge converter only processes a fraction of the total output power, as C_1 provides the bulk of the power buffering. While the entire active filter architecture buffers 2 kW in this application, the full-bridge converter only processes 100 W on average, as shown in Fig. 6.9. Hence, the efficiency penalty on the overall system is small. In this architecture, capacitor C_1 blocks the majority of the bus voltage, such that the voltage across the terminal labeled V_{C3} is only the ripple magnitude of V_{C1}. The full-bridge converter thus experiences low voltage stress, enabling the use of a small-size inductor and low-voltage, high-speed transistors for a small buffer converter size. A current hysteresis control scheme is implemented to match the buffer current with the inverter current, such that the voltage waveform in Fig. 6.9 follows naturally.

A considerable challenge in this architecture is that the losses in the full-bridge converter will drain capacitor C_2 over time. A loss compensation scheme which exploits the phase difference between the buffer current and bus voltage is devised to supply additional energy to capacitor C_2 to compensate for this loss. In our proposed method, the small bus voltage ripple is utilized to deliver a net positive energy into the converter, so that the voltage of C_2 can be maintained within appropriate bounds. A detailed explanation of the control scheme is presented in [69].

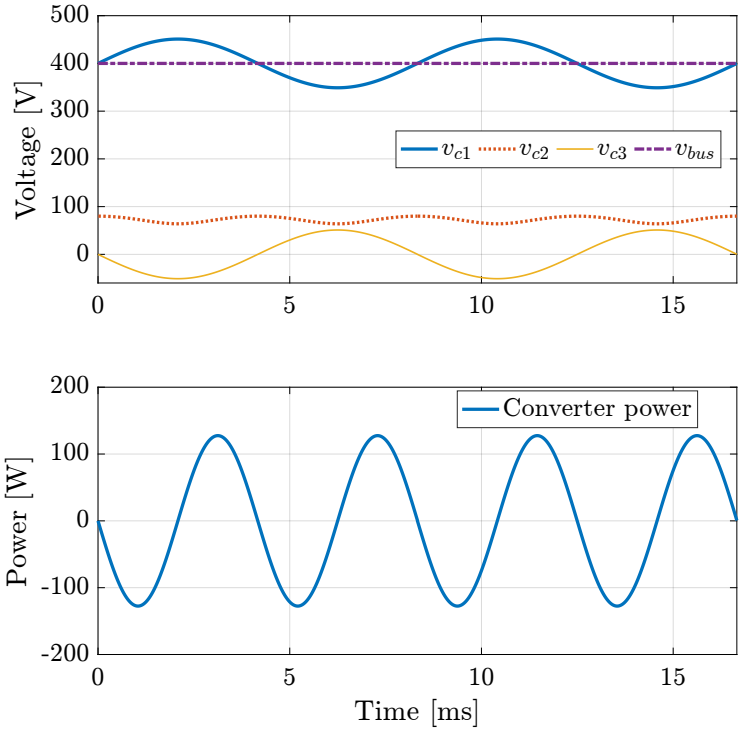


Figure 6.9: Waveforms illustrating the operation of the 2 kW active energy buffer architecture: voltages (top) and converter power (bottom). The power processed by the converter is only a fraction of the total power.

6.3.2 Hardware implementations

One practical issue with sizing ceramic capacitors for energy buffering is that their capacitance decreases in a non-linear fashion as the dc bias increases. It is common for the capacitance to reduce to less than one quarter of the nominal value when biased at the rated dc voltage. Thus, care must be taken to not over- or underestimate the required capacitor volume. The experiment based methodology presented in [86] is followed to determine precisely the energy storage capability of the ceramic capacitors.

Annotated photographs of the buffer converter board are shown in Fig. 6.10. The full-bridge converter and the sensing circuitry are placed on top, together with the microcontroller, which controls both the FCML inverter and the energy buffer. The capacitors C_1 and C_2 on the bottom side are placed such that the inverter flying capacitors and inductors can fit inside. This allows the inverter board to stack on top of the buffer board with minimal unused space in-between, as shown in Fig. 6.12. The auxiliary converter to power both the buffer converter and the inverter from the 450 V are placed in the bottom right corner. A component listing of the buffer converter is shown in Table 6.2.

Table 6.2: Component listing for the active energy buffer.

Component	Part number	Parameters
GaN FETs	EPC 2016C	100 V, 16 mΩ
Capacitors (C_1)	TDK C5750X6S2W225K250KA $\times$ 239	450 V, 2.2 μF $\times$239
Capacitors (C_2)	TDK CKG57NX7R2A106M500JH $\times$ 126	100V, 15 μF $\times$126
Inductor	Vishay IHLP6767GZER470M11 $\times$ 2	47 μH
Power isolators	Analog Devices ADUM5210	
Microcontroller	Texas Instruments TMX320F28377D	

6.4 Electromagnetic Compliance

For grid-interfaced converters, the electromagnetic interference emissions must be kept below the required limits set by regulatory bodies. In this work, the inverter has been designed so that the conducted emissions pass the FCC Part 15 Class B requirements [72]. The strategy for achieving EMC compliance was first to minimize any conducted and radiated EMI through careful layout and component placement. Efforts were made to reduce coupling between high $\mathrm{d}v/\mathrm{d}t$ nodes and sensitive analog circuitry. Particular attention was paid to ground planes, with large copper fills where appropriate. All loops were kept to a minimum, and signals were routed directly above a return path, or ground plane, to minimize the chance of coupling, and unintended radiation of signals. The fast transients of the GaN devices were well managed by the custom GaN modules, which minimize the commutation loops.

Overall, the multilevel architecture provides excellent inherent EMI mitigation, as each switching node only switches between potentials of $\frac{1}{6}V_{\mathrm{DC}}$ at a frequency of $6f_{\mathrm{sw}}$, rather than between 0 and V_{DC} at a frequency of f_{sw}, as is the case for conventional inverter structures. The reduction in switching amplitude and increase in effective ripple frequency help to relax the attenuation requirement for the filter.

In addition to these efforts to minimize the generated EMI, filters were placed at the converter output terminals to keep the small conducted EMI in the system from leaving the enclosure. The schematics of the EMI filters are shown in Fig. 6.11, and the component listing is in Table 6.3. As can be seen from the photographs in Fig. 6.7, the EMC filters constitutes to less than 10% of the inverter area and less than 3% of the volume. It should be noted that in the design competition targeted here, small overall size was the ultimate goal. In a product implementation, safety capacitors with suitable ratings would need to be employed in the EMI filter with larger overall footprints.

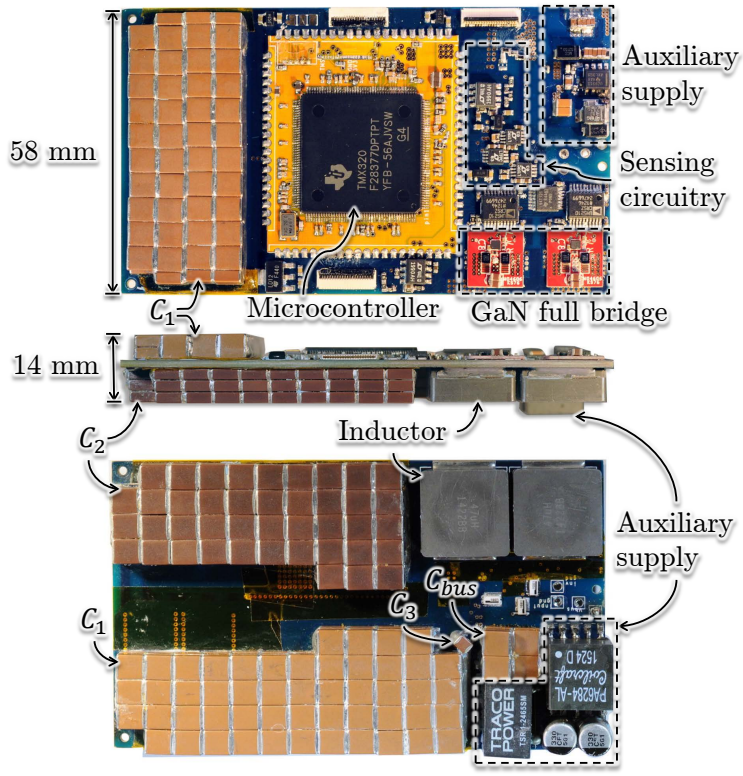


Figure 6.10: Annotated photographs of the active energy buffer board.

6.5 Experimental Results

The box enclosure, milled out of copper with heat-sink fins and fitted with blower fans, is shown in Fig. 6.13. With a dimension of 10.2 cm × 6.14 cm × 2.42 cm (4.02 in × 2.42 in × 0.95 in) and a total volume of 152 cm^3 (9.24 in^3), the inverter prototype achieves a power density of 13.2 W/cm^3 (216 W/in^3). The weight breakdown of the inverter is given in Table 6.4. The high-level performance metrics of the prototype are displayed in Table 6.5. For all metrics listed, the converter meets the specifications required by the Google/IEEE Little Box Challenge [72], and compares favorably against other published inverter prototypes [53, 70, 71] in the competition.

The individual efficiencies of the FCML inverter and the active energy buffer are measured with

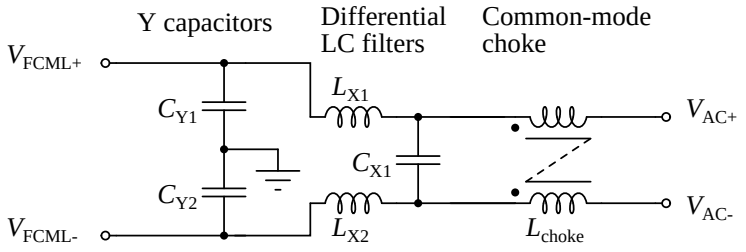


Figure 6.11: Schematic drawing of the EMC filter used in the inverter.

Table 6.3: Component listing of the EMC filter.

Component	Part number	Parameters
L_{X1}, L_{X2}	Coilcraft XAL7030-222ME	2.2 μH
C_{X1}	TDK C5750X6S2W225K250KA	2.2 μF $\times$2
	TDK C2012X7T2W473K125AA	0.047 μF $\times$6
L_{choke}	West coast magnetics 503-6	95.3 μH
C_{Y1}, C_{Y2}	TDK C3216X7T2W104K160AE	0.1 μF $\times$2

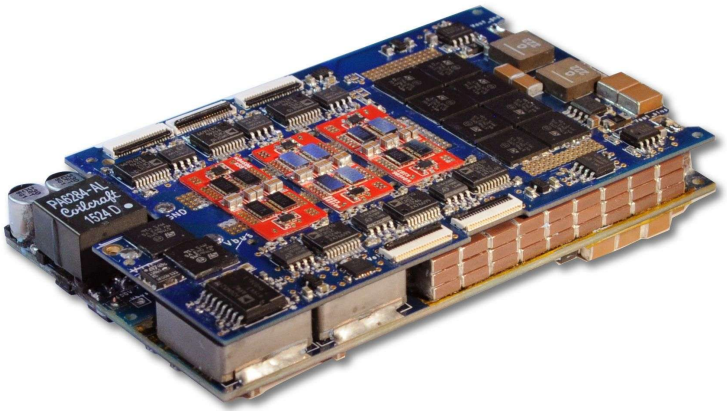


Figure 6.12: Photograph of the FCML inverter board and energy buffer fit together.

Yokogawa WT310 digital power meters, and are plotted in Fig. 6.14. It can be seen that the energy buffer alone is able to achieve a high efficiency of above 99%, thanks to the partial power processing architecture. For the multilevel inverter, the peak conversion efficiency is 98.6% at about half load and the efficiency at full load is above 98%. The efficiency of the inverter at 10% load is about 92%, without any special light load control. Since the output inductor is designed with a small current ripple, the light load efficiency of the converter can be improved by reducing the switching frequency, if so desired. Also shown in Fig. 6.14 is the efficiency after including all power losses from control and cooling fans, with error bars indicating potential measurement errors resulted from the precision limit of the power meters. A 450 V to 12 V fly-back converter and a 12 V to 6.5 V converter provide power for both the cooling fans (which consume about 5 W), and the control and gate driving circuits (which dissipate about 4 W). They represent a constant power loss independent of the load conditions. The overall light load efficiency can be further improved by turning-off the fan when the output power is below a preset threshold. A detailed estimated power loss breakdown at full load is shown in Fig. 6.15.

The full load operation of the energy buffer is shown in Fig. 6.16. At full load, the input current ripple is approximately 760 mA, which is 15% of the average input current. The voltage of C_2 and C_3 as well as the bus voltage are also shown. To generate a resultant bus voltage with a very small ripple, C_3 has a large voltage ripple in order to counter the voltage ripple of C_1 (not shown). The

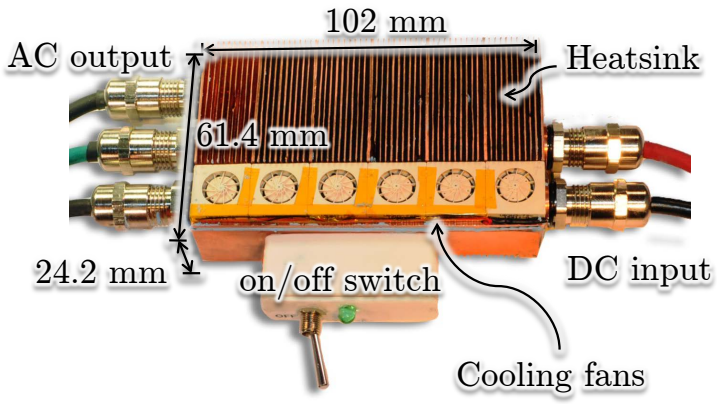


Figure 6.13: Photograph of the inverter prototype inside the heat-sink and enclosure.

Table 6.4: Converter weights breakdown.

Components	Weight (g)	Percentage	Specific power density (W/g)
Multilevel converter board, including start-up and EMC circuits	52	9.7%	38.4
Energy buffer board, including microcontroller and auxiliary power supply	209	39%	9.57
Copper enclosure	275	51.3%	-
Overall	536	100%	3.73

large voltage swing on C_1 is the key to the volume reduction of the buffer capacitors.

The operation of the 7-level inverter can be seen in Fig. 6.17, which shows the switching node voltage as well as the output voltage and current. The output voltage is 240 V RMS and the output current is 8.3 A RMS at full load. The switching node has a unipolar 120 Hz envelope as well as a high-frequency PWM between two smaller voltage levels.

The average flying capacitor voltages are monitored with a National Instruments data acquisition system (PXIe-1073), and are plotted in Fig. 6.18. With a PSPWM control scheme and no active capacitor voltage balancing, the capacitor voltages are evenly distributed across the input voltage range. This is the first demonstration that the FCML converter is able to self-balance capacitor voltages at this high number of levels and switching frequencies, with aggressive flying capacitor sizing. The maximum voltages across the GaN switches are measured and tabulated in Table 6.6. The deviations of switch voltages from ideal ratings are small and the largest increase in blocking voltage is approximately 12%.

The responses of the inverter during a load transient are presented in Fig. 6.19 and Fig. 6.20.

Table 6.5: Key performance specifications.

Specifications	Little Box	Achieved
Rated power	2 kVA	2 kVA
Volume	40 in^3	9.52 in^3 (152 cm^3)
Power density	50 W/in^3	216 W/in^3 (13.2 W/cm^3)
Rated input voltage	450 V	450 V
Rated output voltage	240 V_{RMS}	240 V_{RMS}
Efficiency (CEC Method)	95.0%	97.0%
Efficiency at rated power	95%	97.4%
Load power factor	0.7 – 1.0	0.7 – 1.0
Voltage THD	5%	0.3%
Input current ripple	20%	15%
Max. case temperature	60 °C	57 °C
EMC	FCC Class B	FCC Class B
Ground current	50 mA	1 mA

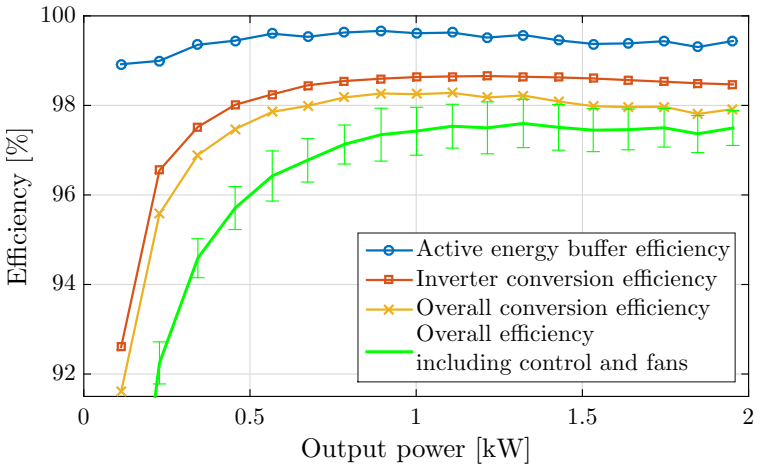


Figure 6.14: Converter efficiencies at different power levels.

Figure 6.19 shows the input current, bus voltage, V_{C2} and V_{C3} during a load step-down from 100% to 75%. The input current ripple comes back within the 20% specification in 80 ms after the load change. Figure 6.20 shows the output voltage and output current of the inverter during the same load step. The output voltage is not impacted by the change in load current.

At full power, the inverter incurs approximately 40 W of power loss. To dissipate this amount of heat, the top of the enclosure is machined with fins that are 2 mm tall. A total of six radial fans are placed on the edge of the top, blowing air across the fins. A thermal image is taken with a thermal camera after the converter reaches thermal steady-state at full power operation, and is shown in Fig. 6.21. It can be seen that the maximum temperature is at 57 °C.

The conducted EMI measurements made with a Tektronix RSA5126A real-time signal analyzer are depicted in Fig. 6.22. For the entire 150 kHz to 30 MHz measurement range, the inverter's

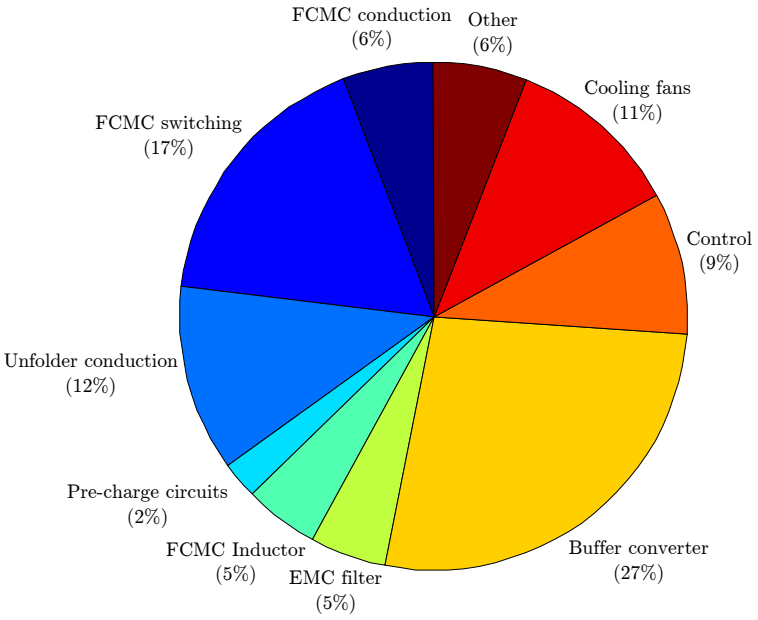


Figure 6.15: Estimated power loss breakdown of the converter at 2 kW load.

Table 6.6: Drain-source voltages across the switches

Switch	S_6	S_5	S_4	S_3	S_2	S_1
Measured at 20% load (V)	78	84	63	81	66	79
Measured at 100% load (V)	70	76	51	71	51	76

conducted EMI emission is lower than the Class B limit. The peak emission closest to the limit is at 720 kHz as expected, which is six times the switching frequency of 120 kHz. There are also peaks with comparable magnitude at the 2nd, 3rd, 4th and 5th harmonics of 120 kHz, which are the consequence of the imperfect capacitor voltage balance, and the lower attenuation strength of the EMC filter at lower frequencies. Parasitics in the filtering elements, such as the equivalent series inductance (ESL) of filter capacitors and inter-winding capacitance of filter inductors, cause the emissions to rise significantly after 10 MHz, but the emissions are still below the limit.

6.6 Chapter Summary

This chapter has presented a 2 kW, 450 V_{DC} to 240 V_{RMS} single-phase inverter. The dc to ac conversion is accomplished through a 7-level flying-capacitor multilevel converter, with GaN transistors switching at 120 kHz, which is the highest switching frequency achieved to date for a 7-level implementation. The commutation loop in the FCML converter is identified, and a switching cell design is used to minimize loop inductance and reduce the drain-source voltage ringing. In addition, the multilevel inverter is complemented by a series-stacked buffer converter for twice-line-frequency ripple compensation. The active energy buffer achieves a high efficiency of 99% while

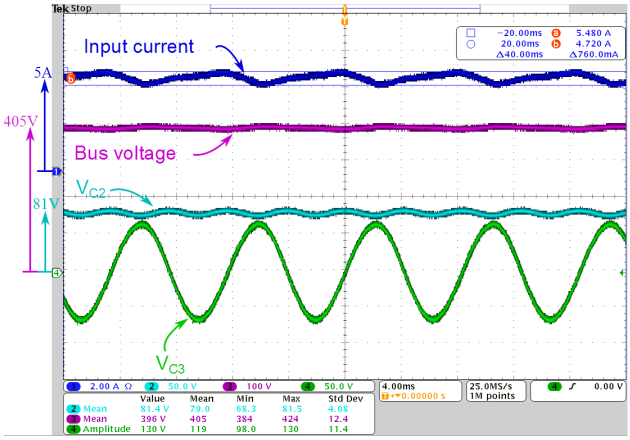


Figure 6.16: Waveforms showing active energy buffer operation at 2kW. Voltage ripple on V_{C3} counters the ripple on V_{C1} so that the bus voltage is constant.

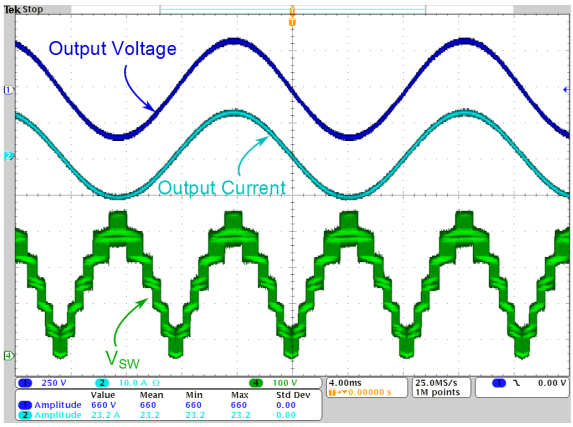


Figure 6.17: Waveforms showing the output voltage, output current and the switching node voltage (V_{SW}) of the 7-level inverter at full load.

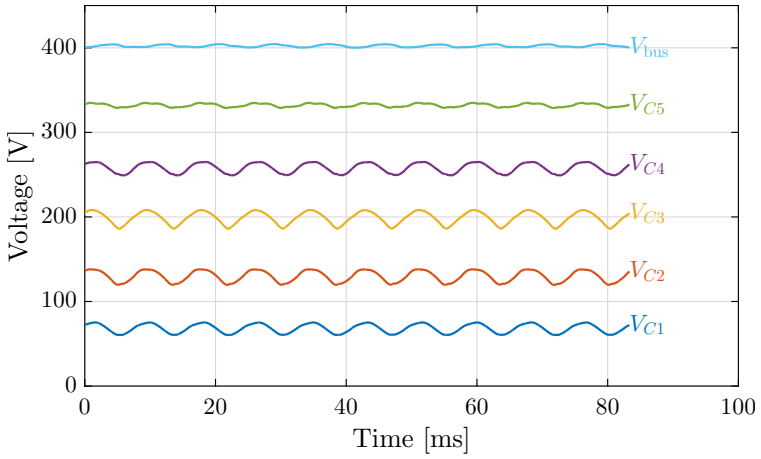


Figure 6.18: Capacitor voltages of the 7-level inverter during full load operation, obtained using National Instruments data acquisition system (PXIe-1073).

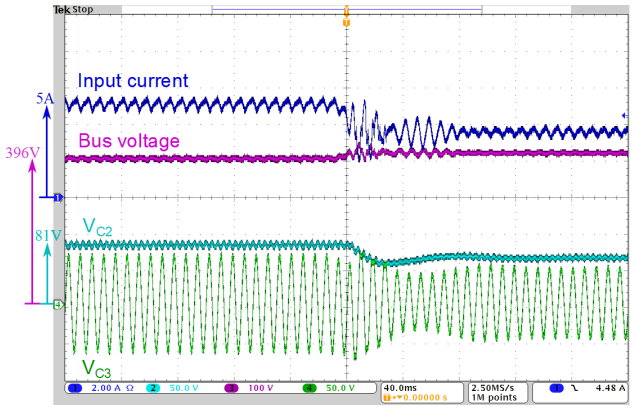


Figure 6.19: Energy buffer operation during a load step-down from 100% to 75%. The input current ripple becomes within specifications after 80 ms.

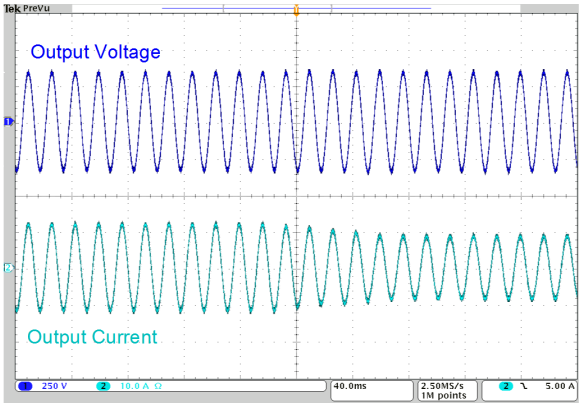


Figure 6.20: Inverter operation during a load step-down from 100% to 75%.

reducing the required capacitor volume by a factor of eight.

The combined inverter prototype successfully demonstrated a 216 W/in^3 power density with a rectangular volume of 9.26 in^3. A peak overall efficiency of 97.6% is achieved, including the power losses from control and cooling fan. The prototype meets all the specifications of the Google/IEEE Little Box Challenge, such as the current ripple, the load transient, the EMC and case temperature requirement, showcasing the capability of the multilevel converter design and the series-stacked active energy buffer.

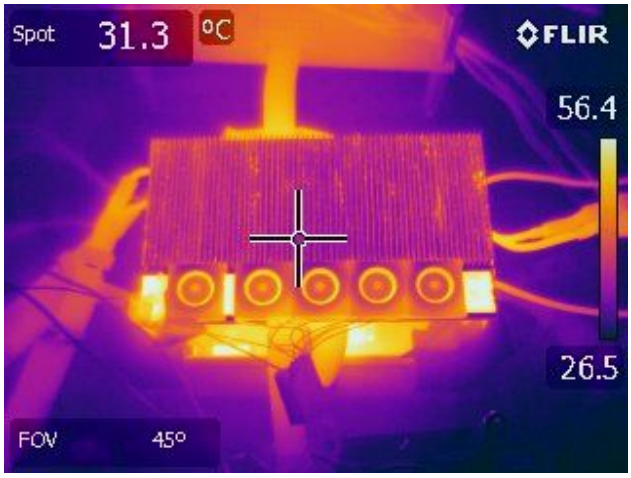


Figure 6.21: Thermal image of the inverter operating at full power (2 kW). The maximum temperature is 57 °C.

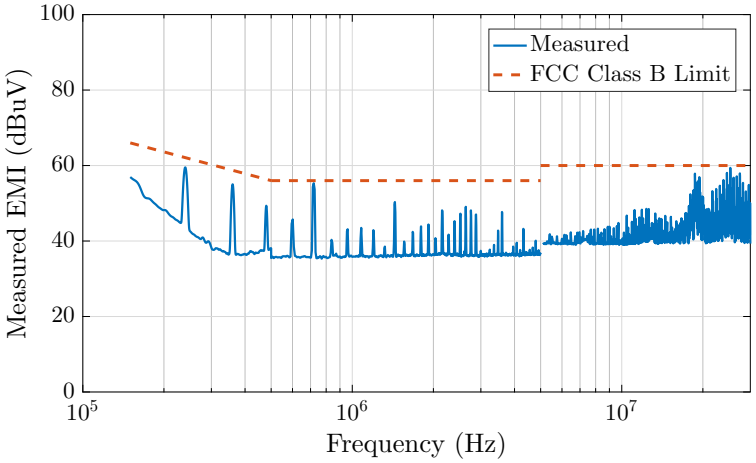


Figure 6.22: Conducted EMI measurement at full power (2 kW) from 150 kHz to 30 MHz, obtained using Tektronix RSA5126A real-time signal analyzer.

CHAPTER 7

SOFT-SWITCHING OPERATION OF HYBRID SC CONVERTERS

7.1 Motivation

For power converters, a higher frequency can usually yield a smaller passive component volume and an improved converter power density. The constant effort to push for a higher switching frequency has been recently aided by the commercialization of GaN switches. Compared to silicon MOSFETs, GaN FETs in general have a lower on-state resistance, output capacitance and gate capacitance, leading to the possibility of switching at a higher frequency while maintaining a high efficiency [87].

There are two major sources of switching losses in a typical power converter with an inductive load. The first is the loss of energy stored by the output capacitance of the switch when it turns on. This capacitance loss is given by

$$P_{\text{Coss}} = \frac{1}{2} f_{\text{sw}} C_{\text{oss}} V_{\text{ds}}^2, \tag{7.1}$$

where C_{oss} is the output capacitance and V_{ds} is the voltage across the switch before it turns on. Since the actual output capacitance of the device is highly non-linear, C_{oss} used here is the energy equivalent value, whose stored energy is the same as that stored by the actual capacitance. GaN switches have much lower such capacitance than MOSFETs [87], and thus a much lower resultant power loss. The other type of switching loss comes from the simultaneous existence of the voltage across the switch and the current through the switch during a switching transition, due to the MOSFET operating in the saturation region. This is because of the fact that when the switch turns on, the switch current first rises to the on-state current before the voltage across the switch can drop; and when the switch turns off, the voltage first rises before the current can drop. The power loss from the overlap can be approximated given by

$$P_{\text{overlap}} = \frac{1}{2} V_{\text{off}} I_{\text{on}} f_{\text{sw}} (t_{\text{turn-on}} + t_{\text{turn-off}}), \tag{7.2}$$

where V_{off} is the off-state voltage, I_{on} is the on-state current, and $t_{\text{turn-on}}$ and $t_{\text{turn-off}}$ are the duration for which the voltage and current overlap when the switch turns on and turns off, respectively. Note that Eq. (7.2) is an approximation suitable for certain kinds of switching transitions, and more details can be found in [88]. Usually, the turn-on time is much longer than the turn-off time,

and the output capacitance of the switch reduces the overlap during device turn-off. Therefore, the turn-on overlap loss is the dominating one. In general, the overlap times are proportional to the gate charges, $(Q_{\mathrm{gd}} + \frac{1}{2}Q_{\mathrm{gs}})$. GaN switches typically have gate charges that are much smaller than those of MOSFETs [87], and thus offer the possibility for a fast turn-on and turn-off transition, and a much lower overlap loss. However, fast transition time causes voltage ringing due to the parasitic inductance in the high $\mathrm{d}i/\mathrm{d}t$ loop. Therefore in practice, the transition time is usually intentionally slowed down by increasing the gate resistance, to increase the damping during the transition period. Even though the GaN switches have the advantages of smaller package inductance, especially with the flip-chip packaging [89], the parasitic inductance from the commutation loop, as well as the ESL from the decoupling capacitance, sets a lower limit on the transition times.

The slowed switch transition time owing to the parasitic inductance is especially prominent in a converter with distributed switches, such as the hybrid SC converters. For these converters, the high $\mathrm{d}i/\mathrm{d}t$ loop can be quite large, and can be difficult to confine through layout and decoupling techniques. For the flying capacitor multilevel converter presented in Chapter 6, a modular switching cell was designed to minimize the parasitic inductance by minimizing the commutation loop and strategic placement of small decoupling capacitors. However, due to the physical size of the decoupling capacitor, there was still a considerable amount of inductance in the switching loop, and a large gate resistance was needed to reduce the voltage ringing to accepted values. As a result, the loss breakdown in Fig. 6.15 shows that the overlap switching loss is dominant. Furthermore, for the hybrid Dickson converters presented in Chapter 4, due to the switched-capacitor configuration, an effective decoupling method cannot be easily obtained. Large gate resistance was used, which severely penalizes the efficiency. Therefore, in order to fully utilize the potential provided by GaN switches for high-frequency and high-efficiency operation, soft-switching techniques are employed on hybrid SC converters to minimize or eliminate the switching losses.

Unlike in hard-switching converters, the switches of soft-switching converters commutate naturally due to the load current, and thus do not have significant voltage-current overlap during the commutation period. Many soft-switching converters are derived from conventional PWM converters [90, 91]. In the quasi-resonant converters (QRC) [90], zero voltage switching (ZVS) is achieved by placing a capacitor in parallel with the switch to slow down the rising of the switch voltage during the turn-off; and zero current switching (ZCS) is achieved by slowing down the rising of current during turn-on with a small inductor connected in series. An additional resonant element is added to release the energy stored in the soft-switching enabling inductor or capacitor in a lossless manner. Other soft-switching converters based on PWM operation exist, such as quasi-square-wave (QSW) converters [92] and zero-voltage-transition (ZVT) converters [93].

Another type of soft-switching converter is the resonant converter [94, 95]. Unlike PWM-based soft-switching converters, resonant converters employ resonance over the entire switching period. Typical resonant converters are series-resonant converter, parallel-resonant converters, LCC converters and LLC converters [96]. These converters are usually optimized for a narrow operating range, and employ transformers to achieve a large voltage step-down or step-up ratio.

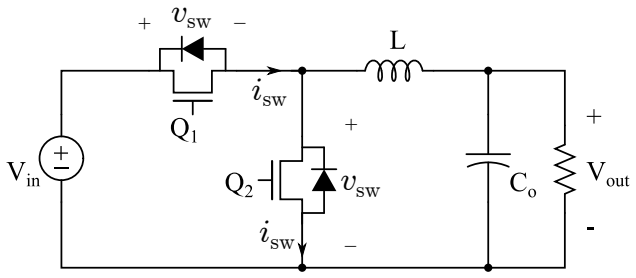


Figure 7.1: Schematic drawing of a buck converter.

Table 7.1: Direction of currents for the buck converter in CCM operation.

	deadtime	State 1	deadtime	State 2
L	+	+	+	+
Q1		+		
Q2	d		d	-

Since the hybrid converters such as the Dickson and FCML converters discussed in Chapters 4 and 5 use PWM technique to regulate the output voltage, the use of the inductor is very similar to conventional PWM converters. Therefore, existing techniques, such as quasi-resonant and quasi-square-wave ZVS switching can be applied. Section 7.2 examines the Dickson converter and the FCML converter for quasi-square-wave (QSW) operation. In addition, the soft-charging SC converters in ZCS resonant mode presented in Chapter 2 are modified to achieve ZVS operation in Section 7.3.

7.2 Quasi-Square-Wave Hybrid SC Converter

To turn on a switch with zero voltage switching, one sufficient condition is that the anti-parallel diode (or body diode diode) is conducting before the switch turns on. This condition demands that the current that flows through the switch is negative during the switch turn-on period. In this work, positive current is defined as current flowing from drain to source of the MOSFET. Take the buck converter in Fig. 7.1 as an example. The direction of the current and switches under CCM (continuous conduction mode) are shown in Table 7.1, where "-" represents a negative current, "+" represents a positive current, and "d" represents a current flowing through the body diode (which is also negative in the direction defined by the switch current). When the high side switch (Q_1) is conducting, its current is always positive, and thus switching loss exists when it turns on. On the other hand, the synchronous switch Q_2 always turns on when the current through it is negative and thus the synchronous switch can turn on with ZVS, provided that the dead-time is long enough for the inductor current to discharge the switching node capacitance, and subsequently turn on its body diode. On the other hand, with QSW operation, the inductor current ripple is designed to be large enough that the valley of the inductor current is below zero at the end of State 2. The negative current charges the device capacitance and forces the conduction of Q_1 body diode, and

Table 7.2: Direction of currents for the buck converter in QSW operation.

	State 1 end	deadtime	State 2 start	State 2 end	deadtime	State 1 start
L	+	+	+	-	-	-
Q1	+				d	-
Q2		d	-	+		

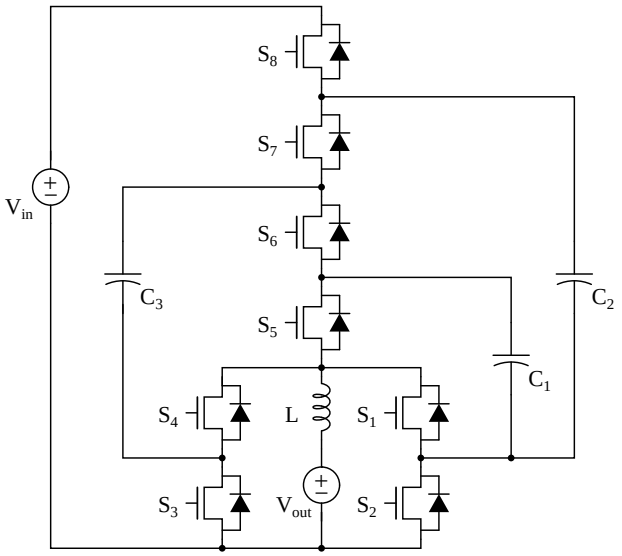


Figure 7.2: Schematic drawing of a hybrid Dickson converter.

thus Q_1 can turn on with ZVS in addition to Q_2. The current directions in QSW operation are shown in Table 7.2.

Here, we extend the concept of QSW for hybrid SC converters, using the Dickson converter as an example, whose schematic is reproduced in Fig. 7.2 with MOSFETs and their body diodes. In order to identify the hard-switched MOSFETs, the directions of current in each switch during each phase and deadtime in CCM operation are shown in Table 7.3. It can be seen that switches $S_1 - S_4$ turn on with negative currents, and thus their body diodes conduct during the deadtime so that the switches can turn on with ZVS. On the other hand, switches $S_5 - S_8$ have a positive current flowing through them, and thus their body diodes do not turn on during the deadtime, resulting in hard-switching. It can be deduced that, if the inductor current is reversed (i.e. the converter is running in boost mode), switches $S_1 - S_4$ would have positive current through them and have hard turn-on, while switches $S_5 - S_8$ would have soft turn-on.

With QSW operation, the current in the inductor has a large ripple by design, and thus reverses direction within each phase (changes from positive to negative in State 0 and from negative to positive in State 1 and State 2), as shown in shown in Table 7.4. It can be seen that now, all of the switches have a negative current through them, and thus all switches can turn on with zero voltage switching. The ZVS operation for state transitions from State 1 to State 0 and from State 0 to State 2 are shown in Fig. 7.3.

Table 7.3: Direction of current for the PWM Dickson converter in CCM operation.

Switch #	State 1	deadtime	State 0	deadtime	State 2	deadtime	State 0	deadtime	State 1
1	-	-	-	d		d	-	-	-
2		d	-	-	-	-	-	d	
3	-	-	-	d		d	-	-	-
4		d	-	-	-	-	-	d	
5	+								+
6					+				
7	+								+
8					+				

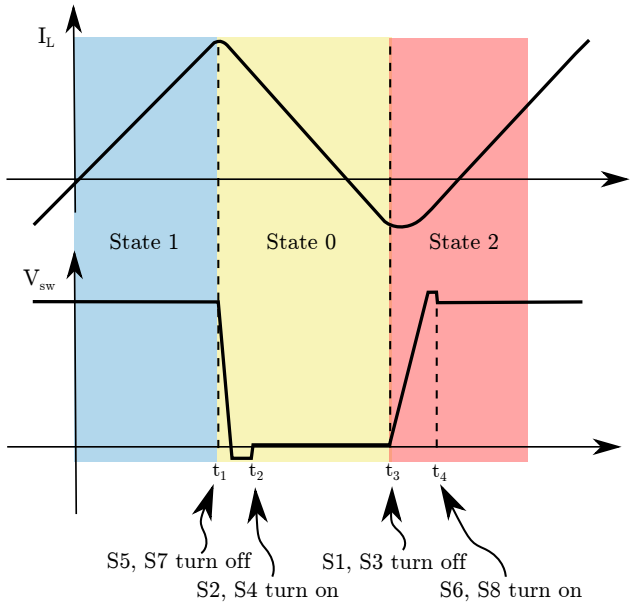


Figure 7.3: QSW operation of the PWM Dickson converter.

The Dickson converter prototype in Chapter 4 is modified to demonstrate the feasibility of the ZVS operation. The 5.6 μH inductor is replaced with a 1.0 μH inductor to increase the current ripple. Figure 7.4 shows the captured waveforms of the switching node voltage and the inductor current. It can be seen that for the soft-switched version, the switching node has a slow slope at both the rising and the falling edge transition, without an overshoot. In contrast, the hard-switched version shows significant drain-source voltage ringing in Fig. 4.9. The measured efficiencies of the Dickson converter in QSW operation are shown in Fig. 7.5.

The QSW Dickson converter inherits similar advantages and disadvantages as the QSW buck converter compared to their hard-switching counterparts. With ZVS operation, both C_{oss} loss and the overlap loss can be eliminated, at the expense of increased conduction loss and core loss. In addition, since the inductor current valley depends on the load conditions (V_{in}, V_{out}, I_{out}), complete ZVS cannot be satisfied at all times without adjusting the switching frequency. This can be seen from the droop in efficiencies in Fig. 7.5 as the load increases for the QSW mode, when the converter transitions from ZVS to hard-switching operation. The transition happens at higher load condition

Table 7.4: Current direction of the PWN Dickson converter in QSW mode of operation. For simplicity, only transition from State 1 to State 2 are shown. Transition from State 2 to State 1 is similar.

Switch number	State 1 (t1)	dead-time	State 0 (t2)	State 0 (t3)	dead-time	State 2 (t4)
1	-	-	-	+		
2		d	-	+	+	+
3	-	-	-	+		
4		d	-	+	+	+
5	+					
6					d	-
7	+					
8					d	-

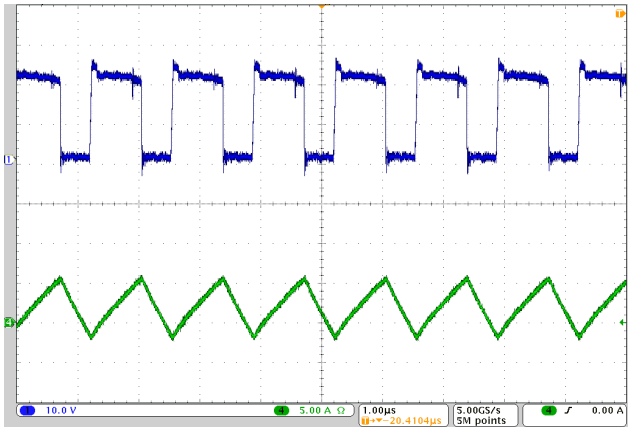


Figure 7.4: Captured waveforms of the switching node voltage (top) and inductor current (bottom) of the QSW Dickson converter. $V_{\text{in}} = 130$ V, $I_{\text{out}} = 3$ A.

if the switching frequency is reduced. Therefore, by varying the switching frequency, the QSW mode of operation can yield higher efficiency across the load range than the hard-switching mode.

While the QSW operation of the hybrid Dickson converter is demonstrated in this section, the method used (by investigating the current direction) can also be used to analyze all other PWM based hybrid SC converters. For example, the FCML converter can also achieve QSW ZVS operation while the series-parallel converter cannot.

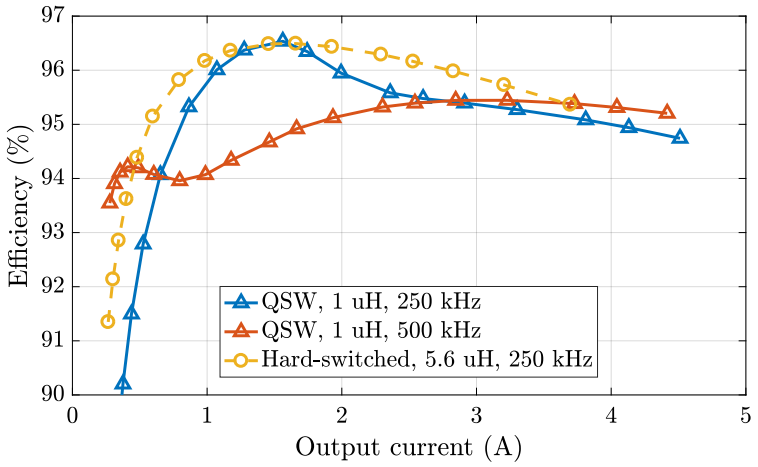


Figure 7.5: Measured efficiencies of the hybrid Dickson converter.

7.3 ZVS Resonant SC Converters

For the soft-charging SC converters shown in Chapter 2, it has been shown that the inductor current goes to zero at the phase transition, as shown in Fig. 2.10b, if the switching frequency is exactly the resonant frequency. Thus, ZCS operation can be easily achieved. With ZCS operation, the prolonged switching transition duration will not cause a significant increase in the overlap switching loss. In this section, it is demonstrated that ZVS operation is also possible, which in addition to having near zero overlap loss, also eliminates the output capacitance loss, and increases the efficiency.

A method to achieve ZVS using the resonant SC converter with the inductor at the output is to make the switching frequency slightly lower than the resonant frequency. In this way, a negative inductor current is again introduced during the switching transition, as shown in Fig. 7.6. To fulfill the ZVS requirement, the bottom switches need to turn on when the inductor current is positive, and the top switches need to turn on when the inductor current is negative.

In order to achieve full ZVS operation, there are a few requirements that the control signal needs to meet. First, the inductor needs to have enough energy to charge and discharge the switching node capacitance. Therefore, the inductor current, I_1 and I_2 need to satisfy

$$LI_1^2 \geq C_{\text{oss}} V_{\text{out}}^2 \tag{7.3}$$

$$LI_2^2 \geq C_{\text{oss}} V_{\text{out}}^2 \,, \tag{7.4}$$

where C_{oss} is the energy equivalent value of the output capacitance of the switches seen at the switching node. In addition, the duration, $t_2 - t_3$, needs to be long enough such that the desired inductor value I_2 can be reached. The second requirement is that the deadtime needs to be long

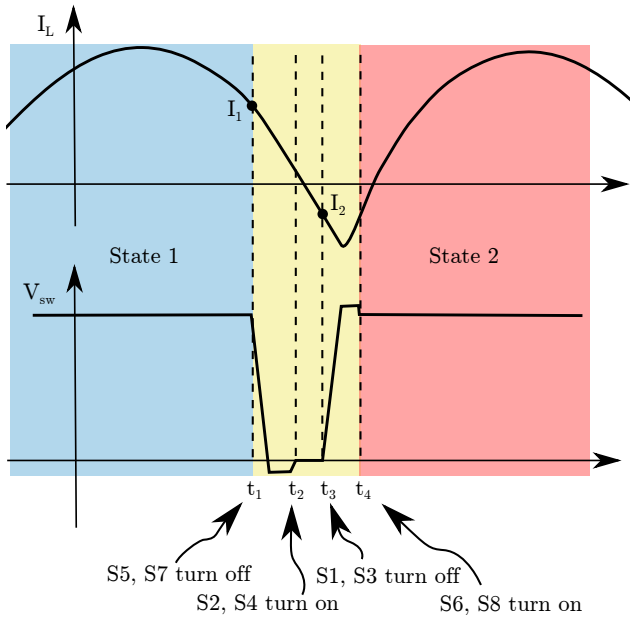


Figure 7.6: ZVS resonant operation of the Dickson converter, showing transition from State 1 to State 2. The transition time is exaggerated for clear illustration.

enough for the switch voltage to fall to zero before the other switches turn on. This means that the durations, $t_1 - t_2$ and $t_3 - t_4$, need to be long enough for the inductor to discharge and charge C_{oss}. Finally, the switching frequency needs to be adjusted so that the desired I_1, as well as the above requirements, is met. These conditions are summarized in Table 7.5.

Table 7.5: ZVS operation requirement.

Item	Requirement
I_1	Large enough to discharge C_{oss}
I_2	Large enough to charge C_{oss}
t_1 - t_2	Long enough for the inductor to discharge C_{oss}
t_2 - t_3	Long enough for the inductor current to reach I_2
t_3 - t_4	Long enough for the inductor to charge C_{oss}

The Dickson converter prototype in Section 4.4 is modified to operate at ZVS resonant mode with a 0.1 μH inductor. Due to the resonant operation, the converter has a fixed conversion ratio of approximately 6-to-1. The switching node voltage and the inductor current waveforms are shown in Fig. 7.7, which resembles the illustrated waveforms in Fig. 7.6. The lack of voltage ringing during state transitions indicates successful ZVS operation. The efficiencies of the converter operating at an input voltage of 108 V and a frequency of 375 kHz are plotted in Fig. 7.8 for both ZCS and ZVS operation. It can be seen that the efficiency under ZVS operation is much higher than that of the ZCS operation, especially at light and medium load, thanks to the elimination of the switching loss. At heavy load, where the conduction loss begins to dominate, the efficiency of the ZVS operation

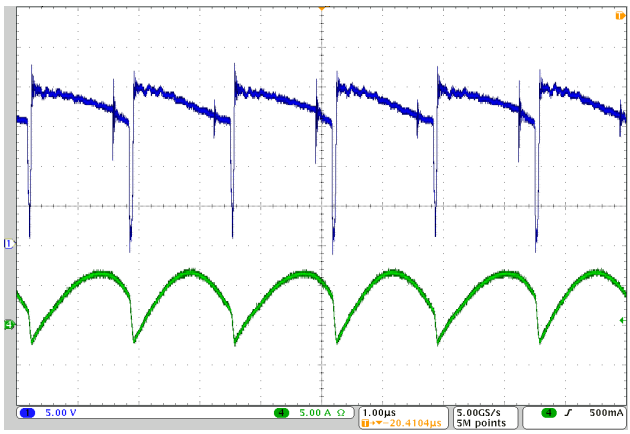


Figure 7.7: Captured waveforms of the switching node voltage (top) and inductor current (bottom) of the resonant Dickson converter in ZVS operation.

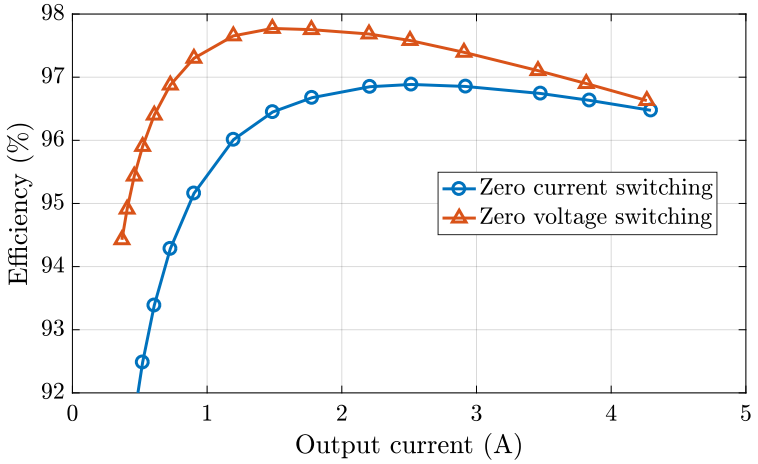


Figure 7.8: Measured efficiency for ZCS and ZVS operations. Input voltage is 108 V and the switching frequency is 375 kHz.

begins to approach that of ZCS operation, due to similar or a slightly higher total RMS current. It should be mentioned that the hardware prototype was designed for hard-switching PWM operation in Chapter 4, and not for ZVS operation. Should the switch selection be optimized (by choosing a lower $R_{\mathrm{ds,on}}$ value) for ZVS operation, the efficiencies of both the QSW and the resonant ZVS operation in this chapter are expected to be further improved.

Table 7.6 lists the inductor used for different operating modes. The selected inductors have a similar volume, resulting in a fair comparison of the converter efficiencies.

Table 7.6: Inductors used for the different operating modes of the hybrid Dickson.

	Hard-switched PWM	QSW PWM	ZCS and ZVS resonant
Part number	Coilcraft XAL7030-562	Coilcraft XAL7030-102	Coilcraft SLC7530S-101
Specification	5.6 μH, 28 mΩ	1.0 μH, 4.55 mΩ	0.1 μH, 0.123 mΩ
Dimension	7.5 x 7.5 x 3.1 mm	7.5 x 7.5 x 3.1 mm	7.5 x 6.7 x 3 mm

7.4 Chapter Summary

In this chapter, zero-voltage switching techniques for the hybrid converters are explored. For the PWM based hybrid converters, the QSW technique is implemented, which allows the inductor current to fall below zero to soft turn on the switches. The technique is demonstrated with the Dickson converter, and is also applicable to the FCML converter. In addition, a ZVS technique is proposed for the fixed-ratio hybrid converters. It has been shown that ZVS operation can achieve a much higher efficiency than ZCS operation, by eliminating the transistor output capacitance loss, while only introduces a minimal increase in conduction loss.

Since the ZVS operation shows great promise for the fixed-ratio hybrid converters, it would be useful to see whether other hybrid topologies can benefit from the same technique. For example, it is applicable to the cascaded 3-level converter in Section 3.1, due to its similar basic structure. In addition to the ZVS techniques investigated in this chapter, other soft-switching techniques can also be explored.

CHAPTER 8

PRACTICAL CHALLENGES WITH HYBRID SC CONVERTERS AND FUTURE WORK

While this work focuses on the fundamental analysis and comparison of active and passive device utilization of hybrid converters, it should be recognized that there are many practical issues associated with circuit implementations that can influence the topology selection and converter design as well. This chapter discusses some of the challenges and possible solutions. First, a survey of current capacitor technologies and their suitability for hybrid converters are presented Section 8.1. Capacitor voltage balancing problem is presented in Section 8.2. Finally, other circuit implementation challenges are presented in Section 8.3.

8.1 Practical Capacitor Selection

The design and selection of inductors for magnetic-based converters are well understood and practiced. For the hybrid converters, the inductor design is similar to that of the resonant converters for the fixed-ratio configuration, and is similar to that of a buck converter for the PWM configuration. In this section, practical aspects in selecting capacitors for hybrid converters are discussed.

Capacitors can be broadly categorized based on the dielectric technology used, such as electrolytic, film and ceramic. It has been shown in Section 3.2 that high energy density is the fundamental reason why the hybrid approach can achieve a higher efficiency and power density than magnetic-based converters. A plot of energy density against energy storage capability for different types of capacitors is shown in Fig. 8.1. It can be seen that film capacitors have an energy density that is one order of magnitude lower than that of ceramic or electrolytic capacitors, and therefore are inferior from a energy density point of view. However, electrolytic capacitors have a low RMS current limit (which comes from either dielectric loss or reliability constraint), and a high series inductance (ESL), both of which render electrolytic capacitors unsuitable for high frequency design. Therefore, for most designs, ceramic capacitors should be used. However, ceramic capacitors only come with small package sizes, as shown by the small total energy storage in Fig. 8.1, and thus for high power designs, film capacitors should be considered instead. The characteristics of the different capacitors are qualitatively compared in Table 8.1.

Ceramic capacitors are categorized into classes based on their dielectric properties [86]. Class I ceramic capacitors (such as C0G and U2J) have a smaller value variation and flat DC bias and temperature characteristics. These properties make Class I ceramic capacitors particularly suitable

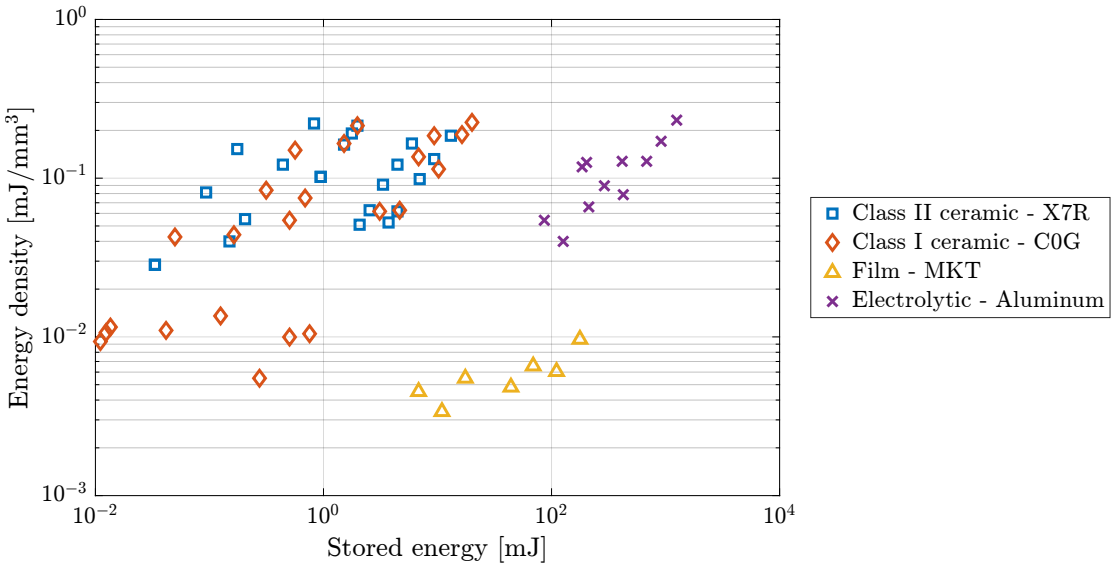


Figure 8.1: Plot of energy density against rated voltage. Dotted lines are the contour of the maximum energy density available.

Table 8.1: Capacitor technology comparison.

	Ceramic	Film	Electrolytic
ESR	small	medium	large
ESL	small	medium	large
RMS current rating	high	medium	low
Energy density	high	medium	high
Available size	small	small and large	large

for resonant hybrid SC converters, as they can easily meet the component matching requirement. Class II ceramic capacitors (such as X7R, X5R, X6S) are less precise, but offer a much larger energy density. The energy densities of X7R and C0G capacitors at different voltages are plotted in Fig. 8.2. It can be observed that at low voltages (< 400 V), the energy density of X7R capacitors can be an order of magnitude higher. On the other hand, the energy density of C0G capacitors increases as voltage increases, and becomes higher than that of X7R at 630 V. As a result, for high voltage designs, C0G (or other Class I) ceramic capacitors should be used. In addition to the constant capacitor values at difference DC bias and different temperature, the C0G capacitors also have a high Q of 1000 (vs. a typical value of 20 to 30 for X7R), which results in a much lower conduction loss and higher current rating. Therefore, even at lower voltages, Class I capacitors can be chosen if the capacitor size is loss limited, rather than energy storage limited.

For FCML and PWM hybrid SC converters, the inductors and capacitors are selected separately. The capacitors are selected based on the allowable voltage ripple, which is usually a few percentage of the nominal capacitor or switch voltage. In this case, the capacitor value variation has no effect on circuit operation, and has a marginal effect on performance. Therefore, Class II ceramics

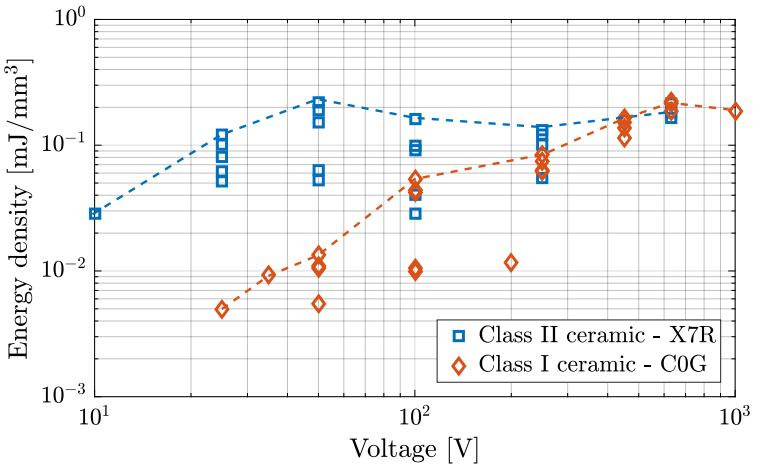


Figure 8.2: Plot of energy density against rated voltage. Dotted lines are the contour of the maximum energy density available.

with the highest energy density are preferable. The preferred capacitor technologies and their corresponding converter topologies are summarized in Table 8.2.

Table 8.2: Hybrid SC topologies and suitable capacitors.

	Resonant SC converter with series inductors	Resonant SC converters with output inductor	FCML and PWM Hybrid SC converters
Class I ceramic	•	•	
Class II ceramic		•	•

In summary, there is not a single type of capacitors that satisfies all the need for use in the hybrid converters. Therefore, developing a type of ceramic capacitor that has a higher energy density than Class I capacitors and a better dc bias characteristic than Class II capacitors can be extremely beneficial to the hybrid topologies.

8.2 Capacitor Balancing

As has been briefly discussed in Section 6.2, capacitor voltage balancing (capacitor voltages being at their nominal values) is crucial to the operation and performance of FCML converters. Previous literature on multilevel converters either focuses on capacitor balancing methods using active sensing and control, or on the dynamics of the self-balance property of PSPWM. While the active balancing methods can robustly regulate the flying capacitor voltages, the added complexity in sensing and control can sometimes be prohibitive, especially for high frequency operations and designs with a large number of levels. On the other hand, current understanding in the community of the self-balance property of the FCML converter is not enough to be relied upon without active

balancing, as many hardware prototypes show severe voltage imbalance [97]. In particular, while it is commonly cited that non-idealities in the circuits cause imbalance, it is not clear what are the non-idealities and to what extent their effects have on the capacitor balance. Therefore, it is useful as a future work to investigate the origins of the capacitor voltage imbalance in practical implementations of FCML converters, so that the responsible non-idealities can be understood, and consequently minimized in the circuit design stage.

In addition, the introduction of the inductor in hybrid SC converters makes the circuit under-constrained, and the capacitor voltages can no longer be determined by KVL as in conventional SC converters, so hybrid SC converters are also afflicted with the same issue of capacitor voltage balancing. Since PWM hybrid converters share a similar operation to FCML converters, it is proposed here that a similar approach as to the FCML converter can be used to model the self-balance mechanism for PWM hybrid SC converters, and that further exploration of the self-balance property can benefit both FCML converters and other hybrid converters. Furthermore, existing theories need to be extended to accommodate the asymmetric duty ratios for different phases, such as with the PWM-based series-parallel and Fibonacci converter introduced in Section 4.5. The self-balance property of fixed-ratio hybrid converters should also be analyzed, as their operation can differ from the PWM based ones.

8.3 Practical Circuit Implementations for Hybrid SC Converters

Since most of the hybrid converters use low voltage switches, whose voltage ratings depend on the capacitor voltages, the switch voltage ratings may be exceeded during the start-up process of the converter, before the capacitors are charged to their respective levels. In many applications where the input voltage can be slowly ramped up to the rated voltage, for example, when the converter is a second stage to a previous stage (e.g., voltage regulator module and intermediate bus architectures), no additional startup circuitry is required, since a soft-start procedure of the previous stage can be utilized. In other cases however, where the input voltage is not well controlled, start-up circuitry needs to be included for the multilevel and hybrid converters. For FCML and Dickson converters, one implementation is to use a top switch that is able to withstand the full input voltage while the flying capacitors charge up. The switch loss and size do not necessarily increase a lot, since for large step-down applications, the top switch has small RMS current and is the smallest switch. In addition, for high number of levels, the top switch is only one of the many switches. Another possible solution is to use a small start-up switch in parallel with a switch that turns on permanently after start-up, as demonstrated in [45,98]. This solution can be more efficient compared to the over-rated-top-switch approach, since there is no additional switching loss. For series-parallel converters, the first switch already has a high voltage rating, and thus can possibly accommodate a pre-charge process with an even smaller penalty.

Another challenge is to deliver power to the floating gate drivers, due to the large number of

switches used by the hybrid converters. In this work, state-of-the-art isolated power supply IC's are used to deliver power to each half-bridge gate driver. While the IC is much smaller compared to conventional isolated converters, thanks to the integrated transformer, its size is still larger than the switches and gate drivers it is powering, and its peak efficiency is quite low at 30% [99]. In [100, 101], modified bootstrap methods are proposed, which are demonstrated to be smaller, cheaper and more efficient than the transformer-based isolated power supply. While the methods were implemented on FCML converters, they can also be adopted by other hybrid topologies such as the Dickson and series-parallel converters. In addition, in [102], a monolithically integrated converter is implemented with all the auxiliary circuits on-chip, and successfully demonstrated high efficiencies across a wide operating range.

While the multilevel and hybrid SC converters add design complexity in terms of pre-charge, level-shifting and control, the challenges can be addressed by the innovation of circuit designers. Addressing the complexity of multilevel and hybrid converters is an on-going research, and can in many cases be worthwhile, given the potential efficiency and power density improvement.

CHAPTER 9

CONCLUSIONS

In this work, hybrid converters are explored, which use both capacitor and inductor in the power transfer process. It is proposed that these converters can achieve high power density and higher efficiency than conventional switched-capacitor converters and switched-inductor converters, thanks to high energy density of capacitors and high energy utilization of these components.

When applied to conventional switched-capacitor topologies, the hybrid approach is able to eliminate the charge sharing loss of the capacitors, thus leading to the reduction of capacitor size without penalizing the efficiency. A general method is presented that can be used to determine which switched-capacitor converter topology is able to achieve full soft-charging operation with a single inductor. It is found that among the classic topologies, series-parallel and Fibonacci converters are able to achieve full soft-charging operation with equal capacitor values. Dickson converter can only approach soft-charging operation with uneven capacitor values. Doubler and ladder converters cannot only achieve partial soft-charging operation. The Dickson converter is then analyzed in detail. A split-phase control technique is presented, which selectively charges and discharges the capacitors, such that full soft-charging operation can be achieved for the Dickson topology. Hardware prototypes are implemented, which show that the hybrid approach is able to achieve simultaneous high efficiency and power density.

Alternative placements for the inductor are then investigated. It is found that by placing an inductor in series with each of the flying capacitors, soft-charging operation can be achieved at the resonant frequency, for all of the existing SC topologies. However, practical constraints need to be observed before these topologies can be realized in hardware. A method to minimize the passive component volume for the hybrid converters is then proposed, by adjusting the capacitor and inductor values, subjected to the resonant frequency constraint. Using the minimized passive component volume, and the switch stress, different hybrid SC converters are compared.

Another drawback of conventional SC converters is the poor efficiency when the output voltage needs to be regulated. Here, a regulation technique using PWM switching is thus presented. This technique can be used on hybrid SC converters to achieve lossless voltage regulation, which is not possible with conventional SC converters. The proposed technique does not introduce additional components, and can achieve continuous voltage regulation. A 80-170 V input, 12 - 24 V output converter is implemented using GaN switches. The peak efficiency is 97%, and high efficiency can be achieved over the entire input and output operating range.

The similarity between the the flying capacitor multilevel (FCML) converters and the hybrid SC converters is then discussed. Both types of converters can be seen as a hybrid converter which uses both capacitors and inductors for energy transfer. A general framework to compare these converters, along with conventional buck converters, is proposed. In this framework, the power losses (including conduction loss and switching loss) are kept constant, while the total passive component volume is used as the figure of merit. The analysis shows that both the FCML converters and the hybrid Dickson converters have a much smaller total volume compared to buck converters, since they have a high utilization of the energy stored by both capacitors and inductors. Hardware prototypes have been implemented and the total reduction in passive components of the hybrid converters is similar to the results predicted by the theoretical analysis.

Based on the same principle of maximizing energy utilization of passive components, a 7-level FCML converter and an active energy buffer are designed and implemented for single phase dc-ac applications. The system achieves a combined power density of 216 W/in^3 and an efficiency of 97.4%, and compares favorably against other solutions in the setting of the Little Box competition.

A common technique to reduce converter size and improve efficiency at high frequency operation is to use soft-switching techniques. Zero voltage switching (ZVS) techniques are explored for hybrid converters, enabling potentials for an even higher power density by minimizing the switching loss and drain-source voltage ringing. Hardware prototypes from the previous sections are modified to support ZVS operation, and measured results show a significant efficiency increase for the fixed-ratio hybrid converter, and improved light-load efficiency for the PWM hybrid converter.

Some of the practical issues associated with the hybrid converter, such as practical capacitor selection, capacitor voltage balancing and other circuit implementation challenges. Future work based on these topics is also suggested.

In summary, this work demonstrated that both in theory and with hardware prototypes, hybrid converters utilizing both capacitors and inductors in the voltage conversion process can have performance superior to that of conventional SC and magnetics-based converters, due to their more efficient utilization of the switches and passive components. It is expected that these hybrid converters will find applications where high efficiency and power density are demanded, and are critical to the core function, so that the associated higher cost premium can be afforded.

APPENDIX A

SOFT-CHARGING OPERATION OF THE DICKSON CONVERTER

A.1 Derivation of the Charge Flow Vector for a 4-to-1 Dickson Converter

For the 4-to-1 Dickson converter in Fig. 2.12, the voltage change vector is defined as

$$\mathbf{\Delta v} = \begin{bmatrix} \Delta v_{in} \\ \mathbf{\Delta v_c} \\ \Delta v_{out} \end{bmatrix} = \begin{bmatrix} \Delta v_{in} \\ \Delta v_{c3} \\ \Delta v_{c2} \\ \Delta v_{c1} \\ \Delta v_{out} \end{bmatrix}. \tag{A.1}$$

Using the KVL equations defined in Eq. (2.33) and examining each loop in Fig 2.25, the following reduced loop matrices can be found:

$$\mathbf{A_{1a}} = \begin{bmatrix} 1 & -1 & 0 & 0 & -1 \\ 0 & 0 & 1 & -1 & -1 \end{bmatrix} \mathbf{A_{2a}} = \begin{bmatrix} 0 & 1 & -1 & 0 & -1 \\ 0 & 0 & 0 & 1 & -1 \end{bmatrix}$$
$$\mathbf{A_{1b}} = \begin{bmatrix} 0 & 0 & 1 & -1 & -1 \end{bmatrix} \quad \mathbf{A_{2b}} = \begin{bmatrix} 0 & 1 & -1 & 0 & -1 \end{bmatrix}. \tag{A.2}$$

In addition, since ΔV_{in} is considered zero for a constant voltage-source input, a row of $\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}$ can be added to each of the reduced loop matrices, resulting in the modified reduced loop matrix $\mathbf{A_{1am}}$, $\mathbf{A_{2am}}$, $\mathbf{A_{1bm}}$ and $\mathbf{A_{2bm}}$. The solution to (2.35) and (A.2) represents the possible change in values that the voltages of the circuit elements can take, constrained by KVL. By definition, the solution is the nullspace of each of the modified reduced loop matrix[1] , and is shown below.

[1]The nullspace can be found, for example, by using the *null* command in Matlab.

$$\mathbf{w^{1a}} = \begin{bmatrix} 0 \\ 0.1225 \\ 0.6325 \\ 0.7550 \\ -0.1225 \end{bmatrix} \begin{bmatrix} 0 \\ -0.6205 \\ 0.4472 \\ -0.1733 \\ 0.6205 \end{bmatrix} \tag{A.3}$$

$$\mathbf{w^{2a}} = \begin{bmatrix} 0 \\ -0.2124 \\ -0.6968 \\ 0.4844 \\ 0.4844 \end{bmatrix} \begin{bmatrix} 0 \\ 0.7449 \\ 0.3383 \\ 0.4066 \\ 0.4066 \end{bmatrix}$$

$$\mathbf{w^{1b}} = \begin{bmatrix} 0 \\ -0.5774 \\ 0.6667 \\ 0.3333 \\ 0.3333 \end{bmatrix} \begin{bmatrix} 0 \\ 0.5774 \\ 0.3333 \\ 0.6667 \\ -0.3333 \end{bmatrix} \begin{bmatrix} 0 \\ 0.5774 \\ 0.3333 \\ -0.3333 \\ 0.6667 \end{bmatrix} \tag{A.4}$$

$$\mathbf{w^{2b}} = \begin{bmatrix} 0 \\ 0.5774 \\ 0.7887 \\ 0 \\ -0.2113 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1.000 \\ 0 \end{bmatrix} \begin{bmatrix} 0 \\ 0.57740 \\ -0.2113 \\ 0 \\ 0.7887 \end{bmatrix}', \tag{A.5}$$

In addition, for soft-charging operation, the output voltage is able to change instantaneously to accommodate the change in the terminal voltage during phase transitions, and thus it is no longer a state in the linear circuit being analyzed. Therefore, Δv_{out} is excluded from the analysis. The bases corresponding to the capacitor voltage change ($\mathbf{\Delta v_c}$) are obtained from the middle elements

of the $\mathbf{w^i}$ vectors.

$$\mathbf{w_c^{1a}} = \begin{bmatrix} 0.1225 \\ 0.6325 \\ 0.7550 \end{bmatrix} \begin{bmatrix} -0.6205 \\ 0.4472 \\ -0.1733 \end{bmatrix} \tag{A.6}$$

$$\mathbf{w_c^{2a}} = \begin{bmatrix} -0.2124 \\ -0.6968 \\ 0.4844 \end{bmatrix} \begin{bmatrix} 0.7449 \\ 0.3383 \\ 0.4066 \end{bmatrix}$$

$$\mathbf{w_c^{1b}} = \begin{bmatrix} -0.5774 \\ 0.6667 \\ 0.3333 \end{bmatrix} \begin{bmatrix} 0.5774 \\ 0.3333 \\ 0.6667 \end{bmatrix} \begin{bmatrix} 0.5774 \\ 0.3333 \\ -0.3333 \end{bmatrix} \tag{A.7}$$

$$\mathbf{w_c^{2b}} = \begin{bmatrix} 0.5774 \\ 0.7887 \\ 0 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 1.000 \end{bmatrix} \begin{bmatrix} 0.57740 \\ -0.2113 \\ 0 \end{bmatrix}, \tag{A.8}$$

The charge vector for the 4-to-1 Dickson converter is defined as

$$\mathbf{q} = \begin{bmatrix} q_{in} \\ \mathbf{q_c} \\ q_{out} \end{bmatrix} = \begin{bmatrix} q_{in} \\ q_{c3} \\ q_{c2} \\ q_{c1} \\ q_{out} \end{bmatrix}. \tag{A.9}$$

Taking the Phase 1 schematic repeated in Fig. A.1 as an example, by applying KCL to Node 1, Node 2 and the ground node respectively, the following equations can be found.

$$\begin{cases} q_{c3} + q_{c1} - q_{out} = 0 \\ -q_{in} - q_{c3} = 0 \\ q_{in} + q_{c2} + q_{out} = 0 \end{cases} \tag{A.10}$$

The number of independent KCL equations for a circuit is given by $n-1$, where n is the number of nodes in the circuit [31]. Therefore, only three nodes from the circuit in Fig. A.1 are used to generate the KCL equations. Expressing these KCL equations using the matrix-vector product form given in (2.37) yields the reduced incidence matrix $\mathbf{B_{1a}}$. The same process is repeated for the other phases and all four of the reduced incidence matrices are given below:

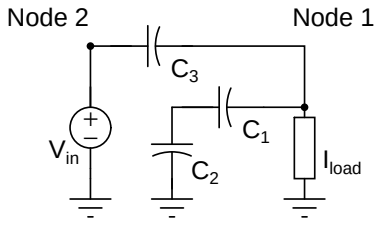


Figure A.1: Phase 1 of the split-phase Dickson converter.

$$\mathbf{B_{1a}} = \begin{bmatrix} 0 & 1 & 0 & 1 & -1 \\ -1 & -1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 \end{bmatrix} \tag{A.11}$$

$$\mathbf{B_{2a}} = \begin{bmatrix} 0 & -1 & -1 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$\mathbf{B_{1b}} = \begin{bmatrix} 0 & 0 & -1 & -1 & 0 \\ 0 & 0 & 0 & 1 & -1 \\ -1 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \tag{A.12}$$

$$\mathbf{B_{2b}} = \begin{bmatrix} 0 & -1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & -1 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 \end{bmatrix}. \tag{A.13}$$

The solution for the possible capacitor charge vectors that satisfy (2.37) and (A.13) are found to

be

$$\mathbf{u^{1a}} = \begin{bmatrix} 0.2443 \\ -0.2443 \\ -0.6109 \\ 0.6109 \\ 0.3666 \end{bmatrix} \begin{bmatrix} -0.5615 \\ 0.5615 \\ -0.0432 \\ 0.0432 \\ 0.6047 \end{bmatrix} \quad \mathbf{u^{2a}} = \begin{bmatrix} 0 \\ 0.6325 \\ -0.6325 \\ -0.3162 \\ -0.3162 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 0 \\ -0.7071 \\ -0.7071 \end{bmatrix}$$

$$\mathbf{u^{1b}} = \begin{bmatrix} 0 \\ 0 \\ -0.5774 \\ 0.5774 \\ 0.5744 \end{bmatrix} \qquad \mathbf{u^{2b}} = \begin{bmatrix} 0 \\ -0.5774 \\ 0.5774 \\ 0 \\ 0.5744 \end{bmatrix} \tag{A.14}$$

Similar to the preceding analysis of the voltage vector, only the elements that correspond to the charge through the capacitors ($\mathbf{q_c}$) are of interest. Again, the corresponding elements are grouped into a set of new vectors, defined as $\mathbf{u_c^i}$.

$$\mathbf{u_c^{1a}} = \begin{bmatrix} -0.2443 \\ -0.6109 \\ 0.6109 \end{bmatrix} \begin{bmatrix} 0.5615 \\ -0.0432 \\ 0.0432 \end{bmatrix} \quad \mathbf{u^{2a}} = \begin{bmatrix} 0.6325 \\ -0.6325 \\ -0.3162 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ -0.7071 \end{bmatrix}$$

$$\mathbf{u_c^{1b}} = \begin{bmatrix} 0 \\ -0.5774 \\ 0.5774 \end{bmatrix} \qquad \mathbf{u_c^{2b}} = \begin{bmatrix} -0.5774 \\ 0.5774 \\ 0 \end{bmatrix}. \tag{A.15}$$

Since each basis in (A.8), $\mathbf{w^i}$ represents a set of voltage changes, it can be related to the charge transferred by multiplying with the respective capacitor values. The result can be represented by

$$\mathbf{c} * \mathbf{w_c^i}, \tag{A.16}$$

where $*$ represents element-wise multiplication and $\mathbf{c}$ is given by

$$\mathbf{c} = \begin{bmatrix} C_3 \\ C_2 \\ C_1 \end{bmatrix}. \tag{A.17}$$

Since the $\mathbf{u_c^i}$ vectors in (A.15) represent the possible charge transfer constrained by KCL and the $\mathbf{c} * \mathbf{w_c^i}$, vectors in (A.16) represent the possible charge transfer due to the change in capacitor voltage constrained by KVL, the actual charge transfer values must satisfy both. To find the actual charge flow, the common space spanned by $\mathbf{u_c^i}$ and $\mathbf{c} * \mathbf{w_c^i}$ can be found, and is defined as $\mathbf{p_c^i}$. Therefore,

$\mathbf{p_c^i}$ can be expressed as

$$\mathbf{p_c^i} = \sum_j \beta_j \mathbf{u^i_{c(j)}} + \gamma_j \mathbf{c} * \mathbf{w^i_{c(j)}}, \tag{A.18}$$

where i is the phase number and j represents the jth basis. For $C_1 = C_2 = C_3$, (A.18) can be solved for β and γ, and the charge vectors are found as

$$\mathbf{p_c^{1a}} = \begin{bmatrix} 0.3714 \\ -0.1857 \\ 0.1857 \end{bmatrix} \quad \mathbf{p_c^{2a}} = \begin{bmatrix} 0.2000 \\ -0.2000 \\ 0.4000 \end{bmatrix}$$
$$\mathbf{p_c^{1b}} = \begin{bmatrix} 0 \\ -0.5774 \\ 0.5774 \end{bmatrix} \mathbf{p_c^{2b}} = \begin{bmatrix} -0.5774 \\ 0.5774 \\ 0 \end{bmatrix}. \tag{A.19}$$

These are the bases for the charge vectors which satisfy KCL and which also result in a capacitor voltage change that satisfies KVL. To find the actual values of the charge transferred, the steady-state condition given in (2.39) results in the following equation:

$$\alpha_{1a}\mathbf{p_c^{1a}} + \alpha_{2a}\mathbf{p_c^{2a}} + \alpha_{1b}\mathbf{p_c^{1b}} + \alpha_{2b}\mathbf{p_c^{2b}} = 0\,. \tag{A.20}$$

Equation (A.20) can be used to find the values of the α's. Finally, the actual charge flow vectors are given by

$$\mathbf{q_c^{1a}} = \alpha_{1a}\mathbf{p_c^{1a}},\ \mathbf{q_c^{2a}} = \alpha_{2a}\mathbf{p_c^{2a}}, \tag{A.21}$$
$$\mathbf{q_c^{1b}} = \alpha_{1b}\mathbf{p_c^{1b}},\ \mathbf{q_c^{2b}} = \alpha_{2b}\mathbf{p_c^{2b}}. \tag{A.22}$$

It should be noted that even though the coefficient values (α, β, γ) are obtained using only the basis whose elements correspond to the capacitors ($\mathbf{u_c^i}$ and $\mathbf{w_c^i}$), their values are also valid for the original basis, $\mathbf{u^i}$ and $\mathbf{w^i}$, which contains the elements corresponding to the input and output source. The overall charge vectors, which also contain the charge flow through the input and output element, can be found using the same set of coefficients and the resultant values are given as in (2.40).

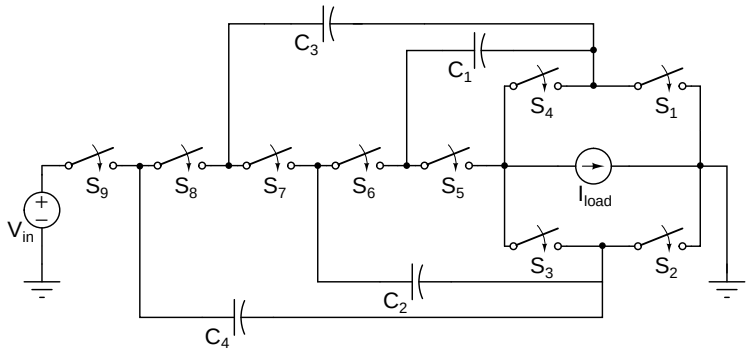
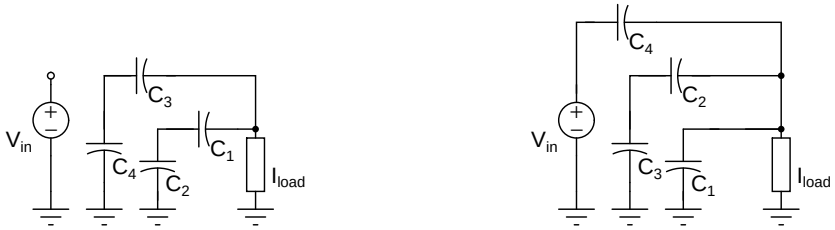


Figure A.2: 5-to-1 Dickson topology.



(a) Phase 1. (b) Phase 2.

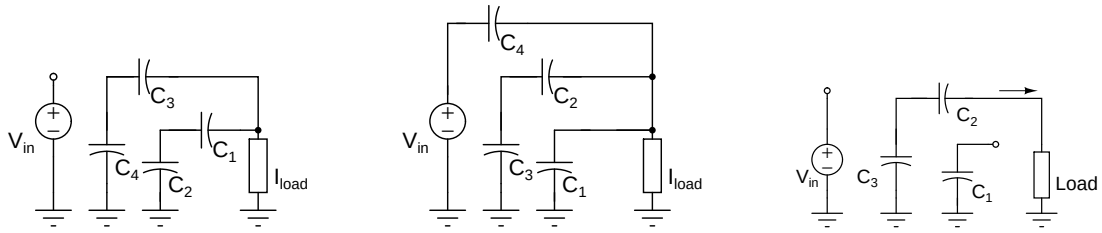
Figure A.3: Two-phase operation of a 4-to-1 Dickson converter.

A.2 Split-phase Control with Odd Conversion Ratios

A 5-to-1 Dickson converter is shown in Fig. A.2 and the corresponding two phases are shown in Fig. A.3. One flying capacitor (C_4) and one switch (S_9) are added to the 4-to-1 Dickson converter to increase to conversion ratio to 5:1. For a Dickson converter with an odd conversion ratio, such as in this case, only a single secondary phase is needed for the split-phase operation, as shown in Fig. A.4. This is because the outermost and innermost switches in the center string (S_9 and S_5) are controlled by the same switching function in an odd conversion ratio topology, rather than the opposite switching function in an even conversion ratio topology. The control signals are shown in Table A.1 and Fig. A.5. As can be seen, there is only one additional control signal (q_3) for split-phase operation, as opposed to two additional signals (q_3 and q_4) for Dickson converters with even conversion ratios.

Table A.1: Control of switches for split-phase 5-to-1 Dickson converter.

Switches	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1
Two-phase	q_1	q_2	q_1	q_2	q_1	q_2	q_1	q_2	q_1
Split-phase	$\boldsymbol{q}_3$	q_2	q_1	q_2	q_1	$\boldsymbol{q}_3$	q_1	q_2	q_1



(a) Phase 1a. (b) Phase 2a. (c) Phase b.

Figure A.4: Split-phase operation of a 5-to-1 Dickson converter.

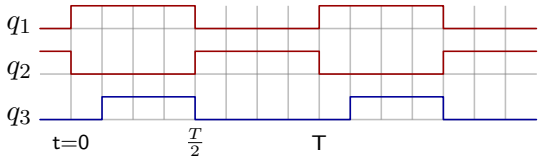


Figure A.5: Control diagrams for split-phase 5-to-1 Dickson converter.

APPENDIX B

EXACT DUTY RATIO OF THE SPLIT-PHASE CONTROL UNDER PWM OPERATION

The duty ratio for the split-phase operation has been calculated in Section 2.4, assuming the load is a constant current load. The split-phase duty ratio is independent of the load current. However, in practice, the inductor current is triangular with a dc offset, rather than being a constant dc value. In this section, the duty ratio of the split-phase is calculated given the duty ratio of the ideal case.

The duty ratios of the split-phase at different inductor current ripple values are plotted in Fig. B.1. It can be seen that with small relative inductor current ripple (i.e. large average inductor current and small absolute ripple), the split-phase duty approaches that calculated in Section 2.4. With relatively large inductor current ripple, the split-phase duty ratio decreases.

Since the relative inductor current ripple can be calculated on the fly using the PWM duty ratio, inductor value, switching frequency and the measurement of the input voltage, and the average inductor current, a feed-forward control can be used to choose the optimal split-phase duty ratio across the input, output voltage as well as the load range.

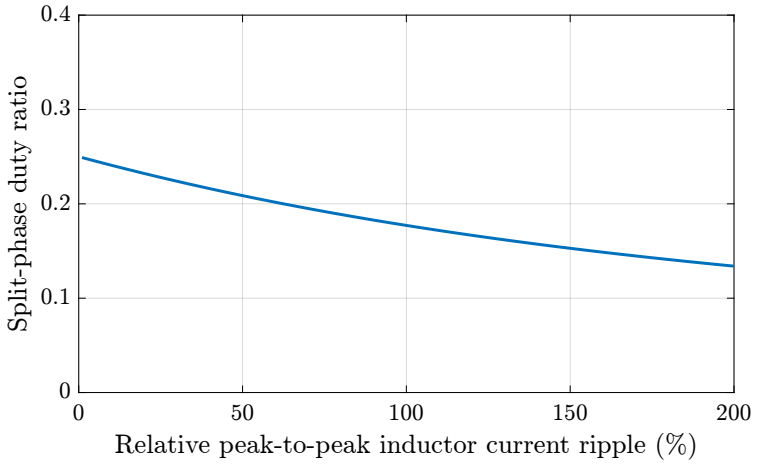


Figure B.1: Schematic of the 6-to-1 hybrid converter prototype.

APPENDIX C

ADDITIONAL CONVERTER LOSS AND MODELING CONSIDERATIONS.

C.1 The Switching Loss of Converters

There are two major sources of switching losses, the capacitance switching loss and the voltage-current overlap loss. These two losses will be investigated separately in this section.

The switching loss of a semiconductor device as a result of the drain-source capacitance is given by

$$\begin{aligned} P_{coss} &\propto f_{sw} C_{oss} V_{ds}^2 \\ &\propto f_{sw} Q_{oss} V_{ds} \,. \end{aligned} \tag{C.1}$$

The related device parameters of GaN switches (Q_{oss}, V_{ds}, R_{ds}) are collected from EPC. The $Q_{oss}V_{ds}$ values (capacitance switching loss metric) are plotted against GV_{ds}^2 in Fig. C.1, where G is $\frac{1}{R_{ds}}$. A linear best fit line is also plotted, which has a slope of 1.06 in log-log scale. This means that GV_{ds}^2 is linearly proportional to $Q_{oss}V_{ds}$, and that it is a good indication of the switching loss as a result from output capacitance discharge.

The switching loss of a semiconductor switch due to the voltage-current overlap during transition is given by

$$P_{\text{overlap}} \propto \sum^{\text{switches}} f_{sw} V_{ds} I_{ds} t_{tr}, \tag{C.2}$$

where $V_{ds}I_{ds}$ is the power dissipation during the transition and t_{tr} is the duration of the switch transition (commutation). Traditionally, t_{tr} is assumed to be proportional to Q_{gd}, since the gate-to-drain charge determines how fast the switch can be turned on. Provided that I_{ds} of the switches are the same across the topologies, $Q_{gd}V_{ds}$ can be used as metric to compare the overlap switching loss. The $Q_{gd}V_{ds}$ values against the GV_{ds}^2 product are plotted in Fig. C.2. The linear best fit line has a slope of 0.96 in log scale. This shows that GV_{ds}^2 is linear with respect to $Q_{gd}V_{ds}$, and thus a good representation of the overlap switching loss. This assumption that I_{ds} is the same for all switches is true for FCMC, but may not be true for a general hybrid SC topology. Therefore, a more accurate representation of the switching loss is $GV_{ds}^2 I_{ds}$, but is omitted in this appendix for simplicity.

In practice, especially for the fast GaN devices, the commutation time, t_{tr} is likely limited by the

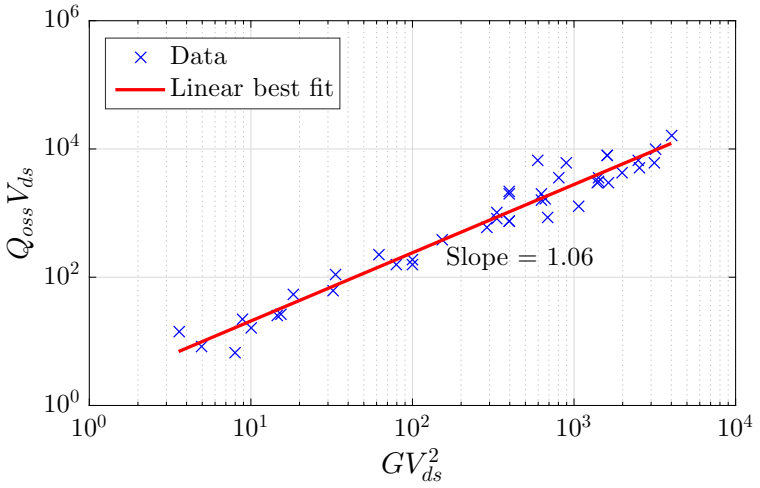


Figure C.1: Plot of capacitance switching loss metric against GV^2 product. Data obtained from EPC GaN switches.

Table C.1: Suitable metrics for switching losses.

Switching loss	Metric
Capacitance loss	GV_{ds}^2
Overlap loss (limited by Q_{gd}, same I_{ds})	GV_{ds}^2
Overlap loss (limited by Q_{gd})	$GV_{ds}^2 I_{ds}$
Overlap loss (limited by loop inductance)	$V_{ds}I_{ds}$

allowable voltage ringing during the switch transition, which depends on the parasitic inductance in the commutation loop, but not Q_{gd}. As a result, Q_{gd} may have limited influence on the switching loss. Therefore, in practice, a suitable metric for the switching loss is $V_{ds}I_{ds}$, assuming that t_{tr} is a constant value determined by the layout inductance. For the FCMC, there are $2(N-1)$ switches with voltage rating of $\frac{V_{\text{in}}}{N-1}$ and current rating of I_{load}. Thus, we have

$$\begin{aligned}\frac{\sum(VI)_{\text{FCMC}}}{\sum(VI)_{\text{buck}}} =& \frac{2(N-1)\times\frac{V_{\text{in}}}{N-1}I_{\text{load}}}{2\times V_{\text{in}}I_{\text{load}}} \\ =& 1,\end{aligned} \tag{C.3}$$

which is the same result given by Eq. (5.3).

Suitable metrics for switching losses are summarized in Table C.1. For simplicity, the sum of GV_{ds}^2 products are used as the overalls switching loss metric since it is a good indication of the capacitance switching loss and also partly reflects the overlap switching loss.

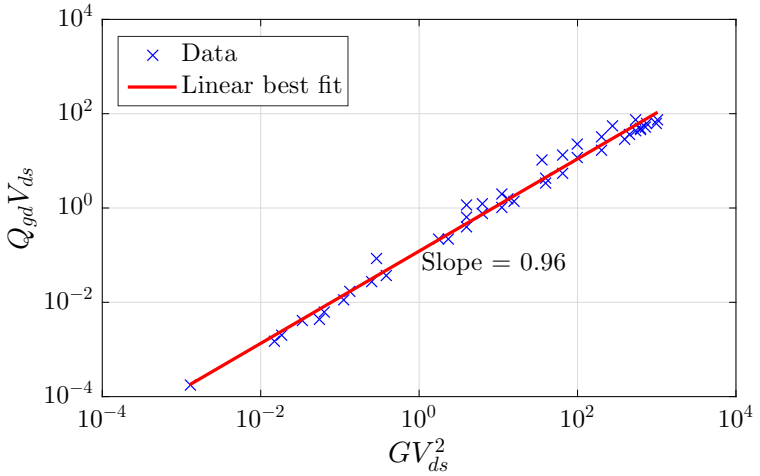


Figure C.2: Plot of overlap switching loss metric against GV^2 product. Data obtained from EPC GaN switches.

C.2 Inductor Volume Metric

The value of an inductor is given by

$$L = \frac{\mu n^2 A_c}{l_m}, \tag{C.4}$$

where μ is the permeability, n is the number of turns, A_c is the cross-sectional area of the core and l_m is the mean length of the magnetic path. The saturation current of an inductor is given by

$$I_{\text{sat}} = \frac{B_{\text{sat}} l_m}{\mu n}, \tag{C.5}$$

where B_{sat} is the saturation flux density. From Eq. (C.4) and Eq. (C.5), we obtain the expression for the LI^2 product of the inductor as

$$LI_{\text{sat}}^2 = \frac{B_{\text{sat}}^2 A_c l_m}{\mu}. \tag{C.6}$$

For a given core material and configuration, B_{sat} and μ are constant, and therefore the LI^2 product is proportional to the volume of the core, $A_c l_m$, which in turn is proportional to the volume of the inductor. It should be noted that here it is assumed that the size of the inductor is constrained by saturation, not by the core loss, which is often the case for the filter inductors used in PWM converters.

In order to validate the expression, the parameters of surface-mount inductors from the Coilcraft XAL and SER families are collected. The volumes of these inductors are plotted against their LI^2 product in Fig. C.3, where I is taken as the saturation current. The linear best fit line for the XAL series has a slope of 1.1, while the best fit line for the SER inductors has a slope of 0.95. This suggests the LI^2 product can be a good indication of the volume of an inductor.

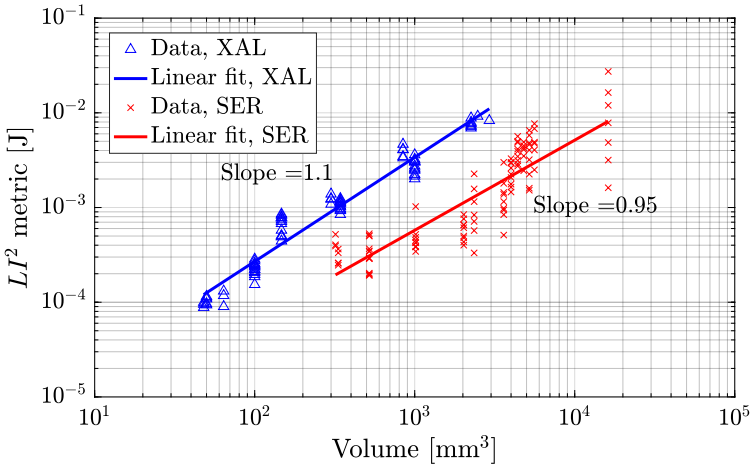


Figure C.3: Plot of LI^2 product against the inductor volumes. Data are obtained from Coilcraft inductors.

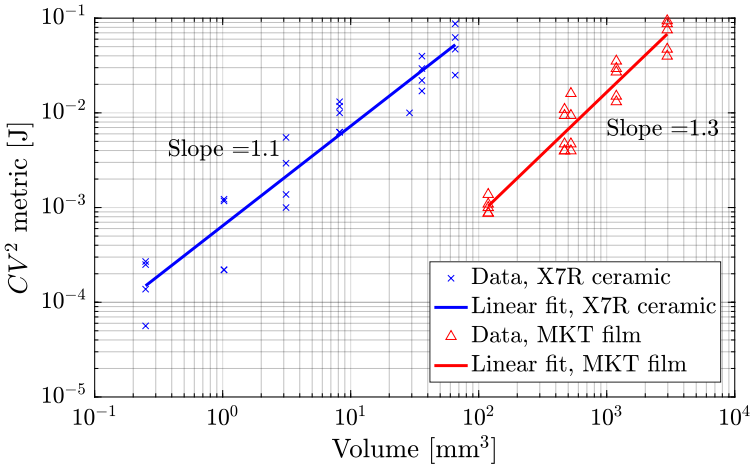


Figure C.4: Plot CV^2 product against the capacitor volumes. Data are obtained from TDK capacitors.

The following series of inductors is used in the plots: Coilcraft XAL4030, XAL4040, XAL5020, XAL5030, XAL5050, XAL7030, XAL7070, XAL1010, XAL1350, XAL1510, XAL1513; Coilcraft SER1360, SER1390, SER1408, SER1410, SER8050, SER8052, SER2915L.

C.3 Capacitor Volume Metric

The parameters of TDK multilayer ceramic capacitor X7R series as well as its metal film capacitor MKT series are collected. The volumes are plotted against CV^2 product in Fig. C.4. The slope of the linear best fit line is 1.1 for the X7R capacitors and the slope for the MKT capacitors is 1.3. Comparing Fig. C.3 and Fig. C.4, it can be seen that the X7R capacitors have on average 150 smaller volume for the same amount of energy stored than the XAL inductors.

Table C.2: Loss scaling of selected Vishay inductors.

FCMC	Part No.	Inductance	Ripple Frequency	I_{sat}	ΔI_L
2-level	IHLP-6767GZ-01	22 μH	100 KHz	23 A	4.8 A
3-level	IHLP-6767DZ-01	10 μH	200 KHz	19.5 A	4.6 A
4-level	IHLP-5050CE-01	5.6 μH	300 KHz	19 A	4.6 A
5-level	IHLP-4040DZ-01	3.3 μH	400 KHz	18.6 A	4.73 A
6-level	IHLP-3232DZ-01	2.2 μH	500 KHz	23 A	4.4 A

FCMC	Part No.	Core loss (W)	AC loss	DC loss	Total loss	Volume
2-level	IHLP-6767GZ-01	1.04 W	2.06 W	1.85 W	4.95 W	2140 mm^3
3-level	IHLP-6767DZ-01	0.80 W	2.28 W	1.80 W	4.89 W	1160 mm^3
4-level	IHLP-5050CE-01	0.76 W	1.56 W	1.26 W	3.58 W	592 mm^3
5-level	IHLP-4040DZ-01	0.66 W	1.43 W	0.93 W	3.03 W	474 mm^3
6-level	IHLP-3232DZ-01	0.48 W	0.34 W	1.48 W	2.30 W	290 mm^3

The following series of capacitors is used in the plots (not all parts in a series are used). MKT capacitors: TDK B32529, B32520, B32521, B32522, B32523; Ceramic capacitors: TDK X7R capacitors with case size 0402, 0603, 0805, 1206, 1812, 2220, each with voltage ratings at 16 V, 25 V, 35 V, 50 V, 100 V, 250 V, 630 V and 1000 V where applicable.

C.4 Inductor Core Loss Consideration

The proposed analytical framework neglects the core loss and ac loss. This section explores the scaling of these losses as the inductor size changes. A common empirical core loss formula is the Steinmetz equation [103] given by

$$P_{core} = \alpha f^{\gamma} \Delta B^{\beta} A_c l_m, \tag{C.7}$$

where α is a constant for each core material, γ is the exponent that reflects the frequency dependent behavior, β reflects the flux swing dependent behavior of the core loss, and $A_c l_m$ is proportional to the volume of the core. β usually has a range of 2 - 3 while γ has a range of 1 - 3. For multilevel converters, while the core loss density increases due to the increase in the ripple frequency as in the comparison method, the volume of the core decreases as A_c decreases (due to the reduction in the required inductance). Thus whether the overall core loss increase or decrease compared to buck converters depends on the exponent γ.

For multilevel converters in general, we have

$$P_{core,ml} = \alpha f_{ml}^{\gamma} \Delta B^{\beta} A_{c,ml} l_m, \tag{C.8}$$

$$= \alpha (\frac{f_{buck}}{K_f})^{\gamma} \Delta B^{\beta} (K_f K_d A_{c,buck}) l_m, \tag{C.9}$$

$$= P_{core,buck} \frac{K_d}{K_f^{\gamma-1}}, \tag{C.10}$$

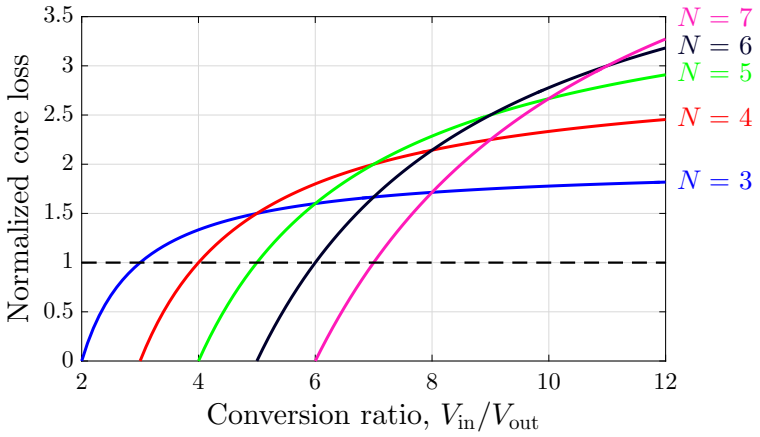


Figure C.5: Core loss of the FCMC inductor normalized by that of the buck converter. $(N-1)$ is the number of levels.

where K_f and K_d are as defined in Eq. (5.7). For the FCMC, the core loss normalized by that of a buck converter (i.e. $\frac{K_d}{K_f^{\gamma-1}}$) is plotted in Fig. C.5, by assuming a γ of 2. It can be seen that when the desired conversion ratio is close to $N-1$, i.e. when K_d factor is dominating, the core loss for the FCMC is smaller. When the desired conversion ratio is much larger than $N-1$, i.e. when K_f factor is dominating, the core loss for the FCMC can be larger than that of the buck converter. It should be noted that the scaling strongly depends on the value of γ. A γ value of 1 means that the core loss for the FCMC is always smaller, and a γ value of 3 can result in a core loss that is much higher than plotted in Fig. C.5. It should be noted here that a more accurate core loss frequency scaling can be obtained using the modified Steinmetz equation [104], which takes into account the triangular inductor current waveform at different duty ratios. The core loss for multilevel converter is expected to be lower than that given by the Steinmetz equation, since its duty ratio is closer to 0.5. In addition, a more rigorous inductor loss scaling is given in [105].

The core loss, ac loss and dc loss of selected inductors from Vishay IHLP family, evaluated at the same current ripple, are obtained from the manufacturer's website and are shown in Table C.2. The operating condition is 100 V to 12 V conversion with an average load current of 8 A. Smaller inductors are chosen for the FCMC converter with more levels according to Fig. 5.5. It can be seen that the core loss (and the total loss) actually decreases as the number of levels increases, despite operating at a higher frequency.

Therefore, while including the core loss in the analysis can yield more accuracy, omitting core loss does not necessarily yield a biased analysis favoring the multilevel converters.

REFERENCES

[1] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM converter power density barriers," in *2007 Power Conversion Conference - Nagoya*, April 2007, pp. P–9–P–29.

[2] S. Cheong, S. Chung, and A. Ioinovici, "Development of power electronics converters based on switched-capacitor circuits," in *[Proceedings] 1992 IEEE International Symposium on Circuits and Systems*, vol. 4. Institute of Electrical and Electronics Engineers (IEEE), 1992, pp. 1907–1910.

[3] J. Kimball, B. Kuhn, and P. Krein, "Increased performance of battery packs by active equalization," in *Vehicle Power and Propulsion Conference, 2007. VPPC 2007. IEEE*, Sept 2007, pp. 323–327.

[4] K. Sano and H. Fujita, "Voltage-balancing circuit based on a resonant switched-capacitor converter for multilevel inverters," *Industry Applications, IEEE Transactions on*, vol. 44, no. 6, pp. 1768–1776, Nov 2008.

[5] M. Chen, K. Afridi, and D. Perreault, "Stacked switched capacitor energy buffer architecture," *Power Electronics, IEEE Transactions on*, vol. 28, no. 11, pp. 5183–5195, Nov 2013.

[6] J. Dickson, "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *Solid-State Circuits, IEEE Journal of*, vol. 11, no. 3, pp. 374–378, Jun 1976.

[7] V. Ng, M. Seeman, and S. Sanders, "Minimum PCB footprint point-of-load dc-dc converter realized with switched-capacitor architecture," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, Sept 2009, pp. 1575–1581.

[8] Y. Ramadass and A. Chandrakasan, "Voltage scalable switched capacitor dc-dc converter for ultra-low-power on-chip applications," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, June 2007, pp. 2353–2359.

[9] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "Resonant switched-capacitor converters for sub-module distributed photovoltaic power management," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1189–1198, March 2013.

[10] S. Ben-Yaakov and A. Kushnerov, "Algebraic foundation of self adjusting switched capacitors converters," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 1582–1589.

[11] S. Ahsanuzzaman, J. Blackman, T. McRae, and A. Prodic, "A low-volume power management module for portable applications based on a multi-output switched-capacitor circuit," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, March 2013, pp. 1473–1479.

[12] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, March 2008.

[13] V. Ng and S. Sanders, "A high-efficiency wide-input-voltage range switched capacitor point-of-load dc-dc converter," *Power Electronics, IEEE Transactions on*, vol. 28, no. 9, pp. 4335–4341, Sept 2013.

[14] P. Lin and L. Chua, "Topological generation and analysis of voltage multiplier circuits," *IEEE Transactions on Circuits and Systems*, vol. 24, no. 10, pp. 517–530, Oct 1977.

[15] M. Makowski and D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, vol. 2, Jun 1995, pp. 1215–1221 vol.2.

[16] B. Arntzen and D. Maksimovic, "Switched-capacitor dc/dc converters with resonant gate drive," *Power Electronics, IEEE Transactions on*, vol. 13, no. 5, pp. 892–902, Sep 1998.

[17] J. Kimball, P. Krein, and K. Cahill, "Modeling of capacitor impedance in switching converters," *Power Electronics Letters, IEEE*, vol. 3, no. 4, pp. 136–140, Dec 2005.

[18] J. M. Henry and J. W. Kimball, "Practical performance analysis of complex switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 127–136, Jan 2011.

[19] M. D. Seeman, "A design methodology for switched-capacitor dc-dc converters," Ph.D. dissertation, EECS Department, University of California, Berkeley, may 2009. [Online]. Available: http://www.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-78.html

[20] S. Pasternak, C. Schaef, and J. Stauth, "Equivalent resistance approach to optimization, analysis and comparison of hybrid/resonant switched-capacitor converters," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–8.

[21] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *2008 IEEE Power Electronics Specialists Conference*, June 2008, pp. 4008–4015.

[22] R. Pilawa-Podgurski and D. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 7, pp. 1557–1567, July 2012.

[23] Y. Lei and R. C. N. Pilawa-Podgurski, "Soft-charging operation of switched-capacitor dc-dc converters with an inductive load," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, March 2014, pp. 2112–2119.

[24] S. Sanders, E. Alon, H.-P. Le, M. Seeman, M. John, and V. Ng, "The road to fully integrated dc-dc conversion via the switched-capacitor approach," *Power Electronics, IEEE Transactions on*, vol. 28, no. 9, pp. 4146–4155, 2013.

[25] N. Sturcken, E. O'Sullivan, N. Wang, P. Herget, B. Webb, L. Romankiw, M. Petracca, R. Davies, R. Fontana, G. Decad, I. Kymissis, A. Peterchev, L. Carloni, W. Gallagher, and K. Shepard, "A 2.5d integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer," *Solid-State Circuits, IEEE Journal of*, vol. 48, no. 1, pp. 244–254, Jan 2013.

[26] J. T. Dibene II, P. R. Marrow, C.-M. Park, H. W. Koertzen, P. Zou, F. Thenus, X. Li, S. W. Montgomery, E. Stanford, R. Fite, and P. Fischer, "A 400 amp fully integrated silicon voltage regulator with in-die magnetic coupled embedded inductors," in *Proc. Appl. Power Electron. Conf., Special Session on On-Die Voltage Regulators*, 2010.

[27] Y. Lei and R. Pilawa-Podgurski, "Analysis of switched-capacitor dc-dc converters in soft-charging operation," in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, June 2013, pp. 1–7.

[28] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650–5664, Oct 2015.

[29] H. Greinacher, "über eine methode, wechselstrom mittels elektrischer ventile und kondensatoren in hochgespannten gleichstrom umzuwandeln," *Zeitschrift für Physik*, vol. 4, no. 2, pp. 195–205, June 1921. [Online]. Available: https://doi.org/10.1007%2Fbf01328615

[30] J.-T. Wu and K.-L. Chang, "MOS charge pumps for low-voltage operation," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, Apr 1998.

[31] L. O. Chua, C. A. Desoer, and E. S. Kuh, *Linear and Nonlinear Circuits*. Mcgraw-Hill College, 1987.

[32] R. May, "Analysis of soft charging switched capacitor power converters," M.S. thesis, ECE Department, University of Illinois, Urbana Champaign, Aug 2013.

[33] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter," in *Control and Modeling for Power Electronics (COMPEL), 2014 IEEE 15th Workshop on*, June 2014, pp. 1–7.

[34] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 770–782, Jan 2016.

[35] J. Strydom, "Dead-time optimization for maximum efficiency," www.epc-co.com, Efficient Power Conversion Corporation, 2013. [Online]. Available: http://epc-co.com/epc/documents/papers/Dead-Time%20Optimization%20for%20Maximum%20Efficiency.pdf

[36] M. Araghchini, J. Chen, V. Doan-Nguyen, D. Harburg, D. Jin, J. Kim, M. S. Kim, S. Lim, B. Lu, D. Piedra, J. Qiu, J. Ranson, M. Sun, X. Yu, H. Yun, M. Allen, J. del Alamo, G. Des-Groseilliers, F. Herrault, J. Lang, C. Levey, C. Murray, D. Otten, T. Palacios, D. Perreault, and C. Sullivan, "A technology overview of the powerchip development program," *Power Electronics, IEEE Transactions on*, vol. 28, no. 9, pp. 4182–4201, 2013.

[37] J. Sun, M. Xu, Y. Ying, and F. Lee, "High power density, high efficiency system two-stage power architecture for laptop computers," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, June 2006, pp. 1–7.

[38] M. Chen, K. Afridi, S. Chakraborty, and D. Perreault, "Multitrack power conversion architecture," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[39] Y. Lei, W. C. Liu, and R. C. N. Pilawa-Podgurski, "An analytical method to evaluate flying capacitor multilevel converters and hybrid switched-capacitor converters for large voltage conversion ratios," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2015, pp. 1–7.

[40] B. Macy, Y. Lei, and R. Pilawa-Podgurski, "A 1.2 MHz, 25 V to 100 V GaN-based resonant Dickson switched-capacitor converter with 1011 W/in3 (61.7 kW/L) power density," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, March 2015, pp. 1472–1478.

[41] W. Li and X. He, "Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications," *Industrial Electronics, IEEE Transactions on*, vol. 58, no. 4, pp. 1239–1250, April 2011.

[42] T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, Jun 1992, pp. 397–403.

[43] M. Khazraei, H. Sepahvand, K. Corzine, and M. Ferdowsi, "A generalized capacitor voltage balancing scheme for flying capacitor multilevel converters," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, Feb 2010, pp. 58–62.

[44] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, June 2010, pp. 492–501.

[45] Y. Lei, C. Barth, S. Qin, W. C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. Pilawa-Podgurski, "A 2 kw, single-phase, 7-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[46] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 549–552, March 2006.

[47] W. Qian, F. Peng, and L. Tolbert, "Development of a 55 kW 3x dc-dc converter for HEV systems," in *Vehicle Power and Propulsion Conference, 2009. VPPC '09. IEEE*, Sept 2009, pp. 433–439.

[48] L. F. Costa, S. A. Mussa, and I. Barbi, "Multilevel buck/boost-type dc-dc converter for high-power and high-voltage application," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 3931–3942, Nov 2014.

[49] K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "Analysis of double step-down two-phase buck converter for VRM," in *INTELEC 05 - Twenty-Seventh International Telecommunications Conference*, Sept 2005, pp. 497–502.

[50] Y. Jang, M. M. Jovanovic, and Y. Panov, "Multiphase buck converters with extended duty cycle," in *2006 Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2006, pp. 38–44.

[51] P. S. Shenoy, M. Amaro, J. Morroni, and D. Freeman, "Comparison of a buck converter and a series capacitor buck converter for high-frequency, high-conversion-ratio voltage regulators," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7006–7015, Oct 2016.

[52] C. K. Cheung, S. C. Tan, C. K. Tse, and A. Ioinovici, "On energy efficiency of switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 862–876, Feb 2013.

[53] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$-pareto optimization and comparative evaluation of inverter concepts considered for the google little box challenge," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–5.

[54] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for hvdc-transmission," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, June 2008, pp. 174–179.

[55] A. Antonopoulos, L. Ängquist, S. Norrga, K. Ilves, L. Harnefors, and H. P. Nee, "Modular multilevel converter ac motor drives with constant torque from zero to nominal speed," *IEEE Transactions on Industry Applications*, vol. 50, no. 3, pp. 1982–1993, May 2014.

[56] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, Jan 2015.

[57] T. Modeer, C. Barth, Y. Lei, and R. Pilawa-Podgurski, "An analytical method for evaluating the power density of multilevel converters," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–5.

[58] J. Huang and K. Corzine, "Extended operation of flying capacitor multilevel inverters," *Power Electronics, IEEE Transactions on*, vol. 21, no. 1, pp. 140–147, Jan 2006.

[59] A. Parastar, A. Gandomkar, and J. K. Seok, "High-efficiency multilevel flying-capacitor dc/dc converter for distributed renewable energy systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7620–7630, Dec 2015.

[60] G. Lefevre and S. V. Mollov, "A soft-switched asymmetric flying-capacitor boost converter with synchronous rectification," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2200–2212, March 2016.

[61] A. B. Ponniran, K. Orikawa, and J. Itoh, "Minimum flying capacitor for n-level capacitor dc-dc boost converter," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3255–3266, July 2016.

[62] K. Kesarwani and J. T. Stauth, "Resonant and multi-mode operation of flying capacitor multi-level dc-dc converters," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2015, pp. 1–8.

[63] L. F. Costa, S. A. Mussa, and I. Barbi, "Multilevel buck/boost-type dc-dc converter for high-power and high-voltage application," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 3931–3942, Nov 2014.

[64] V. Dargahi, A. K. Sadigh, M. Abarzadeh, S. Eskandari, and K. A. Corzine, "A new family of modular multilevel converter based on modified flying-capacitor multicell converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 138–147, Jan 2015.

[65] J. Amini, A. H. Viki, A. Radan, and M. Moallem, "A general control method for multilevel converters based on knapsack problem," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 2–10, Jan 2017.

[66] A. M. Y. M. Ghias, J. Pou, G. J. Capella, P. Acuna, and V. G. Agelidis, "On improving phase-shifted PWM for flying capacitor multilevel converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5384–5388, Aug 2016.

[67] A. Shukla, A. Ghosh, and A. Joshi, "Capacitor voltage balancing schemes in flying capacitor multilevel inverters," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, June 2007, pp. 2367–2372.

[68] S. Qin, Y. Lei, C. Barth, W.-C. Liu, and R. Pilawa-Podgurski, "Architecture and control of a high energy density buffer for power pulsation decoupling in grid-interfaced applications," in *Control and Modeling for Power Electronics (COMPEL), 2015 IEEE 16th Workshop on*, July 2015, pp. 1–8.

[69] S. Qin, Y. Lei, C. Barth, W. C. Liu, and R. C. N. Pilawa-Podgurski, "A high power density series-stacked energy buffer for power pulsation decoupling in single-phase converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4905–4924, June 2017.

[70] C. McHugh, S. Sinha, J. Meyer, S. Pervaiz, J. Lu, F. Zhang, H. Chen, H. Kim, U. Anwar, A. Kumar, A. Sepahvand, S. Jensen, B. Choi, D. Seltzer, R. Erickson, D. Maksimovic, and K. K. Afridi, "A high power density single-phase inverter using stacked switched capacitor energy buffer," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 1947–1953.

[71] X. Zhao, L. Zhang, R. Born, and J. S. Lai, "Solution of input double-line frequency ripple rejection for high-efficiency high-power density string inverter in photovoltaic application," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 1148–1154.

[72] "Little box challenge detailed inverter specifications, testing procedure, and technical approach and testing application requirements for the little box challenge," Online, 2015. [Online]. Available: https://www.littleboxchallenge.com/pdf/LBC-InverterRequirements-20150717.pdf

[73] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: basic concepts and industry applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 955–964, Oct 2002.

[74] Y. Lei, Z. Ye, and R. C. N. Pilawa-Podgurski, "A GaN-based 97% efficient hybrid switched-capacitor converter with lossless regulation capability," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 4264–4270.

[75] Y. Sato, M. Iimura, Y. Dodo, and H. Obara, "A study on minimum required capacitance in flying capacitor multilevel converters for grid-connected applications," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 3502–3507.

[76] D. Reusch, A. Lidow, J. Strydom, and M. de Rooij, "Emerging applications for gan transistors," http://epc-co.com/epc/Portals/0/epc/documents/presentations/CSMantech2013_Emerging%20applications_Reusch.pdf, Efficient Power Conversion Corporation, online; accessed 27-September-2016.

[77] X. Yuan, H. Stemmler, and I. Barbi, "Self-balancing of the clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter under sub-harmonic PWM modulation," *Power Electronics, IEEE Transactions on*, vol. 16, no. 2, pp. 256–263, Mar 2001.

[78] A. Ruderman, B. Reznikov, and M. Margaliot, "Simple analysis of a flying capacitor converter voltage balance dynamics for dc modulation," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, Sept 2008, pp. 260–267.

[79] B. P. McGrath and D. G. Holmes, "Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 543–550, March 2008.

[80] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters - an overview," *Industry Applications, IEEE Transactions on*, vol. 50, no. 5, pp. 3569–3578, Sept 2014.

[81] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A high power density single-phase pwm rectifier with active ripple energy storage," *Power Electronics, IEEE Transactions on*, vol. 26, no. 5, pp. 1430–1443, May 2011.

[82] P. Krein, R. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *Power Electronics, IEEE Transactions on*, vol. 27, no. 11, pp. 4690–4698, Nov 2012.

[83] H. Hu, S. Harb, N. Kutkut, Z. Shen, and I. Batarseh, "A single-stage microinverter without using eletrolytic capacitors," *Power Electronics, IEEE Transactions on*, vol. 28, no. 6, pp. 2677–2687, June 2013.

[84] H. Wang, H.-H. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the dc-link capacitance in a capacitor-supported system," *Power Electronics, IEEE Transactions on*, vol. 29, no. 3, pp. 1163–1175, March 2014.

[85] S. Qin and R. Pilawa-Podgurski, "A power density optimization method for a power pulsation decoupling buffer in single-phase dc-ac converters," in *Energy Conversion Congress and Exposition (ECCE), 2016 IEEE*, Sept 2016.

[86] C. B. Barth, I. Moon, Y. Lei, S. Qin, C. N. Robert, and Pilawa-Podgurski, "Experimental evaluation of capacitors for power buffering in single-phase power converters," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 6269–6276.

[87] A. Lidow and J. Strydom, "Gallium nitride (gan)technology overview," www.epc-co.com, Efficient Power Conversion Corporation, 2012. [Online]. Available: http://epc-co.com/epc/Portals/0/epc/documents/papers/Gallium%20Nitride%20GaN%20Technology%20Overview.pdf

[88] P. Krein, *Elements of Power Electronics*. Oxford University Press, 1998.

[89] D. Reusch, "Impact of parasitics on performance," www.epc-co.com, Efficient Power Conversion Corporation, 2013. [Online]. Available: http://epc-co.com/epc/Portals/0/epc/documents/papers/Impact%20of%20Parasitcs%20on%20Performance.pdf

[90] F. C. Lee, "High-frequency quasi-resonant converter technologies," *Proceedings of the IEEE*, vol. 76, no. 4, pp. 377–390, Apr 1988.

[91] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters," *IEEE Transactions on Industrial Electronics*, vol. 42, no. 6, pp. 595–603, Dec 1995.

[92] V. Vorperian, "Quasi-square-wave converters: topologies and analysis," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 183–191, Apr 1988.

[93] G. Hua, C.-S. Leu, Y. Jiang, and F. C. Y. Lee, "Novel zero-voltage-transition PWM converters," *IEEE Transactions on Power Electronics*, vol. 9, no. 2, pp. 213–219, Mar 1994.

[94] R. Oruganti and F. C. Lee, "Resonant power processors, part i—state plane analysis," *IEEE Transactions on Industry Applications*, vol. IA-21, no. 6, pp. 1453–1460, Nov 1985.

[95] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 174–182, Apr 1988.

[96] B. Yang, "Topology investigation of front end dc/dc converter for distributed power system," Ph.D. dissertation, Virginia Polytechnic Institute and State University, 2003.

[97] J. S. Rentmeister, C. Schaef, B. X. Foo, and J. T. Stauth, "A flying capacitor multilevel converter with sampled valley-current detection for multi-mode operation and capacitor voltage balancing," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–8.

[98] R. C. Pilawa-Podgurski and D. J. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm CMOS," in *37th European Solid State Circuits Conference (ESSCIRC)*, 2011.

[99] Analog Devices Inc., "ADuM5210/ADuM5211/ADuM5212 Data Sheet," pp. 3–4, 2013. [Online]. Available: http://www.analog.com/media/en/technical-documentation/data-sheets/ADuM5210.pdf

[100] Z. Ye and R. C. N. Pilawa-Podgurski, "A power supply circuit for gate driver of GaN-based flying capacitor multi-level converters," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2016, pp. 53–58.

[101] Z. Ye, Y. Lei, W.-C. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Design and implementation of a low-cost and compact floating gate drive power circuit for GaN-based flying capacitor multi-level converters," in *2017 Thirty-Second Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 2925–2931.

[102] W. C. Liu, P. Assem, Y. Lei, P. K. Hanumolu, and R. Pilawa-Podgurski, "10.3 a 94.2switched-capacitor dc-dc converter with wide continuous conversion ratio in 65nm CMOS," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 182–183.

[103] C. P. Steinmetz, "On the law of hysteresis," *Proceedings of the IEEE*, vol. 72, no. 2, pp. 197–221, Feb 1984.

[104] J. Reinert, A. Brockmeyer, and R. W. A. A. D. Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified steinmetz equation," *IEEE Transactions on Industry Applications*, vol. 37, no. 4, pp. 1055–1061, Jul 2001.

[105] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2009, pp. 1–14.