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# ANALYSIS OF ON-CHIP CLOCK DISTRIBUTION SYSTEMS IN HIGH SPEED SYSTEMS

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The problem of estimating the clock skew and net charging time of on-chip clock distribution systems in single chip and multiple chip high speed gallium arsenide and silicon systems is described. Given a set of technology specifications, a number of clock driver designs along with their sensitivity to process variations, and the ability to accurately predict conductor capacitances a method is proposed to select the optimal conductor width, conductor level, and clock distribution net. The proximity of adjacent conductors to the clock net, i.e., the wiring distribution the clock net resides in, is shown to be an important factor when estimating on-chip clock skew. This is especially true in gallium arsenide systems due to the prevalence of capacitive coupling.

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# Analysis of On-Chip Clock Distribution Systems in High Speed Systems[†]

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# 1. Introduction

Most systems designed today are synchronous systems. At the heart of the synchronous system is the system-wide clock signal. A fundamental problem in high speed synchronous systems is how to distribute the clock signals. The clock distribution imposes two constraints on the system. First, the clock skew, the variation in the time the clock signal arrives at the clocked elements, shrinks the available clock period time [1]. Second, the clock period must be sufficiently large to allow the clock distribution net time to charge and discharge. Proper characterization of the clock distribution system is vital to the designs of high speed systems.

The larger the clock skew in the system, the larger the clock period must become to account for the uncertainty of the arrival of the clock signal at the clocked elements. The clock skew, $\delta$, of a system is determined by several factors [2]:

(1) differences in line lengths or path lengths to the various clocked elements,

(2) differences in the line parameters that determine the line time constant, i.e., process variations,

(3) differences in the device threshold voltages of the receiving gate of the clocked elements,

(4) differences in the delays through any active elements inserted in the line.

A common technique proposed to minimize clock skew is to eliminate the differences in the line lengths to the various clocked elements [2, 3].

In our analysis it is emphasized that each factor of clock skew should not be considered separately. For example, we will show that a clock net with equalized path lengths could in fact have a larger clock skew than an alternate clock distribution system or net. The notation $\delta(PL, CR, PV, AE, DT)$ refers to the clock skew as a function of path length, $PL$, crossovers, $CR$,

process variations, $PV$, active elements, $AE$, and device threshold, $DT$. Crossovers of other signal conductors over and under the clock distribution net are also considered to stress their impact on the clock skew and the net charging time.

We will distinguish between the skew of a single chip system, $\delta_{SC}$, and the skew of a multiple chip system, $\delta_{MC}$. Differentiation between the two types of skew is important since in a multiple chip system, the reduction in the single chip clock skew may cause an increase in the multiple chip skew. The term clock skew refers to the maximum clock skew of the system being analyzed.

The analysis will begin by considering the clock skew due to varying path lengths, $\delta(PL)$. The remaining factors of skew will be successively added and their impact will be discussed. We will concentrate on high speed systems. In such systems the use of high resistivity materials such as polysilicon and diffusion will be avoided since these materials add considerable delay to the clock distribution net and result in pessimistic skew values [2, 3]. Although these materials will be avoided, the methods which will be presented do not preclude their use. A number of design issues will be examined, namely, the substrate type, the conductor width and spacing, the conductor level, and the clock distribution net. Two substrate types will be considered, gallium arsenide, GaAs, and silicon, Si.

The paper is organized as follows. In section two the characterization of the clock net conductors is presented. In section three the analysis conditions are set. Afterwards, the skew and the net charging time as a function of path length and then crossovers are discussed. In section four the remaining factors of skew, process variations, active elements, and device threshold, are presented. The results are discussed in section five and the conclusion follows in section six.

# 2. Conductor Characterization

## 2.1. Modeling the Interconnect

On-chip interconnects have distributed capacitance, $c$, inductance, $l$, and resistance, $r$. The line inductance can be neglected even for very fast signal rise times as long as the driving impedances are larger than the line characteristic impedance so that no ringing or overshoot occurs [4]. Once the line impedance becomes greater than the driving impedance transmission line analysis techniques must be used [5]. We will approximate the distributed line with T-networks [6]. The driving device of the line is approximated by its average output impedance *Rdev* and the line is terminated in $Co$, the input capacitance of the receiving device.

The Elmore delay [4, 7] will be employed as an estimate of the delay. Given a branched network, the delay from the input to node $i$ may be defined as

$$T_i = \sum_k C_k R_{ki} \tag{2.1}$$

where $C_k$ is the lumped capacitance at node $k$ and $R_{ki}$ is the total resistance of the portion of the unique path between the input and $i$ that is common with the unique path between the input and $k$. The Elmore delay provides a simple yet useful means to analyze various clock distribution nets with respect to conductor spacing, conductor level, and substrate type .

## 2.2. Capacitance Calculation

The accurate prediction of interconnect capacitance is key to the design of VLSI high performance logic circuits. To this end, two- and three-dimensional capacitance calculation tools have been developed [8, 9, 10]. All capacitances presented in this paper are calculated using CAP2D [10]. The dimensions used are shown in the simplified cross sections of a conductor on GaAs and on Si in

Fig. 2.1.

The capacitance of the middle conductor for a set of five parallel, equally spaced with separation $S$ and width $W$, $W = S$, first level metal (FLM) conductors, and for a set of five second level metal (SLM) conductors is plotted in Fig. 2.2. The capacitance of a single line is also shown. In the analysis which follows, the capacitances are per unit length (pF/cm) and will be referred to as capacitances rather than capacitances per unit length. Observe that the capacitance of both SLM conductor configurations is less than the capacitance of their FLM counterparts, since the conductors are farther away from the ground plane. Also, the impact of line-to-line coupling is significant even for relatively wide conductors on GaAs (apparent from the difference in the single conductor capacitance versus the multiple conductor capacitance).

Since the capacitance of a conductor may depend significantly on the proximity of adjacent conductors, it is instructive to study the effects on conductor capacitance when the proximity of adjacent conductors varies [11]. In the cases analyzed (Table 2.1), the conductor under consideration is the middle conductor from the original set of five parallel conductors. In Table 2.1 the

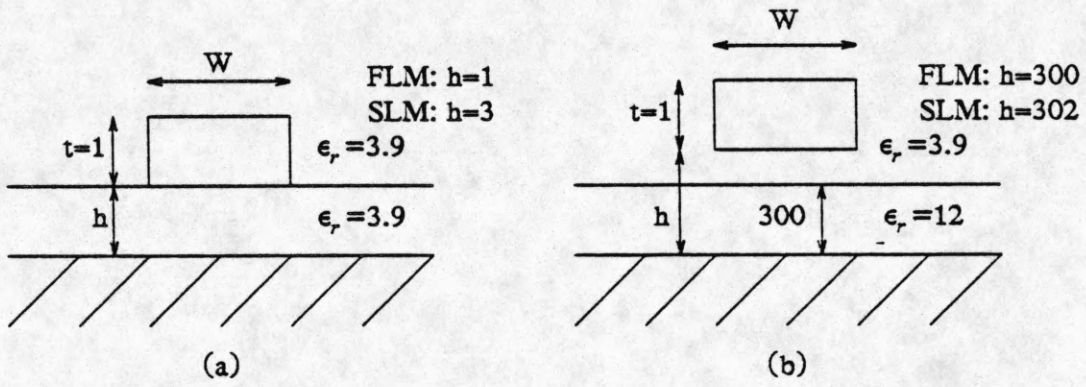


Fig. 2.1. Cross section of a conductor on (a) Si (b) GaAs.

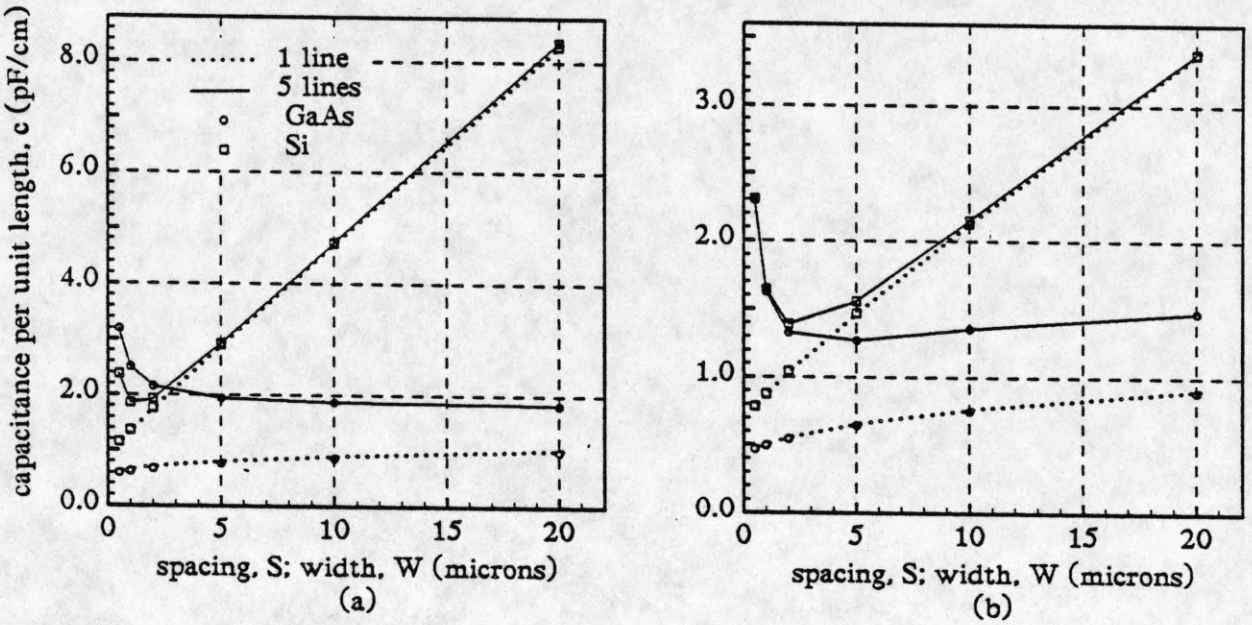


Fig. 2.2. Capacitance per unit length of multiple and single conductors on Si and on GaAs versus conductor width and spacing (a) FLM (b) SLM.

Table 2.1. Adjacent conductor removal.

| case | conductors missing | |
|---|---|---|
| | right | left |
| 0 | 0 | 0 |
| 1 | 1 | 0 |
| 2 | 1 | 1 |
| 3 | 2 | 1 |
| 4 | 2 | 2 |

number in the column labeled "right" indicates the number of adjacent conductors removed from the right side of the conductor under consideration. Two situations will be analyzed. An example is shown in Fig. 2.3. In the first situation five conductors are always present. Thus, right=1, left=0 specifies that the nearest conductor to the conductor under consideration has been moved to the right outermost conductor position. In the second situation an adjacent conductor is removed completely from the system. If, for a given case, the capacitance of situation one is greater than the

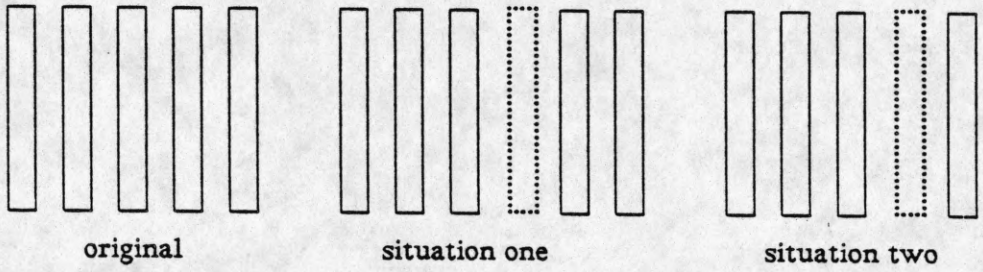


Fig. 2.3. Example of Case 1 of Table 2.1 (the dotted conductor is missing).

capacitance of situation two, then long range coupling is present.

Fig. 2.4 shows that long range coupling effects on GaAs are indeed significant. Also of importance is the size of the decrease in conductor capacitance when adjacent conductors are removed. For conductors on Si with large widths and spacings, negligible coupling occurs. On the other hand, for all conductors on GaAs and for conductors on Si with small conductor width and spacing the presence of adjacent conductors affects the conductor capacitance.

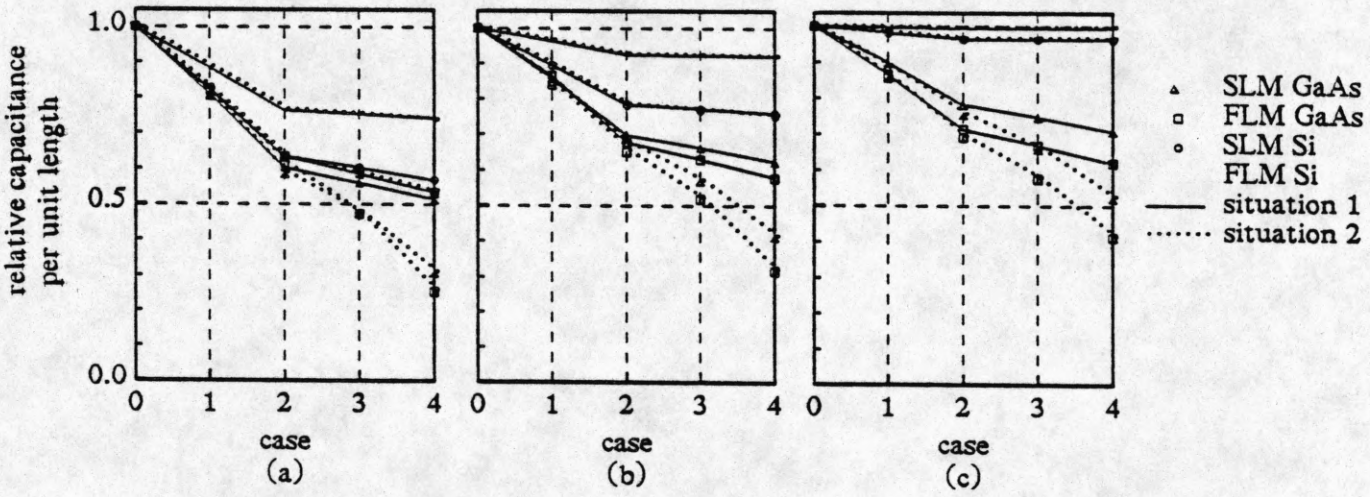


Fig. 2.4. Relative capacitance per unit length for conductors on GaAs and on Si versus the cases of Table 2.1 (a) W=S=1 (b) W=S=2 (c) W=S=6.

# 3. Clock Net Analysis

## 3.1. Problem Formulation

In order to determine the effects of clock net layout on clock skew and net charging time, eight clock distribution nets will be analyzed. The clock nets connect sixteen evenly spaced clocked elements on a 1 cm by 1 cm chip. The even spacing of the clocked elements makes this work applicable to systolic arrays. Unfortunately, most VLSI systems do not contain regularly spaced clock points. The clock distribution system may be hierarchical in design [12] and/or it may be part of an automated place and wire system. The analysis which follows, however, is applicable to all types of designs.

The eight nets under consideration are shown in Fig. 3.1. N1 is an H-tree which has been favored in the literature as reducing clock skew since the paths to each clocked element have equal length [2, 3]. N4 and N5 are common in design; both are perimeter fed and start connecting clock points immediately. N1, N2, and N3 are contingent upon a package technology which allows the nets to be fed from the center of the chip. N6, N7, and N8 are N1, N2, and N3, respectively, with an additional feed line to the center point to enable the nets to be fed from the perimeter of the chip.

In the preceding section it was shown that the proximity of adjacent conductors affects the capacitance of a given conductor. Since it is probable that clock distribution nets on VLSI chips contain adjacent conductors of varying proximity, a number of wiring distributions, which may be superimposed on any of the clock nets in Fig. 3.1, will be studied. For example, if coupling is present between adjacent conductors, a clock net residing in a dense wiring distribution will have a higher clock net conductor capacitance than a clock net residing in a sparse wiring distribution. To

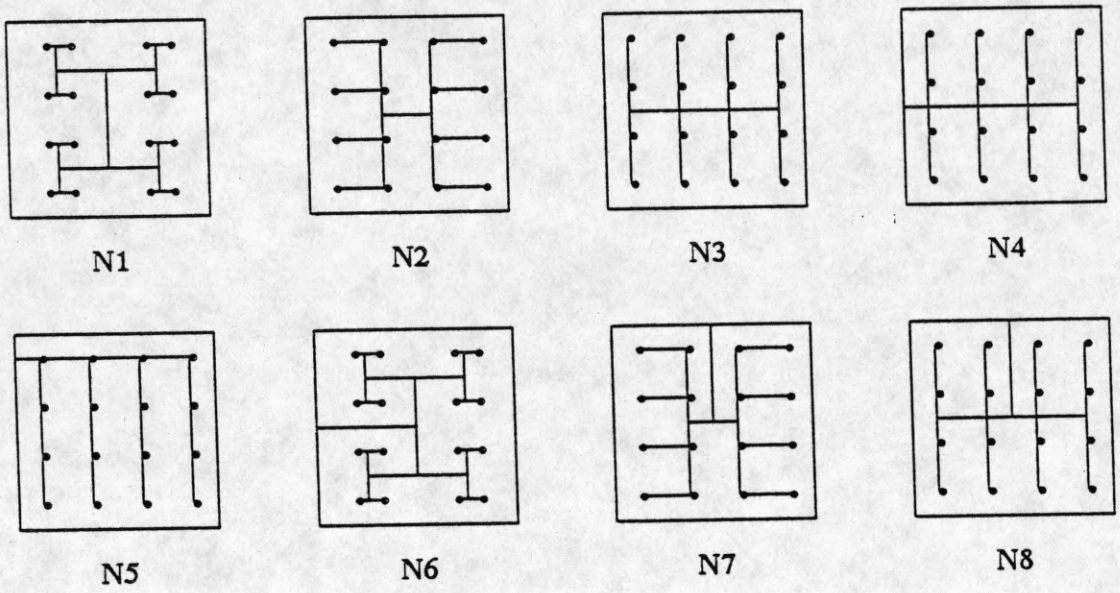


Fig. 3.1. Eight clock distribution nets.

emulate a decrease in wiring density, the cases of Fig. 2.4 (situation one) and the capacitance of an isolated conductor will be used (see Table 3.1).

The six wiring distributions are shown in Fig. 3.2. WD-A and WD-B are uniform wiring distributions with capacitive values representing the opposite ends of the spectrum, that is, the

Table 3.1. Wiring densities.

| case | wiring density |
|---|---|
| 0 | 100% |
| 1 | 80% |
| 2 | 60% |
| 3 | 40% |
| 4 | 20% |

capacitance of an isolated conductor, WD-B, and the capacitance of a conductor surrounded by multiple conductors, WD-A. WD-C and WD-D represent gate array type wiring distributions where the center of the chip is the area most densely populated by wires. WD-C represents a gradual change in wiring density while WD-D represents a more abrupt change in wiring density. WD-E and WD-F can be thought of as distributions occurring in a floor planned chip where a dense wiring distribution is found on one side of the chip and a less densely populated distribution is found on the other side.

### 3.2. Differences in Path Length

Delay equations obtained through the Elmore delay provide insight as to the contribution of each component of the skew and net charging time. Table 3.2 contains equations of $\tau(PL)$, the net

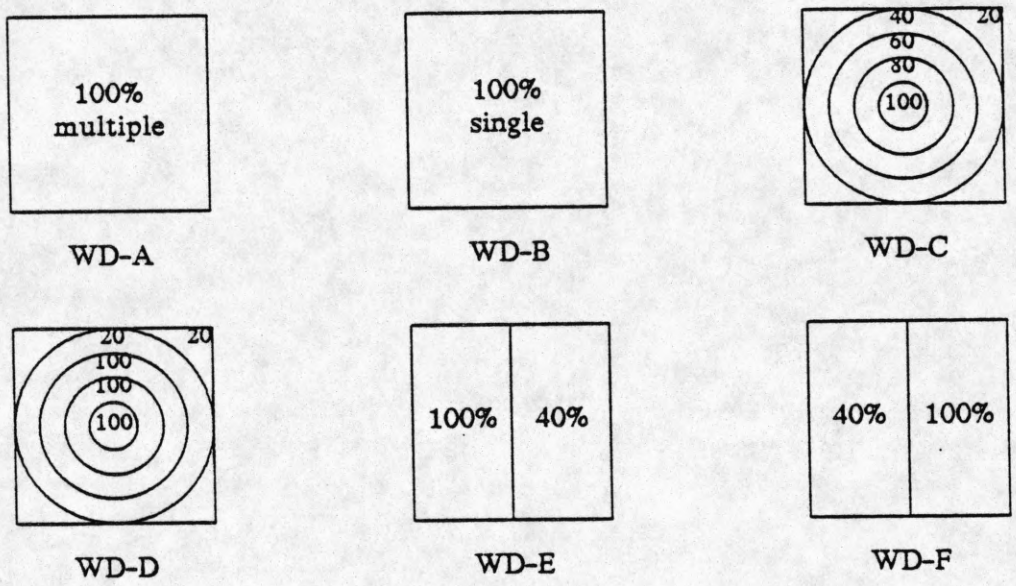


Fig. 3.2. Six wiring distributions.

charging time as a function of path length, and of $\delta_{SC}(PL)$, the single chip skew as a function of path length, for uniform wiring distributions such as WD-A and WD-B. The conductors are modeled using eight T-networks per cm. When comparing N1, N2, and N3 with N6, N7, and N8, respectively, the skews are not affected by the inclusion of the feed line to the perimeter of the chip, while $\tau(PL)$ is affected since the additional resistance of the perimeter feed must be summed over all of the capacitors in the network.

In the examples presented, the conductors are assumed to be aluminum with $\rho = 3\ \mu\Omega{-}cm$ and are charged through $Rdev = 500\Omega$. The input capacitance, $Co$, is assumed to be 30 fF. The single chip skew resulting from varying path lengths is shown in Fig. 3.3(a) and (b) and the net charging time is shown in Fig. 3.3(c) and (d) for two FLM conductor widths. Since the single chip skews due to path length of N1, N2, and N3 are equal to N6, N7, and N8, respectively, the latter are not shown. As expected, given a wiring distribution, the skews of the center-fed nets, N1, N2, and N3, are consistently lower than the skews of the side-fed nets, N4 and N5, and the skew decreases for increasing conductor widths. Also notice the differences in skew and net charging time, given a net type, across the wiring distributions. This can be attributed to coupling between

Table 3.2. $\delta_{SC}(PL)$ and $\tau(PL)$ of clock nets with uniform wiring distributions.

| Net | $\tau(PL)$ | $\delta_{SC}(PL)$ |
|---|---|---|
| N1 | Rdev [36C + 16Co ] + R [102C + 54Co ] | 0 |
| N2 | Rdev [30C + 16Co ] + R [58C + 36Co ] | R [16C + 12Co] |
| N3 | Rdev [30C + 16Co ] + R [66C + 40Co ] | R [32C + 20Co] |
| N4 | Rdev [31C + 16Co ] + R [250C + 136Co ] | R [184C + 100Co] |
| N5 | Rdev [31C + 16Co ] + R [277C + 152Co ] | R [216C + 120Co] |
| N6 | Rdev [40C + 16Co ] + R [406C + 182Co ] | 0 |
| N7 | Rdev [34C + 16Co ] + R [314C + 164Co ] | R [16C + 12Co] |
| N8 | Rdev [34C + 16Co ] + R [322C + 168Co ] | R [32C + 20Co] |

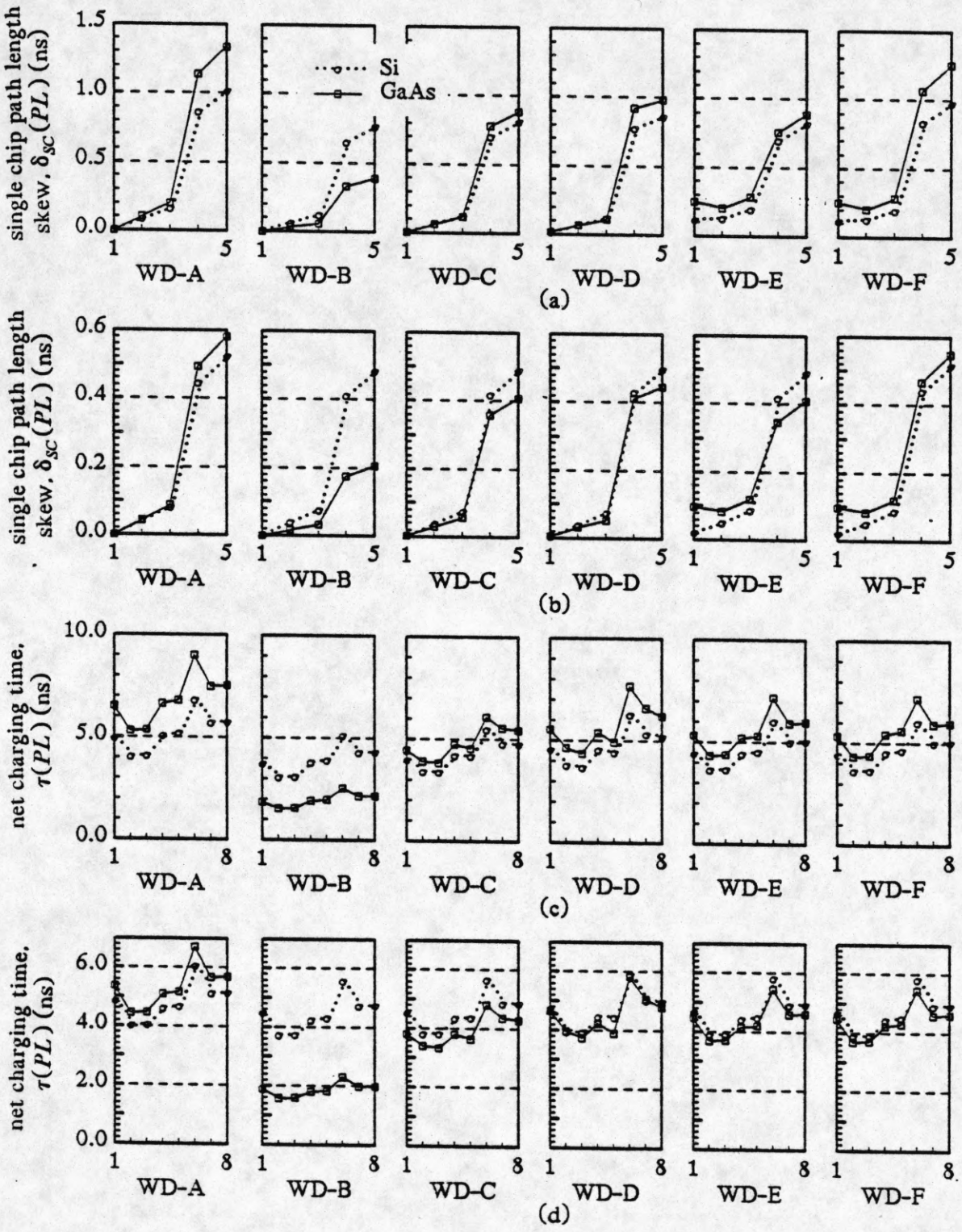


Fig. 3.3. FLM single chip path length skew and net charging time versus net type and wiring distribution: (a) W=S=1 (b) W=S=2 (c) W=S=1 (d) W=S=2.

adjacent conductors.

The net charging time is important not only because it is a limiting factor in the clock period. Varying values of $\tau(PL)$ on different chips contribute to the multiple chip skew. The skew of the multiple chip system, $\delta_{MC}(PL)$, can be found by taking the difference between the delay of the furthest clocked element of the higher $\tau(PL)$ net and the delay of the closest clocked element of the lower $\tau(PL)$ net. This is merely

$$\delta_{MC}(PL) = \tau_U(PL) - \tau_L(PL) + \delta_{SC_L}(PL) \tag{3.1}$$

where $U$ and $L$ refer to *upper* and *lower*, respectively.

If a multiple chip system contains chips with identical net types and wiring distributions then $\delta_{MC}(PL) = \delta_{SC}(PL)$. However, if the system contains identical nets with varying wiring distributions the skew may be more. The multiple chip systems in Fig. 3.4 contains identical nets with two types of wiring distributions, WD-A and WD-C. Even though the capacitance of conductors on GaAs is lower than the capacitance of conductors on Si, given a net and conductor width, the difference in capacitance between the two nets is higher (for the two wiring distributions chosen)

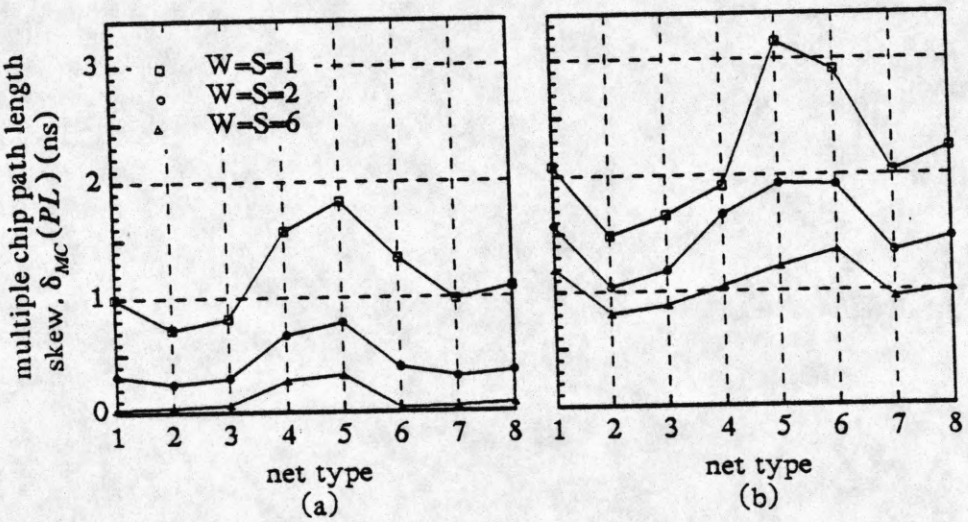


Fig. 3.4. FLM multiple chip skew due to path length for a system containing two wiring distributions, WD-A and WD-C, versus net type: (a) Si (b) GaAs.

for conductors on GaAs, again, due to capacitive coupling. Thus, in this case, the path length skew is higher in the GaAs system.

### 3.3. Crossover Capacitance

Another component of capacitance which must not be neglected is the crossover capacitance. To calculate this term, a three-dimensional capacitance calculation tool is required. Since such a tool was not available, we will demonstrate the effects of crossover capacitance on clock skew and net charging time with a value of 1.5 fF/crossover for a conductor width and spacing of $W = S = 2$. The results may be scaled for varying capacitive values as well as for the total number of crossovers per unit length.

Referring back to the Elmore delay definition it is evident that the impact of crossover capacitance on skew, $\delta_{SC}(CR)$, and net charging time, $\tau(CR)$, can be considered separately since the crossover capacitance is modeled as shunt capacitors along the conductor path. If a fully wired one cm by one cm chip [13] is considered, then 2500 crossovers/cm are possible. Thus, 3.75 pF/cm is present on the net due to crossovers. Recall, the capacitance of a two micron FLM conductor on either GaAs or Si was approximately 2.0 pF/cm. Note that even if the above value is scaled, the added capacitance due to crossovers may be greater than the capacitance of the line itself. The same type of analysis as that of the path length may be carried out for crossovers; a percentage value in wiring density will simply translate into a percentage of crossovers.

# 4. Other Components of Skew

## 4.1. Process Variations

In addition to evaluating skew when process variations are added, we would also like to be able to predict changes in the net charging time and the multiple chip skew and to be able to find ways to minimize the predicted changes by choosing the appropriate combination of conductor width and spacing, substrate type, and conductor level. Consider a conductor. The process variations which could be expected are changes in conductor width, $W$, conductor spacing, $S$, conductor thickness, $t$, and height of the conductor above the ground plane, $h$. Changes in the relative dielectric constant of the passivation layer, $\epsilon_r$, and the conductor resistivity, $\rho$, may also occur. The set of process variations we will consider are $W \pm .3$, $t \pm .25$, and $h \pm .25$.

If a single clock driver is used to drive the clock net, the single chip skew, $\delta_{SC}(PL)$, is in the form

$$\delta_{SC}(PL) = R\,[a_1 C + a_2 Co] \tag{4.1}$$

where $a_i$ is a constant depending on the clock net and the wiring distribution. When process variations affecting the conductor are taken into account the single chip skew becomes

$$\delta_{SC}(PL,PV) = R(1 + \partial R)[a_1 C(1 + \partial C) + a_2 Co] \tag{4.2}$$

where the relative change in $x$ is

$$\partial x = (x_{new} - x_{old})/x_{old}. \tag{4.3}$$

If $a_1 C >> a_2 Co$ (4.2) simplifies to

$$\begin{aligned} \delta_{SC}(PL,PV) &\approx \delta_{SC}(PL) + a_1 CR[\partial C + \partial R + \partial R\ \partial C] \\ &\approx \delta_{SC}(PL)[1 + \partial(RC)]. \end{aligned} \tag{4.4}$$

In the same manner $\tau(PL)$ is in the form

$$\tau(PL) = Rdev[a_3C + a_4Co] + R[a_5C + a_6Co]. \tag{4.5}$$

If, as in the cases analyzed, $a_3C$ $Rdev$ is the dominant factor of the net charging time, then the net charging time when conductor variations are introduced simplifies to

$$\tau(PL,PV) \approx \tau(PL)[1 + \partial C]. \tag{4.6}$$

So, the multiple chip skew due to path length differences and conductor process variations may be approximated as

$$\begin{aligned}\delta_{MC}(PL,PV) \approx \delta_{MC}(PL) + \tau_U(PL)\,\partial C_U - \tau_L(PL)\,\partial C_L \\ + \delta_{SC_L}(PL)\partial(RC)_L.\end{aligned} \tag{4.7}$$

Since $\tau_U(PL) \geq \tau_L(PL) > \delta_{SC_L}(PL)$, the maximum multiple chip skew is attained when the *upper* clock net and the *lower* clock net have conductor process variations which lead to a maximum relative increase and decrease in conductor capacitance, respectively. Note, $\partial C_L$ is a negative value denoting a decrease in the relative change in capacitance. Since multiple chip systems are more common than single chip systems, we will concentrate on minimizing the multiple chip skew.

To assess the impact of conductor width, conductor level, and substrate type on the skew and the net charging time of a clock distribution net, all combinations of the three process variations, eight of them, were used in simulating the relative changes in conductor capacitance and conductor resistance of FLM and SLM conductors on Si and on GaAs. The relative changes in $c$ and $rc$ of FLM conductors and of SLM conductors on GaAs and on Si are shown in Table 4.1 for several conductor widths and spacings. PV1 and PV2 result in the largest relative increase and largest relative decrease in capacitance, respectively. PV3 results in the largest relative increase in $RC$. Notice for PV1 and for PV2 the relative changes in capacitance of SLM conductors are less than those of FLM conductors on Si. Since the capacitance of SLM conductors is less than its FLM counterpart, thereby yielding a lower $\tau(PL)$ for a given conductor width, and since SLM conductors have lower relative changes in capacitance compared to FLM conductors, we will concentrate on the skew of clock nets composed of SLM conductors in order to minimize the maximum skew of the system.

Table 4.1. Relative changes in FLM and SLM $c$ and $rc$.

| | | FLM | | | | SLM | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Si | | GaAs | | Si | | GaAs | |
| W=S | PV | $\partial c$ | $\partial rc$ | $\partial c$ | $\partial rc$ | $\partial c$ | $\partial rc$ | $\partial c$ | $\partial rc$ |
| 2 | 1 | .309 | -.090 | .149 | -.201 | .191 | -.172 | .197 | -.168 |
| | 2 | -.207 | .244 | -.292 | .113 | -.153 | .328 | -.157 | .322 |
| | 3 | .005 | .576 | -.124 | .374 | -.129 | .367 | -.137 | .353 |
| 6 | 1 | .294 | -.014 | .048 | -.202 | .098 | -.164 | .082 | -.176 |
| | 2 | -.186 | .143 | -.143 | .204 | -.087 | .282 | -.075 | .299 |
| | 3 | .175 | .650 | -.046 | .339 | -.007 | .394 | -.031 | .360 |
| 10 | 1 | .301 | -.010 | .029 | -.201 | .090 | -.154 | .059 | -.178 |
| | 2 | -.187 | .118 | -.097 | .241 | -.079 | .266 | -.055 | .299 |
| | 3 | .222 | .680 | -.029 | .335 | .023 | .406 | -.011 | .360 |
| 20 | 1 | .301 | .025 | .015 | -.200 | .087 | -.144 | .037 | -.183 |
| | 2 | -.195 | .089 | -.056 | .277 | -.075 | .252 | -.035 | .306 |
| | 3 | .257 | .702 | -.029 | .335 | .048 | .419 | -.001 | .354 |

For the clock nets analyzed and the conditions $Rdev = 500\Omega$ and $\rho = 3\ \mu\Omega{-}cm$, the maximum multiple chip skew occurs when one chip has process variations PV1 and one chip has process variations PV2. The choice of the set of process variations which yield the maximum skew will be discussed in section five.

Recall that the multiple chip skew due to path lengths is minimized at conductor widths where coupling is minimal, that is, large conductor widths and spacings. When process variations are considered the product $\tau(PL)\,\partial C$, and therefore the product $C\partial C$, should be minimized to incur the smallest increase in $\delta_{MC}(PL,PV)$ over $\delta_{MC}(PL)$. Consider Fig. 2.2 and Table 4.1; a large conductor width and spacing will minimize $C\partial C$ for conductors on a GaAs substrate since both the capacitance and the absolute value of the relative changes in capacitance decrease for increasing conductor widths. Meanwhile, an intermediate conductor width will be needed for a Si substrate since the capacitance is minimized at $W = S \approx 2$ while the absolute value of the relative change in capacitance decreases for increasing conductor widths.

Figure 4.1 shows multiple chip skews due to path length and process variations calculated using the Elmore delay for two different multiple chip systems, one containing two wiring distributions, WD-A and WD-C, and the other containing only WD-A, versus net type, i.e., each multiple chip system contains only one net type. Also shown for reference is the multiple chip skew due to varying path lengths. Consider the multiple chip systems containing only WD-A. Although the multiple chip skews due to path lengths are approximately equal for clock nets on GaAs and for clock nets on Si, when conductor process variations are introduced the multiple chip skew is greater for clock nets on Si. This occurs because, given the fixed clock nets, the clock nets on Si have higher conductor capacitance, and therefore higher net charging times, than the clock nets on GaAs and the absolute changes in conductor capacitance are generally higher for conductors on Si. When two distributions are present the multiple chip skew due to path length increases, more for clock nets on GaAs, thereby increasing the multiple chip skew due to path length and process variations. Note, in all cases the minimum in skew occurs at $W = S = 6$ and $W = S = 20$ for conductors on Si and

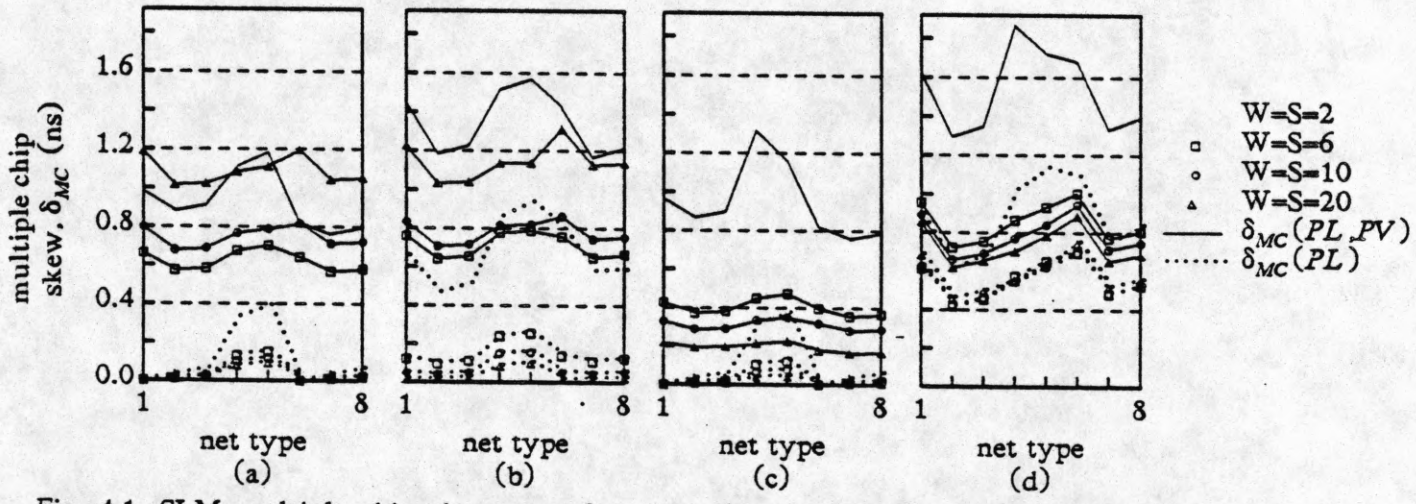


Fig. 4.1. SLM multiple chip skew as a function of path length and conductor process variations and SLM multiple chip skew as a function of path length versus net type and two sets of wiring distributions, one with WD-A and one with WD-A and WD-C for conductors on (a) Si,WD-A (b) Si,WD-A and WD-C (c) GaAs,WD-A (d) GaAs,WD-A and WD-C.

GaAs, respectively.

### 4.2. Active Elements

Throughout this analysis we have assumed a constant value of 500 ohms for the output impedance of the clock driver. Consider the effect on the multiple chip skew when process variations present in the clock driver output are included. Again, making the simplifying approximation $\tau(PL) \approx a_3 C\ Rdev$, the approximation for skew is

$$\begin{aligned} \delta_{MC}(PL, PV, AE) \approx \delta_{MC}(PL) + \delta_{SC_L}(PL)\,\partial(RC)_L \\ + \tau_U(PL)[\partial C_U + \partial Rdev_U + \partial Rdev_U \partial C_U] \\ - \tau_L(PL)[\partial C_L + \partial Rdev_L + \partial Rdev_L \partial C_L]. \end{aligned} \tag{4.8}$$

Note, $\partial Rdev_U$ and $\partial C_U$ are positive and $\partial Rdev_L$ and $\partial C_L$ are negative. It is clear that the conductor width and spacing with the lowest capacitance will yield the smallest increase in $\delta_{MC}(PL, PV, AE)$ over $\delta_{MC}(PL, PV)$ because of the dependencies on the net charging time. It follows that clock nets with a larger total conductor area, the H-net for example, will have larger skews.

Fig. 4.2 shows the multiple chip skew due to path length, process variations, and active elements for two absolute values of the relative changes in clock driver output impedance, $|\partial Rdev| = .5$ and $|\partial Rdev| = .2$ (note the separate scales on all four graphs). As expected smaller skews are associated with the lower changes in impedance. Notice the gap in skews between the two sets of wiring distributions given a net type, substrate type, and conductor width increases for decreasing values of $\partial Rdev$. The gap for these two sets can be approximated by

$$\begin{aligned} \delta_{MC}^{A,C}(PL, PV, AE) - \delta_{MC}^{A}(PL, PV, AE) \approx \\ [\tau_L^A(PL) - \tau_L^{A,C}(PL)][1 + \partial C_L + \partial Rdev_L + \partial C_L \partial Rdev_L] \end{aligned} \tag{4.9}$$

where superscripts $A, C$ and $A$ refer to the two multiple chip systems with WD-A and WD-C and with WD-A, respectively. The difference $(\tau_L^A(PL) - \tau_L^{A,C}(PL))$ is larger for conductors with capacitive coupling given identical net types in the system. As processing is refined and process varia-

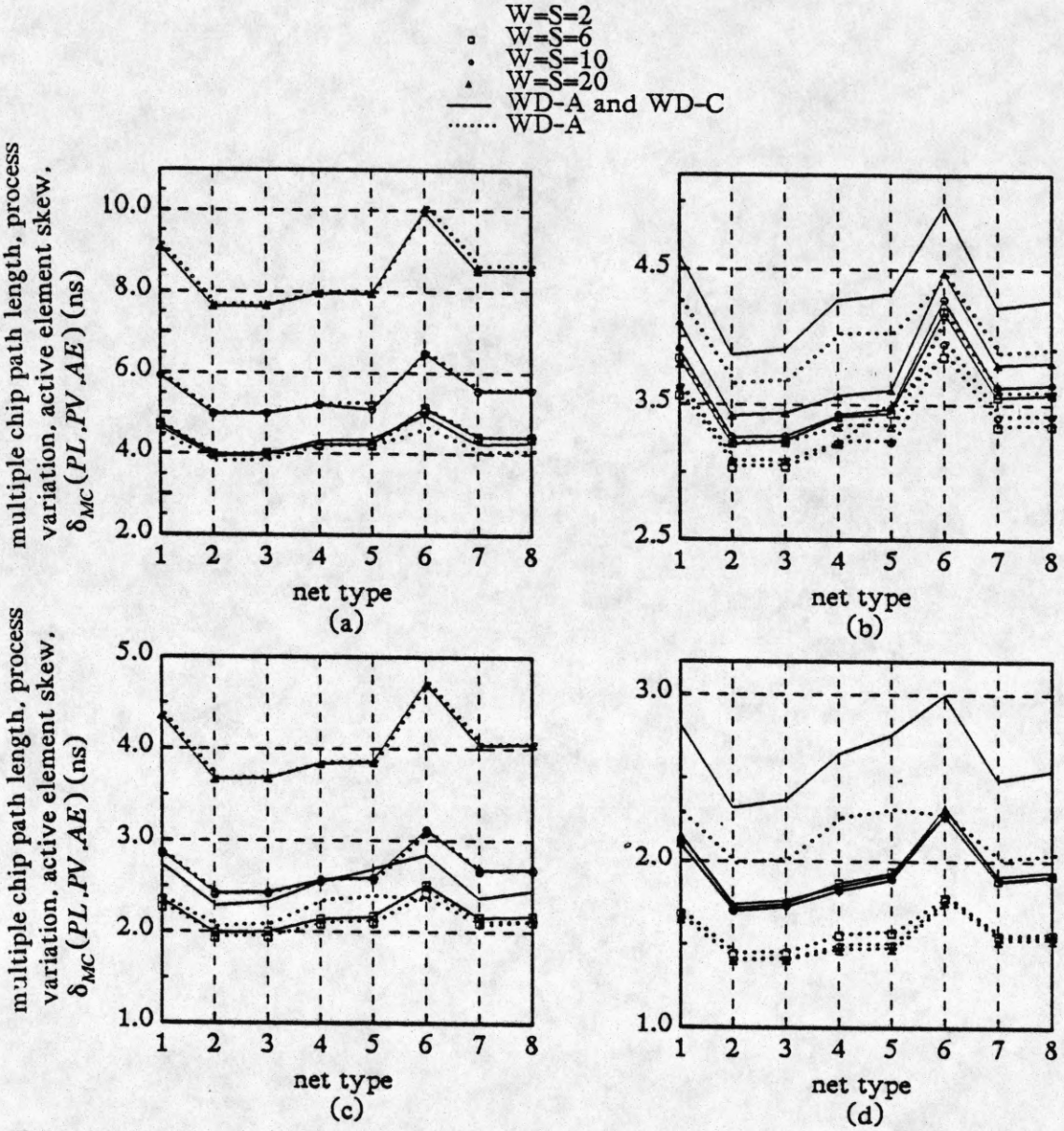


Fig. 4.2. SLM multiple chip skew as a function of path length, process variations, and active elements for two sets of wiring distributions, one with WD-A and one with WD-A and WD-C, versus net type (a) Si, $|\partial R| = .5$ (b) GaAs, $|\partial R| = .5$ (c) Si, $|\partial R| = .2$ (d) GaAs, $|\partial R| = .2$.

tions are decreased, that is, the absolute values of $\partial C_L$ and $\partial Rdev_L$ are decreased, the gap increases. The maximum size of the gap is $\tau_L^A(PL) - \tau_L^{A,C}(PL)$.

### 4.3. Device Threshold

If the voltage waveforms are in the form

$$v(t) = VDD[1 - e^{-t/\tau}] \tag{4.10}$$

where $VDD$ is the high voltage level, then the approximated skew due to path lengths, process variations, active elements, and threshold variations is

$$\begin{aligned}\delta_{MC}(PL,PV,AE,DT) \approx\ & \tau_L(PL)[1 + \partial C_L + \partial Rdev_L + \partial Rdev_L \partial C_L]\, ln[1-VT_L/VDD] \\ & - \tau_U(PL)[1 + \partial C_U + \partial Rdev_U + \partial Rdev_U \partial C_U]\, ln[1 - VT_U/VDD] \\ & - \delta_{SC_L}(PL)[1 + \partial(RC)_L]\, ln[1 - VT_L/VDD].\end{aligned} \tag{4.11}$$

Again, larger skews will result from nets with higher net charging times. Also, tighter process controls on the deviation of threshold voltages will result in lower multiple chip skews.

# 5. Discussion

Approximations of the multiple chip skew were made in order to concentrate on the parameters which contribute the most to skew. If $a_3CRdev$ is not clearly the dominant term in $\tau(PL)$, then the approximation for multiple chip skew will change, that is, if $\tau(PL)$ is simplified as $\tau(PL) \approx a_3CRdev + a_5CR$, then

$$\begin{aligned}\delta_{MC}(PL,PV,AE) &= \tau_U(PL)[1+\partial C_U] - \tau_L(PL)[1+\partial C_L] + \delta_{SC_L}(PL)[1+\partial(RC)_L] \\ &+ a_{3_U}C_U Rdev_U[\partial Rdev_U + \partial Rdev_U \partial C_U] + a_{5_U}C_U R_U[\partial R_U + \partial R_U \partial C_U] \\ &- a_{3_L}C_L Rdev_L[\partial Rdev_L + \partial Rdev_L \partial C_L] - a_{5_L}C_L R_L[\partial R_L + \partial R_L \partial C_L].\end{aligned} \tag{5.1}$$

Two sets of process variations should be chosen such that one set maximizes

$$a_3 Rdev\,\partial C + a_5 R\,\partial(RC) \tag{5.2}$$

on the *upper* clock net and one set minimizes

$$a_3 Rdev\,\partial C + (a_5 - a_1)R\,\partial(RC) \tag{5.3}$$

on the lower clock net. Thus, given a conductor width and spacing and $Rdev$, the two sets of process variations may vary depending on the clock net layout. For the eight clock nets on Si with WD-A Fig. 5.1 compares approximations (4.8) and (5.1) with the Elmore calculations with either $Rdev = 500\Omega$ and $\rho = 3\mu\Omega - cm$ or $Rdev = 250\Omega$ and $\rho = 6\mu\Omega - cm$. As expected (5.1) is more accurate than (4.8) at smaller conductor widths and spacings.

Having estimated the clock skew of a multiple chip system, skew minimization techniques must be investigated. From the analysis presented, it is evident that the net charging time is an important design parameter to minimize. In the restricted cases analyzed, that is, a clock driver with a 500 ohm output impedance driving sixteen clocked elements connected on a 1 cm by 1 cm chip, the net charging time could be reduced by choosing a conductor level and conductor spacing

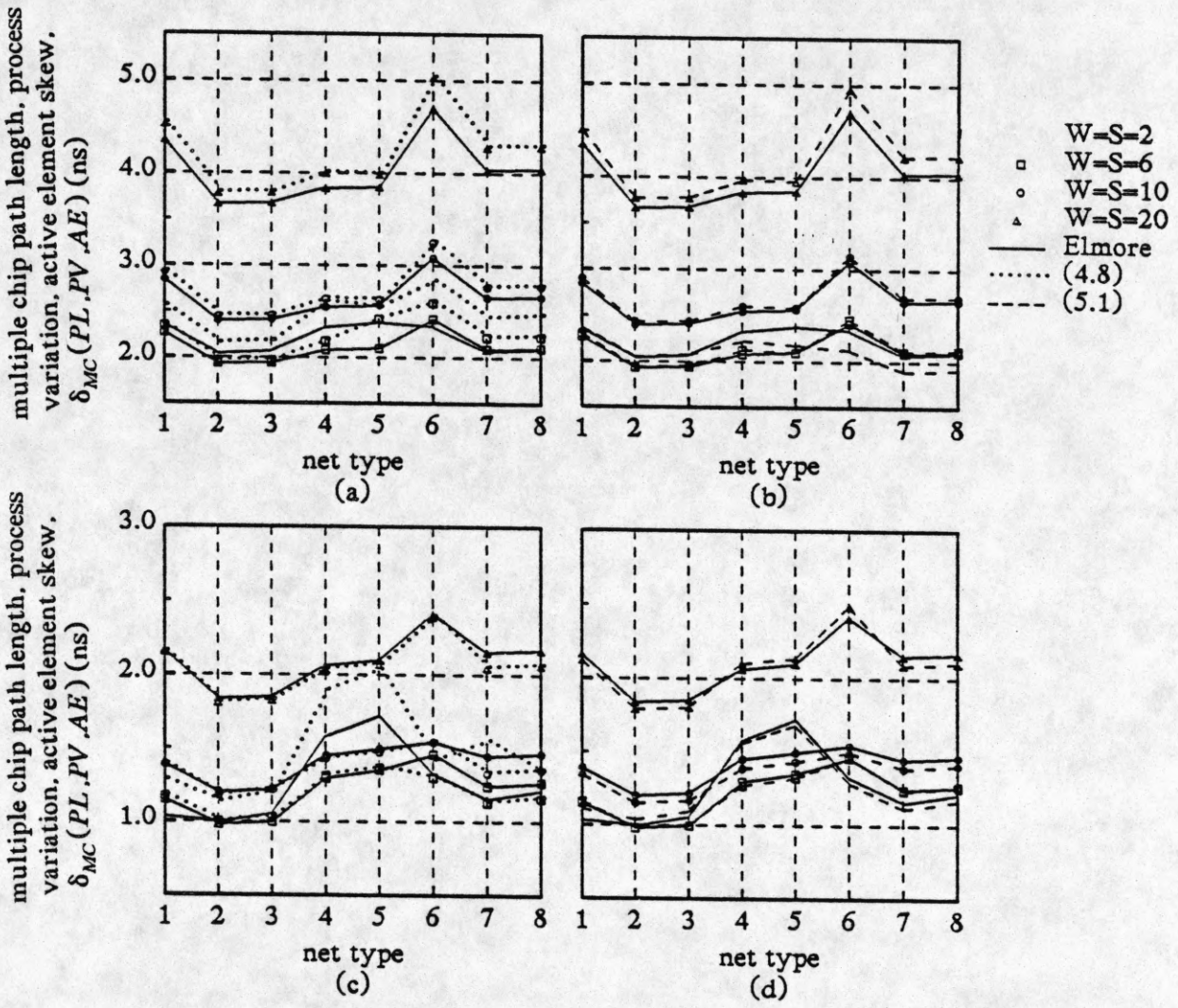


Fig. 5.1. Comparison of approximations (4.8) and (5.1) and the Elmore delay for clock nets on Si with WD-A (a) (4.8), Rdev=500, $\rho$=3 (b) (5.1), Rdev=500, $\rho$=3 (c) (4.8), Rdev=250, $\rho$=6, (d) (5.1), Rdev=250, $\rho$=6.

that yielded a low capacitance per unit length conductor and/or by choosing one clock net design over another. Although the effects of other conductors crossing over and under the clock net was mentioned briefly in section three and not included in the examples afterwards, effects of cross-overs on the net charging time, and therefore on skew, can be appreciable and should not be ignored.

In the design environment, more net charging time reducing options are available. One option is to reduce the driving device resistance. Note that this resistance cannot be reduced without end, because the transmission line domain may be entered and then other skew reducing techniques must be used. As a result, for high speed systems it is entirely possible that a single clock distribution net on a large chip will not suffice. Another option to limit the net charging time, and therefore the skew, is to partition the clock distribution net. Extra clock drivers could be allocated or if the system is pin limited, multiple output stages on a single clock driver may be used. Note though that extra clock drivers may increase the off-chip clock skew if the drivers are not allocated carefully.

Since minimizing the net charging time alone will not necessarily minimize skew, other design parameters which must be considered are the relative changes in the conductor capacitance, the conductor resistance, and the driving device resistance which come about due to process variations. Although clock driver design techniques were not discussed here, it is important to find designs which produce the smallest relative changes under process variations [14].

Two major design difference become apparent when designing clock nets on GaAs versus Si substrates. First, as shown in Fig. 2.3, the capacitance of conductors is less for conductors on GaAs given a conductor width and spacing. Therefore, the clock distribution system on a silicon substrate would have to be partitioned into a smaller number of parts, compared to a clock net on GaAs, to achieve a desirable skew and clock net charging time, assuming no other options were available. Second, capacitance coupling is more prevalent on a GaAs substrate at all conductor widths. In order to achieve an accurate prediction of the skew and net charging time for clock nets on GaAs the capacitance of the conductors must always be calculated based on the proximity of adjacent conductors.

# 6. Conclusions

An optimal on-chip clock distribution system does not always result when all paths to the clocked elements are equalized. Rather an optimal on-chip clock distribution system depends on varying path lengths to the clocked elements, the crossing of conductors over an under the clock net, process variations, the insertion of active elements in the clock net, and the differences in the device threshold of the receiving devices and their relationship to one another. We have shown that the design of an optimal on-chip clock distribution net may vary depending on the conductor width and spacing, the proximity of adjacent conductors to the clock net (wiring distribution), the driving impedance of the clock device, and conductor characteristics such as resistivity. With the use of simplified skew and charging time approximations and a tool which yields an accurate assessment of conductor capacitance predictions of clock skew prior to chip layout may be made and design guidelines may be developed.

# References


[1] C. Mead and L. Conway, *Introduction to VLSI Systems*. Reading, MA: Addison-Wesley, 1980.

[2] D. F. Wann and M. A. Franklin, "Asynchronous and Clocked Control Structures for VLSI Based Interconnection Networks," *IEEE Trans. on Computers*, vol. C-32, pp. 284-293, March 1983.

[3] S. Y. Kung and R. J. Gal-Ezer, "Synchronous versus Asynchronous Computation in Very Large Scale Integrated (VLSI) Array Processors," *SPIE Real Time Signal Processing V*, vol. 341, pp. 53-65, 1982.

[4] W. C. Elmore, "The Transient Response of Damped Linear Networks with Particular Regard to Wideband Amplifiers," *Journal of Applied Physics*, vol. 19, pp. 55-64, January 1948.

[5] E. E. Davidson, "Electrical Design of a High Speed Computer Package," *IBM Journal of Research and Development*, vol. 26, pp. 349-361, May 1982.

[6] T. Sakurai, "Approximation of Wiring Delay in MOSFET LSI," *IEEE Journal of Solid-State Circuits*, vol. SC-18, pp. 418-426, August 1983.

[7] D. L. Carter and D. F. Guise, "Analysis of Signal Propagation Delays and Chip Level Performance Due to Chip Interconnections," in *International Conference on Computer Design: VLSI in Computers*, Port Chester, NY, pp. 218-221, November 1983.

[8] P. Cottrell and E. Buturla, "VLSI Wiring Capacitance," *IBM Journal of Research and Development*, vol. 29, pp. 277-287, May 1985.

[9] H. Yuan, Y. Lin, and S. Chiang, "Properties of Interconnection on Silicon, Sapphire, and Semi-Insulating Gallium Arsenide Substrates," *IEEE Transactions on Electron Devices*, vol. ED-29, April 1982.

[10] C. P. Yuan, *Modeling and Extraction of Interconnect Parameters in Very-Large-Scale Integrated Circuits*. Ph.D. Dissertation, University of Illinois at Urbana-Chanpaign, August 1983.

[11] W. R. Smith and D. E. Snyder, "Circuit Loading and Crosstalk Signals From Capacitance in SOS and Bulk-Silicon Interconnect Channels," *Proc. IEEE VLSI Multilevel Interconnection Conference*, pp. 218-227, June 1984.

[12] E. G. Friedman and S. Powell, "Design and Analysis of a Hierarchical Clock Distribution System for Synchronous Standard Cell/Macrocell VLSI," *IEEE Journal of Solid-State Circuits*, vol. SC-21, pp. 240-246, April 1986.

[13] R. W. Keyes, "The Wire-Limited Logic Chip," *IEEE Journal of Solid-State Circuits*, vol. SC-17, pp. 1232-1233, December 1982.

[14] M. Shoji, "Elimination of Process-Dependent Clock Skew in CMOS VLSI," *IEEE Journal of Solid-State Circuits*, vol. SC-21, pp. 875-880, October 1986.