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While doing RTL simulation (for power estimation purposes), the simulator cannot distinguish between combinational blocks that will eventually be implemented as DOMINO or as static CMOS circuits. Since the simulator uses Boolean models for these blocks, it is implicitly assuming, therefore, that they will be implemented as static CMOS. For those blocks which eventually are implemented as DOMINO, this assumption leads to incorrect estimation of activity factors and signal probabilities which would result in erroneous estimation of power at RTL and hence wrong design decisions. In this paper, we provide a way to predict the activity factor and signal probability at the output of a Boolean function implemented using DOMINO CMOS circuit, from the knowledge of signal probability at the output of same Boolean function implemented using static CMOS circuit.

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Prediction of Activity Factor and Signal Probability in Domino CMOS Circuits†

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Abstract

While doing RTL simulation (for power estimation purposes), the simulator cannot distinguish between combinational blocks that will eventually be implemented as DOMINO or as static CMOS circuits. Since the simulator uses Boolean models for these blocks, it is implicitly assuming, therefore, that they will be implemented as static CMOS. For those blocks which eventually are implemented as DOMINO, this assumption leads to incorrect estimation of activity factors and signal probabilities which would result in erroneous estimation of power at RTL and hence wrong design decisions. In this paper, we provide a way to predict the *activity factor* and *signal probability* at the output of a Boolean function implemented using DOMINO CMOS circuit, from the knowledge of *signal probability* at the output of same Boolean function implemented using static CMOS circuit.

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1. Introduction

High level power estimation has emerged as an important step in the design process, in order to provide early warning of any power problems before the circuit-level design has been specified. With such early warning, the designer can explore design trade-offs at a higher level of abstraction than previously possible, reducing design time and cost.

When estimating the power dissipation of a circuit, some information about signal switching activity and signal probability is required. For high-level power estimation, these signal statistics are obtained by performing some type of high-level simulation, say at the register transfer level (RTL). At RTL, the circuit is composed of combinational blocks that lie between banks of latches or flip-flops, as shown in Fig. 1. We assume that the combinational blocks will eventually be implemented using either DOMINO CMOS or static CMOS logic styles. While doing the RTL simulation, the simulator cannot differentiate between blocks that will eventually be implemented as DOMINO CMOS or as static CMOS. Typically, since the simulator works only with the Boolean function, it is implicitly assuming that all combinational blocks are implemented using static CMOS logic style. For a block which is subsequently implemented in DOMINO, this will result in erroneous estimation of switching activity and signal probability and hence incorrect power estimation. In this paper we will derive expressions for *activity factor* and *signal probability* at the output of DOMINO CMOS circuit in terms of *signal probability* at the output of a static CMOS circuit implementing the same Boolean function.

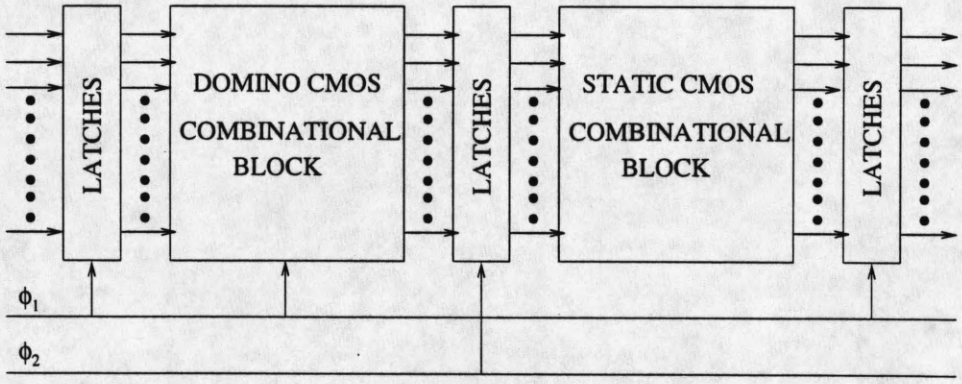

Figure 1. High level description of combinational block

2. Problem formulation

We assume an overall logic design style as shown in Fig. 1, where the blocks marked "LATCHES" contain banks of edge-triggered flip-flops and where the two clocks ϕ_1 and ϕ_2 are non-overlapping. We start with some definitions:

Definition: Activity Factor (AF) at a node is defined as the number of transitions of that node occurring within a given time window of a given vector set divided by the number of transitions of the reference clock over that same time window.

It is clear that AF is a non-negative real number:

$$AF \geq 0.0 \tag{1}$$

For example, suppose a node makes N_t transitions in N clock cycles. Since the clock makes 2 transitions in every clock cycle, then the number of transitions made by the clock is $2N$, and the activity factor of the node is:

$$AF = \frac{N_t}{2N}$$

Definition: Signal Probability (SP) of a node is defined as the fraction of the time that a node is at logic high, within a given time window of a given vector set.

It is clear that SP is a non-negative real number and is no larger than 1:

$$0.0 \leq SP \leq 1.0 \tag{2}$$

For example, suppose a node is high for a total time of $N_h T$, where N_h is the number of times the node is high and T_h is the duration of each high interval (assuming they are all the same length). The total length of time (the time window) is NT, where N is the total number of clock cycles and T is one clock period. Hence, the signal probability of the node is given by:

$$SP = \frac{N_h T_h}{NT}$$

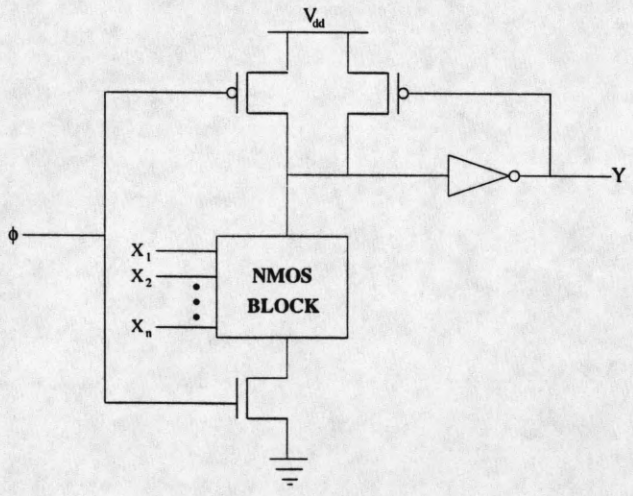

Figure 2. A Boolean function implemented using DOMINO CMOS logic family.

Fig. 2 shows a typical DOMINO CMOS gate that implements the same Boolean function as the static CMOS gate in Fig. 3. The clock ϕ driving the DOMINO gate is one of the two clocks, either ϕ_1 or ϕ_2, of Fig. 1.

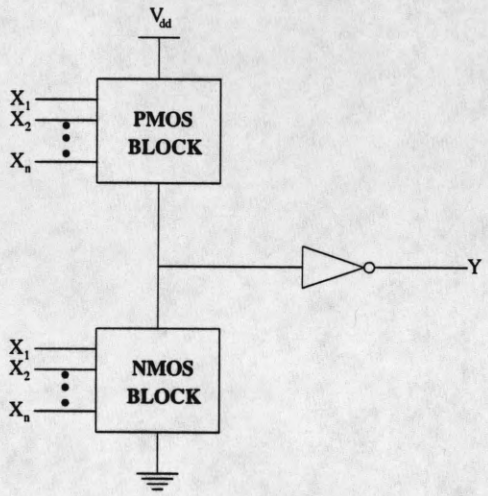

Figure 3. Static CMOS circuit implementing the same Boolean function as by DOMINO CMOS.

Definition: Duty factor (δ). As shown in the Fig. 4, duty factor is the fraction of the time for which a clock signal is high during a clock cycle, i.e.:

$$\delta = \frac{T_h}{T} \tag{3}$$

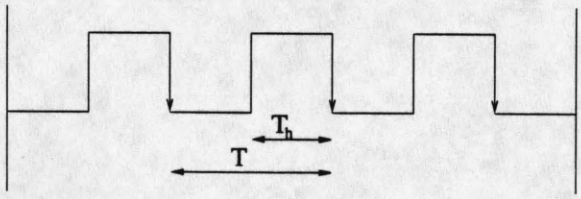

Figure 4. Definition of duty factor

3. Proposed Solution

Our solution is based on the following assumptions:

1. The latch outputs change on at the falling edge of the clock. In other words, the latches are negative edge triggered.

2. All primary inputs must be stable just before and during the evaluate phase.
3. The evaluate clock is same as the reference clock (either ϕ_1 or ϕ_2), except when there is clock gating.
4. RTL simulation uses zero-delay timing models.

In the next two sections we will derive the expressions for AF and SP at the output of DOMINO CMOS circuit for the two cases: without and with clock gating. We will use the symbol SP_s^z to represent SP of a static circuit under zero-delay conditions, and SP_d^z to represent the same for a dynamic (DOMINO) circuit. Likewise, AF_s^z and AF_d^z will be used to represent AF in the static and dynamic cases. In a time window of N clock cycles, we denote by N_h the number of cycles in which a node evaluates to a logic high value.

3.1 Without Clock Gating

Given the above assumptions, we can now prove the following propositions.

Proposition 1 : SP at the output of DOMINO CMOS circuit is given by the following expression:

$$SP_d^z = \delta SP_s^z \tag{4}$$

Proof : For a static implementation, a node is either high for the whole clock cycle or low for the whole clock cycle (given zero-delay). Therefore, it follows from the definition of SP_s^z that:

$$SP_s^z = \frac{N_h}{N} \tag{5}$$

Shown in Fig. 5 are typical waveforms of the clock, the output of a static CMOS circuit, and the output of the corresponding DOMINO CMOS circuit. It can be seen that, in any clock cycle where the output of a static circuit is high, the output of the DOMINO circuit is also high, but only during the evaluate phase. At all other times, the output of the DOMINO circuit is low. Therefore, the output of a DOMINO circuit is high for a total time of $N_h \delta T$. Hence the signal probability at the output of a DOMINO CMOS circuit is given by:

$$SP_d^z = \frac{N_h \delta T}{NT} = \delta SP_s^z \tag{6}$$

Proposition 2: AF at the output of DOMINO CMOS circuit is given by the following expression:

$$AF_d^z = SP_s^z \tag{7}$$

Proof : It is clear from the Fig. 5 that, whenever the output of a DOMINO CMOS circuit goes high during the evaluate phase, it makes exactly two transitions. Hence, the number of transitions made by the output of a DOMINO CMOS circuit is $2N_h$. The clock makes two

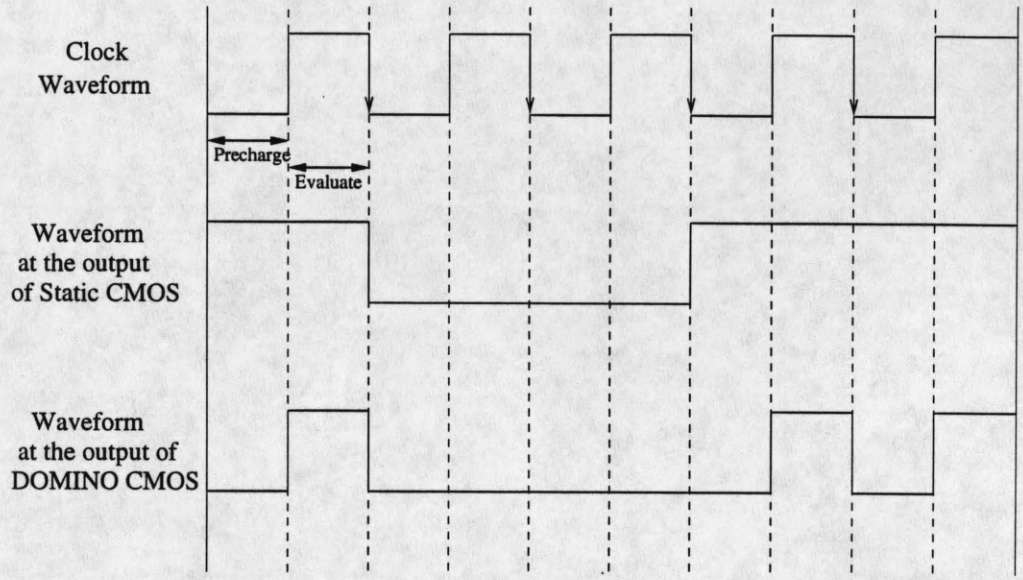

Figure 5. Waveforms at the output of static and DOMINO circuits implementing the same Boolean function.

transitions every clock cycle, therefore the number of transitions made by the clock is $2N$. Hence, AF at the output of a DOMINO CMOS circuit is given by:

$$AF_d^z = \frac{2N_h}{2N} = SP_s^z \tag{8}$$

From (4) and (7) a special relationship between AF_d^z and SP_d^z can be seen, as given by the following expression:

$$SP_d^z = \delta AF_d^z \tag{9}$$

It is not hard to see that this relationship is always true for any DOMINO gate output.

3.2 With Clock Gating

In case of clock gating, the high level circuit remains the same as that in Fig. 1 except that the clock is now being gated by an AND gate as shown in Fig. 6. Notice that, in this case, AF of the gated clock may be less than 1.0 and the DOMINO logic may not evaluate in every cycle of the reference clock. Whenever the enable signal $\mathcal{E}$ is low, ϕ_{gated} will be low regardless of $\phi_{reference}$. Therefore, whenever $\mathcal{E}$ is low, the output of a static CMOS circuit will retain its logic value while the output of a DOMINO CMOS circuit will be forced low. When $\mathcal{E}$ is high, the circuits will behave the same as in the no-clock-gating case.

Define the *random variable* (RV) τ to be a random time point value within the time window of interest, and let τ be uniformly distributed, so that all time points within the window are equally probable. Note that τ is a continuous (rather than discrete) time variable.

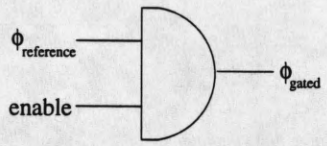

Figure 6. Clock gating

Since τ is random, the value of a logic signal at the time τ is another RV (that takes values in $\{0, 1\}$), whose 1-probability will be denoted by $\mathcal{P}\{x = 1\}$. Let x represent the output of a Boolean function and let x_d be the circuit node corresponding to the dynamic DOMINO CMOS implementation of x and x_s correspond to the static implementation. Note that $SP_s^z = \mathcal{P}\{x_s = 1\} = \mathcal{P}\{x = 1\}$ and $SP_d^z = \mathcal{P}\{x_d = 1\}$. Notice also that for a clock ϕ, the duty cycle is such that $\delta = \mathcal{P}\{\phi = 1\}$. We now define α to be the duty cycle of the enable signal:

$$\alpha = \mathcal{P}\{\mathcal{E} = 1\}$$

The conditional probability of a node x, conditional on the enable signal $\mathcal{E}$ being high, is written as $\mathcal{P}\{x = 1|\mathcal{E} = 1\}$. We will also represent this with the symbol $SP|_{\mathcal{E}=1}$, so that:

$$SP|_{\mathcal{E}=1} = \mathcal{P}\{x = 1|\mathcal{E} = 1\}$$

The interpretation of the conditional probability is as follows. Let $T_{\mathcal{E}}$ be the total cumulative time duration for which $\mathcal{E} = 1$ in the time window of interest. Then, the conditional probability is equal to the fraction of the time duration $T_{\mathcal{E}}$ for which the signal x is high.

Proposition 3: SP at the output of a DOMINO CMOS circuit when there is clock gating is given by the following expression:

$$SP_{d,g}^z = \alpha\delta SP_{s,g}^z|_{\mathcal{E}=1} \approx \alpha\delta SP_{s,g}^z \tag{10}$$

where the subscript g denotes that the clock is gated.

Proof : As before, let x be the output of a Boolean function, x_d be the circuit node corresponding to the dynamic DOMINO CMOS implementation of x, and x_s correspond to the static implementation. It is clear that $SP_{d,g}^z = \mathcal{P}\{x_d = 1\}$. Using conditional probability, we can write:

$$\mathcal{P}\{x_d = 1\} = \mathcal{P}\{x_d = 1|\mathcal{E} = 1\}\mathcal{P}\{\mathcal{E} = 1\} + \mathcal{P}\{x_d = 1|\mathcal{E} = 0\}\mathcal{P}\{\mathcal{E} = 0\} \tag{11}$$

But $\mathcal{P}\{x_d = 1|\mathcal{E} = 0\} = 0$. Hence:

$$\mathcal{P}\{x_d = 1\} = \alpha\mathcal{P}\{x_d = 1|\mathcal{E} = 1\} \tag{12}$$

Also, $\mathcal{P}\{x_d = 1|\mathcal{E} = 1\} = \delta\mathcal{P}\{x_s = 1|\mathcal{E} = 1\}$ as this is equivalent to the case when there is no clock gating. Therefore:

$$\mathcal{P}\{x_d = 1\} = \alpha\delta\mathcal{P}\{x_s = 1|\mathcal{E} = 1\} \tag{13}$$

This leads to the first equality in the proposition. If we make the approximation that the output node and the enable signal are independent of each other, which is probably true in practice, then $\mathcal{P}\{x_s = 1|\mathcal{E} = 1\} \approx \mathcal{P}\{x_s = 1\}$ and, in this case:

$$\mathcal{P}\{x_d = 1\} \approx \alpha\delta P\{x_s = 1\} \tag{14}$$

which leads to the 2nd equality in the proposition.

Proposition 4: AF at the output of a DOMINO CMOS circuit, when there is clock gating is given by the following expression:

$$SP^z_{d,g} = \alpha SP^z_{s,g}|_{\mathcal{E}=1} \approx \alpha SP^z_{s,g} \tag{15}$$

Proof : This follows directly from (9) and (10).

4. Conclusion

In this paper, we have derived expressions for predicting AF and SP at the output of DOMINO CMOS circuit in terms of SP at the output of a static CMOS circuit implementing the same Boolean function, both without and with clock gating. This is useful for high level power estimation.