REPORT R-594 DECEMBER, 1972 UILU-ENG 72-2257

CSL COORDINATED SCIENCE LABORATORY

EXPERIMENTAL UNIT FOR (31,16) BINARY CODE USING MAJORITY-LOGIC DECODING

R. BROWN
C. L. CHEN
R. T. CHIEN
D. COAD
S. NG

UNIVERSITY OF ILLINOIS – URBANA, ILLINOIS

APPROVED FOR PUBLIC RELEASE. DISTRIBUTION UNLIMITED.

UILU-ENG 72-2257

EXPERIMENTAL UNIT FOR (31,16) BINARY CODE USING MAJORITY-LOGIC DECODING

by

R. Brown, C. L. Chen, R. T. Chien, D. Coad, S. Ng

This work was supported in part by the Joint Services Electronics Program (U. S. Army, U. S. Navy, and U. S. Air Force) under Contract No. DAAB-07-72-C-0259, and in part by Rome Air Development Center under Contract No. F30602-72-C-0031.

Reproduction in whole or in part is permitted for any purpose of the United States Government.

Approved for public release. Distribution unlimited.

EXPERIMENTAL UNIT FOR (31,16) BINARY CODE USING MAJORITY-LOGIC DECODING†

R. Brown, C. L. Chen, R. T. Chien, D. Coad, S. Ng

1. General Information

This is an experimental unit which incorporates error correcting coding into digital data communication systems for increased reliability. A short, random correcting block code is used in this unit. The code is taken from the class of Euclidean geometry codes which can be decoded by simple majority logic. The unit is complete with an encoder which encodes a block of information digits into a codeword before transmission, a decoder which determines from each codeword the information digits it contains, and an error generator which simulates a noisy channel. For demonstration purposes teletype machines will be used as the data source and the destination of this unit.

A block diagram of the system is shown in Fig. 1. The system will normally be operated in the following sequence for demonstration:

(1) Direct connection between sending and receiving stations with no encoding and no errors introduced.

(2) Transmission with no encoding, but with errors.

(3) Transmission with encoding and with errors inserted.

The code used has the following characteristics:

(31,16) binary, cyclic Euclidean geometry code

Block length - 31 bits

Information - 16 bits

Parity - 15 bits

Distance - 7

†This work was supported in part by the Joint Services Electronics Program (U. S. Army, U. S. Navy, U. S. Air Force) under Contract No. DAAB-07-72-C-0259 and in part by Rome Air Development Center under Contract No. F30602-72-C-0031.

Error correcting capability - 3 random errors

Decoding - 2-step majority logic decoding

Generator polynomial - $1+X+X^2+X^3+X^5+X^7+X^8+X^9+X^{10}+X^{11}+X^{15}$

Parity check polynomial - $1+X+X^4+X^9+X^{10}+X^{11}+X^{12}+X^{16}$

2. Data Source and Destination

The ASR-33 teletype was selected to be used as the data source and destination of the equipment. The teletype uses an 8-level ASCII code with one start unit and two stop units. This code, including the start and stop units, is 11 units long, at 9.09 milliseconds per unit, or 0.1 second per character. Stripped of the start and stop units, two ASCII characters fit very nicely into the (31,16) code.

The data rate for transmitting the 31 bit code block between encoder and decoder was set at 19.2 KHz. Block start-stop synchronization is used in exactly the same way the ASR-33 teletype uses start-stop synchronization by character. In other words, the steady state, no signal, condition of the line is "marking." A transition to "spacing" signals the beginning of a block of data, in the same way that such a transition signals the beginning of a teletype character.

19.2 KHz is not an integral multiple of 110 Hz. used by the teletype, so two clock frequencies were required for the encoding unit. To avoid wiring clock signals between sending and receiving units, two crystal oscillators were used with the encoder, and two more oscillators with the decoder. All logic hardware is T^2L, and no effort was made to reduce size or power requirements. The T^2L logic hardware was

inexpensive and readily available.

3. Encoder Design

A simplified block diagram of the encoder is shown in Fig. 2. This consists of a 16-bit serial-in, parallel out, input shift register, a 16 bit parallel-in, serial-out, encoder shift register and the associated control circuits for input and output.

The teletype input is controlled by a counter, and an 880 Hz. clock. The 880 Hz. is fed into a 3-bit binary counter which is enabled by the "start" pulse from the teletype. Sampling of the data into the input shift register is accomplished by count no. 4 from the counter, which assures sampling at the mid-point of the input signal unit.

This pulse (no. 4) is also counted by a second counter which inhibits sampling during the first, tenth, and eleventh input pulses since these are the "start" and "stop" pulses generated by the teletype. The control waits for a second character input, which is then handled exactly as the first, except that completion of the read-in of the second character initiates a parallel transfer of the two 8-bit characters to the encoder register, signals the encoder control to start, and prepares to receive the next teletype characters. This transfer of control is accomplished during the "stop" interval, so that the data input can be continuous.

The parallel transfer of the two characters from the input register to the encoder register enables the output control, which causes the encoder register to shift right 32 times. The first bit

on line is always a "zero" which is interpreted as a "start" signal by the receiving equipment. The next 16 bits on line are the data bits, and these are followed by the 15 parity check bits. At the completion of the 32 shifts, a constant "one" is applied to the line, producing a "stop" signal to the decoder receiving equipment. As the data and check bits are shifted out on line, errors may be inserted at specific bit locations as explained in the following paragraphs.

4. Error Generator

The serial error generator, Fig. 3, contains three 5-bit binary counters, arranged to count down using the 19.2 KHz. shift pulses as inputs, and a five bit shift register with feedback taps at bit number 2 and bit number 5. This register generates numbers from 1 to 31 inclusive, then repeats. Logic prevents a 'hang-up" in the "zero" state. The sequence of numbers generated is,

2-5-10-21-11-23-14-29-27-22-12-24-17-3-7-15-31-30-28-25-19-6-13-26-20-9-18-4-8-16 and 1.

Using these numbers as bit addresses, each bit of the 31 bit block can be addressed. A sixth bit of the shift register is used to make the decision to introduce an error, or not to introduce an error in the bit addressed by the shift register. This extends the error sequence to 62 characters, which is almost one full line of the ASR-33 printer, before the sequence repeats.

The 19.2KHz. clock is derived from the 307.2 KHz. crystal oscillator, and a frequency higher than 19.2 KHz. is tapped off from

the dividing circuits such that the shift register is shifted four times, and three bit addresses plus the error control bit is stored in counters A, B and C during the time required to transmit the 19.2 KHz. block sync or "start" pulse. When the 31 bit code block is shifted on line, the shift pulses are used to count down the three counters simultaneously. As each counter passes through "zero" count, a pulse is generated which inserts an error at the bit position corresponding to the number contained in the counter.

Some characters will have no errors since the error bit would normally appear in the 15 check bits, which are not used when transmitting with no encoding. The 16 data bits will have errors inserted in 23 of the 62 characters transmitted before the cycle repeats. However, with the encoder and decoder "IN," and with the error generator "IN," as many as three errors are generated for every block of 31 bits transmitted.

5. Decoder Design

The decoder consists of a 31 bit serial-in, serial-out shift register, a 16 bit serial-in, parallel-out shift register and a 22 bit parallel-in, serial-out shift register for output, plus decoder and output control circuits. A block diagram of the decoder is shown in Fig. 4.

The decoder register supplies inputs to six, 6-input majority gates connected according to the parity check equations for the decoder. A seventh 6-input majority gate is driven by the six majority gates and the output is OR'd with the output of the shift register to produce

the decoded digits. This is shown in Fig. 5. Each majority gate, shown in Fig. 6, is connected to the decoder register through the exclusive-OR gates shown in Fig. 7. The parity check equations are:

Set 1 - orthogonal on (0,7,11,30)

0,7,11,30,1, 2,10,26
0,7,11,30,3,12,14,16
0,7,11,30,4, 5,18,28
0,7,11,30,6,15,20,25
0,7,11,30,8,21,24,27
0,7,11,30,9,13,23,29

Set 2 - orthogonal on (1,16,27,30)

1,16,27,30, 0, 3,10,21
1,16,27,30, 2, 7, 8,14
1,16,27,30, 5,13,20,22
1,16,27,30, 6, 9,17,18
1,16,27,30,11,12,24,26
1,16,27,30,15,19,23,28

Set 3 - orthogonal on (2,23,25,30)

2,23,25,30,0, 6,13,26
2,23,25,30,1, 7,15,29
2,23,25,30,3,18,22,24
2,23,25,30,4, 8,16,19
2,23,25,30,5,12,17,21
2,23,25,30,9,10,11,20

Set 4 - orthogonal on (4,10,17,30)

4,10,17,30, 2, 5,11,19
4,10,17,30, 3, 6,27,29
4,10,17,30, 7,22,26,28
4,10,17,30, 8,12,20,23
4,10,17,30, 9,16,21,25
4,10,17,30,13,14,15,24

Set 5 - orthogonal on (5,24,29,30)

5,24,29,30, 0, 8, 9,28
5,24,29,30, 1,12,22,25
5,24,29,30, 2, 3,15,17
5,24,29,30, 4,11,13,27
5,24,29,30, 6,10,14,19
5,24,29,30, 7,18,21,23

Set 6 - orthogonal on (6,8,22,30)

6,8,22,30, 0,19,24,25
6,8,22,30, 1, 5, 9,14
6,8,22,30, 2,13,16,18
6,8,22,30, 3, 4,23,26
6,8,22,30, 7,17,20,27
6,8,22,30,10,12,28,29

When the block sync, or start, pulse arrives at the input to the decoder register, the control recognizes the transition to "space" and shifts the decoder register 32 times, including the "start" pulse, which is shifted off the right end of the register. After 32 shifts at the 19.2 KHz. rate, the shift register input from the line is disabled and the feedback circuit from the output of the shift register is applied to the input. The control circuits then cause the decoder register to shift right 16 times at a 307.2 KHz. rate, and shifts the 16 corrected bits into the 16 bit serial-in, parallel-out register, after which they are immediately transferred to the output register. This is accomplished during one cycle of the 19.2 KHz. input, so that continuous block transmission is possible.

When the 16 bit data word is transferred to the 22 bit output register, it is transferred as two ASCII coded characters along with the appropriate 0's and 1's for start-stop operation of the ASR-33 teletype. Transfer of the 16 data bits starts output control, which then causes the two characters to be shifted out serially on line at a 110 HZ. bit rate.

It is interesting to note that in terms of time required for accomplishing the various functions, the input or output of two characters requires approximately 0.2 second. Encoding the two characters into a

31 bit block and transmission (and reception) of this block, approximately 1.6 milliseconds. The received 31 bit block is next completely decoded and presented to the output register in 52 microseconds. This "mismatch" in timing is intentional and is, in part, a result of the decision to transfer blocks at 19.2 KHz. Decoding the entire block during one bit time also means no additional buffering, and switching between buffers is not required to output data to the teletype.

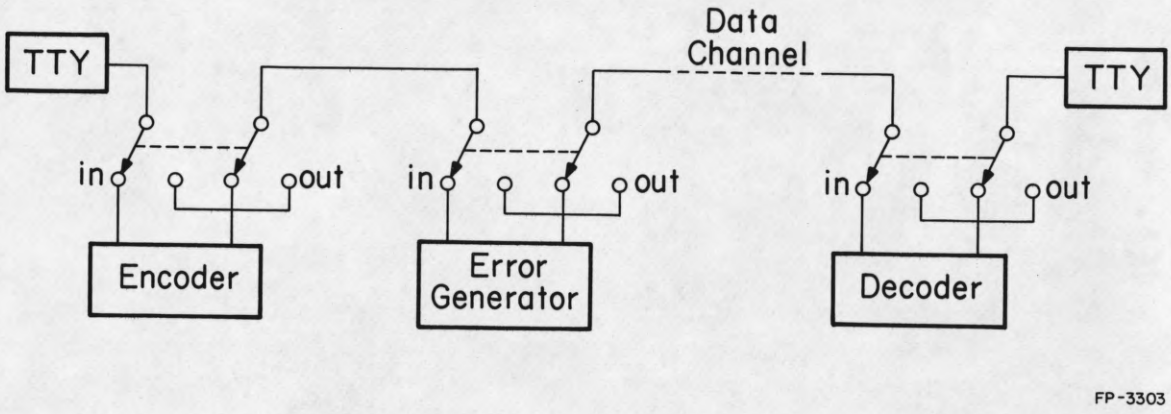

Figure 1. System Plan

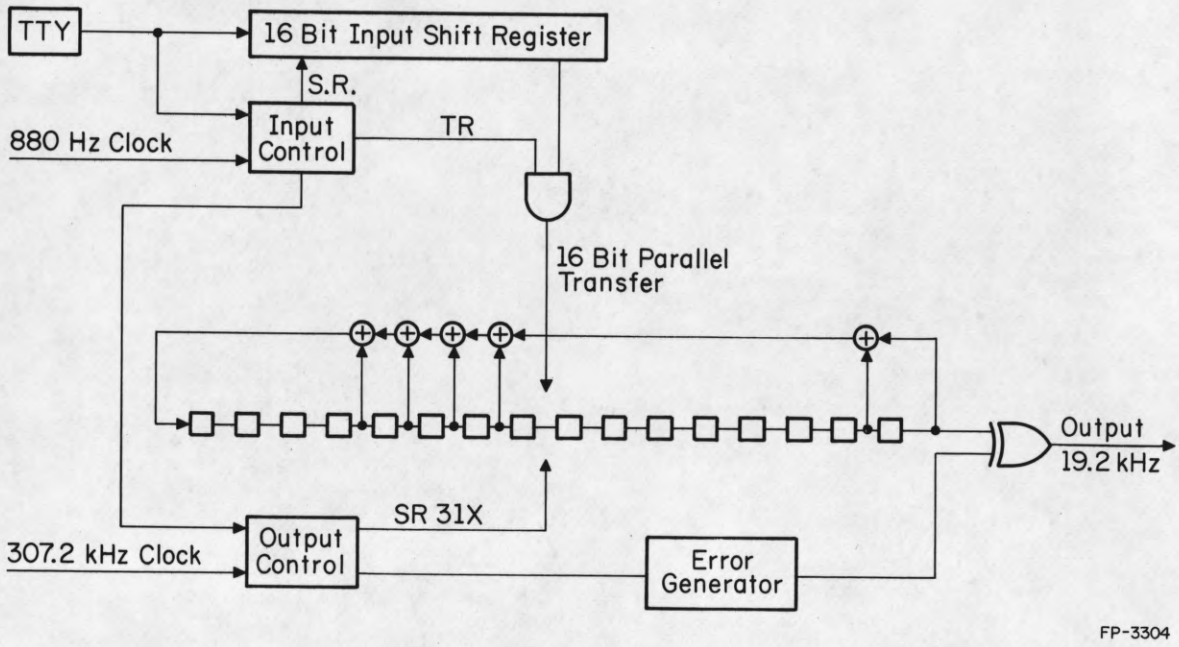

Figure 2. (31,16) Encoder and Error Generator

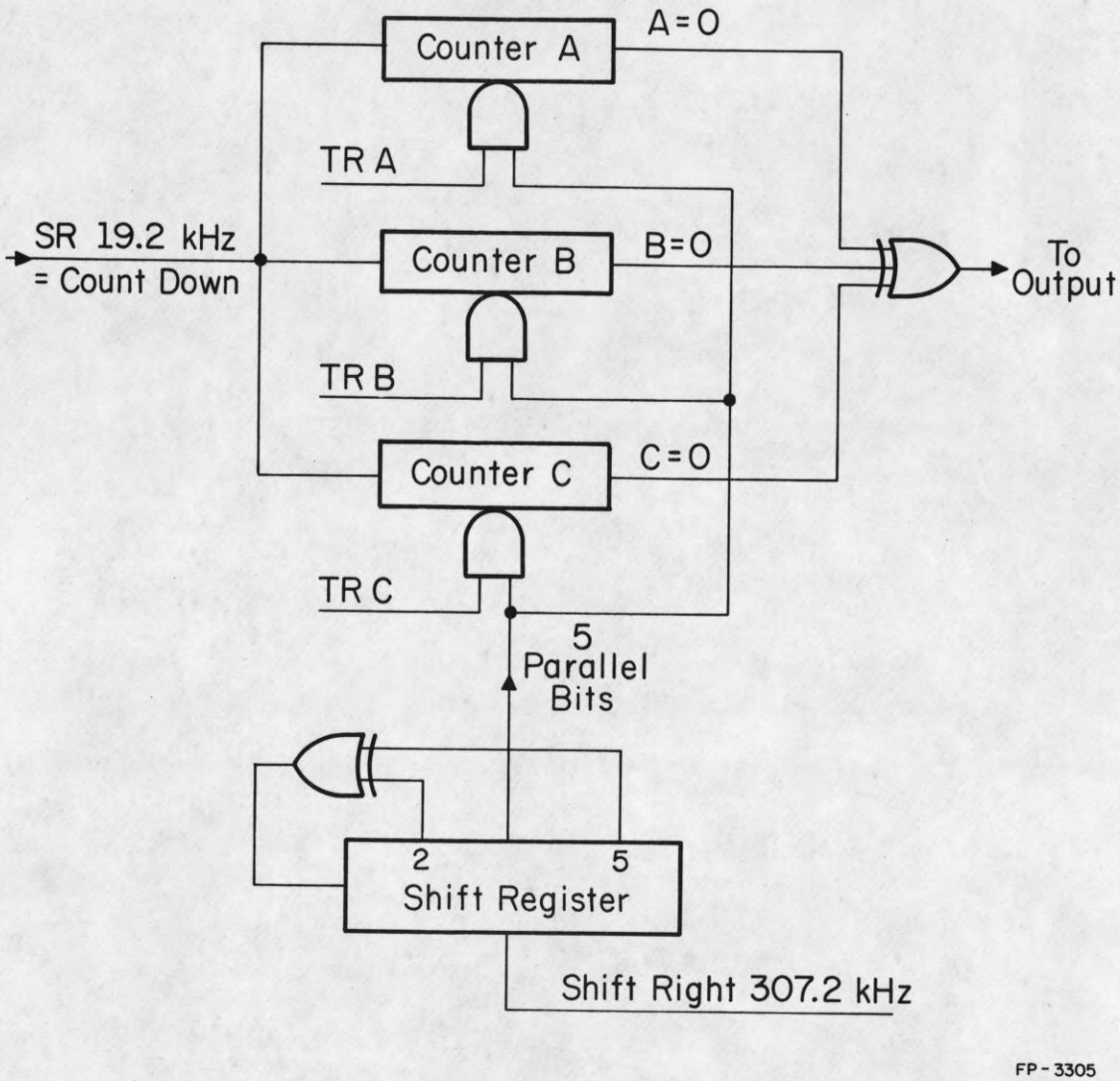

Figure 3. Serial Error Generator

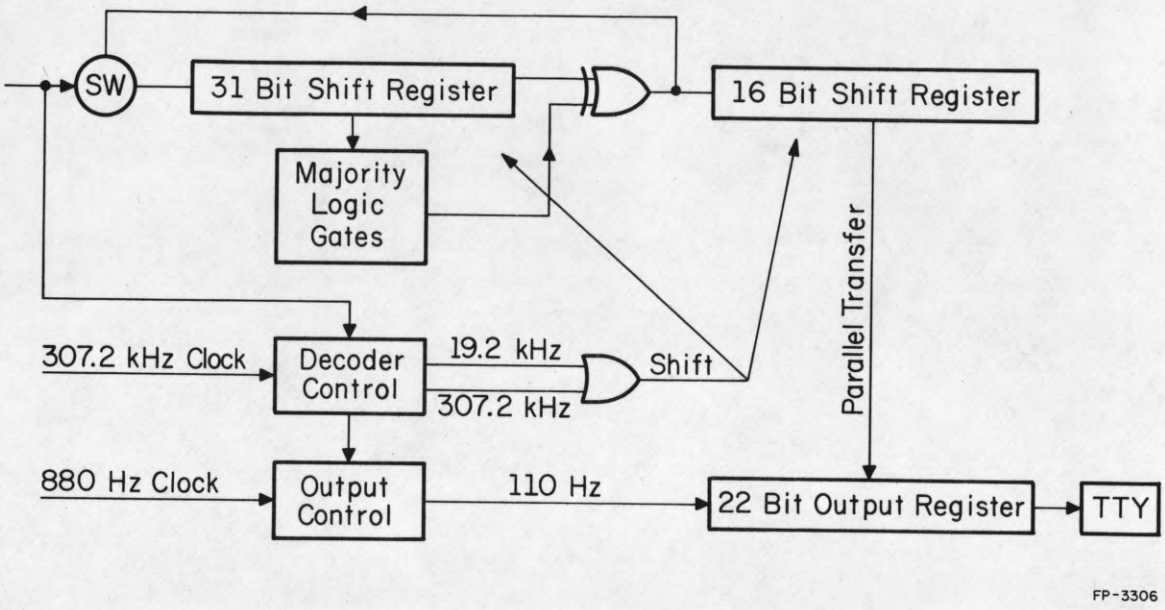

Figure 4. (31,16) Decoder and Output

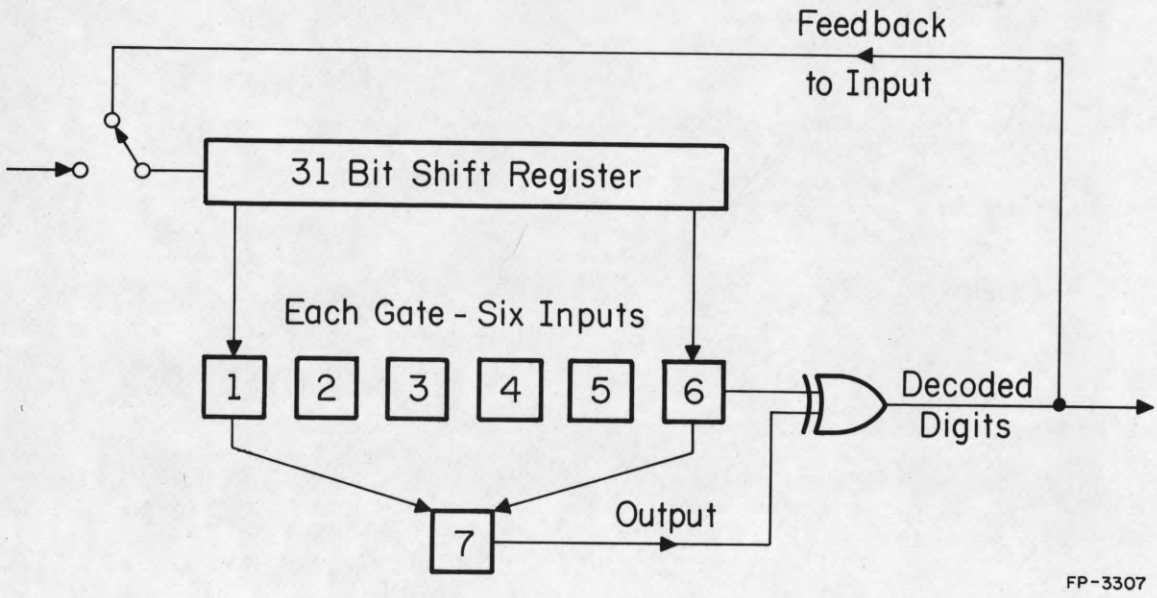

Figure 5. Decoder (31,16)

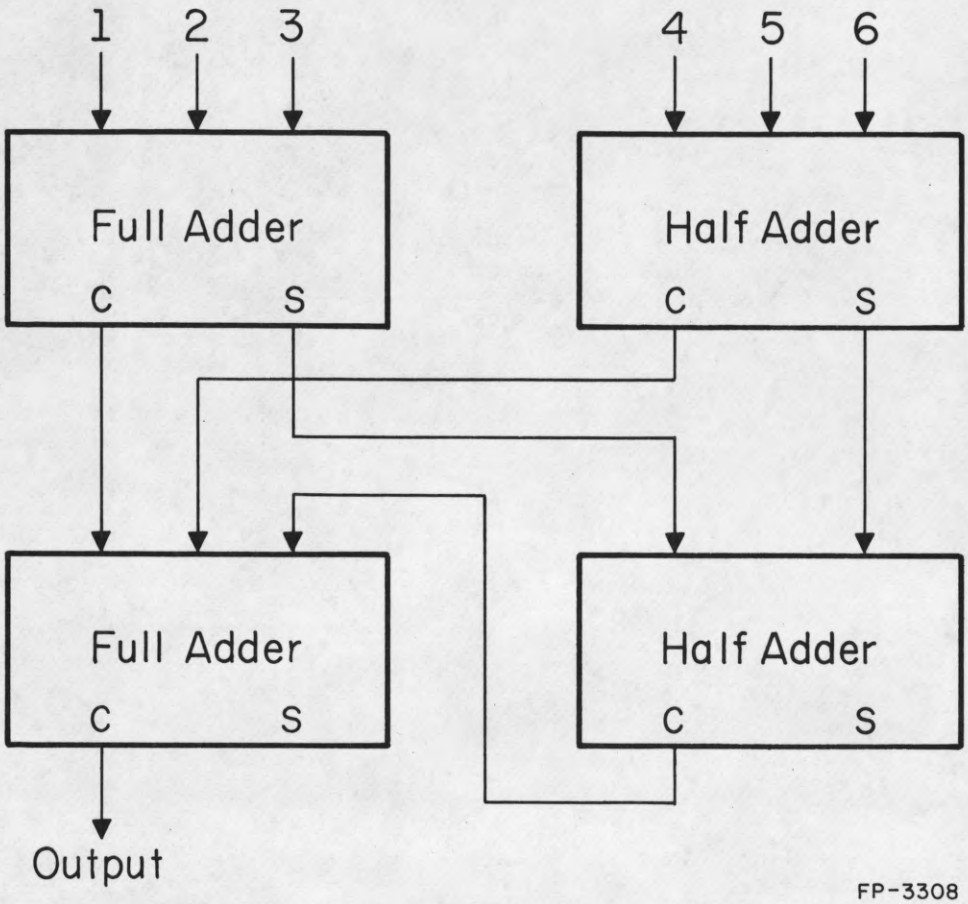

Figure 6. Majority Gate

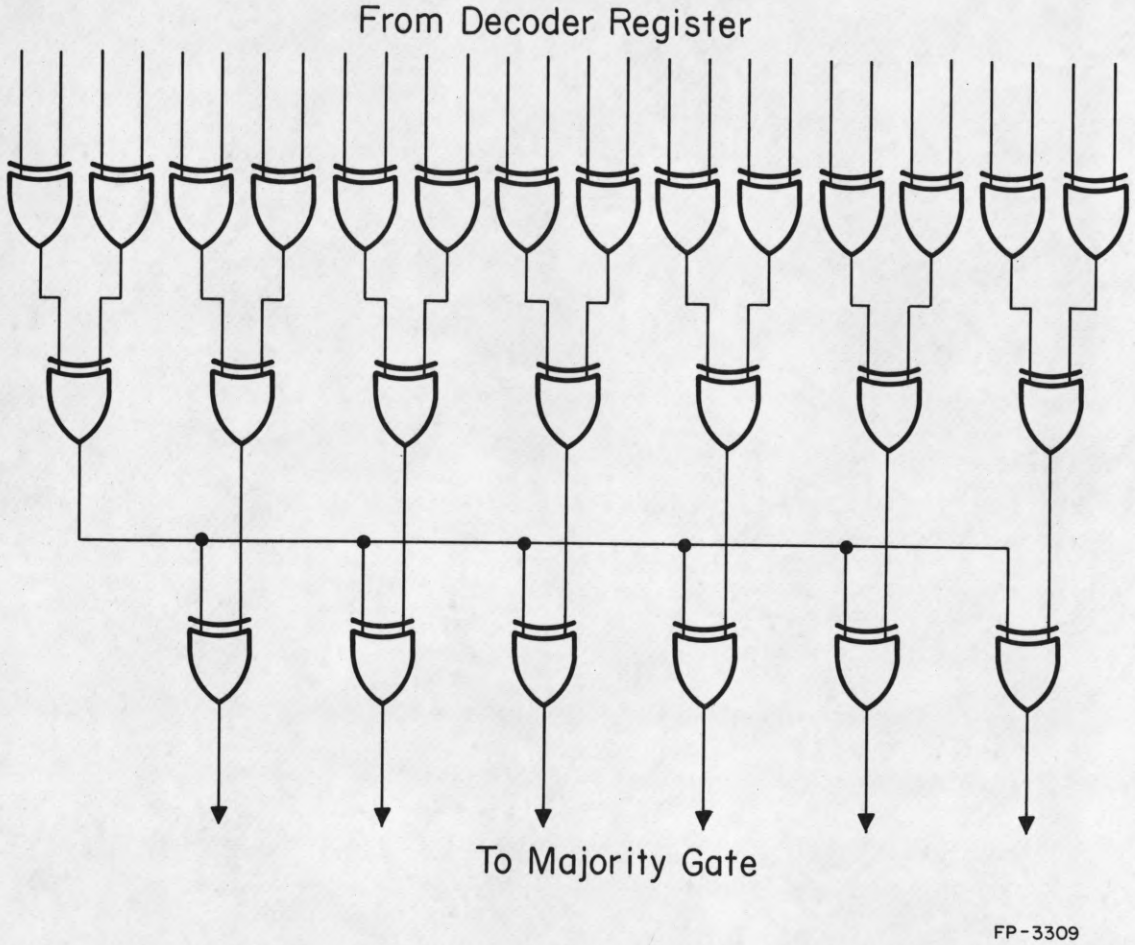

Figure 7. Exclusive-OR Gates

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY *(Corporate author)*
Coordinated Science Laboratory

2a. REPORT SECURITY CLASSIFICATION
UNCLASSIFIED

2b. GROUP

3. REPORT TITLE
EXPERIMENTAL UNIT FOR (31,16) BINARY CODE USING MAJORITY-LOGIC DECODING

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

5. AUTHOR(S) *(First name, middle initial, last name)*
R. Brown, C. L. Chen, R. T. Chien, D. Coad, S. Ng

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
December, 1972	15	0

8a. CONTRACT OR GRANT NO. DAAB-07-72-C-0259; F30602-72-C-0031

b. PROJECT NO.

c.

d.

9a. ORIGINATOR'S REPORT NUMBER(S)
R-594

9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*
UILU-ENG 72-2257

10. DISTRIBUTION STATEMENT
Approved for public release. Distribution unlimited.

11. SUPPLEMENTARY NOTES

12. SPONSORING MILITARY ACTIVITY
Joint Services Electronics Program through U. S. Army Electronics Command; Rome Air Development Center

13. ABSTRACT

This is an experimental unit which incorporates error correcting coding into digital data communication systems for increased reliability. A short, random correcting block code is used in this unit. The code is taken from the class of Euclidean geometry codes which can be decoded by simple majority logic. The unit is complete with an encoder which encodes a block of information digits into a codeword before transmission, a decoder which determines from each codeword the information digits it contains, and an error generator which simulates a noisy channel. For demonstration purposes teletype machines will be used as the data source and the destination of this unit.

DD FORM 1 NOV 65 1473

Security Classification

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Binary codes						
Majority-logic decoding						
Error-correcting codes						