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MATRIX SWITCHES AND ERROR CORRECTING CODES FROM BLOCK DESIGNS

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Abstract

Methods of obtaining matrix switches from block designs have been formulated by Singleton and Neumann. The first part of this report extends Singleton's method for designing unipolar switches to the design of bipolar switches. A new class of low noise switches is obtained by permutation of the winding matrix of noiseless switches and it is shown how these new switches are related to block designs.

The latter part of this report is concerned with methods of obtaining error detecting and error correcting codes from block designs. Some of these codes are found to be optimal.

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1. INTRODUCTION

Addressing is a significant problem in the design of random access magnetic memory core systems used in computers. Coincident current techniques for addressing are well known and widely used. In these systems the selected magnetic core is energized by the coincidence of currents in one horizontal and one vertical driver. In such systems each driver must provide a considerable amount of power and be bidirectional.

To avoid the need for high power drivers, load sharing matrix switches are used, in which the combined power output of a large number of drivers is received by the selected core. Such switches are noiseless if all the cores other than the selected core receive no excitation. The obvious advantage of such switches is that the power requirements of the drivers is greatly reduced. Moreover, such switches will continue to function even if a few drivers fail. However, these advantages are obtained at the cost of a more complex wiring system for the cores. In small memories, the matrix switch itself may be used for storage of information. In larger arrays, output windings on the cores of the matrix switches can be used to generate the read and write pulses for a coincident current magnetic memory array.

Recently a number of papers have appeared on the subject of load sharing matrix switches. Designs for noiseless switches have been suggested by Constantine [1], Marcus [2] and Chien [3]. The design of matrix switches using block designs has been studied by Singleton [4], Neumann [5], Minnick and Haynes [6].

In Chapter 2 the design of noiseless switches based on balanced block designs is discussed. The method of design of unipolar switches suggested by Singleton is extended to the design of bipolar switches also.

In Chapter 3, partially balanced block designs are used to design low noise matrix switches. Again, some of the material is due to Singleton. A new class of low noise switches is obtained by permuting the winding matrix in a particular manner. The connection between these switches and block designs is discussed. This part of the work appears to be original.

The connection between orthogonal matrices, error correcting codes, and matrix switches has been studied by Chien [7]. Bose and Shrikhande [8] have pointed out the connection between orthogonal Hadamard matrices, block designs and error correcting codes. The approach used in the above mentioned papers is generalized and extended to obtaining codes from block designs in Chapter 4. In some cases the codes are found to be optimal and meet the Plotkin [9] bound.

Switch Notation: A magnetic matrix switch is described by its winding matrix $W = [w_{ij}]$, its input matrix $C^r = [c^r_{ij}]$ for the read operation and its input matrix $C^w = [c^{w*}_{ij}]$ for the write operation. The winding matrix for a switch with v outputs and b inputs (excluding the bias input) is given by a v-by-(b+1) matrix. The magnitude of w_{ij} represents the number of turns of the j^{th} input wire on the i^{th} core, the sign of w_{ij} represents the direction of the winding. The $(b+1)^{th}$ input is for bias. In practice there may be two bias wires, one for read and one for write if the read and write bias are unequal. Sometimes it may be possible to get rid of the bias wires completely. The patterns used as read inputs are arranged

as the columns of the (b+1)-by-v read input matrix C^r. For most of the switches discussed here, the first b rows contain only 0 and $\pm$ 1, i.e. all the input drivers are assumed to have a current output of unity. The final row contains the entries for the bias level which may be different from 0 and $\pm$ 1. The v-by-v read output matrix is given by $X^r = [x^r_{ij}] = W.C^r$ where x^r_{ij} is the excitation of the i^{th} core by the j^{th} input pattern during the read operation. Similarly the write output matrix is given by $X^w = [x^w_{ij}] = W.C^w$.

A switch is unipolar if C^r and C^w have only nonnegative entires in their first b rows, and is bipolar if they contain negative entries also. The input drivers of a unipolar switch are unidirectional whereas the drivers of a bipolar switch are bidirectional.

A matrix switch is noiseless if for any input pattern used, only one output is excited, i.e. the read operation is noiseless if $X^r = pI$ and the write operation is noiseless if $X^w = -qI$ where I is the v-by-v identity matrix.

A switch is load sharing if a number of small inputs combine to give a large output. The load sharing factor is the ratio of the total output of the selected core to the output obtained if only one input driver was excited. If W contains only 0's and $\pm$ 1's then the load sharing factor is given by

$$p = \sum_j w_{ij} c_{ji} .$$

The efficiency of a noiseless switch is defined as

$$\eta = \frac{\left|\sum_j w_{ij}\ c_{ji}\right|}{\sum_j \left|w_{ij}\ c_{ji}\right|}$$

where $c_{ji} = c^r_{ji}$ for the read operation and $c_{ji} = c^w_{ji}$ for the write operation.

2. BALANCED BLOCK DESIGNS AND NOISELESS SWITCHES

In a balanced incomplete block design we have v objects arranged in b blocks, each block containing k distinct objects. Each object occurs r times and each pair of objects occur together in λ blocks.

Elementary conditions for the existence of a (v,k,r,b,λ) balanced block design are

i) $vr = bk$

ii) $\lambda(v-1) = r(k-1)$.

As a consequence of these conditions $b \geq v$. If $b = v$, $k = r$, we have a symmetric design, the first condition is satisfied immediately and the second reduces to $k(k-1) = \lambda(v-1)$.

Generally the above conditions are not sufficient for the existence of designs. Known existence theorems are discussed by Mann [10] and Hall [11].

A balanced incomplete block design is conveniently represented by its b-by-v incidence matrix $S = [s_{ij}]$

$s_{ij} = 1$ if the i^{th} block contains the j^{th} element

$= 0$ if the i^{th} block does not contain the j^{th} element.

Each row contains k ones and each column contains r ones.

$$\sum_{j=1}^{b} s_{ja}\, s_{jd} = r \qquad \text{if } a = d$$

$$= \lambda \qquad \text{if } a \neq d \ .$$

Therefore the product $(S)^T.S = (r-\lambda)I + \lambda U$ where U is a v-by-v matrix of all ones.

The complement of a (v,k,r,b,λ) design is obtained by replacing ones by zeros and zeros by ones in S. This gives the incidence matrix $S^c = [s^c_{ij}]$ of a $(v,v-k,b-r,b,b+\lambda-2r)$ balanced block design, and

$$\sum_{j=1}^{b} s^c_{ja}\, s^c_{jd} = b-r \quad \text{if } a=d$$

$$= b+\lambda-2r \quad \text{if } a \neq d$$

Therefore,

$$(S^c)^T \cdot S^c = (r-\lambda)I + (b+\lambda-2r)U$$

Also

$$\sum_{j=1}^{b} s_{ja}\, s_{jd} = \sum_{j=1}^{b} s_{ja}\, s^c_{jd} = 0 \quad \text{if } a = d$$

$$= (r-\lambda) \quad \text{if } a \neq d$$

Therefore

$$(S^c)^T \cdot S = (S)^T \cdot S^c = -(r-\lambda)I + (r-\lambda)U$$

2.1 Design of Switches Based on Balanced Block Designs

The design procedure used here is the one used by Singleton [4] for unipolar switches. The design procedure is extended to bipolar switches. In type I switches all input windings are in the same direction. Type II switches have core windings in both directions.

2.1.1 Type I Switch

a) Unipolar

$$W = \begin{pmatrix} S \\ u \end{pmatrix}^T$$

where u is a row of ones and represents the bias winding.

$$C^r = \begin{pmatrix} S \\ au \end{pmatrix}$$

$$C^w = \begin{pmatrix} S^c \\ du \end{pmatrix}$$

$$X^r = (S)^T \cdot S + aU = (r-\lambda)I + (\lambda+a)U.$$

Putting the bias level $a = -\lambda$ gives

$$X^r = (r-\lambda)I$$

making the read operation noiseless.

Load sharing factor for read operation = $p_r = (r-\lambda)$.

Read efficiency $\eta_r = \frac{r-\lambda}{r+\lambda}$

$$X^w = (S)^T \cdot S^c + dU = -(r-\lambda)I + (r-\lambda+d)U.$$

Putting the bias level $d = \lambda - r$ gives

$$X^w = -(r-\lambda)I$$

making the write operation noiseless.

Load sharing factor for write operation = $p_w = (r-\lambda)$.

Write efficiency $\eta_w = \frac{r-\lambda}{r-\lambda} = 1$.

Such a switch has b + 2 inputs and v outputs. Two bias windings are required since $a \neq d \neq 0$.

b) Bipolar

$$W = \begin{pmatrix} S \\ u \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S - S^c \\ au \end{pmatrix}$$

$$C^w = -C^r$$

$$X^r = (S)^T \cdot S - (S)^T \cdot S^c + aU$$

$$= 2(r-\lambda)I + (2\lambda - r + a)U$$

Putting bias level $a = r - 2\lambda$ gives

$$X^r = 2(r-\lambda)I$$

Load sharing factor $p_r = 2(r-\lambda)$.

Read efficiency $\eta_r = \frac{2(r-\lambda)}{r+|r-2\lambda|}$.

If $r \geq 2\lambda$ $\quad \eta_r = 1$

$r < 2\lambda$ $\quad \eta_r = \frac{r-\lambda}{\lambda}$

Since

$$C^w = -C^r, \; X^w = -X^r = -2(r-\lambda)I$$

and write efficiency $\eta_w = \eta_r$. If $r = 2\lambda$, $a = 0$ and no bias winding is required.

2.1.2 Example of Type I Switch

This switch is based on the (4,2,3,6,1) balanced block design.

$$S = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix}$$

Unipolar switch

$$W = \begin{pmatrix} S \\ u \end{pmatrix}^T = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 \end{bmatrix}$$

$a = -\lambda = -1, \qquad d = \lambda - r = -2$

$$C^r = \begin{pmatrix} S \\ -u \end{pmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \\ -1 & -1 & -1 & -1 \end{bmatrix}, \qquad C^w = \begin{pmatrix} S^c \\ -2u \end{pmatrix} = \begin{bmatrix} 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ -2 & -2 & -2 & -2 \end{bmatrix}$$

$$X^r = 2I = \begin{bmatrix} 2 & 0 & 0 & 0 \\ 0 & 2 & 0 & 0 \\ 0 & 0 & 2 & 0 \\ 0 & 0 & 0 & 2 \end{bmatrix} \quad X^w = -2I$$

The switch has six regular inputs and two bias inputs. The number of outputs is 4.

Load sharing factor $p_r = p_w = 2$.

Read efficiency $\eta_r = \frac{1}{2}$.

Write efficiency $\eta_w = 1$.

Bipolar switch

The W matrix is the same as for the unipolar switch

$$a = r - 2\lambda = 1$$

$$C^r = \begin{pmatrix} S - S^c \\ u \end{pmatrix} = \begin{bmatrix} 1 & 1 & -1 & -1 \\ -1 & -1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ -1 & 1 & -1 & 1 \\ 1 & -1 & -1 & 1 \\ -1 & 1 & 1 & -1 \\ 1 & 1 & 1 & 1 \end{bmatrix}$$

$$C^w = -C^r$$

$$X^r = 4I = \begin{bmatrix} 4 & 0 & 0 & 0 \\ 0 & 4 & 0 & 0 \\ 0 & 0 & 4 & 0 \\ 0 & 0 & 0 & 4 \end{bmatrix} \quad X^w = -4I$$

Load sharing factor $p_r = p_w = 4$.

Efficiency $\eta_r = \eta_w = 1$.

The switch has 7 inputs and 4 outputs.

2.1.3 Type II Switch

a) Unipolar

$$W = \begin{pmatrix} S & -S^c \\ u & \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S \\ au \end{pmatrix}$$

$$C^w = \begin{pmatrix} S^c \\ du \end{pmatrix}$$

$$X^r = (S)^T \cdot S - (S^c)^T \cdot S + aU$$

$$= 2(r-\lambda)I + (2\lambda - r + a)U$$

Putting bias level $a = r - 2\lambda$ gives

$$X^r = 2(r-\lambda)I.$$

Load sharing factor $p_r = 2(r-\lambda)$.

Efficiency $\eta_r = \frac{2(r-\lambda)}{r + |r-2\lambda|} = 1$ if $r \geq 2\lambda$,

$$= \frac{r-\lambda}{\lambda} \text{ if } r < 2\lambda.$$

If $r=2\lambda$ $a=0$ and one bias wire can be eliminated,

$$X^w = (S)^T \cdot S^c - (S^c)^T \cdot S^c + dU$$

$$= -2(r-\lambda)I + (3r - 2\lambda - b + d)U.$$

Putting bias level $d = b + 2\lambda - 3r$

$$X^w = -2(r-\lambda)I$$

Load sharing factor $p_w = 2(r-\lambda)$

Efficiency $\eta_w = \dfrac{2(r-\lambda)}{(b-r) + |b+2\lambda-3r|} = 1$ if $3r \geq b+2\lambda$

$= \dfrac{r-\lambda}{b+\lambda-2r}$ if $3r < b+2\lambda$

If $r=2\lambda$ or $3r = b+2\lambda$ then one of the bias windings can be eliminated since either $a = 0$ or $d = 0$. It is not possible to make both a and d zero.

$a = 0$ implies $r = 2\lambda$

$d = 0$ implies $3r = b+2\lambda$

Then $b = 3r-2\lambda = 2r$.

Also $vr = bk$ and substituting $b = 2r$ gives $v = 2k$.

But the condition $\lambda(v-1) = r(k-1)$ implies $v = 2k-1$ which is contradictory to the earlier found value for v.

This switch will have at least b+1 inputs and v outputs. It is possible to make both η_r and η_w equal to 1 if $r \geq 2\lambda$ and $3r \geq b+2\lambda$. Switches derived from (4t-1, 2t, 2t, 4t-1, t) and (4t-1, 2t-1, 2t-1, 4t-1, t-1) designs which are closely related to Hadamard matrices have this property.

b) Bipolar

$$W = \begin{pmatrix} S-S^c \\ u \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S-S^c \\ au \end{pmatrix}$$

$$C^w = -C^r$$

$$X^r = (S)^T \cdot S + (S^c)^T \cdot S^c - (S)^T \cdot S^c - (S^c)^T \cdot S + aU$$

$$= 4(r-\lambda)I + (b+4\lambda - 4r + a)U$$

Putting bias level $a = -(b + 4\lambda - 4r)$

$$X^r = 4(r-\lambda)I.$$

Load sharing factor $p_r = 4(r-\lambda)$.

Efficiency $\eta_r = \frac{4(r-\lambda)}{b+|b+4\lambda-4r|} = 1$ if $b \leq 4(r-\lambda)$.

$$= \frac{4(r-\lambda)}{2b-4(r-\lambda)} \quad \text{if } b > 4(r-\lambda).$$

Since $C^w = -C^r$, $X^w = -X^r = -4(r-\lambda)I$, $\eta_r = \eta_w$. If $b = 4(r-\lambda)$ $a = 0$, no bias winding is required and the switch also has efficiency 1.

2.1.4 Example of Type II Switch

The (4,2,3,6,1) design is used again.

Unipolar switch.

$$W = \begin{pmatrix} S \\ u \end{pmatrix}^T = \begin{bmatrix} 1 & -1 & 1 & -1 & 1 & -1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 \\ -1 & 1 & 1 & -1 & -1 & 1 & 1 \\ -1 & 1 & -1 & 1 & 1 & -1 & 1 \end{bmatrix}$$

$a = r-2\lambda = 1$, $d = b+2\lambda-3r = -1$.

$$C^r = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 \end{bmatrix}, \qquad C^w = \begin{bmatrix} 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ -1 & -1 & -1 & -1 \end{bmatrix}$$

$$X^r = 4I = \begin{bmatrix} 4 & 0 & 0 & 0 \\ 0 & 4 & 0 & 0 \\ 0 & 0 & 4 & 0 \\ 0 & 0 & 0 & 4 \end{bmatrix}, \quad X^w = -4I$$

Switch has 8 inputs, 4 outputs.

Load sharing factor $p_r = p_w = 4$.

Efficiency $\eta_r = \eta_w = 1$.

Bipolar switch.

The W matrix is the same as for the unipolar switch.

$$a = -(b+4\lambda-4r) = 2$$

$$C^r = \begin{bmatrix} 1 & 1 & -1 & -1 \\ -1 & -1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ -1 & 1 & -1 & 1 \\ 1 & -1 & -1 & 1 \\ -1 & 1 & 1 & -1 \\ 2 & 2 & 2 & 2 \end{bmatrix}, \quad C^w = -C^r$$

$$X^r = 8I = \begin{bmatrix} 8 & 0 & 0 & 0 \\ 0 & 8 & 0 & 0 \\ 0 & 0 & 8 & 0 \\ 0 & 0 & 0 & 8 \end{bmatrix}, \quad X^w = -8I$$

Load sharing factor $p_r = p_w = 8$.

Efficiency $\eta_r = \eta_w = 1$.

The class of switches published by Constantine [1] are type II unipolar switches based on the block designs with parameters (2^{p-1}, 2^{p-2}, $2^{p-1}-1$, 2^p-2, $2^{p-2}-1$). For these designs a=1, d=-1 and the designs yield switches with 2^{p-1} outputs with 2^p inputs, a load sharing factor $p_r = p_w = 2^{p-1}$ and efficiency $\eta_r = \eta_w = 1$. The class of switches suggested by Marcus [2] are

identified with symmetrical designs of the type $(2^p-1,\ 2^{p-1}-1,\ 2^{p-1}-1,\ 2^p-1,\ 2^{p-2}-1)$. These switches are a subclass of the switches suggested by Chien [3] which are type II switches based on (4t-1, 2t-1, 2t-1, 4t-1, t-1) designs. For these switches a=1, d=0 and the switches have 4t-1 outputs with 4t inputs. The load sharing factor $p_r = p_w = 2t$ and efficiency $\eta_r = \eta_w = 1$. These designs are closely related to Hadamard matrices.

2.2 General Design

So far only switches whose winding matrices W contain entries of 0 and $\pm$ 1 have been discussed. A general design procedure such that W can contain other entries also is outlined here.

a) Unipolar switch

$$W = \begin{pmatrix} \alpha S & - \beta S^c \\ u & \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S \\ au \end{pmatrix}$$

$$C^w = \begin{pmatrix} S^c \\ du \end{pmatrix}$$

$$X^r = \alpha (S)^T \cdot S - \beta (S^c)^T \cdot S + aU$$

$$= (\alpha+\beta)(r-\lambda)I + (\alpha\lambda + \beta\lambda - \beta r + a)U$$

Putting bias level $a = \beta r - (\alpha+\beta)\lambda$ gives

$$X^r = (\alpha+\beta)(r-\lambda)I$$

$$\eta_r = \frac{(\alpha+\beta)(r-\lambda)}{\alpha r + |\beta r - (\alpha+\beta)\lambda|} = 1 \text{ if } \beta r \geq (\alpha+\beta)\lambda$$

$$= \frac{(\alpha+\beta)(r-\lambda)}{(\alpha-\beta)r + (\alpha+\beta)\lambda} \text{ if } \beta r < (\alpha+\beta)\lambda$$

$$X^w = \alpha (S)^T \cdot S^c - \beta (S^c)^T \cdot S^c + dU$$

$$= -(\alpha+\beta)(r-\lambda)I + (\alpha r - \alpha\lambda - \beta b - \beta\lambda + 2\beta r + d)U$$

Putting bias level $d = \beta(b-r) - (\alpha+\beta)(r-\lambda)$,

$$X^w = -(\alpha+\beta)(r-\lambda)I$$

$$\eta_w = \frac{(\alpha+\beta)(r-\lambda)}{\beta(b-r) + |\beta(b-r)-(\alpha+\beta)(r-\lambda)|}$$

If $(a+\beta)(r-\lambda) \geq \beta(b-r)$, $\eta_w = 1$.

If $(\alpha+\beta)(r-\lambda) < \beta(b-r)$, $\eta_w = \frac{(\alpha+\beta)(r-\lambda)}{2\beta(b-r)-(\alpha+\beta)(r-\lambda)}$

α and β can be chosen to give either $a=0$ or $d=0$, hence getting rid of one bias winding. However, it is not possible to make both a and d zero.

$a=0$ gives $\beta r = (\alpha+\beta)\lambda$

$d=0$ gives $\beta b - (\alpha+\beta)r = \beta r - (\alpha+\beta)\lambda = 0$.

The necessary condition $vr=bk$ implies

$$\beta vr = (\alpha+\beta)\lambda v$$

and $\beta bk = (\alpha+\beta)rk$.

Therefore,

$$(\alpha+\beta)(\lambda v-rk) = 0.$$

If $(\alpha+\beta) = 0$, $X^r = X^w = 0$, i.e. no output from the switch. If $\lambda v=rk$ the condition $\lambda(v-1) = r(k-1)$ implies $\lambda=r$, in which case S consists of all zeros or all ones.

Therefore, a unipolar switch based on a (v,k,r,b,λ) design will have at least $(b+1)$ inputs and since $v \leq b$ the number of inputs is always larger than the number of outputs.

b) Bipolar switch

$$W = \begin{pmatrix} \alpha S - \beta S^c \\ u \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S - S^c \\ au \end{pmatrix}, \quad C^w = -C^r$$

$$X^r = \alpha(S)^T \cdot S - \beta(S^c) \cdot S - \alpha(S)^T \cdot S^c + \beta(S^c) \cdot S^c + aU$$

$$= 2(\alpha+\beta)(r-\lambda)I + (\beta b + 2\lambda(\alpha+\beta) - r(\alpha+3\beta) + a)U$$

Putting bias level $a = -(\alpha(2\lambda - r) + \beta(b+2\lambda-3r))$.

$$X^r = 2(\alpha+\beta)(r-\lambda)I$$

$$X^w = -2(\alpha+\beta)(r-\lambda)I$$

$$\eta_r = \eta_w = \frac{2(\alpha+\beta)(r-\lambda)}{\alpha r + \beta(b-r) + |\alpha(2\lambda-r) + \beta(b+2\lambda-3r)|}$$

If $(\alpha(2\lambda-r) + \beta(b+2\lambda-3r)) \leq 0$, $\eta_r = \eta_w = 1$.

If $(\alpha(2\lambda-r) + \beta(b+2\lambda-3r)) > 0$, $\eta_r = \eta_w = \frac{(\alpha+\beta)(r-\lambda)}{\alpha\lambda + \beta(b+\lambda-2r)}$.

$a=0$ if $\alpha(2\lambda-r) = \beta(3r-b-2\lambda)$ in which case a bias winding is not required. This can easily be achieved by putting

$$\alpha = (3r-b-2\lambda)$$

$$\beta = (2\lambda-r).$$

Both α and β will never be zero because $\beta=0$ implies $r=2\lambda$. Since $\lambda(v-1)=r(k-1)$ we have $v=2k-1$. $\alpha=0$ implies $b=2r$. Since $vr=bk$ we have $v=2k$ which is contradictory to $v=2k-1$.

The number of inputs to a bipolar switch is b if the bias wires are eliminated. The number of outputs is v. Since $b \geq v$, the number of inputs cannot be less than the number of outputs. The bound $b=v$ is achieved only in the case of symmetrical designs. Therefore, a unipolar switch derived from a balanced block design has at least v+1 inputs for v outputs and a bipolar switch at least v inputs for v outputs. Actually, it is easily seen that no noiseless switch can have more outputs than inputs. Since $X = W.C$ and in a noiseless switch $X = pI$, the rank of X is equal to v, the number

of outputs. Therefore, the ranks of W and C must also be at least v and this implies that the number of inputs must also be at least v.

3. PARTIALLY BALANCED BLOCK DESIGNS AND LOW NOISE SWITCHES

An incomplete block design is said to be partially balanced if it is an arrangement of v objects into b groups, each containing $k < v$ distinct objects such that

i) Each object appears in r groups,

ii) Each object has n_i i^{th} associates $i = 1, 2, \ldots m$,

iii) Any pair of objects are i^{th} associates for some $i = 1, 2, \ldots m$,

iv) Any two objects that are i^{th} associates appear together in λ_i blocks.

If m=1, the resulting design is balanced. If m=2, designs are partially balanced with 2 associate classes. These designs have been studied extensively by Bose, Clatworthy and Shrikhande [12] and Clatworthy [13]. Designs with more than two associate classes have not been studied to any great extent.

Necessary conditions for a partially balanced incomplete block design with 2 associate classes are

i) $vr=bk$,

ii) $n_1+n_2 = v-1$,

iii) $n_1\lambda_1+n_2\lambda_2 = r(k-1)$.

The condition $b \geq v$ which holds in the case of balanced designs is no longer true and switches with more outputs than inputs can be designed using the same techniques as were used earlier. However, such switches will not be noiseless.

The incomplete block design can be represented by its incidence matrix S

$$\sum_{j=1}^{b} s_{ja}\, s_{jd} = r \text{ if } a=b$$

$$= \lambda_i \text{ if } a \neq b \text{ and the } a^{th} \text{ and } b^{th} \text{ objects are } i^{th} \text{ associates.}$$

To facilitate notation we define the matrices $U^1 = [u^1_{jk}]$ and $U^2 = [u^2_{jk}]$ which are v-by-v matrices such that

$u^1_{jk} = 1$, if the j^{th} and k^{th} objects are 1^{st} associates

$= 0$, otherwise.

$u^2_{jk} = 1$, if the j^{th} and k^{th} objects are 2^{nd} associates

$= 0$, otherwise.

Therefore, the matrix $E = [e_{jk}] = (S)^T \cdot S$ has elements

$e_{jk} = r$, if $j=k$

$= \lambda_i$, if $j \neq k$ and the j^{th} and k^{th} objects are i^{th} associates $i=1,2$.

Hence,

$$E = rI + \lambda_1 U^1 + \lambda_2 U^2.$$

The complement of a partially balanced incomplete block design with 2 associate classes (abbreviated to p.b.i.b(2) design) with parameters $(v,k,r,b,\lambda_1, \lambda_2, n_1, n_2)$ is a p.b.i.b.(2) design with parameters $(v,v-k,b-r,b,b-2r+\lambda_1,b-2r+\lambda_2,n_1,n_2)$ and if the j^{th} and k^{th} objects are i^{th} associates in the original design, they are also i^{th} associates in the complimentary design. S^c is the incidence matrix of the complimentary design and is obtained by interchanging ones and zeros in S. The matrix

$F = [f_{jk}] = (S^c)^T \cdot S^c$ has elements

$$f_{jk} = b-r, \text{ if } j=k$$

$$= b-2r+\lambda_i, \text{ if } j \neq k \text{ and the } j^{th} \text{ and } k^{th} \text{ objects are } i^{th} \text{ associates.}$$

Hence,

$$F = (b-r)I + (b-2r+\lambda_1)U^1 + (b-2r+\lambda_2)U^2.$$

The matrix $G = [g_{jk}] = (S)^T \cdot S^c = (S^c)^T \cdot S$ has elements

$$g_{jk} = 0, \text{ if } j=k$$

$$= r-\lambda_i, \text{ if } j \neq k \text{ and the } j^{th} \text{ and } k^{th} \text{ objects are } i^{th} \text{ associates.}$$

Hence,

$$G = (r-\lambda_1)U^1 + (r-\lambda_2)U^2.$$

Since the switches based on p.b.i.b.(2) designs are not noiseless it is worthwhile to discuss the bias scheme and the method for generating the write pulse. The bias scheme depends on what sort of noise can be tolerated in the unselected cores. One possible scheme (referred to as scheme 1) is to choose the bias in such a way that only the selected core receives positive excitation, all other cores receiving zero or negative excitation. Another possible scheme (scheme 2) would be to minimize the magnitude of the excitation of the unselected cores. Scheme 2 will work satisfactorily only if the maximum positive excitation received by any unselected core is insufficient to cause it to switch from one state to the other. In both these schemes only the selected core gives an output if the B-H hysterisis loop of the cores is perfectly rectangular. Since this is not true in practice, the unselected cores will have a slight noise output. Other bias schemes may

be used depending on the specifications of the particular switch.

When a read pulse is generated, only the selected core gets enough positive excitation to switch from one state to the other. Now if a bias wire provides negative excitation to all the cores, only the one previously selected will switch back to its original state, thus generating a write pulse. This method can be employed for obtaining a write pulse. Some noise output will occur in the unselected core due to the deviation of the B-H characteristic from the perfect rectangle. Alternatively the same procedure as was used in noiseless switches can be used.

3.1 Design of Switches Based on p.b.i.b.(2) Designs

3.1.1 Type I Switch

a) Unipolar

$$W = \begin{pmatrix} S \\ u \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S \\ au \end{pmatrix}$$

$$X^r = (S)^T \cdot S + aU$$

$$= (r+a)I + (\lambda_1+a)U^1 + (\lambda_2+a)U^2.$$

Using scheme 1 for bias and using the convention $\lambda_1 > \lambda_2$, put $a = -\lambda_1$

$$X^r = (r-\lambda_1)I - (\lambda_1-\lambda_2)U^2$$

or using scheme 2, put $a = -\frac{(\lambda_1+\lambda_2)}{2}$

$$X^r = (r-\frac{\lambda_1-\lambda_2}{2})I + (\frac{\lambda_1-\lambda_2}{2})U^1 - (\frac{\lambda_1-\lambda_2}{2})U^2.$$

Load sharing factor $p_r = (r+a)$.

If the write pulse is not generated by simply exciting a single bias

wire we can use

$$C^w = \begin{pmatrix} S^c \\ du \end{pmatrix}$$

$$X^w = (S)^T \cdot S^c + dU$$

$$= dI + (r-\lambda_1+d)U^1 + (r-\lambda_2+d)U^2.$$

If

$$d = -(r+a)$$

$$X^w = -X^r$$

Load sharing factor $p_w = (r+a)$.

b) Bipolar

$$W = \begin{pmatrix} S \\ u \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S-S^c \\ au \end{pmatrix}$$

$$X^r = (S)^T \cdot S - (S)^T \cdot S^c + aU$$

$$= (r+a)I + (2\lambda_1 - r+a)U^1 + (2\lambda_2 - r+a)U^2.$$

If bias scheme 1 is employed use

$$a = -(2\lambda_1 - r).$$

If bias scheme 2 is employed use

$$a = -(\lambda_1 + \lambda_2 - r).$$

$$C^w = -\begin{pmatrix} S-S^c \\ du \end{pmatrix}$$

$$X^w = -(r+d)I - (2\lambda_1 - r+d)U^1 - (2\lambda_2 - r+d)U^2.$$

Putting d=a gives $X^w = -X^r$.

Load sharing factor = (r+a).

3.1.2 Example

These switches are based on a block design with parameters (v=12, r=4, k=6, b=8, λ_1=2, λ_2=0, n_1=10, n_2=1) and give 9 input (including bias) - 12

output switches.

$$S = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 \end{bmatrix}$$

For the unipolar switch, using $a = -\left(\frac{\lambda_1+\lambda_2}{2}\right) = -1$ we get

$$X^r = \begin{bmatrix} 3 & 1 & 1 & 1 & 1 & 1 & -1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 3 & 1 & 1 & 1 & 1 & 1 & -1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 3 & 1 & 1 & 1 & 1 & 1 & -1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 3 & 1 & 1 & 1 & 1 & 1 & -1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 3 & 1 & 1 & 1 & 1 & 1 & -1 & 1 \\ 1 & 1 & 1 & 1 & 1 & 3 & 1 & 1 & 1 & 1 & 1 & -1 \\ -1 & 1 & 1 & 1 & 1 & 1 & 3 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & 1 & 1 & 1 & 1 & 3 & 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & 1 & 1 & 1 & 1 & 1 & 3 & 1 & 1 & 1 \\ 1 & 1 & 1 & -1 & 1 & 1 & 1 & 1 & 1 & 3 & 1 & 1 \\ 1 & 1 & 1 & 1 & -1 & 1 & 1 & 1 & 1 & 1 & 3 & 1 \\ 1 & 1 & 1 & 1 & 1 & -1 & 1 & 1 & 1 & 1 & 1 & 3 \end{bmatrix}$$

Load sharing factor = 3.

For the bipolar switch, using a=2,

$$X^r \text{ (bipolar)} = 2X^r \text{ (unipolar)}.$$

Load sharing factor = 6.

3.1.3 Type II Switch

a) Unipolar

$$W = \begin{pmatrix} S-S^c \\ u \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S \\ au \end{pmatrix}$$

$$X^r = (S)^T \cdot S - (S^c)^T \cdot S + aU$$

$$= (r+a)I + (2\lambda_1 - r + a)U^1 + (2\lambda_2 - r + a)U^2,$$

which is the same as the type I bipolar switch.

Using

$$C^w = \begin{pmatrix} S^c \\ du \end{pmatrix}$$

$$X^w = (S)^T \cdot S^c - (S^c)^T \cdot S^c + dU$$

$$= -(b-r-d)I - (2\lambda_1 - 3r + b - d)U^1 - (2\lambda_2 - 3r + b - d)U^2.$$

Putting $d = (b-2r-a)$ gives $X^w = -X^r$.

Load sharing factor = $(r+a)$.

b) Bipolar

$$W = \begin{pmatrix} S-S^c \\ u \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S-S^c \\ au \end{pmatrix}$$

$$X^r = (b+a)I + (b-4r+4\lambda_1+a)U^1 + (b-4r+4\lambda_2+a)U^2.$$

Using scheme 1 for bias

$$a = -(b-4r+4\lambda_1).$$

Using scheme 2

$$a = -(b-4r+2\lambda_1+2\lambda_2) \text{ in which case}$$

$$X^r = (4r-2\lambda_1-2\lambda_2)I + 2(\lambda_1-\lambda_2)U^1 - 2(\lambda_1-\lambda_2)U^2.$$

Load sharing factor = (b+a).

Using $C^w = -C^r$ gives $X^w = -X^r$.

3.1.4 Example

Using the same design as was used in the previous example, the unipolar type II switch yields a switch identical to the type I bipolar switch. The type II bipolar switch using a=4 gives X^r with diagonal entries of 12 and off diagonal entries of $\pm$ 4. Load sharing factor = 12.

3.2 General Design

As in the case of noiseless switches, a general design procedure can be formed, which offers a choice of more parameters to the designer.

a) Unipolar

$$W = \begin{pmatrix} \alpha S - \beta S^c \\ u \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S \\ au \end{pmatrix}$$

$$X^r = \alpha (S)^T \cdot S - \beta (S^c)^T \cdot S + aU$$

$$= (\alpha r + a) I + (\alpha \lambda_1 + \beta \lambda_1 - \beta r + a) U^1 + (\alpha \lambda_2 + \beta \lambda_2 - \beta r + a) U^2.$$

Using

$$C^w = \begin{pmatrix} S^c \\ du \end{pmatrix}$$

$$X^w = \alpha (S)^T \cdot S^c - \beta (S^c)^T \cdot S^c + dU$$

$$= -(\beta b - \beta r - d) I - (\alpha \lambda_1 + \beta \lambda_1 + \beta b - \alpha r - 2\beta r - d) U^1$$

$$-(\alpha \lambda_2 + \beta \lambda_2 + \beta b - \alpha r - 2\beta r - d) U^2.$$

The parameters α, β, a, d can be chosen to give the most desirable load sharing, efficiency and noise.

b) Bipolar

$$W = \begin{pmatrix} \alpha S - \beta^c \\ u \end{pmatrix}^T$$

$$C^r = \begin{pmatrix} S - S^c \\ au \end{pmatrix}$$

$$X^r = \alpha(S)^T \cdot S - \beta(S^c)^T \cdot S - \alpha(S)^T \cdot S^c + \beta(S^c)^T \cdot S^c + aU$$

$$= (\beta b + \alpha r - \beta r + a)I + (\beta b - \alpha r - 3\beta r + 2\alpha\lambda_1 + 2\beta\lambda_1 + a)U^1$$

$$+ (\beta b - \alpha r - 3\beta r + 2\alpha\lambda_2 + 2\beta\lambda_2 + a)U^2$$

Using $C^w = -\begin{pmatrix} S - S^c \\ du \end{pmatrix}$, the expression for X^w is obtained by replacing a by d in X^r and changing the signs of all the terms. Again α, β, a, d can be chosen as desired. Type I and type II switches are the more interesting and special cases of the general design.

This design procedure can be generalized to any partially balanced incomplete block design with m associate classes. For such a design, necessary conditions are

i) $vr = bk$

ii) $\sum_{i=1}^{m} n_i = v-1$ where n_i is the number of i^{th} associates of any object,

iii) $\sum_{i=1}^{m} n_i\lambda_i = r(k-1)$ where λ_i is the number of times i^{th} associates appear together.

For the S and S^c matrices we get the following relations.

$$(S)^T \cdot S = rI + \sum_{i=1}^{m} \lambda_i U^i$$

$$(S^c)^T \cdot S^c = (b-r)I + \sum_{i=1}^{m} (b - 2r + \lambda_i)U^i$$

$$(S)^T \cdot S^c = (S^c)^T \cdot S = \sum_{i=1}^{m} (r - \lambda_i)U^i$$

where U^i is a v-by-v matrix such that

$$u^i_{jk} = 1 \text{ if } j^{th} \text{ and } k^{th} \text{ objects are } i^{th} \text{ associates,}$$

$$= 0 \text{ otherwise.}$$

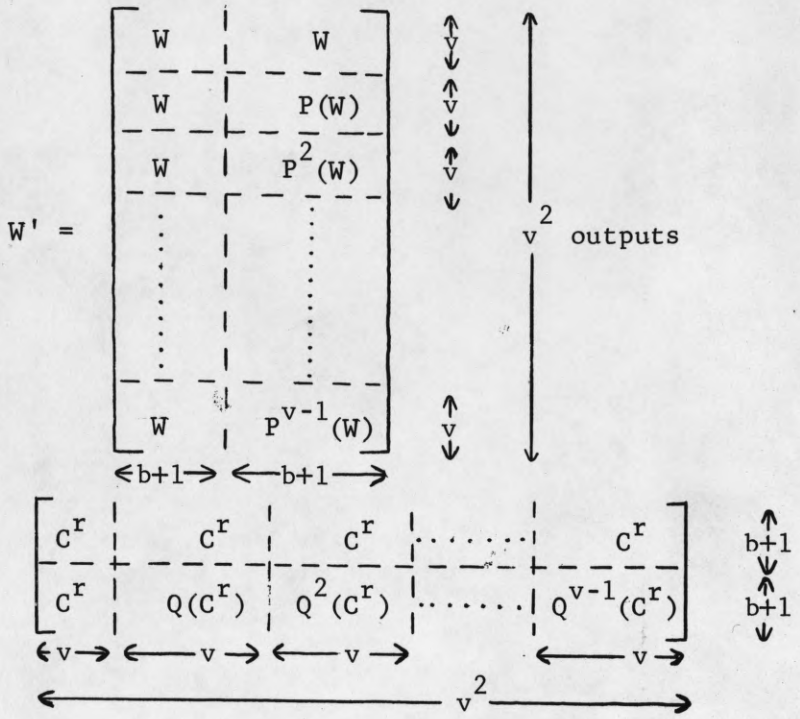
Now using the same procedure as for p.b.i.b.(2) designs, switches can be designed based on p.b.i.b.(m) designs.

3.3 A New Class of Switches

An interesting class of switches can be obtained by permuting the winding matrix of a noiseless switch in a certain manner. Let W and C^r be the winding and input matrices of a v output, b+1 input noiseless switch based on a (v,k,r,b,λ) balanced block design.

The operator P acting on any matrix A is defined as a cyclic permutation operator on the rows of the matrix. If the rows of the matrix A are $\{\alpha_1,\alpha_2,\ldots\alpha_n\}$ in that order, then the rows of P(A) are $\{\alpha_n,\alpha_1,\ldots\alpha_{n-1}\}$, the rows of $P^2(A) = P(P(A))$ are $\{\alpha_{n-1},\alpha_n,\alpha_1,\ldots\alpha_{n-2}\}$. Obviously $P^n(A) = A$. The operator Q acting on any matrix A is defined as a cyclic permutation operator on the columns of the matrix. If the columns of A are $\{\beta_1,\beta_2,\ldots\beta_m\}$ in that order, the columns of Q(A) are $\{\beta_m,\beta_1,\ldots\beta_{m-1}\}$ etc. Again $Q^m(A) = A$.

The winding matrix W' and the read input matrix $C^{r'}$ of the new switch are formed in the following manner:



If the first (b+1) inputs are excited, one row in each of the v W matrices on the left side of W' receives excitation. If the second (b+1) inputs are excited, one row in each of the v permuted W matrices in W' receives excitation. However, no two rows of W' are identical, and one and only one row of W' will receive excitation simultaneously due to both sets of (b+1) inputs. If ℓ is the load sharing factor of the original switch, the selected output will receive a total excitation of 2ℓ units. 2(v-1) other rows of W' will receive ℓ units of excitation each. If a noise excitation of ℓ units is tolerable and is insufficient to cause the switching of the unselected cores, the switch can be used as it is, otherwise a bias wire can provide negative excitation to all the cores to bring the noise excitation down to an acceptable level. The write pulse can be generated simply by a bias wire or by obtaining a $C^{W'}$ matrix from the C^{W}

matrix of the original switch, in a manner identical to obtaining the $C^{r'}$ matrix from the C^{r} matrix.

If we start with a n-by-n+1 noiseless switch based on a Hadamard matrix or a (4t-1,2t-1,2t-1,4t-1,t-1) balanced block design, the permuted switch has n^2 outputs for 2n+2 inputs. Noting that two of the inputs are bias inputs, switched on for all inputs selections, they can be combined into a single input, reducing the total number of inputs to 2n+1. This switch can be compared to a basic n^2 coincident current switch in which the cores are laid out in a n-by-n square with n horizontal drivers and n vertical drivers. Cores are selected by exciting one horizontal and one vertical driver. The selected core gets 2 units of excitation and 2(n-1) unselected cores get 1 unit of excitation. In the permuted switch, the selected core gets 2ℓ units of excitation and 2(n-1) cores get ℓ units of excitation. The basic switch therefore has a load sharing factor of 2 and the permuted switch has a load sharing factor of 2ℓ. If ℓ is large, the drivers for the permuted switch need have much smaller power output than the basic switch. Also, the permuted switch will function better than the basic square switch in the case of driver failure. If one driver fails in the basic square switch, the switch is inoperative because all the cores to which the defective driver is linked cannot be selected. In the permuted switch the failure of 1 driver will cause the excitation to decrease from 2ℓ to 2ℓ-1 units in some selected cores. If ℓ is large, the switch will continue to function.

It can easily be shown that this switch is based on a p.b.i.b.(2) design. Consider the incidence matrix S of the original (v,k,r,b,λ)

balanced block design. Then the matrix S' where

$$S' = \left[\begin{array}{c|c|c|c|c} S & S & S & \cdots\cdots & S \\ \hline S & Q(S) & Q^2(S) & \cdots\cdots & Q^{v-1}(S) \end{array}\right]$$

is the incidence matrix of a p.b.i.b.(2) design with parameters $(v',k',r',b',\lambda_1',\lambda_2',n_1',n_2')$ where

$$v' = v^2$$

$$k' = kv$$

$$r' = 2r$$

$$b' = 2b$$

$$\lambda_1' = r+\lambda$$

$$\lambda_2' = 2\lambda$$

$$n_1' = 2(v-1)$$

$$n_2' = (v-1)^2$$

For proof of this see the appendix. This p.b.i.b.(2) design yields a v^2 output 2b+1 input switch which is exactly the same as the permuted switch with winding matrix W'.

4. BLOCK DESIGNS AND ERROR CORRECTING CODES

In the following discussion it is shown how certain binary error correcting and error detecting codes can be obtained from block designs. The reader is referred to Peterson [14] for an introduction to error-correcting codes.

If S is the incidence matrix of a (v,k,r,b,λ) balanced block design, then consider the columns of S $\alpha_1, \alpha_2, \ldots \alpha_v$ to be binary code vectors of length b. The number of ones in a code vector α_i is called the weight of the vector and is denoted by $\omega(\alpha_i)$. The Hamming distance between two code words α_i and α_j is denoted by $\delta(\alpha_i, \alpha_j)$ and

$$\delta(\alpha_i, \alpha_j) = \omega(\alpha_i) + \omega(\alpha_j) - 2(\alpha_i \cdot \alpha_j)$$

where $(\alpha_i . \alpha_j)$ is the dot product of α_i and α_j and is therefore the number of positions simultaneously occupied by ones in both α_i and α_j.

For S we know that

$$(\alpha_i . \alpha_j) = \lambda \text{ for } i \neq j,$$

$$\therefore \quad \delta(\alpha_i, \alpha_j) = r+r-2\lambda = 2(r-\lambda),$$

i.e. the distance between any two code vectors is $2(r-\lambda)$. Therefore, the design leads to a code of minimum distance $2(r-\lambda)$, the code having v vectors of length b bits.

The complimentary matrix S^c is the incidence matrix of a block design with parameters $(v'=v, k'=v-k, r'=b-r, b'=b, \lambda'=b-2r+\lambda)$ and therefore

$$\delta(\beta_i, \beta_j) = (b-r) + (b-r) - 2(b-2r+\lambda)$$

$$= 2(r-\lambda)$$

where $\beta_1, \beta_2, \ldots \beta_v$ are the columns of S^c. Therefore, the complimentary

design also leads to a code of minimum distance $2(r-\lambda)$, the code having v vectors of length b.

Also, since

$$(\alpha_i \cdot \beta_i) = 0$$

and

$$(\alpha_i \cdot \beta_j) = r-\lambda$$

we have

$$\delta(\alpha_i, \beta_i) = b$$

$$\delta(\alpha_i, \beta_j) = b-2(r-\lambda).$$

If $\delta(\alpha_i, \beta_j) \geq 2(r-\lambda)$, i.e. $b \geq 4(r-\lambda)$, the columns of S and S^c form a code of 2v vectors of length b and minimum distance $2(r-\lambda)$. If $b < 4(r-\lambda)$, then the set of vectors formed by the columns of S and S^c have minimum distance $b-2(r-\lambda)$.

Example: Consider a design with parameters (4,3,3,4,2)

$$S = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 1 \end{bmatrix} \qquad S^c = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}$$

Consider the columns of S and S^c to be the code vectors.

Since

$$2(r-\lambda) = 2$$

and

$$b-2(r-\lambda) = 2,$$

the columns of S and S^c taken together give a code of 8 words of length 4 and minimum distance 2. According to the Plotkin [9] bound $A(4\ell, 2\ell) \leq 8\ell$ this is an optimal code, for no code of length 4 and minimum distance 2 can

have more than 8 code words. Since this code has minimum distance 2, it is capable of detecting all single errors. The error detection scheme in this case is very simple since all code words have weight one or three. A single error will change the weight to an even number. Therefore, a simple parity check circuit which calculates the weight of a received code word will indicate an error if the weight is even.

Other balanced block designs also lead to the optimal codes of 4ℓ bits and minimum distance 2ℓ which meet the Plotkin bound of $A(4\ell, 2\ell) \leq 8\ell$. e.g. the two complimentary designs (16,6,6,16,2) and (16,10,10,16,6) yield the same code of 32 code words, 16 bits long and minimum distance 8.

Some codes of length 4ℓ-2 bits and minimum distance 2ℓ which meet the Plotkin bound of $A(4\ell\text{-}2, 2\ell) \leq 2\ell$ are also generated by the columns of block designs. For example, the designs (4,2,3,6,1), (6,3,5,10,2), (8,4,7,14,3) and (10,5,9,18,4) all yield codes which satisfy the Plotkin bound $A(4\ell\text{-}2, 2\ell) = 2\ell$ for $\ell = 2,3,4$ and 5 respectively. As a matter of fact, all designs with parameters $(2\ell, \ell, 2\ell\text{-}1, 4\ell\text{-}2, \ell\text{-}1)$ will generate codes which meet the Plotkin bound of $A(4\ell\text{-}2, 2\ell) = 2\ell$.

In certain cases the number of code words obtained from a block design can be increased. Consider a matrix S' formed by adding a column of all ones to the incidence matrix S of a block design, i.e. $S' = (\epsilon_b^T, S)$ where ϵ_b is a row of b ones and ϵ_b^T is a column of all ones. If $\alpha_1, \alpha_2, \ldots \alpha_v$ are the columns of S

$$\delta(\epsilon_b^T, \alpha_i) = \omega(\alpha_i) + \omega(\epsilon_b^T) - 2\omega(\alpha_i)$$

$$= b\text{-}r$$

If $b-r \geq 2(r-\lambda)$ then all the columns of S' are at distance of at least $2(r-\lambda)$ from each other, and the number of code words is increased by one. The most interesting application of this is to $(4t-1,2t-1,2t-1,4t-1,t-1)$ block designs, where adding a column of all ones to S yields the $A(4t-1,2t) = 4t$ optimal codes. Bose and Shrikhande [8] have discussed the connection between Hadamard matrices, block designs and optimal codes.

We can also consider the matrix formed by adding a column of all zeros to the incidence matrix S to give a new matrix $S'' = (O_b^T, S)$ where O_b is a row of b zeros and O_b^T is a column of b zeros.

$$\delta(O_b^T, \alpha_i) = \omega(\alpha) = r$$

If $r \geq 2(r-\lambda)$, then the number of code words is increased by one.

It is, however, not possible to add both a column of zeros and a column of ones without changing the minimum distance. If the addition of a column of ones does not change the minimum distance, then $b-r \geq 2(r-\lambda)$ and if the addition of a column of zeros does not change the minimum distance then

$$r \geq 2(r-\lambda).$$

Now

$$r \geq 2(r-\lambda) \text{ implies } 2\lambda \geq r$$

and

$$b-r \geq 2(r-\lambda) \text{ implies } b \geq 3r-2\lambda.$$

For a balanced block design both these conditions cannot be simultaneously true.

Earlier it was shown that if $\alpha_1, \alpha_2, \ldots \alpha_v$ are columns of the incidence matrix S and $\beta_1, \beta_2, \ldots \beta_v$ the columns of S^c then

$$\delta(\alpha_i, \alpha_j) = 2(r-\lambda)$$

$$\delta(\beta_i, \beta_j) = 2(r-\lambda)$$

$$\delta(\alpha_i, \beta_j) = b-2(r-\lambda)$$

Suppose $b < 4(r-\lambda)$ and that $4(r-\lambda)-b = p$. Now consider the new matrix S^* and its complement S^{*c} where

$$S^* = \begin{pmatrix} U_{pxv} \\ S \end{pmatrix}$$

where U_{pxv} is a p-by-v matrix of all ones. If $\alpha_1^*, \alpha_2^*, \ldots \alpha_v^*$ are the columns of S^* and $\beta_1^*, \beta_2^*, \ldots \beta_v^*$ are the columns of S^{*c} then

$$\delta(\alpha_i^*, \alpha_j^*) = \delta(\alpha_i, \alpha_j) = 2(r-\lambda)$$

$$\delta(\beta_i^*, \beta_j^*) = \delta(\beta_i, \beta_j) = 2(r-\lambda)$$

and

$$\delta(\alpha_i^*, \beta_j^*) = \delta(\alpha_i, \beta_j)+p = 2(r-\lambda)$$

i.e. by adding p rows of ones to S, the minimum distance between columns of the new matrices S^* and S^{*c} is $2(r-\lambda)$ if $b < 4(r-\lambda)$.

The above methods of construction of codes are very general and can be applied to any block design. A particular case of this approach has been used by Bose and Shrikhande [8] in the case of (4t-1,2t-1,2t-1,4t-1,t-1) block designs. We form a matrix S^* by adding one row and one column of all ones i.e.

$$S^* = \begin{pmatrix} \epsilon_{v+1} \\ \epsilon_b^T, \; S \end{pmatrix}$$

It has been shown that if in this matrix all the zeros are changed to minus ones a 4t-by-4t Hadamard matrix is obtained. The columns of S^* and its complement form an optimal code of length 4t, minimum distance 2t and number of code words being 8t. The codes are optimal in the sense that they meet the Plotkin bound.

Error correcting and error detecting codes can also be obtained from p.b.i.b.(m) designs. The manner of construction is the same as for balanced block designs. The particular case of p.b.i.b.(2) designs is discussed in greater detail. If S is the incidence matrix of a p.b.i.b.(2) design with parameters $(v,k,r,b,\lambda_1,\lambda_2, n_1, n_2)$ with $\lambda_1 > \lambda_2$ and $\alpha_1,\alpha_2,\ldots\alpha_v$ are the columns of S then the minimum value of $\delta(\alpha_i,\alpha_j) = 2(r-\lambda_1)$. If $\beta_1,\beta_2,\ldots\beta_v$ are the columns of S^c then minimum value of $\delta(\beta_i,\beta_j) = 2(r-\lambda_1)$. Also minimum value of $\delta(\alpha_i,\beta_j) = b-2(r-\lambda_2)$. Thus the columns of S or the columns of S^c will form a code of v code words, each of length b bits and a minimum distance of $2(r-\lambda_1)$. If the columns of both S and S^c are taken together then the minimum distance is $2(r-\lambda_1)$ or $b-2(r-\lambda_2)$, whichever is smaller.

If $b-2(r-\lambda_2) < 2(r-\lambda_1)$ and

$$2(r-\lambda_1) - (b-2r+2\lambda_2) = n,$$

then as before we can add n rows of ones to the matrix S and then the columns of the new matrix and its complement will have minimum distance $2(r-\lambda_1)$. In certain cases a column of zeros or a column of ones or both can be added to S to increase the number of code words. Some interesting examples of codes from p.b.i.b.(2) designs are given below.

The block design with parameters $v=10,k=4,r=2,b=5,\lambda_1=1,\lambda_2=0, n_1=6,n_2=3$, has an incidence matrix S given by

$$S = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

The columns of S give the well known $\binom{5}{2}$ code. The columns of S^c give the $\binom{5}{3}$ code. Both codes have minimum distance 2, with 10 code words of length 5 bits. In both codes we can add a column of all zeros and a column of all ones to increase the number of code words to 12 without decreasing the minimum distance. We can also form a new matrix S^* given by

$$S^* = \begin{pmatrix} \epsilon_{11} \\ \epsilon_5^T, \; S \end{pmatrix}$$

The columns of S^* and their complements yield a code having 22 code words, each 6 bits long and a minimum distance of 2. None of the above codes are optimal since the Plotkin bounds of the relevant codes are $A(5,2) \leq 16$, and $A(6,2) \leq 32$. In certain cases optimal codes are obtained, e.g. the code obtained from the columns of S^* and S^{*c} where S^* is obtained from S by adding a column of all zeros, for the $v=15, k=9, r=6, b=10, \lambda_1=4, \lambda_2=3, n_1=6, n_2=8$, p.b.i.b.(2) design. The code obtained meets the Plotkin bound $A(10,4) \leq 32$.

APPENDIX

A Theorem for the Construction of p.b.i.b.(2) Designs From Balanced Block Designs

Let S be the incidence matrix of a (v,k,r,b,λ) balanced block design. Let $\{\beta_1,\beta_2,\ldots\beta_v\}$ be the v columns of S in that order. Each column contains r ones and no two columns of S are identical. The dot product of the two columns

$$(\beta_i.\beta_j) = r, \text{ if } i=j$$
$$= \lambda, \text{ if } i\neq j.$$

Now consider the matrix S' which consists of 2v b-by-v submatrices

$$S' = \left[\begin{array}{c|c|c|c|c} S & S & S & \cdots\cdots & S \\ \hline S & Q(S) & Q^2(S) & \cdots\cdots & Q^{v-1}(S) \end{array}\right]$$

The operator Q acting on the matrix S is defined as a cyclic permutation operator on the columns of the matrix. The columns of Q(S) are $\{\beta_2,\beta_3,\ldots \beta_v,\beta_1\}$ in that order, the columns of $Q^2(S)$ are $\{\beta_3,\beta_4,\ldots\beta_v,\beta_1,\beta_2\}$ in that order, etc. Obviously,

$$Q^v(S) = S.$$

Since no two columns of S are identical, no two columns of S' are identical. Each of the $v' = v^2$ columns of S' contains $r' = 2r$ ones and each of the $b' = 2b$ rows of S' contains $k' = kv$ ones.

Consider any column β'_s of the matrix S". Each half of β'_s is identical to some column of S. Therefore, we may write $\beta'_s = \beta_n,\beta_m$, i.e. the first half of β'_s is identical to β_n and the second half to β_m.

If

$$s = pv+q \quad 0 < q \leq v$$

then

$$n = q$$

$$m = (p+q)(\text{mod } v), \quad 1 \leq m \leq v.$$

The column β_n occurs once in each upper sub-matrix S in S' and the column β_m occurs once in each lower sub-matrix which is a permutation on the columns of S. We take the dot product of β'_s with each of the other columns of S', i.e. $(\beta'_s.\beta'_t)$ $s \neq t$ and $1 \leq t \leq v^2$. If $\beta'_t = \beta_y, \beta_z$ for some $1 \leq y, z \leq v$

$$(\beta'_s.\beta'_t) = (\beta_n.\beta_y) + (\beta_m.\beta_z).$$

Now for v-1 columns of S' $\beta_y = \beta_n$ and for v-1 columns of S' $\beta_z = \beta_m$ as t takes on the v^2-1 values of $t = 1,2,\ldots s-1,s+1,\ldots v^2$. However, it is not possible that $\beta_y = \beta_n$ and $\beta_z = \beta_m$ simultaneously for any t since that would imply $\beta'_s = \beta'_t$ for $s \neq t$.

If

$$\beta_n = \beta_y, \ (\beta_n.\beta_y) = r$$

and

$$(\beta_m.\beta_z) = \lambda \text{ since } \beta_m \neq \beta_z$$

Also if

$$\beta_m = \beta_z, \ (\beta_n.\beta_y) = \lambda \text{ since } \beta_n \neq \beta_y$$

and

$$(\beta_m.\beta_z) = r$$

Therefore if either $\beta_n = \beta_y$ or $\beta_m = \beta_z$, which is true for 2(v-1) columns of S',

$$(\beta'_s \ . \ \beta'_t) = r + \lambda.$$

For all other columns of S' $\beta_n \neq \beta_y$, $\beta_m \neq \beta_z$ and therefore $(\beta'_s \ . \beta'_t) = 2\lambda$.

It is now easily seen that S' satisfies all the conditions for being the incidence matrix of a p.b.i.b.(2) design. Let each column of S' correspond to one particular object and each row to one particular block. The s^{th} and t^{th} objects are first associates if $(\beta_s' . \beta_t') = r+\lambda = \lambda_1'$ and second associates if $(\beta_s'.\beta_t') = 2\lambda = \lambda_2'$. Each object has $n_1' = 2(v-1)$ first associates and $n_2' = (v-1)^2$ second associates. We have already seen that each column of S' has $r' = 2r$ ones and each row of S' has $k' = kv$ ones.

It is seen that the parameters $v'=v^2, k'=kv, r'=2r, b'=2b, \lambda_1'=r+\lambda, \lambda_2'=2\lambda, n_1'=2(v-1), n_2'=(v-1)^2$ satisfy the necessary conditions for a p.b.i.b.(2) design,

i) $v'r' = b'k'$,

ii) $n_1'+n_2' = v'-1$

iii) $n_1'\lambda_1' + n_2'\lambda_2' = r'(k'-1)$.

Therefore, the matrix S' is the incidence matrix of a p.b.i.b.(2) design and we state result as the following theorem:

Theorem: If S is the incidence matrix of a (v,k,r,b,λ) balanced block design, then the matrix

$$S' = \left[\begin{array}{c|c|c|c|c} S & S & S & \cdots\cdots & S \\ \hline S & Q(S) & Q^2(S) & \cdots\cdots & Q^{v-1}(S) \end{array}\right]$$

is the incidence matrix of a $(v',v',r',b',\lambda_1',\lambda_2',n_1',n_2')$ p.b.i.b.(2) design where

$v' = v^2$ $\quad$ $b' = 2b$ $\quad$ $n_1' = 2(v-1)$

$k' = kv$ $\quad$ $\lambda_1' = r+\lambda$ $\quad$ $n_2' = (v-1)^2$

$v' = 2r$ $\quad$ $\lambda_2' = 2\lambda$

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The latter part of this report is concerned with methods of obtaining error detecting and error correcting codes from block designs. Some of these codes are found to be optimal.

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There is no limitation on the length of the abstract. However, the suggested length is from 150 to 225 words.

14. KEY WORDS: Key words are technically meaningful terms or short phrases that characterize a report and may be used as index entries for cataloging the report. Key words must be selected so that no security classification is required. Identifiers, such as equipment model designation, trade name, military project code name, geographic location, may be used as key words but will be followed by an indication of technical context. The assignment of links, roles, and weights is optional.

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