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AVERAGE INTERCONNECTION LENGTH AND INTERCONNECTION DISTRIBUTION FOR RECTANGULAR ARRAYS

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Average Interconnection Length and Interconnection Distribution

for Rectangular Arrays

Abstract

In this paper we show that it is necessary to utilize different partitioning coefficients in interconnection length analyses which are based on Rent's rule, depending on whether one- or two-dimensional placement strategies are used. β is the partitioning coefficient in the power-law relationship αB^β which provides a measure of the number of interconnection that cross a boundary which encloses B blocks. The partitioning coefficients are $\beta = p/2$ and $\beta = p$ for two- and one-dimensional arrays, respectively, where p is the experimental coefficient, of the Rent relationship $T = aB^p$. Based on these separate partitioning coefficients, an average interconnection length prediction is presented for rectangular arrays that outperforms existing predictions. Examples are given to support this theory.

1. Introduction

The estimation of interconnection lengths on a chip is important for several reasons: it is a rough indicator of the chip size [1], it is a measure of the goodness of cell placement, and it allows a first cut estimate of the delay of a typical logical path on a chip [2]. Estimates of interconnection length can be made in various phases of the design process. Those estimates made in the early stages of the design should rely on a few simple parameters. As more design information becomes available additional parameters may be taken into account to refine the accuracy of the average interconnection length estimate.

The terminal-block relationship, $T=aB^p$, Rent's rule, where a and p are empirical constants and p is typically between .57 and .75 [3] has proved useful in the analysis of interconnection lengths [4-11]. The Rent relationship provides a measure of the number of interconnections which cross a given boundary which encloses B blocks. Simple first cut estimates of the average interconnection length for square arrays can be made in the early stages of a design based on two parameters, the number of cells to be placed on the chip and the empirical coefficient p of the Rent relationship [4]. However, in some instances, the average interconnection length predictions based on the Rent relationship tend to consistently overestimate the actual interconnection length for both rectangular and square arrays [4, 11].

In this paper we will consider the estimation of average interconnection lengths and the distribution of interconnection lengths in analyses based on Rent's rule. We generalize the Rent relationship to the power-law relationship, αB^β, where β is referred to as the partitioning coefficient, and investigate the use of the power-law relationship in a number of studies [4-7, 11]. Based on these investigations we determine whether there is a one-to-one correspondence between p, the empirical coefficient of the Rent relationship, and β, the partitioning coefficient of the power-law relationship. Afterwards we propose an average interconnection length estimate for rectangular arrays based on our findings.

In section 2 we consider the methodology presented by Sastry and Parker [6, 7] in describing interconnection distributions based on Rent's rule. We expand their analysis to a two-dimensional lattice model and introduce the notion of separate partitioning coefficients for one- and two-dimensional placements of logic cells. In section three we consider square arrays. To test our theory on the size of the two-dimensional partitioning coefficient we construct interconnection distributions based on the methodology

used in the derivation of a popular average interconnection length prediction method [4]. We compare our generated interconnection distributions to actual interconnection distributions and afterwards compare predicted average interconnection lengths to actual average interconnection lengths.

In section four we consider rectangular arrays. We show that a rectangular array is characterized by two partitioning coefficients, one for the two-dimensionally placed cells and one for the one-dimensionally placed cells. The concept of a top-down versus bottom-up partitioned array is introduced. An average interconnection length prediction is derived for rectangular arrays and is shown to outperform an existing prediction scheme [11]. In section five the theories presented in the paper are tested out on actual designs collected from the literature [12-17]. Section six contains the conclusions.

2. One-dimensional versus Two-dimensional Partitioning Coefficients

In this section we utilize the approach outlined by Sastry and Parker [6, 7] to characterize interconnection length distributions. Our analysis differs in that we distinguish between different placement strategies which result in one- and two-dimensional array representations. The concept of separate partitioning coefficients for one- and two-dimensional arrays is introduced.

In the analysis, a chip consists of a collection of cells. A cell may be a gate, as in a gate array, or a logic block, as in a master image design. The sample space is the set of the possible placements of a given cell on an array. In the one-dimensional model the cells are placed in a row and a row may be several cells deep. In the two-dimensional model the cells are placed in a lattice. Distances are measured in a radial fashion from an arbitrary origin. When using the lattice model Manhatten distances (horizontal and vertical directions only) are assumed. In each case a cell is considered a point source whose distance from the arbitrary origin is x. Figure 1 shows the one-dimensional row model and the two-dimensional lattice model.

Using the notation of Sastry and Parker [6, 7] let $L(x)$ denote the random variable defined on the sample space that measures the length of an interconnection from its source to the point of crossing at the boundary x. Recall that in the two-dimensional lattice model, the distances are measured in a radial fashion from the origin. Let A denote the event that an interconnection born from a gate in $(t-dt, t)$
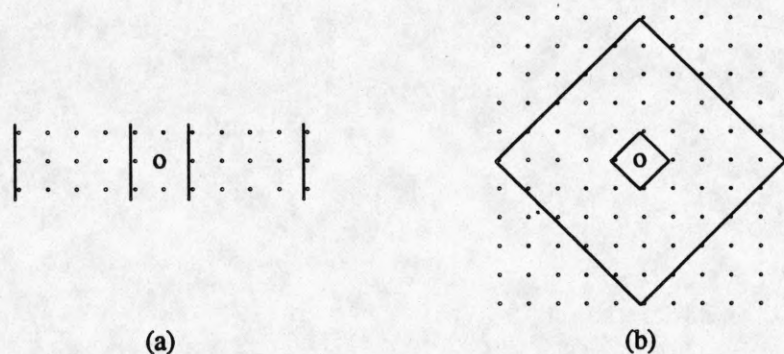
(a)   (b)

Figure 1. (a). A one-dimensional row model with a depth of three. (b). A two-dimensional lattice model. Distances $x=1$ and $x=5$ from the origin o are shown.

crosses the boundary at x:

$$A = x-t < L(x) < x-t+dt, \tag{1}$$

let B denote the event that an interconnection born before t crosses the boundary at x:

$$B = L(x) > x-t, \tag{2}$$

and let C denote the conditional probability that an interconnection crossing the boundary at x was born in $(t-dt,t)$, given that it was born before t:

$$C = A \mid B. \tag{3}$$

If $F(x)$ and $f(x)$ represent the distribution and density functions of $L(x)$, respectively, the probabilities of the three events defined above are given by

$$P(A) = f(x-t)$$

$$P(B) = 1 - F(x-t) \tag{4}$$

$$P(C) = P(A \mid B) = Z(x-t)dt = \frac{f(x-t)dt}{1-F(x-t)}$$

where $P(C) = P(A)/P(B)$ since A is a subset of B. The distribution of interconnection lengths, $F(x)$, may be found by integrating $Z(x-t)$, that is,

$$F(x) = 1 - \exp[-\int_0^x Z(x-t)dt] \tag{5}$$

where $exp(a) = e^a$. Assuming the power-law relationship αB^β yields the number of interconnections crossing any boundary x and B is the number of blocks or cells contained within the boundary, then the power-law relationship can be used to characterize $Z(x-t)$, the instantaneous number of interconnections

crossing the boundary at x.

In the one-dimensional representation of a chip the number of cells in the interval $[0, x]$ is $C(x) = 2Kx$, where K is the depth in cells of the row. Thus, using the power-law relationship it is possible to write

$$\int_0^x Z(x - t)dt = \alpha(2Kx)^\beta. \tag{6}$$

Based on Equation (6), the interconnection length distribution is

$$
\begin{aligned}
F(x) &= 1 - exp\left(-\alpha(2K)^\beta x^\beta\right) \\
&= 1 - \exp(-sx^r)
\end{aligned} \tag{7}
$$

which is a Weibull distribution function with scale parameter $s = \alpha(2K)^\beta$, location parameter 0, and shape parameter $r = \beta$.

In the two-dimensional representation of a chip, the number of cells as a function of x, where x is measured radially from the origin, is $C(x) = 2x^2 + 2x + 1$. If we approximate the number of cells in terms of distance x as $C(x) \approx 2x^2$, then, analogous to the one-dimensional case, the total number of interconnections born in $[0, x]$ which cross the boundary at x leads to

$$\int_0^x Z(x - t)\, dt = \alpha\, (2x^2)^\beta \tag{8}$$

which has the form of a Weibull distribution function with scale parameter $s = \alpha 2^\beta$, location parameter 0, and shape parameter $r = 2\beta$.

The scale parameter s and the shape parameter r of the Weibull distribution can be estimated if the interconnection distributions of a design or logic graph are available. In [6, 7] Weibull parameters were found for interconnection length statistics in the form of quantized frequencies for the three logic graphs given in [5] by using both a graphical method and the method of moments. The graphical estimation of s and r for the three logic graphs and the resulting Weibull density functions in comparison to the experimental data are shown in Figure 2.

We hypothesized that the number of interconnection emanating from a cluster of B logic cells adhered to the power-law relationship αB^β. We now consider whether the actual Rent empirical coefficients of the relationship $T = aB^p$ have a direct one-to-one correspondence with the power-law
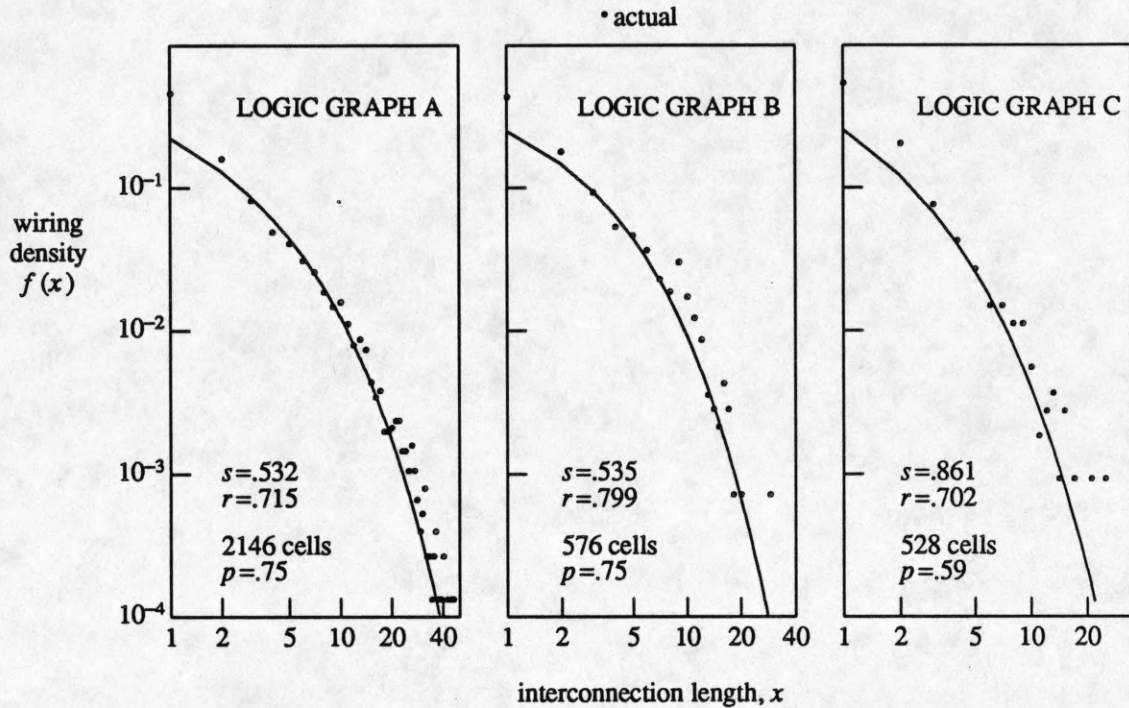
• actual

Figure 2. Weibull density functions with scale parameter s and shape parameter r for the three logic graphs in [5]. p is the experimental Rent coefficient.

coefficients. If we assume the logical graphs in Figure 2 may be represented by the two-dimensional model as is specified in [4, 5] we find for the three logic graphs the shape parameter, $r=2\beta$, does not correspond to $2p$; rather, it is closer to p, where p is the experimental Rent coefficient. This is not unexpected since Weibull density functions with a shape parameter greater than one have a bell-curve shape [18] which is contrary to observed interconnection length distributions in chip designs. Based on this evidence, we propose the following: for two- and one-dimensional placements a partitioning coefficient $\beta=p/2$ and $\beta=p$, respectively, should be used in average interconnection length prediction methods based on Rent's rule. In the remainder of this paper we provide evidence based on previous studies and actual design data collected from the literature that different partitioning coefficients should be utilized depending on whether a one- or two-dimensional placement and routing approach is followed.

3. Interconnection Distributions and Average Length for Square Arrays.

In this section we investigate the effect of using a partitioning coefficient of $\beta=p$ versus using a partitioning coefficient of $\beta=p/2$ as proposed in the previous section on a popular average interconnection length estimate for two-dimensionally placed square arrays [4]. In order to gain more insight as to why one partitioning coefficient may be better than another, we construct interconnection distributions based on the methodology used in deriving Donath's average interconnection length estimate. These interconnection distributions will be compared to previously published interconnection distributions [5]. Afterwards, comparisons of predicted average interconnection lengths are made to the logic examples in [4].

Donath's prediction of average interconnection length relies on the hierarchical nature in the placement of logic cells. The reasoning behind the estimate will be reviewed briefly. Given a logic graph of C logically interconnected nodes, the expected number of boundary terminals may be predicted using the power-law relationship αC^{β}. If we assume a logic graph consisting of C nodes is composed of groups of size N_1 nodes, then the total number of groups of size N_1 in the logic graph is C/N_1 and the total number of terminals associated with a graph of size C divided into groups of size N_1 is

$$\alpha N_1^{\beta} \, C / N_1 \,=\, \alpha N_1^{\beta-1} \, C. \tag{9}$$

If at the next level of the hierarchy, the nodes are divided into groups of size N_2, $N_2 > N_1$, then the number of terminal connections associated with interconnecting the groups of size N_1 is

$$\alpha C \, (N_1^{\beta-1} - N_2^{\beta-1}). \tag{10}$$

The number of *connections* interconnecting the groups of size N_1, $n(N_1)$, is simply some fraction f of those terminals:

$$n(N_1) \,=\, f \, \alpha C \, (N_1^{\beta-1} - N_2^{\beta-1}). \tag{11}$$

For example, for nets which connected two points, $f = 1/2$. It is assumed that the fraction f is uniform throughout all the levels of the hierarchy.

In order to hierarchically partition the logic graph, groups of 4 are used. For example, at level 0, 4 groups of size 1 are interconnected; at level 1, 4 groups of size 4 each are interconnected. Using the method of moments the average interconnection length in cell pitches, R, is given by

$$R = \frac{\sum_{l=0}^{L-1} n(4^l)\, r(4^l)}{\sum_{l=0}^{L-1} n(4^l)} \tag{12}$$

where $r(4^l)$ is the average level l interconnection length of the 4 groups of size 4^l assuming every node in each one of the groups is equally likely to be connected to every other node in the other three of four groups and $L = \log(C)/\log(4)$ is the number of hierarchical levels in the design. For the two-dimensional array model, the average level l interconnection length is

$$r(4^l) = \frac{7}{9}(2^l \hat{x} + 2^l \hat{y}) - \frac{1}{9}(2^{-l}\hat{x} + 2^{-l}\hat{y}) \tag{13}$$

where $\hat{x}$ and $\hat{y}$ correspond to the horizontal and vertical directions, respectively and the average array interconnection length, R, is [4]

$$R = \frac{2}{9}\left[7\frac{C^{\beta-1/2}-1}{4^{\beta-1/2}-1} - \frac{1-C^{\beta-3/2}}{1-4^{\beta-3/2}} \right] \tag{14}$$

for $\beta \neq .5$. Note that the average interconnection length is a function of two parameters, β and C.

In order to construct the interconnection length interconnection density, $f(x)$, based on Donath's average interconnection length prediction method, we need R in the form

$$R = \sum_{x=0}^{x=X_{max}} f(x)\, x \tag{15}$$

which is basically the expected value of $f(x)$. The average path length of four two-dimensionally placed groups of size 4^l may be expressed analytically as shown in Equation (13) or it may also be expressed as the summation

$$r(4^l) = \frac{\sum_{x=0}^{X_{max}} S_{4^l}(x)\, x}{6\, 4^l} \tag{16}$$

where $S_{4^l}(x)$ is the number of paths of length x and 6 is the number of combinations of two groups out of the four groups. We have determined $S_{4^l}(x)$ analytically. Unfortunately $S_{4^l}(x)$ is not a continuous function so a closed form solution for the interconnection density could not be found. Instead, we wrote a program which kept track of the number of interconnections of length x at each level of the hierarchy and, at the end, summed each of the contributions to find the total number of interconnection of each length x. These totals were divided by the total number of interconnections in the design to create a statistical interconnection density. Statistically calculating f(x) is a matter of solving

$$R(\beta) = \frac{\sum_{l=0}^{L-1} fC(1-4^{\beta-1})4^{l(\beta-1)}r(4^l)}{\sum_{l=0}^{L-1} fC(1-4^{\beta-1})4^{l(\beta-1)}}$$

$$= \frac{1-4^{(\beta-1)}}{1-C^{(\beta-1)}}\sum_{l=0}^{L-1}4^{l(\beta-1)}r(4^l)$$

(17)

$$= \frac{1-4^{(\beta-1)}}{6(1-C^{(\beta-1)})}\sum_{l=0}^{L-1}4^{l(\beta-2)}\sum_{x=0}^{x=X_{max}}S_l(x)x$$

$$= \sum_{x=0}^{x=X_{max}}f(x)x.$$

In Figure 3 statistically calculated interconnection frequencies based on the hierarchical partitioning of a logic graph in groups of 4 with two partitioning coefficients, $\beta=p$ and $\beta=p/2$ are plotted along with the
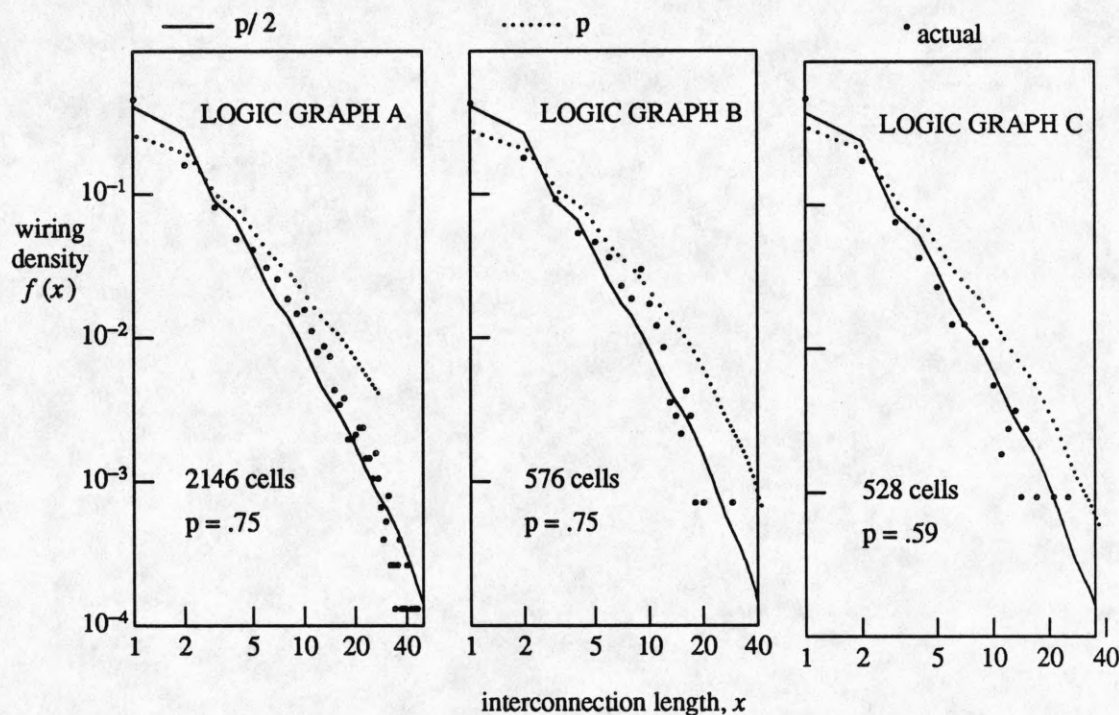

Figure 3. Comparison of interconnection density versus interconnection length: actual, statistically calculated with a partitioning coefficient $\beta=p$, and statistically calculated with a partitioning coefficient $\beta=p/2$, for the three logic graphs in [5].

actual interconnection distributions for three logic graphs. It is evident that a partitioning coefficient of $p/2$ results in a interconnection distribution which more closely resembles the actual interconnection distribution. This being the case, we should also expect that Donath's average interconnection length prediction calculated with a partitioning coefficient of $\beta=p/2$ would also result in a more accurate estimation of the average interconnection length than the originally proposed partitioning coefficient of $\beta=p$. Comparisons made on the logical designs in [4] are shown in Table 1. The average interconnection lengths predicted using a partitioning coefficient of $\beta=p/2$ are closer than those predicted using a partitioning coefficient of $\beta=p$.

4. Average Interconnection Length of Rectangular Arrays

For large designs or designs with a rectangular array, that is, an array of C_x cells by C_y cells with $C_x \neq C_y$, it is a common practice to partition the logic graph into sections, place and wire the smaller sections, and afterwards place and wire the previously wired sections [19]. For a rectangular array with substantially more rows than columns, this would involve dividing the array into several groups, each group consisting of several rows of the array and performing a two-dimensional placement and routing on these individual groups. Afterwards, a one-dimensional placement and routing of the previously wired groups would be performed. A technique used to predict the average interconnection length should take these design steps into account. In this section we develop an average interconnection length prediction for rectangular arrays which is based on partitioning an array first into two-dimensional groups and then into one-dimensional groups. The prediction relies on the proposed separate partition coefficients for one- and

Table 1. Comparison of average interconnection length of the logic designs in [4] using two different partitioning coefficients, $\beta=p$ and $\beta=p/2$, to experimental average lengths.

cells	p	R exp.	$R(p)$	R exp./$R(p)$	$R(p/2)$	R exp./$R(p/2)$
60	.67	1.29	2.76	0.47	2.23	0.58
528	.59	2.15	4.02	0.53	2.70	0.80
576	.75	2.85	5.26	0.54	3.00	0.95
671	.57	2.63	4.07	0.65	2.71	0.97
1239	.47	2.14	3.76	0.57	2.64	0.81
2148	.75	3.50	7.37	0.48	3.36	1.04

two-dimensional array placements. We compare and contrast our prediction with that of Masaki and Yamada [11].

Consider hierarchically partitioning a rectangular array. The partitioning consists of a set of subarrays where each subarray is characterized by the number of groups in the subarray, the cell size of a group, and the placement of the groups relative to one another, i.e., one- or two-dimensional placement. For example, in the previous section on square arrays, $r(4^l)$ can be characterized as a two-dimensional placement of four groups of size 4^l. One may either take a top-down or a bottom-up partitioning approach.

In a top-down partitioning approach the rectangular array is successively divided into four groups, that is, the array is initially divided into four groups and in the next step each of the groups is divided into four groups. The dividing process ends once the smaller dimension of a group is of size one. What remains is a set of 1 by k one-dimensional arrays. In a bottom-up partitioning approach, initially the array is partitioned into set of subarrays of size four and each cell is considered a group. In the next step the array is partitioned into a set of subarrays consisting of four groups of size four. This process continues until the width of the four groups is equal to the width of the array under investigation. The remaining groups are then hierarchically partitioned one-dimensionally into groups of four. The successive divisions of a 16 by 128 cell array is depicted in Table 2 for both a top-down and a bottom-up partitioning approach.

We propose using both a bottom-up partitioning approach and different partitioning coefficients depending on whether a one- or two-dimensional placement is used for predicting the average interconnection length in rectangular arrays. In the average interconnection length prediction method of Masaki and

Table 2. Bottom-up and top-down partitioning of a 16 by 128 cell array.

level	top down			bottom up		
	group size	number of groups	placement dimension	group size	number of groups	placement dimension
1	8x64	4	2D	1x1	4	2D
2	4x32	4	2D	2x2	4	2D
3	2x16	4	2D	4x4	4	2D
4	1x8	4	2D	8x8	4	2D
5	1x1	8	1D	16x16	4	1D
6				16x64	4	1D

Yamada [11] a top down partitioning approach is taken and one partitioning coefficient is used. The average interconnection in terms of two partitioning coefficients, p_1 and p_2 is

$$R(p_2, p_1) = \left[\sum_{l=0}^{L_1-1} n(l, p_1) r_1(l) + \sum_{l=0}^{L_1-1} n(l, p_2) r_2(l) \right] + \left[\sum_{l=0}^{L_1-1} n(l, p_1) + \sum_{l=0}^{L_2-1} n(l, p_2) \right] \tag{18}$$

where the subscripts 1 and 2 refer to the partitioning dimension of the array. If the array is of size C_x cells by C_y cells and $C_x \geq C_y$ then the number of levels in the two- and one-dimensional partitioning are $L_2 = \log(C_y{}^2) / \log(4)$ and $L_1 = \log(C_x/C_y) / \log(4)$, respectively.

The only term which has yet to be defined is $r_1(l)$ which is the one-dimensional average interconnection length at level l for a sub array of four groups. Consider a one-dimensional array with two groups of size w_x by w_y separated by a distance d_x as shown in Figure 4. The total path length between the two groups, which is the total length of interconnection between the two groups assuming each cell in one group is connected to each cell in the other group, is

$$PL(w_x, w_y, d_x) = \sum_{i_a=1}^{w_x} \sum_{j_a=1}^{w_y} \sum_{i_b=1}^{w_x} \sum_{j_b=1}^{w_y} \left([i_b + w_x + d_x - i_a] \hat{x} + |j_b - j_a| \hat{y} \right)$$

$$= w_x{}^2 w_y{}^2 [(w_x + d_x)\hat{x} + (\frac{w_y}{3} - \frac{1}{3 w_y})\hat{y}]. \tag{19}$$

In our application we need 4 groups in a one-dimensional row array; thus, the average path length is

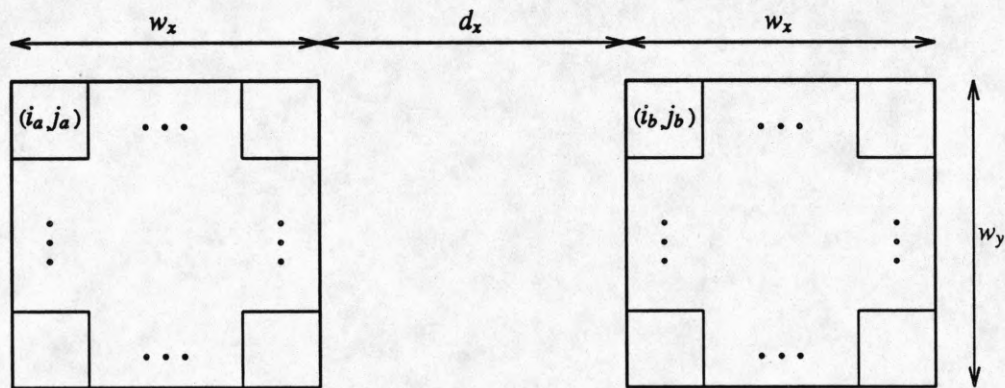Figure 4. Two groups of size w_x cells by w_y cells separated by d_x cells.

$$r_1 = [3\,PL\,(w_x,w_y,0) + 2\,PL\,(w_x,w_y,w_x) + PL\,(w_x,w_y,2w_x)]\,/\,(6w_x{}^2 w_y{}^2)$$

$$= \frac{5}{3} w_x \hat{x} + \frac{1}{3}(w_y - \frac{1}{w_y})\hat{y}. \tag{20}$$

The summation of path lengths for the one-dimensional array may now be expressed as

$$\sum_{l=0}^{L_1-1} n(l,p_1) r(l) = \sum_{l=0}^{L_1-1} \alpha f C\,[(4^l C_y{}^2)^{p_1-1} - (4^{l+1} C_y{}^2)^{p_1-1}]\,[\frac{5}{3} 4^l C_y \hat{x} + \frac{1}{3}(C_y - \frac{1}{C_y})\hat{y}] \tag{21}$$

$$= \alpha f C (1 - 4^{p_1-1})\left[C_y{}^{2p_1-1} \frac{5}{3} \frac{1 - 4^{p_1 L_1}}{1 - 4^{p_1}} \hat{x} + C_y{}^{2p_1-2} \frac{1}{3}(C_y - \frac{1}{C_y}) \frac{1 - 4^{(p_1-1)L_1}}{1 - 4^{p_1-1}} \hat{y} \right].$$

The two-dimensional path length is

$$\sum_{l=0}^{L_2-1} n(l,p_2)\,r_2(l) = \alpha f C (1 - 4^{p_2-1}) \frac{1}{9}\left[7 \frac{4^{(p_2-\frac{1}{2})L_2} - 1}{4^{(p_2-\frac{1}{2})} - 1} - \frac{1 - 4^{(p_2-\frac{3}{2})L_2}}{1 - 4^{(p_2-\frac{3}{2})}} \right] (\hat{x} + \hat{y}). \tag{22}$$

The total number of connections in the rectangular array is

$$\sum_{l=0}^{L_1-1} n(l,p_1) + \sum_{l=0}^{L_2-1} n(l,p_2) = \alpha f C\,(1 - C_y{}^{p_2-1} + C_y{}^{2(p_1-1)} - C^{p_1-1}). \tag{23}$$

The average interconnection length may be found by substituting Equations (21), (22), and (23) into Equation (18). Note that the resulting average interconnection length equation does not depend on αf.

The effect of the differing partitioning coefficients on the interconnection density is shown in Figure 5 for the rectangular array of size 71.31 cells by 20 cells, Part D.3 [11], along with the resulting average interconnection length predictions and the actual average interconnection length. In this example our proposed partitioning coefficients of $\beta = p/2$ for the two-dimensional partitioning and $\beta = p$ for the one-dimensional partitioning more closely predicts the average interconnection length. Note that the slight differences in the three density functions do make significant differences in the final outcome of the average interconnection length.

The remaining examples from [11] are shown in Table 3. $R_{Mas}(\beta)$ is the average interconnection length predicted using the formulas of Masaki and Yamada and $R(\beta_2,\beta_1)$ is our proposed average interconnection length prediction. For the square array examples (Part B) the partitioning coefficient of $\beta = p/2$ provides a better prediction of the average interconnection length as was also shown in the examples in section 2. For part D, two of Masaki and Yamada's predictions are fairly close while one is far off, and for our predictions one is very close and two are far off. Looking more closely we find that although all three
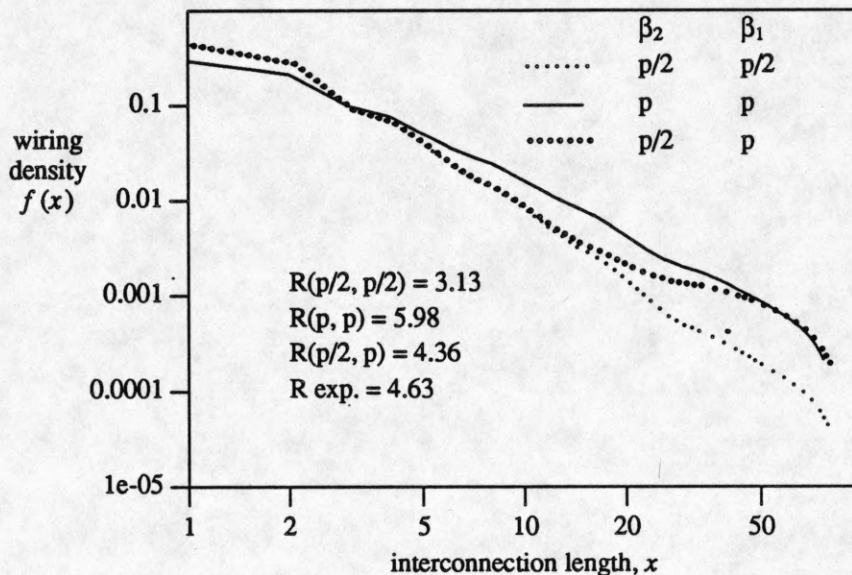
Figure 5. Interconnection densities for the bottom-up partitioning of rectangular array of size 71.31 cells by 20 cells, part D.3 [11], using three combinations of partitioning coefficients.

Table 3. Comparison of average interconnection length with two different partitioning coefficient, $\beta=p$ and $\beta=p/2$, and experimental average interconnection lengths. A Rent coefficient of $p=.666$ is used in all examples.

example	array size	R exp	$R_{Mas}(p)$	R exp/$R_{Mas}(p)$	$R(p/2,p)$	R exp/$R(p/2,p)$
A.1	7.29x10.01	1.998	2.908	0.687	2.391	0.836
A.2	7.53x10.35	2.270	2.955	0.768	2.414	0.940
A.3	7.24x9.95	1.877	2.899	0.648	2.386	0.787
B.1	15.88x15.88	2.736	3.840	0.713	2.637	1.038
B.2	15.36x15.36	2.198	3.784	0.581	2.619	0.839
B.3	15.39x15.39	2.887	3.788	0.762	2.620	1.102
C.1	6.54x8.41	1.579	2.707	0.583	2.271	0.695
C.2	6.77x8.71	1.384	2.754	0.502	2.296	0.603
C.3	6.95x8.93	2.077	2.787	0.745	2.313	0.898
D.1	86.22x20.00	6.159	7.341	0.839	4.704	1.309
D.2	74.34x20.00	6.475	6.821	0.949	4.430	1.462
D.3	71.31x20.00	4.634	6.686	0.693	4.358	1.063

arrays are roughly the same size one average interconnection length is far below the others (4.63 versus 6.16 and 6.48). Assuming these are random placements, we contend that the placement with the lowest average interconnection length represents a very good placement while the other two are not nearly as

good. All in all, our average interconnection method seems to more closely predict the average interconnection length of a rectangular array.

5. Comparison to Actual Designs

In this section we compare our average interconnection length prediction formulas to the average interconnection length prediction of Masaki and Yamada [11] for a series of published designs [12-17]. We consider what type of designs the prediction methods do well on.

It is a common occurrence in logical designs that the entire array is not completely populated with cells. Given an internal array of a chip (not including I/O cells) of size A_x cells by A_y cells with U percent of the cells of the array utilized in a design, then we can approximate the number of cells utilized in each direction as

$$
\begin{aligned}
C_x &= A_x \sqrt{U} \\
C_y &= A_y \sqrt{U}.
\end{aligned}
\tag{24}
$$

For example, in [15] the array is 26 cells by 32 cells and 90% of the cells are utilized; therefore, C_x=24.67 and C_y=30.36. If a utilization is not specified for a design, a utilization of 80% is assumed, although any utilization may be assumed. The utilized cells in each direction and the partitioning coefficients are the parameters of the interconnection length predictions.

The results of the interconnection length prediction formulas are expressed in cell pitches in the x and y directions, R_x and R_y, respectively. To convert this to the average interconnection length in metric units, the cell dimensions need to be determined. In our analysis we assume 85% of a chip dimension is allocated to the wiring of the internal cells; the remaining 15% is allocated to the I/O circuitry. Thus, given a chip of size D_x=7mm by D_y=8mm, the internal wiring dimensions are I_x=5.95mm and I_y=6.80mm. The cell sizes in the x and y directions, S_x and S_y are

$$
\begin{aligned}
S_x &= I_x / C_x \\
S_y &= I_y / C_y
\end{aligned}
\tag{25}
$$

and the average interconnection length, L, is

$$
L = R_x S_x + R_y S_y.
\tag{26}
$$

If the actual wiring statistics are specified in terms of net lengths, then the interconnection length is found

by dividing the net length by the average fanout in the design. If one is not given, a fanout of 2.5 is assumed.

When comparing average interconnection predictions in metric units, L, we will consider a range of Rent coefficients bounded by $p=.666$ and $p=.750$. Since our average length prediction for rectangular arrays, $L(\beta_2,\beta_1)$, relies on separate partitioning coefficients, $\beta_2=p/2$ and $\beta_1=p$, for the two- and one-dimensional placements, respectively, we will compare our prediction to Masaki and Yamada's, $L_{Mas}(\beta)$, using two partitioning coefficients, $\beta=p$ and $\beta=p/2$. The characteristics of the six designs we will consider are given in Table 4. In Figure 6 the actual and predicted interconnection lengths in metric units are compared for the designs in Table 4.

A number of comments are in order. For designs C and D, $C_x \approx C_y$; therefore, our prediction, $L(\beta/2,\beta)$ is similar to $L_{Mas}(p/2)$ and provides an accurate prediction of the actual length. In design B, a rectangular array with C_x roughly twice C_y, $L(p/2,p)$ again most closely predicts the actual interconnection length. Meanwhile, $L_{Mas}(p/2)$ underestimates the length while $L_{Mas}(p)$ overestimates the length. Design A is interesting because this time $L_{Mas}(p)$ also underestimates the actual length. This is attributed to the top-down partitioning which results in a large number of short interconnections.

The average interconnection length formula $L(p/2,p)$ predicted the average lengths of the four designs, A, B, C, and D, quite well. These designs were all automatically placed and wired and were also more or less random. This random aspect even holds true for designs B and C which are multipliers because when viewing the photomicrograph of the chips [13, 14], the cells seem to be more or less uniformly distributed on the chip. In contrast, we consider two design examples, E and F, which tend to have

Table 4. Characteristics of Six Designs Used to Calculating Average Interconnection Length.

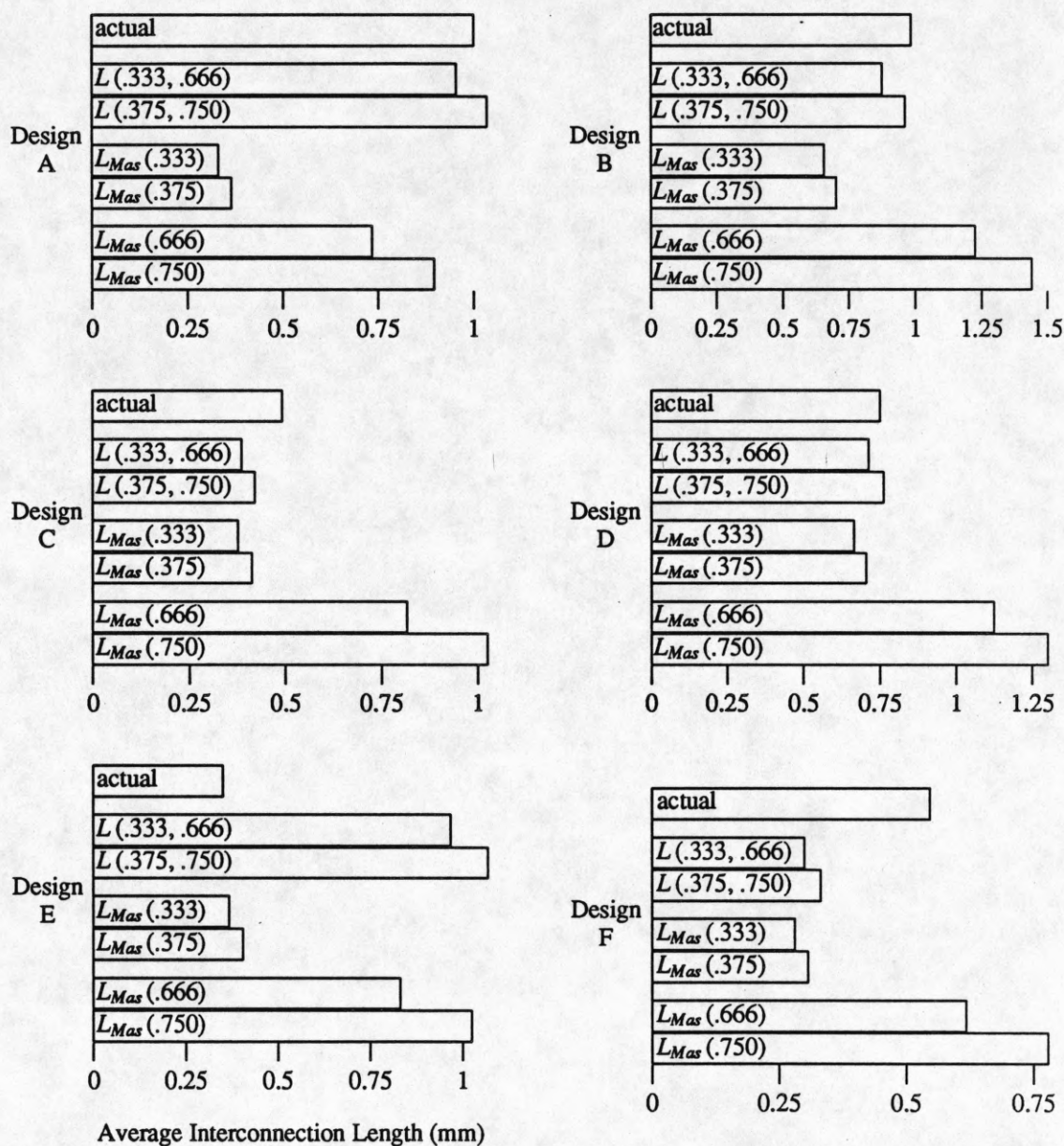| Design	ref.	C_x	C_y	U	$D_x(mm)$	$D_y(mm)$
A	[12]	133	12	.80	6.5	6.5
B	[13]	68	32	.53	9.4	9.2
C	[14]	72	68	.92	9.0	9.2
D	[15]	32	26	.90	7.6	7.3
E	[16]	239	27	.52	7.8	7.8
F	[17]	80	92	.65	7.0	7.0

Figure 6. Actual interconnection lengths and predicted average interconnection lengths of the designs characterized in Table 4, for a range of Rent experimental coefficients bounded by $p=.666$ and $p=.750$.

a more structured layout on the chip. Design E is a 16 bit by 16 bit multiplier and Design F is a micropro-cessor. The predicted average interconnection length for design E is much greater than the actual average interconnection length. A photograph of the fabricated chip which contains Design E [16] gives a clue as

to why this occurred. The layout of the chip is highly structured and occupies less than 75% of the array area. It is possible to modify the internal cell area in the calculations to that which is actually utilized in the design. This would result in smaller cell sizes and, therefore, shorter average interconnection lengths predicted. The prediction for the average interconnection length of design F underestimates the actual average interconnection length. This is because the microprocessor contains a large number of busses and does not truly qualify as a random design. In short, our proposed average interconnection prediction method works best on random logic designs which are more or less uniformly distributed on the cell array.

6. Conclusions

In this paper we proposed the general power-law relationship αB^{β} to provide an estimate of the number of interconnections crossing a boundary which encloses B blocks or cells rather than the typically utilized Rent relationship aB^p. We have shown that it is necessary to utilize different partitioning coefficients, β, in average interconnection length prediction formulas and interconnection density formulas which are based on Rent's rule, depending on whether a one-dimensional or two-dimensional placement strategy is used. The partitioning coefficient is $\beta=p/2$ and $\beta=p$ for two- and one-dimensional arrays, respectively, where p is the experimental Rent coefficient. Based on these finding an average interconnection length estimate is presented for rectangular arrays which outperforms other existing estimates.

7. References

[1]   R. W. Keyes, "The Wire-Limited Logic Chip," *IEEE Journal of Solid-State Circuits*, vol. SC-17, pp. 1232-1233, December 1982.

[2]   A. K. Sinha, J. A. Cooper, Jr., and H. J. Levinstein, "Speed Limitations Due to Interconnect Time Constants in VLSI Integrated Circuits," *IEEE Electron Device Letters*, vol. EDL-3, pp. 90-92, April 1982.

[3]   B. Landman and R. Russo, "On a Pin Versus Block Relationship For Partitions of Logic Graphs," *IEEE Transactions on Computers*, vol. C-20, pp. 1469-1479, December 1971.

[4]   W. Donath, "Placement and Average Interconnection Lengths of Computer Logic," *IEEE Transactions Circuits and Systems*, vol. CAS-26, pp. 272-277, April 1979.

[5]   W. Donath, "Wire Length Distribution for Placement of Computer Logic," *IBM Journal of Research and Development*, vol. 25, pp. 152-155, May 1981.

[6]   S. Sastry and A. C. Parker, "Stochastic Models for Wireability Analysis of Gate Arrays," *IEEE Transactions on Computer-Aided Design*, vol. CAD-5(1), pp. 52-65, January 1986.

[7] S. Sastry and A. Parker, "On the Relation between Wire Length Distribution and the Placement of Logic on Master Slice ICs," *21st Design Automation Conference*, pp. 710-711, 1984.

[8] M. Feuer, "Connectivity of Random Logic," *IEEE Transactions on Computers*, vol. C-31, pp. 29-33, January 1982.

[9] D. Ferry, "Interconnection Lengths and VLSI," *IEEE Circuits and Devices Magazine*, pp. 39-42, July 1985.

[10] D. Schmidt, "Circuit Pack Parameter Estimation Using Rent's Rule," *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, vol. CAD-1, pp. 186-192, October 1982.

[11] A. Masaki and M. Yamada, "Equations for Estimating Wire Length in Various Types of 2-D and 3-D System Packaging Structures," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. CHMT-10(2), pp. 190-198, June 1987.

[12] Y. Nishio, T. Hayashi, and S. Torii, "CMOS Gate Array," *Hitachi Review*, vol. 31(5), pp. 241-244, 1982.

[13] T. Takahashi, H. Nakashiba, T. Nakamura, and K. Kimura, "A High Speed 16-Bit Expandable Multiplier using 5000 Gate ECL Gate Array," *IEEE International Conference on Computer Design: VLSI in Computers*, pp. 264-267, 1983.

[14] M. Suzuki, S. Horiguchi, and T. Sudo, "A 5K-Gate Bipolar Masterslice LSI with a 500ps Loaded Gate Delay," *IEEE Journal of Solid State Circuits*, vol. SC-18(5), pp. 585-592, October 1983.

[15] Y. Ohuchi, M. Sano, F. Sato, H. Nakashiba, M. Nakamae, H. Shiraki, and N. Yoshimura, "Sub-picojoule Bipolar LSI with a 350ps gate delay and 2000 Gates," *IEEE International Conference on Computer Design: VLSI in Computers*, pp. 97-100, 1983.

[16] H. Tago, T. Kobayashi, M. Kobayashi, T. Moriya, and S. Yamamoto, "A 6K-Gate CMOS Gate Array," *IEEE Journal of Solid-State Circuits*, vol. SC-17(5), pp. 907-912, October 1982.

[17] A. H. Dansky, "Bipolar Circuit Design for a 5000-Circuit VLSI Gate Array," *IBM Journal of Research and Development*, vol. 25(3), pp. 116-125, May 1981.

[18] A. Kaufmann, D. Grouchko, and R. Cruon, *Mathematical Models for the Study of the Reliability of Systems*. New York: Academic Press, Inc., 1977.

[19] K. Klein, G. Koetzle, E. Miersch, H. Schettler, U. Schulz, and O. Wagner, "Characteristics of a Set of 12.7-mm Processor Chips," *IEEE Journal of Solid-State Circuits*, vol. SC-22(5), pp. 783-789, October 1987.